POWER9 Processor Registers Specification

Volume 2

Advance

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Revision Log

Each release of this document supersedes all previously released versions. The revision log lists all significant changes made to the document since its initial release.

Version	Revision Date	Description
1.2	31 March 2017	Updated Section 8 PCI0 Chiplet. Updated Section 9 PCI0 Chiplet PCB Slave. Added Section 10 PCI1 and PCI 2 Chiplet.
1.1	31 January 2017	Updated the Terminology and the Overview. No substantive changes to the register descriptions.
1.0	30 August 2016	Initial release.

About this Document

This document describes the registers used by the IBM® POWER9 processor. To ensure you have the most current version of this document, visit the OpenPOWER Connect website.

Who Should Read this Document

This document is intended for system software and hardware developers and application programmers who are developing products that use the POWER9 registers. It is assumed that the reader understands operating systems, microprocessor system design, basic principles of reduced instruction set computer (RISC) processing, and details of the Power Instruction Set Architecture (ISA).

Organization

This document is divided into three volumes, of approximately equal sizes, organized by address ranges.

Volume	Address Range	Contents
1	0x0000_0000 - 0x050F_FFFF	Chip logic registers Processor bus registers
2	0x0600_0000 - 0x200F_FFFF	X bus chiplet registers[1] OB chiplet registers[1] PCI registers Cache and core registers
3	0x0700_0000 - 0x070F_FFFF	Memory controller registers[1]

1. These registers use indirect addresses in the range 0x8000_0000_0000_0000 - 0x8000_0000_0901143F.

In each volume, the table of contents lists the primary divisions in the document. Address maps at the beginning of each chapter list the registers in each chiplet in alphabetical order by mnemonic. Within each chapter, the registers themselves are arranged by their addresses. A register can have multiple addresses with different addresses for different chiplets.

Bit Significance

In the POWER9 documentation, the smallest bit number represents the most significant bit of a field, and the largest bit number represents the least significant bit of a field.

Representation of Numbers

Numbers are generally shown in decimal format, unless otherwise designated. One of the following conventions is used to indicate the numeral system, where "nn" or "NN" indicates the numerical value:

- Binary values are represented as 0bn, `nn'b, or `n'.
  Examples: 0b01, `01'b, or `01'
- Decimal values are represented as nn or `nn'd.
  Examples: 1 or `1'd
- Hexadecimal values are represented as 0xN, x`N', or `NN'h.
  Examples: 0x000000000204000D, x`000000000204000D', or `000000000204000D'h

Note: A bit value that is immaterial, which is called a “don't care” bit, is represented by an “X” or "x."

Representation of Enumerated Registers

To succinctly describe registers that are identical except for a numeral in the register name and mnemonic, a syntax is used that enables these “enumerated registers” to be described in a single register table.

The registers in the DP16 section are enumerated because there are five instances of the DP16 unit for each DDR PHY port. All five instances are required for each DDR PHY port, and, at the chip level, there are eight DDR PHY ports. Each DDR PHY unit is self-contained and comprises four independent ports that connect to DIMM slots. This unit is replicated twice on the POWER9 system to provide a maximum of eight ports. All of the DP16 registers are documented in one replication. The address is the only difference between the two. The first replication is on 0x0000_0000_0700_0000, and the second replication is on 0x0000_0000_0800_0000.

For example: **IOM0**.DDRPHY_DP16_DATA_BIT_ENABLE0_P0_[n]
800000000**7**01103F (SCOM), +0x0400_0000_0000

IOM1.DDRPHY_DP16_DATA_BIT_ENABLE0_P0_[n]
800000000**8**01103F (SCOM), +0x0400_0000_0000

Register Names

The following syntax is used for enumerated register names:

<register name> [n] (n = m:p) where m and p are integers

For example: TWG Control Register [n] (n = 0:15)

Mnemonic

The following syntax is used for enumerated mnemonics:

<mnemonic>_[n], where n is an integer from the enumerated register name

For example: REG_TWGDATA_[n]
REG[n]_TWGDATA

Address Offset

The following syntax is used for enumerated address offsets so that enumerated registers can be described in a single register table. The stride defines the hexadecimal integer to add to the address for each enumeration.

<address_offset>, +<stride>

For example: 0x80030, +0x10

Register Name	DP16 DQ Enable 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQ_BIT_ENABLE0_P0_[n]
Address	800000000701103F (SCOM), +0x0400_0000_0000
Description	A DP16 has 24 possible single-ended data pins that can send or receive data. This register is used to enable and disable each of the 24 pins for data sending or receiving. Any pins on the DP16 that are used as strobes or clocks to capture the data must not be marked as enabled in this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	DATA_BIT_ENABLE_0_15: 1b = Indicates that the DP16 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. 0b = Indicates that the DP16 bit is not used to send or receive data. Bit 48 controls MEMINTD00B(n). Bit 49 controls MEMINTD01B(n). Bit 50 controls MEMINTD02B(n). ... Bit 63 controls MEMINTD15B(n). where n is the DP16 instance number.

Related Documents

The following documents can be helpful when reading this specification. They are available through OpenPOWER Connect or Power.org.

POWER9 Processor User's Manual
POWER9 Processor Datasheets
Power ISA User Instruction Set Architecture - Book I (Version 3.0)
Power ISA Virtual Environment Architecture - Book II (Version 3.0)
Power ISA Operating Environment Architecture (Server Environment) - Book III-S (Version 3.0)

Terminolgy

The following terms are used in volumes 1, 2, or 3 of the *POWER9 Processor Registers Specification*.

Note: Acronyms are not typically expanded in the body of this document.

3DS	Three-dimensional stacking
AADR	Array Access Data Register
AAER	Array Access ECC Register
ABIST	Array built-in self test
ABIST/IOBIST	Array built-in self test / input/output built-in self test
ABUS	**Note:** This is not really an acronym but a name (A bus).
AC	Alternating current
ACK	Acknowledgment or acknowledge. A transmission that is sent as an affirmative response to a data transmission.
ACT	Activate
ACT#	Activate (inverted)
ADC	APSS with analog-to-digital converter
ADDR	Address
ADR	Address
ADU	Alter-display unit
AES	Advanced Encryption Standard
AFSR	Average Frequency Sample Register
AFTR	Average Frequency Threshold Register
AIB	1. ASIC interconnect bus 2. ASIC interface bus
AL	Additive latency. For more information, see the JEDEC DDR3 and DDR4 DRAM specifications.
AMF	Availability management framework
AMux	Analog multiplexer
ANA16	Analog 16 bits
AND write	Current register content is ANDed with write data and the result is stored in the register (access type WO_AND / WOX_AND).
AP	Auto-predischarge. For more information, see the JEDEC DDR3 and DDR4 DRAM specifications.
APB	Advanced peripheral bus
APIN	ADR pin. The logic macro inside DDR units for sending data to the ADR bus.
APSS	Analog power subsystem sweep. Provides real-time power measurements of voltage rails.
ARB	Architecture Review Board
ARE	Address error
ARY	Array
ASB	Advanced system bus

ASBE	Array single-bit error
ASIC	Application-specific integrated circuit
AT	Address translation
ATEST	Analog test pin
ATPG	Advanced test pattern generator
AUE	Array uncorrectable error (UE)
AVP	Architectural verification program. A custom payload used to test a processor or other host hardware or software function.
AVS	Adaptive voltage scaling
Âµ	Micron
Âµs	Microsecond
B	Byte
BA	Bank address
BAR	Base Address Register
BCDE	Block copy download engine
BCE	Block copy engine
BCEBAR	Block Copy Engine Base Address Register
BCECSR	Block Copy Engine Control and Status Register
BCUE	Block copy upload engine
BCW	Buffer control word
BDF	Bus device function
BE	1. Big-endian 2. Branch Trace Enable bit in the MSR (MSRBE) 3. Byte enable
BER	Bit error rate
BG	Bank group
BI	Burn in
BIST	Built-in self test
BL	Bit length
BL8	Burst length 8
BNDY	Boundary I/Os
BSC	Boundary scan cells
BW	Bandwidth
BYPASSN	Bypass low active
c_err_rpt	Common lib error report
CACCR	Core Analog Clock Control Register

CACSR	Core Analog Clocking Status Register
CAL	Calibration
CAM	Content-addressable memory
CAPI	Coherent Accelerator Processor Interface
CAPP	Coherent accelerator processor proxy
CAS	Column-address select
CASN	Column-address select (inverted)
CAW2	An internal pipeline stage designator
CBS	CFAM boot sequencer
CC	1. Clock controller 2. Congruence class
CCB	Change control board
CCFG	Clock control configuration
CCS	Configured command sequencer
CD	Compact disc
CDIMM	Custom dual in-line memory module
CDR	Clock and data recovery
CE	Correctable error. A hardware error that the firmware detects and corrects without impacting the state of the system.
CERR	Common lib error report
CFAM	Common field-replaceable unit (FRU) access macro
CFIR	Chiplet Fault Isolation Register
CGC	Congruence class
checkstop	A severe error inside a processor core that causes a processor core to stop all processing activities. This is the same as a system crash. The operating system is not functional.
chip select	A signal that selects one or more memory modules to respond to a command/address. An exact one-to-one correspondence exists between chip selects and ranks.
CI	1. Cache-inhibited 2. Cast-in
CID	Completer ID. When returning the completion for a transaction, the completer attaches its Bus/Dev/Func to the transaction as a CID. See also RID.
CIDSR	Core IVRM Dropout Sample Register
CK	Clock
CK#	Clock (inverted)
CKE	Clock enable
CKSW	Chicken switch: A programmable mode bit that disables a certain function or changes its behavior.

CL	Column-address select (CAS) latency
CLK	Clock
CMD, cmd	Command
CME	Core management engine
CMOS	Complementary metal-oxide semiconductor
CMSK	Logical built-in self test (LBIST) channel mask
CO	Cast-out
CP	Chip pump
CPB	Coprocessor parameter block
CPI	Cycles per instruction
CPLT	Chiplet
CPLT_CTRL	Chiplet control
CPM	Critical path monitor
CPPM	Core PCB-slave power management macro (PPM)
CPS	Cycle-per-step
CQ	1. Common queue. Refers to the interface to the SMP interconnect. 2. Completion queue
CRC	Cyclic redundancy check
CRESP	Combined response
CS	Chip select
CSID	Chip select ID
CSN	Chip select (inverted)
CTL	Control
CTLE	1. Continuous time linear equalization 2. Continuous time linear equalizer
CTRL	Control
D/A	Display/alter
DAC	Digital-to-analog converter
DACTEST	DAC test
DBG	Debug
DBSR	Debug Status Register
DC	Direct current
DCACHE	Data cache
DCBZ	Data cache block set to zero
DCD	Duty cycle distortion

DCM	Dual-chip module
DCTEST	This is a mode where test operations are executed at very low frequencies.
DDR	Double data rate
DDR3	Double data rate type three
DDR4	Double data rate type four
DDRPHY	Double data rate physical interface
DEC	Decrementer
DERR	Distributed elastic round robin
DFE	1. Decision feedback equalization 2. Decision feedback equalizer
DFI	DDR PHY interface bus
DFT	Design for test
DGEN	Data pattern generator
diag	Diagnostic
DIMM	Dual in-line memory module. A small circuit board with memory-integrated circuits containing signal and power pins on both sides of the board.
DIN	Data in
DL	Downlink
DLDCH	Downlink data channel
DLL	1. Delay-locked loop 2. Dynamic link library
DLL/VREG	Delay-locked loop/voltage regulator
DLL/ZCAL	Delay-locked loop/impedance (Z) calibrator
DMA	1. Direct memory access. A technique for using a special-purpose controller to generate the source and destination addresses for a memory or I/O transfer. 2. Direct memory attach
DP16	Data path 16
DPC	DIMMs per port
DPLL	Digital phase-locked loop
DPLLFREQ	DPLL frequency control
DQ	1. Data 2. Data bit
DQS	Data strobe
DQSCLK	Data strobe clock
DR	1. Data Relocate bit in MSR (MSRDR) 2. Dynamic reconfiguration. The capability of a system to adapt to changes in the hardware/firmware physical or logical configuration, and to be able to use the new configuration, all without having to turn the platform power off or restart the operating system. See the *Power Architecture Platform Requirements (PAPR)* document for more information.

DRAM	Dynamic random-access memory. Storage in which the cells require repetitive application of control signals to retain stored data.
DRTM	Dynamic root of trust for measurement
DSI	Data storage interrupt.
DSM	Digital state machine
DSMP	Distributed symmetric multiprocessing
DTS	Digital thermal sensor
EA	Effective address. An address generated or used by a program to reference memory. A memory-management unit translates an EA to a virtual address (VA), which it then translates to a real address (RA) that accesses real (physical) memory. The maximum size of the effective-address space is 264 bytes.
EAT	1. Effective address translation 2. Event assignment table
ECC	See error correction code
EDAT	Even data
EDI	Elastic differential interface. A bus that consists of high-speed differential I/O links. The memory bus instance of an EDI bus is a “DMI bus,” and the off-module, fabric bus (between processors) instance of an EDI bus is an “A bus.”
EDR	Error Data Register
eDRAM	Embedded dynamic random access memory
EH	Exclusive access hint
EICR	Error Inject Control Register
EIIR	External Interrupt Injection Register
EIMR	External Interrupt Mask Register
EINR	External Interrupt Input Register
EIPR	External Interrupt Polarity Register
EISR	External Interrupt Status Register
EITR	External Interrupt Type Register
ELPR	Error Log Pointer Register
EM	Electron migration
EMC	Extended memory controller
ENOP	End sync/wait step; no operation
EOT	End of transfer
EPS	1. Entry-level power supply 2. Pervasive end points
EQ	Event queue
ERAT	Effective-to-real-address translation, or a buffer or table that contains such translations, or a table entry that contains such a translation.
ERR	Error

error correction code	A code appended to a data block that can detect and correct bit errors within the block.
ERRSUM	Error summary
ERS	Early read start
ETE	Error threshold exceeded
ETU	Express transaction unit
EXT	JTAG EXTEST instruction mode
FARB	Final arbiter. Part of the memory interface command sequencer (scheduler).
FARR	Fast array unload
FBC	Fabric bus connection
FET	Field-effect transistor
FFDC	First failure data capture. A collection of data used upon fail to analyze the root cause of the failure.
FIFO	First in, first out. Refers to one way elements in a queue are processed. It is analogous to “people standing in line.”
FIR	Fault Isolation Register. Register bits that show which piece of hardware failed.
FMAX, fmax	Maximum frequency
FMIN, fmin	Minimum frequency
FMULT	Frequency multiplier
FPGA	Field-programmable gate array
FSAFE	Safe frequency
FSI	1. Flexible service interface. The FSI covers all resources, except FSI slave 0 and slave 1, when addressed from an external service element via the FSI. 2. FRU support interface
FSI2PIB	FRU support/service interface to the pervasive interconnect bus
FSM	Finite state machine
FSP	Flexible service processor. An embedded controller for internal system control tasks in IBM Power Systems™. In addition to the processor core, the following I/O interfaces are integrated into the embedded controller: I²C, JTAG, UART, GPIO, FSI.
FUNC	Functional
FW	Firmware
FWMR	Firmware Mode Register
Gbps	Gigabits per second
GCR	Global control ring
glsmux	Glitchless multiplexer
GND	Ground
GPE	General-purpose engine

GPIO	General-purpose input/output
GPO	Global PHY offset
GPR	General Purpose Register
GPTR	General Purpose Test Register
GZIP	A file format used for file compression and decompression.
H/W	Hardware
HCA	1. Host channel adapter 2. Hot/cold affinity
HID	Hardware implementation dependent
HIRES	High resolution
HLD	High-level design
HMER	Hypervisor Maintenance Exception Register
HMI	Hypervisor maintenance interrupt
HP	High performance
HPC	High-performance computing
HSS	High-speed serial
HTB	Hierarchical test block
HTML	Hypertext Markup Language
HW	Hardware
HWCTRL	Hardware control
HYP	Hypervisor
I/O	Input/output
IAR	Instruction Address Register
IAUE	Intermittent array uncorrectable error
IC	Integrated circuit
ICACHE	Instruction cache
ICE	Intermittent chip error
ICP	Interrupt control presenter
ICRR	Inter-CME Communication Receive Register
ICS	Interrupt controller source
ICSW	Initiate coprocessor store word
ID	Identification
IDCR	IVRM Dropout Configuration Register
IE	Input enable
IEEE	Institute of Electrical and Electronics Engineers

IF	Interface
IFU	Instruction fetch unit
IMA	In-memory accumulate
IMA/PPE/HTM	In-memory accumulate/Power PC® element/hardware trace macro
IMPE	Intermittent mark placed error (MPE)
INIT	Initialization
INOP	Initial sync/wait step; no operation
INT	INTEST instruction support. The INTEST instruction can be triggered through JTAG or through register control.
INTP	Interrupt presenter
INV	JTAG enable inversion macro
IO or I/O	Input/output
IOBIST	Input/output built-in self test
IOOPPE	PPE used for control of I/O macros
IOP	1. I/O processor 2. Internal operation
IOTK	I/O toolkit
IP	1. Interrupt Prefix bit in MSR (MSRIP) 2. Internet protocol
IPL	1. Initial program load. The time between when power is applied to the platform hardware and when the payload is fully functional. 2. Interrupt presenter layer
IPW	Initial pattern write
IR	1. Infrared 2. Instruction Relocate bit in the MSR register (MSRIR)
IRCD	Intermittent register clock driver
IS	Industry standard
ISA	Instruction set architecture
ISU	1. Instruction sequencing unit 2. Interrupt source unit
ITR	Inherent time redundancy
IUE	Intermittent uncorrectable error
IVRM	Internal Voltage Regulation Module
IVRMCR	IVRM Control Register
IVRMDVR	IVRM Data Value Register
JEDEC	Formerly the Joint Electron Device Engineering Council
KHz	Kilohertz
L2SFF	Level 2 (L2) star flip flop
LBIST	Logical built-in self test

LBS	LBIST
LBUS	Local bus
LCB	1. Local clock buffer 2. Logon control block
LEM	Local error macro
LFSR	Linear Feedback Shift Register
LPID	Logical partition identification
LRDIMM	Load-reduced dual in-line memory module
LSB	Least-significant bit or byte
M/S	Master/slave
MA	Memory address
malf	Malfunction alert
MASK	A pattern of bits used to accept or reject bit patterns in another set of data. Hardware interrupts are enabled and disabled by setting or clearing a string of bits, with each interrupt assigned a bit position in a mask register.
MB	1. Mailbox 2. Megabyte
MBA	Memory buffer asynchronous
MBASE	Memory base
Mbps	Megabits per second
MBR	Member
MBS	Memory buffer synchronous
MC	1. Memory channel 2. Memory controller
MCA	The portion of the memory controller that runs synchronously to the memory interface.
MCB	The portion of the memory controller that runs synchronously to the DMI interface.
MCBCM	Memory controller built-in self-test compare mask
MCBCMQ	Memory Controller Built-In Self-Test Compare Mask Register
MCBIST	Memory card built-in self test
MCBIST-RQ	Memory controller built-in self-test to sequencer reorder queue interface
MCBMCAT	Memory controller built-in self-test maintenance current address trap
MCD	Memory coherency directory
MCE	1. Machine check exception 2. Mark corrected error 3. Marked chip correctable error
MCHK	Machine check
MCU	Memory control unit

MDI	Memory directory indicator. The MDI bit specifies the current scope of the data (local versus global).
MEM	Memory
MEMCTL	Memory control
MEMCTLCLKI	Memory controller interface clock
MEMINT	Memory interface
MEMINTCLKO	Memory interface clock
MFSI	Master flexible service interface
MHz	Megahertz
MIB	Memory interface bolt-on. Enables the programmable PowerPC-lite engine (PPE) to access its local memory and pervasive interconnect bus (PIB) interface.
MISO	Master input/slave output
MISR	Multiple Input Shift Register
MMIO	Memory-mapped input/output. Refers to the mapping of the address space required by an I/O device for Load or Store operations into the system's address space.
MOSI	Master output/slave input
MPE	Mark placed error
MPR	Multipurpose Register
MPW	Modify pulse width
MR7	Mode Register 7
MRS	Mode register set
MSB	Most-significant byte
MSGSND	Message send
MSR	Machine State Register
MT/s	Megatransfers per second
MTMSR	Move to Machine State Register instruction
MTSPR	Move to Special Purpose Register instruction
MULT	Multiplier
Multiple ranks	More than one rank of memory modules, where the data buses from each rank are connected to a common data bus of a single port. Data bus connections have multiple drops equal to the number of ranks attached. When more than one rank exists, this memory is depth-expanded memory.
MUX	Multiplexer
N/A	Not applicable
N/M	Memory command throttling mechanism specifying how many (N) commands are allowed to be issued to memory within every M-wide time window.
N/P	N-channel or p-channel transistor type

N1L	The name of a type of latch
NA	Not applicable
NACK	Negative acknowledgment
NBTI	Negative bias temperature instability
NC	Not connected; that is, the data cannot be written or read by that access.
NCE	New correctable error
NCF	NVIDIA® NVLink™ configuration fatal
NCLK	Nest clock
NCU	Noncacheable unit
NCX	Same as NC, but unstable (can be changed functionally)
NFET	Negative field-effect transistor
NHTM	Nest hardware trace macro
NM	See N/M.
NMMU	Nest memory management unit
NOP	No operation. A single-cycle operation that does not affect registers or generate bus activity.
NPU	NVLink processing unit
NVF	NVLink fatal
NVLD	Non-valid read/write data address
NVT	NFET threshold voltage
NX	Nest accelerator
OCB	On-chip controller (OCC) control bridge
OCC	On-chip controller. Provides power and thermal management, power cap enforcement, over-temperature protection, and low-power mode management.
OCCERRPT	OCC Error Reporting Register
OCI	On-chip-controller interface. Interface used by power management.
ODAT	Odd data
ODT	On-die termination
OE	Output enable
OEAR	OCI Error Address Register
OESR	OCI Error Status Register
OF	Open firmware
OHA	On-chiplet hardware assist
OISR	OCC Interrupt Source Register
OITR	OCC Interrupt Type Register

OJCFG	OCC JTAG Configuration Register
OJIC	OCC JTAG Instruction and Control Register
OJSTAT	OCC JTAG Status Register
OJTDI	OCC JTAG TDI Register
OOB	Out-of-band bus
OPB	On-chip peripheral bus
OPCG	On-product clock generator
OPCGGO	On-product clock generator “GO” signal
OR write	Current register content is ORed with write data and the result is stored in the register (access type WO_OR/WOX_OR).
OS	1. Open source 2. Operating system
OSC	Oscillator
OSCSW	Oscillator switch
OTP	One-time programmable
OTPROM	One-time programmable read-only memory
p2s	Parallel-to-serial machine
PBA	1. Pending bit array 2. Per buffer addressability 3. Power management processor bus interface 4. Power bus access (used by power management)
PBAX	PBA messaging
PC	1. Performance counter 2. Personal computer 3. Pervasive core unit 4. PHY control
PCB	1. Pervasive control bus. Processor logic that provides a generic, modular structure for communication between pervasive (glue logic between chiplets) elements. The PCB is used for read and full write access. 2. Printed circuit board
PCBIF	Pervasive control bus interface
PCBMS	PCB multiplexer
PCBSLAVE	Pervasive control bus slave macro
PCI	Peripheral Component Interconnect. An all-encompassing term referring to conventional PCI, PCI-X, and PCI Express.
PCIEX	Peripheral Component Interface Express
PCIS	The synchronous part of the PCI domain
PCLK	Processor clock
PD	1. Power down 2. Presence detect
PDA	Per DRAM addressability

PDR	Power Down Register
PE	1. Parity error 2. Partitionable endpoint. The smallest entity that can be partitioned in endpoint partitioning. 3. Product engineering
PEC	PCI Express controller
PECE	Power-savings exit control enable
PECESR	PECE Sample Register
PERCAL	Periodic calibration
PERV	Pervasive
PF	1. Pad fill keyword 2. Physical function. The physical function of an IOV adapter. For more information, see the PCI-SIG *I/O Virtualization (IOV) Specifications*. 3. Prefetch machine
PFET	Positive field-effect transistor
phase rotator step	Phase rotators are used extensively within the DDR PHY to adjust delays of signals. Each phase rotator has 128 phase-rotator steps in a clock period. Therefore, delay values, or phase-rotator settings, have a granularity of 1/128 of a clock period.
PHB	1. PCIe host bridge. An entity that attaches a PCIe bus to the system. 2. Power Systems host bridge
PHY	Physical layer
PHYP	Power hypervisor
PHYTOP	Physical layer top of hierarchy
PIB	Pervasive interconnect bus. A bus that provides access from masters through external interfaces and internal masters to common PIB attached slaves. The PIB is used for read and full write access.
PIB/LPC	Pervasive interconnect bus/low pin count
PIBMEM	Memory attached to the PIB bus and used by the self-boot engine (SBE)
PID	Process ID
PIG	Programmable interrupt generator
PIN	External C4 chip input pin
PIT	Programmable interval timer
plat	Pipeline staging latch
PLL	Phase-locked loop
PLLREG	Phase-Locked Loop Register
PM	Power management
PMC	1. Performance monitor counter 2. Power management control
PMCR	Power Management Control Register

PMCRS	Power Management Control Register shadow
PMISC	Pervasive miscellaneous
PMU	Performance monitor unit
POR	Power-on reset
port	A memory interface of variable width, consisting of an address/command bus and a data bus, connected to one or more ranks of memory. When multiple ranks are connected to a port, this memory is depth-expanded memory.
PPE	Programmable PowerPC-lite engine
PPM	1. Parts per million 2. PCB-slave power-management component
PPMPIG	PPM programmable interrupt generator
PR	1. Phase rotator 2. Privileged bit in the MSR (MSRPR)
PRBS	Pseudo-random binary sequence
PRD	Processor runtime diagnostic
PRE	Mnemonic for the DDR3 and DDR4 precharge command
PRESP	Processor response
PRPG	Pseudo-random pattern generator
PSC	Parallel-to-serial communication
PSCOM	Parallel-to-serial communication
PSCOMLE	Parallel-to-serial communication light edition
PSCR	Processor Stop Control Register
PSCRS	Processor Stop Control Register shadow
PSI	Processor support interface
PSRO	Performance sort-ring oscillator
PSU	Power supply unit
PUP	Pull-up
PURR	Processor Utilization Resource Register
PVREF	Precision voltage reference
PVT	Process voltage temperature
PVTN	Process voltage temperature N-type field effect transistor
PVTP	Process voltage temperature P-type field effect transistor
PW	Partial write
QACSR	Quad Analog Clock Status Register
QCSR	Quad Configuration Status Register
QFMR	Quad Frequency Measurement Register

QIDSR	Quad/Cache IVRM Dropout Sample Register
QMFR	Quad Frequency Measurement Register
QOS, QoS	Quality of service. This usually relates to a guarantee of minimum bandwidth for streaming applications.
QPMMR	Quad Power Management Mode Register
QPMMR[FSAFE]	A field in the QPMMR register to indicate the safe frequency to drop to in the event a heartbeat is lost.
QPPM	Quad PCB slave power management (cache)
R/W	Read/write
RA	Real address. An address for physical storage, which includes physical memory, local storage, and memory-mapped I/O registers. The maximum size of the real address space is 262 bytes.
RAM	1. Random-access memory 2. Resource allocation management
RAMDBG	A register that provides access to the PPE core's XIR3 debug register
RAMEDR	A register that provides access to the PPE core's XIR4 debug register
RAMGA	A register that provides access to the PPE core's XIR2 debug register
RAMRA	A register that provides access to the PPE core's XIR1 debug register
Rank	One or more memory modules that have a common command/address bus, a common chip select, and separate data bus connections. When more than one memory module exists, this memory is width-expanded memory.
Rank group	Up to four ranks of memory that have nearly identical timing characteristics such that the same DDR PHY delay and configuration values can be used to access all ranks. This configuration allows resources in the DDR PHY to be shared.
RAS	1. Reliability, availability, and serviceability. A combination of design methodologies, system policies, and intrinsic capabilities that, taken together, balance improved hardware availability with the costs required to achieve it. Reliability is the degree to which the hardware remains free of faults. Availability is the ability of the system to continue operating despite predicted or experienced faults. Serviceability is how efficiently and nondisruptively broken hardware can be fixed. 2. Row-address strobe
RASN	Row-address strobe (inverted)
RC	1. Read control 2. Root complex. Connects a PCIe bus into the system.
RCD	Register clock driver
RCD/LRDIM	Register clock driver/load-reduced dual in-line memory module
RCE	Retry CE: A correctable data error (CE) that occurs on the retry of a previous read.
RD	Read
RDATA	Read data
RDCLK	Read clock
RDDACK	Read acknowledgment

RDIMM	Registered dual in-line memory module
RDIV	Reference clock divide
RECR	Read ECC Control Register
REF	Mnemonic used for the DDR3 and DDR4 refresh command.
REFCLK	Reference clock
REG	Register
REGF	Register file
REPR	Array repair
REQ	Request
RFIR	Recoverable FIR
RISC	Reduced instruction set computing
RISCTRACE	A tool used to reconstruct a code flow from a hardware debug trace
RJR	Receiver random jitter
RLDRAM	Reduced latency dynamic random access memory
RLO	Read latency offset
RMW	Read-modify-write
RNG	Random number generator
RO	Read only
ROM	Read-only memory
ROX	Read only but unstable. Can be changed functionally. Hardware can change the value between reads of the register.
RRQ	Read reorder queue
RTL	Register transfer level
RTT	Requester ID (RID) translation table
RTY	Retry
RUN-N, RUNN	Run the engine for N cycles
RUNTIMECTRQ	Runtime counter facility
RW	Readable and writable
RW_WAND	Readable and writable. A write ANDs written data with existing data and stores the result.
RW_WCLEAR	Readable and writable. Any write to the address clears the bits regardless of value.
RW_WOR	Readable and writable. A write ORs written data with existing data and stores the result.
RWITM	Read with intent to modify
RWX	Same as RW, but unstable. Can be changed functionally.
RWX_WAND	Same as RW_WAND, but unstable. Can be changed functionally.

RWX_WCLEAR	Same as RW_WCLEAR, but unstable. Can be changed functionally.
RWX_WCLRPART	Same as RW_WCLRPART, but unstable. Can be changed functionally.
RWX_WOR	Same as RW_WOR, but unstable. Can be changed functionally.
RWX_WSETPART	Same as RW_WSETPART, but unstable. Can be changed functionally.
RX	Receive
RXBIST	Receive built-in self test
RXCTL	Receive control
SAB	Secure access bit
SBASE	SRAM base address in the core management engine (CME), used by the CME block copy engine (BCE)
SBE	1. Self-boot engine. Initializes the processor chip and then loads or invokes the hostboot IPL firmware base image. 2. State bit entry
SC	Store clean (transactional memory value before a speculative store)
SCAN	Refers to shifting groups of latch states internal to a chip to read or write them when functionally not in use.
SCE	Symbol mark corrected error
SCM	Single-chip module
SCOM	Serial communications. SCOM is used for read and full write access.
SCOM1	Serial communications 1. SCOM1 is used for AND write access.
SCOM2	Serial communications 2. SCOM2 is used for OR write access.
SDM	Secure debug mode
SE	1. Scan enable 2. Single-step trace enabled bit in the MSR (MSRSE)
SEC	Single error correction
SEEPROM	Serial electrically erasable programmable read-only memory. An EEPROM memory device that can only be read, but which can be reprogrammed by an external programmer. Note that the hostboot is able to initiate writes to SEEPROMS connected to the circuit board through a serial bus.
SEL	Select
SEQ	Sequencer
SG	Scan gate
SHA	Secure hash algorithm
SIB	Service interface bolt-on. Allows the GPE to communicate with the PIB and the I^2C interface.
SICR	Stop Interface Control Register
Single rank	One rank of memory modules, where all the data bus connections are wired point-to-point to the DDR PHY. The data bus connections include read data, write data, read clocks/strobes, and write clock/strobes.
SIR	Security Isolation Register. Similar to a Fault Isolation Register.

SISR	Stop Interface Status Register
SKEWADJ	Analog clock skew adjust macro
SLB	Segment lookaside buffer. This buffer is used to map an effective address to a virtual address.
SM	State machine
SMDR	Same master rank, different slave rank
SMP	Symmetric multiprocessing
SMT	1. Simultaneous multithreading 2. Surface mount
SN	Snoop machine
SNOE	Scan net optimization enhancement
SNOP	Start sync/wait step; no operation
SOI	Silicon-on-insulator
SP	Service processor
SPATTN	Special attention
SPCIF	Specification
SPI	Serial peripheral interface. Refers to a 4-wire, serial, full-duplex bus with masters and slaves. Commonly used to interface with sensors, control devices, and so on in embedded systems.
SPR	Special-purpose register
SPRD	Special-purpose register data
SPS	1. Steps per sync 2. Sleep Pstate
SPURR	Scaled Processor Utilization Resource Register
SRAM	Static random access memory
SRC	Service reference code
SRQ	Store reorder queue
STEP	Supplier test enablement program
STR	Self time refresh
SUE	Special uncorrectable error
SUE/UE	Special uncorrectable error/uncorrectable error
SW	Software
SYNC	Synchronize
SYS	System
SYSCLK	System clock
TB	Time base
TBD	To be determined

TC	Traffic class. In PCIe, this defines a priority between PCI transactions within a virtual channel (VC).
TCE	1. Translation control entry. Used to translate an I/O address page number to a real page number in system memory. 2. Two-symbol correctable error
TCK	JTAG clock; test clock
TDI	Test data in
TDM	1. Time division multiplexed 2. Time domain multiplexing
TDM command mode	A DDR PHY configuration that supports two ports that share a common address/command bus. The addresses and commands for both ports are time division multiplexed on the common address/command bus. Individual chip selects select which ranks respond to a given address/command. Ranks connected to different ports can be selected to respond to the same command.
TDO	Test data out
TDR	1. Translation control entry (TCE) data random-access memory (RAM) 2. Time-domain reflectometry
TE	Test enable
TFMR	Time Facility Management Register
THD	Thread
TI	Terminate immediately
TID	Thread ID
TLB	Translation lookaside buffer. An on-chip cache that translates virtual addresses (VAs) to real addresses (RAs). A TLB caches page-table entries for the most recently accessed pages, thereby eliminating the necessity to access the page table from memory during load-store operations.
TLBI	Translation lookaside buffer invalidate
TLBIE	Translation lookaside buffer invalidate entry instruction
TM	Transactional memory
TMR	Timer
TMS	Test mode select
TOD	Time of day
TPM	1. Top of peripheral memory 2. Trusted platform module
TPMD	Trusted platform module
tREFI	Refresh interval
TSV	Trans silicon via
TWSM	Table walk state machine
TX	Transmit
TXBIST	Transmit built-in self test

TXCTL	Transmit control
TZ	Tile zone
UDE	Unconditional debug event
UE	Uncorrectable error
UI	1. User interface 2. Unit interval
UL	Uplink
ULCCH	Uplink control channel
ULDCH	Uplink data channel
UMAC	User-mode access control
VAS	Virtual accelerator switchboard
VC	Virtual channel
VCC	Voltage supply
VCO	Voltage controlled oscillator
VCTR	VDM Count Threshold Register
VDCR	VDM Droop Count Register
VDM	Voltage droop monitor
VDSR	VDM Data Sample Register
VECR	VDM Event Count Register
VGA	1. Variable gain amplifier 2. Video graphics array
VHDL	VHSIC hardware description language
VHSIC	Very high speed integrated circuit
VID	Voltage identification
VIO	Voltage I/O
VITL	Vital
VMEAS	Voltage measurement
VMX	Vector multimedia extension
VNCR	VDM Non-Droop Count Register
VPAD	Pad voltage
VPROTH	Voltage protect high
VREF	Voltage reference
VREG	1. Voltage regulator 2. Voltage regulation
VRM	Voltage regulator module
VSU	Vector scalar unit
VT	Voltage control

WAT	Workaround macro
WC	1. Worst case 2. Write control
Wdata, WDATA	Write data
WDF	Designator for the memory controller's read-modify-write data flow and associated control.
WDFCFG	Configuration facilities for the WDF logic.
WECR	Write ECC Control Register
WEN	Write enable
WLO	Write latency offset
WO	Write only
WO_1P	Write only; one pulse length is equal to one register cycle.
WO_AND	Same as RW_WAND, but the bits are write-only.
WO_CLEAR	Same as RW_WCLEAR, but the bits are write-only.
WO_CLRPART	Same as RW_WCLRPART, but the bits are write-only.
WO_n_mP	Write only pulsed. A write of ‘1’ creates a pulse for a minimum of n register clocks and a maximum of m register clocks. A read returns ‘0’.
WO_nP	Write only pulsed. A write of ‘1’ creates a pulse for n register clocks. A read returns ‘0’.
WO_OR	Same as RW_WOR, but the bits are write-only.
WO_SETPART	Same as RW_WSETPART, but the bits are write-only.
WOF	1. Who's on first? 2. Workload optimized frequency
WOX_AND	Same as WO_AND, but unstable. Can be changed functionally.
WOX_CLEAR	Same as WO_CLEAR, but unstable. Can be changed functionally.
WOX_CLRPART	Same as WO_CLRPART, but unstable. Can be changed functionally.
WOX_n_mP	Same as WO_n_mP, but unstable. Can be changed functionally.
WOX_nP	Same as WO_nP, but unstable. Can be changed functionally.
WOX_OR	Same as WO_OR, but unstable. Can be changed functionally.
WOX_SETPART	Same as WO_SETPART, but unstable. Can be changed functionally.
WR	Write
WRCNTL	Write control
WRD	Write data. Designator for the portion of the memory controller's write data flow that generates the outbound memory ECC check bits.
WRQ	Write reorder queue
WRT	Designator for the memory controller's write data flow.
WRTCFG	Configuration facilities for the memory controller's WRT logic.

XBUS	Note: This is not really an acronym but a name (X bus).
XCR	External Control Register
XER	Fixed-Point Exception Register
XFIR	X Fault Isolation Register
XIR	1. External Interface Register 2. External interface to the PPE IR Register
XIVR	External Interrupt Vector Register for the OCC (405)
XOR	Exclusive OR
XSCOM	Extended SCOM. Special, fast SCOM that allows the processor cores to directly SCOM the PIB. Processor buses must be enabled to the slave processor chips for the master processor to XSCOM them.
XSR	External Status Register for PPE
XSTOP	Checkstop
ZCAL	Impedance (Z) calibration
ZCNTLCPURO	Periodic impedance (Z) calibration
ZCONTROL	Impedance (Z) control
ZQ	I/O impedance
ZQCal	I/O impedance calibration

1. POWER9 Processor Overview

The POWER9 processor is a superscalar symmetric multiprocessor designed for use in servers and large-cluster systems. It uses 14 nm technology with 17 metal layers. The POWER9 processor can have up to 24 cores enabled on a single chip. It supports direct-attach memory. It supports a maximum symmetric multiprocessing (SMP) size of two sockets and is targeted for scale-out workloads. Each POWER9 core supports up to four threads using simultaneous multithreading (SMT). The SMT can be dynamically tuned so that each core has one, two, or four threads

This document describes the POWER9 registers and related accessing method.

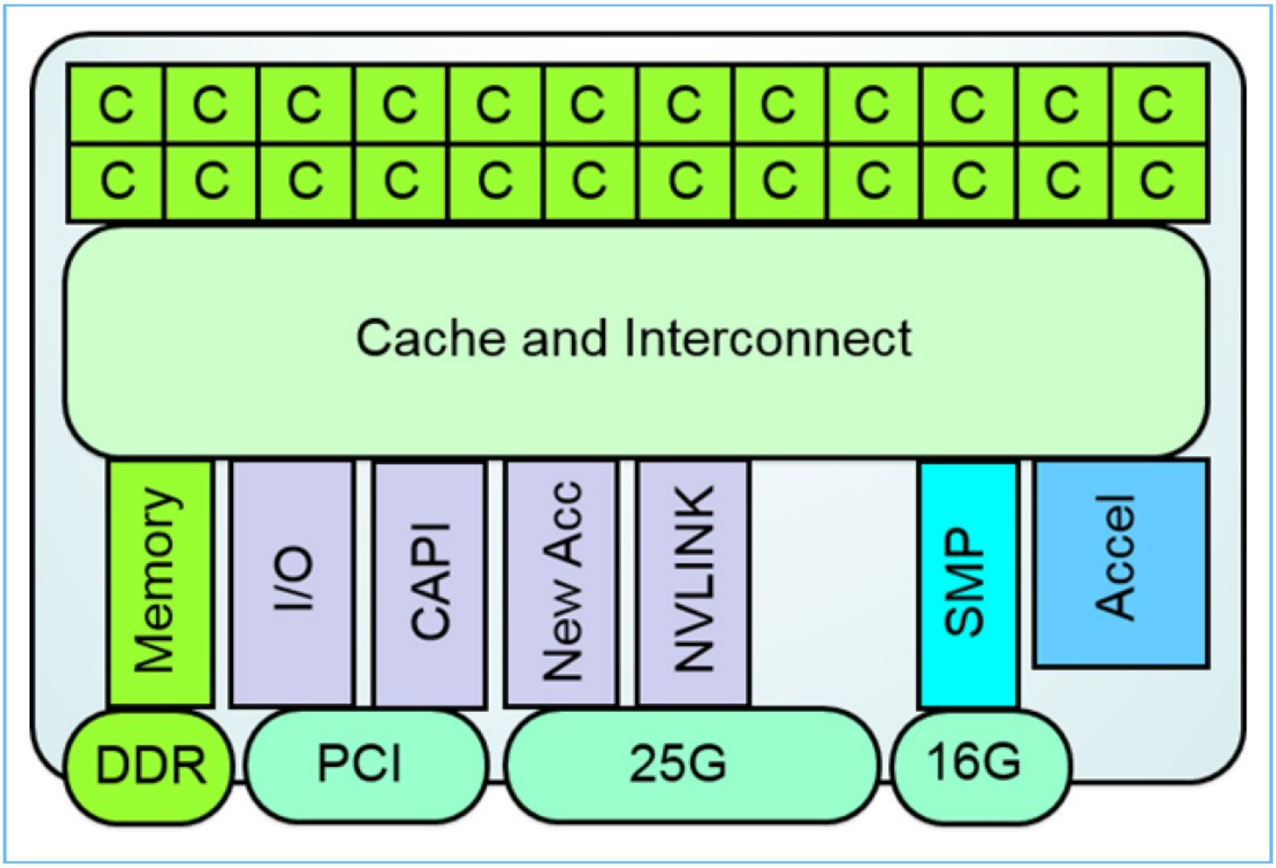
1.1 POWER9 Processor Features

Figure 1 on page 31 shows the POWER9 processor, which supports the following features:

- Twenty-four POWER9 chiplets, which contain one POWER9 core, an L2 cache, and an L3 cache.
  - On-chip accelerators.
  - Coherent Accelerator Processor Interface (CAPI), which enables an FPGA or ASIC to connect coherently to the POWER9 processor SMP interconnect via the PCIe bus.
  - On-chip compression, encryption, and data movement initiated by the hypervisor, GZIP engine, or nest MMU to enable user access to all accelerators.

    - In-core user invocation of encryption using the Advanced Encryption Standard (AES) and the secure hash algorithm (SHA).
- Two memory controllers that support direct-attached DDR4 memory:
    - Support four direct-attach memory buses (DDR 0, 1, 6, and 7).
    - Support ×4 and ×8, 4 - 16 Gb DRAMs and 3D stacked DRAMs.
    - Support registered dual in-line memory modules (RDIMMs) and lad-reduced dual in-line memory modules (LRDIMMs).
- Processor SMP interconnect.
    - Supports one inter-node SMP X bus link.
    - Maximum two-socket SMP.
- Three PCIe controllers (PEC) with 16 lanes of PCI Express Gen 4 I/O.
    - PEC0: one ×16 lanes.
    - PEC1: two ×8 lanes (bifurcation).
    - PEC2: one ×16 lane mode, two ×8 lanes (bifurcation), or one ×8 lane and two ×4 lanes (trifurcation).
    - PEC0 and PEC2 support CAPI 2.0.
- Power management.
- Pervasive interface.

Figure 1: POWER9 Processor General Diagram



1.2 POWER9 Processor Pervasive Structure

Figure 2 on page 33 shows the POWER9 chip from a pervasive-centric point of view. The different colors denote different chiplets from a pervasive perspective. Each chiplet consists of one global clock controller and multiple local clock controllers, which enable a chiplet to service multiple different clock regions. Multiple clock regions can run at the same frequency, but can be turned off independently. The chip contains 24 cores capable of running at different frequencies. The pervasive logic supports these 24 cores.

Figure 2: POWER9 Processor from a Pervasive Point of View

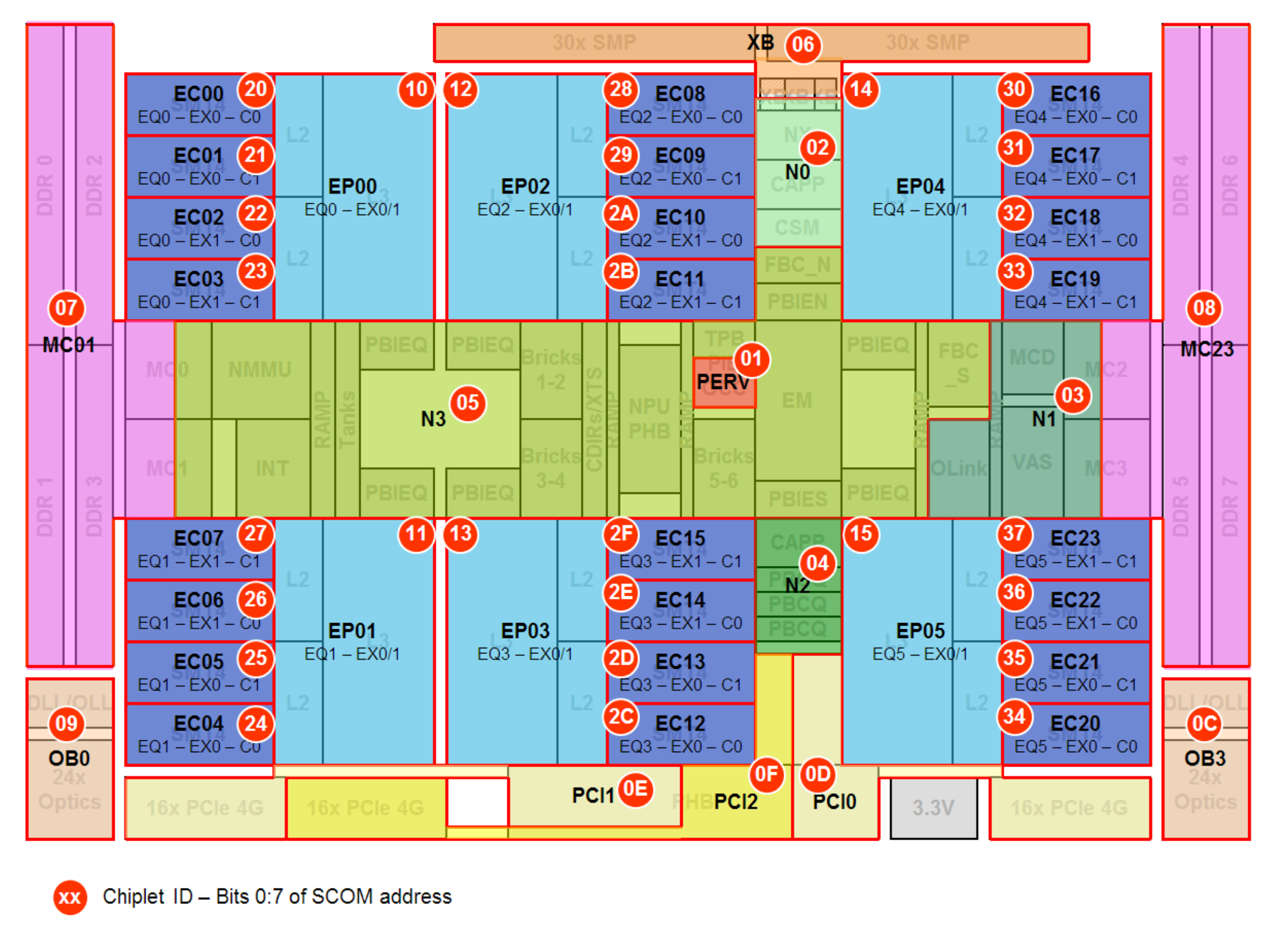


Figure 3 on page 34 lists the chiplets in the design, and their controlling pervasive blocks, by chiplet ID.

Figure 3 POWER9 Chiplets and IDs

ID	Chiplet
0x00	PIB PIB bus (no cplt.)
0x01	PERV Pervasive
0x02	N0 Nest North
0x03	N1 Nest East
0x04	N2 Nest South
0x05	N3 Nest West
0x06	XB XBus
0x07	MC01 Mem. Ctrl. West
0x08	MC23 Mem Ctrl. East
0x09	OB0 OBus 0
0x0A	
0x0B	
0x0C	OB3 OBus 3
0x0D	PCI0 PCIe 0
0x0E	PCI1 PCIe 1
0x0F	PCI2 PCIe 2

ID	Chiplet
0x10	EP00 – Cache EQ0, EX0/1 Virtual EX IDs: EX00: 0x10 EX01: 0x18
0x11	EP01 – Cache EQ1, EX0/1 Virtual EX IDs: EX00: 0x11 EX01: 0x19
0x12	EP02 – Cache EQ2, EX0/1 Virtual EX IDs: EX00: 0x12 EX01: 0x1A
0x13	EP03 – Cache EQ3, EX0/1 Virtual EX IDs: EX00: 0x13 EX01: 0x1B

ID	Chiplet
0x20	EC00 – SMT4 Core EQ0, EX0, C0
0x21	EC01 – SMT4 Core EQ0, EX0, C1
0x22	EC02 – SMT4 Core EQ0, EX1, C0
0x23	EC03 – SMT4 Core EQ0, EX1, C1
0x24	EC04 – SMT4 Core EQ1, EX0, C0
0x25	EC05 – SMT4 Core EQ1, EX0, C1
0x26	EC06 – SMT4 Core EQ1, EX1, C0
0x27	EC07 – SMT4 Core EQ1, EX1, C1
0x28	EC08 – SMT4 Core EQ2, EX0, C0
0x29	EC09 – SMT4 Core EQ2, EX0, C1
0x2A	EC10 – SMT4 Core EQ2, EX1, C0
0x2B	EC11 – SMT4 Core EQ2, EX1, C1
0x2C	EC12 – SMT4 Core EQ3, EX0, C0
0x2D	EC13 – SMT4 Core EQ3, EX0, C1
0x2E	EC14 – SMT4 Core EQ3, EX1, C0
0x2F	EC15 – SMT4 Core EQ3, EX1, C1

ID	Chiplet
0x14	EP04 – Cache EQ4, EX0/1 Virtual EX IDs: EX00: 0x14 EX01: 0x1C
0x15	EP05 – Cache EQ5, EX0/1 Virtual EX IDs: EX00: 0x15 EX01: 0x1D

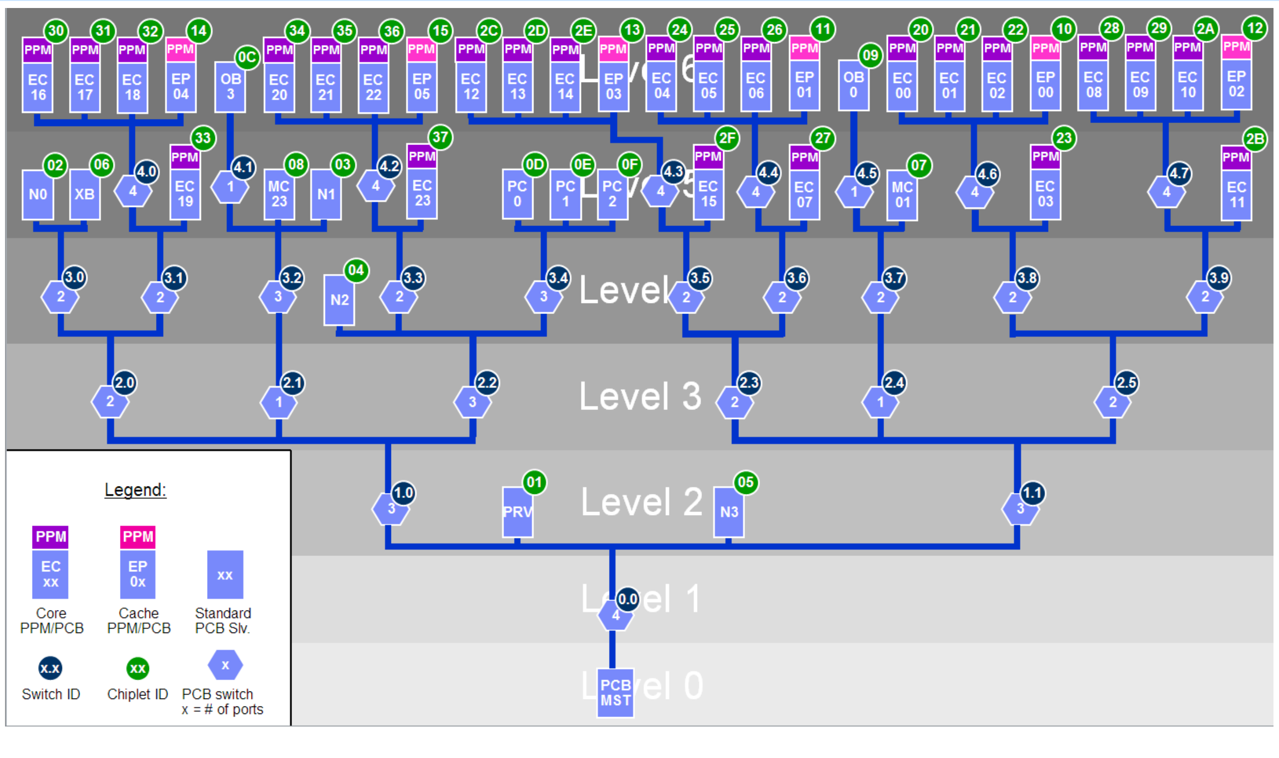
ID	Chiplet
0x30	EC16 – SMT4 Core EQ4, EX0, C0
0x31	EC17 – SMT4 Core EQ4, EX0, C1
0x32	EC18 – SMT4 Core EQ4, EX1, C0
0x33	EC19 – SMT4 Core EQ4, EX1, C1
0x34	EC20 – SMT4 Core EQ5, EX0, C0
0x35	EC21 – SMT4 Core EQ5, EX0, C1
0x36	EC22 – SMT4 Core EQ5, EX1, C0
0x37	EC23 – SMT4 Core EQ5, EX1, C1

1.2.1 Pervasive Control Bus and Pervasive Interconnect Bus

The pervasive control bus (PCB) provides a generic, modular structure for communication between the pervasive elements. The PCB provides the POWER9 pervasive unit with an interface to the pervasive functions on the various POWER9 processor chiplets. For this purpose, a PCB master is implemented inside the POWER9 pervasive logic. This master, by means of the PCB interconnect, communicates with the PCB slave located in each chiplet. The PCB master sends commands, such as read and write requests, to the PCB slaves. The slaves, on the other hand, respond to the commands received from the master, and also notify the master of interrupts that occur in the slave's chiplet.

Figure 4 on page 35 shows the PCB structure that services all the chiplets.

Figure 4: Pervasive Control Bus Structure and Chiplets



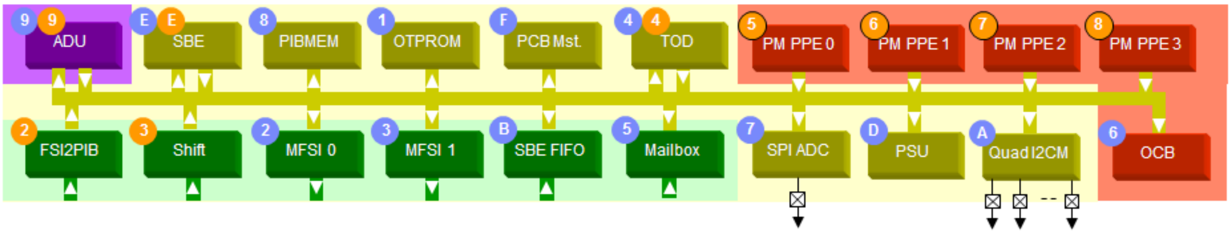
The PCB switch features two independent channels for the PCB topology. The downstream input channel provides a fan-out to the downstream output ports, which are connected either to another switch in a multistage topology or directly to a slave. The upstream output channel is arbitrated between requests from the upstream input ports, which is the case when replying to a multicast operation.

The pervasive interconnect bus (PIB) provides access from the masters via the external interfaces and the internal masters to the common PIB-attached slaves. *Figure 5* on page 36 shows the PIB masters and slaves.

- The external interfaces include the I^2C slave and the flexible service interface (FSI).
- The internal masters include the FSI shift engine, FSI2PIB, and the XSCOM/alter-display unit (ADU).
- The PIB-attached slaves include the PCB master, PIB2OPB, general-purpose register (GPR), I^2C master, and the I^2C slave.

The PIB facilitates transactions between multiple PIB masters and multiple PIB slaves. For each transaction, the PIB arbiter establishes a point-to-point connection between a single requesting master and a single slave uniquely addressed by the master.

Figure 5: PIB Masters and Slaves



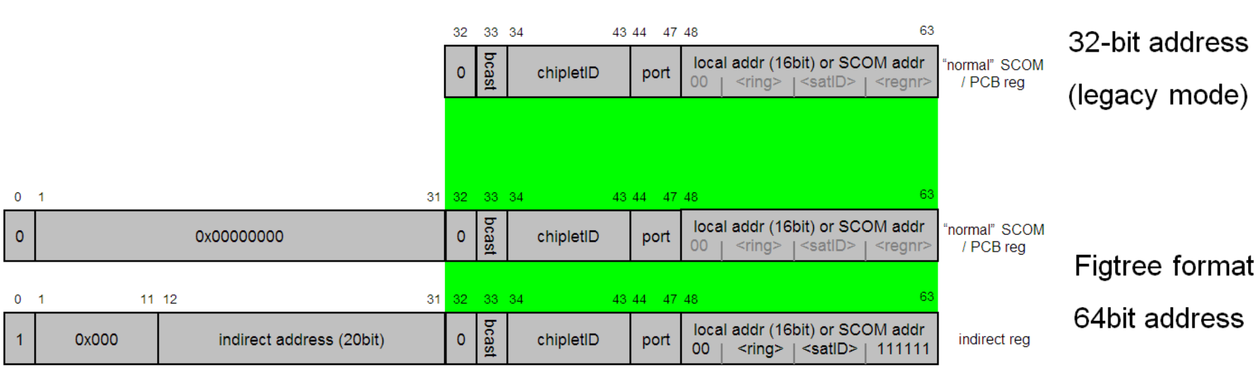
- Pervasive Interconnect Bus (PIB):
  - 9 PIB master (2x CFAM, 4x OCC, 1x Bridge, 2x PIB domain)
  - 13 PIB slaves (4x CFAM, 1x OCC, 1x Bridge, 7x PIB domain)
- Pervasive Connect Bus (PCB):
  - Root in PIB (PCB Master)
  - Provides tree-like switch network to all chiplets
  - 30 Chiplets defined as of now
- PIB & PCB domain run at 465 - 600 MHz (Nest Clock 4:1)
- PIB & PCB domain get initialized (scan0 & clock start) by the pervasive clock controller which is controlled by the new *CFAM Boot Sequencer* (CBS)
- PIB & PCB are trusted domains – no direct access from Service Elements (FSP/BMC) in secured chips

ID #	Master	Domain	Slave	Domain
0x0	LBUS		LBUS	
0x1	free		OTPROM	pib
0x2	FSI2PIB	cfam	FSI Master 0	cfam
0x3	FSISHIFT	cfam	FSI Master 1	cfam
0x4	TOD	pib	TOD	pib
0x5	PM PPE 0	occ	FSI Mailbox	cfam
0x6	PM PPE 1	occ	OCI Bridge	occ
0x7	PM PPE 2	occ	SPI ADC	pib
0x8	PM PPE 3	occ	PIBMEM	pib
0x9	ADU	bridge	ADU	bridge
0xA	free		I2C master	pib
0xB	free		SBE FIFO	cfam
0xC	free		free	
0xD	free		PSU	pib
0xE	SBE	pib	SBE	pib
0xF	CME		PCB Master	pib

1.2.2 PCB Address Space

Figure 6 shows the address format used to access all pervasive facilities. The legacy 32-bit format is shown as well as the translation in the 64-bit format (add 32 zeros as the most-significant bits). The new extended address format that enables access to the large address SCOM satellites (up to 31 bits) is also listed. The most significant bit is '1' in that case.

Figure 6: Common Pervasive Address Map Format

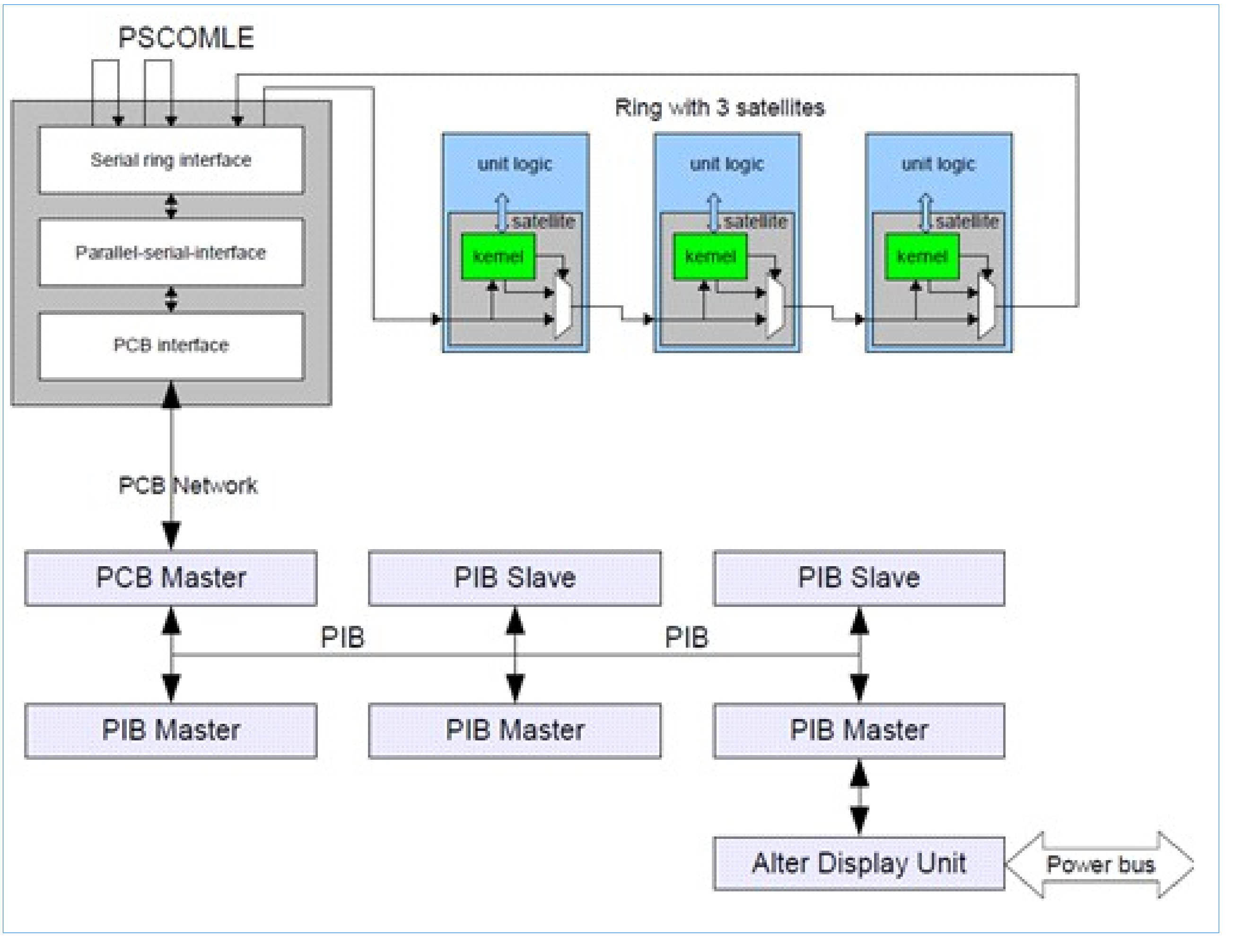


1.2.3 SCOM

SCOM provides a serial communication infrastructure within the pervasive infrastructure. The central control unit is referred to as the parallel-to-serial communication light edition (PSCOMLE). It controls all communication with respect to the serial interface. The end-point nodes are referred to as satellites. A satellite is located in the unit logic. The satellites are connected to the PSCOMLE and each other in a physical ring. The PSCOMLE can support up to 15 rings. Each ring has a local address space that is used to address an individual satellite in a given ring and within the unit logic that uses the satellite with a dedicated register. If this address space is not sufficient, an indirect address can be used to further extend the address range within a satellite.

Figure 7 shows the principal pervasive infrastructure to access the SCOM-enabled registers in a chiplet. A SCOM access can be initiated from the masters connected to the PIB, such as the ADU. SCOM satellites are distributed inside the chiplet and are organized in serial SCOM rings. For each chiplet, there is one instance of the PSCOMLE macro that receives the request from the PCB network.

Figure 7: Infrastructure to Access SCOM Registers

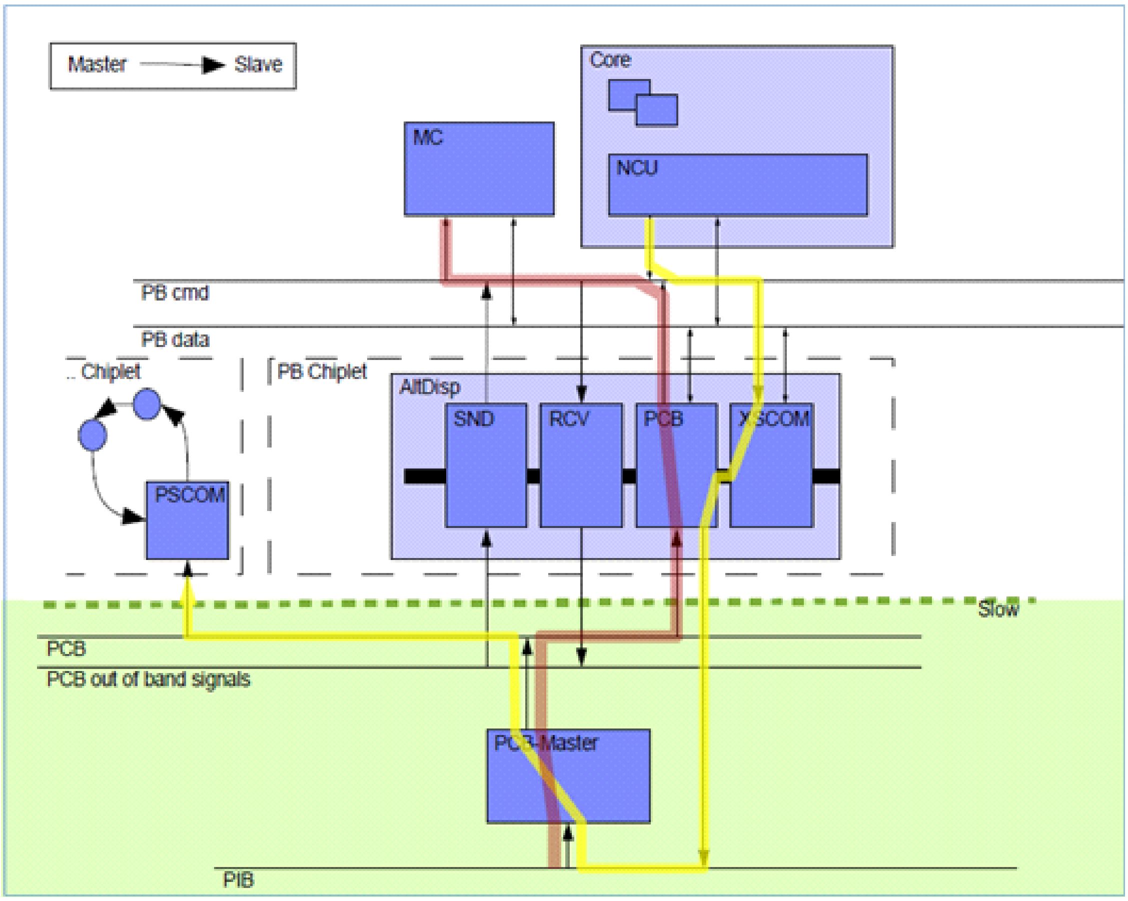


1.2.4 XSCOM

The alter/display unit (ADU) acts as a bridge between the processor bus and the PCB. The ADU enables access to any memory-mapped PIB/PCB register in the system by external SCOM (XSCOM.) The XSCOM is responsible for handling memory-mapped PIB/PCB register access, which originates from the non-pervasive logic of the processor. For example, a read/write operation can originate from a processor core and is presented on the processor bus by the non-cacheable unit (NCU). The alter/display unit XSCOM routes the request through a PIB master to the PIB. The PIB master notifies the ADU when it is complete. For a read operation, the ADU routes the resulting data to the processor bus, which sends the information back to the requester (in the example, the NCU). It then arrives at the core. The XSCOM memory-mapped address range, by default, locates at 0x0003FC0000000000.

Figure 8 shows an example of a read and write to a memory-mapped PCB address space.

Figure 8: Read and Write to Memory-Mapped PCB Address Space



1.3 Register Accessing Type

A register can have multiple addresses, with a different address for different chiplets. The types of access permitted can vary by chiplets. *Table 1* on page 39 summarizes the valid register access types.

Table 1: Register Access Types

Access Type	Description
NC	Not connected; the data cannot be written or read by that access.
NCX	Same as NC, but unstable. Can be changed functionally.
RO	Read only. Only to be used if a bit is tied. Status bits should be ROX.
ROX	Same as RO, but unstable. Can be changed functionally.
ROX_CLRPART	Same as ROX, but a read access clears the bits after they have been accessed.
RW	Readable and writable.
RW_WAND	Readable and writable. A write ANDs written data with existing data and stores the result.
RW_WCLEAR	Readable and writable. A write of a ‘1’ clears the bit. A write of a ‘0’ does nothing.
RW_WCLRPART	Readable and writable. Any write to the address clears the bits regardless of the value.
RW_WOR	Readable and writable. A write ORs written data with existing data and stores the result.
RW_WSETPART	Readable and writable. Any write to the address sets the bits regardless of the value.
RWX	Same as RW, but unstable. Can be changed functionally.
RWX_WAND	Same as RW_WAND, but unstable. Can be changed functionally.
RWX_WCLEAR	Same as RW_WCLEAR, but unstable. Can be changed functionally.
RWX_WCLRPART	Same as RW_WCLRPART, but unstable. Can be changed functionally.
RWX_WOR	Same as RW_WOR, but unstable. Can be changed functionally.
RWX_WSETPART	Same as RW_WSETPART, but unstable. Can be changed functionally.
WO	Same as RW, but bits are write-only.
WO_1P	Write only; one pulse length is equal to one register cycle.
WO_AND	Same as RW_WAND, but bits are write-only.
WO_CLEAR	Same as RW_WCLEAR, but bits are write-only.
WO_CLRPART	Same as RW_WCLRPART, but bits are write-only.
WO_n_mP	Write-only pulsed. A write of ‘1’ creates a pulse for a minimum of n register clocks and a maximum of m register clocks. A read returns ‘0’.
WO_nP	Write-only pulsed. A write of ‘1’ creates a pulse for n register clocks. A read returns ‘0’.
WO_OR	Same as RW_WOR, but bits are write-only.
WO_SETPART	Same as RW_WSETPART, but bits are write-only.
WOX	Same as WO, but unstable. Can be changed functionally.
WOX_AND	Same as WO_AND, but unstable. Can be changed functionally.
WOX_CLEAR	Same as WO_CLEAR, but unstable. Can be changed functionally.
WOX_CLRPART	Same as WO_CLRPART, but unstable. Can be changed functionally.
WOX_n_mP	Same as WO_n_mP, but unstable. Can be changed functionally.
WOX_nP	Same as WO_nP, but unstable. Can be changed functionally.

Access Type	Description
WOX_OR	Same as WO_OR, but unstable. Can be changed functionally.
WOX_SETPART	Same as WO_SETPART, but unstable. Can be changed functionally.

2. XBUS Chiplet

The POWER9 processor registers are listed alphabetically by mnemonic in the following address table.

Mnemonic	Address	Page
IOF1.BUSCTL.SCOM.FIR_ACTION0_REG	0x0000000006011006	92
IOF1.BUSCTL.SCOM.FIR_ACTION1_REG	0x0000000006011007	93
IOF1.BUSCTL.SCOM.FIR_MASK_REG	0x0000000006011003	91
IOF1.BUSCTL.SCOM.FIR_REG	0x0000000006011000	89
IOF1.BUSCTL.SCOM.FIR_WOF_REG	0x0000000006011008	93
IOF1.BUSCTL.SCOM.SCOM_MODE_PB	0x0000000006011020	93
IOF2.BUSCTL.SCOM.FIR_ACTION0_REG	0x0000000006011406	97
IOF2.BUSCTL.SCOM.FIR_ACTION1_REG	0x0000000006011407	97
IOF2.BUSCTL.SCOM.FIR_MASK_REG	0x0000000006011403	95
IOF2.BUSCTL.SCOM.FIR_REG	0x0000000006011400	94
IOF2.BUSCTL.SCOM.FIR_WOF_REG	0x0000000006011408	98
IOF2.BUSCTL.SCOM.SCOM_MODE_PB	0x0000000006011420	98
IOFPPE.PPE.ARB.ARB.CSAR	0x000000000601084D	83
IOFPPE.PPE.ARB.ARB.CSCR	0x000000000601084A	82
IOFPPE.PPE.ARB.ARB.CSDR	0x000000000601084E	83
IOFPPE.PPE.PPE.PPE.MIB.MIB_XIICAC	0x0000000006010859	87
IOFPPE.PPE.PPE.PPE.MIB.MIB_XIMEM	0x0000000006010857	86
IOFPPE.PPE.PPE.PPE.MIB.MIB_XISGB	0x0000000006010858	87
IOFPPE.PPE.PPE.PPE.PPE.PPE_XIDBGPRO	0x0000000006010855	85
IOFPPE.PPE.PPE.PPE.PPE.PPE_XIRAMDBG	0x0000000006010853	84
IOFPPE.PPE.PPE.PPE.PPE.PPE_XIRAMEDR	0x0000000006010854	85
IOFPPE.PPE.PPE.PPE.PPE.PPE_XIRAMGA	0x0000000006010852	84
IOFPPE.PPE.PPE.PPE.PPE.PPE_XIRAMRA	0x0000000006010851	83
IOFPPE.PPE.PPE.PPE.PPE.PPE_XIXCR	0x0000000006010850	83
IOFPPE.PPE.PPE_FIR_ACTION0_REG	0x0000000006010846	81
IOFPPE.PPE.PPE_FIR_ACTION1_REG	0x0000000006010847	81
IOFPPE.PPE.PPE_FIR_MASK_REG	0x0000000006010843	80
IOFPPE.PPE.PPE_FIR_REG	0x0000000006010840	80
IOFPPE.PPE.PPE_FIR_WOF_REG	0x0000000006010848	81
IOFPPE.SCOM_PPE_CNTL	0x0000000006010860	88
IOFPPE.SCOM_PPE_FLAGS	0x0000000006010863	89
IOFPPE.SCOM_PPE_WORK_REG1	0x0000000006010861	88
IOFPPE.SCOM_PPE_WORK_REG2	0x0000000006010862	88
PB.IOE.LL0.IOEL_CONFIG	0x000000000601180A	103
PB.IOE.LL0.IOEL_CONTROL	0x000000000601180B	104
PB.IOE.LL0.IOEL_DLL_STATUS	0x0000000006011828	113
PB.IOE.LL0.IOEL_ERR_INJ_LFSR	0x000000000601181B	108
PB.IOE.LL0.IOEL_FIR_ACTION0_REG	0x0000000006011806	102
PB.IOE.LL0.IOEL_FIR_ACTION1_REG	0x0000000006011807	102
PB.IOE.LL0.IOEL_FIR_MASK_REG	0x0000000006011803	101
PB.IOE.LL0.IOEL_FIR_REG	0x0000000006011800	98
PB.IOE.LL0.IOEL_FIR_WOF_REG	0x0000000006011808	103

Mnemonic	Address	Page
PB.IOE.LL0.IOEL_LAT_MEASURE	0x000000000601180E	104
PB.IOE.LL0.IOEL_LINK0_EDPL_STATUS	0x0000000006011824	111
PB.IOE.LL0.IOEL_LINK0_ERROR_STATUS	0x0000000006011816	106
PB.IOE.LL0.IOEL_LINK0_INFO	0x0000000006011814	105
PB.IOE.LL0.IOEL_LINK0_QUALITY	0x0000000006011826	112
PB.IOE.LL0.IOEL_LINK0_SYN_CAPTURE	0x0000000006011822	111
PB.IOE.LL0.IOEL_LINK1_EDPL_STATUS	0x0000000006011825	112
PB.IOE.LL0.IOEL_LINK1_ERROR_STATUS	0x0000000006011817	107
PB.IOE.LL0.IOEL_LINK1_INFO	0x0000000006011815	106
PB.IOE.LL0.IOEL_LINK1_QUALITY	0x0000000006011827	113
PB.IOE.LL0.IOEL_LINK1_SYN_CAPTURE	0x0000000006011823	111
PB.IOE.LL0.IOEL_PERF_COUNTERS_0	0x000000000601181E	110
PB.IOE.LL0.IOEL_PERF_COUNTERS_1	0x000000000601181F	110
PB.IOE.LL0.IOEL_PERF_COUNT_LSB_0	0x0000000006011820	110
PB.IOE.LL0.IOEL_PERF_COUNT_LSB_1	0x0000000006011821	110
PB.IOE.LL0.IOEL_PERF_SEL_CONFIG	0x000000000601181D	109
PB.IOE.LL0.IOEL_PERF_TRACE_CONFIG	0x000000000601181C	108
PB.IOE.LL0.IOEL_REPLAY_THRESHOLD	0x0000000006011818	107
PB.IOE.LL0.IOEL_SEC_CONFIG	0x000000000601180D	104
PB.IOE.LL0.IOEL_SL_ECC_THRESHOLD	0x0000000006011819	108
PB.IOE.LL1.IOEL_CONFIG	0x0000000006011C0A	117
PB.IOE.LL1.IOEL_CONTROL	0x0000000006011C0B	118
PB.IOE.LL1.IOEL_DLL_STATUS	0x0000000006011C28	128
PB.IOE.LL1.IOEL_ERR_INJ_LFSR	0x0000000006011C1B	122
PB.IOE.LL1.IOEL_FIR_ACTION0_REG	0x0000000006011C06	116
PB.IOE.LL1.IOEL_FIR_ACTION1_REG	0x0000000006011C07	117
PB.IOE.LL1.IOEL_FIR_MASK_REG	0x0000000006011C03	115
PB.IOE.LL1.IOEL_FIR_REG	0x0000000006011C00	114
PB.IOE.LL1.IOEL_FIR_WOF_REG	0x0000000006011C08	117
PB.IOE.LL1.IOEL_LAT_MEASURE	0x0000000006011C0E	119
PB.IOE.LL1.IOEL_LINK0_EDPL_STATUS	0x0000000006011C24	126
PB.IOE.LL1.IOEL_LINK0_ERROR_STATUS	0x0000000006011C16	120
PB.IOE.LL1.IOEL_LINK0_INFO	0x0000000006011C14	119
PB.IOE.LL1.IOEL_LINK0_QUALITY	0x0000000006011C26	127
PB.IOE.LL1.IOEL_LINK0_SYN_CAPTURE	0x0000000006011C22	125
PB.IOE.LL1.IOEL_LINK1_EDPL_STATUS	0x0000000006011C25	126
PB.IOE.LL1.IOEL_LINK1_ERROR_STATUS	0x0000000006011C17	121
PB.IOE.LL1.IOEL_LINK1_INFO	0x0000000006011C15	120
PB.IOE.LL1.IOEL_LINK1_QUALITY	0x0000000006011C27	127
PB.IOE.LL1.IOEL_LINK1_SYN_CAPTURE	0x0000000006011C23	125
PB.IOE.LL1.IOEL_PERF_COUNTERS_0	0x0000000006011C1E	124
PB.IOE.LL1.IOEL_PERF_COUNTERS_1	0x0000000006011C1F	124
PB.IOE.LL1.IOEL_PERF_COUNT_LSB_0	0x0000000006011C20	125
PB.IOE.LL1.IOEL_PERF_COUNT_LSB_1	0x0000000006011C21	125
PB.IOE.LL1.IOEL_PERF_SEL_CONFIG	0x0000000006011C1D	124
PB.IOE.LL1.IOEL_PERF_TRACE_CONFIG	0x0000000006011C1C	123
PB.IOE.LL1.IOEL_REPLAY_THRESHOLD	0x0000000006011C18	121
PB.IOE.LL1.IOEL_SEC_CONFIG	0x0000000006011C0D	118

Mnemonic	Address	Page
PB.IOE.LL1.IOEL_SL_ECC_THRESHOLD	0x0000000006011C19	122
PB.IOE.LL2.IOEL_CONFIG	0x000000000601200A	132
PB.IOE.LL2.IOEL_CONTROL	0x000000000601200B	132
PB.IOE.LL2.IOEL_DLL_STATUS	0x0000000006012028	142
PB.IOE.LL2.IOEL_ERR_INJ_LFSR	0x000000000601201B	137
PB.IOE.LL2.IOEL_FIR_ACTION0_REG	0x0000000006012006	131
PB.IOE.LL2.IOEL_FIR_ACTION1_REG	0x0000000006012007	131
PB.IOE.LL2.IOEL_FIR_MASK_REG	0x0000000006012003	129
PB.IOE.LL2.IOEL_FIR_REG	0x0000000006012000	128
PB.IOE.LL2.IOEL_FIR_WOF_REG	0x0000000006012008	131
PB.IOE.LL2.IOEL_LAT_MEASURE	0x000000000601200E	133
PB.IOE.LL2.IOEL_LINK0_EDPL_STATUS	0x0000000006012024	140
PB.IOE.LL2.IOEL_LINK0_ERROR_STATUS	0x0000000006012016	135
PB.IOE.LL2.IOEL_LINK0_INFO	0x0000000006012014	134
PB.IOE.LL2.IOEL_LINK0_QUALITY	0x0000000006012026	141
PB.IOE.LL2.IOEL_LINK0_SYN_CAPTURE	0x0000000006012022	139
PB.IOE.LL2.IOEL_LINK1_EDPL_STATUS	0x0000000006012025	141
PB.IOE.LL2.IOEL_LINK1_ERROR_STATUS	0x0000000006012017	135
PB.IOE.LL2.IOEL_LINK1_INFO	0x0000000006012015	134
PB.IOE.LL2.IOEL_LINK1_QUALITY	0x0000000006012027	142
PB.IOE.LL2.IOEL_LINK1_SYN_CAPTURE	0x0000000006012023	140
PB.IOE.LL2.IOEL_PERF_COUNTERS_0	0x000000000601201E	138
PB.IOE.LL2.IOEL_PERF_COUNTERS_1	0x000000000601201F	139
PB.IOE.LL2.IOEL_PERF_COUNT_LSB_0	0x0000000006012020	139
PB.IOE.LL2.IOEL_PERF_COUNT_LSB_1	0x0000000006012021	139
PB.IOE.LL2.IOEL_PERF_SEL_CONFIG	0x000000000601201D	138
PB.IOE.LL2.IOEL_PERF_TRACE_CONFIG	0x000000000601201C	137
PB.IOE.LL2.IOEL_REPLAY_THRESHOLD	0x0000000006012018	136
PB.IOE.LL2.IOEL_SEC_CONFIG	0x000000000601200D	133
PB.IOE.LL2.IOEL_SL_ECC_THRESHOLD	0x0000000006012019	136
TP.TCXB.XB.BIST	0x000000000603000B	151
TP.TCXB.XB.CC_ATOMIC_LOCK_REG	0x00000000060303FF	160
TP.TCXB.XB.CC_PROTECT_MODE_REG	0x00000000060303FE	160
TP.TCXB.XB.CLK_REGION	0x0000000006030006	148
TP.TCXB.XB.CLOCK_STAT_ARY	0x000000000603000A	150
TP.TCXB.XB.CLOCK_STAT_NSL	0x0000000006030009	149
TP.TCXB.XB.CLOCK_STAT_SL	0x0000000006030008	148
TP.TCXB.XB.CPLT_CONF0	0x0000000006000008	49
TP.TCXB.XB.CPLT_CONF1	0x0000000006000009	50
TP.TCXB.XB.CPLT_CTRL0	0x0000000006000000	46
TP.TCXB.XB.CPLT_CTRL1	0x0000000006000001	48
TP.TCXB.XB.CPLT_MASK0	0x0000000006000101	52
TP.TCXB.XB.CPLT_STAT0	0x0000000006000100	51
TP.TCXB.XB.CTRL_ATOMIC_LOCK_REG	0x00000000060003FF	52
TP.TCXB.XB.CTRL_PROTECT_MODE_REG	0x00000000060003FE	52
TP.TCXB.XB.DBG_CBS_CC	0x0000000006030013	159
TP.TCXB.XB.EPS.DBG.DBG_INST1_COND_REG_1	0x00000000060107C1	68
TP.TCXB.XB.EPS.DBG.DBG_INST1_COND_REG_2	0x00000000060107C2	71

Mnemonic	Address	Page
TP.TCXB.XB.EPS.DBG.DBG_INST1_COND_REG_3	0x00000000060107C3	72
TP.TCXB.XB.EPS.DBG.DBG_INST2_COND_REG_1	0x00000000060107C4	72
TP.TCXB.XB.EPS.DBG.DBG_INST2_COND_REG_2	0x00000000060107C5	74
TP.TCXB.XB.EPS.DBG.DBG_INST2_COND_REG_3	0x00000000060107C6	75
TP.TCXB.XB.EPS.DBG.DBG_MODE_REG	0x00000000060107C0	67
TP.TCXB.XB.EPS.DBG.DBG_TRACE_MODE_REG_2	0x00000000060107CF	79
TP.TCXB.XB.EPS.DBG.DBG_TRACE_REG_0	0x00000000060107CD	76
TP.TCXB.XB.EPS.DBG.DBG_TRACE_REG_1	0x00000000060107CE	77
TP.TCXB.XB.EPS.DBG.DEBUG_TRACE_CONTROL	0x00000000060107D0	79
TP.TCXB.XB.EPS.DBG.XTRA_TRACE_MODE	0x00000000060107D1	80
TP.TCXB.XB.EPS.FIR.GXSTOP0_MASK_REG	0x0000000006040014	167
TP.TCXB.XB.EPS.FIR.GXSTOP1_MASK_REG	0x0000000006040015	167
TP.TCXB.XB.EPS.FIR.GXSTOP2_MASK_REG	0x0000000006040016	168
TP.TCXB.XB.EPS.FIR.GXSTOP_TRIG_REG	0x0000000006040013	166
TP.TCXB.XB.EPS.FIR.LOCAL_FIR_ACTION0	0x0000000006040010	166
TP.TCXB.XB.EPS.FIR.LOCAL_FIR_ACTION1	0x0000000006040011	166
TP.TCXB.XB.EPS.FIR.LOCAL_FIR_MASK	0x000000000604000D	165
TP.TCXB.XB.EPS.FIR.MODE_REG	0x0000000006040008	163
TP.TCXB.XB.EPS.FIR.SUM_MASK_REG	0x0000000006040017	168
TP.TCXB.XB.EPS.PSC.PSC.ADDR_TRAP_REG	0x0000000006010003	55
TP.TCXB.XB.EPS.PSC.PSC.ATOMIC_LOCK_MASK_LATCH_REG	0x0000000006010007	56
TP.TCXB.XB.EPS.PSC.PSC.PSCOM_ERROR_MASK	0x0000000006010002	54
TP.TCXB.XB.EPS.PSC.PSC.PSCOM_MODE_REG	0x0000000006010000	52
TP.TCXB.XB.EPS.PSC.PSC.PSCOM_STATUS_ERROR_REG	0x0000000006010001	53
TP.TCXB.XB.EPS.PSC.PSC.RING_FENCE_MASK_LATCH_REG	0x0000000006010008	56
TP.TCXB.XB.EPS.PSC.PSC.WRITE_PROTECT_ENABLE_REG	0x0000000006010005	55
TP.TCXB.XB.EPS.PSC.PSC.WRITE_PROTECT_RINGS_REG	0x0000000006010006	55
TP.TCXB.XB.EPS.THERM.CONTROL_REG	0x0000000006050012	172
TP.TCXB.XB.EPS.THERM.DTS_RESULT0	0x0000000006050000	170
TP.TCXB.XB.EPS.THERM.DTS_TRC_RESULT	0x0000000006050003	170
TP.TCXB.XB.EPS.THERM.ERR_STATUS_REG	0x0000000006050013	173
TP.TCXB.XB.EPS.THERM.INJECT_REG	0x0000000006050011	172
TP.TCXB.XB.EPS.THERM.SKITTER_CLKSRC_REG	0x0000000006050016	174
TP.TCXB.XB.EPS.THERM.SKITTER_DATA0	0x0000000006050019	175
TP.TCXB.XB.EPS.THERM.SKITTER_DATA1	0x000000000605001A	175
TP.TCXB.XB.EPS.THERM.SKITTER_DATA2	0x000000000605001B	175
TP.TCXB.XB.EPS.THERM.SKITTER_FORCE_REG	0x0000000006050014	174
TP.TCXB.XB.EPS.THERM.SKITTER_MODE_REG	0x0000000006050010	171
TP.TCXB.XB.EPS.THERM.THERM_MODE_REG	0x000000000605000F	170
TP.TCXB.XB.EPS.THERM.TIMESTAMP_COUNTER_READ	0x000000000605001C	176
TP.TCXB.XB.ERROR_STATUS	0x000000000603000F	155
TP.TCXB.XB.FIR_MASK	0x0000000006040002	162
TP.TCXB.XB.HOSTATTN	0x0000000006040009	163
TP.TCXB.XB.HOSTATTN_MASK	0x000000000604001A	169
TP.TCXB.XB.LOCAL_FIR	0x000000000604000A	164
TP.TCXB.XB.LOCAL_XSTOP_ERR	0x0000000006040018	168
TP.TCXB.XB.LOCAL_XSTOP_MASK	0x0000000006040019	169
TP.TCXB.XB.OPCG_ALIGN	0x0000000006030001	144

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TP.TCXB.XB.OPCG_CAPT1	0x0000000006030010	157
TP.TCXB.XB.OPCG_CAPT2	0x0000000006030011	158
TP.TCXB.XB.OPCG_CAPT3	0x0000000006030012	158
TP.TCXB.XB.OPCG_REG0	0x0000000006030002	145
TP.TCXB.XB.OPCG_REG1	0x0000000006030003	146
TP.TCXB.XB.OPCG_REG2	0x0000000006030004	146
TP.TCXB.XB.RFIR	0x0000000006040001	161
TP.TCXB.XB.SCAN_REGION_TYPE	0x0000000006030005	147
TP.TCXB.XB.SPATTN	0x0000000006040004	162
TP.TCXB.XB.SPA_MASK	0x0000000006040007	163
TP.TCXB.XB.SYNC_CONFIG	0x0000000006030000	142
TP.TCXB.XB.TRA0.TR0.TRACE_HI_DATA_REG	0x0000000006010400	56
TP.TCXB.XB.TRA0.TR0.TRACE_LO_DATA_REG	0x0000000006010401	56
TP.TCXB.XB.TRA0.TR0.TRACE_TRCTRL_CONFIG	0x0000000006010402	57
TP.TCXB.XB.TRA0.TR0.TRACE_TRDATA_CONFIG_0	0x0000000006010403	57
TP.TCXB.XB.TRA0.TR0.TRACE_TRDATA_CONFIG_1	0x0000000006010404	57
TP.TCXB.XB.TRA0.TR0.TRACE_TRDATA_CONFIG_2	0x0000000006010405	58
TP.TCXB.XB.TRA0.TR0.TRACE_TRDATA_CONFIG_3	0x0000000006010406	58
TP.TCXB.XB.TRA0.TR0.TRACE_TRDATA_CONFIG_4	0x0000000006010407	58
TP.TCXB.XB.TRA0.TR0.TRACE_TRDATA_CONFIG_5	0x0000000006010408	58
TP.TCXB.XB.TRA0.TR0.TRACE_TRDATA_CONFIG_9	0x0000000006010409	58
TP.TCXB.XB.TRA0.TR1.TRACE_HI_DATA_REG	0x0000000006010440	60
TP.TCXB.XB.TRA0.TR1.TRACE_LO_DATA_REG	0x0000000006010441	60
TP.TCXB.XB.TRA0.TR1.TRACE_TRCTRL_CONFIG	0x0000000006010442	60
TP.TCXB.XB.TRA0.TR1.TRACE_TRDATA_CONFIG_0	0x0000000006010443	61
TP.TCXB.XB.TRA0.TR1.TRACE_TRDATA_CONFIG_1	0x0000000006010444	61
TP.TCXB.XB.TRA0.TR1.TRACE_TRDATA_CONFIG_2	0x0000000006010445	61
TP.TCXB.XB.TRA0.TR1.TRACE_TRDATA_CONFIG_3	0x0000000006010446	61
TP.TCXB.XB.TRA0.TR1.TRACE_TRDATA_CONFIG_4	0x0000000006010447	62
TP.TCXB.XB.TRA0.TR1.TRACE_TRDATA_CONFIG_5	0x0000000006010448	62
TP.TCXB.XB.TRA0.TR1.TRACE_TRDATA_CONFIG_9	0x0000000006010449	62
TP.TCXB.XB.TRA1.TR0.TRACE_HI_DATA_REG	0x0000000006010480	64
TP.TCXB.XB.TRA1.TR0.TRACE_LO_DATA_REG	0x0000000006010481	64
TP.TCXB.XB.TRA1.TR0.TRACE_TRCTRL_CONFIG	0x0000000006010482	64
TP.TCXB.XB.TRA1.TR0.TRACE_TRDATA_CONFIG_0	0x0000000006010483	65
TP.TCXB.XB.TRA1.TR0.TRACE_TRDATA_CONFIG_1	0x0000000006010484	65
TP.TCXB.XB.TRA1.TR0.TRACE_TRDATA_CONFIG_2	0x0000000006010485	65
TP.TCXB.XB.TRA1.TR0.TRACE_TRDATA_CONFIG_3	0x0000000006010486	65
TP.TCXB.XB.TRA1.TR0.TRACE_TRDATA_CONFIG_4	0x0000000006010487	65
TP.TCXB.XB.TRA1.TR0.TRACE_TRDATA_CONFIG_5	0x0000000006010488	66
TP.TCXB.XB.TRA1.TR0.TRACE_TRDATA_CONFIG_9	0x0000000006010489	66
TP.TCXB.XB.XFIR	0x0000000006040000	161
TP.TCXB.XB.XSTOP1	0x000000000603000C	152
TP.TCXB.XB.XSTOP2	0x000000000603000D	153
TP.TCXB.XB.XSTOP3	0x000000000603000E	154

The POWER9 processor registers are listed in the following tables.

Register Name	**Chiplet Control Register 0**
Mnemonic	TP.TCXB.XB.CPLT_CTRL0
Address	0000000006000000 (SCOM) 0000000006000010 (SCOM1) 0000000006000020 (SCOM2)
Description	This register contains the first set of vital chiplet controls.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_OR	WO_CLEAR	CTRL_CC_ABSTCLK_MUXSEL_DC: Select the ABIST clock source for arrays on a chiplet boundary. When set to 1, clocks are used from a chiplet with ABIST.
1	RW	WO_OR	WO_CLEAR	TC_UNIT_SYNCCLK_MUXSEL_DC: Select the synchronous clock for asynchronous latches. (The initial value is 1.)
2	RW	WO_OR	WO_CLEAR	CTRL_CC_FLUSHMODE_INH_DC: Prevent pipeline latches from going into flush mode. (The initial value is 1.)
3	RW	WO_OR	WO_CLEAR	CTRL_CC_FORCE_ALIGN_DC: Force an alignment signal to be sent. (The initial value is 1. Drop before dropping flushmode_inh.)
4	RW	WO_OR	WO_CLEAR	TC_UNIT_ARY_WRT_THRU_DC: Set the array into write-through mode. Used for LBIST.
5	RW	WO_OR	WO_CLEAR	TC_UNIT_AVP_MODE: AVP mode. Switches from refresh pulse to phase counter.
6	RW	WO_OR	WO_CLEAR	FREE_USAGE_6A: Free usage.
7	RW	WO_OR	WO_CLEAR	FREE_USAGE_7A: Free usage.
8	RW	WO_OR	WO_CLEAR	CTRL_CC_ABIST_RECOV_DISABLE_DC: New signal to disable recovery.
9	RW	WO_OR	WO_CLEAR	FREE_USAGE_9A: Free usage.
10	RW	WO_OR	WO_CLEAR	TC_UNIT_IOBIST_TX_WRAP_ENABLE_DC:
11	RW	WO_OR	WO_CLEAR	RESERVED_11A: Reserved.
12	RW	WO_OR	WO_CLEAR	TC_SKIT_MODE_BIST_DC:
13	RW	WO_OR	WO_CLEAR	TC_UNIT_DETERMINISTIC_TEST_ENABLE_DC: Forces login into deterministic test mode. For example, for LBIST.
14	RW	WO_OR	WO_CLEAR	TC_UNIT_CONSTRAIN_SAFESCAN_DC: Safe scan of the N1L latches. Prevent a lock when switching the SE.
15	RW	WO_OR	WO_CLEAR	TC_UNIT_RRFA_TEST_ENABLE_DC:
16	RW	WO_OR	WO_CLEAR	TC_NBTI_HDR_ENABLE_OVR_DC: NBTI.
17	RW	WO_OR	WO_CLEAR	TC_NBTI_PROBE_GATE_DC: NBTI.
18	RW	WO_OR	WO_CLEAR	RESERVED_18A: Reserved.
19	RW	WO_OR	WO_CLEAR	RESERVED_19A: Reserved.
20:27	RW	WO_OR	WO_CLEAR	TC_PSRO_SEL_DC: PSRO select.
28	RW	WO_OR	WO_CLEAR	TC_BSC_WRAPSEL_DC: Wrap select for BSC.
29	RW	WO_OR	WO_CLEAR	TC_BSC_INTMODE_DC: INT mode for BSC.
30	RW	WO_OR	WO_CLEAR	TC_BSC_INV_DC: INV for BSC mode.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
31	RW	WO_OR	WO_CLEAR	TC_BSC_EXTMODE_DC: EXT mode for BSC.
32	RW	WO_OR	WO_CLEAR	TC_REFCLK_DRVR_EN_DC: Reference clock driver enable.
33	RW	WO_OR	WO_CLEAR	RESERVED_33A: Reserved.
34	RW	WO_OR	WO_CLEAR	RESERVED_34A: Reserved.
35	RW	WO_OR	WO_CLEAR	RESERVED_35A: Reserved.
36	RW	WO_OR	WO_CLEAR	TC_OELCC_EDGE_DELAYED_DC: Enables delaying the alignment by one fast cycle. Only used in dual mesh chiplets.
37	RW	WO_OR	WO_CLEAR	TC_OELCC_ALIGN_FLUSH_DC: Forces the alignment and odd/even toggling latch into a flush state. For DFT only.
38	RW	WO_OR	WO_CLEAR	RESERVED_38A: Reserved.
39	RW	WO_OR	WO_CLEAR	RESERVED_39A: Reserved.
40:41	RW	WO_OR	WO_CLEAR	CTRL_MISC_CLKDIV_SEL_DC: Clock divider select. 00 = 1024:1 01 = 64:1 10 = 16:1 11 = 4:1
42	RW	WO_OR	WO_CLEAR	RESERVED_42A: Reserved.
43	RW	WO_OR	WO_CLEAR	RESERVED_43A: Reserved.
44	RW	WO_OR	WO_CLEAR	CTRL_CC_DCTEST_DC: TE = 1 only. Enable DCTEST.
45	RW	WO_OR	WO_CLEAR	CTRL_CC_OTP_PRGMODE_DC: TE = 1 only. OTP ROM program mode
46	RW	WO_OR	WO_CLEAR	CTRL_CC_SSS_CALIBRATE_DC: TE = 1 only. Sensors calibration.
47	RW	WO_OR	WO_CLEAR	CTRL_CC_PIN_LBIST_DC: TE = 1 only. PIN LBIST mode. The LBIST is controlled by the pin, not by the OPCG.
48	RW	WO_OR	WO_CLEAR	FREE_USAGE_48A: Free usage.
49	RW	WO_OR	WO_CLEAR	FREE_USAGE_49A: Free usage.
50	RW	WO_OR	WO_CLEAR	FREE_USAGE_50A: Free usage.
51	RW	WO_OR	WO_CLEAR	FREE_USAGE_51A: Free usage.
52	RW	WO_OR	WO_CLEAR	FREE_USAGE_52A: Free usage.
53	RW	WO_OR	WO_CLEAR	FREE_USAGE_53A: Free usage.
54	RW	WO_OR	WO_CLEAR	FREE_USAGE_54A: Free usage.
55	RW	WO_OR	WO_CLEAR	FREE_USAGE_55A: Free usage.
56	RW	WO_OR	WO_CLEAR	FREE_USAGE_56A: Free usage.
57	RW	WO_OR	WO_CLEAR	FREE_USAGE_57A: Free usage.
58	RW	WO_OR	WO_CLEAR	FREE_USAGE_58A: Free usage.
59	RW	WO_OR	WO_CLEAR	FREE_USAGE_59A: Free usage.
60	RW	WO_OR	WO_CLEAR	FREE_USAGE_60A: Free usage.
61	RW	WO_OR	WO_CLEAR	FREE_USAGE_61A: Free usage.
62	RW	WO_OR	WO_CLEAR	FREE_USAGE_62A: Free usage.
63	RW	WO_OR	WO_CLEAR	FREE_USAGE_63A: Free usage.

Register Name	Chiplet Control Register 1
Mnemonic	TP.TCXB.XB.CPLT_CTRL1
Address	0000000006000001 (SCOM) 0000000006000011 (SCOM1) 0000000006000021 (SCOM2)
Description	This register contains the second set of vital chiplet controls.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_OR	WO_CLEAR	UNUSED_0B: Unused.
1	RW	WO_OR	WO_CLEAR	UNUSED_1B: Unused.
2	RW	WO_OR	WO_CLEAR	UNUSED_2B: Unused.
3	RW	WO_OR	WO_CLEAR	TC_VITL_REGION_FENCE: VITL fence. Protect the VITL region logic from pollution by other regions during LBIST, or when the chiplet is not initialized and running yet.
4	RW	WO_OR	WO_CLEAR	TC_PERV_REGION_FENCE: Fence for the pervasive region.
5	RW	WO_OR	WO_CLEAR	TC_REGION1_FENCE: Fence for regions iox0 - iof.
6	RW	WO_OR	WO_CLEAR	TC_REGION2_FENCE: Fence for regions iox1 - iof.
7	RW	WO_OR	WO_CLEAR	TC_REGION3_FENCE: Fence for regions iox2 - iof.
8	RW	WO_OR	WO_CLEAR	TC_REGION4_FENCE: Fence for regions ioppe - iof.
9	RW	WO_OR	WO_CLEAR	TC_REGION5_FENCE: Fence for regions pbiox0 - pb.
10	RW	WO_OR	WO_CLEAR	TC_REGION6_FENCE: Fence for regions pbiox1 - pb.
11	RW	WO_OR	WO_CLEAR	TC_REGION7_FENCE: Fence for regions pbiox2 - pb.
12	RW	WO_OR	WO_CLEAR	UNUSED_12B: Unused.
13	RW	WO_OR	WO_CLEAR	UNUSED_13B: Unused.
14	RW	WO_OR	WO_CLEAR	UNUSED_14B: Unused.
15	RW	WO_OR	WO_CLEAR	RESERVED: Reserved.
16	RW	WO_OR	WO_CLEAR	TC_UNIT_MULTICYCLE_TEST_FENCE:
17	RW	WO_OR	WO_CLEAR	UNUSED_17B: Unused.
18	RW	WO_OR	WO_CLEAR	UNUSED_18B: Unused.
19	RW	WO_OR	WO_CLEAR	UNUSED_19B: Unused.
20	RW	WO_OR	WO_CLEAR	UNUSED_20B: Unused.
21	RW	WO_OR	WO_CLEAR	UNUSED_21B: Unused.
22	RW	WO_OR	WO_CLEAR	UNUSED_22B: Unused.
23	RW	WO_OR	WO_CLEAR	UNUSED_23B: Unused.
24	RW	WO_OR	WO_CLEAR	UNUSED_24B: Unused.
25	RW	WO_OR	WO_CLEAR	UNUSED_25B: Unused.
26	RW	WO_OR	WO_CLEAR	UNUSED_26B: Unused.
27	RW	WO_OR	WO_CLEAR	UNUSED_27B: Unused.
28	RW	WO_OR	WO_CLEAR	UNUSED_28B: Unused.
29	RW	WO_OR	WO_CLEAR	UNUSED_29B: Unused.
30	RW	WO_OR	WO_CLEAR	UNUSED_30B: Unused.
31	RW	WO_OR	WO_CLEAR	UNUSED_31B: Unused.

Register Name	Chiplet Configuration Register 0
Mnemonic	TP.TCXB.XB.CPLT_CONF0
Address	0000000006000008 (SCOM) 0000000006000018 (SCOM1) 0000000006000028 (SCOM2)
Description	This register contains the first set of vital chiplet configuration functions.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:5	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE0_SEL_DC: Probe 0 select.
6	RW	WO_OR	WO_CLEAR	RESERVED_6C: Reserved.
7	RW	WO_OR	WO_CLEAR	RESERVED_7C: Reserved.
8:13	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE1_SEL_DC: Probe 1 select.
14	RW	WO_OR	WO_CLEAR	RESERVED_14C: Reserved.
15	RW	WO_OR	WO_CLEAR	RESERVED_15C: Reserved.
16:21	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE2_SEL_DC: Probe 2 select.
22	RW	WO_OR	WO_CLEAR	RESERVED_22C: Reserved.
23	RW	WO_OR	WO_CLEAR	RESERVED_23C: Reserved.
24:29	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE3_SEL_DC: Probe 3 select.
30	RW	WO_OR	WO_CLEAR	RESERVED_30C: Reserved.
31	RW	WO_OR	WO_CLEAR	RESERVED_31C: Reserved.
32	RW	WO_OR	WO_CLEAR	CTRL_CC_OFLOW_FEH_SEL_DC: ABIST overflow/failure indication select.
33	RW	WO_OR	WO_CLEAR	CTRL_CC_SCAN_PROTECT_DC: Enables scan protection. Enables the scan collision error mechanism.
34	RW	WO_OR	WO_CLEAR	CTRL_CC_SDIS_DC_N: Disables the scan diagnostic scan path.
35	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_35C: Reserved for test control.
36	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_36C: Reserved for test control.
37	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_37C: Reserved for test control.
38	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_38C: Reserved for test control.
39	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_39C: Reserved for test control.
40	RW	WO_OR	WO_CLEAR	CTRL_EPS_MASK_VITL_PCB_ERR_DC: Mask VITL PCB errors from CC or CPLT_CTRL.
41	RW	WO_OR	WO_CLEAR	CTRL_CC_MASK_VITL_SCAN_OPCG_ERR_DC: Mask VITL errors in CC that are not PCB related.
42	RW	WO_OR	WO_CLEAR	RESERVED_42C: Reserved.
43	RW	WO_OR	WO_CLEAR	RESERVED_43C: Reserved.
44	RW	WO_OR	WO_CLEAR	FREE_USAGE_44C: Free usage.
45	RW	WO_OR	WO_CLEAR	FREE_USAGE_45C: Free usage.
46	RW	WO_OR	WO_CLEAR	FREE_USAGE_46C: Free usage.
47	RW	WO_OR	WO_CLEAR	FREE_USAGE_47C: Free usage.
48:51	RW	WO_OR	WO_CLEAR	TC_UNIT_GROUP_ID_DC: Group ID.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
52:54	RW	WO_OR	WO_CLEAR	TC_UNIT_CHIP_ID_DC: Chip ID.
55	RW	WO_OR	WO_CLEAR	RESERVED_ID_55C: Reserved ID.
56:60	RW	WO_OR	WO_CLEAR	TC_UNIT_SYS_ID_DC: System ID.
61	RW	WO_OR	WO_CLEAR	RESERVED_ID_61C: Reserved ID.
62	RW	WO_OR	WO_CLEAR	RESERVED_ID_62C: Reserved ID.
63	RW	WO_OR	WO_CLEAR	RESERVED_ID_63C: Reserved ID.

Register Name	Chiplet Configuration Register 1
Mnemonic	TP.TCXB.XB.CPLT_CONF1
Address	0000000006000009 (SCOM) 0000000006000019 (SCOM1) 0000000006000029 (SCOM2)
Description	This register contains the second set of vital chiplet configuration functions.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:2	RW	WO_OR	WO_CLEAR	TC_IOX_MUX_VSEL: Analog multiplexer (AMux) control.
3	RW	WO_OR	WO_CLEAR	UNUSED: Unused.
4	RW	WO_OR	WO_CLEAR	TC_PBE0_IOVALID_DC:
5	RW	WO_OR	WO_CLEAR	TC_PBE1_IOVALID_DC:
6	RW	WO_OR	WO_CLEAR	TC_PBE2_IOVALID_DC:
7	RW	WO_OR	WO_CLEAR	TC_PBE3_IOVALID_DC:
8	RW	WO_OR	WO_CLEAR	TC_PBE4_IOVALID_DC:
9	RW	WO_OR	WO_CLEAR	TC_PBE5_IOVALID_DC:
10	RW	WO_OR	WO_CLEAR	IOVALID_10D:
11	RW	WO_OR	WO_CLEAR	IOVALID_11D:
12	RW	WO_OR	WO_CLEAR	FREE_USAGE_12D: Free usage.
13	RW	WO_OR	WO_CLEAR	FREE_USAGE_13D: Free usage.
14	RW	WO_OR	WO_CLEAR	FREE_USAGE_14D: Free usage.
15	RW	WO_OR	WO_CLEAR	FREE_USAGE_15D: Free usage.
16	RW	WO_OR	WO_CLEAR	FREE_USAGE_16D: Free usage.
17	RW	WO_OR	WO_CLEAR	FREE_USAGE_17D: Free usage.
18	RW	WO_OR	WO_CLEAR	FREE_USAGE_18D: Free usage.
19	RW	WO_OR	WO_CLEAR	FREE_USAGE_19D: Free usage.
20	RW	WO_OR	WO_CLEAR	FREE_USAGE_20D: Free usage.
21	RW	WO_OR	WO_CLEAR	FREE_USAGE_21D: Free usage.
22	RW	WO_OR	WO_CLEAR	FREE_USAGE_22D: Free usage.
23	RW	WO_OR	WO_CLEAR	FREE_USAGE_23D: Free usage.
24	RW	WO_OR	WO_CLEAR	FREE_USAGE_24D: Free usage.
25	RW	WO_OR	WO_CLEAR	FREE_USAGE_25D: Free usage.
26	RW	WO_OR	WO_CLEAR	FREE_USAGE_26D: Free usage.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
27	RW	WO_OR	WO_CLEAR	FREE_USAGE_27D: Free usage.
28	RW	WO_OR	WO_CLEAR	FREE_USAGE_28D: Free usage.
29	RW	WO_OR	WO_CLEAR	FREE_USAGE_29D: Free usage.
30	RW	WO_OR	WO_CLEAR	FREE_USAGE_30D: Free usage.
31	RW	WO_OR	WO_CLEAR	FREE_USAGE_31D: Free usage.

Register Name	Chiplet Status Register
Mnemonic	TP.TCXB.XB.CPLT_STAT0
Address	0000000006000100 (SCOM)
Description	An interrupt is sent out on a bit change if not masked by the Chiplet Mask Register. A mask only masks the interrupt, *not* the status register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	SRAM_ABIST_DONE_DC: SRAM and eDRAM ABIST done.
1	ROX	DRAM_ABIST_DONE_DC: Unused in POWER9 DD1.
2	ROX	RESERVED_2E: Reserved.
3	ROX	RESERVED_3E: Reserved.
4	ROX	TC_DIAG_PORT0_OUT: Diagnostic output port.
5	ROX	TC_DIAG_PORT1_OUT: Diagnostic output port.
6	ROX	RESERVED_6E: Reserved.
7	ROX	PLL_DESTOUT: Reserved.
8	ROX	CC_CTRL_OPCG_DONE_DC: OPCG done. For LBIST, ABIST, or other OPCG runs.
9	ROX	CC_CTRL_CHIPLET_IS_ALIGNED_DC: Indicates that the chiplet is aligned.
10	ROX	FREE_USAGE_10E: Free usage.
11	ROX	FREE_USAGE_11E: Free usage.
12	ROX	FREE_USAGE_12E: Free usage.
13	ROX	FREE_USAGE_13E: Free usage.
14	ROX	FREE_USAGE_14E: Free usage.
15	ROX	FREE_USAGE_15E: Free usage.
16	ROX	FREE_USAGE_16E: Free usage.
17	ROX	FREE_USAGE_17E: Free usage.
18	ROX	FREE_USAGE_18E: Free usage.
19	ROX	FREE_USAGE_19E: Free usage.
20	ROX	FREE_USAGE_20E: Free usage.
21	ROX	FREE_USAGE_21E: Free usage.
22	ROX	FREE_USAGE_22E: Free usage.
23	ROX	FREE_USAGE_23E: Free usage.

Register Name	Chiplet Mask Register
Mnemonic	TP.TCXB.XB.CPLT_MASK0
Address	0000000006000101 (SCOM)
Description	This register masks an interrupt when a bit changes in the Chiplet Status Register. It does *not* mask the status itself.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CPLTMASK0: This field provides bitwise masking of the Chiplet Status Register.

Register Name	Control Protect Mode Register
Mnemonic	TP.TCXB.XB.CTRL_PROTECT_MODE_REG
Address	00000000060003FE (SCOM)
Description	This register enables read and write protection.

Bits	SCOM	Field Mnemonic: Description
0	RW	CTRL_READ_PROTECT_ENABLE: This bit enables read protection.
1	RW	CTRL_WRITE_PROTECT_ENABLE: This bit enables write protection.

Register Name	Atomic Lock Register
Mnemonic	TP.TCXB.XB.CTRL_ATOMIC_LOCK_REG
Address	00000000060003FF (SCOM)
Description	This register enables an atomic lock and an atomic lock counter.

Bits	SCOM	Field Mnemonic: Description
0	RW	CTRL_ATOMIC_LOCK_ENABLE: This bit enables an atomic lock.
1:4	ROX	CTRL_ATOMIC_ID: This field contains the atomic ID.
5:7	RO	constant = 0b000
8:15	ROX	CTRL_ATOMIC_ACTIVITY: This field is an atomic lock counter.

Register Name	PSCOMLE Mode Register
Mnemonic	TP.TCXB.XB.EPS.PSC.PSC.PSCOM_MODE_REG
Address	0000000006010000 (SCOM)
Description	This is the parallel-to-serial communication light edition (PSCOMLE) mode register.

Bits	SCOM	Field Mnemonic: Description
0	RW	ABORT_ON_PCB_ADDR_PARITY_ERROR: Abort on a PCB address parity error.
1	RW	ABORT_ON_PCB_WDATA_PARITY_ERROR: Abort on a PCB write data parity error.
2	RW	UNUSED_2B. Unused.
3	RW	ABORT_ON_DL_RETURN_WDATA_PARITY_ERROR: Abort on a DL return write data parity error.
4	RW	WATCHDOG_ENABLE: Watchdog enable.

Bits	SCOM	Field Mnemonic: Description
5:6	RW	SCOM_HANG_LIMIT: 0b11 = 256 0b10 = 512 0b01 = 768 0b00 = 1023
7	RW	FORCE_ALL_RINGS: This bit is set to a logical 1 if all rings must be enabled independent of the ring address.
8	RW	FSM_SELFRESET_ON_STATEVEC_PARITYERROR_ENABLE: FSM self reset on statevec parity error enable.
9:11	RW	RESERVED_PSCOM_MODE_LT: Reserved.

Register Name	PSCOMLE Error Register
Mnemonic	TP.TCXB.XB.EPS.PSC.PSC.PSCOM_STATUS_ERROR_REG
Address	0000000006010001 (SCOM)
Description	This is the parallel-to-serial communication light edition (PSCOMLE) error register.

Bits	SCOM	Field Mnemonic: Description
0	RWX	ACCUMULATED_PCB_WDATA_PARITY_ERROR: Accumulated PCB write data parity error.
1	RWX	ACCUMULATED_PCB_ADDRESS_PARITY_ERROR: Accumulated PCB address parity error.
2	RWX	ACCUMULATED_DL_RETURN_WDATA_PARITY_ERROR: Accumulated DL return write data parity error.
3	RWX	ACCUMULATED_DL_RETURN_P0_ERROR: Accumulated DL return P0 error.
4	RWX	ACCUMULATED_UL_RDATA_PARITY_ERROR: Accumulated UL read data parity error.
5	RWX	ACCUMULATED_UL_P0_ERROR: Accumulated UL P0 error.
6	RWX	ACCUMULATED_PARITY_ERROR_ON_INTERFACE_MACHINE: Accumulated parity error on interface machine.
7	RWX	ACCUMULATED_PARITY_ERROR_ON_P2S_MACHINE: Accumulated parity error on p2s machine.
8	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_ULCCH: Accumulated timeout while waiting for ULCCH.
9	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: Accumulated timeout while waiting for DLDCH return.
10	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_ULDCH: Accumulated timeout while waiting for ULDCH.
11	RWX	ACCUMULATED_PSCOM_PARALLEL_WRITE_NVLD: Accumulated PSCOM parallel write NVLD.
12	RWX	ACCUMULATED_PSCOM_PARALLEL_READ_NVLD: Accumulated PSCOM parallel read NVLD.
13	RWX	ACCUMULATED_PSCOM_PARALLEL_ADDR_INVALID: Accumulated PSCOM parallel address invalid.
14	RWX	ACCUMULATED_PCB_COMMAND_PARITY_ERROR: Accumulated PCB command parity error.
15	RWX	ACCUMULATED_GENERAL_TIMEOUT: Accumulated general timeout.
16	RWX	ACCUMULATED_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: Accumulated satellite acknowledge access violation.
17	RWX	ACCUMULATED_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: Accumulated satellite acknowledge invalid register.
18	RWX	TRAPPED_PCB_WDATA_PARITY_ERROR: Trapped PCB write data parity error.
19	RWX	TRAPPED_PCB_ADDRESS_PARITY_ERROR: Trapped PCB address parity error.

Bits	SCOM	Field Mnemonic: Description
20	RWX	TRAPPED_DL_RETURN_WDATA_PARITY_ERROR: Trapped DL return write data parity error.
21	RWX	TRAPPED_DL_RETURN_P0_ERROR: Trapped DL return P0 error.
22	RWX	TRAPPED_UL_RDATA_PARITY_ERROR: Trapped UL read data parity error.
23	RWX	TRAPPED_UL_P0_ERROR: Trapped UL P0 error.
24	RWX	TRAPPED_PARITY_ERROR_ON_INTERFACE_MACHINE: Trapped parity error on interface machine.
25	RWX	TRAPPED_PARITY_ERROR_ON_P2S_MACHINE: Trapped parity error on p2s machine.
26	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_ULCCH: Trapped timeout while waiting for ULCCH.
27	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: Trapped timeout while waiting for DLDCH return.
28	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_ULDCH: Trapped timeout while waiting for ULDCH.
29	RWX	TRAPPED_PSCOM_PARALLEL_WRITE_NVLD: Trapped PSCOM parallel write NVLD.
30	RWX	TRAPPED_PSCOM_PARALLEL_READ_NVLD: Trapped PSCOM parallel read NVLD.
31	RWX	TRAPPED_PSCOM_PARALLEL_ADDR_INVALID: Trapped PSCOM parallel address invalid.
32	RWX	TRAPPED_PCB_COMMAND_PARITY_ERROR: Trapped PCB command parity error.
33	RWX	TRAPPED_GENERAL_TIMEOUT: Trapped general timeout.
34	RWX	TRAPPED_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: Trapped satellite acknowledge access violation.
35	RWX	TRAPPED_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: Trapped satellite acknowledge invalid register.

Register Name	PSCOMLE Error Mask Register
Mnemonic	TP.TCXB.XB.EPS.PSC.PSC.PSCOM_ERROR_MASK
Address	0000000006010002 (SCOM)
Description	This is the parallel-to-serial communication light edition (PSCOMLE) error mask register.

Bits	SCOM	Field Mnemonic: Description
0	RW	MASK_PCB_WDATA_PARITY_ERROR: Mask PCB write data parity error.
1	RW	MASK_PCB_ADDRESS_PARITY_ERROR: Mask PCB address parity error.
2	RW	MASK_DL_RETURN_WDATA_PARITY_ERROR: Mask DL return write data parity error.
3	RW	MASK_DL_RETURN_P0_ERROR: Mask DL return P0 error.
4	RW	MASK_UL_RDATA_PARITY_ERROR: Mask UL read data parity error.
5	RW	MASK_UL_P0_ERROR: Mask UL P0 error.
6	RW	MASK_PARITY_ERROR_ON_INTERFACE_MACHINE: Mask parity error on the interface machine.
7	RW	MASK_PARITY_ERROR_ON_P2S_MACHINE: Mask parity error on the p2s machine.
8	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_ULCCH: Mask timeout while waiting for ULCCH.
9	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: Mask timeout while waiting for DLDCH return.
10	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_ULDCH: Mask timeout while waiting or ULDCH.
11	RW	MASK_PSCOM_PARALLEL_WRITE_NVLD: Mask PSCOM parallel write NVLD.
12	RW	MASK_PSCOM_PARALLEL_READ_NVLD: Mask PSCOM parallel read NVLD.
13	RW	MASK_PSCOM_PARALLEL_ADDR_INVALID: Mask PSCOM parallel address invalid.

Bits	SCOM	Field Mnemonic: Description
14	RW	MASK_PCB_COMMAND_PARITY_ERROR: Mask PCB command parity error.
15	RW	MASK_GENERAL_TIMEOUT: Mask general timeout.
16	RW	MASK_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: Mask satellite acknowledge access violation.
17	RW	MASK_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: Mask satellite acknowledge invalid register.

Register Name	PSCOMLE Address Trap Register
Mnemonic	TP.TCXB.XB.EPS.PSC.PSC.ADDR_TRAP_REG
Address	0000000006010003 (SCOM)
Description	This is the parallel-to-serial communication light edition (PSCOMLE) address trap register.

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	PCB_ADDRESS_OF_LAST_TRANSACTION_WITH_ERROR: This field contains the PCB address of the last transaction with an error.
16	ROX	PCB_READ_NOTWRITE_OF_LAST_TRANSACTION_WITH_ERROR: PCB read, not write, of the last transaction with an error.
17	ROX	RESERVED_ADDR_LAST_TRAP_LT: Reserved 0.
18:30	ROX	SERIAL2PARALLEL_STATE_MACHINE_AT_TIME_OF_ERROR: Serial2 parallel state machine at the time of the error.
31	ROX	SATELLITE_ACKNOWLEDGE_BIT_RETURN_PARITY: Satellite acknowledge bit: This bit is set to 1 if no parity error is detected in the satellite number or acknowledgment bits.
32	ROX	SATELLITE_ACKNOWLEDGE_BIT_WRITE_PARITY_ERROR: This bit is set if a write parity error is detected by the satellite.
33	ROX	SATELLITE_ACKNOWLEDGE_BIT_ACCESS_VIOLATION: This bit is set if an invalid read or write access is detected by the satellite.
34	ROX	SATELLITE_ACKNOWLEDGE_BIT_INVALID_REGISTER: This bit is set if an invalid register address is detected by the satellite.

Register Name	Ring Lock Enable Register
Mnemonic	TP.TCXB.XB.EPS.PSC.PSC.WRITE_PROTECT_ENABLE_REG
Address	0000000006010005 (SCOM)
Description	This register enables the ring lock.

Bits	SCOM	Field Mnemonic: Description
0	RW	ENABLE_RING_LOCKING: General enable of ring locking upon a write to a specific ring.
1	RW	RESERVED_RING_LOCKING: Reserved.

Register Name	Write Protect Rings Register
Mnemonic	TP.TCXB.XB.EPS.PSC.PSC.WRITE_PROTECT_RINGS_REG
Address	0000000006010006 (SCOM)
Description	This register writes ring protect bit maps.

Bits	SCOM	Field Mnemonic: Description
0:15	RW	WRITE_PROTECT_RINGS: Write protect bit map for each ring.

Register Name	Atomic Lock Mask Register
Mnemonic	TP.TCXB.XB.EPS.PSC.PSC.ATOMIC_LOCK_MASK_LATCH_REG
Address	0000000006010007 (SCOM)
Description	This register provides a bit mask for atomic locking.

Bits	SCOM	Field Mnemonic: Description
0:15	RW	ATOMIC_LOCK_MASK: This field provides a bit mask for atomic locking on a ring-by-ring basis.

Register Name	Ring Fence Enable Mask Register
Mnemonic	TP.TCXB.XB.EPS.PSC.PSC.RING_FENCE_MASK_LATCH_REG
Address	0000000006010008 (SCOM)
Description	This register provides a bit mask for ring fencing.

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:15	RW	RING_FENCE_ENABLE_MASK: This field provides a bit mask for ring fencing on a ring-by-ring basis.

Register Name	Trace Array High Data Register
Mnemonic	TP.TCXB.XB.TRA0.TR0.TRACE_HI_DATA_REG
Address	0000000006010400 (SCOM)
Description	This register provides the high trace-array data.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: This field contains trace array data 0:63.

Register Name	Trace Array Low Data Register
Mnemonic	TP.TCXB.XB.TRA0.TR0.TRACE_LO_DATA_REG
Address	0000000006010401 (SCOM)
Description	This register provides the low trace-array data.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace array data 64:95.
32:41	ROX	TRACE_ADDRESS: Trace address.
42:50	ROX	TRACE_LAST_BANK: Trace last bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace last bank valid.
52	ROX	TRACE_WRITE_ON_RUN: Trace write-on-run indicator.
53	ROX	TRACE_RUNNING: Trace run indicator.

Bits	SCOM	Field Mnemonic: Description
54:63	ROX	TRACE_HOLD_ADDRESS: Trace hold address (pointing to the last entry).

Register Name	Trace Control Configuration Register
Mnemonic	TP.TCXB.XB.TRA0.TR0.TRACE_TRCTRL_CONFIG
Address	0000000006010402 (SCOM)
Description	This register contains trace control configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	STORE_ON_TRIG_MODE: This bit enables store on trigger mode.
1	RW	WRITE_ON_RUN_MODE: This bit enables an unconditional forced write when a trace runs.
2:9	RW	EXTEND_TRIG_MODE: This field contains the counter value for extended trigger mode.
10	RW	BANK_MODE: This bit enables bank mode.
11	RW	ENH_TRACE_MODE: This bit enables enhanced trace mode.
12	RW	LOCAL_CLOCK_GATE_CONTROL: When this bit is set, internal clock gating is disabled. The trace control logic and the trace data pipeline are always clocked.
13	RW	UNUSED_13B. Unused.
14:17	RW	TRACE_SELCT_CONTROL: This field is a selector for two sets of external trace bus multiplexers: tra_mux0_sel(0:1) and tra_mux1_sel(0:1).
18:21	RW	SPARE_CONTROL: This field contains spare control bits.

Register Name	Trace Data Configuration Register 0
Mnemonic	TP.TCXB.XB.TRA0.TR0.TRACE_TRDATA_CONFIG_0
Address	0000000006010403 (SCOM)
Description	This register contains a trace data compare mask for bits 0 – 63.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: This field contains a trace data compare mask for bits 0 - 63.

Register Name	Trace Data Configuration Register 1
Mnemonic	TP.TCXB.XB.TRA0.TR0.TRACE_TRDATA_CONFIG_1
Address	0000000006010404 (SCOM)
Description	This register contains a trace data compare mask for bits 64 – 87.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: This field contains a trace data compare mask for bits 64 – 87.

Register Name	Trace Data Configuration Register 2
Mnemonic	TP.TCXB.XB.TRA0.TR0.TRACE_TRDATA_CONFIG_2
Address	0000000006010405 (SCOM)
Description	This register contains patterns A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: Pattern match for pattern A 0 – 23.
24:47	RW	PATTERNB: Pattern match for pattern B 0 - 23.

Register Name	Trace Data Configuration Register 3
Mnemonic	TP.TCXB.XB.TRA0.TR0.TRACE_TRDATA_CONFIG_3
Address	0000000006010406 (SCOM)
Description	This register contains patterns C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNC: Pattern match for pattern C 0 – 23.
24:47	RW	PATTERND: Pattern match for pattern D 0 – 23.

Register Name	Trace Data Configuration Register 4
Mnemonic	TP.TCXB.XB.TRA0.TR0.TRACE_TRDATA_CONFIG_4
Address	0000000006010407 (SCOM)
Description	This register contains masks A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: Mask A.
24:47	RW	MASKB: Mask B.

Register Name	Trace Data Configuration Register 5
Mnemonic	TP.TCXB.XB.TRA0.TR0.TRACE_TRDATA_CONFIG_5
Address	0000000006010408 (SCOM)
Description	This register contains masks C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: Mask C.
24:47	RW	MASKD: Mask D.

Register Name	Trace Data Configuration Register 9
Mnemonic	TP.TCXB.XB.TRA0.TR0.TRACE_TRDATA_CONFIG_9
Address	0000000006010409 (SCOM)
Description	This register contains trace data configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disable trace data compression (store data every cycle).
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Take into account (care about) changes in the error bit for trace data compression (default = 0).
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.
10:13	RW	TRIG0_OR_MASK: **Note**: The OR of all selected MATCHes is ORed with the result of TRIG0_AND. 0b1XXX selects MATCHA OR 0bX1XX selects MATCHB OR 0bXX1X selects MATCHC OR 0bXXX1 selects MATCHD OR 0b0000 selects to not OR any MATCHes.
14:17	RW	TRIG0_AND_MASK: **Note**: The AND of the following selected MATCHes is ORed with the result of TRIG0_OR. 0b1XXX selects MATCHA AND 0bX1XX selects MATCHB AND 0bXX1X selects MATCHC AND 0bXXX1 selects MATCHD AND 0b0000 selects to not AND any MATCHes together to form TRIG0.
18:21	RW	TRIG1_OR_MASK: **Note**: The OR of all selected MATCHes is ORed with the result of TRIG1_AND. 0b1XXX selects MATCHA OR 0bX1XX selects MATCHB OR 0bXX1X selects MATCHC OR 0bXXX1 selects MATCHD OR 0b0000 selects to not OR any MATCHes to form TRIG1.
22:25	RW	TRIG1_AND_MASK: **Note**: The AND of the following selected MATCHes is ORed with the result of TRIG1_OR. 0b1XXX selects MATCHA AND 0bX1XX selects MATCHB AND 0bXX1X selects MATCHC AND 0bXXX1 selects MATCHD AND 0b0000 selects to not AND any MATCHes together to form TRIG1.
26	RW	TRIG0_NOT_MODE: Invert TRIG0 before using it.
27	RW	TRIG1_NOT_MODE: Invert TRIG1 before using it.

Bits	SCOM	Field Mnemonic: Description
28:31	RW	MATCH_NOT_MODE: Invert the match polarity before using it to form a TRIGger. 0b1000 inverts MATCHA. 0b0100 inverts MATCHB. 0b0010 inverts MATCHC. 0b0001 inverts MATCHD.
32:35	RW	Reserved field.
36	RW	DD1_STRETCH_TRIGGER_PULSES: (DD1 workaround) Stretch trigger output pulses to two clocks. This bit must be enabled for MCFAST and L2FAST traces.
37	RW	Reserved field.

Register Name	Trace Array High Data Register
Mnemonic	TP.TCXB.XB.TRA0.TR1.TRACE_HI_DATA_REG
Address	0000000006010440 (SCOM)
Description	This register provides the high trace array data.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: This field contains trace array data 0:63.

Register Name	Trace Array Low Data Register
Mnemonic	TP.TCXB.XB.TRA0.TR1.TRACE_LO_DATA_REG
Address	0000000006010441 (SCOM)
Description	This register provides the low trace array data.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace array data 64:95.
32:41	ROX	TRACE_ADDRESS: Trace address.
42:50	ROX	TRACE_LAST_BANK: Trace last bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace last bank valid.
52	ROX	TRACE_WRITE_ON_RUN: Trace write-on-run indicator.
53	ROX	TRACE_RUNNING: Trace run indicator.
54:63	ROX	TRACE_HOLD_ADDRESS: Trace hold address (pointing to the last entry).

Register Name	Trace Control Configuration Register
Mnemonic	TP.TCXB.XB.TRA0.TR1.TRACE_TRCTRL_CONFIG
Address	0000000006010442 (SCOM)
Description	This register contains trace control configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	STORE_ON_TRIG_MODE: This bit enables store on trigger mode.
1	RW	WRITE_ON_RUN_MODE: This bit enables an unconditional forced write when a trace runs.
2:9	RW	EXTEND_TRIG_MODE: This field contains the counter value for extended trigger mode.

Bits	SCOM	Field Mnemonic: Description
10	RW	BANK_MODE: This bit enables bank mode.
11	RW	ENH_TRACE_MODE: This bit enables enhanced trace mode.
12	RW	LOCAL_CLOCK_GATE_CONTROL: When this bit is set, internal clock gating is disabled. The trace control logic and the trace data pipeline are always clocked.
13	RW	UNUSED_13B. Unused.
14:17	RW	TRACE_SELCT_CONTROL: This field is a selector for two sets of external trace bus multiplexers: tra_mux0_sel(0:1) and tra_mux1_sel(0:1).
18:21	RW	SPARE_CONTROL: This field contains spare control bits.

Register Name	Trace Data Configuration Register 0
Mnemonic	TP.TCXB.XB.TRA0.TR1.TRACE_TRDATA_CONFIG_0
Address	0000000006010443 (SCOM)
Description	This register contains a trace data compare mask for bits 0 – 63.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: This field contains a trace data compare mask for bits 0 - 63.

Register Name	Trace Data Configuration Register 1
Mnemonic	TP.TCXB.XB.TRA0.TR1.TRACE_TRDATA_CONFIG_1
Address	0000000006010444 (SCOM)
Description	This register contains a trace data compare mask for bits 64 – 87.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: This field contains a trace data compare mask for bits 64 – 87.

Register Name	Trace Data Configuration Register 2
Mnemonic	TP.TCXB.XB.TRA0.TR1.TRACE_TRDATA_CONFIG_2
Address	0000000006010445 (SCOM)
Description	This register contains patterns A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: Pattern match for pattern A 0 – 23.
24:47	RW	PATTERNB: Pattern match for pattern B 0 - 23.

Register Name	Trace Data Configuration Register 3
Mnemonic	TP.TCXB.XB.TRA0.TR1.TRACE_TRDATA_CONFIG_3
Address	0000000006010446 (SCOM)
Description	This register contains patterns C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNC: Pattern match for pattern C 0 – 23.
24:47	RW	PATTERND: Pattern match for pattern D 0 – 23.

Register Name	Trace Data Configuration Register 4
Mnemonic	TP.TCXB.XB.TRA0.TR1.TRACE_TRDATA_CONFIG_4
Address	0000000006010447 (SCOM)
Description	This register contains masks A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: Mask A.
24:47	RW	MASKB: Mask B.

Register Name	Trace Data Configuration Register 5
Mnemonic	TP.TCXB.XB.TRA0.TR1.TRACE_TRDATA_CONFIG_5
Address	0000000006010448 (SCOM)
Description	This register contains masks C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: Mask C.
24:47	RW	MASKD: Mask D.

Register Name	Trace Data Configuration Register 9
Mnemonic	TP.TCXB.XB.TRA0.TR1.TRACE_TRDATA_CONFIG_9
Address	0000000006010449 (SCOM)
Description	This register contains trace data configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disable trace data compression (store data every cycle).
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Take into account (care about) changes in the error bit for trace data compression (default = 0).
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.

Bits	SCOM	Field Mnemonic: Description
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.
10:13	RW	TRIG0_OR_MASK: **Note**: The OR of all selected MATCHes is ORed with result of TRIG0_AND: 0b1XXX selects MATCHA OR 0bX1XX selects MATCHB OR 0bXX1X selects MATCHC OR 0bXXX1 selects MATCHD OR 0b0000 selects to not OR any MATCHes.
14:17	RW	TRIG0_AND_MASK: **Note**: The AND of the following selected MATCHes is ORed with result of TRIG0_OR: 0b1XXX selects MATCHA AND 0bX1XX selects MATCHB AND 0bXX1X selects MATCHC AND 0bXXX1 selects MATCHD AND 0b0000 selects to not AND any MATCHes together to form TRIG0.
18:21	RW	TRIG1_OR_MASK: **Note**: The OR of all selected MATCHes is ORed with the result of TRIG1_AND: 0b1XXX selects MATCHA OR 0bX1XX selects MATCHB OR 0bXX1X selects MATCHC OR 0bXXX1 selects MATCHD OR 0b0000 selects to not OR any MATCHes to form TRIG1.
22:25	RW	TRIG1_AND_MASK: **Note**: The AND of the following selected MATCHes is ORed with the result of TRIG1_OR: 0b1XXX selects MATCHA AND 0bX1XX selects MATCHB AND 0bXX1X selects MATCHC AND 0bXXX1 selects MATCHD AND 0b0000 selects to not AND any MATCHes together to form TRIG1.
26	RW	TRIG0_NOT_MODE: Invert TRIG0 before using it.
27	RW	TRIG1_NOT_MODE: Invert TRIG1 before using it.
28:31	RW	MATCH_NOT_MODE: Invert the match polarity before using it to form a TRIGger. 0b1000 inverts MATCHA. 0b0100 inverts MATCHB. 0b0010 inverts MATCHC. 0b0001 inverts MATCHD.
32:35	RW	Reserved field.
36	RW	DD1_STRETCH_TRIGGER_PULSES: (DD1 workaround) Stretch trigger output pulses to two clocks. This bit must be enabled for MCFAST and L2FAST traces.
37	RW	Reserved field.

Register Name	Trace Array High Data Register
Mnemonic	TP.TCXB.XB.TRA1.TR0.TRACE_HI_DATA_REG
Address	0000000006010480 (SCOM)
Description	This register provides the high trace-array data.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: This field contains trace array data 0:63.

Register Name	Trace Array Low Data Register
Mnemonic	TP.TCXB.XB.TRA1.TR0.TRACE_LO_DATA_REG
Address	0000000006010481 (SCOM)
Description	This register provides the low trace-array data.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace array data 64:95.
32:41	ROX	TRACE_ADDRESS: Trace address.
42:50	ROX	TRACE_LAST_BANK: Trace last bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace last bank valid.
52	ROX	TRACE_WRITE_ON_RUN: Trace write-on-run indicator.
53	ROX	TRACE_RUNNING: Trace run indicator.
54:63	ROX	TRACE_HOLD_ADDRESS: Trace hold address (pointing to the last entry).

Register Name	Trace Control Configuration Register
Mnemonic	TP.TCXB.XB.TRA1.TR0.TRACE_TRCTRL_CONFIG
Address	0000000006010482 (SCOM)
Description	This register contains trace control configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	STORE_ON_TRIG_MODE: This bit enables store on trigger mode.
1	RW	WRITE_ON_RUN_MODE: This bit enables an unconditional forced write when a trace runs.
2:9	RW	EXTEND_TRIG_MODE: This field contains the counter value for extended trigger mode.
10	RW	BANK_MODE: This bit enables bank mode.
11	RW	ENH_TRACE_MODE: This bit enables enhanced trace mode.
12	RW	LOCAL_CLOCK_GATE_CONTROL: When this bit is set, internal clock gating is disabled. The trace control logic and the trace data pipeline are always clocked.
13	RW	UNUSED_13B. Unused.
14:17	RW	TRACE_SELCT_CONTROL: This field is a selector for two sets of external trace bus multiplexers: tra_mux0_sel(0:1) and tra_mux1_sel(0:1).
18:21	RW	SPARE_CONTROL: This field contains spare control bits.

Register Name	Trace Data Configuration Register 0
Mnemonic	TP.TCXB.XB.TRA1.TR0.TRACE_TRDATA_CONFIG_0
Address	0000000006010483 (SCOM)
Description	This register contains a trace data compare mask for bits 0 – 63.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: This field contains a trace data compare mask for bits 0 - 63.

Register Name	Trace Data Configuration Register 1
Mnemonic	TP.TCXB.XB.TRA1.TR0.TRACE_TRDATA_CONFIG_1
Address	0000000006010484 (SCOM)
Description	This register contains a trace data compare mask for bits 64 – 87.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: This field contains a trace data compare mask for bits 64 – 87.

Register Name	Trace Data Configuration Register 2
Mnemonic	TP.TCXB.XB.TRA1.TR0.TRACE_TRDATA_CONFIG_2
Address	0000000006010485 (SCOM)
Description	This register contains patterns A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: Pattern match for pattern A 0 – 23.
24:47	RW	PATTERNB: Pattern match for pattern B 0 - 23.

Register Name	Trace Data Configuration Register 3
Mnemonic	TP.TCXB.XB.TRA1.TR0.TRACE_TRDATA_CONFIG_3
Address	0000000006010486 (SCOM)
Description	This register contains patterns C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNC: Pattern match for pattern C 0 – 23.
24:47	RW	PATTERND: Pattern match for pattern D 0 – 23.

Register Name	Trace Data Configuration Register 4
Mnemonic	TP.TCXB.XB.TRA1.TR0.TRACE_TRDATA_CONFIG_4
Address	0000000006010487 (SCOM)
Description	This register contains masks A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: Mask A.
24:47	RW	MASKB: Mask B.

Register Name	Trace Data Configuration Register 5
Mnemonic	TP.TCXB.XB.TRA1.TR0.TRACE_TRDATA_CONFIG_5
Address	0000000006010488 (SCOM)
Description	This register contains masks C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: Mask C.
24:47	RW	MASKD: Mask D.

Register Name	Trace Data Configuration Register 9
Mnemonic	TP.TCXB.XB.TRA1.TR0.TRACE_TRDATA_CONFIG_9
Address	0000000006010489 (SCOM)
Description	This register contains trace data configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disable trace data compression (store data every cycle).
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Take into account (care about) changes in the error bit for trace data compression (default = 0).
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.

Bits	SCOM	Field Mnemonic: Description
10:13	RW	TRIG0_OR_MASK: **Note**: The OR of all selected MATCHes is ORed with result of TRIG0_AND: 0b1XXX selects MATCHA OR 0bX1XX selects MATCHB OR 0bXX1X selects MATCHC OR 0bXXX1 selects MATCHD OR 0b0000 selects to not OR any MATCHes.
14:17	RW	TRIG0_AND_MASK: **Note**: The AND of the following selected MATCHes is ORed with result of TRIG0_OR: 0b1XXX selects MATCHA AND 0bX1XX selects MATCHB AND 0bXX1X selects MATCHC AND 0bXXX1 selects MATCHD AND 0b0000 selects to not AND any MATCHes together to form TRIG0.
18:21	RW	TRIG1_OR_MASK: **Note**: The OR of all selected MATCHes is ORed with the result of TRIG1_AND: 0b1XXX selects MATCHA OR 0bX1XX selects MATCHB OR 0bXX1X selects MATCHC OR 0bXXX1 selects MATCHD OR 0b0000 selects to not OR any MATCHes to form TRIG1.
22:25	RW	TRIG1_AND_MASK: **Note**: The AND of the following selected MATCHes is ORed with the result of TRIG1_OR: 0b1XXX selects MATCHA AND 0bX1XX selects MATCHB AND 0bXX1X selects MATCHC AND 0bXXX1 selects MATCHD AND 0b0000 selects to not AND any MATCHes together to form TRIG1.
26	RW	TRIG0_NOT_MODE: Invert TRIG0 before using it.
27	RW	TRIG1_NOT_MODE: Invert TRIG1 before using it.
28:31	RW	MATCH_NOT_MODE: Invert the match polarity before using it to form a TRIGger. 0b1000 inverts MATCHA. 0b0100 inverts MATCHB. 0b0010 inverts MATCHC. 0b0001 inverts MATCHD.
32:35	RW	Reserved field.
36	RW	DD1_STRETCH_TRIGGER_PULSES: (DD1 workaround) Stretch trigger output pulses to two clocks. This bit must be enabled for MCFAST and L2FAST traces.
37	RW	Reserved field.

Register Name	**Debug Mode Register**
Mnemonic	TP.TCXB.XB.EPS.DBG.DBG_MODE_REG
Address	00000000060107C0 (SCOM)
Description	This is debug macro configuration register 0 for the configuration component.

Bits	SCOM	Field Mnemonic: Description
0:2	RW	GLB_BRCST_MODE: Global broadcast mode (0 - 2): 100 = dbg_trace_run and dbg_trace_freeze. 101 = pc_tcdbg_trace_run_fncd and dbg_trace_freeze. 110 = dbg_triggers_out(0 to 1). 111 = pc_tcdbg_triggers(0 to 1) (from core.)

Bits	SCOM	Field Mnemonic: Description
3:5	RW	TRACE_SEL_MODE: Select source for trace_run and bank: 001 = core trace run and bank. 010 = tp broadcast run and 0. 011 = tc_dbg_inter_brcst latched. 100 = tc_dbg_dbg_sync_brcst_rcv. else: dbg_trace_run and dbg_trace_bank.
6:7	RW	TRIG_SEL_MODE: Select source for tcdbg_trigger(0): 10 = global broadcast. 11 = pc_tcdbg_trigger (from core). else: dbg_triggers_out(0:1).
8	RW	STOP_ON_XSTOP_SELECTION: This bit enables a trace stop on a checkstop.
9	RW	STOP_ON_RECOV_ERR_SELECTION: This bit enables a trace stop on a recoverable error.
10	RW	STOP_ON_SPATTN_SELECTION: This bit enables a trace stop on special attention.
11	RW	FREEZE_SEL_MODE: Select the freeze source: 0 = Local debug freeze. 1 = Via broadcast: tp_tcdbg_glb_brcst(1).
12:13	RW	SYNC_BRCST_MODE: Originally used for synchronous broadcast mode; currently unused because obsolete. See trace_sel_mode.
14	RO	constant = 0b0 sync_brcst_mode
15	RO	constant = 0b0
16:31	ROX	DBG_STATUS: Debug status.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	Debug Instance 1 Condition 1 Register
Mnemonic	TP.TCXB.XB.EPS.DBG.DBG_INST1_COND_REG_1
Address	00000000060107C1 (SCOM)
Description	This is debug macro configuration register 1 for front-end component 1.

Bits	SCOM	Field Mnemonic: Description
0:7	RW	INST1_COND1_SEL_A: Multiplexer for cond1_trig_in(0). 000 select constant 0 001 select constant 1 -- CONDITION FEEDBACK -- 002 select inst1_dbg_cond1. 003 select inst1_dbg_cond2. 004 select inst1_dbg_cond3. 005 select inst1_dbg_cond2timeout. 006 select inst2_dbg_cond1. 007 select inst2_dbg_cond2. 008 select inst2_dbg_cond3. 009 select inst2_dbg_cond2timeout. 010 select inst3_dbg_cond1 - unused, tied down. 011 select inst3_dbg_cond2 - unused, tied down. 012 select inst3_dbg_cond3 - unused, tied down. 013 select inst3_dbg_cond2timeout - unused, tied down. 014 select inst4_dbg_cond1 - unused, tied down. 015 select inst4_dbg_cond2 - unused, tied down. 016 select inst4_dbg_cond3 - unused, tied down. 017 select inst4_dbg_cond2timeout - unused, tied down. 018 select inst1_dbg_trig_sp.

Bits	SCOM	Field Mnemonic: Description
		019 select inst2_dbg_trig_sp. 020 select inst3_dbg_trig_sp - unused, tied down. 021 select inst4_dbg_trig_sp - unused, tied down. 022 select tctrc_tcdbg_trigger_a(0). 023 select tctrc_tcdbg_trigger_b(0). 024 select tctrc_tcdbg_trigger_a(0) and tctrc_tcdbg_trigger_b(0). 025 select tctrc_tcdbg_trigger_a(1). 026 select tctrc_tcdbg_trigger_b(1). 027 select tctrc_tcdbg_trigger_a(1) and tctrc_tcdbg_trigger_b(1). 028 select tctrc_tcdbg_trigger_a(2). 029 select tctrc_tcdbg_trigger_b(2). 030 select tctrc_tcdbg_trigger_a(2) and tctrc_tcdbg_trigger_b(2). 031 select tctrc_tcdbg_trigger_a(3). 032 select tctrc_tcdbg_trigger_b(3). 033 select tctrc_tcdbg_trigger_a(3) and tctrc_tcdbg_trigger_b(3). 034 select tctrc_tcdbg_trigger_a(4). 035 select tctrc_tcdbg_trigger_b(4). 036 select tctrc_tcdbg_trigger_a(4) and tctrc_tcdbg_trigger_b(4). 037 select tctrc_tcdbg_trigger_a(5). 038 select tctrc_tcdbg_trigger_b(5). 039 select tctrc_tcdbg_trigger_a(5) and tctrc_tcdbg_trigger_b(5). 040 select tctrc_tcdbg_trigger_a(6). 041 select tctrc_tcdbg_trigger_b(6). 042 select tctrc_tcdbg_trigger_a(6) and tctrc_tcdbg_trigger_b(6). 043 select tctrc_tcdbg_trigger_a(7). 044 select tctrc_tcdbg_trigger_b(7). 045 select tctrc_tcdbg_trigger_a(7) and tctrc_tcdbg_trigger_b(7). 046 select tctrc_tcdbg_trigger_a(8). 047 select tctrc_tcdbg_trigger_b(8). 048 select tctrc_tcdbg_trigger_a(8) and tctrc_tcdbg_trigger_b(8). 049 select tctrc_tcdbg_trigger_a(9). 050 select tctrc_tcdbg_trigger_b(9). 051 select tctrc_tcdbg_trigger_a(9) and tctrc_tcdbg_trigger_b(9). 052 select tctrc_tcdbg_trigger_a(10). 053 select tctrc_tcdbg_trigger_b(10). 054 select tctrc_tcdbg_trigger_a(10) and tctrc_tcdbg_trigger_b(10). 055 select tctrc_tcdbg_trigger_a(11). 056 select tctrc_tcdbg_trigger_b(11). 057 select tctrc_tcdbg_trigger_a(11) and tctrc_tcdbg_trigger_b(11). 058 select tctrc_tcdbg_trigger_a(12). 059 select tctrc_tcdbg_trigger_b(12). 060 select tctrc_tcdbg_trigger_a(12) and tctrc_tcdbg_trigger_b(12). 061 select tctrc_tcdbg_trigger_a(13). 062 select tctrc_tcdbg_trigger_b(13). 063 select tctrc_tcdbg_trigger_a(13) and tctrc_tcdbg_trigger_b(13). 064 select tctrc_tcdbg_trigger_a(14). 065 select tctrc_tcdbg_trigger_b(14). 066 select tctrc_tcdbg_trigger_a(14) and tctrc_tcdbg_trigger_b(14). 067 select tctrc_tcdbg_trigger_a(15). 068 select tctrc_tcdbg_trigger_b(15). 069 select tctrc_tcdbg_trigger_a(15) and tctrc_tcdbg_trigger_b(15). 070 select tctrc_tcdbg_trigger_a(16). 071 select tctrc_tcdbg_trigger_b(16). 072 select tctrc_tcdbg_trigger_a(16) and tctrc_tcdbg_trigger_b(16). 073 select tctrc_tcdbg_trigger_a(17). 074 select tctrc_tcdbg_trigger_b(17). 075 select tctrc_tcdbg_trigger_a(17) and tctrc_tcdbg_trigger_b(17). -- LOGIC (UNIT) TRIGGERS -- EP: 0:3 L3C0, 4:7 L3C1, 8:9 GX, 10 TP (hang), 11 spare, 12:13 MCA, 14:15 spare. ES: 0:4 L4C, 5:6 L4F, 7:8 TPTOD, 9 TP (hang), 10:15 spare. 076 select logic_trigger_in(0).

Bits	SCOM	Field Mnemonic: Description
		077 select logic_trigger_in(1). 078 select logic_trigger_in(2). 079 select logic_trigger_in(3). 080 select logic_trigger_in(4). 081 select logic_trigger_in(5). 082 select logic_trigger_in(6). 083 select logic_trigger_in(7). 084 select logic_trigger_in(8). 085 select logic_trigger_in(9). 086 select logic_trigger_in(10). 087 select logic_trigger_in(11). 088 select logic_trigger_in(12). 089 select logic_trigger_in(13). 090 select logic_trigger_in(14). 091 select logic_trigger_in(15). 092 select pc_tcdbg_trigger(0). 093 select pc_tcdbg_trigger(1). 094 select tctrc_tcdbg_glb_brcst(0). 095 select tctrc_tcdbg_glb_brcst(1). 096 select xstop_err. 097 select recov_err. 098 select spattn. 099 select fir_dbg_local_xstop_err. 100 select tc_dbg_inter_brcst(0). 101 select tc_dbg_inter_brcst(1). -- CORE TRIGGERS (EP chip only) -- **Note:** set core_slave_mode to honor ec[0:5]_tc_trace_run. 102 select core trigger 0: any rising edge of ec[0:5]_tc_trace_run(0). 103 select core trigger 1: any rising edge of ec[0:5]_tc_trace_run(1). 104 select core trigger 2: any falling edge of ec[0:5]_tc_trace_run(0). 105 select core trigger 3: any falling edge of ec[0:5]_tc_trace_run(1). 106 select glb_trig_or_trace_in(0). 107 select glb_trig_or_trace_in(1). 108 select core_local_brcst_trc(0). 109 select core_local_brcst_trc(1). 110 select glb_freeze_brcst_rec(0). 111 select trig_2_extern_in(0). 112 select trig_2_extern_in(1). 113 select dbg_triggers_out(2). 114 select dbg_triggers_out(3). 115 select dbg_triggers_out(4). 116 select dbg_triggers_out(5). 117 select dbg_triggers_out(6). 118 select tcdbg_trigger_in(0). 119 select tcdbg_trigger_in(1).
8:15	RW	INST1_COND1_SEL_B: Multiplexer for cond1_trig_in(1). Selection as cond1_trig_in(0).
16:23	RW	INST1_COND2_SEL_A: Multiplexer for cond2_trig_in(0). Selection as cond1_trig_in(0).
24:31	RW	INST1_COND2_SEL_B: Multiplexer for cond2_trig_in(1). Selection as cond1_trig_in(0).
32	RW	INST1_C1_INAROW_MODE: Front-end instance 1, counter 1 in-a-row mode.
33	RW	INST1_AND_TRIGGER_MODE1: Front-end instance 1 and trigger mode condition 1.
34	RW	INST1_NOT_TRIGGER_MODE1: Front-end instance 1 inverted trigger mode condition 1.
35	RW	INST1_EDGE_TRIGGER_MODE1: Front-end instance 1 edge trigger mode condition 1.
36:38	RWX	INST1_UNUSED_1: Unused.

Bits	SCOM	Field Mnemonic: Description
39	RW	INST1_C2_INAROW_MODE: Front-end instance 1, counter 2 in-a-row mode.
40	RW	INST1_AND_TRIGGER_MODE2: Front-end instance 1 and trigger mode2.
41	RW	INST1_NOT_TRIGGER_MODE2: Front-end instance 1 inverted (not) trigger.
42	RW	INST1_EDGE_TRIGGER_MODE2: Front-end instance 1 edge trigger.
43:45	RWX	INST1_UNUSED_2: Unused
46	RW	INST1_COND3_ENABLE_RESET: Front-end instance 1 condition 3 enable.
47	RW	INST1_EXACT_TO_MODE: Front-end instance 1 exact timeout mode.
48	RW	INST1_RESET_C2TIMER_ON_C1: Front-end instance 1 reset condition 2 timer on condition 1.
49	RW	INST1_RESET_C3_ON_C0: Front-end instance 1 reset condition 3 on condition 0.
50	RW	INST1_SLOW_TO_MODE: Front-end instance 1 slow timeout mode.
51	RW	INST1_EXACT_RESET_C3_ON_TO: Front-end instance 1 exact reset condition 3 on timeout.
52:55	RW	INST1_C1_COUNT_LT: Instance 1 condition 1 counter compare value.
56:59	RW	INST1_C2_COUNT_LT: Instance 1 condition 2 counter compare value.
60:62	RW	INST1_RESET_C3_SELECT: Front-end instance 1: reset condition 3 for reset_c3_on_c0: 0b100 = dbg_cross_couple_triggers(4) 0b101 = dbg_cross_couple_triggers(12) 0b110 = dbg_cross_couple_triggers(20) 0b111 = dbg_cross_couple_triggers(28)

Register Name	Debug Instance 1 Condition 2 Register
Mnemonic	TP.TCXB.XB.EPS.DBG.DBG_INST1_COND_REG_2
Address	00000000060107C2 (SCOM)
Description	This is debug macro configuration register 2 for front-end component 1.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	INST1_CROSS_COUPLE_SELECT_1_A: Cross coupling is the same for all selectors: 00000 selects inst1_cond1_trig_a. 00001 selects inst1_cond1_trig_b. 00010 selects inst1_cond2_trig_a. 00011 selects inst1_cond2_trig_b. 00100 selects inst1_condition1. 00101 selects inst1_condition2. 00110 selects inst1_condition3. 00111 selects inst1_cond2_timeout. 01000 selects inst2_cond1_trig_a. 01001 selects inst2_cond1_trig_b. 01010 selects inst2_cond2_trig_a. 01011 selects inst2_cond2_trig_b. 01100 selects inst2_condition1. 01101 selects inst2_condition2. 01110 selects inst2_condition3. 01111 selects inst2_cond2_timeout. 10000 selects inst3_cond1_trig_a. 10001 selects inst3_cond1_trig_b. 10010 selects inst3_cond2_trig_a. 10011 selects inst3_cond2_trig_b. 10100 selects inst3_condition1. 10101 selects inst3_condition2. 10110 selects inst3_condition3.

Bits	SCOM	Field Mnemonic: Description
		10111 selects inst3_cond2_timeout. 11000 selects inst4_cond1_trig_a. 11001 selects inst4_cond1_trig_b. 11010 selects inst4_cond2_trig_a. 11011 selects inst4_cond2_trig_b. 11100 selects inst4_condition1. 11101 selects inst4_condition2. 11110 selects inst4_condition3. 11111 selects inst4_cond2_timeout.
5:9	RW	INST1_CROSS_COUPLE_SELECT_1_B: Instance 1 cross couple select 1 b.
10:14	RW	INST1_CROSS_COUPLE_SELECT_2_A: Instance 1 cross couple select 2 a.
15:19	RW	INST1_CROSS_COUPLE_SELECT_2_B: Instance 1 cross couple select 2 b.
20:43	RW	INST1_TO_CMP_LT: Compare value for special counter sp_cnt_lt in debug component 1.
44	RW	INST1_FORCE_TEST_MODE: Force test mode to indicate to compare without an actual compare.

Register Name	Debug Instance 1 Condition 3 Register
Mnemonic	TP.TCXB.XB.EPS.DBG.DBG_INST1_COND_REG_3
Address	00000000060107C3 (SCOM)
Description	This is debug macro configuration register 3 for the front-end 1 component.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	INST1_SP_COUNT_LT: Timeout counter to_cmp compare value for dbg_cond_comp_1.

Register Name	Debug Instance 2 Condition 1 Register
Mnemonic	TP.TCXB.XB.EPS.DBG.DBG_INST2_COND_REG_1
Address	00000000060107C4 (SCOM)
Description	This is debug macro configuration register 1 for the front-end 1 component.

Bits	SCOM	Field Mnemonic: Description
0:7	RW	INST2_COND1_SEL_A: Multiplexer for cond1_trig_in(0). 000 select constant 0 001 select constant 1 -- CONDITION FEEDBACK -- 002 select inst2_dbg_cond1. 003 select inst2_dbg_cond2. 004 select inst2_dbg_cond3. 005 select inst2_dbg_cond2timeout. 006 select inst2_dbg_cond1. 007 select inst2_dbg_cond2. 008 select inst2_dbg_cond3. 009 select inst2_dbg_cond2timeout. 010 select inst3_dbg_cond1 - unused, tied down. 011 select inst3_dbg_cond2 - unused, tied down. 012 select inst3_dbg_cond3 - unused, tied down. 013 select inst3_dbg_cond2timeout - unused, tied down. 014 select inst4_dbg_cond1 - unused, tied down. 015 select inst4_dbg_cond2 - unused, tied down. 016 select inst4_dbg_cond3 - unused, tied down. 017 select inst4_dbg_cond2timeout - unused, tied down.

Bits	SCOM	Field Mnemonic: Description
		018 select inst2_dbg_trig_sp. 019 select inst2_dbg_trig_sp. 020 select inst3_dbg_trig_sp - unused, tied down. 021 select inst4_dbg_trig_sp - unused, tied down. 022 select tctrc_tcdbg_trigger_a(0). 023 select tctrc_tcdbg_trigger_b(0). 024 select tctrc_tcdbg_trigger_a(0) and tctrc_tcdbg_trigger_b(0). 025 select tctrc_tcdbg_trigger_a(1). 026 select tctrc_tcdbg_trigger_b(1). 027 select tctrc_tcdbg_trigger_a(1) and tctrc_tcdbg_trigger_b(1). 028 select tctrc_tcdbg_trigger_a(2). 029 select tctrc_tcdbg_trigger_b(2). 030 select tctrc_tcdbg_trigger_a(2) and tctrc_tcdbg_trigger_b(2). 031 select tctrc_tcdbg_trigger_a(3). 032 select tctrc_tcdbg_trigger_b(3). 033 select tctrc_tcdbg_trigger_a(3) and tctrc_tcdbg_trigger_b(3). 034 select tctrc_tcdbg_trigger_a(4). 035 select tctrc_tcdbg_trigger_b(4). 026 select tctrc_tcdbg_trigger_a(4) and tctrc_tcdbg_trigger_b(4). 027 select tctrc_tcdbg_trigger_a(5). 028 select tctrc_tcdbg_trigger_b(5). 029 select tctrc_tcdbg_trigger_a(5) and tctrc_tcdbg_trigger_b(5). 030 select tctrc_tcdbg_trigger_a(6). 031 select tctrc_tcdbg_trigger_b(6). 032 select tctrc_tcdbg_trigger_a(6) and tctrc_tcdbg_trigger_b(6). 033 select tctrc_tcdbg_trigger_a(7). 034 select tctrc_tcdbg_trigger_b(7). 035 select tctrc_tcdbg_trigger_a(7) and tctrc_tcdbg_trigger_b(7). 036 select tctrc_tcdbg_trigger_a(8). 037 select tctrc_tcdbg_trigger_b(8). 038 select tctrc_tcdbg_trigger_a(8) and tctrc_tcdbg_trigger_b(8). 039 select tctrc_tcdbg_trigger_a(9). 040 select tctrc_tcdbg_trigger_b(9). 041 select tctrc_tcdbg_trigger_a(9) and tctrc_tcdbg_trigger_b(9). 042 select xstop_err. 043 select recov_err. 044 select spattn. 045 select fir_dbg_local_xstop_err. 046 select tc_dbg_inter_brcst(0). 047 select tc_dbg_inter_brcst(1). -- LOGIC (UNIT) TRIGGERS -- EP: 0:3 L3C0, 4:7 L3C1, 8:9 GX, 10 TP (hang), 11 spare, 12:13 MCA, 14:15 spare. ES: 0:4 L4C, 5:6 L4F, 7:8 TPTOD, 9 TP (hang), 10:15 spare. 102 select logic_trigger_in(0). 103 select logic_trigger_in(1). 104 select logic_trigger_in(2). 105 select logic_trigger_in(3). 106 select logic_trigger_in(4). 107 select logic_trigger_in(5). 108 select logic_trigger_in(6). 109 select logic_trigger_in(7). 110 select logic_trigger_in(8). 111 select logic_trigger_in(9). 112 select logic_trigger_in(10). 113 select logic_trigger_in(11). 114 select logic_trigger_in(12). 115 select logic_trigger_in(13). 116 select logic_trigger_in(14). 117 select logic_trigger_in(15). -- CORE TRIGGERS (EP chip only) -- **Note:** set core_slave_mode to honor ec[0:5]_tc_trace_run.

Bits	SCOM	Field Mnemonic: Description
		118 select core trigger 0: any rising edge of ec[0:5]_tc_trace_run(0). 119 select core trigger 1: any rising edge of ec[0:5]_tc_trace_run(1). 120 select core trigger 2: any falling edge of ec[0:5]_tc_trace_run(0). 121 select core trigger 3: any falling edge of ec[0:5]_tc_trace_run(1). -- BROADCAST / ERRORS. 122 select glb_trc_bdcst_recv (received global broadcast). 123 select edge detected fir_dbg_xstop_err. 124 select edge detected fir_dbg_recov_err. 125 select edge detected fir_dbg_spatn. 126 ... 127 select constant 0 (unused)
8:15	RW	INST2_COND1_SEL_B: Multiplexer for cond1_trig_in(1). Selection as cond1_trig_in(0).
16:23	RW	INST2_COND2_SEL_A: Multiplexer for cond2_trig_in(0). Selection as cond1_trig_in(0).
24:31	RW	INST2_COND2_SEL_B: Multiplexer for cond2_trig_in(1). Selection as cond1_trig_in(0).
32	RW	INST2_C1_INAROW_MODE: Front-end instance 1 counter 1 in-a-row mode.
33	RW	INST2_AND_TRIGGER_MODE1: Front-end instance 1 and trigger mode condition1.
34	RW	INST2_NOT_TRIGGER_MODE1: Front-end instance 1 inverted trigger mode condition1.
35	RW	INST2_EDGE_TRIGGER_MODE1: Front-end instance 1 edge trigger mode condition1.
36:38	RWX	INST2_UNUSED_1: Unused.
39	RW	INST2_C2_INAROW_MODE: Front-end instance 1 counter 2 in-a-row mode.
40	RW	INST2_AND_TRIGGER_MODE2: Front-end instance 1 and trigger mode2.
41	RW	INST2_NOT_TRIGGER_MODE2: Front-end instance 1 inverted (not) trigger.
42	RW	INST2_EDGE_TRIGGER_MODE2: Front-end instance 1 edge trigger.
43:45	RWX	INST2_UNUSED_2: Unused.
46	RW	INST2_COND3_ENABLE_RESET: Front-end instance 1 condition 3 enable.
47	RW	INST2_EXACT_TO_MODE: Front-end instance 1 exact timeout mode.
48	RW	INST2_RESET_C2TIMER_ON_C1: Front-end instance 1 reset condition 2 timer on condition 1.
49	RW	INST2_RESET_C3_ON_C0: Front-end instance 1 reset condition 3 on condition 0.
50	RW	INST2_SLOW_TO_MODE: Front-end instance 1 slow timeout mode.
51	RW	INST2_EXACT_RESET_C3_ON_TO: Front-end instance 1 exact reset condition 3 on timeout.
52:55	RW	INST2_C1_COUNT_LT: Instance 2 condition 1 counter compare value.
56:59	RW	INST2_C2_COUNT_LT: Instance 2 condition 2 counter compare value.
60:62	RW	INST2_RESET_C3_SELECT: Front-end instance 1, reset condition 3 for reset_c3_on_c0: 0b100 = dbg_cross_couple_triggers(4). 0b101 = dbg_cross_couple_triggers(12). 0b110 = dbg_cross_couple_triggers(20). 0b111 = dbg_cross_couple_triggers(28).

Register Name	Debug Instance 2 Condition 2 Register
Mnemonic	TP.TCXB.XB.EPS.DBG.DBG_INST2_COND_REG_2
Address	00000000060107C5 (SCOM)
Description	This is debug macro configuration register 2 for the front-end 1 component.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	INST2_CROSS_COUPLE_SELECT_1_A: Cross coupling is the same for all selectors: 00000 selects inst2_cond1_trig_a. 00001 selects inst2_cond1_trig_b. 00010 selects inst2_cond2_trig_a. 00011 selects inst2_cond2_trig_b. 00100 selects inst2_condition1. 00101 selects inst2_condition2. 00110 selects inst2_condition3. 00111 selects inst2_cond2_timeout. 01000 selects inst2_cond1_trig_a. 01001 selects inst2_cond1_trig_b. 01010 selects inst2_cond2_trig_a. 01011 selects inst2_cond2_trig_b. 01100 selects inst2_condition1. 01101 selects inst2_condition2. 01110 selects inst2_condition3. 01111 selects inst2_cond2_timeout. 10000 selects inst3_cond1_trig_a. 10001 selects inst3_cond1_trig_b. 10010 selects inst3_cond2_trig_a. 10011 selects inst3_cond2_trig_b. 10100 selects inst3_condition1. 10101 selects inst3_condition2. 10110 selects inst3_condition3. 10111 selects inst3_cond2_timeout. 11000 selects inst4_cond1_trig_a. 11001 selects inst4_cond1_trig_b. 11010 selects inst4_cond2_trig_a. 11011 selects inst4_cond2_trig_b. 11100 selects inst4_condition1. 11101 selects inst4_condition2. 11110 selects inst4_condition3. 11111 selects inst4_cond2_timeout.
5:9	RW	INST2_CROSS_COUPLE_SELECT_1_B: Instance 2 cross couple select 1 b.
10:14	RW	INST2_CROSS_COUPLE_SELECT_2_A: Instance 2 cross couple select 2 a.
15:19	RW	INST2_CROSS_COUPLE_SELECT_2_B: Instance 2 cross couple select 2 b.
20:43	RW	INST2_TO_CMP_LT: Compare value for special counter sp_cnt_lt in debug component 2.
44	RW	INST2_FORCE_TEST_MODE: Force test mode to indicate to compare without actual compare.

Register Name	Debug Instance 2 Condition 3 Register
Mnemonic	TP.TCXB.XB.EPS.DBG.DBG_INST2_COND_REG_3
Address	00000000060107C6 (SCOM)
Description	This is debug macro configuration register 2 for the front-end 1 component.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	INST2_SP_COUNT_LT: Timeout counter to_cmp compare value for dbg_cond_comp_1.

Register Name	Debug Trace 0 Register
Mnemonic	TP.TCXB.XB.EPS.DBG.DBG_TRACE_REG_0
Address	00000000060107CD (SCOM)
Description	This is debug macro configuration register 10 for the debug back-end component.

Bits	SCOM	Field Mnemonic: Description
0	RW	INST1_COND3_ENABLE: This bit enables of instance 1 condition 3.
1	RW	INST2_COND3_ENABLE: This bit enables of instance 2 condition 3.
2	RW	INST3_COND3_ENABLE: Unused.
3	RW	INST4_COND3_ENABLE: Unused.
4	RW	INST1_SLOW_LFSR_MODE: This bit enables slow LFSR mode for front-end instance 1.
5	RW	INST2_SLOW_LFSR_MODE: This bit enables slow LFSR mode for front-end instance 2.
6	RW	INST3_SLOW_LFSR_MODE: Unused.
7	RW	INST4_SLOW_LFSR_MODE: Unused.
8:9	RW	INST1_CONDITION1_TRIG_SEL: This field selects instance 1 condition 1 for output (external) triggers: 00 = do nothing. 01 = trigger_out(0). 10 = trigger_out(1). 11 = trigger_out(2).
10:11	RW	INST1_CONDITION2_TRIG_SEL: This field selects instance 1 condition 2 for output (external) triggers: 00 = do nothing. 01 = trigger_out(0). 10 = trigger_out(1). 11 = trigger_out(2).
12:13	RW	INST1_C2_TIMEOUT_TRIG_SEL: This field selects instance 1 condition 2 time-out counter for output: 00 = do nothing. 01 = trigger_out(0). 10 = trigger_out(1). 11 = trigger_out(2).
14:15	RW	INST2_CONDITION1_TRIG_SEL: This field selects instance 2 condition 1 for output (external) triggers: 00 = do nothing. 01 = trigger_out(0). 10 = trigger_out(1). 11 = trigger_out(2).
16:17	RW	INST2_CONDITION2_TRIG_SEL: This field selects instance 2 condition 2 trigger for output (external) triggers: 00 = do nothing. 01 = trigger_out(0). 10 = trigger_out(1). 11 = trigger_out(2).
18:19	RW	INST2_C2_TIMEOUT_TRIG_SEL: This field selects instance 2 condition 2 time-out counter for output: 00 = do nothing. 01 = trigger_out(0). 10 = trigger_out(1). 11 = trigger_out(2).
20:31	RO	constant = 0b000000000000
32	RW	EXT_TRIG_ON_STOP: This bit enables trigger on stop.
33	RW	EXT_TRIG_ON_FREEZE: This bit enables trigger on freeze.
34:38	RW	CORE_RAS0_TRIG_SEL:

Bits	SCOM	Field Mnemonic: Description
39:43	RW	CORE_RAS1_TRIG_SEL:
44:45	RW	PC_TP_TRIG_SEL:
46:49	RW	DBG_ARM_SEL:
50:53	RW	TRIG0_LEVEL_SEL: This field selects additional conditions for output (external) trigger signal trigger_out(0). **Note:** Some are N/A (inst3/4 conditions are tied to zero). 0001 = inst1_cond3_state_int(1). 0010 = inst1_cond3_state_int(0). 0011 = inst2_cond3_state_int(1). 0100 = inst2_cond3_state_int(0). 0101 = inst3_cond3_state_int(1). 0110 = inst3_cond3_state_int(0). 0111 = inst4_cond3_state_int(1). 1000 = inst4_cond3_state_int(0). 1001 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1). 1010 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1). 1011 = inst3_cond3_state_int(1) or inst4_cond3_state_int(1). 1100 = inst3_cond3_state_int(1) and inst4_cond3_state_int(1). 1101 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1). 1110 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1) and inst3_cond3_state_int(1). 1111 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1) or inst4_cond3_state_int(1).
54:57	RW	TRIG1_LEVEL_SEL: This field selects additional conditions for output (external) trigger signal trigger_out(1). **Note:** Some are N/A (inst3/4 conditions are tied to zero). 0001 = inst1_cond3_state_int(1). 0010 = inst1_cond3_state_int(0). 0011 = inst2_cond3_state_int(1). 0100 = inst2_cond3_state_int(0). 0101 = inst3_cond3_state_int(1). 0110 = inst3_cond3_state_int(0). 0111 = inst4_cond3_state_int(1). 1000 = inst4_cond3_state_int(0). 1001 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1). 1010 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1). 1011 = inst3_cond3_state_int(1) or inst4_cond3_state_int(1). 1100 = inst3_cond3_state_int(1) and inst4_cond3_state_int(1). 1101 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1). 1110 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1) and inst3_cond3_state_int(1). 1111 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1) or inst4_cond3_state_int(1).
58:63	RO	constant = 0b000000

Register Name	**Debug Trace 1 Register**
Mnemonic	TP.TCXB.XB.EPS.DBG.DBG_TRACE_REG_1
Address	00000000060107CE (SCOM)
Description	This is debug macro configuration register 11 for the back-end component.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	INST1_CONDITION1_ACTION_DO: Instance 1 action selection, condition 1: 00 = nothing 01 = start 10 = stop 11 = run-N: start now, stop after n cycles
2:3	RW	INST1_CONDITION2_ACTION_DO: Instance 1 action selection, condition 2: 00 = nothing 01 = start 10 = stop 11 = run-N: start now, stop after n cycles
4:5	RW	INST1_C2_TIMEOUT_ACTION_DO: Instance 1 action selection, c2_timeout: 00 = nothing 01 = start 10 = stop 11 = run-N: start now, stop after n cycles
6:7	RW	INST2_CONDITION1_ACTION_DO: Instance 2 action selection, condition 1: 00 = nothing 01 = start 10 = stop 11 = run-N: start now, stop after n cycles
8:9	RW	INST2_CONDITION2_ACTION_DO: Instance 2 action selection, condition 2: 00 = nothing 01 = start 10 = stop 11 = run-N: start now, stop after n cycles
10:11	RW	INST2_C2_TIMEOUT_ACTION_DO: Instance 2 action selection, c2_timeout: 00 = nothing 01 = start 10 = stop 11 = run-N: start now, stop after n cycles
12:23	RO	constant = 0b000000000000
24	RW	INST1_CONDITION1_ACTION_WAITN: For wait-N.
25	RW	INST1_CONDITION2_ACTION_WAITN: For wait-N.
26	RW	INST1_C2_TIMEOUT_ACTION_WAITN: For wait-N.
27	RW	INST2_CONDITION1_ACTION_WAITN: For wait-N.
28	RW	INST2_CONDITION2_ACTION_WAITN: For wait-N.
29	RW	INST2_C2_TIMEOUT_ACTION_WAITN: For wait-N.
30:35	RO	constant = 0b000000
36	RW	INST1_CONDITION1_ACTION_BANK: Trace bank switch (instance 1, condition1).
37	RW	INST1_CONDITION2_ACTION_BANK: Trace bank switch (instance 1, condition2).
38	RW	INST1_C2_TIMEOUT_ACTION_BANK: Trace bank switch (instance 1, c2_timeout).
39	RW	INST2_CONDITION1_ACTION_BANK: Trace bank switch (instance 2, condition1).
40	RW	INST2_CONDITION2_ACTION_BANK: Trace bank switch (instance 2, condition2).
41	RW	INST2_C2_TIMEOUT_ACTION_BANK: Trace bank switch (instance 2, c2_timeout).
42:47	RO	constant = 0b000000

Bits	SCOM	Field Mnemonic: Description
48:50	RW	INST1_CHECKSTOP_MODE_LT: Select an additional condition with fir_error_lt for dbg_fir_xstop_on_trig output: 000 = inst1_condition1_lt. 001 = inst1_condition2_lt. 010 = inst1_condition3_lt. 011 = inst1_cond2_timeout_lt. 1XX = Disable checkstop_mode.
51	RW	INST1_CHECKSTOP_MODE_SELECTOR: enable_fir_trig_xstop: Enable a checkstop on the debug trigger: 0 = Disable a checkstop on the debug trigger 1 = Enable a checkstop on the debug trigger
52:54	RW	INST2_CHECKSTOP_MODE_LT: Select an additional condition with fir_error_lt for dbg_fir_xstop_on_trig output: 000 = inst2_condition1_lt. 001 = inst2_condition2_lt. 010 = inst2_condition3_lt. 011 = inst2_cond2_timeout_lt. 1XX = Disable checkstop_mode.
55	RW	INST2_CHECKSTOP_MODE_SELECTOR: enable_fir_error_xstop: Enable a checkstop on a FIR error: 0 = Disable a checkstop on a FIR error. 1 = Enable a checkstop on a FIR error.
56:63	RO	constant = 0b00000000

Register Name	**Debug Trace Mode 2 Register**
Mnemonic	TP.TCXB.XB.EPS.DBG.DBG_TRACE_MODE_REG_2
Address	00000000060107CF (SCOM)
Description	This is debug macro configuration register 12 for the back-end component.

Bits	SCOM	Field Mnemonic: Description
0:15	RW	RUNN_COUNT_COMPARE_VALUE: Compare value for the run-N counter used in trace modes run-N and wait-N.
16	RW	IMM_FREEZE_MODE: Immediate freeze mode.
17	RW	STOP_ON_ERR: Stop and freeze on checkstop.
18	RW	BANK_ON_RUNN_MATCH: Bank switch on run-N match.
19	RW	FORCE_TEST_MODE: FORCE run-N condition to be true.
20	RW	ACCUM_HIST_MODE: Accumulate history mode; do not clear history mode when trace_run is active.
21	RW	FRZ_COUNT_ON_FRZ: Freeze condition counters on trace freeze.

Register Name	**Debug Trace Control Register**
Mnemonic	TP.TCXB.XB.EPS.DBG.DEBUG_TRACE_CONTROL
Address	00000000060107D0 (SCOM)
Description	This is the trace start/stop/rest using SCOM command register. This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0	WOX	Reserved field.
1	WOX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
2	WOX	Reserved field.

Register Name	Extra Trace Mode Register
Mnemonic	TP.TCXB.XB.EPS.DBG.XTRA_TRACE_MODE
Address	00000000060107D1 (SCOM)
Description	This register provides an extra or dedicated trace mode register for core triggers

Bits	SCOM	Field Mnemonic: Description
0:37	RW	XTRA_TRACE_MODE_DATA: Extra or dedicated trace mode register for core triggers.

Register Name	PPE FIR Register
Mnemonic	IOFPPE.PPE.PPE_FIR_REG
Address	0000000006010840 (SCOM) 0000000006010841 (SCOM1) 0000000006010842 (SCOM2)
Description	This is the PPE Fault Isolation Register (FIR) for the chip pervasive logic.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:3	RWX	WOX_AND	WOX_OR	PPE_FIR_ERROR: PPE FIR; PPE general error.
4	RWX	WOX_AND	WOX_OR	PPE_FIR_HALTED: PPE FIR; PPE halted.
5	RWX	WOX_AND	WOX_OR	PPE_FIR_WATCHDOG_TIMEOUT: PPE FIR; PPE watchdog timer timed out.
6	RWX	WOX_AND	WOX_OR	PPE_MMIO_FIR_DATA_IN: PPE FIR; MMIO data in error.
7	RWX	WOX_AND	WOX_OR	ARB_FIR_MISSED_SCRUB_TICK: PPE FIR; The arbiter missed a scrub tick.
8	RWX	WOX_AND	WOX_OR	ARB_FIR_ARY_UE: PPE FIR; An arbiter array UE error occurred.
9	RWX	WOX_AND	WOX_OR	ARB_FIR_ARY_CE: PPE FIR; An arbiter array CE error occurred.
10	RWX	WOX_AND	WOX_OR	RESERVED: PPE FIR; Reserved FIR bit.
11	RWX	WOX_AND	WOX_OR	FIR_SCOMFIR_ERROR: FIR; A SCOM FSM or FIR register parity error occurred.
12	RWX	WOX_AND	WOX_OR	FIR_SCOMFIR_ERROR_CLONE: FIR; A SCOM FSM or FIR register parity error occurred.
13:26	RO	RO	RO	constant = 0b00000000000000

Register Name	PPE FIR Mask Register
Mnemonic	IOFPPE.PPE.PPE_FIR_MASK_REG
Address	0000000006010843 (SCOM) 0000000006010844 (SCOM1) 0000000006010845 (SCOM2)
Description	This register masks an interrupt when a bit changes in the PPE FIR Register. (Action0,Mask) = Action Select (0,0) = Recoverable Error (0,1) = Masked

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:3	RWX	WOX_AND	WOX_OR	PPE_FIR_ERROR_MASK: This field masks a PPE general error.
4	RWX	WOX_AND	WOX_OR	PPE_FIR_HALTED_MASK: This bit masks the PPE halted error.
5	RWX	WOX_AND	WOX_OR	PPE_FIR_WATCHDOG_TIMEOUT_MASK: This bit masks the PPE watchdog timer timed out.
6	RWX	WOX_AND	WOX_OR	PPE_MMIO_FIR_DATA_IN_MASK: This bit masks the MMIO data in error.
7	RWX	WOX_AND	WOX_OR	ARB_FIR_MISSED_SCRUB_TICK_MASK: This bit masks the arbiter missed a scrub tick error.
8	RWX	WOX_AND	WOX_OR	ARB_FIR_ARY_UE_MASK: This bit masks the arbiter array UE error.
9	RWX	WOX_AND	WOX_OR	ARB_FIR_ARY_CE_MASK: This bit masks the arbiter array CE error.
10	RWX	WOX_AND	WOX_OR	RESERVED_MASK: This bit masks a reserved FIR bit.
11	RWX	WOX_AND	WOX_OR	INTERNAL_SCOM_ERROR_MASK: This bit is the internal SCOM error mask.
12	RWX	WOX_AND	WOX_OR	INTERNAL_SCOM_ERROR_MASK_CLONE: This bit is the internal SCOM error mask clone.
13:26	RO	RO	RO	constant = 0b00000000000000

Register Name	Fault Isolation Action0 Register
Mnemonic	IOFPPE.PPE.PPE_FIR_ACTION0_REG
Address	0000000006010846 (SCOM)
Description	This is the fault isolation action 0 register.

Bits	SCOM	Field Mnemonic: Description
0:12	RW	PPE_FIR_ACTION0: Action 0 for FIR(0:12).
13:26	RO	constant = 0b00000000000000

Register Name	Fault Isolation Action1 Register
Mnemonic	IOFPPE.PPE.PPE_FIR_ACTION1_REG
Address	0000000006010847 (SCOM)
Description	This is the fault isolation action 1 register.

Bits	SCOM	Field Mnemonic: Description
0:12	RW	PPE_FIR_ACTION1: Action 1 for FIR(0:12).
13:26	RO	constant = 0b00000000000000

Register Name	FIR WOF Register
Mnemonic	IOFPPE.PPE.PPE_FIR_WOF_REG
Address	0000000006010848 (SCOM)
Description	This who's on first register indicates which error occurred first. This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:12	RWX_WCLRREG	Reserved field.
13:26	RO	constant = 0b00000000000000

Register Name	PPE Local SRAM Control Register
Mnemonic	IOFPPE.PPE.ARB.ARB.CSCR
Address	000000000601084A (SCOM) 000000000601084B (SCOM1) 000000000601084C (SCOM2)
Description	This register contains PPE local SRAM controls.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_CLEAR	WO_OR	CSCR_SRAM_ACCESS_MODE: SRAM access mode.
1	RWX	WOX_CLEAR	WOX_OR	CSCR_SRAM_SCRUB_ENABLE: Enable background scrub (atomic read-write) to periodically check, and if needed correct, the data in the SRAM for bit flips due to alpha particles. This bit is cleared by the hardware when a UE is detected to assist with fault analysis.
2	RW	WO_CLEAR	WO_OR	CSCR_ECC_CORRECT_DIS: Do not correct the data coming out of the array on ECC-detected correctable errors. This causes CEs to report an error back to the PPE in addition to the usual UEs.
3	RW	WO_CLEAR	WO_OR	CSCR_ECC_DETECT_DIS: Do not flag an error back to the PPE for ECC miscompares. Data from the SRAM is always treated as good. **Note:** Errors are always detected and reported to the FIR. They must be masked there independently from this bit.
4	RW	WO_CLEAR	WO_OR	CSCR_ECC_INJECT_TYPE: Used only when ECC_INJECT_ERR is set. When set to 1, this bit causes an ECC error to be reported on every SRAM read. When 0, this bit causes a single ECC error to be indicated on the next SRAM read that occurs because it also clears ECC_INJECT_ERR when that happens.
5	RWX	WOX_CLEAR	WOX_OR	CSCR_ECC_INJECT_ERR: When set, the hardware injects or causes a fake uncorrectable error (UE) to be reported to both the PPE and the FIR on all SRAM reads. The SRAM contents are not modified. The type of error to inject is determined by the previous bit. If ECC_INJECT_TYPE = 1, this bit clears when the first error is injected. **Note:** This bit can also be set by the PPE local register CFMSR.
6:7	RW	WO_CLEAR	WO_OR	CSCR_SPARE_6_7: Implemented but unused.
8:46	RO	RO	RO	constant = 0b000000000000000000000000000000000000000
47:59	RWX	WOX_CLEAR	WOX_OR	CSCR_SRAM_SCRUB_INDEX: 32KB Scrub index. This field is auto-incremented by hardware for every scrub operation. Upon a UE detection, this field is overwritten with the index of the doubleword containing the error. **Note:** SRAM_SCRUB_ENABLE must be set to 0 when writing this field to prevent one cycle window from ignoring this write if a scrub update happens to occur concurrently.
60:63	RO	RO	RO	constant = 0b0000

Register Name	PPE Local SRAM Address Register
Mnemonic	IOFPPE.PPE.ARB.ARB.CSAR
Address	000000000601084D (SCOM)
Description	This register contains the address of an SRAM entry.

Bits	SCOM	Field Mnemonic: Description
0:15	RO	constant = 0b0000000000000000
16:28	RW	CSAR_SRAM_ADDRESS: This field contains the address of an 8-byte SRAM entry in the 32 KB SRAM array.
29:63	RO	constant = 0b00000000000000000000000000000000000

Register Name	PPE Local SRAM Data Register
Mnemonic	IOFPPE.PPE.ARB.ARB.CSDR
Address	000000000601084E (SCOM)
Description	This register contains the data associated with the SRAM entry at the address indicated in the PPE Local SRAM Address Register.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	CSDR_SRAM_DATA: This field contains the 8-byte SRAM data entry for the address given by the SRAM_ADDRESS. Reads cause this register to be written with data from the local SRAM. Writes cause the local SRAM to be written with the contents of this register.

Register Name	PPE External Interface External Control Register
Mnemonic	IOFPPE.PPE.PPE.PPE.PPE.PPE_XIXCR
Address	0000000006010850 (SCOM)
Description	This register contains the PPE External Control Register command.

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:3	WOX	PPE_XIXCR_XCR: PPE External Control Register command. 000 = Clear Debug Status. 001 = Halt. 010 = Resume. 011 = Single-step. 100 = Toggle XSR[TRH]. 101 = Soft Reset. 110 = Hard Reset. 111 = Force Halt.
4:63	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000

Register Name	PPE External Interface RAMRA Register
Mnemonic	IOFPPE.PPE.PPE.PPE.PPE.PPE_XIRAMRA
Address	0000000006010851 (SCOM)
Description	This register provides access to the PPE core's XIR1 debug register.

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:3	WOX	PPE_XIXCR_XCR: PPE External Control Register command. 000 = Clear Debug Status. 001 = Halt. 010 = Resume. 011 = Single-step. 100 = Toggle XSR[TRH]. 101 = Soft Reset. 110 = Hard Reset. 111 = Force Halt.
4:31	RO	constant = 0b0000000000000000000000000000
32:63	WOX	PPE_XIRAMRA_SPRG0: SPRG0 register value. By convention, this field is used by the PPE code to keep status information. SPRG0 is a 32-bit scratch register. SPRG0 can only be written as an XIR when the processor is halted (XSR[HS] = '1').

Register Name	PPE External Interface RAMGA Register
Mnemonic	IOFPPE.PPE.PPE.PPE.PPE.PPE_XIRAMGA
Address	0000000006010852 (SCOM)
Description	This register provides access to the PPE core's XIR2 debug register.

Bits	SCOM	Field Mnemonic: Description
0:31	WOX	PPE_XIRAMGA_IR: PPE Instruction Register. Writes to this field cause a RAM operation. This field can only be written when the processor is halted (XSR[HS] = '1'). This field provides the requested PPE instruction to execute.
32:63	WOX	PPE_XIRAMRA_SPRG0: SPRG0 register value. By convention, this field is used by the PPE code to keep status information. SPRG0 is a 32-bit scratch register. SPRG0 can only be written as an XIR when the processor is halted (XSR[HS] = '1').

Register Name	PPE External Interface RAMDBG Register
Mnemonic	IOFPPE.PPE.PPE.PPE.PPE.PPE_XIRAMDBG
Address	0000000006010853 (SCOM)
Description	This register provides access to the PPE core's XIR3 debug register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1:3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.
7	ROX	Reserved field.
8	ROX	Reserved field.
9:11	ROX	NULL_MSR_SIBRC:
12	ROX	Reserved field.
13	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
14	ROX	NULL_MSR_WE:
15	ROX	Reserved field.
16:19	ROX	Reserved field.
20	ROX	NULL_MSR_LP:
21	ROX	Reserved field.
22:23	RO	constant = 0b00
24	ROX	Reserved field.
25	ROX	Reserved field.
26:27	RO	constant = 0b00
28	ROX	Reserved field.
29:31	ROX	Reserved field.
32:63	RWX	PPE_XIRAMRA_SPRG0: SPRG0 register value. By convention, this field is used by the PPE code to keep status information. SPRG0 is a 32-bit scratch register. SPRG0 can only be written as an XIR when the processor is halted (XSR[HS] = '1').

Register Name	PPE External Interface RAMEDR Register
Mnemonic	IOFPPE.PPE.PPE.PPE.PPE.PPE_XIRAMEDR
Address	0000000006010854 (SCOM)
Description	This register provides access to the PPE core's XIR4 debug register.

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	PPE_XIRAMGA_IR: PPE Instruction Register. Writes to this field cause a RAM operation. This field can only be written when the processor is halted (XSR[HS] = '1'). This field provides the requested PPE instruction to execute.
32:63	ROX	PPE_XIRAMEDR_EDR: Error Data Register. These bits are set on PPE interrupts caused by an error.

Register Name	PPE External Interface DBGPRO Register
Mnemonic	IOFPPE.PPE.PPE.PPE.PPE.PPE_XIDBGPRO
Address	0000000006010855 (SCOM)
Description	PPE External Interface DBGPRO Register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1:3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.
7	ROX	Reserved field.
8	ROX	Reserved field.
9:11	ROX	NULL_MSR_SIBRC:
12	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
13	ROX	Reserved field.
14	ROX	NULL_MSR_WE:
15	ROX	Reserved field.
16:19	ROX	Reserved field.
20	ROX	NULL_MSR_LP:
21	ROX	Reserved field.
22:23	RO	constant = 0b00
24	ROX	Reserved field.
25	ROX	Reserved field.
26:27	RO	constant = 0b00
28	ROX	Reserved field.
29:31	ROX	Reserved field.
32:61	RWX	Reserved field.
62:63	RO	constant = 0b00

Register Name	External Interface Memory Information Register
Mnemonic	IOFPPE.PPE.PPE.PPE.MIB.MIB_XIMEM
Address	0000000006010857 (SCOM)
Description	Memory interface bolt-on (MIB) registers enable the programmable PowerPC-lite engine (PPE) to access its local memory and pervasive interconnect bus (PIB) interface. This register accesses memory information.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MIB_XIMEM_MEM_ADDR: This field contains the byte address of the current or previous transaction in the MEM transaction buffer.
32	ROX	MIB_XIMEM_MEM_R_NW: This bit indicates the transaction type of the current or previous transaction in the MEM transaction buffer. 1 = Read. 0 = Write.
33	ROX	MIB_XIMEM_MEM_BUSY: This bit indicates if the transaction buffer is occupied with an ongoing transaction. “Busy” is cleared when the transaction is completed.
34	ROX	MIB_XIMEM_MEM_IMPRECISE_ERROR_PENDING: This bit indicates that the current or previous transaction had an imprecise error. It is cleared when it is reported back to the PPE. **Note:** The address of the erroneous transaction is copied into the SGB address latches such that the memory interface can continue to service I-fetches.
35:42	ROX	MIB_XIMEM_MEM_BYTE_ENABLE: This field contains byte enables of the current or previous transaction in the MEM transaction buffer.
43	ROX	MIB_XIMEM_MEM_LINE_MODE: This bit indicates the line mode of the current or previous transaction in the MEM transaction buffer. When set to `1', it indicates a 32-byte read request.
44:48	RO	constant = 0b00000
49:51	ROX	MIB_XIMEM_MEM_ERROR: MEM transaction buffer error code. The current or previous transaction got an error on the memory interface when this field is non-zero.
52:61	RO	constant = 0b0000000000

Bits	SCOM	Field Mnemonic: Description
62	ROX	MIB_XIMEM_MEM_IFETCH_PENDING: When set to '1', this bit indicates that an instruction fetch is pending on the MEM interface.
63	ROX	MIB_XIMEM_MEM_DATAOP_PENDING: When set to '1', this bit indicates that a data transaction is pending on the MEM interface.

Register Name	**External Interface Store Gather Buffer Information Register**
Mnemonic	IOFPPE.PPE.PPE.PPE.MIB.MIB_XISGB
Address	0000000006010858 (SCOM)
Description	This register contains store gather buffer (SGB) information.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MIB_XISGB_STORE_ADDRESS: This field contains either the SGB address 4-byte tag or the address of an imprecise store error that occurred when performing a previous data transaction.
32:34	RO	constant = 0b000
35	ROX	MIB_XIMEM_MEM_IMPRECISE_ERROR_PENDING: This bit indicates that the current or previous transaction had an imprecise error. It is cleared when it is reported back to the PPE. **Note:** The address of the erroneous transaction is copied into the SGB address latches such that the memory interface can continue to service I-fetches.
36:39	ROX	MIB_XISGB_SGB_BYTE_VALID: This field contains byte valid bits within the 4-byte tag. It is cleared when the SGB contents are committed. This means that they are either flushed to memory or copied into the transaction buffer. **Note:** These bits can never be set if an MEM imprecise error is pending.
40:62	RO	constant = 0b00000000000000000000000
63	ROX	MIB_XISGB_SGB_FLUSH_PENDING: When set to '1'. this bit indicates that a store gather buffer flush to memory is pending on the MEM interface. This can only happen if MEM_BUSY in the MEM transaction buffer is '0'.

Register Name	**External Interface Instruction Cache Information Register**
Mnemonic	IOFPPE.PPE.PPE.PPE.MIB.MIB_XIICAC
Address	0000000006010859 (SCOM)
Description	This register contains instruction cache information.

Bits	SCOM	Field Mnemonic: Description
0:26	ROX	Reserved field.
27:31	RO	constant = 0b00000
32	ROX	Reserved field.
33	RO	constant = 0b0
34	ROX	Reserved field.
35	ROX	MIB_XIMEM_MEM_IFETCH_PENDING: When set to '1', this bit indicates that an instruction fetch is pending on the MEM interface.
36:39	ROX	Reserved field.
40:43	ROX	Reserved field.
44	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
45	ROX	Reserved field.
46	ROX	Reserved field.
47	ROX	Reserved field.
48:63	RO	constant = 0b0000000000000000

Register Name	PPE Miscellaneous Control Register
Mnemonic	IOFPPE.SCOM_PPE_CNTL
Address	0000000006010860 (SCOM)
Description	This register contains miscellaneous PPE controls.

Bits	SCOM	Field Mnemonic: Description
0	RW	SCOM_PPE_IORESET: This bit resets the I/O-specific logic in the PPE macro. (This does not actually reset the PPE or ARB logic.)
1	RW	SCOM_PPE_PDWN: This bit powers down I/O-specific logic in the PPE macro. (This does not actually reset the PPE or ARB logic.)
2	RW	SCOM_PPE_INTERRUPT: This bit manually forces an external interrupt in the PPE.
3	RW	SCOM_PPE_ARB_ECC_INJECT_ERR: This bit forces an ECC error in the memory arbiter.
4:15	RW	SCOM_PPE_SPARES: This field contains PPE miscellaneous control spares.
16:31	RO	constant = 0b0000000000000000

Register Name	PPE Work Register 1
Mnemonic	IOFPPE.SCOM_PPE_WORK_REG1
Address	0000000006010861 (SCOM)
Description	This is the first PPE Work Register.

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	SCOM_PPE_WORK1: PPE Work Register field 1.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	PPE Work Register 2
Mnemonic	IOFPPE.SCOM_PPE_WORK_REG2
Address	0000000006010862 (SCOM)
Description	This is the second PPE Work Register.

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	SCOM_PPE_WORK2: PPE Work Register field 2.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	PPE Flag Register
Mnemonic	IOFPPE.SCOM_PPE_FLAGS
Address	0000000006010863 (SCOM) 0000000006010864 (SCOM1) 0000000006010865 (SCOM2)
Description	This register contains the PPE flags.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:15	RWX	WOX_OR	WOX_CLEAR	SCOM_PPE_FLAGS_FIELD: PPE flags register field.
16:31	RO	RO	RO	constant = 0b0000000000000000

Register Name	Pervasive FIR Register
Mnemonic	IOF1.BUSCTL.SCOM.FIR_REG
Address	0000000006011000 (SCOM) 0000000006011001 (SCOM1) 0000000006011002 (SCOM2)
Description	This is the local Fault Isolation Register (FIR) for the chip pervasive logic.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_RX_INVALID_STATE_OR_PARITY_ERROR: This bit indicates that a receive state machine parity error or mode register parity error occurred.
1	RWX	WOX_AND	WOX_OR	FIR_TX_INVALID_STATE_OR_PARITY_ERROR: This bit indicates that a transmit state machine parity error or mode register parity error occurred.
2	RWX	WOX_AND	WOX_OR	FIR_GCR_HANG_ERROR: This bit indicates that the per-bus GCR ring hang detector error occurred.
3:7	RWX	WOX_AND	WOX_OR	RESERVED3_7: Reserved.
8	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_TRAINING_ERROR: This bit indicates that an initialization training error occurred on bus 0.
9	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_SPARE_DEPLOYED: This bit indicates that a spare lane was deployed to repair another lane on bus 0.
10	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_MAX_SPARES_EXCEEDED: This bit indicates that the maximum number of spare lanes was exceeded on bus 0. The bus is no longer capable of transferring data.
11	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_RECAL_OR_DYN_REPAIR_ERROR: This bit indicates that a bus recalibration or dynamic repair error occurred on bus 0.
12	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_TOO_MANY_BUS_ERRORS: This bit indicates that a bus experienced too many random lane errors on bus 0.
13:15	RWX	WOX_AND	WOX_OR	RESERVED13_15: Reserved.
16	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_TRAINING_ERROR: This bit indicates that an initialization training error occurred on bus 1.
17	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_SPARE_DEPLOYED: This bit indicates that a spare lane was deployed to repair another lane on bus 1.
18	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_MAX_SPARES_EXCEEDED: This bit indicates that the maximum number of spare lanes was exceeded on bus 1. The bus is no longer capable of transferring data.
19	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_RECAL_OR_DYN_REPAIR_ERROR: This bit indicates that a bus recalibration or dynamic repair error occurred on bus 1.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
20	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_TOO_MANY_BUS_ERRORS: This bit indicates that a bus experienced too many random lane errors on bus 1.
21:23	RWX	WOX_AND	WOX_OR	RESERVED21_23: Reserved.
24	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_TRAINING_ERROR: This bit indicates that an initialization training error occurred on bus 2.
25	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_SPARE_DEPLOYED: This bit indicates that a spare lane was deployed to repair another lane on bus 2.
26	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_MAX_SPARES_EXCEEDED: This bit indicates that the maximum number of spare lanes has been exceeded on bus 2. The bus is no longer capable of transferring data.
27	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_RECAL_OR_DYN_REPAIR_ERROR: This bit indicates that a bus recalibration or dynamic repair error occurred on bus 2.
28	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_TOO_MANY_BUS_ERRORS:This bit indicates that a bus experienced too many random lane errors on bus 2.
29:31	RWX	WOX_AND	WOX_OR	RESERVED29_31: Reserved.
32	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_TRAINING_ERROR: This bit indicates that an initialization training error occurred on bus 3.
33	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_SPARE_DEPLOYED: This bit indicates that a spare lane was deployed to repair another lane on bus 3.
34	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_MAX_SPARES_EXCEEDED: This bit indicates that the maximum number of spare lanes was exceeded on bus 3. The bus is no longer capable of transferring data.
35	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_RECAL_OR_DYN_REPAIR_ERROR: This bit indicates that a bus recalibration or dynamic repair error occurred on bus 3.
36	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_TOO_MANY_BUS_ERRORS: This bit indicates that a bus experienced too many random lane errors on bus 3.
37:39	RWX	WOX_AND	WOX_OR	RESERVED37_39: Reserved.
40	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_TRAINING_ERROR: This bit indicates that an initialization training error occurred on bus 4.
41	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_SPARE_DEPLOYED: This bit indicates that a spare lane was deployed to repair another lane on bus 4.
42	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_MAX_SPARES_EXCEEDED: This bit indicates that the maximum number of spare lanes was exceeded on bus 4. The bus is no longer capable of transferring data.
43	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_RECAL_OR_DYN_REPAIR_ERROR: This bit indicates that a bus recalibration or dynamic repair error has occurred on bus 4.
44	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_TOO_MANY_BUS_ERRORS: This bit indicates that a bus experienced too many random lane errors on bus 4.
45:47	RWX	WOX_AND	WOX_OR	RESERVED45_47: Reserved.
48	RWX	WOX_AND	WOX_OR	FIR_SCOMFIR_ERROR: This bit indicates that a SCOM FSM or FIR register parity error occurred.
49	RWX	WOX_AND	WOX_OR	FIR_SCOMFIR_ERROR_CLONE: This bit indicates that a SCOM FSM or FIR register parity error occurred.
50:63	RO	RO	RO	constant = 0b00000000000000

Register Name	Pervasive FIR Mask Register
Mnemonic	IOF1.BUSCTL.SCOM.FIR_MASK_REG
Address	0000000006011003 (SCOM) 0000000006011004 (SCOM1) 0000000006011005 (SCOM2)
Description	This register provides a bit mask for the Pervasive FIR Register. (Action0,Mask) = Action Select (0,0) = Recoverable Error (0,1) = Masked

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_RX_INVALID_STATE_OR_PARITY_ERROR_MASK: This bit masks the receive state machine parity error or mode register parity error.
1	RWX	WOX_AND	WOX_OR	FIR_TX_INVALID_STATE_OR_PARITY_ERROR_MASK: This bit masks the transmit state machine parity error or mode register parity error.
2	RWX	WOX_AND	WOX_OR	FIR_GCR_HANG_ERROR_MASK: This bit masks the GCR ring hang detector error.
3:7	RWX	WOX_AND	WOX_OR	RESERVED3_7_MASK: Reserved.
8	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_TRAINING_ERROR_MASK: This bit masks the initialization training error on bus 0.
9	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_SPARE_DEPLOYED_MASK: This bit masks the spare lane has been deployed indication on bus 0.
10	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_MAX_SPARES_EXCEEDED_MASK: This bit masks the maximum number of spare lanes has been exceeded error on bus 0.
11	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_RECAL_OR_DYN_REPAIR_ERROR_MASK: This bit masks the bus recalibration or dynamic repair error on bus 0.
12	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_TOO_MANY_BUS_ERRORS_MASK: This bit masks the too many random lane errors on bus 0.
13:15	RWX	WOX_AND	WOX_OR	RESERVED13_15_MASK: Reserved.
16	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_TRAINING_ERROR_MASK: This bit masks the initialization training error on bus 1.
17	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_SPARE_DEPLOYED_MASK: This bit masks the spare lane has been deployed indication on bus 1.
18	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_MAX_SPARES_EXCEEDED_MASK: This bit masks the maximum number of spare lanes has been exceeded error on bus 1.
19	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_RECAL_OR_DYN_REPAIR_ERROR_MASK: This bit masks the bus recalibration or dynamic repair error on bus 1.
20	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_TOO_MANY_BUS_ERRORS_MASK: This bit masks the too many random lane errors on bus 1.
21:23	RWX	WOX_AND	WOX_OR	RESERVED21_23_MASK: Reserved.
24	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_TRAINING_ERROR_MASK: This bit masks the initialization training error on bus 2.
25	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_SPARE_DEPLOYED_MASK: This bit masks the spare lane has been deployed indication on bus 2.
26	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_MAX_SPARES_EXCEEDED_MASK: This bit masks the maximum number of spare lanes has been exceeded error on bus 2.
27	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_RECAL_OR_DYN_REPAIR_ERROR_MASK: This bit masks the bus recalibration or dynamic repair error on bus 2.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
28	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_TOO_MANY_BUS_ERRORS_MASK: This bit masks the too many random lane errors on bus 2.
29:31	RWX	WOX_AND	WOX_OR	RESERVED29_31_MASK: Reserved.
32	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_TRAINING_ERROR_MASK: This bit masks the initialization training error on bus 3.
33	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_SPARE_DEPLOYED_MASK: This bit masks the spare lane has been deployed indication on bus 3.
34	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_MAX_SPARES_EXCEEDED_MASK: This bit masks the maximum number of spare lanes has been exceeded error on bus 3.
35	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_RECAL_OR_DYN_REPAIR_ERROR_MASK: This bit masks the bus recalibration or dynamic repair error on bus 3.
36	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_TOO_MANY_BUS_ERRORS_MASK: This bit masks the too many random lane errors on bus 3.
37:39	RWX	WOX_AND	WOX_OR	RESERVED37_39_MASK: Reserved.
40	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_TRAINING_ERROR_MASK: This bit masks the initialization training error on bus 4.
41	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_SPARE_DEPLOYED_MASK: This bit masks the spare lane has been deployed indication on bus 4.
42	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_MAX_SPARES_EXCEEDED_MASK: This bit masks the maximum number of spare lanes has been exceeded error on bus 4.
43	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_RECAL_OR_DYN_REPAIR_ERROR_MASK: This bit masks the bus recalibration or dynamic repair error on bus 4.
44	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_TOO_MANY_BUS_ERRORS_MASK: This bit masks the too many random lane errors on bus 4.
45:47	RWX	WOX_AND	WOX_OR	RESERVED45_47_MASK: Reserved.
48	RWX	WOX_AND	WOX_OR	INTERNAL_SCOM_ERROR_MASK: This bit is the internal SCOM error mask.
49	RWX	WOX_AND	WOX_OR	INTERNAL_SCOM_ERROR_MASK_CLONE: This bit is the internal SCOM error mask clone.
50:63	RO	RO	RO	constant = 0b00000000000000

Register Name	Fault Isolation Action0 Register
Mnemonic	IOF1.BUSCTL.SCOM.FIR_ACTION0_REG
Address	0000000006011006 (SCOM)
Description	This is the Fault Isolation Action0 Register.

Bits	SCOM	Field Mnemonic: Description
0:49	RW	FIR_ACTION0: Action 0 for FIR(0:49).
50:63	RO	constant = 0b00000000000000

Register Name	Fault Isolation Action1 Register
Mnemonic	IOF1.BUSCTL.SCOM.FIR_ACTION1_REG
Address	0000000006011007 (SCOM)
Description	This is the Fault Isolation Action1 Register.

Bits	SCOM	Field Mnemonic: Description
0:49	RW	FIR_ACTION1: Action 1 for FIR(0:49).
50:63	RO	constant = 0b00000000000000

Register Name	FIR WOF Register
Mnemonic	IOF1.BUSCTL.SCOM.FIR_WOF_REG
Address	0000000006011008 (SCOM)
Description	This who's on first register indicates which error occurred first.

Bits	SCOM	Field Mnemonic: Description
0:49	RWX_WCLRREG	Reserved field.
50:63	RO	constant = 0b00000000000000

Register Name	Normal SCOM Mode Register
Mnemonic	IOF1.BUSCTL.SCOM.SCOM_MODE_PB
Address	0000000006011020 (SCOM)
Description	This is the normal SCOM mode register.

Bits	SCOM	Field Mnemonic: Description
0	RWX	GCR_TEST_MODE: This bit puts the register logic into GCR test mode, which allows all read/write registers to be read and written by the diagnostic code to verify all register accesses. This mode gates off both logic inputs to the registers and the outputs from the logic. The outputs are gated to their scan flush value.
1	RWX	ENABLE_GCR_OFL_BUFF: This bit enables the second GCR overflow buffer. One buffer is used by default.
2	RWX	IORESET_HARD_BUS0: This bit enables an I/O hard reset per-bus and a GCR reset.
3	RWX	MMIO_PG_REG_ACCESS: MMIO PG register access is blocked by default. Setting this bit high grants MMIO access to the PG registers.
4:7	RWX	SCOM_MODE_PB_SPARES1: This field contains SCOM mode register spares.
8:10	RWX	GCR_HANG_DET_SEL: This field is used to select the GCR hang detect threshold.
11	ROX	GCR_BUFFER_ENABLED_RO_SIGNAL: This flag indicates that the extra GCR buffer is active. If the SCOM GCR enable buffer is off, it means that the hang threshold was reached.
12	RWX	GCR_HANG_ERROR_MASK: This bit is a mask for the GCR hang error when the second buffer is enabled.
13	RWX	GCR_HANG_ERROR_INJ: This bit is an inject for the GCR hang error.
14	RWX	PPE_GCR_MODE: This bit puts the register logic into GCR test mode, which allows all read/write registers to be read and written by the diagnostic code to verify all register accesses. This mode gates off both logic inputs to the registers as well as the outputs from the logic. The outputs are gated to their scan flush value.
15:22	RWX	CHAN_FAIL_MASK: This field is a channel fail mask.
23:30	RWX	SCOM_MODE_PB_SPARES2: This field contains SCOM mode register spares.

Bits	SCOM	Field Mnemonic: Description
31:63	RO	constant = 0b000000000000000000000000000000000

Register Name	Pervasive FIR Register
Mnemonic	IOF2.BUSCTL.SCOM.FIR_REG
Address	0000000006011400 (SCOM) 0000000006011401 (SCOM1) 0000000006011402 (SCOM2)
Description	This is the local Fault Isolation Register (FIR) for the chip pervasive logic.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_RX_INVALID_STATE_OR_PARITY_ERROR: This bit indicates that a receive state machine parity error or mode register parity error occurred.
1	RWX	WOX_AND	WOX_OR	FIR_TX_INVALID_STATE_OR_PARITY_ERROR: This bit indicates that a transmit state machine parity error or mode register parity error occurred.
2	RWX	WOX_AND	WOX_OR	FIR_GCR_HANG_ERROR: This bit indicates that the per-bus GCR ring hang detector error occurred.
3:7	RWX	WOX_AND	WOX_OR	RESERVED3_7: Reserved.
8	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_TRAINING_ERROR: This bit indicates that an initialization training error occurred on bus 0.
9	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_SPARE_DEPLOYED: This bit indicates that a spare lane was deployed to repair another lane on bus 0.
10	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_MAX_SPARES_EXCEEDED: This bit indicates that the maximum number of spare lanes was exceeded on bus 0. The bus is no longer capable of transferring data.
11	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_RECAL_OR_DYN_REPAIR_ERROR: This bit indicates that a bus recalibration or dynamic repair error occurred on bus 0.
12	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_TOO_MANY_BUS_ERRORS: This bit indicates that a bus experienced too many random lane errors on bus 0.
13:15	RWX	WOX_AND	WOX_OR	RESERVED13_15: Reserved.
16	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_TRAINING_ERROR: This bit indicates that an initialization training error occurred on bus 1.
17	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_SPARE_DEPLOYED: This bit indicates that a spare lane was deployed to repair another lane on bus 1.
18	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_MAX_SPARES_EXCEEDED: This bit indicates that the maximum number of spare lanes was exceeded on bus 1. The bus is no longer capable of transferring data.
19	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_RECAL_OR_DYN_REPAIR_ERROR: This bit indicates that a bus recalibration or dynamic repair error occurred on bus 1.
20	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_TOO_MANY_BUS_ERRORS: This bit indicates that a bus experienced too many random lane errors on bus 1.
21:23	RWX	WOX_AND	WOX_OR	RESERVED21_23: Reserved.
24	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_TRAINING_ERROR: This bit indicates that an initialization training error occurred on bus 2.
25	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_SPARE_DEPLOYED: This bit indicates that a spare lane was deployed to repair another lane on bus 2.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
26	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_MAX_SPARES_EXCEEDED: This bit indicates that the maximum number of spare lanes has been exceeded on bus 2. The bus is no longer capable of transferring data.
27	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_RECAL_OR_DYN_REPAIR_ERROR: This bit indicates that a bus recalibration or dynamic repair error occurred on bus 2.
28	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_TOO_MANY_BUS_ERRORS:This bit indicates that a bus experienced too many random lane errors on bus 2.
29:31	RWX	WOX_AND	WOX_OR	RESERVED29_31: Reserved.
32	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_TRAINING_ERROR: This bit indicates that an initialization training error occurred on bus 3.
33	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_SPARE_DEPLOYED: This bit indicates that a spare lane was deployed to repair another lane on bus 3.
34	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_MAX_SPARES_EXCEEDED: This bit indicates that the maximum number of spare lanes was exceeded on bus 3. The bus is no longer capable of transferring data.
35	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_RECAL_OR_DYN_REPAIR_ERROR: This bit indicates that a bus recalibration or dynamic repair error occurred on bus 3.
36	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_TOO_MANY_BUS_ERRORS: This bit indicates that a bus experienced too many random lane errors on bus 3.
37:39	RWX	WOX_AND	WOX_OR	RESERVED37_39: Reserved.
40	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_TRAINING_ERROR: This bit indicates that an initialization training error occurred on bus 4.
41	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_SPARE_DEPLOYED: This bit indicates that a spare lane was deployed to repair another lane on bus 4.
42	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_MAX_SPARES_EXCEEDED: This bit indicates that the maximum number of spare lanes was exceeded on bus 4. The bus is no longer capable of transferring data.
43	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_RECAL_OR_DYN_REPAIR_ERROR: This bit indicates that a bus recalibration or dynamic repair error occurred on bus 4.
44	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_TOO_MANY_BUS_ERRORS: This bit indicates that a bus experienced too many random lane errors on bus 4.
45:47	RWX	WOX_AND	WOX_OR	RESERVED45_47: Reserved
48	RWX	WOX_AND	WOX_OR	FIR_SCOMFIR_ERROR: This bit indicates that a SCOM FSM or FIR register parity error occurred.
49	RWX	WOX_AND	WOX_OR	FIR_SCOMFIR_ERROR_CLONE: This bit indicates that a SCOM FSM or FIR register parity error occurred.
50:63	RO	RO	RO	constant = 0b00000000000000

Register Name	Pervasive FIR Mask Register
Mnemonic	IOF2.BUSCTL.SCOM.FIR_MASK_REG
Address	0000000006011403 (SCOM) 0000000006011404 (SCOM1) 0000000006011405 (SCOM2)
Description	This register provides a bit mask for the Pervasive FIR Register. (Action0,Mask) = Action Select (0,0) = Recoverable Error (0,1) = Masked

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_RX_INVALID_STATE_OR_PARITY_ERROR_MASK: This bit masks the receive state machine parity error or mode register parity error.
1	RWX	WOX_AND	WOX_OR	FIR_TX_INVALID_STATE_OR_PARITY_ERROR_MASK: This bit masks the transmit state machine parity error or mode register parity error.
2	RWX	WOX_AND	WOX_OR	FIR_GCR_HANG_ERROR_MASK: This bit masks the GCR ring hang detector error.
3:7	RWX	WOX_AND	WOX_OR	RESERVED3_7_MASK: Reserved.
8	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_TRAINING_ERROR_MASK: This bit masks the initialization training error on bus 0.
9	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_SPARE_DEPLOYED_MASK: This bit masks the spare lane has been deployed indication on bus 0.
10	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_MAX_SPARES_EXCEEDED_MASK: This bit masks the maximum number of spare lanes has been exceeded error on bus 0.
11	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_RECAL_OR_DYN_REPAIR_ERROR_MASK: This bit masks the bus recalibration or dynamic repair error on bus 0.
12	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_TOO_MANY_BUS_ERRORS_MASK: This bit masks the too many random lane errors on bus 0.
13:15	RWX	WOX_AND	WOX_OR	RESERVED13_15_MASK: Reserved.
16	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_TRAINING_ERROR_MASK: This bit masks the initialization training error on bus 1.
17	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_SPARE_DEPLOYED_MASK: This bit masks the spare lane has been deployed indication on bus 1.
18	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_MAX_SPARES_EXCEEDED_MASK: This bit masks the maximum number of spare lanes has been exceeded error on bus 1.
19	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_RECAL_OR_DYN_REPAIR_ERROR_MASK: This bit masks the bus recalibration or dynamic repair error on bus 1.
20	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_TOO_MANY_BUS_ERRORS_MASK: This bit masks the too many random lane errors on bus 1.
21:23	RWX	WOX_AND	WOX_OR	RESERVED21_23_MASK: Reserved.
24	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_TRAINING_ERROR_MASK: This bit masks the initialization training error on bus 2.
25	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_SPARE_DEPLOYED_MASK: This bit masks the spare lane has been deployed indication on bus 2.
26	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_MAX_SPARES_EXCEEDED_MASK: This bit masks the maximum number of spare lanes has been exceeded error on bus 2.
27	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_RECAL_OR_DYN_REPAIR_ERROR_MASK: This bit masks the bus recalibration or dynamic repair error on bus 2.
28	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_TOO_MANY_BUS_ERRORS_MASK: This bit masks the too many random lane errors on bus 2.
29:31	RWX	WOX_AND	WOX_OR	RESERVED29_31_MASK: Reserved.
32	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_TRAINING_ERROR_MASK: This bit masks the initialization training error on bus 3.
33	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_SPARE_DEPLOYED_MASK: This bit masks the spare lane has been deployed indication on bus 3.
34	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_MAX_SPARES_EXCEEDED_MASK: This bit masks the maximum number of spare lanes has been exceeded error on bus 3.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
35	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_RECAL_OR_DYN_REPAIR_ERROR_MASK: This bit masks the bus recalibration or dynamic repair error on bus 3.
36	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_TOO_MANY_BUS_ERRORS_MASK: This bit masks the too many random lane errors on bus 3.
37:39	RWX	WOX_AND	WOX_OR	RESERVED37_39_MASK: Reserved.
40	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_TRAINING_ERROR_MASK: This bit masks the initialization training error on bus 4.
41	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_SPARE_DEPLOYED_MASK: This bit masks the spare lane has been deployed indication on bus 4.
42	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_MAX_SPARES_EXCEEDED_MASK: This bit masks the maximum number of spare lanes has been exceeded error on bus 4.
43	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_RECAL_OR_DYN_REPAIR_ERROR_MASK: This bit masks the bus recalibration or dynamic repair error on bus 4.
44	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_TOO_MANY_BUS_ERRORS_MASK: This bit masks the too many random lane errors on bus 4.
45:47	RWX	WOX_AND	WOX_OR	RESERVED45_47_MASK: Reserved.
48	RWX	WOX_AND	WOX_OR	INTERNAL_SCOM_ERROR_MASK: This bit is the internal SCOM error mask.
49	RWX	WOX_AND	WOX_OR	INTERNAL_SCOM_ERROR_MASK_CLONE: This bit is the internal SCOM error mask clone.
50:63	RO	RO	RO	constant = 0b00000000000000

Register Name	Fault Isolation Action0 Register
Mnemonic	IOF2.BUSCTL.SCOM.FIR_ACTION0_REG
Address	0000000006011406 (SCOM)
Description	This is the Fault Isolation Action0 Register.

Bits	SCOM	Field Mnemonic: Description
0:49	RW	FIR_ACTION0: Action 0 for FIR(0:49).
50:63	RO	constant = 0b00000000000000

Register Name	Fault Isolation Action1 Register
Mnemonic	IOF2.BUSCTL.SCOM.FIR_ACTION1_REG
Address	0000000006011407 (SCOM)
Description	This is the Fault Isolation Action1 Register.

Bits	SCOM	Field Mnemonic: Description
0:49	RW	FIR_ACTION1: Action 1 for FIR(0:49).
50:63	RO	constant = 0b00000000000000

Register Name	FIR WOF Register
Mnemonic	IOF2.BUSCTL.SCOM.FIR_WOF_REG
Address	0000000006011408 (SCOM)
Description	This who's on first register indicates which error occurred first.

Bits	SCOM	Field Mnemonic: Description
0:49	RWX_WCLRREG	Reserved field.
50:63	RO	constant = 0b00000000000000

Register Name	Normal SCOM Mode Register
Mnemonic	IOF2.BUSCTL.SCOM.SCOM_MODE_PB
Address	0000000006011420 (SCOM)
Description	This is the normal SCOM mode register.

Bits	SCOM	Field Mnemonic: Description
0	RWX	GCR_TEST_MODE: This bit puts the register logic into GCR test mode, which allows all read/write registers to be read and written by the diagnostic code to verify all register accesses. This mode gates off both logic inputs to the registers and the outputs from the logic. The outputs are gated to their scan flush value.
1	RWX	ENABLE_GCR_OFL_BUFF: This bit enables the second GCR overflow buffer. One buffer is used by default.
2	RWX	IORESET_HARD_BUS0: This bit enables an I/O hard reset per-bus and a GCR reset.
3	RWX	MMIO_PG_REG_ACCESS: MMIO PG register access is blocked by default. Setting this bit high grants MMIO access to the PG registers.
4:7	RWX	SCOM_MODE_PB_SPARES1: This field contains SCOM mode register spares.
8:10	RWX	GCR_HANG_DET_SEL: This field is used to select the GCR hang detect threshold.
11	ROX	GCR_BUFFER_ENABLED_RO_SIGNAL: This flag indicates that the extra GCR buffer is active. If the SCOM GCR enable buffer is off, it means that the hang threshold was reached.
12	RWX	GCR_HANG_ERROR_MASK: This bit is a mask for the GCR hang error when the second buffer is enabled.
13	RWX	GCR_HANG_ERROR_INJ: This bit is an inject for the GCR hang error.
14	RWX	PPE_GCR_MODE: This bit puts the register logic into GCR test mode, which allows all read/write registers to be read and written by the diagnostic code to verify all register accesses. This mode gates off both logic inputs to the registers as well as the outputs from the logic. The outputs are gated to their scan flush value.
15:22	RWX	CHAN_FAIL_MASK: This field is a channel fail mask.
23:30	RWX	SCOM_MODE_PB_SPARES2: This field contains SCOM mode register spares.
31:63	RO	constant = 0b000000000000000000000000000000000

Register Name	ELL FIR Register
Mnemonic	PB.IOE.LL0.IOEL_FIR_REG
Address	0000000006011800 (SCOM) 0000000006011801 (SCOM1) 0000000006011802 (SCOM2)
Description	This is the ELL Fault Isolation Register (FIR).

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_LINK0_TRAINED: Link 0 trained.
1	RWX	WOX_AND	WOX_OR	FIR_LINK1_TRAINED: Link 1 trained.
2:3	RWX	WOX_AND	WOX_OR	RESERVED.
4	RWX	WOX_AND	WOX_OR	FIR_LINK0_REPLAY_THRESHOLD: Link 0 replay threshold.
5	RWX	WOX_AND	WOX_OR	FIR_LINK1_REPLAY_THRESHOLD: Link 1 replay threshold.
6	RWX	WOX_AND	WOX_OR	FIR_LINK0_CRC_ERROR: Link 0 CRC error.
7	RWX	WOX_AND	WOX_OR	FIR_LINK1_CRC_ERROR: Link 1 CRC error.
8	RWX	WOX_AND	WOX_OR	FIR_LINK0_NAK_RECEIVED: Link 0 NAK received.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
9	RWX	WOX_AND	WOX_OR	FIR_LINK1_NAK_RECEIVED: Link 1 NAK received.
10	RWX	WOX_AND	WOX_OR	FIR_LINK0_REPLAY_BUFFER_FULL: Link 0 replay buffer full.
11	RWX	WOX_AND	WOX_OR	FIR_LINK1_REPLAY_BUFFER_FULL: Link 1 replay buffer full.
12	RWX	WOX_AND	WOX_OR	FIR_LINK0_SL_ECC_THRESHOLD: Link 0 SL ECC threshold.
13	RWX	WOX_AND	WOX_OR	FIR_LINK1_SL_ECC_THRESHOLD: Link 1 SL ECC threshold.
14	RWX	WOX_AND	WOX_OR	FIR_LINK0_SL_ECC_CORRECTABLE: Link 0 SL ECC correctable.
15	RWX	WOX_AND	WOX_OR	FIR_LINK1_SL_ECC_CORRECTABLE: Link 1 SL ECC correctable.
16	RWX	WOX_AND	WOX_OR	FIR_LINK0_SL_ECC_UE: Link 0 SL ECC UE.
17	RWX	WOX_AND	WOX_OR	FIR_LINK1_SL_ECC_UE: Link 1 SL ECC UE.
18:39	RWX	WOX_AND	WOX_OR	RESERVED.
40	RWX	WOX_AND	WOX_OR	FIR_LINK0_TCOMPLETE_BAD: Link 0 complete bad.
41	RWX	WOX_AND	WOX_OR	FIR_LINK1_TCOMPLETE_BAD: Link 1 complete bad.
42:43	RWX	WOX_AND	WOX_OR	RESERVED.
44	RWX	WOX_AND	WOX_OR	FIR_LINK0_SPARE_DONE: Link 0 spare done.
45	RWX	WOX_AND	WOX_OR	FIR_LINK1_SPARE_DONE: Link 1 spare done.
46	RWX	WOX_AND	WOX_OR	FIR_LINK0_TOO_MANY_CRC_ERRORS: Link 0 too many CRC errors.
47	RWX	WOX_AND	WOX_OR	FIR_LINK1_TOO_MANY_CRC_ERRORS: Link 1 too many CRC errors.
48:50	RWX	WOX_AND	WOX_OR	RESERVED.
51	RWX	WOX_AND	WOX_OR	FIR_PSAVE_INVALID_STATE: Psave invalid state.
52	RWX	WOX_AND	WOX_OR	FIR_LINK0_CORRECTABLE_ARRAY_ERROR: Link 0 correctable array error.
53	RWX	WOX_AND	WOX_OR	FIR_LINK1_CORRECTABLE_ARRAY_ERROR: Link 1 correctable array error.
54	RWX	WOX_AND	WOX_OR	FIR_LINK0_UNCORRECTABLE_ARRAY_ERROR: Link 0 uncorrectable array error.
55	RWX	WOX_AND	WOX_OR	FIR_LINK1_UNCORRECTABLE_ARRAY_ERROR: Link 1 uncorrectable array error.
56	RWX	WOX_AND	WOX_OR	FIR_LINK0_TRAINING_FAILED: Link 0 training failed.
57	RWX	WOX_AND	WOX_OR	FIR_LINK1_TRAINING_FAILED: Link 1 training failed.
58	RWX	WOX_AND	WOX_OR	FIR_LINK0_UNRECOVERABLE_ERROR: Link 0 unrecoverable error.
59	RWX	WOX_AND	WOX_OR	FIR_LINK1_UNRECOVERABLE_ERROR: Link 1 unrecoverable error.
60	RWX	WOX_AND	WOX_OR	FIR_LINK0_INTERNAL_ERROR: Link 0 internal error.
61	RWX	WOX_AND	WOX_OR	FIR_LINK1_INTERNAL_ERROR: Link 1 internal error.
62	RWX	WOX_AND	WOX_OR	FIR_SCOM_ERR_DUP: FIR SCOM error dup.
63	RWX	WOX_AND	WOX_OR	FIR_SCOM_ERR: FIR SCOM error.

Register Name	ELL FIR Mask Register
Mnemonic	PB.IOE.LL0.IOEL_FIR_MASK_REG
Address	0000000006011803 (SCOM) 0000000006011804 (SCOM1) 0000000006011805 (SCOM2)
Description	This register provides a bit mask for the ELL FIR Register.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_LINK0_TRAINED_MASK: Link 0 trained mask.
1	RWX	WOX_AND	WOX_OR	FIR_LINK1_TRAINED_MASK: Link 1 trained mask.
2:3	RWX	WOX_AND	WOX_OR	RESERVED.
4	RWX	WOX_AND	WOX_OR	FIR_LINK0_REPLAY_THRESHOLD_MASK: Link 0 replay threshold mask.
5	RWX	WOX_AND	WOX_OR	FIR_LINK1_REPLAY_THRESHOLD_MASK: Link 1 replay threshold mask.
6	RWX	WOX_AND	WOX_OR	FIR_LINK0_CRC_ERROR_MASK: Link 0 CRC error mask.
7	RWX	WOX_AND	WOX_OR	FIR_LINK1_CRC_ERROR_MASK: Link 1 CRC error mask.
8	RWX	WOX_AND	WOX_OR	FIR_LINK0_NAK_RECEIVED_MASK: Link 0 NAK received mask.
9	RWX	WOX_AND	WOX_OR	FIR_LINK1_NAK_RECEIVED_MASK: Link 1 NAK received mask.
10	RWX	WOX_AND	WOX_OR	FIR_LINK0_REPLAY_BUFFER_FULL_MASK: Link 0 replay buffer full mask.
11	RWX	WOX_AND	WOX_OR	FIR_LINK1_REPLAY_BUFFER_FULL_MASK: Link 1 replay buffer full mask.
12	RWX	WOX_AND	WOX_OR	FIR_LINK0_SL_ECC_THRESHOLD_MASK: Link 0 SL ECC threshold mask.
13	RWX	WOX_AND	WOX_OR	FIR_LINK1_SL_ECC_THRESHOLD_MASK: Link 1 SL ECC threshold mask.
14	RWX	WOX_AND	WOX_OR	FIR_LINK0_SL_ECC_CORRECTABLE_MASK: Link 0 SL ECC correctable mask.
15	RWX	WOX_AND	WOX_OR	FIR_LINK1_SL_ECC_CORRECTABLE_MASK: Link 1 SL ECC correctable mask.
16	RWX	WOX_AND	WOX_OR	FIR_LINK0_SL_ECC_UE_MASK: Link 0 SL ECC UE mask.
17	RWX	WOX_AND	WOX_OR	FIR_LINK1_SL_ECC_UE_MASK: Link 1 SL ECC UE mask.
18:39	RWX	WOX_AND	WOX_OR	RESERVED.
40	RWX	WOX_AND	WOX_OR	FIR_LINK0_TCOMPLETE_BAD_MASK: Link 0 complete bad mask.
41	RWX	WOX_AND	WOX_OR	FIR_LINK1_TCOMPLETE_BAD_MASK: Link 1 complete bad mask.
42:43	RWX	WOX_AND	WOX_OR	RESERVED.
44	RWX	WOX_AND	WOX_OR	FIR_LINK0_SPARE_DONE_MASK: Link 0 spare done mask.
45	RWX	WOX_AND	WOX_OR	FIR_LINK1_SPARE_DONE_MASK: Link 1 spare done mask.
46	RWX	WOX_AND	WOX_OR	FIR_LINK0_TOO_MANY_CRC_ERRORS_MASK: Link 0 too many CRC errors mask.
47	RWX	WOX_AND	WOX_OR	FIR_LINK1_TOO_MANY_CRC_ERRORS_MASK: Link 1 too many CRC errors mask.
48:50	RWX	WOX_AND	WOX_OR	RESERVED.
51	RWX	WOX_AND	WOX_OR	FIR_PSAVE_INVALID_STATE_MASK: Psave invalid state mask.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
52	RWX	WOX_AND	WOX_OR	FIR_LINK0_CORRECTABLE_ARRAY_ERROR_MASK: Link 0 correctable array error mask.
53	RWX	WOX_AND	WOX_OR	FIR_LINK1_CORRECTABLE_ARRAY_ERROR_MASK: Link 1 correctable array error mask.
54	RWX	WOX_AND	WOX_OR	FIR_LINK0_UNCORRECTABLE_ARRAY_ERROR_MASK: Link 0 uncorrectable array error mask.
55	RWX	WOX_AND	WOX_OR	FIR_LINK1_UNCORRECTABLE_ARRAY_ERROR_MASK: Link 1 uncorrectable array error mask.
56	RWX	WOX_AND	WOX_OR	FIR_LINK0_TRAINING_FAILED_MASK: Link 0 training failed mask.
57	RWX	WOX_AND	WOX_OR	FIR_LINK1_TRAINING_FAILED_MASK: Link 1 training failed mask.
58	RWX	WOX_AND	WOX_OR	FIR_LINK0_UNRECOVERABLE_ERROR_MASK: Link 0 unrecoverable error mask.
59	RWX	WOX_AND	WOX_OR	FIR_LINK1_UNRECOVERABLE_ERROR_MASK: Link 1 unrecoverable error mask.
60	RWX	WOX_AND	WOX_OR	FIR_LINK0_INTERNAL_ERROR_MASK: Link 0 internal error mask.
61	RWX	WOX_AND	WOX_OR	FIR_LINK1_INTERNAL_ERROR_MASK: Link 1 internal error mask.
62	RWX	WOX_AND	WOX_OR	FIR_SCOM_ERR_DUP_MASK: FIR SCOM error dup mask.
63	RWX	WOX_AND	WOX_OR	FIR_SCOM_ERR_MASK: FIR SCOM error mask.

Register Name	**ELL FIR Action 0 Register**
Mnemonic	PB.IOE.LL0.IOEL_FIR_ACTION0_REG
Address	0000000006011806 (SCOM)
Description	This is the ELL Fault Isolation Action 0 Register.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	IOEL_FIR_ACTION0: processor bus FIR MSB of action select for corresponding bit in FIR. (Action0,Action1) = Action Select. (0,0) = Checkstop. (0,1) = Recoverable error to service processor. (1,0) = Special attention to service processor. (1,1) = Invalid.

Register Name	**ELL FIR Action 1 Register**
Mnemonic	PB.IOE.LL0.IOEL_FIR_ACTION1_REG
Address	0000000006011807 (SCOM)
Description	This is the ELL Fault Isolation Action 1 Register.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	IOEL_FIR_ACTION1: processor bus FIR LSB of action select for corresponding bit in FIR. (Action0,Action1) = Action Select. (0,0) = Checkstop. (0,1) = Recoverable error to service processor. (1,0) = Special attention to service processor. (1,1) = Invalid.

Register Name	FIR WOF Register
Mnemonic	PB.IOE.LL0.IOEL_FIR_WOF_REG
Address	0000000006011808 (SCOM)
Description	This who's on first register indicates which error occurred first.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	IOEL_FIR_WOF: The WOF Register locks on the first error.

Register Name	ELL Configuration Register
Mnemonic	PB.IOE.LL0.IOEL_CONFIG
Address	000000000601180A (SCOM)
Description	This register contains ELL configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_LINK_PAIR: When 1, the two links operate as a pair. When 0, only one link is used or they are independent.
1	RW	CONFIG_DISABLE_SL_ECC: When 1, disable spare lane ECC correction.
2	RW	CONFIG_CRC_LANE_ID: When 1, use lane IDs from CRC for lane sparing.
3	RW	CONFIG_EDPL_LANE_ID: When 1, use lane IDs from EDPL for lane sparing.
4	RW	CONFIG_SL_UE_CRC_ERR: When 1, UEs on the SL ECC cause the packet to be treated as a CRC error.
5	RW	CONFIG_REPORT_SL_CHKBIT_ERR: When 1, SL ECC single-bit errors on check bits are reported to the FIR.
6	RW	CONFIG_BW_SAMPLE_SIZE: When 1, use 256 packets for the sample (instead of 64).
7	RW	CONFIG_BW_WINDOW_SIZE: When 1, shorten the sample window.
8:11	RW	CONFIG_UNUSED1: Spare bits.
12:15	RW	CONFIG_PACKET_DELAY_LIMIT: This field indicates the number of cycles of delay of frame data that are required for the packet to be considered delayed or replayed. (0 is 16 cycles.)
16:19	RW	CONFIG_TDM_DELAY: This field indicates the adjustment factor of delay for entering or exiting TDM mode.
20	RW	CONFIG_AUTO_TDM_TX: When 1, use the transmit bandwidth for automatically entering TDM mode.
21	RW	CONFIG_AUTO_TDM_RX: When 1, use the receive bandwidth for automatically entering TDM mode.
22	RW	CONFIG_AUTO_TDM_AND_NOT_OR: When 1, both the bandwidth and error rate are needed. Otherwise, either the bandwidth or the error rate is needed.
23	RW	CONFIG_UNUSED2: Spare bits.
24:27	RW	CONFIG_AUTO_TDM_BW_DIFF: Bandwidth difference for auto-entry TMD mode.
28:31	RW	CONFIG_AUTO_TDM_ERROR_RATE: This field contains the error rate for the auto-entry TDM mode.
32:47	RW	CONFIG_UNUSED3: Spare bits.
48:51	RWX	CONFIG_TIMEOUT: This field contains the program timeout values, from 1 µs to 65 ms.
52:63	RWX	CONFIG_TIMER_1US: This field contains the program number of cycles in 1 µs.

Register Name	ELL Control Register
Mnemonic	PB.IOE.LL0.IOEL_CONTROL
Address	000000000601180B (SCOM)
Description	This register contains ELL control fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONTROL_UNUSED0A: Spare bits.
1	RW	LINK0_STARTUP: When 1, start initialization/training.
2:7	RW	CONTROL_UNUSED0B: Spare bits.
8:11	RWX	LINK0_ERR_INJ_COMMAND: This field contains the command to perform link error injection.
12:27	RWX	LINK0_ERR_INJ_COMMAND_LANES: This field indicates the lanes for an error-injection command.
28:31	RWX	LINK0_COMMAND: This field contains the command to perform an operation.
32	RW	CONTROL_UNUSED1A: Spare bits.
33	RW	LINK1_STARTUP: When 1, start initialization/training.
34:39	RW	CONTROL_UNUSED1B: Spare bits.
40:43	RWX	LINK1_ERR_INJ_COMMAND: This field contains the command to perform link error injection.
44:59	RWX	LINK1_ERR_INJ_COMMAND_LANES: This field indicates the lanes for an error-injection command.
60:63	RWX	LINK1_COMMAND: This field contains the command to perform an operation.

Register Name	ELL Secondary Configuration Register
Mnemonic	PB.IOE.LL0.IOEL_SEC_CONFIG
Address	000000000601180D (SCOM)
Description	This register contains additional ELL configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_ENABLE_ERR_INJ: When 1, enable error injection (LFSR runs).
1:15	RW	CONFIG_UNUSED4: Spare bits.
16:17	RW	CONFIG_SBE_ERROR_RATE: This field indicates the error-injection SBE rate.
18:23	RW	CONFIG_RAND_ERROR_RATE: This field indicates error-injection rate N (from 1 to 38). Probability is 2^{-N}.
24:47	RW	CONFIG_UNUSED5: Spare bits.
48:63	RW	CONFIG_EDPL_RATE: When 0, disable EDPL. Otherwise, this field indicates the number of packets between EDPL packets.

Register Name	ELL Latency Measurement Register
Mnemonic	PB.IOE.LL0.IOEL_LAT_MEASURE
Address	000000000601180E (SCOM)
Description	This register contains latency measurements.

Bits	SCOM	Field Mnemonic: Description
0	ROX	LINK0_ROUND_TRIP_VALID: When 1, the round-trip value is valid.
1	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
2:11	ROX	LINK0_ROUND_TRIP: This field indicates the round-trip time in cycles.
12	ROX	LINK1_ROUND_TRIP_VALID: When 1, the round-trip value is valid.
13	RO	constant = 0b0
14:23	ROX	LINK1_ROUND_TRIP: This field indicates the round-trip time in cycles.
24	ROX	LOCAL_LATENCY_DIFFERENCE_VALID: When 1, the local latency difference is valid.
25	ROX	LOCAL_LATENCY_LONGER_LINK: When 1, link 1 had the longer latency.
26:28	RO	constant = 0b000
29:35	ROX	LOCAL_LATENCY_DIFFERENCE: This field contains the received difference in latency between the links.
36	ROX	REMOTE_LATENCY_DIFFERENCE_VALID: When 1, the remote latency difference is valid.
37	ROX	REMOTE_LATENCY_LONGER_LINK: When 1, link 1 had the longer latency.
38:40	RO	constant = 0b000
41:47	ROX	REMOTE_LATENCY_DIFFERENCE: This field contains the transmit difference in latency between the links (as received by other side).
48	RO	constant = 0b0
49:55	RWX	LINK0_TOD_LATENCY: This field indicates the latency of TOD pulses for link 0.
56	RO	constant = 0b0
57:63	RWX	LINK1_TOD_LATENCY: This field indicates the latency of TOD pulses for link 1.

Register Name	ELL Link0 Information Register
Mnemonic	PB.IOE.LL0.IOEL_LINK0_INFO
Address	0000000006011814 (SCOM)
Description	This register contains information about link 0.

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	LINK0_MAX_TIMEOUT: This field indicates the maximum value reached by the timeout counter.
16	ROX	LINK0_FRAME_CAP_VALID: When 1, the error capture is valid.
17	ROX	LINK0_FRAME_CAP_INST: Array instance.
18	RO	constant = 0b0
19:23	ROX	LINK0_FRAME_CAP_ADDR: This field contains the array address of the captured error.
24:31	ROX	LINK0_FRAME_CAP_SYN: This field contains the syndrome of the captured error.
32	ROX	LINK0_REPLAY_CAP_VALID: When 1, the error capture is valid.
33	RO	constant = 0b0
34	ROX	LINK0_REPLAY_CAP_INST: Array instance.
35:36	RO	constant = 0b00
37:43	ROX	LINK0_REPLAY_CAP_ADDR: This field contains the array address of the captured error.
44:51	ROX	LINK0_REPLAY_CAP_SYN: This field contains the syndrome of the captured error.
52	ROX	LINK0_ACK_FIFO_CAP_VALID: When 1, the error capture is valid.
53:56	RO	constant = 0b0000
57:63	ROX	LINK0_ACK_FIFO_CAP_ADDR: This field contains the array address of the captured error.

Register Name	ELL Link1 Information Register
Mnemonic	PB.IOE.LL0.IOEL_LINK1_INFO
Address	0000000006011815 (SCOM)
Description	This register contains information about link 1.

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	LINK1_MAX_TIMEOUT: This field indicates the maximum value reached by the timeout counter.
16	ROX	LINK1_FRAME_CAP_VALID: When 1, the error capture is valid.
17	ROX	LINK1_FRAME_CAP_INST: Array instance.
18	RO	constant = 0b0
19:23	ROX	LINK1_FRAME_CAP_ADDR: This field contains the array address of the captured error.
24:31	ROX	LINK1_FRAME_CAP_SYN: This field contains the syndrome of the captured error.
32	ROX	LINK1_REPLAY_CAP_VALID: When 1, the error capture is valid.
33	RO	constant = 0b0
34	ROX	LINK1_REPLAY_CAP_INST: Array instance.
35:36	RO	constant = 0b00
37:43	ROX	LINK1_REPLAY_CAP_ADDR: This field contains the array address of the captured error.
44:51	ROX	LINK1_REPLAY_CAP_SYN: This field contains the syndrome of the captured error.
52	ROX	LINK1_ACK_FIFO_CAP_VALID: When 1, the error capture is valid.
53:56	RO	constant = 0b0000
57:63	ROX	LINK1_ACK_FIFO_CAP_ADDR: This field contains the array address of the captured error.

Register Name	ELL Link 0 Error Status Register
Mnemonic	PB.IOE.LL0.IOEL_LINK0_ERROR_STATUS
Address	0000000006011816 (SCOM)
Description	This register contains link 0 error status information.

Bits	SCOM	Field Mnemonic: Description
0	WOX	LINK0_RESET_KEEPER: Reset keeper for the Link 0 Error Status Register.
1:3	ROX	LINK0_ERROR_STATUS_CE: c_err_rpt for correctable array errors.
4:7	RO	constant = 0b0000
8:9	ROX	LINK0_ERROR_STATUS_UE: c_err_rpt for uncorrectable array errors.
10:15	RO	constant = 0b000000
16:17	ROX	LINK0_ERROR_STATUS_TRAIN: c_err_rpt for training errors.
18:23	RO	constant = 0b000000
24:34	ROX	LINK0_ERROR_STATUS_UNRECOV: c_err_rpt for unrecoverable errors.
35:43	RO	constant = 0b000000000
44:61	ROX	LINK0_ERROR_STATUS_INTERNAL: c_err_rpt for internal errors.
62:63	RO	constant = 0b00

Register Name	ELL Link 1 Error Status Register
Mnemonic	PB.IOE.LL0.IOEL_LINK1_ERROR_STATUS
Address	0000000006011817 (SCOM)
Description	This register contains link 1 error status information.

Bits	SCOM	Field Mnemonic: Description
0	WOX	LINK1_RESET_KEEPER: Reset keeper for the Link 1 Error Status Register.
1:3	ROX	LINK1_ERROR_STATUS_CE: c_err_rpt for correctable array errors.
4:7	RO	constant = 0b0000
8:9	ROX	LINK1_ERROR_STATUS_UE: c_err_rpt for uncorrectable array errors.
10:15	RO	constant = 0b000000
16:17	ROX	LINK1_ERROR_STATUS_TRAIN: c_err_rpt for training errors.
18:23	RO	constant = 0b000000
24:34	ROX	LINK1_ERROR_STATUS_UNRECOV: c_err_rpt for unrecoverable errors.
35:43	RO	constant = 0b000000000
44:61	ROX	LINK1_ERROR_STATUS_INTERNAL: c_err_rpt for internal errors.
62:63	RO	constant = 0b00

Register Name	ELL Replay Threshold Register
Mnemonic	PB.IOE.LL0.IOEL_REPLAY_THRESHOLD
Address	0000000006011818 (SCOM)
Description	This register contains replay threshold controls.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	THRESH_REPLAY_TB_SEL: Replay threshold timebase select.
4:7	RW	THRESH_REPLAY_TAP_SEL: Replay threshold tap select.
8:10	RW	THRESH_REPLAY_ENABLE: Replay threshold error enable.
11:25	RW	THRESH_REPLAY_UNUSED1: Spare bits.
26	RWX	THRESH_REPLAY_LINK0_CLEAR: Replay threshold counter clear.
27	RWX	THRESH_REPLAY_LINK1_CLEAR: Replay threshold counter clear.
28	RW	THRESH_REPLAY_DIS_TB_CLEAR: Threshold disable timebase clear.
29	RW	THRESH_REPLAY_DIS_TAP_CLEAR: Threshold disable tap clear.
30	RW	THRESH_REPLAY_DIS_TAP_STOP: Threshold disable tap stop.
31	RW	THRESH_REPLAY_UNUSED2: Spare bits.
32:47	ROX	THRESH_REPLAY_LINK0_COUNT: Replay threshold count.
48:63	ROX	THRESH_REPLAY_LINK1_COUNT: Replay threshold count.

Register Name	ELL SL ECC Threshold Register
Mnemonic	PB.IOE.LL0.IOEL_SL_ECC_THRESHOLD
Address	0000000006011819 (SCOM)
Description	This register contains SL ECC threshold controls.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	THRESH_SL_ECC_TB_SEL: SL ECC threshold timebase select.
4:7	RW	THRESH_SL_ECC_TAP_SEL: SL ECC threshold tap select.
8:9	RW	THRESH_SL_ECC_ENABLE: SL ECC threshold error enable.
10:25	RW	THRESH_SL_ECC_UNUSED1: Spare bits.
26	RWX	THRESH_SL_ECC_LINK0_CLEAR: SL ECC threshold counter clear.
27	RWX	THRESH_SL_ECC_LINK1_CLEAR: SL ECC threshold counter clear.
28	RW	THRESH_SL_ECC_DIS_TB_CLEAR: Threshold disable timebase clear.
29	RW	THRESH_SL_ECC_DIS_TAP_CLEAR: Threshold disable tap clear.
30	RW	THRESH_SL_ECC_DIS_TAP_STOP: Threshold disable tap stop.
31	RW	THRESH_SL_ECC_UNUSED2: Spare bits.
32:47	ROX	THRESH_SL_ECC_LINK0_COUNT: SL ECC Threshold count.
48:63	ROX	THRESH_SL_ECC_LINK1_COUNT: SL ECC Threshold count.

Register Name	ELL Error Injection LFSR Register
Mnemonic	PB.IOE.LL0.IOEL_ERR_INJ_LFSR
Address	000000000601181B (SCOM)
Description	This is the linear feedback shift register (LFSR) for error injection.

Bits	SCOM	Field Mnemonic: Description
0:60	RWX	ERR_INJ_LFSR: Error injection LFSR.
61:63	RO	constant = 0b000

Register Name	ELL Performance Monitor and Trace Configuration Register
Mnemonic	PB.IOE.LL0.IOEL_PERF_TRACE_CONFIG
Address	000000000601181C (SCOM)
Description	This register monitors and configures the performance counters and traces.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	CONFIG_ENABLE_PERF_0: Performance counter enable.
2:3	RW	CONFIG_ENABLE_PERF_1: Performance counter enable.
4:5	RW	CONFIG_ENABLE_PERF_2: Performance counter enable.
6:7	RW	CONFIG_ENABLE_PERF_3: Performance counter enable.
8:9	RW	CONFIG_ENABLE_PERF_4: Performance counter enable.
10:11	RW	CONFIG_ENABLE_PERF_5: Performance counter enable.

Bits	SCOM	Field Mnemonic: Description
12:13	RW	CONFIG_ENABLE_PERF_6: Performance counter enable.
14:15	RW	CONFIG_ENABLE_PERF_7: Performance counter enable.
16:17	RW	CONFIG_PERF_SIZE_0: Performance counter size.
18:19	RW	CONFIG_PERF_SIZE_1: Performance counter size.
20:21	RW	CONFIG_PERF_SIZE_2: Performance counter size.
22:23	RW	CONFIG_PERF_SIZE_3: Performance counter size.
24:25	RW	CONFIG_PERF_SIZE_4: Performance counter size.
26:27	RW	CONFIG_PERF_SIZE_5: Performance counter size.
28:29	RW	CONFIG_PERF_SIZE_6: Performance counter size.
30:31	RW	CONFIG_PERF_SIZE_7: Performance counter size.
32	RW	CONFIG_PMULET_FREEZE_MODE: PMUlet freeze mode: 0 = Freeze on full. 1 = Free run.
33	RW	CONFIG_COMMON_FREEZE_MODE: Common freeze mode: 0 = Independent per PMUlet. 1 = Any counter full freezes all.
34	RW	CONFIG_PERF_RESET_MODE: PMUlet reset mode: 0 = Reset on read. 1 = Reset on write.
35	RW	CONFIG_PERFTRACE_ENABLE: Performance trace enable. Multiplex performance trace data onto the trace bus.
36	RW	CONFIG_PERFTRACE_FIXED_WINDOW: Performance trace fixed window mode. Take a sample every 255 or 255 x 128 cycles.
37	RW	CONFIG_PERFTRACE_PRESCALE: Performance trace prescale mode, wide-angle view. Performance counts are prescaled by 128.
38:39	RW	CONFIG_PERFTRACE_MODE: Performance trace input selection.
40:51	RW	CONFIG_TRACE_CONFIG_0: Selection for trace bus bits 0:43.
52:63	RW	CONFIG_TRACE_CONFIG_1: Selection for trace bus bits 44:87.

Register Name	ELL Performance Monitor Selection Register
Mnemonic	PB.IOE.LL0.IOEL_PERF_SEL_CONFIG
Address	000000000601181D (SCOM)
Description	This register selects performance counters.

Bits	SCOM	Field Mnemonic: Description
0:7	RW	CONFIG_PERF_SELECT_0: Selection performance counter.
8:15	RW	CONFIG_PERF_SELECT_1: Selection performance counter.
16:23	RW	CONFIG_PERF_SELECT_2: Selection performance counter.
24:31	RW	CONFIG_PERF_SELECT_3: Selection performance counter.
32:39	RW	CONFIG_PERF_SELECT_4: Selection performance counter.
40:47	RW	CONFIG_PERF_SELECT_5: Selection performance counter.
48:55	RW	CONFIG_PERF_SELECT_6: Selection performance counter.

Bits	SCOM	Field Mnemonic: Description
56:63	RW	CONFIG_PERF_SELECT_7: Selection performance counter.

Register Name	ELL Performance Monitor Counter Register 0
Mnemonic	PB.IOE.LL0.IOEL_PERF_COUNTERS_0
Address	000000000601181E (SCOM)
Description	This register contains the 16 MSb of performance monitor counters 0 – 3.

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRREG	PERFMON_COUNTER_0: Performance counter 16 MSb.
16:31	RWX_WCLRREG	PERFMON_COUNTER_1: Performance counter 16 MSb.
32:47	RWX_WCLRREG	PERFMON_COUNTER_2: Performance counter 16 MSb.
48:63	RWX_WCLRREG	PERFMON_COUNTER_3: Performance counter 16 MSb.

Register Name	ELL Performance Monitor Counter Register 1
Mnemonic	PB.IOE.LL0.IOEL_PERF_COUNTERS_1
Address	000000000601181F (SCOM)
Description	This register contains the 16 MSb of performance monitor counters 4 – 7.

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRREG	PERFMON_COUNTER_4: Performance counter 16 MSb.
16:31	RWX_WCLRREG	PERFMON_COUNTER_5: Performance counter 16 MSb.
32:47	RWX_WCLRREG	PERFMON_COUNTER_6: Performance counter 16 MSb.
48:63	RWX_WCLRREG	PERFMON_COUNTER_7: Performance counter 16 MSb.

Register Name	ELL Performance Monitor Counter LSB Register 0
Mnemonic	PB.IOE.LL0.IOEL_PERF_COUNT_LSB_0
Address	0000000006011820 (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	RESERVED.

Register Name	ELL Performance Monitor Counter LSB Register 1
Mnemonic	PB.IOE.LL0.IOEL_PERF_COUNT_LSB_1
Address	0000000006011821 (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	RESERVED.

Register Name	ELL Link 0 Syndrome Capture Register
Mnemonic	PB.IOE.LL0.IOEL_LINK0_SYN_CAPTURE
Address	0000000006011822 (SCOM)
Description	This register contains syndrome information for captured link 0 errors.

Bits	SCOM	Field Mnemonic: Description
0:27	RWX	LINK0_LINK_CAP_CRC_SYN: This field contains the CRC syndrome for a captured link error.
28:35	RWX	LINK0_LINK_CAP_CRC_SYN_UNUSED1: Spare bits.
36:43	RWX	LINK0_LINK_CAP_SLECC_SYN0: This field contains SL ECC syndrome 0 for a captured link error.
44:51	RWX	LINK0_LINK_CAP_SLECC_SYN1: This field contains SL ECC syndrome 1 for a captured link error.
52:54	RWX	LINK0_LINK_CAP_CRC_SYN_UNUSED2: Spare bits.
55	RWX	LINK0_LINK_CAP_VALID: This bit indicates that the captured link error is valid.
56:58	RWX	LINK0_LINK_CAP_CRC_SYN_UNUSED3: Spare bits.
59:63	RWX	LINK0_LINK_CAP_CRC_LANE: This field contains the CRC lane from the syndrome decode.

Register Name	ELL Link 1 Syndrome Capture Register
Mnemonic	PB.IOE.LL0.IOEL_LINK1_SYN_CAPTURE
Address	0000000006011823 (SCOM)
Description	This register contains syndrome information for captured link 1 errors.

Bits	SCOM	Field Mnemonic: Description
0:27	RWX	LINK1_LINK_CAP_CRC_SYN: This field contains the CRC syndrome for a captured link error.
28:35	RWX	LINK1_LINK_CAP_CRC_SYN_UNUSED1: Spare bits.
36:43	RWX	LINK1_LINK_CAP_SLECC_SYN0: This field contains SL ECC syndrome 0 for a captured link error.
44:51	RWX	LINK1_LINK_CAP_SLECC_SYN1: This field contains SL ECC syndrome 1 for a captured link error.
52:54	RWX	LINK1_LINK_CAP_CRC_SYN_UNUSED2: Spare bits.
55	RWX	LINK1_LINK_CAP_VALID: This bit indicates that the captured link error is valid.
56:58	RWX	LINK1_LINK_CAP_CRC_SYN_UNUSED3: Spare bits.
59:63	RWX	LINK1_LINK_CAP_CRC_LANE: This field contains the CRC lane from the syndrome decode.

Register Name	ELL Link 0 EDPL Status Register
Mnemonic	PB.IOE.LL0.IOEL_LINK0_EDPL_STATUS
Address	0000000006011824 (SCOM)
Description	This register contains counts of EDPL errors.

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	LINK0_EDPL_ERROR_COUNT_0: Count of EDPL errors.
4:7	ROX	LINK0_EDPL_ERROR_COUNT_1: Count of EDPL errors.
8:11	ROX	LINK0_EDPL_ERROR_COUNT_2: Count of EDPL errors.

Bits	SCOM	Field Mnemonic: Description
12:15	ROX	LINK0_EDPL_ERROR_COUNT_3: Count of EDPL errors.
16:19	ROX	LINK0_EDPL_ERROR_COUNT_4: Count of EDPL errors.
20:23	ROX	LINK0_EDPL_ERROR_COUNT_5: Count of EDPL errors.
24:27	ROX	LINK0_EDPL_ERROR_COUNT_6: Count of EDPL errors.
28:31	ROX	LINK0_EDPL_ERROR_COUNT_7: Count of EDPL errors.
32:35	ROX	LINK0_EDPL_ERROR_COUNT_8: Count of EDPL errors.
36:39	ROX	LINK0_EDPL_ERROR_COUNT_9: Count of EDPL errors.
40:43	ROX	LINK0_EDPL_ERROR_COUNT_10: Count of EDPL errors.
44:47	ROX	LINK0_EDPL_ERROR_COUNT_11: Count of EDPL errors.
48:63	RO	constant = 0b0000000000000000

Register Name	ELL Link 1 EDPL Status Register
Mnemonic	PB.IOE.LL0.IOEL_LINK1_EDPL_STATUS
Address	0000000006011825 (SCOM)
Description	This register contains counts of EDPL errors.

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	LINK1_EDPL_ERROR_COUNT_0: Count of EDPL errors.
4:7	ROX	LINK1_EDPL_ERROR_COUNT_1: Count of EDPL errors.
8:11	ROX	LINK1_EDPL_ERROR_COUNT_2: Count of EDPL errors.
12:15	ROX	LINK1_EDPL_ERROR_COUNT_3: Count of EDPL errors.
16:19	ROX	LINK1_EDPL_ERROR_COUNT_4: Count of EDPL errors.
20:23	ROX	LINK1_EDPL_ERROR_COUNT_5: Count of EDPL errors.
24:27	ROX	LINK1_EDPL_ERROR_COUNT_6: Count of EDPL errors.
28:31	ROX	LINK1_EDPL_ERROR_COUNT_7: Count of EDPL errors.
32:35	ROX	LINK1_EDPL_ERROR_COUNT_8: Count of EDPL errors.
36:39	ROX	LINK1_EDPL_ERROR_COUNT_9: Count of EDPL errors.
40:43	ROX	LINK1_EDPL_ERROR_COUNT_10: Count of EDPL errors.
44:47	ROX	LINK1_EDPL_ERROR_COUNT_11: Count of EDPL errors.
48:63	RO	constant = 0b0000000000000000

Register Name	ELL Link 0 Link Quality Status Register
Mnemonic	PB.IOE.LL0.IOEL_LINK0_QUALITY
Address	0000000006011826 (SCOM)
Description	This register contains transmit and receive bandwidth and error-rate measurements.

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:11	ROX	LINK0_TX_BW: Measure of the transmit bandwidth.

Bits	SCOM	Field Mnemonic: Description
12	RO	constant = 0b0
13:23	ROX	LINK0_RX_BW: Measure of the receive bandwidth.
24	RO	constant = 0b0
25:47	ROX	LINK0_ERROR_RATE: Measure of the received error rate.
48:63	RO	constant = 0b0000000000000000

Register Name	ELL Link1 Link Quality Status Register
Mnemonic	PB.IOE.LL0.IOEL_LINK1_QUALITY
Address	0000000006011827 (SCOM)
Description	This register contains transmit and receive bandwidth and error-rate measurements.

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:11	ROX	LINK1_TX_BW: Measure of the transmit bandwidth.
12	RO	constant = 0b0
13:23	ROX	LINK1_RX_BW: Measure of the receive bandwidth.
24	RO	constant = 0b0
25:47	ROX	LINK1_ERROR_RATE: Measure of the received error rate.
48:63	RO	constant = 0b0000000000000000

Register Name	ELL Status Register
Mnemonic	PB.IOE.LL0.IOEL_DLL_STATUS
Address	0000000006011828 (SCOM)
Description	This register contains status information.

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b0000
4:7	ROX	LINK0_CURRENT_STATE: This field indicates the current state of the initialization/training state machine.
8:11	RO	constant = 0b0000
12:15	ROX	LINK0_PRIOR_STATE: This field indicates the prior state of the initialization/training state machine.
16:18	RO	constant = 0b000
19:23	ROX	LINK0_MAX_PKT_TIMER: This field contains the maximum value reached by the packet delay counter.
24:27	RO	constant = 0b0000
28:31	ROX	LINK1_CURRENT_STATE: This field indicates the current state of the initialization/training state machine.
32:35	RO	constant = 0b0000
36:39	ROX	LINK1_PRIOR_STATE: This field indicates the prior state of the initialization/training state machine.
40:42	RO	constant = 0b000
43:47	ROX	LINK1_MAX_PKT_TIMER: This field contains the maximum value reached by the packet delay counter.
48:63	RO	constant = 0b0000000000000000

Register Name	**ELL FIR Register**
Mnemonic	PB.IOE.LL1.IOEL_FIR_REG
Address	0000000006011C00 (SCOM) 0000000006011C01 (SCOM1) 0000000006011C02 (SCOM2)
Description	This is the ELL Fault Isolation Register (FIR).

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_LINK0_TRAINED: Link 0 trained.
1	RWX	WOX_AND	WOX_OR	FIR_LINK1_TRAINED: Link 1 trained.
2:3	RWX	WOX_AND	WOX_OR	RESERVED.
4	RWX	WOX_AND	WOX_OR	FIR_LINK0_REPLAY_THRESHOLD: Link 0 replay threshold.
5	RWX	WOX_AND	WOX_OR	FIR_LINK1_REPLAY_THRESHOLD: Link 1 replay threshold.
6	RWX	WOX_AND	WOX_OR	FIR_LINK0_CRC_ERROR: Link 0 CRC error.
7	RWX	WOX_AND	WOX_OR	FIR_LINK1_CRC_ERROR: Link 1 CRC error.
8	RWX	WOX_AND	WOX_OR	FIR_LINK0_NAK_RECEIVED: Link 0 NAK received.
9	RWX	WOX_AND	WOX_OR	FIR_LINK1_NAK_RECEIVED: Link 1 NAK received.
10	RWX	WOX_AND	WOX_OR	FIR_LINK0_REPLAY_BUFFER_FULL: Link 0 replay buffer full.
11	RWX	WOX_AND	WOX_OR	FIR_LINK1_REPLAY_BUFFER_FULL: Link 1 replay buffer full.
12	RWX	WOX_AND	WOX_OR	FIR_LINK0_SL_ECC_THRESHOLD: Link 0 SL ECC threshold.
13	RWX	WOX_AND	WOX_OR	FIR_LINK1_SL_ECC_THRESHOLD: Link 1 SL ECC threshold.
14	RWX	WOX_AND	WOX_OR	FIR_LINK0_SL_ECC_CORRECTABLE: Link 0 SL ECC correctable.
15	RWX	WOX_AND	WOX_OR	FIR_LINK1_SL_ECC_CORRECTABLE: Link 1 SL ECC correctable.
16	RWX	WOX_AND	WOX_OR	FIR_LINK0_SL_ECC_UE: Link 0 SL ECC UE.
17	RWX	WOX_AND	WOX_OR	FIR_LINK1_SL_ECC_UE: Link 1 SL ECC UE.
18:39	RWX	WOX_AND	WOX_OR	RESERVED.
40	RWX	WOX_AND	WOX_OR	FIR_LINK0_TCOMPLETE_BAD: Link 0 complete bad.
41	RWX	WOX_AND	WOX_OR	FIR_LINK1_TCOMPLETE_BAD: Link 1 complete bad.
42:43	RWX	WOX_AND	WOX_OR	RESERVED.
44	RWX	WOX_AND	WOX_OR	FIR_LINK0_SPARE_DONE: Link 0 spare done.
45	RWX	WOX_AND	WOX_OR	FIR_LINK1_SPARE_DONE: Link 1 spare done.
46	RWX	WOX_AND	WOX_OR	FIR_LINK0_TOO_MANY_CRC_ERRORS: Link 0 too many CRC errors.
47	RWX	WOX_AND	WOX_OR	FIR_LINK1_TOO_MANY_CRC_ERRORS: Link 1 too many CRC errors.
48:50	RWX	WOX_AND	WOX_OR	RESERVED.
51	RWX	WOX_AND	WOX_OR	FIR_PSAVE_INVALID_STATE: Psave invalid state.
52	RWX	WOX_AND	WOX_OR	FIR_LINK0_CORRECTABLE_ARRAY_ERROR: Link 0 correctable array error.
53	RWX	WOX_AND	WOX_OR	FIR_LINK1_CORRECTABLE_ARRAY_ERROR: Link 1 correctable array error.
54	RWX	WOX_AND	WOX_OR	FIR_LINK0_UNCORRECTABLE_ARRAY_ERROR: Link 0 uncorrectable array error.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
55	RWX	WOX_AND	WOX_OR	FIR_LINK1_UNCORRECTABLE_ARRAY_ERROR: Link 1 uncorrectable array error.
56	RWX	WOX_AND	WOX_OR	FIR_LINK0_TRAINING_FAILED: Link 0 training failed.
57	RWX	WOX_AND	WOX_OR	FIR_LINK1_TRAINING_FAILED: Link 1 training failed.
58	RWX	WOX_AND	WOX_OR	FIR_LINK0_UNRECOVERABLE_ERROR: Link 0 unrecoverable error.
59	RWX	WOX_AND	WOX_OR	FIR_LINK1_UNRECOVERABLE_ERROR: Link 1 unrecoverable error.
60	RWX	WOX_AND	WOX_OR	FIR_LINK0_INTERNAL_ERROR: Link 0 internal error.
61	RWX	WOX_AND	WOX_OR	FIR_LINK1_INTERNAL_ERROR: Link 1 internal error.
62	RWX	WOX_AND	WOX_OR	FIR_SCOM_ERR_DUP: FIR SCOM error dup.
63	RWX	WOX_AND	WOX_OR	FIR_SCOM_ERR: FIR SCOM error.

Register Name	ELL FIR Mask Register
Mnemonic	PB.IOE.LL1.IOEL_FIR_MASK_REG
Address	0000000006011C03 (SCOM) 0000000006011C04 (SCOM1) 0000000006011C05 (SCOM2)
Description	This register provides a bit mask for the ELL FIR Register.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_LINK0_TRAINED_MASK: Link 0 trained mask.
1	RWX	WOX_AND	WOX_OR	FIR_LINK1_TRAINED_MASK: Link 1 trained mask.
2:3	RWX	WOX_AND	WOX_OR	RESERVED.
4	RWX	WOX_AND	WOX_OR	FIR_LINK0_REPLAY_THRESHOLD_MASK: Link 0 replay threshold mask.
5	RWX	WOX_AND	WOX_OR	FIR_LINK1_REPLAY_THRESHOLD_MASK: Link 1 replay threshold mask.
6	RWX	WOX_AND	WOX_OR	FIR_LINK0_CRC_ERROR_MASK: Link 0 CRC error mask.
7	RWX	WOX_AND	WOX_OR	FIR_LINK1_CRC_ERROR_MASK: Link 1 CRC error mask.
8	RWX	WOX_AND	WOX_OR	FIR_LINK0_NAK_RECEIVED_MASK: Link 0 NAK received mask.
9	RWX	WOX_AND	WOX_OR	FIR_LINK1_NAK_RECEIVED_MASK: Link 1 NAK received mask.
10	RWX	WOX_AND	WOX_OR	FIR_LINK0_REPLAY_BUFFER_FULL_MASK: Link 0 replay buffer full mask.
11	RWX	WOX_AND	WOX_OR	FIR_LINK1_REPLAY_BUFFER_FULL_MASK: Link 1 replay buffer full mask.
12	RWX	WOX_AND	WOX_OR	FIR_LINK0_SL_ECC_THRESHOLD_MASK: Link 0 SL ECC threshold mask.
13	RWX	WOX_AND	WOX_OR	FIR_LINK1_SL_ECC_THRESHOLD_MASK: Link 1 SL ECC threshold mask.
14	RWX	WOX_AND	WOX_OR	FIR_LINK0_SL_ECC_CORRECTABLE_MASK: Link 0 SL ECC correctable mask.
15	RWX	WOX_AND	WOX_OR	FIR_LINK1_SL_ECC_CORRECTABLE_MASK: Link 1 SL ECC correctable mask.
16	RWX	WOX_AND	WOX_OR	FIR_LINK0_SL_ECC_UE_MASK: Link 0 SL ECC UE mask.
17	RWX	WOX_AND	WOX_OR	FIR_LINK1_SL_ECC_UE_MASK: Link 1 SL ECC UE mask.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
18:39	RWX	WOX_AND	WOX_OR	RESERVED.
40	RWX	WOX_AND	WOX_OR	FIR_LINK0_TCOMPLETE_BAD_MASK: Link 0 complete bad mask.
41	RWX	WOX_AND	WOX_OR	FIR_LINK1_TCOMPLETE_BAD_MASK: Link 1 complete bad mask.
42:43	RWX	WOX_AND	WOX_OR	RESERVED.
44	RWX	WOX_AND	WOX_OR	FIR_LINK0_SPARE_DONE_MASK: Link 0 spare done mask.
45	RWX	WOX_AND	WOX_OR	FIR_LINK1_SPARE_DONE_MASK: Link 1 spare done mask.
46	RWX	WOX_AND	WOX_OR	FIR_LINK0_TOO_MANY_CRC_ERRORS_MASK: Link 0 too many CRC errors mask.
47	RWX	WOX_AND	WOX_OR	FIR_LINK1_TOO_MANY_CRC_ERRORS_MASK: Link 1 too many CRC errors mask.
48:50	RWX	WOX_AND	WOX_OR	RESERVED.
51	RWX	WOX_AND	WOX_OR	FIR_PSAVE_INVALID_STATE_MASK: Psave invalid state mask.
52	RWX	WOX_AND	WOX_OR	FIR_LINK0_CORRECTABLE_ARRAY_ERROR_MASK: Link 0 correctable array error mask.
53	RWX	WOX_AND	WOX_OR	FIR_LINK1_CORRECTABLE_ARRAY_ERROR_MASK: Link 1 correctable array error mask.
54	RWX	WOX_AND	WOX_OR	FIR_LINK0_UNCORRECTABLE_ARRAY_ERROR_MASK: Link 0 uncorrectable array error mask.
55	RWX	WOX_AND	WOX_OR	FIR_LINK1_UNCORRECTABLE_ARRAY_ERROR_MASK: Link 1 uncorrectable array error mask.
56	RWX	WOX_AND	WOX_OR	FIR_LINK0_TRAINING_FAILED_MASK: Link 0 training failed mask.
57	RWX	WOX_AND	WOX_OR	FIR_LINK1_TRAINING_FAILED_MASK: Link 1 training failed mask.
58	RWX	WOX_AND	WOX_OR	FIR_LINK0_UNRECOVERABLE_ERROR_MASK: Link 0 unrecoverable error mask.
59	RWX	WOX_AND	WOX_OR	FIR_LINK1_UNRECOVERABLE_ERROR_MASK: Link 1 unrecoverable error mask.
60	RWX	WOX_AND	WOX_OR	FIR_LINK0_INTERNAL_ERROR_MASK: Link 0 internal error mask.
61	RWX	WOX_AND	WOX_OR	FIR_LINK1_INTERNAL_ERROR_MASK: Link 1 internal error mask.
62	RWX	WOX_AND	WOX_OR	FIR_SCOM_ERR_DUP_MASK: FIR SCOM error dup mask.
63	RWX	WOX_AND	WOX_OR	FIR_SCOM_ERR_MASK: FIR SCOM error mask.

Register Name	ELL FIR Action 0 Register
Mnemonic	PB.IOE.LL1.IOEL_FIR_ACTION0_REG
Address	0000000006011C06 (SCOM)
Description	This is the ELL Fault Isolation Action 0 Register.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	IOEL_FIR_ACTION0: processor bus FIR MSB of action select for corresponding bit in FIR. (Action0,Action1) = Action Select. (0,0) = Checkstop. (0,1) = Recoverable error to service processor. (1,0) = Special attention to service processor. (1,1) = Invalid.

Register Name	ELL FIR Action 1 Register
Mnemonic	PB.IOE.LL1.IOEL_FIR_ACTION1_REG
Address	0000000006011C07 (SCOM)
Description	This is the ELL Fault Isolation Action0 Register.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	IOEL_FIR_ACTION1: processor bus FIR LSB of action select for corresponding bit in FIR. (Action0,Action1) = Action Select. (0,0) = Checkstop. (0,1) = Recoverable error to service processor. (1,0) = Special attention to service processor. (1,1) = Invalid.

Register Name	FIR WOF Register
Mnemonic	PB.IOE.LL1.IOEL_FIR_WOF_REG
Address	0000000006011C08 (SCOM)
Description	This who's on first register indicates which error occurred first.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	IOEL_FIR_WOF: The WOF Register locks on the first error.

Register Name	ELL Configuration Register
Mnemonic	PB.IOE.LL1.IOEL_CONFIG
Address	0000000006011C0A (SCOM)
Description	This register contains ELL configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_LINK_PAIR: When 1, the two links operate as a pair. When 0, only one link is used or they are independent.
1	RW	CONFIG_DISABLE_SL_ECC: When 1, disable spare lane ECC correction.
2	RW	CONFIG_CRC_LANE_ID: When 1, use lane IDs from CRC for lane sparing.
3	RW	CONFIG_EDPL_LANE_ID: When 1, use lane IDs from EDPL for lane sparing.
4	RW	CONFIG_SL_UE_CRC_ERR: When 1, UEs on the SL ECC cause the packet to be treated as a CRC error.
5	RW	CONFIG_REPORT_SL_CHKBIT_ERR: When 1, SL ECC single-bit errors on check bits are reported to the FIR.
6	RW	CONFIG_BW_SAMPLE_SIZE: When 1, use 256 packets for the sample (instead of 64).
7	RW	CONFIG_BW_WINDOW_SIZE: When 1, shorten the sample window.
8:11	RW	CONFIG_UNUSED1: Spare bits.
12:15	RW	CONFIG_PACKET_DELAY_LIMIT: This field indicates the number of cycles of delay of frame data that are required for the packet to be considered delayed or replayed. (0 is 16 cycles.)
16:19	RW	CONFIG_TDM_DELAY: This field indicates the adjustment factor of delay for entering or exiting TDM mode.
20	RW	CONFIG_AUTO_TDM_TX: When 1, use the transmit bandwidth for automatically entering TDM mode.
21	RW	CONFIG_AUTO_TDM_RX: When 1, use the receive bandwidth for automatically entering TDM mode.

Bits	SCOM	Field Mnemonic: Description
22	RW	CONFIG_AUTO_TDM_AND_NOT_OR: When 1, both the bandwidth and error rate are needed. Otherwise, either the bandwidth or the error rate is needed.
23	RW	CONFIG_UNUSED2: Spare bits.
24:27	RW	CONFIG_AUTO_TDM_BW_DIFF: Bandwidth difference for auto-entry TMD mode.
28:31	RW	CONFIG_AUTO_TDM_ERROR_RATE: This field contains the error rate for the auto-entry TDM mode.
32:47	RW	CONFIG_UNUSED3: Spare bits.
48:51	RWX	CONFIG_TIMEOUT: This field contains the program timeout values, from 1 µs to 65 ms.
52:63	RWX	CONFIG_TIMER_1US: This field contains the program number of cycles in 1 µs.

Register Name	ELL Control Register
Mnemonic	PB.IOE.LL1.IOEL_CONTROL
Address	0000000006011C0B (SCOM)
Description	This register contains ELL control fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONTROL_UNUSED0A: Spare bits.
1	RW	LINK0_STARTUP: When 1, start initialization/training.
2:7	RW	CONTROL_UNUSED0B: Spare bits.
8:11	RWX	LINK0_ERR_INJ_COMMAND: This field contains the command to perform link error injection.
12:27	RWX	LINK0_ERR_INJ_COMMAND_LANES: This field indicates the lanes for an error-injection command.
28:31	RWX	LINK0_COMMAND: This field contains the command to perform an operation.
32	RW	CONTROL_UNUSED1A: Spare bits.
33	RW	LINK1_STARTUP: When 1, start initialization/training.
34:39	RW	CONTROL_UNUSED1B: Spare bits.
40:43	RWX	LINK1_ERR_INJ_COMMAND: This field contains the command to perform link error injection.
44:59	RWX	LINK1_ERR_INJ_COMMAND_LANES: This field indicates the lanes for an error-injection command.
60:63	RWX	LINK1_COMMAND: This field contains the command to perform an operation.

Register Name	ELL Secondary Configuration Register
Mnemonic	PB.IOE.LL1.IOEL_SEC_CONFIG
Address	0000000006011C0D (SCOM)
Description	This register contains additional ELL configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_ENABLE_ERR_INJ: When 1, enable error injection (LFSR runs).
1:15	RW	CONFIG_UNUSED4: Spare bits.
16:17	RW	CONFIG_SBE_ERROR_RATE: This field indicates the error-injection SBE rate.
18:23	RW	CONFIG_RAND_ERROR_RATE: This field indicates error-injection rate N (from 1 to 38). Probability is 2^{-N}.
24:47	RW	CONFIG_UNUSED5: Spare bits.

Bits	SCOM	Field Mnemonic: Description
48:63	RW	CONFIG_EDPL_RATE: When 0, disable EDPL. Otherwise, this field indicates the number of packets between EDPL packets.

Register Name	ELL Latency Measurement Register
Mnemonic	PB.IOE.LL1.IOEL_LAT_MEASURE
Address	0000000006011C0E (SCOM)
Description	This register contains latency measurements.

Bits	SCOM	Field Mnemonic: Description
0	ROX	LINK0_ROUND_TRIP_VALID: When 1, the round-trip value is valid.
1	RO	constant = 0b0
2:11	ROX	LINK0_ROUND_TRIP: This field indicates the round-trip time in cycles.
12	ROX	LINK1_ROUND_TRIP_VALID: When 1, the round-trip value is valid.
13	RO	constant = 0b0
14:23	ROX	LINK1_ROUND_TRIP: This field indicates the round-trip time in cycles.
24	ROX	LOCAL_LATENCY_DIFFERENCE_VALID: When 1, the local latency difference is valid.
25	ROX	LOCAL_LATENCY_LONGER_LINK: When 1, link 1 had the longer latency.
26:28	RO	constant = 0b000
29:35	ROX	LOCAL_LATENCY_DIFFERENCE: This field contains the received difference in latency between the links.
36	ROX	REMOTE_LATENCY_DIFFERENCE_VALID: When 1, the remote latency difference is valid.
37	ROX	REMOTE_LATENCY_LONGER_LINK: When 1, link 1 had the longer latency.
38:40	RO	constant = 0b000
41:47	ROX	REMOTE_LATENCY_DIFFERENCE: This field contains the transmit difference in latency between the links (as received by other side).
48	RO	constant = 0b0
49:55	RWX	LINK0_TOD_LATENCY: This field indicates the latency of TOD pulses for link 0.
56	RO	constant = 0b0
57:63	RWX	LINK1_TOD_LATENCY: This field indicates the latency of TOD pulses for link 1.

Register Name	ELL Link0 Information Register
Mnemonic	PB.IOE.LL1.IOEL_LINK0_INFO
Address	0000000006011C14 (SCOM)
Description	This register contains information about link 0.

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	LINK0_MAX_TIMEOUT: This field indicates the maximum value reached by the timeout counter.
16	ROX	LINK0_FRAME_CAP_VALID: When 1, the error capture is valid.
17	ROX	LINK0_FRAME_CAP_INST: Array instance.
18	RO	constant = 0b0
19:23	ROX	LINK0_FRAME_CAP_ADDR: This field contains the array address of the captured error.

Bits	SCOM	Field Mnemonic: Description
24:31	ROX	LINK0_FRAME_CAP_SYN: This field contains the syndrome of the captured error.
32	ROX	LINK0_REPLAY_CAP_VALID: When 1, the error capture is valid.
33	RO	constant = 0b0
34	ROX	LINK0_REPLAY_CAP_INST: Array instance.
35:36	RO	constant = 0b00
37:43	ROX	LINK0_REPLAY_CAP_ADDR: This field contains the array address of the captured error.
44:51	ROX	LINK0_REPLAY_CAP_SYN: This field contains the syndrome of the captured error.
52	ROX	LINK0_ACK_FIFO_CAP_VALID: When 1, the error capture is valid.
53:56	RO	constant = 0b0000
57:63	ROX	LINK0_ACK_FIFO_CAP_ADDR: This field contains the array address of the captured error.

Register Name	ELL Link1 Information Register
Mnemonic	PB.IOE.LL1.IOEL_LINK1_INFO
Address	0000000006011C15 (SCOM)
Description	This register contains information about link 1.

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	LINK1_MAX_TIMEOUT: This field indicates the maximum value reached by the timeout counter.
16	ROX	LINK1_FRAME_CAP_VALID: When 1, the error capture is valid.
17	ROX	LINK1_FRAME_CAP_INST: Array instance.
18	RO	constant = 0b0
19:23	ROX	LINK1_FRAME_CAP_ADDR: This field contains the array address of the captured error.
24:31	ROX	LINK1_FRAME_CAP_SYN: This field contains the syndrome of the captured error.
32	ROX	LINK1_REPLAY_CAP_VALID: When 1, the error capture is valid.
33	RO	constant = 0b0
34	ROX	LINK1_REPLAY_CAP_INST: Array instance.
35:36	RO	constant = 0b00
37:43	ROX	LINK1_REPLAY_CAP_ADDR: This field contains the array address of the captured error.
44:51	ROX	LINK1_REPLAY_CAP_SYN: This field contains the syndrome of the captured error.
52	ROX	LINK1_ACK_FIFO_CAP_VALID: When 1, the error capture is valid.
53:56	RO	constant = 0b0000
57:63	ROX	LINK1_ACK_FIFO_CAP_ADDR: This field contains the array address of the captured error.

Register Name	ELL Link 0 Error Status Register
Mnemonic	PB.IOE.LL1.IOEL_LINK0_ERROR_STATUS
Address	0000000006011C16 (SCOM)
Description	This register contains link 0 error status information.

Bits	SCOM	Field Mnemonic: Description
0	WOX	LINK0_RESET_KEEPER: Reset keeper for the Link 0 Error Status Register.
1:3	ROX	LINK0_ERROR_STATUS_CE: c_err_rpt for correctable array errors.
4:7	RO	constant = 0b0000
8:9	ROX	LINK0_ERROR_STATUS_UE: c_err_rpt for uncorrectable array errors.
10:15	RO	constant = 0b000000
16:17	ROX	LINK0_ERROR_STATUS_TRAIN: c_err_rpt for training errors.
18:23	RO	constant = 0b000000
24:34	ROX	LINK0_ERROR_STATUS_UNRECOV: c_err_rpt for unrecoverable errors.
35:43	RO	constant = 0b000000000
44:61	ROX	LINK0_ERROR_STATUS_INTERNAL: c_err_rpt for internal errors.
62:63	RO	constant = 0b00

Register Name	**ELL Link 1 Error Status Register**
Mnemonic	PB.IOE.LL1.IOEL_LINK1_ERROR_STATUS
Address	0000000006011C17 (SCOM)
Description	This register contains link 1 error status information.

Bits	SCOM	Field Mnemonic: Description
0	WOX	LINK1_RESET_KEEPER: Reset keeper for the Link 1 Error Status Register.
1:3	ROX	LINK1_ERROR_STATUS_CE: c_err_rpt for correctable array errors.
4:7	RO	constant = 0b0000
8:9	ROX	LINK1_ERROR_STATUS_UE: c_err_rpt for uncorrectable array errors.
10:15	RO	constant = 0b000000
16:17	ROX	LINK1_ERROR_STATUS_TRAIN: c_err_rpt for training errors.
18:23	RO	constant = 0b000000
24:34	ROX	LINK1_ERROR_STATUS_UNRECOV: c_err_rpt for unrecoverable errors.
35:43	RO	constant = 0b000000000
44:61	ROX	LINK1_ERROR_STATUS_INTERNAL: c_err_rpt for internal errors.
62:63	RO	constant = 0b00

Register Name	**ELL Replay Threshold Register**
Mnemonic	PB.IOE.LL1.IOEL_REPLAY_THRESHOLD
Address	0000000006011C18 (SCOM)
Description	This register contains replay threshold controls.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	THRESH_REPLAY_TB_SEL: Replay threshold timebase select.
4:7	RW	THRESH_REPLAY_TAP_SEL: Replay threshold tap select.
8:10	RW	THRESH_REPLAY_ENABLE: Replay threshold error enable.

Bits	SCOM	Field Mnemonic: Description
11:25	RW	THRESH_REPLAY_UNUSED1: Spare bits.
26	RWX	THRESH_REPLAY_LINK0_CLEAR: Replay threshold counter clear.
27	RWX	THRESH_REPLAY_LINK1_CLEAR: Replay threshold counter clear.
28	RW	THRESH_REPLAY_DIS_TB_CLEAR: Threshold disable timebase clear.
29	RW	THRESH_REPLAY_DIS_TAP_CLEAR: Threshold disable tap clear.
30	RW	THRESH_REPLAY_DIS_TAP_STOP: Threshold disable tap stop.
31	RW	THRESH_REPLAY_UNUSED2: Spare bits.
32:47	ROX	THRESH_REPLAY_LINK0_COUNT: Replay threshold count.
48:63	ROX	THRESH_REPLAY_LINK1_COUNT: Replay threshold count.

Register Name	ELL SL ECC Threshold Register
Mnemonic	PB.IOE.LL1.IOEL_SL_ECC_THRESHOLD
Address	0000000006011C19 (SCOM)
Description	This register contains SL ECC threshold controls.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	THRESH_SL_ECC_TB_SEL: SL ECC threshold timebase select.
4:7	RW	THRESH_SL_ECC_TAP_SEL: SL ECC threshold tap select.
8:9	RW	THRESH_SL_ECC_ENABLE: SL ECC threshold error enable.
10:25	RW	THRESH_SL_ECC_UNUSED1: Spare bits.
26	RWX	THRESH_SL_ECC_LINK0_CLEAR: SL ECC threshold counter clear.
27	RWX	THRESH_SL_ECC_LINK1_CLEAR: SL ECC threshold counter clear.
28	RW	THRESH_SL_ECC_DIS_TB_CLEAR: Threshold disable timebase clear.
29	RW	THRESH_SL_ECC_DIS_TAP_CLEAR: Threshold disable tap clear.
30	RW	THRESH_SL_ECC_DIS_TAP_STOP: Threshold disable tap stop.
31	RW	THRESH_SL_ECC_UNUSED2: Spare bits.
32:47	ROX	THRESH_SL_ECC_LINK0_COUNT: SL ECC Threshold count.
48:63	ROX	THRESH_SL_ECC_LINK1_COUNT: SL ECC Threshold count.

Register Name	ELL Error Injection LFSR Register
Mnemonic	PB.IOE.LL1.IOEL_ERR_INJ_LFSR
Address	0000000006011C1B (SCOM)
Description	This is the linear feedback shift register (LFSR) for error injection.

Bits	SCOM	Field Mnemonic: Description
0:60	RWX	ERR_INJ_LFSR: Error injection LFSR.
61:63	RO	constant = 0b000

Register Name	ELL Performance Monitor and Trace Configuration Register
Mnemonic	PB.IOE.LL1.IOEL_PERF_TRACE_CONFIG
Address	0000000006011C1C (SCOM)
Description	This register monitors and configures the performance counters and traces.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	CONFIG_ENABLE_PERF_0: Performance counter enable.
2:3	RW	CONFIG_ENABLE_PERF_1: Performance counter enable.
4:5	RW	CONFIG_ENABLE_PERF_2: Performance counter enable.
6:7	RW	CONFIG_ENABLE_PERF_3: Performance counter enable.
8:9	RW	CONFIG_ENABLE_PERF_4: Performance counter enable.
10:11	RW	CONFIG_ENABLE_PERF_5: Performance counter enable.
12:13	RW	CONFIG_ENABLE_PERF_6: Performance counter enable.
14:15	RW	CONFIG_ENABLE_PERF_7: Performance counter enable.
16:17	RW	CONFIG_PERF_SIZE_0: Performance counter size.
18:19	RW	CONFIG_PERF_SIZE_1: Performance counter size.
20:21	RW	CONFIG_PERF_SIZE_2: Performance counter size.
22:23	RW	CONFIG_PERF_SIZE_3: Performance counter size.
24:25	RW	CONFIG_PERF_SIZE_4: Performance counter size.
26:27	RW	CONFIG_PERF_SIZE_5: Performance counter size.
28:29	RW	CONFIG_PERF_SIZE_6: Performance counter size.
30:31	RW	CONFIG_PERF_SIZE_7: Performance counter size.
32	RW	CONFIG_PMULET_FREEZE_MODE: PMUlet freeze mode: 0 = Freeze on full. 1 = Free run.
33	RW	CONFIG_COMMON_FREEZE_MODE: Common freeze mode: 0 = Independent per PMUlet. 1 = Any counter full freezes all.
34	RW	CONFIG_PERF_RESET_MODE: PMUlet reset mode: 0 = Reset on read. 1 = Reset on write.
35	RW	CONFIG_PERFTRACE_ENABLE: Performance trace enable. Multiplex performance trace data onto the trace bus.
36	RW	CONFIG_PERFTRACE_FIXED_WINDOW: Performance trace fixed window mode. Take a sample every 255 or 255 x 128 cycles.
37	RW	CONFIG_PERFTRACE_PRESCALE: Performance trace prescale mode, wide-angle view. Performance counts are prescaled by 128.
38:39	RW	CONFIG_PERFTRACE_MODE: Performance trace input selection.
40:51	RW	CONFIG_TRACE_CONFIG_0: Selection for trace bus bits 0:43.
52:63	RW	CONFIG_TRACE_CONFIG_1: Selection for trace bus bits 44:87.

Register Name	ELL Performance Monitor Selection Register
Mnemonic	PB.IOE.LL1.IOEL_PERF_SEL_CONFIG
Address	0000000006011C1D (SCOM)
Description	This register selects performance counters.

Bits	SCOM	Field Mnemonic: Description
0:7	RW	CONFIG_PERF_SELECT_0: Selection performance counter.
8:15	RW	CONFIG_PERF_SELECT_1: Selection performance counter.
16:23	RW	CONFIG_PERF_SELECT_2: Selection performance counter.
24:31	RW	CONFIG_PERF_SELECT_3: Selection performance counter.
32:39	RW	CONFIG_PERF_SELECT_4: Selection performance counter.
40:47	RW	CONFIG_PERF_SELECT_5: Selection performance counter.
48:55	RW	CONFIG_PERF_SELECT_6: Selection performance counter.
56:63	RW	CONFIG_PERF_SELECT_7: Selection performance counter.

Register Name	ELL Performance Monitor Counter Register 0
Mnemonic	PB.IOE.LL1.IOEL_PERF_COUNTERS_0
Address	0000000006011C1E (SCOM)
Description	This register contains the 16 MSb of performance monitor counters 0 – 3.

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRREG	PERFMON_COUNTER_0: Performance counter 16 MSb.
16:31	RWX_WCLRREG	PERFMON_COUNTER_1: Performance counter 16 MSb.
32:47	RWX_WCLRREG	PERFMON_COUNTER_2: Performance counter 16 MSb.
48:63	RWX_WCLRREG	PERFMON_COUNTER_3: Performance counter 16 MSb.

Register Name	ELL Performance Monitor Counter Register 1
Mnemonic	PB.IOE.LL1.IOEL_PERF_COUNTERS_1
Address	0000000006011C1F (SCOM)
Description	This register contains the 16 MSb of performance monitor counters 4 – 7.

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRREG	PERFMON_COUNTER_4: Performance counter 16 MSb.
16:31	RWX_WCLRREG	PERFMON_COUNTER_5: Performance counter 16 MSb.
32:47	RWX_WCLRREG	PERFMON_COUNTER_6: Performance counter 16 MSb.
48:63	RWX_WCLRREG	PERFMON_COUNTER_7: Performance counter 16 MSb.

Register Name	ELL Performance Monitor Counter LSB Register 0
Mnemonic	PB.IOE.LL1.IOEL_PERF_COUNT_LSB_0
Address	0000000006011C20 (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	RESERVED.

Register Name	ELL Performance Monitor Counter LSB Register 1
Mnemonic	PB.IOE.LL1.IOEL_PERF_COUNT_LSB_1
Address	0000000006011C21 (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	RESERVED.

Register Name	ELL Link 0 Syndrome Capture Register
Mnemonic	PB.IOE.LL1.IOEL_LINK0_SYN_CAPTURE
Address	0000000006011C22 (SCOM)
Description	This register contains syndrome information for captured link 0 errors.

Bits	SCOM	Field Mnemonic: Description
0:27	RWX	LINK0_LINK_CAP_CRC_SYN: This field contains the CRC syndrome for a captured link error.
28:35	RWX	LINK0_LINK_CAP_CRC_SYN_UNUSED1: Spare bits.
36:43	RWX	LINK0_LINK_CAP_SLECC_SYN0: This field contains SL ECC syndrome 0 for a captured link error.
44:51	RWX	LINK0_LINK_CAP_SLECC_SYN1: This field contains SL ECC syndrome 1 for a captured link error.
52:54	RWX	LINK0_LINK_CAP_CRC_SYN_UNUSED2: Spare bits.
55	RWX	LINK0_LINK_CAP_VALID: This bit indicates that the captured link error is valid.
56:58	RWX	LINK0_LINK_CAP_CRC_SYN_UNUSED3: Spare bits.
59:63	RWX	LINK0_LINK_CAP_CRC_LANE: This field contains the CRC lane from the syndrome decode.

Register Name	ELL Link 1 Syndrome Capture Register
Mnemonic	PB.IOE.LL1.IOEL_LINK1_SYN_CAPTURE
Address	0000000006011C23 (SCOM)
Description	This register contains syndrome information for captured link 1 errors.

Bits	SCOM	Field Mnemonic: Description
0:27	RWX	LINK1_LINK_CAP_CRC_SYN: This field contains the CRC syndrome for a captured link error.
28:35	RWX	LINK1_LINK_CAP_CRC_SYN_UNUSED1: Spare bits.
36:43	RWX	LINK1_LINK_CAP_SLECC_SYN0: This field contains SL ECC syndrome 0 for a captured link error.

Bits	SCOM	Field Mnemonic: Description
44:51	RWX	LINK1_LINK_CAP_SLECC_SYN1: This field contains SL ECC syndrome 1 for a captured link error.
52:54	RWX	LINK1_LINK_CAP_CRC_SYN_UNUSED2: Spare bits.
55	RWX	LINK1_LINK_CAP_VALID: This bit indicates that the captured link error is valid.
56:58	RWX	LINK1_LINK_CAP_CRC_SYN_UNUSED3: Spare bits.
59:63	RWX	LINK1_LINK_CAP_CRC_LANE: This field contains the CRC lane from the syndrome decode.

Register Name	**ELL Link 0 EDPL Status Register**
Mnemonic	PB.IOE.LL1.IOEL_LINK0_EDPL_STATUS
Address	0000000006011C24 (SCOM)
Description	This register contains counts of EDPL errors.

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	LINK0_EDPL_ERROR_COUNT_0: Count of EDPL errors.
4:7	ROX	LINK0_EDPL_ERROR_COUNT_1: Count of EDPL errors.
8:11	ROX	LINK0_EDPL_ERROR_COUNT_2: Count of EDPL errors.
12:15	ROX	LINK0_EDPL_ERROR_COUNT_3: Count of EDPL errors.
16:19	ROX	LINK0_EDPL_ERROR_COUNT_4: Count of EDPL errors.
20:23	ROX	LINK0_EDPL_ERROR_COUNT_5: Count of EDPL errors.
24:27	ROX	LINK0_EDPL_ERROR_COUNT_6: Count of EDPL errors.
28:31	ROX	LINK0_EDPL_ERROR_COUNT_7: Count of EDPL errors.
32:35	ROX	LINK0_EDPL_ERROR_COUNT_8: Count of EDPL errors.
36:39	ROX	LINK0_EDPL_ERROR_COUNT_9: Count of EDPL errors.
40:43	ROX	LINK0_EDPL_ERROR_COUNT_10: Count of EDPL errors.
44:47	ROX	LINK0_EDPL_ERROR_COUNT_11: Count of EDPL errors.
48:63	RO	constant = 0b0000000000000000

Register Name	**ELL Link 1 EDPL Status Register**
Mnemonic	PB.IOE.LL1.IOEL_LINK1_EDPL_STATUS
Address	0000000006011C25 (SCOM)
Description	This register contains counts of EDPL errors.

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	LINK1_EDPL_ERROR_COUNT_0: Count of EDPL errors.
4:7	ROX	LINK1_EDPL_ERROR_COUNT_1: Count of EDPL errors.
8:11	ROX	LINK1_EDPL_ERROR_COUNT_2: Count of EDPL errors.
12:15	ROX	LINK1_EDPL_ERROR_COUNT_3: Count of EDPL errors.
16:19	ROX	LINK1_EDPL_ERROR_COUNT_4: Count of EDPL errors.
20:23	ROX	LINK1_EDPL_ERROR_COUNT_5: Count of EDPL errors.
24:27	ROX	LINK1_EDPL_ERROR_COUNT_6: Count of EDPL errors.

Bits	SCOM	Field Mnemonic: Description
28:31	ROX	LINK1_EDPL_ERROR_COUNT_7: Count of EDPL errors.
32:35	ROX	LINK1_EDPL_ERROR_COUNT_8: Count of EDPL errors.
36:39	ROX	LINK1_EDPL_ERROR_COUNT_9: Count of EDPL errors.
40:43	ROX	LINK1_EDPL_ERROR_COUNT_10: Count of EDPL errors.
44:47	ROX	LINK1_EDPL_ERROR_COUNT_11: Count of EDPL errors.
48:63	RO	constant = 0b0000000000000000

Register Name	ELL Link 0 Link Quality Status Register
Mnemonic	PB.IOE.LL1.IOEL_LINK0_QUALITY
Address	0000000006011C26 (SCOM)
Description	This register contains transmit and receive bandwidth and error-rate measurements.

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:11	ROX	LINK0_TX_BW: Measure of the transmit bandwidth.
12	RO	constant = 0b0
13:23	ROX	LINK0_RX_BW: Measure of the receive bandwidth.
24	RO	constant = 0b0
25:47	ROX	LINK0_ERROR_RATE: Measure of the received error rate.
48:63	RO	constant = 0b0000000000000000

Register Name	ELL Link1 Link Quality Status Register
Mnemonic	PB.IOE.LL1.IOEL_LINK1_QUALITY
Address	0000000006011C27 (SCOM)
Description	This register contains transmit and receive bandwidth and error-rate measurements.

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:11	ROX	LINK1_TX_BW: Measure of the transmit bandwidth.
12	RO	constant = 0b0
13:23	ROX	LINK1_RX_BW: Measure of the receive bandwidth.
24	RO	constant = 0b0
25:47	ROX	LINK1_ERROR_RATE: Measure of the received error rate.
48:63	RO	constant = 0b0000000000000000

Register Name	ELL Status Register
Mnemonic	PB.IOE.LL1.IOEL_DLL_STATUS
Address	0000000006011C28 (SCOM)
Description	This register contains status information.

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b0000
4:7	ROX	LINK0_CURRENT_STATE: This field indicates the current state of the initialization/training state machine.
8:11	RO	constant = 0b0000
12:15	ROX	LINK0_PRIOR_STATE: This field indicates the prior state of the initialization/training state machine.
16:18	RO	constant = 0b000
19:23	ROX	LINK0_MAX_PKT_TIMER: This field contains the maximum value reached by the packet delay counter.
24:27	RO	constant = 0b0000
28:31	ROX	LINK1_CURRENT_STATE: This field indicates the current state of the initialization/training state machine.
32:35	RO	constant = 0b0000
36:39	ROX	LINK1_PRIOR_STATE: This field indicates the prior state of the initialization/training state machine.
40:42	RO	constant = 0b000
43:47	ROX	LINK1_MAX_PKT_TIMER: This field contains the maximum value reached by the packet delay counter.
48:63	RO	constant = 0b0000000000000000

Register Name	ELL FIR Register
Mnemonic	PB.IOE.LL2.IOEL_FIR_REG
Address	0000000006012000 (SCOM) 0000000006012001 (SCOM1) 0000000006012002 (SCOM2)
Description	This is the ELL Fault Isolation Register (FIR).

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_LINK0_TRAINED: Link 0 trained.
1	RWX	WOX_AND	WOX_OR	FIR_LINK1_TRAINED: Link 1 trained.
2:3	RWX	WOX_AND	WOX_OR	RESERVED.
4	RWX	WOX_AND	WOX_OR	FIR_LINK0_REPLAY_THRESHOLD: Link 0 replay threshold.
5	RWX	WOX_AND	WOX_OR	FIR_LINK1_REPLAY_THRESHOLD: Link 1 replay threshold.
6	RWX	WOX_AND	WOX_OR	FIR_LINK0_CRC_ERROR: Link 0 CRC error.
7	RWX	WOX_AND	WOX_OR	FIR_LINK1_CRC_ERROR: Link 1 CRC error.
8	RWX	WOX_AND	WOX_OR	FIR_LINK0_NAK_RECEIVED: Link 0 NAK received.
9	RWX	WOX_AND	WOX_OR	FIR_LINK1_NAK_RECEIVED: Link 1 NAK received.
10	RWX	WOX_AND	WOX_OR	FIR_LINK0_REPLAY_BUFFER_FULL: Link 0 replay buffer full.
11	RWX	WOX_AND	WOX_OR	FIR_LINK1_REPLAY_BUFFER_FULL: Link 1 replay buffer full.
12	RWX	WOX_AND	WOX_OR	FIR_LINK0_SL_ECC_THRESHOLD: Link 0 SL ECC threshold.
13	RWX	WOX_AND	WOX_OR	FIR_LINK1_SL_ECC_THRESHOLD: Link 1 SL ECC threshold.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
14	RWX	WOX_AND	WOX_OR	FIR_LINK0_SL_ECC_CORRECTABLE: Link 0 SL ECC correctable.
15	RWX	WOX_AND	WOX_OR	FIR_LINK1_SL_ECC_CORRECTABLE: Link 1 SL ECC correctable.
16	RWX	WOX_AND	WOX_OR	FIR_LINK0_SL_ECC_UE: Link 0 SL ECC UE.
17	RWX	WOX_AND	WOX_OR	FIR_LINK1_SL_ECC_UE: Link 1 SL ECC UE.
18:39	RWX	WOX_AND	WOX_OR	RESERVED.
40	RWX	WOX_AND	WOX_OR	FIR_LINK0_TCOMPLETE_BAD: Link 0 complete bad.
41	RWX	WOX_AND	WOX_OR	FIR_LINK1_TCOMPLETE_BAD: Link 1 complete bad.
42:43	RWX	WOX_AND	WOX_OR	RESERVED.
44	RWX	WOX_AND	WOX_OR	FIR_LINK0_SPARE_DONE: Link 0 spare done.
45	RWX	WOX_AND	WOX_OR	FIR_LINK1_SPARE_DONE: Link 1 spare done.
46	RWX	WOX_AND	WOX_OR	FIR_LINK0_TOO_MANY_CRC_ERRORS: Link 0 too many CRC errors.
47	RWX	WOX_AND	WOX_OR	FIR_LINK1_TOO_MANY_CRC_ERRORS: Link 1 too many CRC errors.
48:50	RWX	WOX_AND	WOX_OR	RESERVED.
51	RWX	WOX_AND	WOX_OR	FIR_PSAVE_INVALID_STATE: Psave invalid state.
52	RWX	WOX_AND	WOX_OR	FIR_LINK0_CORRECTABLE_ARRAY_ERROR: Link 0 correctable array error.
53	RWX	WOX_AND	WOX_OR	FIR_LINK1_CORRECTABLE_ARRAY_ERROR: Link 1 correctable array error.
54	RWX	WOX_AND	WOX_OR	FIR_LINK0_UNCORRECTABLE_ARRAY_ERROR: Link 0 uncorrectable array error.
55	RWX	WOX_AND	WOX_OR	FIR_LINK1_UNCORRECTABLE_ARRAY_ERROR: Link 1 uncorrectable array error.
56	RWX	WOX_AND	WOX_OR	FIR_LINK0_TRAINING_FAILED: Link 0 training failed.
57	RWX	WOX_AND	WOX_OR	FIR_LINK1_TRAINING_FAILED: Link 1 training failed.
58	RWX	WOX_AND	WOX_OR	FIR_LINK0_UNRECOVERABLE_ERROR: Link 0 unrecoverable error.
59	RWX	WOX_AND	WOX_OR	FIR_LINK1_UNRECOVERABLE_ERROR: Link 1 unrecoverable error.
60	RWX	WOX_AND	WOX_OR	FIR_LINK0_INTERNAL_ERROR: Link 0 internal error.
61	RWX	WOX_AND	WOX_OR	FIR_LINK1_INTERNAL_ERROR: Link 1 internal error.
62	RWX	WOX_AND	WOX_OR	FIR_SCOM_ERR_DUP: FIR SCOM error dup.
63	RWX	WOX_AND	WOX_OR	FIR_SCOM_ERR: FIR SCOM error.

Register Name	ELL FIR Mask Register
Mnemonic	PB.IOE.LL2.IOEL_FIR_MASK_REG
Address	0000000006012003 (SCOM) 0000000006012004 (SCOM1) 0000000006012005 (SCOM2)
Description	This register provides a bit mask for the ELL FIR Register.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_LINK0_TRAINED_MASK: Link 0 trained mask.
1	RWX	WOX_AND	WOX_OR	FIR_LINK1_TRAINED_MASK: Link 1 trained mask.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
2:3	RWX	WOX_AND	WOX_OR	RESERVED.
4	RWX	WOX_AND	WOX_OR	FIR_LINK0_REPLAY_THRESHOLD_MASK: Link 0 replay threshold mask.
5	RWX	WOX_AND	WOX_OR	FIR_LINK1_REPLAY_THRESHOLD_MASK: Link 1 replay threshold mask.
6	RWX	WOX_AND	WOX_OR	FIR_LINK0_CRC_ERROR_MASK: Link 0 CRC error mask.
7	RWX	WOX_AND	WOX_OR	FIR_LINK1_CRC_ERROR_MASK: Link 1 CRC error mask.
8	RWX	WOX_AND	WOX_OR	FIR_LINK0_NAK_RECEIVED_MASK: Link 0 NAK received mask.
9	RWX	WOX_AND	WOX_OR	FIR_LINK1_NAK_RECEIVED_MASK: Link 1 NAK received mask.
10	RWX	WOX_AND	WOX_OR	FIR_LINK0_REPLAY_BUFFER_FULL_MASK: Link 0 replay buffer full mask.
11	RWX	WOX_AND	WOX_OR	FIR_LINK1_REPLAY_BUFFER_FULL_MASK: Link 1 replay buffer full mask.
12	RWX	WOX_AND	WOX_OR	FIR_LINK0_SL_ECC_THRESHOLD_MASK: Link 0 SL ECC threshold mask.
13	RWX	WOX_AND	WOX_OR	FIR_LINK1_SL_ECC_THRESHOLD_MASK: Link 1 SL ECC threshold mask.
14	RWX	WOX_AND	WOX_OR	FIR_LINK0_SL_ECC_CORRECTABLE_MASK: Link 0 SL ECC correctable mask.
15	RWX	WOX_AND	WOX_OR	FIR_LINK1_SL_ECC_CORRECTABLE_MASK: Link 1 SL ECC correctable mask.
16	RWX	WOX_AND	WOX_OR	FIR_LINK0_SL_ECC_UE_MASK: Link 0 SL ECC UE mask.
17	RWX	WOX_AND	WOX_OR	FIR_LINK1_SL_ECC_UE_MASK: Link 1 SL ECC UE mask.
18:39	RWX	WOX_AND	WOX_OR	RESERVED.
40	RWX	WOX_AND	WOX_OR	FIR_LINK0_TCOMPLETE_BAD_MASK: Link 0 complete bad mask.
41	RWX	WOX_AND	WOX_OR	FIR_LINK1_TCOMPLETE_BAD_MASK: Link 1 complete bad mask.
42:43	RWX	WOX_AND	WOX_OR	RESERVED.
44	RWX	WOX_AND	WOX_OR	FIR_LINK0_SPARE_DONE_MASK: Link 0 spare done mask.
45	RWX	WOX_AND	WOX_OR	FIR_LINK1_SPARE_DONE_MASK: Link 1 spare done mask.
46	RWX	WOX_AND	WOX_OR	FIR_LINK0_TOO_MANY_CRC_ERRORS_MASK: Link 0 too many CRC errors mask.
47	RWX	WOX_AND	WOX_OR	FIR_LINK1_TOO_MANY_CRC_ERRORS_MASK: Link 1 too many CRC errors mask.
48:50	RWX	WOX_AND	WOX_OR	RESERVED.
51	RWX	WOX_AND	WOX_OR	FIR_PSAVE_INVALID_STATE_MASK: Psave invalid state mask.
52	RWX	WOX_AND	WOX_OR	FIR_LINK0_CORRECTABLE_ARRAY_ERROR_MASK: Link 0 correctable array error mask.
53	RWX	WOX_AND	WOX_OR	FIR_LINK1_CORRECTABLE_ARRAY_ERROR_MASK: Link 1 correctable array error mask.
54	RWX	WOX_AND	WOX_OR	FIR_LINK0_UNCORRECTABLE_ARRAY_ERROR_MASK: Link 0 uncorrectable array error mask.
55	RWX	WOX_AND	WOX_OR	FIR_LINK1_UNCORRECTABLE_ARRAY_ERROR_MASK: Link 1 uncorrectable array error mask.
56	RWX	WOX_AND	WOX_OR	FIR_LINK0_TRAINING_FAILED_MASK: Link 0 training failed mask.
57	RWX	WOX_AND	WOX_OR	FIR_LINK1_TRAINING_FAILED_MASK: Link 1 training failed mask.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
58	RWX	WOX_AND	WOX_OR	FIR_LINK0_UNRECOVERABLE_ERROR_MASK: Link 0 unrecoverable error mask.
59	RWX	WOX_AND	WOX_OR	FIR_LINK1_UNRECOVERABLE_ERROR_MASK: Link 1 unrecoverable error mask.
60	RWX	WOX_AND	WOX_OR	FIR_LINK0_INTERNAL_ERROR_MASK: Link 0 internal error mask.
61	RWX	WOX_AND	WOX_OR	FIR_LINK1_INTERNAL_ERROR_MASK: Link 1 internal error mask.
62	RWX	WOX_AND	WOX_OR	FIR_SCOM_ERR_DUP_MASK: FIR SCOM error dup mask.
63	RWX	WOX_AND	WOX_OR	FIR_SCOM_ERR_MASK: FIR SCOM error mask.

Register Name	ELL FIR Action 0 Register
Mnemonic	PB.IOE.LL2.IOEL_FIR_ACTION0_REG
Address	0000000006012006 (SCOM)
Description	This is the ELL Fault Isolation Action 0 Register.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	IOEL_FIR_ACTION0: processor bus FIR MSB of action select for corresponding bit in FIR. (Action0,Action1) = Action Select. (0,0) = Checkstop. (0,1) = Recoverable error to service processor. (1,0) = Special attention to service processor. (1,1) = Invalid.

Register Name	ELL FIR Action 1 Register
Mnemonic	PB.IOE.LL2.IOEL_FIR_ACTION1_REG
Address	0000000006012007 (SCOM)
Description	This is the ELL Fault Isolation Action0 Register.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	IOEL_FIR_ACTION1: processor bus FIR LSB of action select for corresponding bit in FIR. (Action0,Action1) = Action Select. (0,0) = Checkstop. (0,1) = Recoverable error to service processor. (1,0) = Special attention to service processor. (1,1) = Invalid.

Register Name	FIR WOF Register
Mnemonic	PB.IOE.LL2.IOEL_FIR_WOF_REG
Address	0000000006012008 (SCOM)
Description	This who's on first register indicates which error occurred first.

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	IOEL_FIR_WOF: The WOF Register locks on the first error.

Register Name	ELL Configuration Register
Mnemonic	PB.IOE.LL2.IOEL_CONFIG
Address	000000000601200A (SCOM)
Description	This register contains ELL configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_LINK_PAIR: When 1, the two links operate as a pair. When 0, only one link is used or they are independent.
1	RW	CONFIG_DISABLE_SL_ECC: When 1, disable spare lane ECC correction.
2	RW	CONFIG_CRC_LANE_ID: When 1, use lane IDs from CRC for lane sparing.
3	RW	CONFIG_EDPL_LANE_ID: When 1, use lane IDs from EDPL for lane sparing.
4	RW	CONFIG_SL_UE_CRC_ERR: When 1, UEs on the SL ECC cause the packet to be treated as a CRC error.
5	RW	CONFIG_REPORT_SL_CHKBIT_ERR: When 1, SL ECC single-bit errors on check bits are reported to the FIR.
6	RW	CONFIG_BW_SAMPLE_SIZE: When 1, use 256 packets for the sample (instead of 64).
7	RW	CONFIG_BW_WINDOW_SIZE: When 1, shorten the sample window.
8:11	RW	CONFIG_UNUSED1: Spare bits.
12:15	RW	CONFIG_PACKET_DELAY_LIMIT: This field indicates the number of cycles of delay of frame data that are required for the packet to be considered delayed or replayed. (0 is 16 cycles.)
16:19	RW	CONFIG_TDM_DELAY: This field indicates the adjustment factor of delay for entering or exiting TDM mode.
20	RW	CONFIG_AUTO_TDM_TX: When 1, use the transmit bandwidth for automatically entering TDM mode.
21	RW	CONFIG_AUTO_TDM_RX: When 1, use the receive bandwidth for automatically entering TDM mode.
22	RW	CONFIG_AUTO_TDM_AND_NOT_OR: When 1, both the bandwidth and error rate are needed. Otherwise, either the bandwidth or the error rate is needed.
23	RW	CONFIG_UNUSED2: Spare bits.
24:27	RW	CONFIG_AUTO_TDM_BW_DIFF: Bandwidth difference for auto-entry TMD mode.
28:31	RW	CONFIG_AUTO_TDM_ERROR_RATE: This field contains the error rate for the auto-entry TDM mode.
32:47	RW	CONFIG_UNUSED3: Spare bits.
48:51	RWX	CONFIG_TIMEOUT: This field contains the program timeout values, from 1 µs to 65 ms.
52:63	RWX	CONFIG_TIMER_1US: This field contains the program number of cycles in 1 µs.

Register Name	ELL Control Register
Mnemonic	PB.IOE.LL2.IOEL_CONTROL
Address	000000000601200B (SCOM)
Description	This register contains ELL control fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONTROL_UNUSED0A: Spare bits.
1	RW	LINK0_STARTUP: When 1, start initialization/training.
2:7	RW	CONTROL_UNUSED0B: Spare bits.
8:11	RWX	LINK0_ERR_INJ_COMMAND: This field contains the command to perform link error injection.
12:27	RWX	LINK0_ERR_INJ_COMMAND_LANES: This field indicates the lanes for an error-injection command.

Bits	SCOM	Field Mnemonic: Description
28:31	RWX	LINK0_COMMAND: This field contains the command to perform an operation.
32	RW	CONTROL_UNUSED1A: Spare bits.
33	RW	LINK1_STARTUP: When 1, start initialization/training.
34:39	RW	CONTROL_UNUSED1B: Spare bits.
40:43	RWX	LINK1_ERR_INJ_COMMAND: This field contains the command to perform link error injection.
44:59	RWX	LINK1_ERR_INJ_COMMAND_LANES: This field indicates the lanes for an error-injection command.
60:63	RWX	LINK1_COMMAND: This field contains the command to perform an operation.

Register Name	ELL Secondary Configuration Register
Mnemonic	PB.IOE.LL2.IOEL_SEC_CONFIG
Address	000000000601200D (SCOM)
Description	This register contains additional ELL configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_ENABLE_ERR_INJ: When 1, enable error injection (LFSR runs).
1:15	RW	CONFIG_UNUSED4: Spare bits.
16:17	RW	CONFIG_SBE_ERROR_RATE: This field indicates the error-injection SBE rate.
18:23	RW	CONFIG_RAND_ERROR_RATE: This field indicates error-injection rate N (from 1 to 38). Probability is 2^{-N}.
24:47	RW	CONFIG_UNUSED5: Spare bits.
48:63	RW	CONFIG_EDPL_RATE: When 0, disable EDPL. Otherwise, this field indicates the number of packets between EDPL packets.

Register Name	ELL Latency Measurement Register
Mnemonic	PB.IOE.LL2.IOEL_LAT_MEASURE
Address	000000000601200E (SCOM)
Description	This register contains latency measurements.

Bits	SCOM	Field Mnemonic: Description
0	ROX	LINK0_ROUND_TRIP_VALID: When 1, the round-trip value is valid.
1	RO	constant = 0b0
2:11	ROX	LINK0_ROUND_TRIP: This field indicates the round-trip time in cycles.
12	ROX	LINK1_ROUND_TRIP_VALID: When 1, the round-trip value is valid.
13	RO	constant = 0b0
14:23	ROX	LINK1_ROUND_TRIP: This field indicates the round-trip time in cycles.
24	ROX	LOCAL_LATENCY_DIFFERENCE_VALID: When 1, the local latency difference is valid.
25	ROX	LOCAL_LATENCY_LONGER_LINK: When 1, link 1 had the longer latency.
26:28	RO	constant = 0b000
29:35	ROX	LOCAL_LATENCY_DIFFERENCE: This field contains the received difference in latency between the links.
36	ROX	REMOTE_LATENCY_DIFFERENCE_VALID: When 1, the remote latency difference is valid.

Bits	SCOM	Field Mnemonic: Description
37	ROX	REMOTE_LATENCY_LONGER_LINK: When 1, link 1 had the longer latency.
38:40	RO	constant = 0b000
41:47	ROX	REMOTE_LATENCY_DIFFERENCE: This field contains the transmit difference in latency between the links (as received by other side).
48	RO	constant = 0b0
49:55	RWX	LINK0_TOD_LATENCY: This field indicates the latency of TOD pulses for link 0.
56	RO	constant = 0b0
57:63	RWX	LINK1_TOD_LATENCY: This field indicates the latency of TOD pulses for link 1.

Register Name	ELL Link 0 Information Register
Mnemonic	PB.IOE.LL2.IOEL_LINK0_INFO
Address	0000000006012014 (SCOM)
Description	This register contains information about link 0.

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	LINK0_MAX_TIMEOUT: This field indicates the maximum value reached by the timeout counter.
16	ROX	LINK0_FRAME_CAP_VALID: When 1, the error capture is valid.
17	ROX	LINK0_FRAME_CAP_INST: Array instance.
18	RO	constant = 0b0
19:23	ROX	LINK0_FRAME_CAP_ADDR: This field contains the array address of the captured error.
24:31	ROX	LINK0_FRAME_CAP_SYN: This field contains the syndrome of the captured error.
32	ROX	LINK0_REPLAY_CAP_VALID: When 1, the error capture is valid.
33	RO	constant = 0b0
34	ROX	LINK0_REPLAY_CAP_INST: Array instance.
35:36	RO	constant = 0b00
37:43	ROX	LINK0_REPLAY_CAP_ADDR: This field contains the array address of the captured error.
44:51	ROX	LINK0_REPLAY_CAP_SYN: This field contains the syndrome of the captured error.
52	ROX	LINK0_ACK_FIFO_CAP_VALID: When 1, the error capture is valid.
53:56	RO	constant = 0b0000
57:63	ROX	LINK0_ACK_FIFO_CAP_ADDR: This field contains the array address of the captured error.

Register Name	ELL Link 1 Information Register
Mnemonic	PB.IOE.LL2.IOEL_LINK1_INFO
Address	0000000006012015 (SCOM)
Description	This register contains information about link 1.

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	LINK1_MAX_TIMEOUT: This field indicates the maximum value reached by the timeout counter.
16	ROX	LINK1_FRAME_CAP_VALID: When 1, the error capture is valid.

Bits	SCOM	Field Mnemonic: Description
17	ROX	LINK1_FRAME_CAP_INST: Array instance.
18	RO	constant = 0b0
19:23	ROX	LINK1_FRAME_CAP_ADDR: This field contains the array address of the captured error.
24:31	ROX	LINK1_FRAME_CAP_SYN: This field contains the syndrome of the captured error.
32	ROX	LINK1_REPLAY_CAP_VALID: When 1, the error capture is valid.
33	RO	constant = 0b0
34	ROX	LINK1_REPLAY_CAP_INST: Array instance.
35:36	RO	constant = 0b00
37:43	ROX	LINK1_REPLAY_CAP_ADDR: This field contains the array address of the captured error.
44:51	ROX	LINK1_REPLAY_CAP_SYN: This field contains the syndrome of the captured error.
52	ROX	LINK1_ACK_FIFO_CAP_VALID: When 1, the error capture is valid.
53:56	RO	constant = 0b0000
57:63	ROX	LINK1_ACK_FIFO_CAP_ADDR: This field contains the array address of the captured error.

Register Name	ELL Link 0 Error Status Register
Mnemonic	PB.IOE.LL2.IOEL_LINK0_ERROR_STATUS
Address	0000000006012016 (SCOM)
Description	This register contains link 0 error status information.

Bits	SCOM	Field Mnemonic: Description
0	WOX	LINK0_RESET_KEEPER: Reset keeper for the Link 0 Error Status Register.
1:3	ROX	LINK0_ERROR_STATUS_CE: c_err_rpt for correctable array errors.
4:7	RO	constant = 0b0000
8:9	ROX	LINK0_ERROR_STATUS_UE: c_err_rpt for uncorrectable array errors.
10:15	RO	constant = 0b000000
16:17	ROX	LINK0_ERROR_STATUS_TRAIN: c_err_rpt for training errors.
18:23	RO	constant = 0b000000
24:34	ROX	LINK0_ERROR_STATUS_UNRECOV: c_err_rpt for unrecoverable errors.
35:43	RO	constant = 0b000000000
44:61	ROX	LINK0_ERROR_STATUS_INTERNAL: c_err_rpt for internal errors.
62:63	RO	constant = 0b00

Register Name	ELL Link 1 Error Status Register
Mnemonic	PB.IOE.LL2.IOEL_LINK1_ERROR_STATUS
Address	0000000006012017 (SCOM)
Description	This register contains link 1 error status information.

Bits	SCOM	Field Mnemonic: Description
0	WOX	LINK1_RESET_KEEPER: Reset keeper for the Link 1 Error Status Register.

Bits	SCOM	Field Mnemonic: Description
1:3	ROX	LINK1_ERROR_STATUS_CE: c_err_rpt for correctable array errors.
4:7	RO	constant = 0b0000
8:9	ROX	LINK1_ERROR_STATUS_UE: c_err_rpt for uncorrectable array errors.
10:15	RO	constant = 0b000000
16:17	ROX	LINK1_ERROR_STATUS_TRAIN: c_err_rpt for training errors.
18:23	RO	constant = 0b000000
24:34	ROX	LINK1_ERROR_STATUS_UNRECOV: c_err_rpt for unrecoverable errors.
35:43	RO	constant = 0b000000000
44:61	ROX	LINK1_ERROR_STATUS_INTERNAL: c_err_rpt for internal errors.
62:63	RO	constant = 0b00

Register Name	ELL Replay Threshold Register
Mnemonic	PB.IOE.LL2.IOEL_REPLAY_THRESHOLD
Address	0000000006012018 (SCOM)
Description	This register contains replay threshold controls.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	THRESH_REPLAY_TB_SEL: Replay threshold timebase select.
4:7	RW	THRESH_REPLAY_TAP_SEL: Replay threshold tap select.
8:10	RW	THRESH_REPLAY_ENABLE: Replay threshold error enable.
11:25	RW	THRESH_REPLAY_UNUSED1: Spare bits.
26	RWX	THRESH_REPLAY_LINK0_CLEAR: Replay threshold counter clear.
27	RWX	THRESH_REPLAY_LINK1_CLEAR: Replay threshold counter clear.
28	RW	THRESH_REPLAY_DIS_TB_CLEAR: Threshold disable timebase clear.
29	RW	THRESH_REPLAY_DIS_TAP_CLEAR: Threshold disable tap clear.
30	RW	THRESH_REPLAY_DIS_TAP_STOP: Threshold disable tap stop.
31	RW	THRESH_REPLAY_UNUSED2: Spare bits.
32:47	ROX	THRESH_REPLAY_LINK0_COUNT: Replay threshold count.
48:63	ROX	THRESH_REPLAY_LINK1_COUNT: Replay threshold count.

Register Name	ELL SL ECC Threshold Register
Mnemonic	PB.IOE.LL2.IOEL_SL_ECC_THRESHOLD
Address	0000000006012019 (SCOM)
Description	This register contains SL ECC threshold controls.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	THRESH_SL_ECC_TB_SEL: SL ECC threshold timebase select.
4:7	RW	THRESH_SL_ECC_TAP_SEL: SL ECC threshold tap select.
8:9	RW	THRESH_SL_ECC_ENABLE: SL ECC threshold error enable.

Bits	SCOM	Field Mnemonic: Description
10:25	RW	THRESH_SL_ECC_UNUSED1: Spare bits.
26	RWX	THRESH_SL_ECC_LINK0_CLEAR: SL ECC threshold counter clear.
27	RWX	THRESH_SL_ECC_LINK1_CLEAR: SL ECC threshold counter clear.
28	RW	THRESH_SL_ECC_DIS_TB_CLEAR: Threshold disable timebase clear.
29	RW	THRESH_SL_ECC_DIS_TAP_CLEAR: Threshold disable tap clear.
30	RW	THRESH_SL_ECC_DIS_TAP_STOP: Threshold disable tap stop.
31	RW	THRESH_SL_ECC_UNUSED2: Spare bits.
32:47	ROX	THRESH_SL_ECC_LINK0_COUNT: SL ECC Threshold count.
48:63	ROX	THRESH_SL_ECC_LINK1_COUNT: SL ECC Threshold count.

Register Name	ELL Error Injection LFSR Register
Mnemonic	PB.IOE.LL2.IOEL_ERR_INJ_LFSR
Address	000000000601201B (SCOM)
Description	This is the linear feedback shift register (LFSR) for error injection.

Bits	SCOM	Field Mnemonic: Description
0:60	RWX	ERR_INJ_LFSR: Error injection LFSR.
61:63	RO	constant = 0b000

Register Name	ELL Performance Monitor and Trace Configuration Register
Mnemonic	PB.IOE.LL2.IOEL_PERF_TRACE_CONFIG
Address	000000000601201C (SCOM)
Description	This register monitors and configures the performance counters and traces.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	CONFIG_ENABLE_PERF_0: Performance counter enable.
2:3	RW	CONFIG_ENABLE_PERF_1: Performance counter enable.
4:5	RW	CONFIG_ENABLE_PERF_2: Performance counter enable.
6:7	RW	CONFIG_ENABLE_PERF_3: Performance counter enable.
8:9	RW	CONFIG_ENABLE_PERF_4: Performance counter enable.
10:11	RW	CONFIG_ENABLE_PERF_5: Performance counter enable.
12:13	RW	CONFIG_ENABLE_PERF_6: Performance counter enable.
14:15	RW	CONFIG_ENABLE_PERF_7: Performance counter enable.
16:17	RW	CONFIG_PERF_SIZE_0: Performance counter size.
18:19	RW	CONFIG_PERF_SIZE_1: Performance counter size.
20:21	RW	CONFIG_PERF_SIZE_2: Performance counter size.
22:23	RW	CONFIG_PERF_SIZE_3: Performance counter size.
24:25	RW	CONFIG_PERF_SIZE_4: Performance counter size.
26:27	RW	CONFIG_PERF_SIZE_5: Performance counter size.

Bits	SCOM	Field Mnemonic: Description
28:29	RW	CONFIG_PERF_SIZE_6: Performance counter size.
30:31	RW	CONFIG_PERF_SIZE_7: Performance counter size.
32	RW	CONFIG_PMULET_FREEZE_MODE: PMUlet freeze mode: 0 = Freeze on full. 1 = Free run.
33	RW	CONFIG_COMMON_FREEZE_MODE: Common freeze mode: 0 = Independent per PMUlet. 1 = Any counter full freezes all.
34	RW	CONFIG_PERF_RESET_MODE: PMUlet reset mode: 0 = Reset on read. 1 = Reset on write.
35	RW	CONFIG_PERFTRACE_ENABLE: Performance trace enable. Multiplex performance trace data onto the trace bus.
36	RW	CONFIG_PERFTRACE_FIXED_WINDOW: Performance trace fixed window mode. Take a sample every 255 or 255 x 128 cycles.
37	RW	CONFIG_PERFTRACE_PRESCALE: Performance trace prescale mode, wide-angle view. Performance counts are prescaled by 128.
38:39	RW	CONFIG_PERFTRACE_MODE: Performance trace input selection.
40:51	RW	CONFIG_TRACE_CONFIG_0: Selection for trace bus bits 0:43.
52:63	RW	CONFIG_TRACE_CONFIG_1: Selection for trace bus bits 44:87.

Register Name	**ELL Performance Monitor Selection Register**
Mnemonic	PB.IOE.LL2.IOEL_PERF_SEL_CONFIG
Address	000000000601201D (SCOM)
Description	This register selects performance counters.

Bits	SCOM	Field Mnemonic: Description
0:7	RW	CONFIG_PERF_SELECT_0: Selection performance counter.
8:15	RW	CONFIG_PERF_SELECT_1: Selection performance counter.
16:23	RW	CONFIG_PERF_SELECT_2: Selection performance counter.
24:31	RW	CONFIG_PERF_SELECT_3: Selection performance counter.
32:39	RW	CONFIG_PERF_SELECT_4: Selection performance counter.
40:47	RW	CONFIG_PERF_SELECT_5: Selection performance counter.
48:55	RW	CONFIG_PERF_SELECT_6: Selection performance counter.
56:63	RW	CONFIG_PERF_SELECT_7: Selection performance counter.

Register Name	**ELL Performance Monitor Counter Register 0**
Mnemonic	PB.IOE.LL2.IOEL_PERF_COUNTERS_0
Address	000000000601201E (SCOM)
Description	This register contains the 16 MSb of performance monitor counters 0 – 3.

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRREG	PERFMON_COUNTER_0: Performance counter 16 MSb.
16:31	RWX_WCLRREG	PERFMON_COUNTER_1: Performance counter 16 MSb.
32:47	RWX_WCLRREG	PERFMON_COUNTER_2: Performance counter 16 MSb.
48:63	RWX_WCLRREG	PERFMON_COUNTER_3: Performance counter 16 MSb.

Register Name	ELL Performance Monitor Counter Register 1
Mnemonic	PB.IOE.LL2.IOEL_PERF_COUNTERS_1
Address	000000000601201F (SCOM)
Description	This register contains the 16 MSb of performance monitor counters 4 – 7.

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRREG	PERFMON_COUNTER_4: Performance counter 16 MSb.
16:31	RWX_WCLRREG	PERFMON_COUNTER_5: Performance counter 16 MSb.
32:47	RWX_WCLRREG	PERFMON_COUNTER_6: Performance counter 16 MSb.
48:63	RWX_WCLRREG	PERFMON_COUNTER_7: Performance counter 16 MSb.

Register Name	ELL Performance Monitor Counter LSB Register 0
Mnemonic	PB.IOE.LL2.IOEL_PERF_COUNT_LSB_0
Address	0000000006012020 (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	RESERVED.

Register Name	ELL Performance Monitor Counter LSB Register 1
Mnemonic	PB.IOE.LL2.IOEL_PERF_COUNT_LSB_1
Address	0000000006012021 (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	RESERVED.

Register Name	ELL Link 0 Syndrome Capture Register
Mnemonic	PB.IOE.LL2.IOEL_LINK0_SYN_CAPTURE
Address	0000000006012022 (SCOM)
Description	This register contains syndrome information for captured link 0 errors. Capture register

Bits	SCOM	Field Mnemonic: Description
0:27	RWX	LINK0_LINK_CAP_CRC_SYN: This field contains the CRC syndrome for a captured link error.

Bits	SCOM	Field Mnemonic: Description
28:35	RWX	LINK0_LINK_CAP_CRC_SYN_UNUSED1: Spare bits.
36:43	RWX	LINK0_LINK_CAP_SLECC_SYN0: This field contains SL ECC syndrome 0 for a captured link error.
44:51	RWX	LINK0_LINK_CAP_SLECC_SYN1: This field contains SL ECC syndrome 1 for a captured link error.
52:54	RWX	LINK0_LINK_CAP_CRC_SYN_UNUSED2: Spare bits.
55	RWX	LINK0_LINK_CAP_VALID: This bit indicates that the captured link error is valid.
56:58	RWX	LINK0_LINK_CAP_CRC_SYN_UNUSED3: Spare bits.
59:63	RWX	LINK0_LINK_CAP_CRC_LANE: This field contains the CRC lane from the syndrome decode.

Register Name	ELL Link 1 Syndrome Capture Register
Mnemonic	PB.IOE.LL2.IOEL_LINK1_SYN_CAPTURE
Address	0000000006012023 (SCOM)
Description	This register contains syndrome information for captured link 1 errors.

Bits	SCOM	Field Mnemonic: Description
0:27	RWX	LINK1_LINK_CAP_CRC_SYN: This field contains the CRC syndrome for a captured link error.
28:35	RWX	LINK1_LINK_CAP_CRC_SYN_UNUSED1: Spare bits.
36:43	RWX	LINK1_LINK_CAP_SLECC_SYN0: This field contains SL ECC syndrome 0 for a captured link error.
44:51	RWX	LINK1_LINK_CAP_SLECC_SYN1: This field contains SL ECC syndrome 1 for a captured link error.
52:54	RWX	LINK1_LINK_CAP_CRC_SYN_UNUSED2: Spare bits.
55	RWX	LINK1_LINK_CAP_VALID: This bit indicates that the captured link error is valid.
56:58	RWX	LINK1_LINK_CAP_CRC_SYN_UNUSED3: Spare bits.
59:63	RWX	LINK1_LINK_CAP_CRC_LANE: This field contains the CRC lane from the syndrome decode.

Register Name	ELL Link 0 EDPL Status Register
Mnemonic	PB.IOE.LL2.IOEL_LINK0_EDPL_STATUS
Address	0000000006012024 (SCOM)
Description	This register contains counts of EDPL errors.

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	LINK0_EDPL_ERROR_COUNT_0: Count of EDPL errors.
4:7	ROX	LINK0_EDPL_ERROR_COUNT_1: Count of EDPL errors.
8:11	ROX	LINK0_EDPL_ERROR_COUNT_2: Count of EDPL errors.
12:15	ROX	LINK0_EDPL_ERROR_COUNT_3: Count of EDPL errors.
16:19	ROX	LINK0_EDPL_ERROR_COUNT_4: Count of EDPL errors.
20:23	ROX	LINK0_EDPL_ERROR_COUNT_5: Count of EDPL errors.
24:27	ROX	LINK0_EDPL_ERROR_COUNT_6: Count of EDPL errors.
28:31	ROX	LINK0_EDPL_ERROR_COUNT_7: Count of EDPL errors.
32:35	ROX	LINK0_EDPL_ERROR_COUNT_8: Count of EDPL errors.
36:39	ROX	LINK0_EDPL_ERROR_COUNT_9: Count of EDPL errors.

Bits	SCOM	Field Mnemonic: Description
40:43	ROX	LINK0_EDPL_ERROR_COUNT_10: Count of EDPL errors.
44:47	ROX	LINK0_EDPL_ERROR_COUNT_11: Count of EDPL errors.
48:63	RO	constant = 0b0000000000000000

Register Name	ELL Link 1 EDPL Status Register
Mnemonic	PB.IOE.LL2.IOEL_LINK1_EDPL_STATUS
Address	0000000006012025 (SCOM)
Description	This register contains counts of EDPL errors.

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	LINK1_EDPL_ERROR_COUNT_0: Count of EDPL errors.
4:7	ROX	LINK1_EDPL_ERROR_COUNT_1: Count of EDPL errors.
8:11	ROX	LINK1_EDPL_ERROR_COUNT_2: Count of EDPL errors.
12:15	ROX	LINK1_EDPL_ERROR_COUNT_3: Count of EDPL errors.
16:19	ROX	LINK1_EDPL_ERROR_COUNT_4: Count of EDPL errors.
20:23	ROX	LINK1_EDPL_ERROR_COUNT_5: Count of EDPL errors.
24:27	ROX	LINK1_EDPL_ERROR_COUNT_6: Count of EDPL errors.
28:31	ROX	LINK1_EDPL_ERROR_COUNT_7: Count of EDPL errors.
32:35	ROX	LINK1_EDPL_ERROR_COUNT_8: Count of EDPL errors.
36:39	ROX	LINK1_EDPL_ERROR_COUNT_9: Count of EDPL errors.
40:43	ROX	LINK1_EDPL_ERROR_COUNT_10: Count of EDPL errors.
44:47	ROX	LINK1_EDPL_ERROR_COUNT_11: Count of EDPL errors.
48:63	RO	constant = 0b0000000000000000

Register Name	ELL Link 0 Link Quality Status Register
Mnemonic	PB.IOE.LL2.IOEL_LINK0_QUALITY
Address	0000000006012026 (SCOM)
Description	This register contains transmit and receive bandwidth and error-rate measurements.

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:11	ROX	LINK0_TX_BW: Measure of the transmit bandwidth.
12	RO	constant = 0b0
13:23	ROX	LINK0_RX_BW: Measure of the receive bandwidth.
24	RO	constant = 0b0
25:47	ROX	LINK0_ERROR_RATE: Measure of the received error rate.
48:63	RO	constant = 0b0000000000000000

Register Name	ELL Link1 Link Quality Status Register
Mnemonic	PB.IOE.LL2.IOEL_LINK1_QUALITY
Address	0000000006012027 (SCOM)
Description	This register contains transmit and receive bandwidth and error-rate measurements.

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:11	ROX	LINK1_TX_BW: Measure of the transmit bandwidth.
12	RO	constant = 0b0
13:23	ROX	LINK1_RX_BW: Measure of the receive bandwidth.
24	RO	constant = 0b0
25:47	ROX	LINK1_ERROR_RATE: Measure of the received error rate.
48:63	RO	constant = 0b0000000000000000

Register Name	ELL Status Register
Mnemonic	PB.IOE.LL2.IOEL_DLL_STATUS
Address	0000000006012028 (SCOM)
Description	This register contains status information.

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b0000
4:7	ROX	LINK0_CURRENT_STATE: This field indicates the current state of the initialization/training state machine.
8:11	RO	constant = 0b0000
12:15	ROX	LINK0_PRIOR_STATE: This field indicates the prior state of the initialization/training state machine.
16:18	RO	constant = 0b000
19:23	ROX	LINK0_MAX_PKT_TIMER: This field contains the maximum value reached by the packet delay counter.
24:27	RO	constant = 0b0000
28:31	ROX	LINK1_CURRENT_STATE: This field indicates the current state of the initialization/training state machine.
32:35	RO	constant = 0b0000
36:39	ROX	LINK1_PRIOR_STATE: This field indicates the prior state of the initialization/training state machine.
40:42	RO	constant = 0b000
43:47	ROX	LINK1_MAX_PKT_TIMER: This field contains the maximum value reached by the packet delay counter.
48:63	RO	constant = 0b0000000000000000

Register Name	Synchronization Configuration Register
Mnemonic	TP.TCXB.XB.SYNC_CONFIG
Address	0000000006030000 (SCOM)
Description	This register configures the congruence class (CC) counters.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	SYNC_PULSE_DELAY: This field configures the delay of the incoming synchronization pulse. The default is eight latches including asynchronous. Cycles delay of the reset of the phase counter: 0000 = 8. 0001 = 2. 0010 = 3. 0011 = 4. 0100 = 5. 0101 = 6. 0110 = 7. 0111 = 8. 1000 = 9. 1001 = 10. 1010 = 11. 1011 = 12. 1100 = 13. 1101 = 14. 1110 = 15. 1111 = 16.

Bits	SCOM	Field Mnemonic: Description
4	RW	LISTEN_TO_SYNC_PULSE_DIS: This bit disables phase-counter synchronization by the sync_pulse signal. The default is enabled. **Note:** When listen_to_sync is enabled, the chiplet gets corrupted for 200 cycles.
5	RW	SYNC_PULSE_INPUT_SEL: The default is 0. When set to 1, the alternative input of the sync_pulse is used. **Note:** When the input select is toggled, the chiplet gets corrupted for 200 cycles.
6	RW	USE_SYNC_FOR_SCAN: If this bit is set, use OPCG initial alignment for scan requests.
7	RW	CLEAR_CHIPLET_IS_ALIGNED: This bit clears the chiplet_is_aligned bit. For more information, see the Chiplet Status Register on page 51.
8	RW	UNIT_REGION_CLKCMD_ENABLE: This bit enables the unit interface to start or stop one dedicated region. It is used for the POWER9 cache/core.
9	RW	DISABLE_PCB_ITR: This bit disables interrupt generation within the CC. An interrupt is sent on each hld event.
10	RW	ENABLE_VITL_ALIGN_CHECK: This bit enables the vital alignment check to compare the alignment of an incoming synchronization pulse with the 2:1 vital LCB.
11	RW	SYNC_PULSE_OUT_DIS: When set to 1, this bit disables sync_pulse output. The master chiplet does not send synchronization pulses to slave chiplets anymore.
12:19	RW	UNUSED1219: Unused.

Register Name	**OPCG Alignment Register**
Mnemonic	TP.TCXB.XB.OPCG_ALIGN
Address	0000000006030001 (SCOM)
Description	This register is used to align the on-product clock generator (OPCG).

Bits	SCOM	Field Mnemonic: Description
0:3	RW	INOP_ALIGN: INOP phase alignment. (0: none, 1: 2:1, 2: 3:1, 3: 4:1, 4: 6:1, 5: 8:1, 6: 12:1, 7: 16:1, 8: 24:1, 9-15: 48:1).
4:7	RW	SNOP_ALIGN: SNOP phase alignment. (0: none, 1: 2:1, 2: 3:1, 3: 4:1, 4: 6:1, 5: 8:1, 6: 12:1, 7: 16:1, 8: 24:1, 9-15: 48:1).
8:11	RW	ENOP_ALIGN: ENOP phase alignment. (0: none, 1: 2:1, 2: 3:1, 3: 4:1, 4: 6:1, 5: 8:1, 6: 12:1, 7: 16:1, 8: 24:1, 9-15: 48:1).
12:19	RW	INOP_WAIT: INOP cycle delay (0 - 255).
20:31	RW	SNOP_WAIT: SNOP cycle delay (0 - 4095).
32:39	RW	ENOP_WAIT: ENOP cycle delay (0 - 255).
40	RW	INOP_FORCE_SG: INOP: Set the SG high during INOP.
41	RW	SNOP_FORCE_SG: SNOP: Set the SG high during SNOP.
42	RW	ENOP_FORCE_SG: ENOP: Set the SG high during ENOP (including LOOP phase).
43	RW	NO_WAIT_ON_CLK_CMD: 0 = A clock change request first waits the OPCG_WAIT cycles. 1 = A clock change request does not wait, when not in flush.
44:45	RW	ALIGN_SOURCE_SELECT: 0 = Use the INOPA setting from opcg_reg0. 1 = Use the rising edge of the synchronization pulse. 2 = Use the unit0_sync_lvl to align (for AVP refresh0). 3 = Use the unit1_sync_lvl to align (for AVP efresh1).
46	RW	UNUSED46: Unused.

Bits	SCOM	Field Mnemonic: Description
47:51	RW	SCAN_RATIO: This field contains the scan ratio (n = 0 - 15: (n+1):1, 16: 24:1, 17: 32:1, 18: 48:1, 19: 64:1, 20: 128:1). The default is 4:1 = 00011.
52:63	RW	OPCG_WAIT_CYCLES: This field contains the old PAD value. It is the delay at the beginning and end of the OPCG run that allows DC signals to arrive at the right time (0 4095). It must be higher than the pipeline latch depth. The default is 0x020.

Register Name	OPCG Control Register 0
Mnemonic	TP.TCXB.XB.OPCG_REG0
Address	0000000006030002 (SCOM)
Description	This register contains OPCG controls.

Bits	SCOM	Field Mnemonic: Description
0	RW	RUNN_MODE: 0 = BIST-mode is used for the LBIST. 1 = RUNN-mode is used for the ABIST/IOBIST.
1	RWX	OPCG_GO: Start the OPCG. This bit is cleared when the OPCG is done. Poll for opcg_done in the cplt_start register.
2	RWX	RUN_SCAN0: Run scan0. This bit overrides all the BIST mode settings except the scan_ratio. It starts a scan0 run. The bit is cleared when the OPCG is done. Poll for opcg_done in the cplt_start register.
3	RW	SCAN0_MODE: Set the PRPGs in scan0_mode but do not run the automatic scan0 sequence.
4	RWX	OPCG_IN_SLAVE_MODE: When selected, the OPCG waits for the master chiplet to get started. When Keep_MS_Mode is 0, SLAVE_MODE is cleared after an incoming trigger.
5	RWX	OPCG_IN_MASTER_MODE: When selected, the OPCG sends a trigger to all slave chiplets, When Keep_MS_MODE equals 0, MASTER_MODE is cleared after sending out one master trigger.
6	RW	KEEP_MS_MODE: When set to 1, the OPCG in master/slave mode bits are not cleared after one incoming OPCG trigger. The default is clear the master/slave mode bits.
7	RW	TRIGGER_OPCG_ON_UNIT0_SYNC_LVL: The unit pin is used for the AVP can trigger OPCG (unit0_sync_lvl).
8	RW	TRIGGER_OPCG_ON_UNIT1_SYNC_LVL: The unit pin used for the AVP can trigger OPCG (unit1_sync_lvl).
9	RWX	RUN_CHIPLET_SCAN0: Run scan0 on all regions and types. will clear the chiplet at all.
10	RWX	RUN_CHIPLET_SCAN0_NO_PLL: Run scan0 on all regions and types. This clears the chiplet at all exclude PLL regions. The PLL can keep running.
11	RW	RUN_OPCG_ON_UPDATE_DR: Start the OPCG engine when the scan updated signal (update_dr) is received (set pulse). This bit must be set to 1 for a set-pulse WRITE.
12	RW	RUN_OPCG_ON_CAPTURE_DR: Start the OPCG engine when the scan updated (capture_dr) is received (set pulse) This bit must be set to 1 for a set-pulse READ.
13	RW	STOP_RUNN_ON_XSTOP: Run-N mode: This bit stops run-n on a checkstop.
14	RW	OPCG_STARTS_BIST: Run-N mode: The OPCG engine controls start_bist for ABIST or IOBIST. For more information, see the BIST Register on page 151.
15:20	RW	UNUSED1520: Unused.
21:63	RWX	LOOP_COUNT: This field is the loop counter for LBIST and RUNN. When written, it contains the target value. When read, it contains the current counter value. It counts from 0 to the target value.

Register Name	OPCG Control Register 1
Mnemonic	TP.TCXB.XB.OPCG_REG1
Address	0000000006030003 (SCOM)
Description	This register contains OPCG controls.

Bits	SCOM	Field Mnemonic: Description
0:11	RW	SCAN_COUNT: BIST mode: Channel scan count (s = 0 - 4095) runn-mode: start_bist match value(0:11).
12:23	RW	MISR_A_VAL: BIST mode: The a value for the MISR aperture. runn-mode: start_bist match value(12:23).
24:35	RW	MISR_B_VAL: BIST mode: The b value for the MISR aperture. runn-mode: start_bist match value(24:35).
36:47	RW	MISR_INIT_WAIT: BIST mode: The delay MISR aperture. The MISRs become active after this number of loops.
48	RW	OPCG_SUPPRESS_EVEN_CLK: When this bit is set, the OPCG only creates even, not odd, clocks. This bit is used for runn to create only one clock in the fast domain. The default is 0.
49	RW	SCAN_CLK_USE_EVEN: When this bit is set, the OPCG generates a scan clock in even cycles instead of odd. The default is 0 (odd) for a scan.
50:51	RW	UNUSED2: Unused.
52	RW	RTIM_THOLD_FORCE: This bit forces rtim_thold low when not in test_dc mode. (It must be 0 at all times.)
53	RW	DISABLE_ARY_CLK_DURING_FILL: LBIST and SCAN0: This bit prevents the firing of ARY HLD during an NSL-fill.
54	RW	SG_HIGH_DURING_FILL: LBIST and SCAN0: Hold SG high during an NSL-fill.
55:56	RW	LBIST_SKITTER_CTL: BIST mode: 00 = Enable skitter during lbist_ip. 01 = Enable skitter when misr_active. See misr_init_wait. 10 = Skitter OPCG_GO mode. The falling edge = start. The rising edge = stop. 11 = Unused.
57	RW	MISR_MODE: BIST mode: MISR aperture mode. 0 = a-1 to b-1. 1 = Start to a and b to end.
58	RW	INFINITE_MODE: Infinite mode. RUNN and LBIST run forever and ignore the loop count.
59:63	RW	NSL_FILL_COUNT: BIST mode: NSL-fill count (0 - 31).

Register Name	OPCG Control Register 2
Mnemonic	TP.TCXB.XB.OPCG_REG2
Address	0000000006030004 (SCOM)
Description	This register contains OPCG controls.

Bits	SCOM	Field Mnemonic: Description
0	RWX	OPCG_GO2: OPCG go for broadcast sequences (start sequence).
1:3	RW	PRPG_WEIGHTING: prpg_activate: 1/2, 1/4, 1/8, 1/16, 1/2, 3/4, 7/8, 15/16.
4:15	RWX	PRPG_VALUE: This bit is set to 0 for PRPG always on. Else seed.
16:27	RW	PRPG_A_VAL: This field contains the a value for the PRPG aperture.
28:39	RW	PRPG_B_VAL: This field contains the b value for the PRPG aperture.
40	RW	PRPG_MODE: PRPG aperture mode. 0 = a-1 to b-1. 1 = Start to a and b to end.

Bits	SCOM	Field Mnemonic: Description
41:63	RW	UNUSED41_63: unused.

Register Name	Scan Region and Type Register
Mnemonic	TP.TCXB.XB.SCAN_REGION_TYPE
Address	0000000006030005 (SCOM)
Description	This register identifies the scan regions and types.

Bits	SCOM	Field Mnemonic: Description
0	RWX	SYSTEM_FAST_INIT: The default is 0. When this bit is set to 1, the MASK bits in the CMSK chain decide which part is scanned or scan0. MASK = 1 = scan0. MASK = 0 = part or scan chain.
1:2	RO	constant = 0b00
3	NCX	SCAN_REGION_VITL: Scan clock region vitl (vital = clock).
4	RWX	SCAN_REGION_PERV: Scan clock region perv (pervasive).
5	RWX	SCAN_REGION_UNIT1: Scan clock region iox0 - iof.
6	RWX	SCAN_REGION_UNIT2: Scan clock region iox1 - iof.
7	RWX	SCAN_REGION_UNIT3: Scan clock region iox2 - iof.
8	RWX	SCAN_REGION_UNIT4: Scan clock region ioppe - iof.
9	RWX	SCAN_REGION_UNIT5: Scan clock region pbiox0 - pb.
10	RWX	SCAN_REGION_UNIT6: Scan clock region pbiox1 - pb.
11	RWX	SCAN_REGION_UNIT7: Scan clock region pbiox2 - pb.
12	RWX	SCAN_REGION_UNIT8: Scan clock region unused.
13	RWX	SCAN_REGION_UNIT9: Scan clock region unused.
14	RWX	SCAN_REGION_UNIT10: Scan clock region plliox - iof.
15:47	RO	constant = 0b000000000000000000000000000000000
48	RW	SCAN_TYPE_FUNC: Scan chain func (functional).
49	RW	SCAN_TYPE_CFG: Scan chain mode (boot configuration and debug configuration).
50	RW	SCAN_TYPE_CCFG_GPTR: Scan chain CCFG or GPTR (pervasive: CCFG, others: GPTR).
51	RW	SCAN_TYPE_REGF: Scan chain regf (register files).
52	RW	SCAN_TYPE_LBIST: Scan chain lbst (LBIST).
53	RW	SCAN_TYPE_ABIST: Scan chain abst (ABIST).
54	RW	SCAN_TYPE_REPR: Scan chain repr (array repair).
55	RW	SCAN_TYPE_TIME: Scan chain time (array timing).
56	RW	SCAN_TYPE_BNDY: Scan chain bndy (boundary I/Os).
57	RW	SCAN_TYPE_FARR: Scan chain farr (fast array unload).
58	RW	SCAN_TYPE_CMSK: Scan chain cmsk (LBIST channel mask).
59	RW	SCAN_TYPE_INEX: Scan chain idex (c14 ASIC).
60:63	RO	constant = 0b0000

Register Name	Start/Stop Clocks Register
Mnemonic	TP.TCXB.XB.CLK_REGION
Address	0000000006030006 (SCOM)
Description	This register controls clock regions.

Bits	SCOM	Field Mnemonic: Description
0:1	RWX	CLOCK_CMD: This field contains the command for clock control: 00 = NOP 01 = Start 10= Stop 11 = Pulse (one pulse).
2	RWX	SLAVE_MODE: When selected, the clock command waits for the master chiplet to get started. This bit is cleared after an incoming slave trigger and Keep_MS_Mode_after_trigger is set to 0.
3	RWX	MASTER_MODE: When selected, the clock command sends out a trigger to all slave chiplets. This bit is cleared after sending out one master trigger and Keep_MS_Mode_after_trigger is set to 0.
4	RWX	CLOCK_REGION_PERV: For clock region perv (Pervasive).
5	RWX	CLOCK_REGION_UNIT1: For clock region iox0 - iof.
6	RWX	CLOCK_REGION_UNIT2: For clock region iox1 - iof.
7	RWX	CLOCK_REGION_UNIT3: For clock region iox2 - iof.
8	RWX	CLOCK_REGION_UNIT4: For clock region ioppe - iof.
9	RWX	CLOCK_REGION_UNIT5: For clock region pbiox0 - pb.
10	RWX	CLOCK_REGION_UNIT6: For clock region pbiox1 - pb.
11	RWX	CLOCK_REGION_UNIT7: For clock region pbiox2 - pb.
12	RWX	CLOCK_REGION_UNIT8: For clock region unused.
13	RWX	CLOCK_REGION_UNIT9: For clock region unused.
14	RWX	CLOCK_REGION_UNIT10: For clock region plliox - iof.
15:47	RO	constant = 0b000000000000000000000000000000000
48	RWX	SEL_THOLD_SL: Select the SL thresholds.
49	RWX	SEL_THOLD_NSL: Select the NSL thresholds.
50	RWX	SEL_THOLD_ARY: Select the array thresholds.
51	RO	constant = 0b0
52	RW	CLOCK_PULSE_USE_EVEN: For dual mesh support. The default for pulse is the odd phase. When this bit is set, the pulse is applied on the even phase.
53:63	RO	constant = 0b00000000000

Register Name	SL Clock Status Register
Mnemonic	TP.TCXB.XB.CLOCK_STAT_SL
Address	0000000006030008 (SCOM)
Description	This register contains clock status.

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b1111

Bits	SCOM	Field Mnemonic: Description
4	ROX	CLOCK_STATUS_PERV_SL: This bit indicates the status of the pervasive SL HLD. 0 = Run. 1 = Stop.
5	ROX	CLOCK_STATUS_UNIT1_SL: This bit indicates the status of iox0 - iof SL HLD. 0 = Run. 1 = Stop.
6	ROX	CLOCK_STATUS_UNIT2_SL: This bit indicates the status of iox1 - iof SL HLD. 0 = Run. 1 = Stop.
7	ROX	CLOCK_STATUS_UNIT3_SL: This bit indicates the status of iox2 - iof SL HLD. 0 = Run. 1 = Stop.
8	ROX	CLOCK_STATUS_UNIT4_SL: This bit indicates the status of ioppe - iof SL HLD. 0 = Run. 1 = Stop.
9	ROX	CLOCK_STATUS_UNIT5_SL: This bit indicates the status of pbiox0 - pb SL HLD. 0 = Run. 1 = Stop.
10	ROX	CLOCK_STATUS_UNIT6_SL: This bit indicates the status of pbiox1 - pb SL HLD. 0 = Run. 1 = Stop.
11	ROX	CLOCK_STATUS_UNIT7_SL: This bit indicates the status of pbiox2 - pb SL HLD. 0 = Run. 1 = Stop.
12	ROX	CLOCK_STATUS_UNIT8_SL: This bit indicates the status of unused SL HLD. 0 = Run. 1 = Stop.
13	ROX	CLOCK_STATUS_UNIT9_SL: This bit indicates the status of unused SL HLD. 0 = Run. 1 = Stop.
14	ROX	CLOCK_STATUS_UNIT10_SL: This bit indicates the status of plliox - iof SL HLD. 0 = Run. 1 = Stop.
15:63	RO	constant = 0b1111111111111111111111111111111111111111111111111

Register Name	NSL Clock Status Register
Mnemonic	TP.TCXB.XB.CLOCK_STAT_NSL
Address	0000000006030009 (SCOM)
Description	This register contains clock status.

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b1111
4	ROX	CLOCK_STATUS_PERV_NSL: This bit indicates the status of pervasive NSL HLD. 0 = Run. 1 = Stop.
5	ROX	CLOCK_STATUS_UNIT1_NSL: This bit indicates the status of iox0 - iof NSL HLD. 0 = Run. 1 = Stop.

Bits	SCOM	Field Mnemonic: Description
6	ROX	CLOCK_STATUS_UNIT2_NSL: This bit indicates the status of iox1 - iof NSL HLD. 0 = Run. 1 = Stop.
7	ROX	CLOCK_STATUS_UNIT3_NSL: This bit indicates the status of iox2 - iof NSL HLD. 0 = Run. 1 = Stop.
8	ROX	CLOCK_STATUS_UNIT4_NSL: This bit indicates the status of ioppe - iof NSL HLD. 0 = Run. 1 = Stop.
9	ROX	CLOCK_STATUS_UNIT5_NSL: This bit indicates the status of pbiox0 - pb NSL HLD. 0 = Run. 1 = Stop.
10	ROX	CLOCK_STATUS_UNIT6_NSL: This bit indicates the status of pbiox1 - pb NSL HLD. 0 = Run. 1 = Stop.
11	ROX	CLOCK_STATUS_UNIT7_NSL: This bit indicates the status of pbiox2 - pb NSL HLD. 0 = Run. 1 = Stop.
12	ROX	CLOCK_STATUS_UNIT8_NSL: This bit indicates the status of unused NSL HLD. 0 = Run. 1 = Stop.
13	ROX	CLOCK_STATUS_UNIT9_NSL: This bit indicates the status of unused NSL HLD. 0 = Run. 1 = Stop.
14	ROX	CLOCK_STATUS_UNIT10_NSL: This bit indicates the status of plliox - iof NSL HLD. 0 = Run. 1 = Stop.
15:63	RO	constant = 0b1111111111111111111111111111111111111111111111111

Register Name	Array Clock Status Register
Mnemonic	TP.TCXB.XB.CLOCK_STAT_ARY
Address	000000000603000A (SCOM)
Description	This register contains clock status.

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b1111
4	ROX	CLOCK_STATUS_PERV_ARY: This bit indicates the status of the pervasive array HLD. 0 = Run. 1 = Stop.
5	ROX	CLOCK_STATUS_UNIT1_ARY: This bit indicates the status of iox0 - iof array HLD. 0 = Run. 1 = Stop.
6	ROX	CLOCK_STATUS_UNIT2_ARY: This bit indicates the status of iox1 - iof array HLD. 0 = Run. 1 = Stop.
7	ROX	CLOCK_STATUS_UNIT3_ARY: This bit indicates the status of iox2 - iof array HLD. 0 = Run. 1 = Stop.

Bits	SCOM	Field Mnemonic: Description
8	ROX	CLOCK_STATUS_UNIT4_ARY: This bit indicates the status of ioppe - iof array HLD. 0 = Run. 1 = Stop.
9	ROX	CLOCK_STATUS_UNIT5_ARY: This bit indicates the status of pbiox0 - pb array HLD. 0 = Run. 1 = Stop.
10	ROX	CLOCK_STATUS_UNIT6_ARY: This bit indicates the status of pbiox1 - pb array HLD. 0 = Run. 1 = Stop.
11	ROX	CLOCK_STATUS_UNIT7_ARY: This bit indicates the status of pbiox2 - pb array HLD. 0 = Run. 1 = Stop.
12	ROX	CLOCK_STATUS_UNIT8_ARY: This bit indicates the status of unused array HLD. 0 = Run. 1 = Stop.
13	ROX	CLOCK_STATUS_UNIT9_ARY: This bit indicates the status of unused array HLD. 0 = Run. 1 = Stop.
14	ROX	CLOCK_STATUS_UNIT10_ARY: This bit indicates the status of plliox - iof array HLD. 0 = Run. 1 = Stop.
15:63	RO	constant = 0b1111111111111111111111111111111111111111111111111

Register Name	BIST Register
Mnemonic	TP.TCXB.XB.BIST
Address	000000000603000B (SCOM)
Description	This register provides ABIST and IOBIST controls per region.

Bits	SCOM	Field Mnemonic: Description
0	RW	TC_BIST_START_TEST_DC: Keep this bit 0 during ABIST/IOBIST. It can be used to bypass the RUN-N start. When this bit is set, the BIST_START_TEST goes high immediately without waiting for RUN-N. BIST starts with the first HLD clock cycle.
1	RW	TC_SRAM_ABIST_MODE_DC: This bit selects the ABIST engines for SRAMs.
2	RW	TC_EDRAM_ABIST_MODE_DC: This bit selects the ABIST engines for eDRAMs.
3	RW	TC_IOBIST_MODE_DC: This bit selects the IOBIST engines.
4	RW	BIST_PERV: Pervasive region: 1 = BIST_START_TEST for this region is triggered. 0 = The region does not take part in the ABIST/IOBIST run.
5	RW	BIST_UNIT1: Region iox0 - iof: 1 = BIST_START_TEST for this region is triggered. 0 = The region does not take part in the ABIST/IOBIST run
6	RW	BIST_UNIT2: Region iox1 - iof: 1 = BIST_START_TEST for this region is triggered. 0 = The region does not take part in the ABIST/IOBIST run
7	RW	BIST_UNIT3: Region iox2 - iof: 1 = BIST_START_TEST for this region is triggered. 0 = The region does not take part in the ABIST/IOBIST run

Bits	SCOM	Field Mnemonic: Description
8	RW	BIST_UNIT4: Region ioppe - iof: 1 = BIST_START_TEST for this region is triggered. 0 = The region does not take part in the ABIST/IOBIST run
9	RW	BIST_UNIT5: Region pbiox0 - pb: 1 = BIST_START_TEST for this region is triggered. 0 = The region does not take part in the ABIST/IOBIST run
10	RW	BIST_UNIT6: Region pbiox1 - pb: 1 = BIST_START_TEST for this region is triggered. 0 = The region does not take part in the ABIST/IOBIST run
11	RW	BIST_UNIT7: Region pbiox2 - pb: 1 = BIST_START_TEST for this region is triggered. 0 = The region does not take part in the ABIST/IOBIST run
12	RW	BIST_UNIT8: Region unused: 1 = BIST_START_TEST for this region is triggered. 0 = The region does not take part in the ABIST/IOBIST run
13	RW	BIST_UNIT9: Region unused: 1 = BIST_START_TEST for this region is triggered. 0 = The region does not take part in the ABIST/IOBIST run
14	RW	BIST_UNIT10: Region plliox - iof: 1 = BIST_START_TEST for this region is triggered. 0 = The region does not take part in the ABIST/IOBIST run
15:47	RO	constant = 0b000000000000000000000000000000000
48	RW	BIST_STROBE_WINDOW_EN: This bit enables the strobe window only in TE = 1 mode. The OPCGGO tester pin enables ABIST compare after the ABIST is started. A special setup in the ABIST engine is required. The default is 0. System mode cannot enable this feature.
49:63	RO	constant = 0b000000000000000

Register Name	Checkstop Register 1
Mnemonic	TP.TCXB.XB.XSTOP1
Address	000000000603000C (SCOM)
Description	This register provides checkstop controls per region.

Bits	SCOM	Field Mnemonic: Description
0	RW	XSTOP1_MASK_B: This bit is a mask for a checkstop to clockstop of select regions (see xstop_perv, xstop_unit0..n). 0 = Ignore checkstop. 1 = Stop on checkstop.
1	RW	XSTOP1_UNUSED:
2	RW	TRIGGER_OPCG_ON_XSTOP1: This bit triggers OPCG on a checkstop instead of performing a clockstop.
3	RW	XSTOP1_WAIT_ALLWAYS: When set to 1, a checkstop waits independent from flush. The default is no wait, when flush is not set.
4	RW	XSTOP1_PERV: Region pervasive: 1 = The region is stopped. 0 = The region keeps running on a checkstop.
5	RW	XSTOP1_UNIT1: Region iox0 - iof: 1 = The region is stopped. 0 = The region keeps running on a checkstop.

Bits	SCOM	Field Mnemonic: Description
6	RW	XSTOP1_UNIT2: Region iox1 - iof: 1 = The region is stopped. 0 = The region keeps running on a checkstop.
7	RW	XSTOP1_UNIT3: Region iox2 - iof: 1 = The region is stopped. 0 = The region keeps running on a checkstop.
8	RW	XSTOP1_UNIT4: Region ioppe - iof: 1 = The region is stopped. 0 = The region keeps running on a checkstop.
9	RW	XSTOP1_UNIT5: Region pbiox0 - pb: 1 = The region is stopped. 0 = The region keeps running on a checkstop.
10	RW	XSTOP1_UNIT6: Region pbiox1 - pb: 1 = The region is stopped. 0 = The region keeps running on a checkstop.
11	RW	XSTOP1_UNIT7: Region pbiox2 - pb: 1 = The region is stopped. 0 = The region keeps running on a checkstop.
12	RW	XSTOP1_UNIT8: Region unused: 1 = The region is stopped. 0 = The region keeps running on a checkstop.
13	RW	XSTOP1_UNIT9: Region unused: 1 = The region is stopped. 0 = The region keeps running on a checkstop.
14	RW	XSTOP1_UNIT10: Region plliox - iof: 1 = The region is stopped. 0 = The region keeps running on a checkstop.
15:47	RO	constant = 0b000000000000000000000000000000000
48:59	RW	XSTOP1_WAIT_CYCLES: This field defines how many cycle a checkstop waits, after dropping flush, before thresholds are dropped. Between 0 - 4095 cycles are possible.
60:63	RO	constant = 0b0000

Register Name	Checkstop Register 2
Mnemonic	TP.TCXB.XB.XSTOP2
Address	000000000603000D (SCOM)
Description	This register provides checkstop controls per region.

Bits	SCOM	Field Mnemonic: Description
0	RW	XSTOP2_MASK_B: This bit is a mask for a checkstop to clockstop of select regions (see xstop_perv, xstop_unit0..n). 0 = Ignore checkstop. 1 = Stop on checkstop.
1	RW	XSTOP2_UNUSED: Unused.
2	RW	TRIGGER_OPCG_ON_XSTOP2: This bit triggers OPCG on a checkstop instead of performing a clockstop.
3	RW	XSTOP2_WAIT_ALLWAYS: When set to 1, a checkstop waits independent from flush. The default is no wait, when flush is not set.

Bits	SCOM	Field Mnemonic: Description
4	RW	XSTOP2_PERV: Region pervasive: 1 = The region is stopped. 0 = The region keeps running on a checkstop.
5	RW	XSTOP2_UNIT1: Region iox0 - iof: 1 = The region is stopped. 0 = The region keeps running on a checkstop.
6	RW	XSTOP2_UNIT2: Region iox1 - iof: 1 = The region is stopped. 0 = The region keeps running on a checkstop.
7	RW	XSTOP2_UNIT3: Region iox2 - iof: 1 = The region is stopped. 0 = The region keeps running on a checkstop.
8	RW	XSTOP2_UNIT4: Region ioppe - iof: 1 = The region is stopped. 0 = The region keeps running on a checkstop.
9	RW	XSTOP2_UNIT5: Region pbiox0 - pb: 1 = The region is stopped. 0 = The region keeps running on a checkstop.
10	RW	XSTOP2_UNIT6: Region pbiox1 - pb: 1 = The region is stopped. 0 = The region keeps running on a checkstop.
11	RW	XSTOP2_UNIT7: Region pbiox2 - pb: 1 = The region is stopped. 0 = The region keeps running on a checkstop.
12	RW	XSTOP2_UNIT8: Region unused: 1 = The region is stopped. 0 = The region keeps running on a checkstop.
13	RW	XSTOP2_UNIT9: Region unused: 1 = The region is stopped. 0 = The region keeps running on a checkstop.
14	RW	XSTOP2_UNIT10: Region plliox - iof: 1 = The region is stopped. 0 = The region keeps running on a checkstop.
15:47	RO	constant = 0b000000000000000000000000000000000
48:59	RW	XSTOP2_WAIT_CYCLES: This field defines how many cycle a checkstop waits, after dropping flush, before thresholds are dropped. Between 0 - 4095 cycles are possible.
60:63	RO	constant = 0b0000

Register Name	Checkstop Register 3
Mnemonic	TP.TCXB.XB.XSTOP3
Address	000000000603000E (SCOM)
Description	This register provides checkstop controls per region.

Bits	SCOM	Field Mnemonic: Description
0	RW	XSTOP3_MASK_B: This bit is a mask for a checkstop to clockstop of select regions (see xstop_perv, xstop_unit0..n). 0 = Ignore checkstop. 1 = Stop on checkstop.

Bits	SCOM	Field Mnemonic: Description
1	RW	XSTOP3_UNUSED: Unused.
2	RW	TRIGGER_OPCG_ON_XSTOP3: This bit triggers OPCG on a checkstop instead of performing a clockstop.
3	RW	XSTOP3_WAIT_ALLWAYS: When set to 1, a checkstop waits independent from flush. The default is no wait, when flush is not set.
4	RW	XSTOP3_PERV: Region pervasive: 1 = The region is stopped. 0 = The region keeps running on a checkstop.
5	RW	XSTOP3_UNIT1: Region iox0 - iof: 1 = The region is stopped. 0 = The region keeps running on a checkstop.
6	RW	XSTOP3_UNIT2: Region iox1 - iof: 1 = The region is stopped. 0 = The region keeps running on a checkstop.
7	RW	XSTOP3_UNIT3: Region iox2 - iof: 1 = The region is stopped. 0 = The region keeps running on a checkstop.
8	RW	XSTOP3_UNIT4: Region ioppe - iof: 1 = The region is stopped. 0 = The region keeps running on a checkstop.
9	RW	XSTOP3_UNIT5: Region pbiox0 - pb: 1 = The region is stopped. 0 = The region keeps running on a checkstop.
10	RW	XSTOP3_UNIT6: Region pbiox1 - pb: 1 = The region is stopped. 0 = The region keeps running on a checkstop.
11	RW	XSTOP3_UNIT7: Region pbiox2 - pb: 1 = The region is stopped. 0 = The region keeps running on a checkstop.
12	RW	XSTOP3_UNIT8: Region unused: 1 = The region is stopped. 0 = The region keeps running on a checkstop.
13	RW	XSTOP3_UNIT9: Region unused: 1 = The region is stopped. 0 = The region keeps running on a checkstop.
14	RW	XSTOP3_UNIT10: Region plliox - iof: 1 = The region is stopped. 0 = The region keeps running on a checkstop.
15:47	RO	constant = 0b000000000000000000000000000000000
48:59	RW	XSTOP3_WAIT_CYCLES: This field defines how many cycle a checkstop waits, after dropping flush, before thresholds are dropped. Between 0 - 4095 cycles are possible.
60:63	RO	constant = 0b0000

Register Name	Error Status Register
Mnemonic	TP.TCXB.XB.ERROR_STATUS
Address	000000000603000F (SCOM)
Description	This register contains the clock-controller (CC) error status bits.

Bits	SCOM	Field Mnemonic: Description
0	RWX	PCB_WRITE_NOT_ALLOWED_ERR: This bit indicates a write on a read-only register.
1	RWX	PCB_READ_NOT_ALLOWED_ERR: This bit indicates a read not allowed, maybe a write-only register.
2	RWX	PCB_PARITY_ON_CMD_ERR: This bit indicates a parity error on a command.
3	RWX	PCB_ADDRESS_NOT_VALID_ERR: This bit indicates an invalid address.
4	RWX	PCB_PARITY_ON_ADDR_ERR: This bit indicates a parity error on an address.
5	RWX	PCB_PARITY_ON_DATA_ERR: This bit indicates a parity error on data.
6	RWX	PCB_PROTECTED_ACCESS_INVALID_ERR: This bit indicates a protection violation.
7	RWX	PCB_PARITY_ON_SPCIF_ERR: This bit indicates a parity error on SPCIF.
8	RWX	PCB_WRITE_AND_OPCG_IP_ERR: This bit indicates a PCB write while the OPCG is running.
9	RWX	SCAN_READ_AND_OPCG_IP_ERR: This bit indicates a scan read when the OPCG is running.
10	RWX	CLOCK_CMD_CONFLICT_ERR:This bit indicates a clock command is in progress.
11	RWX	SCAN_COLLISION_ERR: This bit indicates a scan region selected of running region.
12	RWX	PREVENTED_SCAN_COLLISION_ERR: This bit indicates a PCB request to set a scan region that is running.
13	RWX	OPCG_TRIGGER_ERR: This bit indicates a OPCG gets triggered while the OPCG is running.

Bits	SCOM	Field Mnemonic: Description
14	RWX	PHASE_CNT_CORRUPTION_ERR: This bit indicates that phase counters inside the chiplet are out of sync.
15	RWX	CLOCK_CMD_PREVENTED_ERR: This bit indicates a security or scan collision prevented a clock start.
16	RWX	PARITY_ON_OPCG_SM_ERR: This bit indicates a parity error on the OPCG state machine.
17	RWX	PARITY_ON_CLOCK_MUX_REG_ERR: This bit indicates a parity error on the scan, clock region, type, or clock status register.
18	RWX	PARITY_ON_OPCG_REG_ERR: This bit indicates a parity error on the OPCG registers.
19	RWX	PARITY_ON_SYNC_CONFIG_REG_ERR: This bit indicates a parity error on the sync configuration register.
20	RWX	PARITY_ON_XSTOP_REG_ERR: This bit indicates a parity error on the checkstop register.
21	RWX	PARITY_ON_GPIO_REG_ERR: This bit indicates a parity error on the GP0, 4, 5, or 6 registers.
22	RWX	CLKCMD_REQUEST_ERR: This bit indicates a region clock command has one request pending but gets a second one.
23	RWX	CBS_PROTOCOL_ERR: This bit indicates a CBS protocol error. The REQ/ACK sequence is wrong.
24	RWX	VITL_ALIGN_ERR: This bit indicates the VITL alignment is out of sync to the sync pulse.
25	RWX	UNIT_SYNC_LVL_ERR: This bit indicates that the Unit0 and Unit1 sync level pulse are not in sync. The AVP is broken.
26	RWX	PARITY_ON_SELFBOOT_CMD_STATE_ERR: This bit indicates a parity error on the self-boot command state.
27	RWX	UNUSED_ERROR27: Unused.
28	RWX	UNUSED_ERROR28: Unused.
29	RWX	UNUSED_ERROR29: Unused.
30	RWX	UNUSED_ERROR30: Unused.
31	RWX	UNUSED_ERROR31: Unused.

Register Name	OPCG Control Capture Register 1
Mnemonic	TP.TCXB.XB.OPCG_CAPT1
Address	0000000006030010 (SCOM)
Description	This register contains information about sequence cycles.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	COUNT: 0000 = 12 cycles 0001 – 1100 = Cycles 1 – 12. 1101 – 1111 = 24 normal, no fast.
4:8	RW	SEQ_01: Sequence cycle 1 for normal/slow region (sl, nsl, ary, se, fce).
9:13	RW	SEQ_02: Sequence cycle 2 for normal/slow region (sl, nsl, ary, se, fce).
14:18	RW	SEQ_03: Sequence cycle 3 for normal/slow region (sl, nsl, ary, se, fce).
19:23	RW	SEQ_04: Sequence cycle 4 for normal/slow region (sl, nsl, ary, se, fce).
24:28	RW	SEQ_05: Sequence cycle 5 for normal/slow region (sl, nsl, ary, se, fce).
29:33	RW	SEQ_06: Sequence cycle 6 for normal/slow region (sl, nsl, ary, se, fce).
34:38	RW	SEQ_07: Sequence cycle 7 for normal/slow region (sl, nsl, ary, se, fce).

Bits	SCOM	Field Mnemonic: Description
39:43	RW	SEQ_08: Sequence cycle 8 for normal/slow region (sl, nsl, ary, se, fce).
44:48	RW	SEQ_09: Sequence cycle 9 for normal/slow region (sl, nsl, ary, se, fce).
49:53	RW	SEQ_10: Sequence cycle 10 for normal/slow region (sl, nsl, ary, se, fce).
54:58	RW	SEQ_11: Sequence cycle 11 for normal/slow region (sl, nsl, ary, se, fce).
59:63	RW	SEQ_12: Sequence cycle 12 for normal/slow region (sl, nsl, ary, se, fce).

Register Name	OPCG Control Capture Register 2
Mnemonic	TP.TCXB.XB.OPCG_CAPT2
Address	0000000006030011 (SCOM)
Description	This register contains information about sequence cycles.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	UNUSED_CAPT2:
4:8	RW	SEQ_13_01EVEN: Sequence cycle 1. Even, for fast region, or cycle 13, for normal region (sl, nsl, ary, se, fce).
9:13	RW	SEQ_14_01ODD: Sequence cycle 1. Odd, for fast region, or cycle 14, for normal region (sl, nsl, ary, se, fce).
14:18	RW	SEQ_15_02EVEN: Sequence cycle 2. Even, for fast region, or cycle 15, for normal region (sl, nsl, ary, se, fce).
19:23	RW	SEQ_16_02ODD: Sequence cycle 2. Odd, for fast region, or cycle 16, for normal region (sl, nsl, ary, se, fce).
24:28	RW	SEQ_17_03EVEN: Sequence cycle 3. Even, for fast region, or cycle 17, for normal region (sl, nsl, ary, se, fce).
29:33	RW	SEQ_18_03ODD: Sequence cycle 3. Odd, for fast region, or cycle 18, for normal region (sl, nsl, ary, se, fce).
34:38	RW	SEQ_19_04EVEN: Sequence cycle 4. Even, for fast region, or cycle 19, for normal region (sl, nsl, ary, se, fce).
39:43	RW	SEQ_20_04ODD: Sequence cycle 4. Odd, for fast region, or cycle 20, for normal region (sl, nsl, ary, se, fce).
44:48	RW	SEQ_21_05EVEN: Sequence cycle 5. Even, for fast region, or cycle 21, for normal region (sl, nsl, ary, se, fce).
49:53	RW	SEQ_22_05ODD: Sequence cycle 5. Odd, for fast region, or cycle 22, for normal region (sl, nsl, ary, se, fce).
54:58	RW	SEQ_23_06EVEN: Sequence cycle 6 . Even, for fast region, or cycle 23, for normal region (sl, nsl, ary, se, fce).
59:63	RW	SEQ_24_06ODD: Sequence cycle 6. Odd, for fast region, or cycle 24, for normal region (sl, nsl, ary, se, fce).

Register Name	OPCG Control Register Capture 3
Mnemonic	TP.TCXB.XB.OPCG_CAPT3
Address	0000000006030012 (SCOM)
Description	This register contains information about sequence cycles.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	UNUSED_CAPT3:
4:8	RW	SEQ_07EVEN: Sequence cycle 7. Even, for fast region (sl, nsl, ary, se, fce).
9:13	RW	SEQ_07ODD: Sequence cycle 7. Odd, for fast region (sl, nsl, ary, se, fce).
14:18	RW	SEQ_08EVEN: Sequence cycle 8. Even, for fast region (sl, nsl, ary, se, fce).
19:23	RW	SEQ_08ODD: Sequence cycle 8. Odd, for fast region (sl, nsl, ary, se, fce).
24:28	RW	SEQ_09EVEN: Sequence cycle 9. Even, for fast region (sl, nsl, ary, se, fce).
29:33	RW	SEQ_09ODD: Sequence cycle 9. Odd, for fast region (sl, nsl, ary, se, fce).
34:38	RW	SEQ_10EVEN: Sequence cycle 10. Even, for fast region (sl, nsl, ary, se, fce).
39:43	RW	SEQ_10ODD: Sequence cycle 10. Odd, for fast region (sl, nsl, ary, se, fce).
44:48	RW	SEQ_11EVEN: Sequence cycle 11. Even, for fast region (sl, nsl, ary, se, fce).
49:53	RW	SEQ_11ODD: Sequence cycle 11. Odd, for fast region (sl, nsl, ary, se, fce).
54:58	RW	SEQ_12EVEN: Sequence cycle 12. Even, for fast region (sl, nsl, ary, se, fce).
59:63	RW	SEQ_12ODD: Sequence cycle 12. Odd, for fast region (sl, nsl, ary, se, fce).

Register Name	Debug CBS CC Register
Mnemonic	TP.TCXB.XB.DBG_CBS_CC
Address	0000000006030013 (SCOM)
Description	This register is used for debugging.

Bits	SCOM	Field Mnemonic: Description
0	ROX	DBG_RESET_EP: Reset the endpoint. Are the CC and CTRL in a reset state?
1	ROX	DBG_OPCG_IP: OPCG in progress, not idle.
2	ROX	DBG_VITL_CLKOFF: VITL HLD stopped, when enabled. Need pipeline-latch-depth cycles to switch this latch.
3	ROX	DBG_TEST_ENABLE: Test enable.
4	ROX	DBG_CBS_REQ: CBS interface: request (latched).
5:7	ROX	DBG_CBS_CMD: CBS interface: command (latched).
8:12	ROX	DBG_CBS_STATE: CBS command state machine. 00000 = Idle.
13	ROX	DBG_SECURITY_DEBUG_MODE: Status of the security mode bit.
14	ROX	DBG_CBS_PROTOCOL_ERROR: CBS protocol error. A REQ is raised, although the state machine is not in IDLE. Need reset_ep to clear this bit. There is no impact on the IPL.
15	ROX	DBG_PCB_IDLE: The PCB interface is in the IDLE state.

Bits	SCOM	Field Mnemonic: Description
16:19	ROX	DBG_CURRENT_OPCG_MODE: This field contains the current or latest OPCG mode. 0 = NOP. 1 = LBIST. 2 = ABIST. 3 = RUNN. 4 = SCAN0. 5 = SCAN. 6 = SCAN rotate. 7 = SCAN with UpdateDR. 8 = SCAN with CaptureDR. 9 = CLK Change Request. 0 – 15 = Unused.
20:23	ROX	DBG_LAST_OPCG_MODE: Previous OPCG mode.
24	ROX	DBG_PCB_ERROR: PCB interface error. Read the CC Error Register or set CBS_CMD = 001 to switch FSI CBS debug information to the CC Error Register.
25	ROX	DBG_PARITY_ERROR: Any parity error or non-PCB parity. Read the CC Error Register or set CBS_CMD = 001 to switch FSI CBS Debug Information to the CC Error Register.
26	ROX	DBG_CC_ERROR: Any other CC error. Read the CC Error Register or set CBS_CMD = 001 to switch FSI CBS debug information to the CC Error Register.
27	ROX	DBG_CHIPLET_IS_ALIGNED: This bit 1 when the a valid align pulse was send out.
28	ROX	DBG_PCB_REQUEST_SINCE_RESET: Reset clears this bit. The first PCB request sets it.
29	ROX	DBG_PARANOIA_TEST_ENABLE_CHANGE: The rising or falling edge on test enable, after reset. Need reset_ep to clear. There is no impact on IPL.
30	ROX	DBG_PARANOIA_VITL_CLKOFF_CHANGE: Rising or falling edge on vitl_clkoff, after reset. Need reset_ep to clear. There is no impact on IPL.
31	ROX	TP_TPFSI_CBS_ACK: Only representation of the CC ACK signal going to the FSI.

Register Name	CC Protect Mode Register
Mnemonic	TP.TCXB.XB.CC_PROTECT_MODE_REG
Address	00000000060303FE (SCOM)
Description	This register enables read and write protection.

Bits	SCOM	Field Mnemonic: Description
0	RW	CC_READ_PROTECT_ENABLE: Enable read protection.
1	RW	CC_WRITE_PROTECT_ENABLE: Enable write protection.

Register Name	Atomic Lock Register
Mnemonic	TP.TCXB.XB.CC_ATOMIC_LOCK_REG
Address	00000000060303FF (SCOM)
Description	This register enables an atomic lock.

Bits	SCOM	Field Mnemonic: Description
0	RW	CC_ATOMIC_LOCK_ENABLE: This bit enables an atomic lock.
1:4	ROX	CC_ATOMIC_ID: This field contains the atomic ID.
5:7	RO	constant = 0b000

Bits	SCOM	Field Mnemonic: Description
8:15	ROX	CC_ATOMIC_ACTIVITY: This field is the atomic lock counter.

Register Name	Global Checkstop FIR
Mnemonic	TP.TCXB.XB.XFIR
Address	0000000006040000 (SCOM)
Description	This is a fault-isolation register for global FIRs.

Bits	SCOM	Field Mnemonic: Description
0	RWX	XFIR_IN0: Summary bit (any checkstop).
1	RWX	XFIR_IN1: Checkstop broadcast over the OOB.
2	RWX	XFIR_IN2: Unused.
3	RWX	XFIR_IN3: Checkstop from the pervasive unit.
4	RWX	XFIR_IN4: Checkstop from PBIOX0.
5	RWX	XFIR_IN5: Checkstop from PBIOX1.
6	RWX	XFIR_IN6: Checkstop from PBIOX2 FIR.
7	RWX	XFIR_IN7: Unused.
8	RWX	XFIR_IN8: Checkstop from IOX0 FIR.
9	RWX	XFIR_IN9: Checkstop from IOX1 FIRP.
10	RWX	XFIR_IN10: Checkstop from IOX2 FIR.
11	RWX	XFIR_IN11: Checkstop from IOPPE FIR.
12:25	RWX	XFIR_IN12: Unused.
26	RWX	XFIR_IN26: Checkstop on the debug trigger.

Register Name	Global Recoverable FIR
Mnemonic	TP.TCXB.XB.RFIR
Address	0000000006040001 (SCOM)
Description	This is a fault-isolation register for global recoverable errors.

Bits	SCOM	Field Mnemonic: Description
0	ROX	RFIR_IN0: Local checkstop from PBIOX0, PBIOX1, PBIOX2, IOPPE.
1	ROX	LFIR_RECOV_ERR: Recoverable error from the pervasive unit.
2	ROX	RFIR_IN4: Recoverable error from PBIOX0.
3	ROX	RFIR_IN5: Recoverable error from PBIOX1.
4	ROX	RFIR_IN6: Recoverable error from PBIOX2.
5	ROX	RFIR_IN7: unused.
6	ROX	RFIR_IN8: Recoverable error from IOX0 FIR.
7	ROX	RFIR_IN9: Recoverable error from IOX1 FIR.
8	ROX	RFIR_IN10: Recoverable error from IOX2 FIR.
9	ROX	RFIR_IN11: Recoverable error from IOPPE FIR.

Bits	SCOM	Field Mnemonic: Description
10:23	ROX	RFIR_IN12: Unused.

Register Name	FIR Mask Register
Mnemonic	TP.TCXB.XB.FIR_MASK
Address	0000000006040002 (SCOM)
Description	This is a FIR mask register.

Bits	SCOM	Field Mnemonic: Description
0	RW	FIR_MASK_IN0: Mask for the XFIR summary bit (any checkstop).
1	RW	FIR_MASK_IN1: Mask for the XFIR from other chiplets.
2	RW	FIR_MASK_IN2: unused.
3	RW	FIR_MASK_IN3: Mask for the XFIR from the pervasive unit.
4	RW	FIR_MASK_IN4: Mask for PBIOX0 XFIR and RFIR.
5	RW	FIR_MASK_IN5: Mask for PBIOX1 XFIR and RFIR.
6	RW	FIR_MASK_IN6: Mask for PBIOX2 XFIR and RFIR.
7	RW	FIR_MASK_IN7: Unused.
8	RW	FIR_MASK_IN8: Mask for IOX0 XFIR and RFIR.
9	RW	FIR_MASK_IN9: Mask for IOX1 XFIR and RFIR.
10	RW	FIR_MASK_IN10: Mask for IOX2 XFIR and RFIR.
11	RW	FIR_MASK_IN11: Mask for IOPPE XFIR and RFIR.
12:25	RW	FIR_MASK_IN12: Unused.
26	RW	FIR_MASK_IN26: Mask for debug trigger and local checkstop to recoverable error.

Register Name	Special Attention Register
Mnemonic	TP.TCXB.XB.SPATTN
Address	0000000006040004 (SCOM) 0000000006040005 (SCOM1) 0000000006040006 (SCOM2)
Description	This register contains special attention fields.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	ROX	NCX	NCX	SPATTN_IN0: Special attention from PBIOx0.
1	ROX	NCX	NCX	SPATTN_IN1: Special attention from PBIOx1.
2	ROX	NCX	NCX	SPATTN_IN2: Special attention from PBIOx2.
3	ROX	NCX	NCX	SPATTN_IN3: Unused.
4	ROX	NCX	NCX	SPATTN_IN4: Special attention from IOx0.
5	ROX	NCX	NCX	SPATTN_IN5: Special attention from IOx1.
6	ROX	NCX	NCX	SPATTN_IN6: Special attention from IOx2.
7	ROX	NCX	NCX	SPATTN_IN7: Special attention from IOPPE.
8	ROX	NCX	NCX	SPATTN_IN8: Unused special attentions.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
9	ROX	NCX	NCX	SPATTN_IN9: Unused special attentions.

Register Name	Special Attention Mask Register
Mnemonic	TP.TCXB.XB.SPA_MASK
Address	0000000006040007 (SCOM)
Description	This register provides a special attention mask.

Bits	SCOM	Field Mnemonic: Description
0:9	RW	SPA_MASK_IN: Special attention mask.

Register Name	Mode Register
Mnemonic	TP.TCXB.XB.EPS.FIR.MODE_REG
Address	0000000006040008 (SCOM)
Description	This register contains mode bits.

Bits	SCOM	Field Mnemonic: Description
0	RW	MODE_IN0: Unused.
1	RW	MODE_IN1: Unused.
2	RW	MODE_IN2: Unused.
3	RW	MODE_IN3: Unused.
4	RW	MODE_IN4: Stop chip TOD on checkstop (unused in POWER9).
5	RW	MODE_IN5: Stop chip TOD on recoverable (unused in POWER9).
6	RW	MODE_IN6: Disable the propagation of checkstops to other chips.
7	RW	MODE_IN7: Unused.
8	RW	MODE_IN8: Enable checkstop on special attention.
9	RW	MODE_IN9: Mask direct/local error.
10	RW	MODE_IN10: Unused.
11	RW	MODE_IN11: Unused.
12:15	RW	MODE_IN: Unused.

Register Name	Host Attention Register
Mnemonic	TP.TCXB.XB.HOSTATTN
Address	0000000006040009 (SCOM)
Description	This register contains host attention bits.

Bits	SCOM	Field Mnemonic: Description
0	ROX	HOSTATTN_IN0: Host Attention Summary Bit.
1	ROX	HOSTATTN_IN1: Unused.
2	ROX	HOSTATTN_IN2: Unused.

Bits	SCOM	Field Mnemonic: Description
3	ROX	HOSTATTN_IN3: Unused.
4	ROX	HOSTATTN_IN4: Unused.
5	ROX	HOSTATTN_IN5: Unused.
6	ROX	HOSTATTN_IN6: Unused.
7	ROX	HOSTATTN_IN7: Unused.
8	ROX	HOSTATTN_IN8: Unused.
9	ROX	HOSTATTN_IN9: Unused.
10	ROX	HOSTATTN_IN10: Unused.
11	ROX	HOSTATTN_IN11: Unused.
12	ROX	HOSTATTN_IN12: Unused.
13	ROX	HOSTATTN_IN13: Unused.
14	ROX	HOSTATTN_IN14: Unused.
15	ROX	HOSTATTN_IN15: Unused.
16	ROX	HOSTATTN_IN16: Unused.
17	ROX	HOSTATTN_IN17: Unused.
18	ROX	HOSTATTN_IN18: Unused.
19	ROX	HOSTATTN_IN19: Unused.
20	ROX	HOSTATTN_IN20: Unused.
21	ROX	HOSTATTN_IN21: Unused.
22	ROX	HOSTATTN_IN22: Unused.

Register Name	Local FIR
Mnemonic	TP.TCXB.XB.LOCAL_FIR
Address	000000000604000A (SCOM) 000000000604000B (SCOM1) 000000000604000C (SCOM2)
Description	This is a fault-isolation register for local errors.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_IN0: CFIR internal parity error.
1	RWX	WOX_AND	WOX_OR	FIR_IN1: Local errors from GPIO (PCB error).
2	RWX	WOX_AND	WOX_OR	FIR_IN2: Local errors from CC (PCB error).
3	RWX	WOX_AND	WOX_OR	FIR_IN3: Local errors from CC (OPCG, parity, scan collision, and so on).
4	RWX	WOX_AND	WOX_OR	FIR_IN4: Local errors from PSC (PCB error).
5	RWX	WOX_AND	WOX_OR	FIR_IN5: Local errors from PSC (parity error).
6	RWX	WOX_AND	WOX_OR	FIR_IN6: Local errors from Thermal (parity error).
7	RWX	WOX_AND	WOX_OR	FIR_IN7: Local errors from Thermal (PCB error).
8	RWX	WOX_AND	WOX_OR	FIR_IN8: Local errors from Thermal (Trip error critical).
9	RWX	WOX_AND	WOX_OR	FIR_IN9: Local errors from Thermal (Trip error fatal).
10	RWX	WOX_AND	WOX_OR	FIR_IN10: Thermal voltage trip error.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
11	RWX	WOX_AND	WOX_OR	FIR_IN11: Local errors from Debug (error).
12	RWX	WOX_AND	WOX_OR	FIR_IN12: Local errors from Trace Array 0 (SCOM error).
13	RWX	WOX_AND	WOX_OR	FIR_IN13: Local errors from Trace Array 0.
14	RWX	WOX_AND	WOX_OR	FIR_IN14: Local errors from Trace Array 1 (SCOM error).
15	RWX	WOX_AND	WOX_OR	FIR_IN15: Local errors from Trace Array 1.
16	RWX	WOX_AND	WOX_OR	FIR_IN16: Unused.
17	RWX	WOX_AND	WOX_OR	FIR_IN17: Unused.
18	RWX	WOX_AND	WOX_OR	FIR_IN18: Unused.
19	RWX	WOX_AND	WOX_OR	FIR_IN19: Unused.
20	RWX	WOX_AND	WOX_OR	FIR_IN20: Unused.
21	RWX	WOX_AND	WOX_OR	FIR_IN21: Unused.
22	RWX	WOX_AND	WOX_OR	FIR_IN22: Unused.
23	RWX	WOX_AND	WOX_OR	FIR_IN23: Unused.
24	RWX	WOX_AND	WOX_OR	FIR_IN24: Unused.
25	RWX	WOX_AND	WOX_OR	FIR_IN25: Unused.
26	RWX	WOX_AND	WOX_OR	FIR_IN26: Unused.
27	RWX	WOX_AND	WOX_OR	FIR_IN27: Unused.
28	RWX	WOX_AND	WOX_OR	FIR_IN28: Unused.
29	RWX	WOX_AND	WOX_OR	FIR_IN29: Unused.
30	RWX	WOX_AND	WOX_OR	FIR_IN30: Unused.
31	RWX	WOX_AND	WOX_OR	FIR_IN31: Unused.
32	RWX	WOX_AND	WOX_OR	FIR_IN32: Unused.
33	RWX	WOX_AND	WOX_OR	FIR_IN33: Unused.
34	RWX	WOX_AND	WOX_OR	FIR_IN34: Unused.
35	RWX	WOX_AND	WOX_OR	FIR_IN35: Unused.
36	RWX	WOX_AND	WOX_OR	FIR_IN36: Unused.
37	RWX	WOX_AND	WOX_OR	FIR_IN37: Unused.
38	RWX	WOX_AND	WOX_OR	FIR_IN38: Unused.
39	RWX	WOX_AND	WOX_OR	FIR_IN39: Unused.
40	RWX	WOX_AND	WOX_OR	FIR_IN40: Unused.
41	RWX	WOX_AND	WOX_OR	FIR_IN41: Malfunction alert broadcast via the OOB.

Register Name	Local FIR Mask Register
Mnemonic	TP.TCXB.XB.EPS.FIR.LOCAL_FIR_MASK
Address	000000000604000D (SCOM) 000000000604000E (SCOM1) 000000000604000F (SCOM2)
Description	This register masks the local FIR bits.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:41	RW	WO_AND	WO_OR	LFIR_MASK_IN: Mask for the LEM error collection vector.

Register Name	Local FIR Action0 Register
Mnemonic	TP.TCXB.XB.EPS.FIR.LOCAL_FIR_ACTION0
Address	0000000006040010 (SCOM)
Description	Local FIR Action0

Bits	SCOM	Field Mnemonic: Description
0:41	RW	FIR_ACTION0_IN: Action0 mask.

Register Name	Local FIR Action1 Register
Mnemonic	TP.TCXB.XB.EPS.FIR.LOCAL_FIR_ACTION1
Address	0000000006040011 (SCOM)
Description	Local FIR Action1

Bits	SCOM	Field Mnemonic: Description
0:41	RW	FIR_ACTION1_IN: Action1 mask.

Register Name	Group Checkstop Mask Register
Mnemonic	TP.TCXB.XB.EPS.FIR.GXSTOP_TRIG_REG
Address	0000000006040013 (SCOM)
Description	This register masks group checkstops.

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP_TRIG_IN0: Mask bit for a system checkstop.
1	RW	GXSTP_TRIG_IN1: Mask bit for a recoverable error.
2	RW	GXSTP_TRIG_IN2: Mask bit for a special attention.
3	RW	GXSTP_TRIG_IN3: Mask bit for a local checkstop.
4	RW	GXSTP_TRIG_IN4: Mask bit for a type 4 error (host attention).
5	RW	GXSTP_TRIG_IN5: Mask bit for an OOB sys_checkstop input (0).
6	RW	GXSTP_TRIG_IN6: Mask bit for an OOB sys_checkstop input (1).
7	RW	GXSTP_TRIG_IN7: Mask bit for a group checkstop input (0).
8	RW	GXSTP_TRIG_IN8: Mask bit for a group checkstop input (1).
9	RW	GXSTP_TRIG_IN9: Mask bit for a debug checkstop on a trigger.
10	RW	GXSTP_TRIG_IN10: Unused.
11	RW	GXSTP_TRIG_IN11: Unused.

Register Name	Group0 Checkstop Mask Register
Mnemonic	TP.TCXB.XB.EPS.FIR.GXSTOP0_MASK_REG
Address	0000000006040014 (SCOM)
Description	This register masks group 0 checkstops.

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP0_TRIG_IN0: Mask bit for system checkstop.
1	RW	GXSTP0_TRIG_IN1: Mask bit for a recoverable error.
2	RW	GXSTP0_TRIG_IN2: Mask bit for a special attention.
3	RW	GXSTP0_TRIG_IN3: Mask bit for a local checkstop.
4	RW	GXSTP0_TRIG_IN4: Mask bit for a type 4 error (host attention).
5	RW	GXSTP0_TRIG_IN5: Mask bit for an OOB sys_checkstop input (0).
6	RW	GXSTP0_TRIG_IN6: Mask bit for an OOB sys_checkstop input (1).
7	RW	GXSTP0_TRIG_IN7: Mask bit for a group checkstop input (0).
8	RW	GXSTP0_TRIG_IN8: Mask bit for a group checkstop input (1).
9	RW	GXSTP0_TRIG_IN9: Mask bit for a debug checkstop on a trigger.
10	RW	GXSTP0_TRIG_IN10: Unused.
11	RW	GXSTP0_TRIG_IN11: Unused.

Register Name	Group1 Checkstop Mask Register
Mnemonic	TP.TCXB.XB.EPS.FIR.GXSTOP1_MASK_REG
Address	0000000006040015 (SCOM)
Description	This register masks group 1 checkstops.

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP1_TRIG_IN0: Mask bit for a system checkstop.
1	RW	GXSTP1_TRIG_IN1: Mask bit for a recoverable error.
2	RW	GXSTP1_TRIG_IN2: Mask bit for a special attention.
3	RW	GXSTP1_TRIG_IN3: Mask bit for a local checkstop.
4	RW	GXSTP1_TRIG_IN4: Mask bit for a type 4 error (host attention).
5	RW	GXSTP1_TRIG_IN5: Mask bit for an OOB sys_checkstop input (0).
6	RW	GXSTP1_TRIG_IN6: Mask bit for an OOB sys_checkstop input (1).
7	RW	GXSTP1_TRIG_IN7: Mask bit for a group checkstop input (0).
8	RW	GXSTP1_TRIG_IN8: Mask bit for a group checkstop input (1).
9	RW	GXSTP1_TRIG_IN9: Mask bit for a debug checkstop on a trigger.
10	RW	GXSTP1_TRIG_IN10: Unused.
11	RW	GXSTP1_TRIG_IN11: Unused.

Register Name	Group2 Checkstop Mask Register
Mnemonic	TP.TCXB.XB.EPS.FIR.GXSTOP2_MASK_REG
Address	0000000006040016 (SCOM)
Description	This register masks group 2 checkstops.

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP2_TRIG_IN0: Mask bit for a system checkstop.
1	RW	GXSTP2_TRIG_IN1: Mask bit for a recoverable error.
2	RW	GXSTP2_TRIG_IN2: Mask bit for a special attention.
3	RW	GXSTP2_TRIG_IN3: Mask bit for a local checkstop.
4	RW	GXSTP2_TRIG_IN4: Mask bit for a type 4 error (host attention).
5	RW	GXSTP2_TRIG_IN5: Mask bit for an OOB sys_checkstop input (0).
6	RW	GXSTP2_TRIG_IN6: Mask bit for an OOB sys_checkstop input (1).
7	RW	GXSTP2_TRIG_IN7: Mask bit for a group checkstop input (0).
8	RW	GXSTP2_TRIG_IN8: Mask bit for a group checkstop input (1).
9	RW	GXSTP2_TRIG_IN9: Mask bit for a debug checkstop on a trigger.
10	RW	GXSTP2_TRIG_IN10: Unused.
11	RW	GXSTP2_TRIG_IN11: Unused.

Register Name	Summary Mask Register
Mnemonic	TP.TCXB.XB.EPS.FIR.SUM_MASK_REG
Address	0000000006040017 (SCOM)
Description	This register contains summary bits.

Bits	SCOM	Field Mnemonic: Description
0	RW	SMASK_IN0: System checkstop summary bit.
1	RW	SMASK_IN1: Recoverable summary bit.
2	RW	SMASK_IN2: Special attention summary bit.
3	RW	SMASK_IN3: Local checkstop summary bit.
4	RW	SMASK_IN4: Type4 host attention summary bit.

Register Name	Local Checkstop Register
Mnemonic	TP.TCXB.XB.LOCAL_XSTOP_ERR
Address	0000000006040018 (SCOM)
Description	This register contains local checkstop bits.

Bits	SCOM	Field Mnemonic: Description
0	ROX	LOCAL_XSTOP_IN0: Local checkstop summary bit 0.
1	ROX	LOCAL_XSTOP_IN1: Local checkstop from pbiox0 bit 0.
2	ROX	LOCAL_XSTOP_IN2: Local checkstop from pbiox1 bit 0.

Bits	SCOM	Field Mnemonic: Description
3	ROX	LOCAL_XSTOP_IN3: Local checkstop from pbiox2 bit 0.
4	ROX	LOCAL_XSTOP_IN4: Unused.
5	ROX	LOCAL_XSTOP_IN5: Local checkstop from iox0.
6	ROX	LOCAL_XSTOP_IN6: Local checkstop from iox1.
7	ROX	LOCAL_XSTOP_IN7: Local checkstop from iox2.
8	ROX	LOCAL_XSTOP_IN8: Local checkstop from ppe.
9	ROX	LOCAL_XSTOP_IN9: Unused.
10	ROX	LOCAL_XSTOP_IN10: Unused.
11	ROX	LOCAL_XSTOP_IN11: Unused.
12	ROX	LOCAL_XSTOP_IN12: Unused.
13	ROX	LOCAL_XSTOP_IN13: Unused.
14	ROX	LOCAL_XSTOP_IN14: Unused.
15	ROX	LOCAL_XSTOP_IN15: Unused.
16	ROX	LOCAL_XSTOP_IN16: Unused.
17	ROX	LOCAL_XSTOP_IN17: Unused.
18	ROX	LOCAL_XSTOP_IN18: Unused.
19	ROX	LOCAL_XSTOP_IN19: Unused.
20	ROX	LOCAL_XSTOP_IN20: Unused.
21	ROX	LOCAL_XSTOP_IN21: Unused.
22	ROX	LOCAL_XSTOP_IN22: Unused.

Register Name	Local Checkstop Mask Register
Mnemonic	TP.TCXB.XB.LOCAL_XSTOP_MASK
Address	0000000006040019 (SCOM)
Description	This register masks local checkstops.

Bits	SCOM	Field Mnemonic: Description
0:21	RW	LOCAL_XSTOP_MASK_IN: Local checkstop mask.

Register Name	Host Attention Mask Register
Mnemonic	TP.TCXB.XB.HOSTATTN_MASK
Address	000000000604001A (SCOM)
Description	This register masks host attention.

Bits	SCOM	Field Mnemonic: Description
0:21	RW	HOSTATTN_MASK_IN: Host attention mask.

Register Name	DTS Loop1 Results Register
Mnemonic	TP.TCXB.XB.EPS.THERM.DTS_RESULT0
Address	0000000006050000 (SCOM)
Description	This register contains digital thermal sensor (DTS) results.

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	DTS_0_RESULT: Calibrated DTS result of the sensor with ID 0.
16:31	ROX	DTS_1_RESULT: Calibrated DTS result of the sensor with ID 1.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	DTS Trace Results Register
Mnemonic	TP.TCXB.XB.EPS.THERM.DTS_TRC_RESULT
Address	0000000006050003 (SCOM)
Description	This register contains DTS trace results.

Bits	SCOM	Field Mnemonic: Description
0:43	ROX	TIMESTAMP_COUNTER_VALUE: Time stamp counter value during DTS trace mode.
44	ROX	TIMESTAMP_COUNTER_OVERFLOW_ERR: Overflow error bit of the time stamp counter value during DTS trace mode.
45:47	RO	constant = 0b000
48:63	ROX	DTS_1_RESULT: Calibrated DTS result of the sensor with ID 1.

Register Name	CPM and DTS Enables and Controls Register
Mnemonic	TP.TCXB.XB.EPS.THERM.THERM_MODE_REG
Address	000000000605000F (SCOM)
Description	This register is used to enable and control the critical path monitor (CPM) and digital thermal sensor (DTS).

Bits	SCOM	Field Mnemonic: Description
0	RW	THERM_DIS_CPM_BUBBLE_CORR: Critical path result bubble correction active.
1	RW	THERM_FORCE_THRES_ACT: This bit forces tpc_therm_thres_mac clock gating off and activates the clocks.
2:4	RW	THERM_THRES_TRIP_ENA: therm_thres_trip compare enables. 1xx = trip0 – warning. x1x = trip1 – critical. xx1 = trip2 – fatal.
5	RW	THERM_DTS_SAMPLE_ENA: 0 = No DTS sampling. 1 = DTS sampling is enabled and a below counter compare match can occur.

Bits	SCOM	Field Mnemonic: Description
6:9	RW	THERM_SAMPLE_PULSE_CNT: A 16 MHz sample pulse is fed into an 18-bit counter. With the therm_sample_pulse_cnt it is possible to select a high-order bit of the counter to enable resolutions of sampling DTSs between 2.5 µs and 80 ms. An edge-detection circuit detects the rising edge of the selected counter bit, and this triggers a DTS sample. 0000 = 16 ms 0001 = 8 ms 0010 = 4 ms 0011 = 2 ms 0100 = 1 ms 0101 = 0.5 ms 0110 = 250 µs 0111 = 125 µs 1000 = 62 .5 µs 1001 = 31.3 µs 1010 = 15.6 µs 1011 = 7.8 µs 1100 = 3.9 µs 1101 = 2 µs 1110 = 1 µs 1111 = 0.5 µs
10:11	RW	THERM_THRES_MODE_ENA: Forces maximum or minimum mode in the threshold unit: 00 = Is off. 11 = Is legal. 10 = Maximum mode. 01 = Minimum mode.
12	RW	DTS_TRIGGER_MODE: Unused.
13	RW	DTS_TRIGGER_SEL: Unused.
14	RW	THERM_THRES_OVERFLOW_MASK: 0 = therm_overflow_err is enabled. 1 = therm_overflow_err is disabled.
15	RW	THERM_MODE_UNUSED: Unused.
16:19	RW	THERM_DTS_READ_SEL: Selects which DTS result is provided with PCB read addr_v(4): 0000 = DTS 0 0001 = DTS 1 0010 = DTS 2 0100 = DTS 4 1111 = Worst-case sensor
20:21	RW	THERM_DTS_ENABLE_L1: Loop1 DTS enables: 1x = DTS 0 available. x1 = DTS 1 available.
22:34	RO	constant = 0b0000000000000
35:36	RW	Reserved field.

Register Name	Skitter Control Register
Mnemonic	TP.TCXB.XB.EPS.THERM.SKITTER_MODE_REG
Address	0000000006050010 (SCOM)
Description	This register controls skitter.

Bits	SCOM	Field Mnemonic: Description
0	RW	SKITTER_HOLD_SAMPLE: Forces skitter to hold the current sample.

Bits	SCOM	Field Mnemonic: Description
1	RW	DISABLE_SKITTER_STICKINESS: If '0', accumulation mode. A '1' samples a new value each cycle and resets the sticky value.
2:3	RW	SKITTER_MODE_UNUSED1: Unused.
4:5	RW	SKITTER_HOLD_DBGTRIG_SEL: bit0 = hold_on_trigger0 bit1 = hold_on_trigger1
6:7	RW	SKITTER_RESET_TRIG_SEL: bit0 = reset_sticky_on_trigger0 bit1 = reset_sticky_on_trigger1
8:9	RW	SKITTER_SAMPLE_GUTS: Selects the guts to measure: 00 = guts1. 01 = guts2. 10 = guts3. 11 = guts4.
10:43	RO	constant = 0b0000000000000000000000000000000000
44	ROX	SKITTER_HOLD_SAMPLE_WITH_TRIGGER: Forces skitter to hold the current sample on the DBG trigger. This has the highest priority.
45	ROX	SKITTER_DATA_V_LT:If '1', the data requested by a skitter force read register has finished and data is present in the skitter data register in the collector macro. The data can be read by any combination of V25/V26/V27 PCB reads.

Register Name	Error Injection Control Register
Mnemonic	TP.TCXB.XB.EPS.THERM.INJECT_REG
Address	0000000006050011 (SCOM)
Description	This register controls error injection.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	THERM_INJECT_TRIP: 00 = No injection. 01 = Warning trip-level injection. 10 = Critical trip-level injection. 11 = Fatal trip-level injection.
2:3	RW	THERM_INJECT_MODE: 00 = No injection. 01 = Injection on the next DTS sample. 10 = Solid injection for the next DTS samples until the bit setting changes. 11 = Not used.

Register Name	Control/Force Reset Register
Mnemonic	TP.TCXB.XB.EPS.THERM.CONTROL_REG
Address	0000000006050012 (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0	WO_1P	Reserved field.
1	WO_1P	Reserved field.

Bits	SCOM	Field Mnemonic: Description
2	WO_1P	Reserved field.
3	WO_1P	Reserved field.
4	WO_1P	Reserved field.
5	WO_1P	Reserved field.
6	WO_1P	Reserved field.
7	WO_1P	Reserved field.
8	WO_1P	Reserved field.
9	WO_1P	Reserved field.
10	WO_1P	Reserved field.
11	WO_1P	Reserved field.
12	WO_1P	Reserved field.

Register Name	Thermal Error Status Register
Mnemonic	TP.TCXB.XB.EPS.THERM.ERR_STATUS_REG
Address	0000000006050013 (SCOM)
Description	This register contains error masks.

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	Reserved field.
2	ROX	Reserved field.
3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.
7	ROX	Reserved field.
8	ROX	Reserved field.
9	ROX	Reserved field.
10	ROX	Reserved field.
11	ROX	Reserved field.
12	ROX	Reserved field.
13	ROX	Reserved field.
14	ROX	Reserved field.
15	ROX	Reserved field.
16	ROX	SERIAL_SHIFTCNT_MODEREG_PARITY_ERR_MASK: Serial shift-count parity error mask.
17	ROX	THERM_MODEREG_PARITY_ERR_MASK: Thermal-mode register parity error mask.
18	ROX	SKITTER_MODEREG_PARITY_ERR_MASK: Skitter-mode register parity error mask.
19	ROX	SKITTER_FORCEREG_PARITY_ERR_MASK: Skitter force register parity error mask.
20	ROX	SCAN_INIT_VERSION_REG_PARITY_ERR_MASK: Scan init version register parity error mask.

Bits	SCOM	Field Mnemonic: Description
21	ROX	VOLT_MODEREG_PARITY_ERR_MASK: Volt mode register parity error mask.
22	RO	constant = 0b0
23	ROX	COUNT_STATE_ERR_MASK: Count state machine error mask.
24	ROX	RUN_STATE_ERR_MASK: Run state machine error mask.
25	ROX	THRES_STATE_ERR_MASK: Threshold state machine error mask.
26	ROX	OVERFLOW_ERR_MASK: DTS calibration calculation overflow error mask.
27	ROX	SHIFTER_PARITY_ERR_MASK: Shifter parity error mask.
28	ROX	SHIFTER_VALID_ERR_MASK: Shifter valid error mask.
29	ROX	TIMEOUT_ERR_MASK: Timeout error mask.
30	ROX	F_SKITTER_READ_ERR_MASK: Force skitter read one hot error mask.
31	ROX	PCB_ERR_MASK: Pervasive control bus error mask.
32:39	RO	constant = 0b00000000
40:43	ROX	Reserved field.
44:46	ROX	Reserved field.
47	ROX	Reserved field.
48	ROX	Reserved field.
49:50	ROX	Reserved field.
51:54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Skitter Force Read Register
Mnemonic	TP.TCXB.XB.EPS.THERM.SKITTER_FORCE_REG
Address	0000000006050014 (SCOM)
Description	This register forces a skitter read.

Bits	SCOM	Field Mnemonic: Description
0	RW	F_SKITTER_READ: Forces the read of that particular skitter.

Register Name	Skitter Clock SRC Control Register
Mnemonic	TP.TCXB.XB.EPS.THERM.SKITTER_CLKSRC_REG
Address	0000000006050016 (SCOM)
Description	This register contains skitter controls.

Bits	SCOM	Field Mnemonic: Description
0:2	RW	SKITTER0_CLKSRC: Selects the clock to measure: 000 = Local mesh clock 001 = External pin skitter_c1_1_in 010 = Local d1clk only if d_mode = 1 011 = External pin skitter_c1_2_in 100 = Local lclk only if d_mode = 1 101 = External pin skitter_c1_3_in 110 = Unused 111 = External pin skitter_c1_4_in
3:35	RO	constant = 0b000000000000000000000000000000000
36:37	RW	SKITTER0_DELAY_SELECT: Selects the delay to be added between the clock source multiplexer and the inverter chain of skitter0. (The base line delay is 12.2 psec.) 00 = No delay 01 = 0.6 psec 10 = 1.8 psec 11 = 5 psec

Register Name	Skitter Data Register Read Bits 0:63
Mnemonic	TP.TCXB.XB.EPS.THERM.SKITTER_DATA0
Address	0000000006050019 (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	RESERVED.

Register Name	Skitter Data Register Read Bits 32:95
Mnemonic	TP.TCXB.XB.EPS.THERM.SKITTER_DATA1
Address	000000000605001A (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	RESERVED.

Register Name	Skitter Data Register Read Bits 64:127
Mnemonic	TP.TCXB.XB.EPS.THERM.SKITTER_DATA2
Address	000000000605001B (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	RESERVED.

Register Name	Time Stamp Counter Read Register
Mnemonic	TP.TCXB.XB.EPS.THERM.TIMESTAMP_COUNTER_READ
Address	000000000605001C (SCOM)
Description	This register contains the time-stamp counter value during DTS trace mode and an overflow error bit.

Bits	SCOM	Field Mnemonic: Description
0:43	ROX	TIMESTAMP_COUNTER_VALUE: Time-stamp counter value during DTS trace mode.
44	ROX	TIMESTAMP_COUNTER_OVERFLOW_ERR: Overflow error bit of the time stamp counter value during DTS trace mode.

3. XBUS Chiplet PCB Slave

The POWER9 processor registers are listed alphabetically by mnemonic in the following address table.

Mnemonic	Address	Page
TP.TPCHIP.NET.PCBSLXB.ASSIST_INTERRUPT_REG	0x00000000060F0011	180
TP.TPCHIP.NET.PCBSLXB.ATOMIC_LOCK_REG	0x00000000060F03FF	187
TP.TPCHIP.NET.PCBSLXB.ATTN_INTERRUPT_REG	0x00000000060F001A	181
TP.TPCHIP.NET.PCBSLXB.EDRAM_STATUS	0x00000000060F0029	185
TP.TPCHIP.NET.PCBSLXB.ERROR_REG	0x00000000060F001F	182
TP.TPCHIP.NET.PCBSLXB.HANG_PULSE_0_REG	0x00000000060F0020	183
TP.TPCHIP.NET.PCBSLXB.HANG_PULSE_1_REG	0x00000000060F0021	183
TP.TPCHIP.NET.PCBSLXB.HANG_PULSE_2_REG	0x00000000060F0022	183
TP.TPCHIP.NET.PCBSLXB.HANG_PULSE_3_REG	0x00000000060F0023	184
TP.TPCHIP.NET.PCBSLXB.HANG_PULSE_4_REG	0x00000000060F0024	184
TP.TPCHIP.NET.PCBSLXB.HANG_PULSE_5_REG	0x00000000060F0025	184
TP.TPCHIP.NET.PCBSLXB.HANG_PULSE_6_REG	0x00000000060F0026	184
TP.TPCHIP.NET.PCBSLXB.HEARTBEAT_REG	0x00000000060F0018	181
TP.TPCHIP.NET.PCBSLXB.MULTICAST_GROUP_1	0x00000000060F0001	178
TP.TPCHIP.NET.PCBSLXB.MULTICAST_GROUP_2	0x00000000060F0002	178
TP.TPCHIP.NET.PCBSLXB.MULTICAST_GROUP_3	0x00000000060F0003	179
TP.TPCHIP.NET.PCBSLXB.MULTICAST_GROUP_4	0x00000000060F0004	179
TP.TPCHIP.NET.PCBSLXB.NET_CTRL0	0x00000000060F0040	185
TP.TPCHIP.NET.PCBSLXB.NET_CTRL1	0x00000000060F0044	186
TP.TPCHIP.NET.PCBSLXB.PLL_LOCK_REG	0x00000000060F0019	181
TP.TPCHIP.NET.PCBSLXB.PRE_COUNTER_REG	0x00000000060F0028	185
TP.TPCHIP.NET.PCBSLXB.PRIMARY_ADDRESS_REG	0x00000000060F0000	177
TP.TPCHIP.NET.PCBSLXB.PROTECT_MODE_REG	0x00000000060F03FE	187
TP.TPCHIP.NET.PCBSLXB.RECOV_INTERRUPT_REG	0x00000000060F001B	181
TP.TPCHIP.NET.PCBSLXB.SLAVE_CONFIG_REG	0x00000000060F001E	182
TP.TPCHIP.NET.PCBSLXB.TIMEOUT_REG	0x00000000060F0010	180
TP.TPCHIP.NET.PCBSLXB.VITAL_SCAN_OUT	0x00000000060F0017	180
TP.TPCHIP.NET.PCBSLXB.XSTOP_INTERRUPT_REG	0x00000000060F001C	181

The POWER9 processor registers are listed in the following tables.

Register Name	Primary PCB Slave Address Register
Mnemonic	TP.TPCHIP.NET.PCBSLXB.PRIMARY_ADDRESS_REG
Address	00000000060F0000 (SCOM)
Description	This register contains the PCB slave's primary address.

Bits	SCOM	Field Mnemonic: Description
0:5	RO	Reserved.

Register Name	Multicast Group 1 Register
Mnemonic	TP.TPCHIP.NET.PCBSLXB.MULTICAST_GROUP_1
Address	00000000060F0001 (SCOM)
Description	Multicast Group Registers 1 – 4 are used to are used to assign chiplets to a specific multicast group within the pervasive connect bus (PCB). Multicast groups make it possible to address more than a single chiplet at a time. They are used to read or write the same resource in multiple chiplets at the same time. **Note:** Multicast groups are initially set up at IPL, but they can be modified at any time by firmware or power management code.

Bits	SCOM	Field Mnemonic: Description
0:2	RO	constant = 111
3:5	RW	MULTICAST1_GROUP: Multicast group1 setting. Set this field to a multicast group that this chiplet should be a member of. The chiplet can be assigned to up to four multicast groups by setting this field in the four multicast group registers to the corresponding multicast group numbers. If the chiplet is member of less than four multicast groups, set this field to 0b111 in the multicast group register that is not required. The 0b111 setting indicates multicast group 7; all chiplets are members of multicast group 7 regardless of any multicast register being set to 0b111. 000: Multicast group 0. 001: Multicast group 1. 010: Multicast group 2. 011: Multicast group 3. 100: Multicast group 4 – unused. 101: Multicast group 5 – unused. 110: Multicast group 6 – unused. 111: Multicast group 7.

Register Name	Multicast Group 2 Register
Mnemonic	TP.TPCHIP.NET.PCBSLXB.MULTICAST_GROUP_2
Address	00000000060F0002 (SCOM)
Description	Multicast Group Registers 1 – 4 are used to are used to assign chiplets to a specific multicast group within the pervasive connect bus (PCB). Multicast groups make it possible to address more than a single chiplet at a time. They are used to read or write the same resource in multiple chiplets at the same time. **Note:** Multicast groups are initially set up at IPL, but they can be modified at any time by firmware or power management code.

Bits	SCOM	Field Mnemonic: Description
0:2	RO	constant = 111

Bits	SCOM	Field Mnemonic: Description
3:5	RW	MULTICAST2_GROUP: Multicast group2 setting. Set this field to a multicast group that this chiplet should be a member of. The chiplet can be assigned to up to four multicast groups by setting this field in the four multicast group registers to the corresponding multicast group numbers. If the chiplet is member of less than four multicast groups, set this field to 0b111 in the multicast group register that is not required. The 0b111 setting indicates multicast group 7; all chiplets are members of multicast group 7 regardless of any multicast register being set to 0b111. 000: Multicast group 0. 001: Multicast group 1. 010: Multicast group 2. 011: Multicast group 3. 100: Multicast group 4 – unused. 101: Multicast group 5 – unused. 110: Multicast group 6 – unused. 111: Multicast group 7.

Register Name	Multicast Group 3 Register
Mnemonic	TP.TPCHIP.NET.PCBSLXB.MULTICAST_GROUP_3
Address	00000000060F0003 (SCOM)
Description	Multicast Group Registers 1 – 4 are used to are used to assign chiplets to a specific multicast group within the pervasive connect bus (PCB). Multicast groups make it possible to address more than a single chiplet at a time. They are used to read or write the same resource in multiple chiplets at the same time. **Note:** Multicast groups are initially set up at IPL, but they can be modified at any time by firmware or power management code.

Bits	SCOM	Field Mnemonic: Description
0:2	RO	constant = 111
3:5	RW	MULTICAST3_GROUP: Multicast group3 setting. Set this field to a multicast group that this chiplet should be a member of. The chiplet can be assigned to up to four multicast groups by setting this field in the four multicast group registers to the corresponding multicast group numbers. If the chiplet is member of less than four multicast groups, set this field to 0b111 in the multicast group register that is not required. The 0b111 setting indicates multicast group 7; all chiplets are members of multicast group 7 regardless of any multicast register being set to 0b111. 000: Multicast group 0. 001: Multicast group 1. 010: Multicast group 2. 011: Multicast group 3. 100: Multicast group 4 – unused. 101: Multicast group 5 – unused. 110: Multicast group 6 – unused. 111: Multicast group 7.

Register Name	Multicast Group 4 Register
Mnemonic	TP.TPCHIP.NET.PCBSLXB.MULTICAST_GROUP_4
Address	00000000060F0004 (SCOM)
Description	Multicast Group Registers 1 – 4 are used to are used to assign chiplets to a specific multicast group within the pervasive connect bus (PCB). Multicast groups make it possible to address more than a single chiplet at a time. They are used to read or write the same resource in multiple chiplets at the same time. **Note:** Multicast groups are initially set up at IPL, but they can be modified at any time by firmware or power management code.

Bits	SCOM	Field Mnemonic: Description
0:2	RO	constant = 111
3:5	RW	MULTICAST4_GROUP: Multicast group4 setting. Set this field to a multicast group that this chiplet should be a member of. The chiplet can be assigned to up to four multicast groups by setting this field in the four multicast group registers to the corresponding multicast group numbers. If the chiplet is member of less than four multicast groups, set this field to 0b111 in the multicast group register that is not required. The 0b111 setting indicates multicast group 7; all chiplets are members of multicast group 7 regardless of any multicast register being set to 0b111. 000: Multicast group 0. 001: Multicast group 1. 010: Multicast group 2. 011: Multicast group 3. 100: Multicast group 4 – unused. 101: Multicast group 5 – unused. 110: Multicast group 6 – unused. 111: Multicast group 7.

Register Name	Timeout Select Register
Mnemonic	TP.TPCHIP.NET.PCBSLXB.TIMEOUT_REG
Address	00000000060F0010 (SCOM)
Description	This register contains the int_timeout setting.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	Reserved field.

Register Name	Assist Interrupt Register
Mnemonic	TP.TPCHIP.NET.PCBSLXB.ASSIST_INTERRUPT_REG
Address	00000000060F0011 (SCOM)
Description	This register contains the attn, recov, and xstop (checkstop) settings.

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved.
1	ROX	Reserved.
2	ROX	Reserved.

Register Name	Vital Scan Out Register
Mnemonic	TP.TPCHIP.NET.PCBSLXB.VITAL_SCAN_OUT
Address	00000000060F0017 (SCOM)
Description	This register contains the vital scan out settings.

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved.

Register Name	Chiplet Heartbeat Register
Mnemonic	TP.TPCHIP.NET.PCBSLXB.HEARTBEAT_REG
Address	00000000060F0018 (SCOM)
Description	This register indicates whether a chiplet heartbeat is detected.

Bits	SCOM	Field Mnemonic: Description
0	ROX	HEARTBEAT_DEAD: A chiplet heartbeat is not detected.

Register Name	PLL Lock Indications Register
Mnemonic	TP.TPCHIP.NET.PCBSLXB.PLL_LOCK_REG
Address	00000000060F0019 (SCOM)
Description	This register contains lock indications from the PLLs,

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	Reserved.

Register Name	Attention Interrupt Register
Mnemonic	TP.TPCHIP.NET.PCBSLXB.ATTN_INTERRUPT_REG
Address	00000000060F001A (SCOM)
Description	This register contains the attn setting.

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved.

Register Name	Recovery Interrupt Register
Mnemonic	TP.TPCHIP.NET.PCBSLXB.RECOV_INTERRUPT_REG
Address	00000000060F001B (SCOM)
Description	This register contains the recoverable interrupt setting.

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.

Register Name	Checkstop Interrupt Register
Mnemonic	TP.TPCHIP.NET.PCBSLXB.XSTOP_INTERRUPT_REG
Address	00000000060F001C (SCOM)
Description	This register contains the checkstop interrupt setting.

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.

Register Name	Slave Configuration Register
Mnemonic	TP.TPCHIP.NET.PCBSLXB.SLAVE_CONFIG_REG
Address	00000000060F001E (SCOM)
Description	This is the slave configuration register.

Bits	SCOM	Field Mnemonic: Description
0	RW	CFG_DISABLE_PERV_THOLD_CHECK: This bit disables the pervasive threshold check.
1	RW	CFG_DISABLE_MALF_PULSE_GEN: This bit disables pulse generation for a malfunction alert. Switch back to level.
2	RW	CFG_STOP_HANG_CNT_SYS_XSTP: This bit disables the hang counter stop for a system checkstop.
3	RW	CFG_DISABLE_CL_ATOMIC_LOCK: This bit disables the atomic lock for the chiplet accesses.
4	RW	CFG_DISABLE_HEARTBEAT: This bit disables the check for voltage and gridclock in the chiplet.
5	RW	CFG_DISABLE_FORCE_TO_ZERO: This bit disables the force to zero for error cases.
6	RW	CFG_PM_DISABLE: This bit disables the power management set/reset interface for net_ctrl registers.
7	RW	CFG_PM_MUX_DISABLE: This bit disables the power-management multiplex request signal.
8:13	RW	ERROR_MASK: These are mask bits for slave error reporting.
14:15	RW	RESERVED.

Register Name	Error Capture Register
Mnemonic	TP.TPCHIP.NET.PCBSLXB.ERROR_REG
Address	00000000060F001F (SCOM)
Description	This register is used to capture errors.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	CE_ERROR: Correctable error on the PCB bus.
1:3	RWX_WCLEAR	CHIPLET_ERRORS: Errors reported by chiplet. 000 = No error. 001 = XSCOM command blocked due to pending errors. 010 = Chiplet offline. 011 = Partial good. 100 = Invalid address, address error, or bad access type. 101 = Clock error. 110 = Parity error, received unexpected packet, or wrong packet number. 111 = Timeout. This register is for debug purposes only. It only holds meaningful data if it is cleared after each error.
4	RWX_WCLEAR	PARITY_ERROR: Parity error on the PCB interface.
5	RWX_WCLEAR	DATA_BUFFER_ERROR: Parity error in the data buffer.
6	RWX_WCLEAR	ADDR_BUFFER_ERROR: Parity error in the address buffer.
7	RWX_WCLEAR	PCB_FSM_ERROR: Invalid state error in the PCB FSM.
8	RWX_WCLEAR	CL_FSM_ERROR: Invalid state error in the chiplet FSM.
9	RWX_WCLEAR	INT_RX_FSM_ERROR: Invalid state error in the interrupt RX FSM.
10	RWX_WCLEAR	INT_TX_FSM_ERROR: Invalid state error in the interrupt TX FSM.
11	RWX_WCLEAR	INT_TYPE_ERROR: Invalid interrupt type.
12	RWX_WCLEAR	CL_DATA_ERROR: Parity error on the chiplet interface.

Bits	SCOM	Field Mnemonic: Description
13	RWX_WCLEAR	INFO_ERROR: Parity error on the chiplet information lines.
14	RWX_WCLEAR	UNUSED_0:
15	RWX_WCLEAR	CHIPLET_ATOMIC_LOCK_ERROR: Chiplet atomic lock error.
16	RWX_WCLEAR	PCB_INTERFACE_ERROR: Error on the PCB interface component for the internal endpoint.
17	RWX_WCLEAR	CHIPLET_OFFLINE: A heartbeat check indicated that the chiplet is offline.
18	RWX_WCLEAR	EDRAM_SEQUENCE_ERR: Error in eDRAM power-up sequence.
19	RWX_WCLEAR	CTRL_REG_PARITY_ERROR: The control register parity is bad.
20	RWX_WCLEAR	ADDRESS_REG_PARITY_ERROR: The address register parity is bad.
21	RWX_WCLEAR	TIMEOUT_REG_PARITY_ERROR: The timeout select register parity is bad.
22	RWX_WCLEAR	CONFIG_REG_PARITY_ERROR: The slave configuration register parity is bad.
23	RWX_WCLEAR	UNUSED_1:
24	RWX_WCLEAR	DIV_REG_PARITY_ERROR: The divider register parity is bad.
25:28	RWX_WCLEAR	PLL_UNLOCK_ERROR: Unlock from the chiplet PLL.

Register Name	Hang Pulse Generation Register 0
Mnemonic	TP.TPCHIP.NET.PCBSLXB.HANG_PULSE_0_REG
Address	00000000060F0020 (SCOM)
Description	This register contains hang pulse 0 information.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_0: Value of hang pulse 0. Time period = 2^{value} x (precounter_reg + 1) / pcb_freq. 34 ≥ value > 0.
6	RW	SUPPRESS_HANG_0: If set to '1', hang pulses are suppressed in case of a checkstop.

Register Name	Hang Pulse Generation Register 1
Mnemonic	TP.TPCHIP.NET.PCBSLXB.HANG_PULSE_1_REG
Address	00000000060F0021 (SCOM)
Description	This register contains hang pulse 1 information.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_1: This field contains the value of hang pulse 1. The time period equals 2^{value} x (precounter_reg + 1) / pcb_freq. The range of valid values is 34 – 0.
6	RW	SUPPRESS_HANG_1: If set to '1', hang pulses are suppressed in case of a checkstop.

Register Name	Hang Pulse Generation Register 2
Mnemonic	TP.TPCHIP.NET.PCBSLXB.HANG_PULSE_2_REG
Address	00000000060F0022 (SCOM)
Description	This register contains hang pulse 2 information.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_2: This field contains the value of hang pulse 2. The time period equals 2^{value} x (precounter_reg + 1) / pcb_freq. The range of valid values is 34 – 0.
6	RW	SUPPRESS_HANG_2: If set to '1', hang pulses are suppressed in case of a checkstop.

Register Name	Hang Pulse Generation Register 3
Mnemonic	TP.TPCHIP.NET.PCBSLXB.HANG_PULSE_3_REG
Address	00000000060F0023 (SCOM)
Description	This register contains hang pulse 3 information.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_3: This field contains the value of hang pulse 3. The time period equals 2^{value} x (precounter_reg + 1) / pcb_freq. The range of valid values is 34 – 0.
6	RW	SUPPRESS_HANG_3: If set to '1', hang pulses are suppressed in case of a checkstop.

Register Name	Hang Pulse Generation Register 4
Mnemonic	TP.TPCHIP.NET.PCBSLXB.HANG_PULSE_4_REG
Address	00000000060F0024 (SCOM)
Description	This register contains hang pulse 4 information.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_4: This field contains the value of hang pulse 4. The time period equals 2^{value} x (precounter_reg + 1) / pcb_freq. The range of valid values is 34 – 0.
6	RW	SUPPRESS_HANG_4: If set to '1', hang pulses are suppressed in case of a checkstop.

Register Name	Hang Pulse Generation Register 5
Mnemonic	TP.TPCHIP.NET.PCBSLXB.HANG_PULSE_5_REG
Address	00000000060F0025 (SCOM)
Description	This register contains hang pulse 5 information. This hang counter is exclusively used to generate the malfunction alert pulse.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_5: This field contains the value of hang pulse 5. The time period equals 2^{value} x (precounter_reg + 1) / pcb_freq. The range of valid values is 34 – 0.
6	RW	SUPPRESS_HANG_5: If set to '1', hang pulses are suppressed in case of a checkstop.

Register Name	Hang Pulse Generation Register 6
Mnemonic	TP.TPCHIP.NET.PCBSLXB.HANG_PULSE_6_REG
Address	00000000060F0026 (SCOM)
Description	This register contains hang pulse 6 information. This hang counter is exclusively used for heartbeat generation.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_6: This field contains the value of hang pulse 6. The time period equals 2^{value} x (precounter_reg + 1) / pcb_freq. The range of valid values is 34 – 0.
6	RW	SUPPRESS_HANG_6: If set to '1', hang pulses are suppressed in case of a checkstop.

Register Name	Hang Counter Clock Divider Register
Mnemonic	TP.TPCHIP.NET.PCBSLXB.PRE_COUNTER_REG
Address	00000000060F0028 (SCOM)
Description	This register is the divider for the hang counter clock.

Bits	SCOM	Field Mnemonic: Description
0:7	RW	PRE_COUNTER: This field is the divider for the hang counter clock. It divides the clock by n + 1. (The default is n = 0).

Register Name	eDRAM Control Status Register
Mnemonic	TP.TPCHIP.NET.PCBSLXB.EDRAM_STATUS
Address	00000000060F0029 (SCOM)
Description	This register contains the eDRAM control status.

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	EDRAM_STAT: This field contains the eDRAM control status.

Register Name	NET CTRL0 Register (NA in PERV CPLT)
Mnemonic	TP.TPCHIP.NET.PCBSLXB.NET_CTRL0
Address	00000000060F0040 (SCOM) 00000000060F0041 (SCOM1) 00000000060F0042 (SCOM2)
Description	NET CTRL0 Register (NA in PERV CPLT)

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	CHIPLET_ENABLE: This bit is set if the chiplet is good.
1	RWX	RWX_WAND	RWX_WOR	PCB_EP_RESET: The output is ORed to the global EP reset.
2	RWX	RWX_WAND	RWX_WOR	CLK_ASYNC_RESET: POWER9 cache chiplet: EQ skew adjust reset. POWER9 core chiplet: Core duty cycle adjust reset. POWER9 memory chiplet: Memory glitchless multiplexer asynchronous reset.
3	RWX	RWX_WAND	RWX_WOR	PLL_TEST_EN: Test enable for chiplet PLL.
4	RWX	RWX_WAND	RWX_WOR	PLL_RESET: Reset for the chiplet PLL.
5	RWX	RWX_WAND	RWX_WOR	PLL_BYPASS: Enable bypass for the chiplet PLL.
6	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN: Scan control for the chiplet vital domain.
7	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN_IN: Scan in for the chiplet vital domain.
8	RWX	RWX_WAND	RWX_WOR	VITAL_PHASE: Phase for the vital domain.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
9	RWX	RWX_WAND	RWX_WOR	FLUSH_ALIGN_OVR: When set to 1, this mechanism overrides automatic control by the clock controller of the flush, flush_nto1, and align signals in the chiplet.
10	RWX	RWX_WAND	RWX_WOR	VITAL_AL: Align for vital domain.
11	RWX	RWX_WAND	RWX_WOR	ACT_DIS: ACT disable control for LCBs in the vital logic.
12	RWX	RWX_WAND	RWX_WOR	MPW1: Modify pulse width 1 (MPW1) control for LCBs in the vital logic.
13	RWX	RWX_WAND	RWX_WOR	MPW2: Modify pulse width 2 (MPW2) control for LCBs in the vital logic.
14	RWX	RWX_WAND	RWX_WOR	MPW3: Modify pulse width 3 (MPW3) control for LCBs in the vital logic.
15	RWX	RWX_WAND	RWX_WOR	DELAY_LCLKR: LCB control signal for vital logic.
16	RWX	RWX_WAND	RWX_WOR	VITAL_THOLD: Threshold for the chiplet vital domain.
17	RWX	RWX_WAND	RWX_WOR	FLUSH_SCAN_N: Flush scan control.
18	RWX	RWX_WAND	RWX_WOR	FENCE_EN: Fencing signal for chiplet.
19	RWX	RWX_WAND	RWX_WOR	CPLT_RCTRL: Chiplet receiver enable.
20	RWX	RWX_WAND	RWX_WOR	CPLT_DCTRL: Chiplet driver enable.
21	RWX	RWX_WAND	RWX_WOR	Reserved.
22	RWX	RWX_WAND	RWX_WOR	ADJ_FUNC_CLKSEL: POWER9 cache chiplet: Clock select for the skew adjust/duty cycle adjust logic. POWER9 core chiplet: Skew sense to skew adjust fencing.
23:24	RWX	RWX_WAND	RWX_WOR	Reserved.
25	RWX	RWX_WAND	RWX_WOR	TP_FENCE_PCB: Fence the chiplet from the PCB bus. If set, the PCB slave reports “Chiplet Offline.”
26	RWX	RWX_WAND	RWX_WOR	LVLTRANS_FENCE: Fence control for the level translators.
27	RWX	RWX_WAND	RWX_WOR	ARRAY_WRITE_ASSIST_EN: Array write assist.
28	RWX	RWX_WAND	RWX_WOR	HTB_INTEST: HTB intest mode.
29	RWX	RWX_WAND	RWX_WOR	HTB_EXTEST: HTB intest mode.
30	RWX	RWX_WAND	RWX_WOR	Reserved.
31	RWX	RWX_WAND	RWX_WOR	PLLFORCE_OUT_EN: PLL force out enable.

Register Name	NET CTRL1 Register
Mnemonic	TP.TPCHIP.NET.PCBSLXB.NET_CTRL1
Address	00000000060F0044 (SCOM) 00000000060F0045 (SCOM1) 00000000060F0046 (SCOM2)
Description	This register contains NET controls. It is not applicable to the pervasive chiplet.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	PLL_CLKIN_SEL: PLL clkin select.
1	RWX	RWX_WAND	RWX_WOR	CLK_DCC_BYPASS_EN: POWER9 cache chiplet: L2-0, L2-1, L3 duty cycle control bypass. POWER9 core chiplet: Core duty cycle control bypass. POWER9 memory chiplet: Memory duty cycle control bypass.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
2	RWX	RWX_WAND	RWX_WOR	CLK_PDLY_BYPASS_EN: POWER9 cache chiplet: L2-0, L2-1, L3 programmable delay bypass. POWER9 core chiplet: Core programmable delay bypass. POWER9 memory chiplet: Memory programmable delay bypass.
3	RWX	RWX_WAND	RWX_WOR	CLK_DIV_BYPASS_EN: Enable clock divider bypass.
4	RWX	RWX_WAND	RWX_WOR	REFCLK_CLKMUX0_SEL: Select for reference clock mux0.
5	RWX	RWX_WAND	RWX_WOR	REFCLK_CLKMUX1_SEL: Select for reference clock mux1.
6	RWX	RWX_WAND	RWX_WOR	PLL_BNDY_BYPASS_EN: Bypass for IOP PLL.
7	RWX	RWX_WAND	RWX_WOR	Reserved.
8:15	RWX	RWX_WAND	RWX_WOR	DPLL_TEST_SEL: DPLL testout MUXing.
16:19	RWX	RWX_WAND	RWX_WOR	SB_STRENGTH: Sector buffer driver strength.
20	RWX	RWX_WAND	RWX_WOR	ASYNC_TYPE: This is a control signal for testing latches with asynchronous set and reset capabilities.
21	RWX	RWX_WAND	RWX_WOR	ASYNC_OBS: This is a control signal for testing latches with asynchronous set and reset capabilities.
22	RWX	RWX_WAND	RWX_WOR	CPM_CAL_SET: CPM calibrate.
23	RWX	RWX_WAND	RWX_WOR	SENSEADJ_RESET0: POWER9 cache chiplet: L2-0 duty cycle adjust reset.
24	RWX	RWX_WAND	RWX_WOR	SENSEADJ_RESET1: POWER9 cache chiplet: L2-1 duty cycle adjust reset.
25	RWX	RWX_WAND	RWX_WOR	CLK_PULSE_EN: Clock pulse mode enable.
26:27	RWX	RWX_WAND	RWX_WOR	CLK_PULSE_MODE: Clock pulse mode setting.
28:31	RWX	RWX_WAND	RWX_WOR	Reserved.

Register Name	Protect Mode Register
Mnemonic	TP.TPCHIP.NET.PCBSLXB.PROTECT_MODE_REG
Address	00000000060F03FE (SCOM)
Description	This register is used to enable read and write protection.

Bits	SCOM	Field Mnemonic: Description
0	RW	READ_PROTECT_ENABLE: Enable read protection.
1	RW	WRITE_PROTECT_ENABLE: Enable write protection.

Register Name	Atomic Lock Register
Mnemonic	TP.TPCHIP.NET.PCBSLXB.ATOMIC_LOCK_REG
Address	00000000060F03FF (SCOM)
Description	This register contains atomic lock information.

Bits	SCOM	Field Mnemonic: Description
0	RW	ATOMIC_LOCK_ENABLE: Enable the atomic lock.
1:4	ROX	ATOMIC_ID: This field contains the atomic ID.
5:7	RO	constant = 000

Bits	SCOM	Field Mnemonic: Description
8:15	ROX	ATOMIC_ACTIVITY: This is the atomic lock counter.

4. XBUS Chiplet Indirect

The POWER9 processor registers are listed alphabetically by mnemonic in the following address table.

Mnemonic	Address	Page
IOF2.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.RX_FIR_ERROR_INJECT_PB	0x800F98000601143F	1180
IOF2.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.RX_FIR_MASK_PB	0x800F90000601143F	1180
IOF2.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.RX_FIR_PB	0x800F88000601143F	1180
IOF2.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.RX_FIR_RESET_PB	0x800F80000601143F	1179
IOF2.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.SPARE_MODE_PB	0x800F34000601143F	1178
IOF2.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.TX_IMPCAL2_PB	0x800F3C000601143F	1179
IOF2.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.TX_IMPCAL_NVAL_PB	0x800F0C000601143F	1176
IOF2.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.TX_IMPCAL_PB	0x800F04000601143F	1176
IOF2.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.TX_IMPCAL_PVAL_PB	0x800F14000601143F	1176
IOF2.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.TX_IMPCAL_P_4X_PB	0x800F1C000601143F	1177
IOF2.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.TX_IMPCAL_SWO1_PB	0x800F24000601143F	1177
IOF2.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.TX_IMPCAL_SWO2_PB	0x800F2C000601143F	1178
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL10_EO_PG	0x800920000601143F	1088
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL11_EO_PG	0x800928000601143F	1089
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL12_EO_PG	0x800930000601143F	1089
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL13_EO_PG	0x800938000601143F	1090
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL14_EO_PG	0x800940000601143F	1091
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL15_EO_PG	0x800948000601143F	1091
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL1_EO_PG	0x8008D8000601143F	1080
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL1_E_PG	0x8009F0000601143F	1110
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL2_EO_PG	0x8008E0000601143F	1082
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL3_EO_PG	0x8008E8000601143F	1083
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL4_EO_PG	0x8008F0000601143F	1084
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL4_E_PG	0x8009F8000601143F	1111
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL5_EO_PG	0x8008F8000601143F	1084
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL6_EO_PG	0x800900000601143F	1085
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL8_EO_PG	0x800910000601143F	1086
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL9_EO_PG	0x800918000601143F	1087
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTLX11_E_PG	0x800A30000601143F	1112
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTLX7_EO_PG	0x800908000601143F	1085
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE10_EO_PG	0x800858000601143F	1068
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE10_E_PG	0x8009D8000601143F	1108
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE11_EO_PG	0x800860000601143F	1068
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE11_E_PG	0x8009E0000601143F	1109
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE12_EO_PG	0x800868000601143F	1069
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE12_E_PG	0x8009E8000601143F	1109
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE13_EO_PG	0x800870000601143F	1070
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE14_EO_PG	0x800878000601143F	1071
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE15_EO_PG	0x800880000601143F	1071
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE16_EO_PG	0x800888000601143F	1072
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE17_EO_PG	0x800890000601143F	1073
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE18_EO_PG	0x800898000601143F	1073

Mnemonic	Address	Page
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE19_EO_PG	0x8008A0000601143F	1074
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE1_EO_PG	0x800810000601143F	1061
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE1_E_PG	0x800990000601143F	1097
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE20_EO_PG	0x8008A8000601143F	1074
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE21_EO_PG	0x8008B0000601143F	1075
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE22_EO_PG	0x8008B8000601143F	1076
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE23_EO_PG	0x8008C0000601143F	1078
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE24_EO_PG	0x8008C8000601143F	1079
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE26_EO_PG	0x800968000601143F	1094
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE27_EO_PG	0x800970000601143F	1095
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE28_EO_PG	0x800978000601143F	1096
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE29_EO_PG	0x8008D0000601143F	1080
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE2_EO_PG	0x800818000601143F	1061
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE2_E_PG	0x800998000601143F	1099
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE3_EO_PG	0x800820000601143F	1062
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE3_E_PG	0x8009A0000601143F	1100
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE4_EO_PG	0x800828000601143F	1063
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE4_E_PG	0x8009A8000601143F	1100
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE5_EO_PG	0x800830000601143F	1064
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE5_E_PG	0x8009B0000601143F	1101
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE6_EO_PG	0x800838000601143F	1065
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE6_E_PG	0x8009B8000601143F	1102
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE7_EO_PG	0x800840000601143F	1066
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE7_E_PG	0x8009C0000601143F	1102
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE8_EO_PG	0x800848000601143F	1067
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE8_E_PG	0x8009C8000601143F	1104
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE9_EO_PG	0x800850000601143F	1067
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE9_E_PG	0x8009D0000601143F	1106
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_STAT1_EO_PG	0x800950000601143F	1092
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_STAT1_E_PG	0x800A38000601143F	1113
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_STAT2_EO_PG	0x800958000601143F	1093
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_STAT2_E_PG	0x800A40000601143F	1114
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_STAT3_EO_PG	0x800960000601143F	1093
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_STAT4_E_PG	0x800A50000601143F	1114
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_STAT5_E_PG	0x800A58000601143F	1115
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_STAT6_E_PG	0x800A60000601143F	1116
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_STATX8_E_PG	0x800A68000601143F	1116
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_ID1_PG	0x800808000601143F	1060
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_ID2_PG	0x800980000601143F	1097
IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_SPARE_MODE_PG	0x800800000601143F	1059
IOF2.RX.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_CNTL1_E_PG	0x800BE8000601143F	1145
IOF2.RX.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_CNTLX1_EO_PG	0x800B88000601143F	1138
IOF2.RX.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_SPARE_MODE_PG	0x800B80000601143F	1137
IOF2.RX.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT10_EO_PG	0x800BD8000601143F	1144
IOF2.RX.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT11_EO_PG	0x800BE0000601143F	1144
IOF2.RX.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT12_EO_PG	0x800BF0000601143F	1146
IOF2.RX.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT13_E_PG	0x800BF8000601143F	1147
IOF2.RX.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT1_EO_PG	0x800B90000601143F	1139

Mnemonic	Address	Page
IOF2.RX.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT2_EO_PG	0x800B98000601143F	1140
IOF2.RX.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT3_EO_PG	0x800BA0000601143F	1140
IOF2.RX.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT4_EO_PG	0x800BA8000601143F	1141
IOF2.RX.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT5_EO_PG	0x800BB0000601143F	1141
IOF2.RX.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT6_EO_PG	0x800BB8000601143F	1142
IOF2.RX.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT7_EO_PG	0x800BC0000601143F	1142
IOF2.RX.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT8_EO_PG	0x800BC8000601143F	1143
IOF2.RX.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT9_EO_PG	0x800BD0000601143F	1143
IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_FIR1_ERROR_INJECT_PG	0x800A98000601143F	1120
IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_FIR1_MASK_PG	0x800A90000601143F	1119
IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_FIR1_PG	0x800A88000601143F	1118
IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_FIR2_ERROR_INJECT_PG	0x800B10000601143F	1132
IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_FIR2_MASK_PG	0x800B08000601143F	1131
IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_FIR2_PG	0x800B00000601143F	1130
IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_FIR_TRAINING_MASK_PG	0x800AA8000601143F	1123
IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_FIR_TRAINING_PG	0x800AA0000601143F	1121
IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_CNTL2_EO_PG	0x800AE0000601143F	1127
IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_CNTL3_EO_PG	0x800AE8000601143F	1128
IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_CNTL4_EO_PG	0x800AF0000601143F	1129
IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_CNTLX1_EO_PG	0x800AB0000601143F	1124
IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_MODE1_E_PG	0x800AF8000601143F	1130
IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_SPARE_MODE_PG	0x800A80000601143F	1117
IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_STAT10_E_PG	0x800B60000601143F	1137
IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_STAT1_EO_PG	0x800AB8000601143F	1124
IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_STAT1_E_PG	0x800B18000601143F	1132
IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_STAT2_EO_PG	0x800AC0000601143F	1125
IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_STAT2_E_PG	0x800B20000601143F	1133
IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_STAT3_EO_PG	0x800AC8000601143F	1125
IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_STAT3_E_PG	0x800B28000601143F	1134
IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_STAT4_EO_PG	0x800AD0000601143F	1126
IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_STAT4_E_PG	0x800B30000601143F	1134
IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_STAT5_EO_PG	0x800AD8000601143F	1127
IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_STAT7_E_PG	0x800B48000601143F	1135
IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_STAT8_E_PG	0x800B50000601143F	1135
IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_STAT9_E_PG	0x800B58000601143F	1136
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL	0x8003000D0601143F	765
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x8002480D0601143F	617
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL	0x8003080D0601143F	784
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x8002500D0601143F	637
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL	0x8003100D0601143F	796
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x8002580D0601143F	651
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x8002600D0601143F	665
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x8002400D0601143F	587

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IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x8002200D0601143F	540
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL	0x8002C00D0601143F	724
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x8002280D0601143F	557
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL	0x8002C80D0601143F	746
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x8002300D0601143F	568
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x8002680D0601143F	678
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x8002700D0601143F	695
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x8002780D0601143F	709
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x8002180D0601143F	526
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x8002100D0601143F	517
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_PL	0x8002080D0601143F	508
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x8002000D0601143F	495
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x8000080D0601143F	283
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL	0x8000800D0601143F	387
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x8000100D0601143F	301
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL	0x8000880D0601143F	399
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x8000180D0601143F	317
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL	0x8000900D0601143F	411
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x8000200D0601143F	329
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL	0x8000980D0601143F	423
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x8000280D0601143F	342
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL	0x8000A00D0601143F	435
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x8000300D0601143F	354
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL	0x8000A80D0601143F	447
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x8000380D0601143F	365
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL	0x8000B00D0601143F	459
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x8000400D0601143F	376

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IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL	0x8000B80D0601143F	470
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL	0x8000C00D0601143F	481
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x8000000D0601143F	267
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL	0x8003000F0601143F	767
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x8002480F0601143F	619
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL	0x8003080F0601143F	784
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x8002500F0601143F	638
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL	0x8003100F0601143F	797
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x8002580F0601143F	652
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x8002600F0601143F	665
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x8002400F0601143F	589
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x8002200F0601143F	541
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL	0x8002C00F0601143F	726
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x8002280F0601143F	558
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL	0x8002C80F0601143F	747
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x8002300F0601143F	568
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x8002680F0601143F	679
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x8002700F0601143F	696
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x8002780F0601143F	710
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x8002180F0601143F	527
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x8002100F0601143F	517
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_PL	0x8002080F0601143F	508
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x8002000F0601143F	495
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x8000080F0601143F	284
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL	0x8000800F0601143F	387
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x8000100F0601143F	302
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL	0x8000880F0601143F	399
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x8000180F0601143F	318
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL	0x8000900F0601143F	411

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IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x8000200F0601143F	330
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL	0x8000980F0601143F	423
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x8000280F0601143F	342
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL	0x8000A00F0601143F	435
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x8000300F0601143F	355
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL	0x8000A80F0601143F	447
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x8000380F0601143F	366
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL	0x8000B00F0601143F	459
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x8000400F0601143F	377
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL	0x8000B80F0601143F	470
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL	0x8000C00F0601143F	481
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x8000000F0601143F	268
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL	0x8003000E0601143F	766
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x8002480E0601143F	618
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL	0x8003080E0601143F	784
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x8002500E0601143F	638
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL	0x8003100E0601143F	796
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x8002580E0601143F	652
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x8002600E0601143F	665
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x8002400E0601143F	588
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x8002200E0601143F	541
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL	0x8002C00E0601143F	725
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x8002280E0601143F	558
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL	0x8002C80E0601143F	746
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x8002300E0601143F	568
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x8002680E0601143F	678
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x8002700E0601143F	695
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x8002780E0601143F	709

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IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x8002180E0601143F	526
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x8002100E0601143F	517
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_PL	0x8002080E0601143F	508
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x8002000E0601143F	495
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x8000080E0601143F	284
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL	0x8000800E0601143F	387
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x8000100E0601143F	302
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL	0x8000880E0601143F	399
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x8000180E0601143F	318
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL	0x8000900E0601143F	411
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x8000200E0601143F	330
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL	0x8000980E0601143F	423
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x8000280E0601143F	342
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL	0x8000A00E0601143F	435
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x8000300E0601143F	354
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL	0x8000A80E0601143F	447
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x8000380E0601143F	365
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL	0x8000B00E0601143F	459
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x8000400E0601143F	376
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL	0x8000B80E0601143F	470
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL	0x8000C00E0601143F	481
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x8000000E0601143F	267
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL	0x800300100601143F	767
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x800248100601143F	619
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL	0x800308100601143F	784
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x800250100601143F	638
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL	0x800310100601143F	797
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x800258100601143F	653
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x800260100601143F	666

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IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x800240100601143F	590
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x800220100601143F	542
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL	0x8002C0100601143F	726
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x800228100601143F	558
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL	0x8002C8100601143F	747
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x800230100601143F	569
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x800268100601143F	679
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x800270100601143F	696
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x800278100601143F	710
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x800218100601143F	527
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x800210100601143F	517
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_PL	0x800208100601143F	508
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x800200100601143F	496
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x800008100601143F	285
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL	0x800080100601143F	388
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x800010100601143F	303
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL	0x800088100601143F	400
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x800018100601143F	318
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL	0x800090100601143F	412
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x800020100601143F	330
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL	0x800098100601143F	424
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x800028100601143F	343
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL	0x8000A0100601143F	436
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x800030100601143F	355
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL	0x8000A8100601143F	448
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x800038100601143F	366
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL	0x8000B0100601143F	460

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IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x800040100601143F	377
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL	0x8000B8100601143F	471
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL	0x8000C0100601143F	482
IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x800000100601143F	268
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL	0x8003000B0601143F	764
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x8002480B0601143F	616
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL	0x8003080B0601143F	783
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x8002500B0601143F	637
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL	0x8003100B0601143F	795
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x8002580B0601143F	650
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x8002600B0601143F	664
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x8002400B0601143F	585
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x8002200B0601143F	539
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL	0x8002C00B0601143F	723
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x8002280B0601143F	557
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL	0x8002C80B0601143F	745
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x8002300B0601143F	567
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x8002680B0601143F	677
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x8002700B0601143F	694
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x8002780B0601143F	709
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x8002180B0601143F	525
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x8002100B0601143F	516
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_PL	0x8002080B0601143F	507
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x8002000B0601143F	494
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x8000080B0601143F	282
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL	0x8000800B0601143F	386
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x8000100B0601143F	300
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL	0x8000880B0601143F	398
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x8000180B0601143F	317

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IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL	0x8000900B0601143F	410
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x8000200B0601143F	329
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL	0x8000980B0601143F	422
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x8000280B0601143F	341
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL	0x8000A00B0601143F	434
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x8000300B0601143F	353
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL	0x8000A80B0601143F	446
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x8000380B0601143F	364
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL	0x8000B00B0601143F	458
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x8000400B0601143F	376
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL	0x8000B80B0601143F	469
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL	0x8000C00B0601143F	480
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x8000000B0601143F	266
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL	0x800300090601143F	763
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x800248090601143F	615
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL	0x800308090601143F	782
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x800250090601143F	636
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL	0x800310090601143F	794
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x800258090601143F	650
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x800260090601143F	664
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x800240090601143F	583
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x800220090601143F	538
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL	0x8002C0090601143F	722
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x800228090601143F	556
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL	0x8002C8090601143F	744
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x800230090601143F	566
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x800268090601143F	676
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x800270090601143F	693

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IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x800278090601143F	708
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x800218090601143F	525
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x800210090601143F	516
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_PL	0x800208090601143F	507
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x800200090601143F	493
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x800008090601143F	281
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL	0x800080090601143F	385
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x800010090601143F	299
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL	0x800088090601143F	397
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x800018090601143F	316
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL	0x800090090601143F	409
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x800020090601143F	328
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL	0x800098090601143F	421
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x800028090601143F	340
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL	0x8000A0090601143F	433
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x800030090601143F	353
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL	0x8000A8090601143F	445
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x800038090601143F	364
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL	0x8000B0090601143F	457
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x800040090601143F	375
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL	0x8000B8090601143F	469
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL	0x8000C0090601143F	479
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x800000090601143F	265
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL	0x8003000C0601143F	765
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x8002480C0601143F	617
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL	0x8003080C0601143F	783
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x8002500C0601143F	637
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL	0x8003100C0601143F	796
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x8002580C0601143F	651

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IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x8002600C0601143F	665
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x8002400C0601143F	586
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x8002200C0601143F	539
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL	0x8002C00C0601143F	724
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x8002280C0601143F	557
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL	0x8002C80C0601143F	745
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x8002300C0601143F	567
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x8002680C0601143F	677
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x8002700C0601143F	695
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x8002780C0601143F	709
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x8002180C0601143F	526
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x8002100C0601143F	516
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_PL	0x8002080C0601143F	507
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x8002000C0601143F	494
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x8000080C0601143F	283
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL	0x8000800C0601143F	386
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x8000100C0601143F	301
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL	0x8000880C0601143F	398
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x8000180C0601143F	317
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL	0x8000900C0601143F	410
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x8000200C0601143F	329
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL	0x8000980C0601143F	422
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x8000280C0601143F	341
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL	0x8000A00C0601143F	434
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x8000300C0601143F	354
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL	0x8000A80C0601143F	446
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x8000380C0601143F	365

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IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL	0x8000B00C0601143F	458
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x8000400C0601143F	376
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL	0x8000B80C0601143F	470
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL	0x8000C00C0601143F	480
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x8000000C0601143F	266
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL	0x8003000A0601143F	764
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x8002480A0601143F	615
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL	0x8003080A0601143F	783
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x8002500A0601143F	636
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL	0x8003100A0601143F	795
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x8002580A0601143F	650
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x8002600A0601143F	664
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x8002400A0601143F	584
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x8002200A0601143F	538
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL	0x8002C00A0601143F	722
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x8002280A0601143F	557
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL	0x8002C80A0601143F	744
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x8002300A0601143F	567
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x8002680A0601143F	676
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x8002700A0601143F	694
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x8002780A0601143F	708
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x8002180A0601143F	525
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x8002100A0601143F	516
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_PL	0x8002080A0601143F	507
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x8002000A0601143F	493
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x8000080A0601143F	282
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL	0x8000800A0601143F	386
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x8000100A0601143F	300
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL	0x8000880A0601143F	398

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IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x8000180A0601143F	316
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL	0x8000900A0601143F	410
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x8000200A0601143F	328
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL	0x8000980A0601143F	422
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x8000280A0601143F	341
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL	0x8000A00A0601143F	434
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x8000300A0601143F	353
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL	0x8000A80A0601143F	446
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x8000380A0601143F	364
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL	0x8000B00A0601143F	458
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x8000400A0601143F	375
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL	0x8000B80A0601143F	469
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL	0x8000C00A0601143F	480
IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x8000000A0601143F	265
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL	0x800300070601143F	762
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x800248070601143F	613
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL	0x800308070601143F	782
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x800250070601143F	635
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL	0x800310070601143F	793
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x800258070601143F	649
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x800260070601143F	663
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x800240070601143F	582
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x800220070601143F	536
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL	0x8002C0070601143F	720
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x800228070601143F	556
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL	0x8002C8070601143F	743
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x800230070601143F	566
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x800268070601143F	675

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IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x800270070601143F	692
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x800278070601143F	707
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x800218070601143F	524
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x800210070601143F	515
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_PL	0x800208070601143F	506
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x800200070601143F	492
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x800008070601143F	280
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL	0x800080070601143F	385
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x800010070601143F	298
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL	0x800088070601143F	397
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x800018070601143F	315
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL	0x800090070601143F	409
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x800020070601143F	327
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL	0x800098070601143F	421
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x800028070601143F	339
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL	0x8000A0070601143F	433
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x800030070601143F	352
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL	0x8000A8070601143F	445
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x800038070601143F	363
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL	0x8000B0070601143F	457
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x800040070601143F	374
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL	0x8000B8070601143F	468
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL	0x8000C0070601143F	479
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x800000070601143F	264
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL	0x800300110601143F	768
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x800248110601143F	620
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL	0x800308110601143F	785
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x800250110601143F	639
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL	0x800310110601143F	798

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IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x800258110601143F	653
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x800260110601143F	666
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x800240110601143F	591
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x800220110601143F	542
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL	0x8002C0110601143F	727
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x800228110601143F	558
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL	0x8002C8110601143F	748
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x800230110601143F	569
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x800268110601143F	680
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x800270110601143F	697
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x800278110601143F	710
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x800218110601143F	527
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x800210110601143F	518
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_PL	0x800208110601143F	509
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x800200110601143F	496
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x800008110601143F	285
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL	0x800080110601143F	388
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x800010110601143F	303
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL	0x800088110601143F	400
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x800018110601143F	319
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL	0x800090110601143F	412
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x800020110601143F	331
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL	0x800098110601143F	424
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x800028110601143F	343
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL	0x8000A0110601143F	436
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x800030110601143F	355
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL	0x8000A8110601143F	448

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IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x800038110601143F	366
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL	0x8000B0110601143F	460
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x800040110601143F	377
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL	0x8000B8110601143F	471
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL	0x8000C0110601143F	482
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x800000110601143F	269
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL	0x800300060601143F	761
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x800248060601143F	613
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL	0x800308060601143F	782
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x800250060601143F	635
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL	0x800310060601143F	793
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x800258060601143F	648
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x800260060601143F	663
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x800240060601143F	581
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x800220060601143F	536
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL	0x8002C0060601143F	720
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x800228060601143F	555
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL	0x8002C8060601143F	742
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x800230060601143F	565
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x800268060601143F	674
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x800270060601143F	692
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x800278060601143F	707
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x800218060601143F	524
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x800210060601143F	515
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_PL	0x800208060601143F	506
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x800200060601143F	492
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x800008060601143F	280
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL	0x800080060601143F	384
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x800010060601143F	298

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IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL	0x800088060601143F	396
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x800018060601143F	315
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL	0x800090060601143F	408
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x800020060601143F	327
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL	0x800098060601143F	420
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x800028060601143F	339
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL	0x8000A0060601143F	432
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x800030060601143F	352
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL	0x8000A8060601143F	444
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x800038060601143F	363
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL	0x8000B0060601143F	456
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x800040060601143F	374
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL	0x8000B8060601143F	468
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL	0x8000C0060601143F	478
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x800000060601143F	264
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL	0x800300080601143F	762
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x800248080601143F	614
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL	0x800308080601143F	782
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IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL	0x800310080601143F	794
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x800258080601143F	649
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x800260080601143F	663
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x800240080601143F	583
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x800220080601143F	537
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL	0x8002C0080601143F	721
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x800228080601143F	556
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL	0x8002C8080601143F	743
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x800230080601143F	566

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IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x800268080601143F	675
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x800270080601143F	693
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x800278080601143F	708
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x800218080601143F	525
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x800210080601143F	515
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_PL	0x800208080601143F	506
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x800200080601143F	492
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x800008080601143F	281
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL	0x800080080601143F	385
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x800010080601143F	299
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL	0x800088080601143F	397
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x800018080601143F	316
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL	0x800090080601143F	409
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x800020080601143F	328
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL	0x800098080601143F	421
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x800028080601143F	340
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL	0x8000A0080601143F	433
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x800030080601143F	353
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL	0x8000A8080601143F	445
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x800038080601143F	363
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL	0x8000B0080601143F	457
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x800040080601143F	375
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL	0x8000B8080601143F	468
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL	0x8000C0080601143F	479
IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x800000080601143F	265
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL	0x800300040601143F	760
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x800248040601143F	611
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL	0x800308040601143F	781

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IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x800250040601143F	634
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL	0x800310040601143F	792
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x800258040601143F	647
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x800260040601143F	662
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x800240040601143F	579
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x800220040601143F	535
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL	0x8002C0040601143F	718
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x800228040601143F	555
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL	0x8002C8040601143F	741
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x800230040601143F	565
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x800268040601143F	673
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IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x800278040601143F	707
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x800218040601143F	524
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x800210040601143F	514
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IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x800200040601143F	491
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IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x800010040601143F	297
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL	0x800088040601143F	396
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x800018040601143F	314
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL	0x800090040601143F	408
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x800020040601143F	326
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL	0x800098040601143F	420
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x800028040601143F	338
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL	0x8000A0040601143F	432
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x800030040601143F	351

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IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL	0x8000A8040601143F	444
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IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL	0x8000B0040601143F	456
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x800040040601143F	374
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL	0x8000B8040601143F	467
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL	0x8000C0040601143F	478
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x800000040601143F	263
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL	0x800300020601143F	759
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x800248020601143F	610
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL	0x800308020601143F	780
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x800250020601143F	633
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL	0x800310020601143F	791
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x800258020601143F	647
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x800260020601143F	662
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x800240020601143F	577
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x800220020601143F	533
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL	0x8002C0020601143F	717
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x800228020601143F	554
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL	0x8002C8020601143F	740
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x800230020601143F	564
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x800268020601143F	672
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x800270020601143F	690
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x800278020601143F	706
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x800218020601143F	523
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x800210020601143F	514
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_PL	0x800208020601143F	505
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x800200020601143F	490
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x800008020601143F	278
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL	0x800080020601143F	383

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IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x800010020601143F	296
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL	0x800088020601143F	395
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x800018020601143F	314
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL	0x800090020601143F	407
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x800020020601143F	326
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL	0x800098020601143F	419
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x800028020601143F	338
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL	0x8000A0020601143F	431
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x800030020601143F	351
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL	0x8000A8020601143F	443
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x800038020601143F	361
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL	0x8000B0020601143F	455
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x800040020601143F	373
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL	0x8000B8020601143F	467
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL	0x8000C0020601143F	477
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x800000020601143F	262
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL	0x800300050601143F	760
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x800248050601143F	612
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL	0x800308050601143F	781
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x800250050601143F	634
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL	0x800310050601143F	792
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x800258050601143F	648
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x800260050601143F	663
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x800240050601143F	580
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x800220050601143F	535
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL	0x8002C0050601143F	719
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x800228050601143F	555
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL	0x8002C8050601143F	742

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IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x800230050601143F	565
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x800268050601143F	674
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x800270050601143F	691
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x800278050601143F	707
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x800218050601143F	524
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x800210050601143F	515
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_PL	0x800208050601143F	506
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x800200050601143F	491
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x800008050601143F	279
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL	0x800080050601143F	384
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x800010050601143F	297
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL	0x800088050601143F	396
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x800018050601143F	315
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL	0x800090050601143F	408
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x800020050601143F	327
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL	0x800098050601143F	420
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x800028050601143F	339
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL	0x8000A0050601143F	432
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x800030050601143F	352
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL	0x8000A8050601143F	444
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x800038050601143F	362
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL	0x8000B0050601143F	456
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x800040050601143F	374
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL	0x8000B8050601143F	468
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL	0x8000C0050601143F	478
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x800000050601143F	263
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL	0x800300030601143F	759
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x800248030601143F	611

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IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL	0x800308030601143F	781
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x800250030601143F	634
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL	0x800310030601143F	791
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x800258030601143F	647
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x800260030601143F	662
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x800240030601143F	578
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x800220030601143F	534
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL	0x8002C0030601143F	718
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x800228030601143F	555
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL	0x8002C8030601143F	741
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x800230030601143F	564
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x800268030601143F	673
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x800270030601143F	690
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x800278030601143F	706
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x800218030601143F	523
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x800210030601143F	514
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_PL	0x800208030601143F	505
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x800200030601143F	490
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x800008030601143F	278
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL	0x800080030601143F	383
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x800010030601143F	296
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL	0x800088030601143F	395
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x800018030601143F	314
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL	0x800090030601143F	407
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x800020030601143F	326
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL	0x800098030601143F	419
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x800028030601143F	338
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL	0x8000A0030601143F	431

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IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x800030030601143F	351
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL	0x8000A8030601143F	443
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x800038030601143F	362
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL	0x8000B0030601143F	455
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x800040030601143F	373
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL	0x8000B8030601143F	467
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL	0x8000C0030601143F	477
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x800000030601143F	262
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL	0x800300000601143F	757
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x800248000601143F	609
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL	0x800308000601143F	780
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x800250000601143F	633
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL	0x800310000601143F	790
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x800258000601143F	646
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x800260000601143F	661
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x800240000601143F	575
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x800220000601143F	532
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL	0x8002C0000601143F	716
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x800228000601143F	554
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL	0x8002C8000601143F	740
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x800230000601143F	563
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x800268000601143F	671
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x800270000601143F	689
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x800278000601143F	705
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x800218000601143F	522
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x800210000601143F	513
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_FIR_PL	0x800208000601143F	504
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x800200000601143F	489
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x800008000601143F	277

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IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL	0x800080000601143F	382
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x800010000601143F	295
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL	0x800088000601143F	394
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x800018000601143F	313
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL	0x800090000601143F	406
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x800020000601143F	325
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL	0x800098000601143F	418
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x800028000601143F	337
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL	0x8000A0000601143F	430
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x800030000601143F	350
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL	0x8000A8000601143F	442
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x800038000601143F	361
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL	0x8000B0000601143F	454
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x800040000601143F	373
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL	0x8000B8000601143F	466
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL	0x8000C0000601143F	476
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x800000000601143F	261
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL	0x800300010601143F	758
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x800248010601143F	609
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL	0x800308010601143F	780
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x800250010601143F	633
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL	0x800310010601143F	791
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x800258010601143F	646
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x800260010601143F	661
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x800240010601143F	576
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x800220010601143F	533
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL	0x8002C0010601143F	716
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x800228010601143F	554

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IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x800268010601143F	672
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x800270010601143F	690
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x800278010601143F	706
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x800218010601143F	523
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x800210010601143F	514
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IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x800010010601143F	295
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IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x800020010601143F	325
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL	0x800098010601143F	419
IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x800028010601143F	337
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IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x800030010601143F	351
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IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL	0x8000B0010601143F	455
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IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#0.RX_WORK_REGS.RX_WORK_STAT2_EO_PL	0x8003900D0601143F	880
IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#0.RX_WORK_REGS.RX_WORK_STAT3_EO_PL	0x8003980D0601143F	898
IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#1.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL	0x8003800F0601143F	813
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IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#10.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL	0x800380060601143F	809
IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#10.RX_WORK_REGS.RX_WORK_STAT1_EO_PL	0x800388060601143F	833
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IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#11.RX_WORK_REGS.RX_WORK_STAT2_EO_PL	0x800390080601143F	878
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IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#13.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL	0x800380020601143F	807
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IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#16.RX_WORK_REGS.RX_WORK_STAT3_EO_PL	0x800398000601143F	894
IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#17.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL	0x800380010601143F	807
IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#17.RX_WORK_REGS.RX_WORK_STAT1_EO_PL	0x800388010601143F	829
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IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#2.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL	0x8003800E0601143F	813
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IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#2.RX_WORK_REGS.RX_WORK_STAT3_EO_PL	0x8003980E0601143F	898
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IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#23.RX_WORK_REGS.RX_WORK_STAT2_EO_PL	0x800390170601143F	884
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IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL15_EO_PG	0x800948200601143F	1092
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL1_EO_PG	0x8008D8200601143F	1081
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL1_E_PG	0x8009F0200601143F	1110
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL2_EO_PG	0x8008E0200601143F	1083
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL3_EO_PG	0x8008E8200601143F	1084
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL4_EO_PG	0x8008F0200601143F	1084
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL4_E_PG	0x8009F8200601143F	1111
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL5_EO_PG	0x8008F8200601143F	1085
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL6_EO_PG	0x800900200601143F	1085
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL8_EO_PG	0x800910200601143F	1086
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL9_EO_PG	0x800918200601143F	1087
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTLX11_E_PG	0x800A30200601143F	1112
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTLX7_EO_PG	0x800908200601143F	1086
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE10_EO_PG	0x800858200601143F	1068
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE10_E_PG	0x8009D8200601143F	1108
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE11_EO_PG	0x800860200601143F	1069

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IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE12_EO_PG	0x800868200601143F	1070
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE12_E_PG	0x8009E8200601143F	1109
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE13_EO_PG	0x800870200601143F	1070
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE14_EO_PG	0x800878200601143F	1071
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE15_EO_PG	0x800880200601143F	1072
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE16_EO_PG	0x800888200601143F	1072
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE17_EO_PG	0x800890200601143F	1073
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IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE19_EO_PG	0x8008A0200601143F	1074
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE1_EO_PG	0x800810200601143F	1061
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE1_E_PG	0x800990200601143F	1098
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE20_EO_PG	0x8008A8200601143F	1075
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE21_EO_PG	0x8008B0200601143F	1076
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE22_EO_PG	0x8008B8200601143F	1077
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE23_EO_PG	0x8008C0200601143F	1078
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE24_EO_PG	0x8008C8200601143F	1079
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE26_EO_PG	0x800968200601143F	1094
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE27_EO_PG	0x800970200601143F	1095
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE28_EO_PG	0x800978200601143F	1096
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE29_EO_PG	0x8008D0200601143F	1080
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE2_EO_PG	0x800818200601143F	1062
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE2_E_PG	0x800998200601143F	1099
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE3_EO_PG	0x800820200601143F	1063
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE3_E_PG	0x8009A0200601143F	1100
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE4_EO_PG	0x800828200601143F	1063
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE4_E_PG	0x8009A8200601143F	1101
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IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE5_E_PG	0x8009B0200601143F	1101
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE6_EO_PG	0x800838200601143F	1065
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE6_E_PG	0x8009B8200601143F	1102
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE7_EO_PG	0x800840200601143F	1066
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE7_E_PG	0x8009C0200601143F	1103
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IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE8_E_PG	0x8009C8200601143F	1105
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE9_EO_PG	0x800850200601143F	1067
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE9_E_PG	0x8009D0200601143F	1107
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_STAT1_EO_PG	0x800950200601143F	1092
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IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_STAT4_E_PG	0x800A50200601143F	1115
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_STAT5_E_PG	0x800A58200601143F	1115
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IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_STATX8_E_PG	0x800A68200601143F	1117
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_ID1_PG	0x800808200601143F	1060
IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_ID2_PG	0x800980200601143F	1097

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IOF2.RX.RX1.RXCTL.DATASM.DATASM_REGS.RX_DATASM_CNTL1_E_PG	0x800BE8200601143F	1145
IOF2.RX.RX1.RXCTL.DATASM.DATASM_REGS.RX_DATASM_CNTLX1_EO_PG	0x800B88200601143F	1139
IOF2.RX.RX1.RXCTL.DATASM.DATASM_REGS.RX_DATASM_SPARE_MODE_PG	0x800B80200601143F	1138
IOF2.RX.RX1.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT10_EO_PG	0x800BD8200601143F	1144
IOF2.RX.RX1.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT11_EO_PG	0x800BE0200601143F	1145
IOF2.RX.RX1.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT12_EO_PG	0x800BF0200601143F	1146
IOF2.RX.RX1.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT13_E_PG	0x800BF8200601143F	1147
IOF2.RX.RX1.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT1_EO_PG	0x800B90200601143F	1140
IOF2.RX.RX1.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT2_EO_PG	0x800B98200601143F	1140
IOF2.RX.RX1.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT3_EO_PG	0x800BA0200601143F	1141
IOF2.RX.RX1.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT4_EO_PG	0x800BA8200601143F	1141
IOF2.RX.RX1.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT5_EO_PG	0x800BB0200601143F	1141
IOF2.RX.RX1.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT6_EO_PG	0x800BB8200601143F	1142
IOF2.RX.RX1.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT7_EO_PG	0x800BC0200601143F	1143
IOF2.RX.RX1.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT8_EO_PG	0x800BC8200601143F	1143
IOF2.RX.RX1.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT9_EO_PG	0x800BD0200601143F	1144
IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_FIR1_ERROR_INJECT_PG	0x800A98200601143F	1121
IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_FIR1_MASK_PG	0x800A90200601143F	1120
IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_FIR1_PG	0x800A88200601143F	1119
IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_FIR2_ERROR_INJECT_PG	0x800B10200601143F	1132
IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_FIR2_MASK_PG	0x800B08200601143F	1132
IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_FIR2_PG	0x800B00200601143F	1131
IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_FIR_TRAINING_MASK_PG	0x800AA8200601143F	1123
IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_FIR_TRAINING_PG	0x800AA0200601143F	1122
IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_GLBSM_CNTL2_EO_PG	0x800AE0200601143F	1128
IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_GLBSM_CNTL3_EO_PG	0x800AE8200601143F	1129
IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_GLBSM_CNTL4_EO_PG	0x800AF0200601143F	1129
IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_GLBSM_CNTLX1_EO_PG	0x800AB0200601143F	1124
IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_GLBSM_MODE1_E_PG	0x800AF8200601143F	1130
IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_GLBSM_SPARE_MODE_PG	0x800A80200601143F	1118
IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_GLBSM_STAT10_E_PG	0x800B60200601143F	1137
IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_GLBSM_STAT1_EO_PG	0x800AB8200601143F	1125
IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_GLBSM_STAT1_E_PG	0x800B18200601143F	1133
IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_GLBSM_STAT2_EO_PG	0x800AC0200601143F	1125
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IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_GLBSM_STAT3_E_PG	0x800B28200601143F	1134
IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_GLBSM_STAT4_EO_PG	0x800AD0200601143F	1126
IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_GLBSM_STAT4_E_PG	0x800B30200601143F	1134
IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_GLBSM_STAT5_EO_PG	0x800AD8200601143F	1127
IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_GLBSM_STAT7_E_PG	0x800B48200601143F	1135
IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_GLBSM_STAT8_E_PG	0x800B50200601143F	1136
IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_GLBSM_STAT9_E_PG	0x800B58200601143F	1136
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL	0x800300210601143F	769
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x800248210601143F	621
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL	0x800308210601143F	785

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IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL	0x800310210601143F	799
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x800258210601143F	654
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x800260210601143F	667
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x800240210601143F	592
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x800220210601143F	544
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL	0x8002C0210601143F	728
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x800228210601143F	559
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL	0x8002C8210601143F	749
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x800230210601143F	570
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x800268210601143F	681
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x800270210601143F	698
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x800278210601143F	711
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x800218210601143F	528
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x800210210601143F	518
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_PL	0x800208210601143F	509
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x800200210601143F	497
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x800008210601143F	286
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL	0x800080210601143F	389
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x800010210601143F	304
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL	0x800088210601143F	401
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x800018210601143F	319
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL	0x800090210601143F	413
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x800020210601143F	331
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL	0x800098210601143F	425
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x800028210601143F	344
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL	0x8000A0210601143F	437
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x800030210601143F	356

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IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x800038210601143F	367
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL	0x8000B0210601143F	461
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x800040210601143F	378
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL	0x8000B8210601143F	471
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL	0x8000C0210601143F	483
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x800000210601143F	269
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL	0x800300230601143F	770
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x800248230601143F	623
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL	0x800308230601143F	786
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x800250230601143F	640
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL	0x800310230601143F	800
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x800258230601143F	655
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x800260230601143F	667
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x800240230601143F	594
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x800220230601143F	545
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL	0x8002C0230601143F	730
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x800228230601143F	559
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL	0x8002C8230601143F	750
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x800230230601143F	570
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x800268230601143F	682
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x800270230601143F	699
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x800278230601143F	711
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x800218230601143F	528
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x800210230601143F	519
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_PL	0x800208230601143F	510
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x800200230601143F	498
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x800008230601143F	287
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL	0x800080230601143F	389

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IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x800010230601143F	305
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL	0x800088230601143F	401
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x800018230601143F	320
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL	0x800090230601143F	413
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x800020230601143F	332
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL	0x800098230601143F	425
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x800028230601143F	345
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL	0x8000A0230601143F	437
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x800030230601143F	356
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL	0x8000A8230601143F	449
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x800038230601143F	368
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL	0x8000B0230601143F	461
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x800040230601143F	378
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL	0x8000B8230601143F	472
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL	0x8000C0230601143F	484
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x800000230601143F	270
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL	0x800300200601143F	769
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x800248200601143F	621
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL	0x800308200601143F	785
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x800250200601143F	639
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL	0x800310200601143F	798
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x800258200601143F	653
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x800260200601143F	666
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x800240200601143F	591
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x800220200601143F	543
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL	0x8002C0200601143F	728
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x800228200601143F	559
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL	0x8002C8200601143F	748

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IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x800230200601143F	569
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x800268200601143F	680
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x800270200601143F	697
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x800278200601143F	711
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x800218200601143F	527
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x800210200601143F	518
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_PL	0x800208200601143F	509
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x800200200601143F	497
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x800008200601143F	286
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL	0x800080200601143F	388
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x800010200601143F	304
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL	0x800088200601143F	400
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x800018200601143F	319
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL	0x800090200601143F	412
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x800020200601143F	331
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL	0x800098200601143F	424
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x800028200601143F	344
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL	0x8000A0200601143F	436
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IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL	0x8000A8200601143F	448
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IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL	0x8000B0200601143F	460
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IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL	0x8000B8200601143F	471
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL	0x8000C0200601143F	483
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x800000200601143F	269
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL	0x800300220601143F	770
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x800248220601143F	622

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IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL	0x800308220601143F	786
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x800250220601143F	640
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL	0x800310220601143F	799
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x800258220601143F	654
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IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x800240220601143F	593
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x800220220601143F	544
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL	0x8002C0220601143F	729
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x800228220601143F	559
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL	0x8002C8220601143F	749
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x800230220601143F	570
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IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x800278220601143F	711
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x800218220601143F	528
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x800210220601143F	518
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_PL	0x800208220601143F	509
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x800200220601143F	498
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x800008220601143F	287
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL	0x800080220601143F	389
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x800010220601143F	305
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL	0x800088220601143F	401
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x800018220601143F	320
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL	0x800090220601143F	413
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x800020220601143F	332
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL	0x800098220601143F	425
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IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x800030220601143F	356
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IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x800038220601143F	367
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IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x800040220601143F	378
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL	0x8000B8220601143F	472
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL	0x8000C0220601143F	483
IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x800000220601143F	270
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL	0x800300270601143F	773
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x800248270601143F	625
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL	0x800308270601143F	787
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x800250270601143F	642
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL	0x800310270601143F	801
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x800258270601143F	656
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x800260270601143F	668
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x800240270601143F	598
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x800220270601143F	547
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL	0x8002C0270601143F	732
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x800228270601143F	561
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL	0x8002C8270601143F	752
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x800230270601143F	572
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x800268270601143F	684
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x800270270601143F	700
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x800278270601143F	713
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x800218270601143F	529
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x800210270601143F	520
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_PL	0x800208270601143F	511
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x800200270601143F	500
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x800008270601143F	289

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IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL	0x800080270601143F	391
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x800010270601143F	307
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL	0x800088270601143F	403
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x800018270601143F	321
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL	0x800090270601143F	415
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x800020270601143F	333
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL	0x800098270601143F	427
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x800028270601143F	346
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL	0x8000A0270601143F	439
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x800030270601143F	357
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL	0x8000A8270601143F	451
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x800038270601143F	369
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL	0x8000B0270601143F	463
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x800040270601143F	379
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL	0x8000B8270601143F	473
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL	0x8000C0270601143F	485
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x800000270601143F	272
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL	0x800300250601143F	772
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x800248250601143F	624
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL	0x800308250601143F	786
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x800250250601143F	641
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL	0x800310250601143F	801
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x800258250601143F	656
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x800260250601143F	668
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x800240250601143F	596
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x800220250601143F	546
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL	0x8002C0250601143F	731
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x800228250601143F	560

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IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL	0x8002C8250601143F	751
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x800230250601143F	571
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x800268250601143F	683
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x800270250601143F	700
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x800278250601143F	712
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x800218250601143F	529
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x800210250601143F	519
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_PL	0x800208250601143F	510
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x800200250601143F	499
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x800008250601143F	288
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL	0x800080250601143F	390
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x800010250601143F	306
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL	0x800088250601143F	402
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x800018250601143F	321
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL	0x800090250601143F	414
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x800020250601143F	333
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL	0x800098250601143F	426
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x800028250601143F	345
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL	0x8000A0250601143F	438
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x800030250601143F	357
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL	0x8000A8250601143F	450
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x800038250601143F	368
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL	0x8000B0250601143F	462
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x800040250601143F	379
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL	0x8000B8250601143F	473
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL	0x8000C0250601143F	484
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x800000250601143F	271
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL	0x800300260601143F	772

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IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x800248260601143F	625
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL	0x800308260601143F	787
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x800250260601143F	641
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL	0x800310260601143F	801
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x800258260601143F	656
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x800260260601143F	668
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x800240260601143F	597
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x800220260601143F	547
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL	0x8002C0260601143F	732
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x800228260601143F	560
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL	0x8002C8260601143F	751
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x800230260601143F	571
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x800268260601143F	683
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x800270260601143F	700
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x800278260601143F	712
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x800218260601143F	529
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x800210260601143F	519
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_PL	0x800208260601143F	510
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x800200260601143F	499
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x800008260601143F	289
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL	0x800080260601143F	390
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x800010260601143F	307
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL	0x800088260601143F	402
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x800018260601143F	321
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL	0x800090260601143F	414
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x800020260601143F	333
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL	0x800098260601143F	426
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x800028260601143F	346

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IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL	0x8000A0260601143F	438
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x800030260601143F	357
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL	0x8000A8260601143F	450
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x800038260601143F	369
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL	0x8000B0260601143F	462
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x800040260601143F	379
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL	0x8000B8260601143F	473
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL	0x8000C0260601143F	485
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x800000260601143F	272
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL	0x800300240601143F	771
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x800248240601143F	623
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL	0x800308240601143F	786
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x800250240601143F	641
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL	0x800310240601143F	800
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x800258240601143F	655
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x800260240601143F	667
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x800240240601143F	595
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x800220240601143F	545
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL	0x8002C0240601143F	730
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x800228240601143F	560
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL	0x8002C8240601143F	750
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x800230240601143F	571
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x800268240601143F	682
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x800270240601143F	699
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x800278240601143F	712
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x800218240601143F	528
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x800210240601143F	519
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_PL	0x800208240601143F	510
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x800200240601143F	498

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IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x800008240601143F	288
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL	0x800080240601143F	390
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x800010240601143F	306
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL	0x800088240601143F	402
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x800018240601143F	320
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL	0x800090240601143F	414
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x800020240601143F	332
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL	0x800098240601143F	426
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x800028240601143F	345
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL	0x8000A0240601143F	438
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x800030240601143F	357
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL	0x8000A8240601143F	450
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x800038240601143F	368
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL	0x8000B0240601143F	462
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x800040240601143F	379
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL	0x8000B8240601143F	472
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL	0x8000C0240601143F	484
IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x800000240601143F	271
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL	0x800300280601143F	774
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x800248280601143F	626
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL	0x800308280601143F	787
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x800250280601143F	642
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL	0x800310280601143F	802
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x800258280601143F	657
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x800260280601143F	669
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x800240280601143F	599
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x800220280601143F	548
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL	0x8002C0280601143F	733

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IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x800228280601143F	561
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL	0x8002C8280601143F	752
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x800230280601143F	572
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x800268280601143F	684
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x800270280601143F	701
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x800278280601143F	713
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x800218280601143F	530
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x800210280601143F	520
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_PL	0x800208280601143F	511
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x800200280601143F	500
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x800008280601143F	290
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL	0x800080280601143F	391
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x800010280601143F	308
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL	0x800088280601143F	403
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x800018280601143F	322
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL	0x800090280601143F	415
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x800020280601143F	334
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL	0x800098280601143F	427
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x800028280601143F	347
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL	0x8000A0280601143F	439
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x800030280601143F	358
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL	0x8000A8280601143F	451
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x800038280601143F	369
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL	0x8000B0280601143F	463
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x800040280601143F	380
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL	0x8000B8280601143F	473
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL	0x8000C0280601143F	485

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IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x800000280601143F	273
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL	0x8003002A0601143F	775
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x8002482A0601143F	627
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL	0x8003082A0601143F	788
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x8002502A0601143F	643
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL	0x8003102A0601143F	803
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x8002582A0601143F	658
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x8002602A0601143F	669
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x8002402A0601143F	601
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x8002202A0601143F	549
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL	0x8002C02A0601143F	734
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x8002282A0601143F	561
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL	0x8002C82A0601143F	753
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x8002302A0601143F	573
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x8002682A0601143F	685
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x8002702A0601143F	702
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x8002782A0601143F	713
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x8002182A0601143F	530
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x8002102A0601143F	520
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_PL	0x8002082A0601143F	511
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x8002002A0601143F	501
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x8000082A0601143F	291
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL	0x8000802A0601143F	392
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x8000102A0601143F	309
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL	0x8000882A0601143F	404
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x8000182A0601143F	322
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL	0x8000902A0601143F	416
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x8000202A0601143F	334
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL	0x8000982A0601143F	428

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IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x8000282A0601143F	347
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL	0x8000A02A0601143F	440
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x8000302A0601143F	358
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL	0x8000A82A0601143F	452
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x8000382A0601143F	370
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL	0x8000B02A0601143F	464
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x8000402A0601143F	380
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL	0x8000B82A0601143F	474
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL	0x8000C02A0601143F	486
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x8000002A0601143F	273
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL	0x800300290601143F	774
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x800248290601143F	627
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL	0x800308290601143F	788
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x800250290601143F	642
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL	0x800310290601143F	802
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x800258290601143F	657
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x800260290601143F	669
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x800240290601143F	599
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x800220290601143F	548
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL	0x8002C0290601143F	734
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x800228290601143F	561
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL	0x8002C8290601143F	753
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x800230290601143F	572
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x800268290601143F	685
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x800270290601143F	701
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x800278290601143F	713
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x800218290601143F	530
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x800210290601143F	520
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_PL	0x800208290601143F	511

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IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x800200290601143F	501
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x800008290601143F	290
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL	0x800080290601143F	391
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x800010290601143F	308
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL	0x800088290601143F	403
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x800018290601143F	322
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL	0x800090290601143F	415
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x800020290601143F	334
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL	0x800098290601143F	427
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x800028290601143F	347
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL	0x8000A0290601143F	439
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x800030290601143F	358
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL	0x8000A8290601143F	451
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x800038290601143F	370
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL	0x8000B0290601143F	463
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x800040290601143F	380
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL	0x8000B8290601143F	474
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL	0x8000C0290601143F	486
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x800000290601143F	273
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL	0x800300310601143F	779
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x800248310601143F	632
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL	0x800308310601143F	790
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x800250310601143F	645
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL	0x800310310601143F	806
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x800258310601143F	661
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x800260310601143F	671
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x800240310601143F	608
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x800220310601143F	553

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IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL	0x8002C0310601143F	739
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x800228310601143F	563
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL	0x8002C8310601143F	757
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x800230310601143F	575
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x800268310601143F	689
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x800270310601143F	705
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x800278310601143F	715
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x800218310601143F	532
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x800210310601143F	522
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_PL	0x800208310601143F	513
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x800200310601143F	504
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x800008310601143F	294
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL	0x800080310601143F	394
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x800010310601143F	312
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL	0x800088310601143F	406
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x800018310601143F	325
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL	0x800090310601143F	418
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x800020310601143F	337
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL	0x800098310601143F	430
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x800028310601143F	350
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL	0x8000A0310601143F	442
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x800030310601143F	360
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL	0x8000A8310601143F	454
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x800038310601143F	372
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL	0x8000B0310601143F	466
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x800040310601143F	382
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL	0x8000B8310601143F	476

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IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL	0x8000C0310601143F	489
IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x800000310601143F	277
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL	0x8003002E0601143F	777
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x8002482E0601143F	630
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL	0x8003082E0601143F	789
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x8002502E0601143F	644
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL	0x8003102E0601143F	805
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x8002582E0601143F	659
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x8002602E0601143F	670
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x8002402E0601143F	605
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x8002202E0601143F	551
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL	0x8002C02E0601143F	737
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x8002282E0601143F	562
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL	0x8002C82E0601143F	755
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x8002302E0601143F	574
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x8002682E0601143F	687
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x8002702E0601143F	704
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x8002782E0601143F	715
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x8002182E0601143F	531
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x8002102E0601143F	521
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_PL	0x8002082E0601143F	512
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x8002002E0601143F	503
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x8000082E0601143F	293
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL	0x8000802E0601143F	393
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x8000102E0601143F	311
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL	0x8000882E0601143F	405
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x8000182E0601143F	324
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL	0x8000902E0601143F	417
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x8000202E0601143F	336

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IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL	0x8000982E0601143F	429
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x8000282E0601143F	349
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL	0x8000A02E0601143F	441
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x8000302E0601143F	359
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL	0x8000A82E0601143F	453
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x8000382E0601143F	371
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL	0x8000B02E0601143F	465
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x8000402E0601143F	381
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL	0x8000B82E0601143F	475
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL	0x8000C02E0601143F	488
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x8000002E0601143F	275
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL	0x8003002C0601143F	776
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x8002482C0601143F	629
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL	0x8003082C0601143F	788
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x8002502C0601143F	643
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL	0x8003102C0601143F	804
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x8002582C0601143F	659
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x8002602C0601143F	670
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x8002402C0601143F	602
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x8002202C0601143F	550
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL	0x8002C02C0601143F	736
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x8002282C0601143F	562
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL	0x8002C82C0601143F	754
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x8002302C0601143F	573
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x8002682C0601143F	686
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x8002702C0601143F	703
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x8002782C0601143F	714
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x8002182C0601143F	531

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IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x8002102C0601143F	521
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_PL	0x8002082C0601143F	512
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x8002002C0601143F	502
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x8000082C0601143F	292
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL	0x8000802C0601143F	392
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x8000102C0601143F	310
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL	0x8000882C0601143F	404
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x8000182C0601143F	323
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL	0x8000902C0601143F	416
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x8000202C0601143F	335
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL	0x8000982C0601143F	428
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x8000282C0601143F	348
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL	0x8000A02C0601143F	440
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x8000302C0601143F	359
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL	0x8000A82C0601143F	452
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x8000382C0601143F	371
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL	0x8000B02C0601143F	464
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x8000402C0601143F	381
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL	0x8000B82C0601143F	474
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL	0x8000C02C0601143F	487
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x8000002C0601143F	274
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL	0x8003002D0601143F	777
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x8002482D0601143F	629
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL	0x8003082D0601143F	789
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x8002502D0601143F	644
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL	0x8003102D0601143F	804
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x8002582D0601143F	659
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x8002602D0601143F	670
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x8002402D0601143F	604

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IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x8002202D0601143F	551
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL	0x8002C02D0601143F	736
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x8002282D0601143F	562
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL	0x8002C82D0601143F	755
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x8002302D0601143F	574
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x8002682D0601143F	687
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x8002702D0601143F	703
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x8002782D0601143F	714
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x8002182D0601143F	531
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x8002102D0601143F	521
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_PL	0x8002082D0601143F	512
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x8002002D0601143F	502
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x8000082D0601143F	292
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL	0x8000802D0601143F	393
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x8000102D0601143F	310
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL	0x8000882D0601143F	405
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x8000182D0601143F	323
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL	0x8000902D0601143F	417
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x8000202D0601143F	335
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL	0x8000982D0601143F	429
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x8000282D0601143F	348
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL	0x8000A02D0601143F	441
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x8000302D0601143F	359
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL	0x8000A82D0601143F	453
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x8000382D0601143F	371
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL	0x8000B02D0601143F	465
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x8000402D0601143F	381

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IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL	0x8000B82D0601143F	475
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL	0x8000C02D0601143F	487
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x8000002D0601143F	275
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL	0x8003002B0601143F	775
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x8002482B0601143F	628
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL	0x8003082B0601143F	788
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x8002502B0601143F	643
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL	0x8003102B0601143F	803
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x8002582B0601143F	658
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x8002602B0601143F	669
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x8002402B0601143F	602
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x8002202B0601143F	550
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL	0x8002C02B0601143F	735
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x8002282B0601143F	562
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL	0x8002C82B0601143F	754
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x8002302B0601143F	573
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x8002682B0601143F	686
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x8002702B0601143F	702
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x8002782B0601143F	714
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x8002182B0601143F	530
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x8002102B0601143F	521
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_PL	0x8002082B0601143F	512
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x8002002B0601143F	501
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x8000082B0601143F	291
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL	0x8000802B0601143F	392
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x8000102B0601143F	309
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL	0x8000882B0601143F	404
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x8000182B0601143F	323
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL	0x8000902B0601143F	416

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IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x8000202B0601143F	335
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL	0x8000982B0601143F	428
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x8000282B0601143F	348
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL	0x8000A02B0601143F	440
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x8000302B0601143F	359
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL	0x8000A82B0601143F	452
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x8000382B0601143F	370
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL	0x8000B02B0601143F	464
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x8000402B0601143F	380
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL	0x8000B82B0601143F	474
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL	0x8000C02B0601143F	486
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x8000002B0601143F	274
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL	0x8003002F0601143F	778
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x8002482F0601143F	631
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL	0x8003082F0601143F	789
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x8002502F0601143F	645
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL	0x8003102F0601143F	805
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x8002582F0601143F	660
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x8002602F0601143F	671
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x8002402F0601143F	606
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x8002202F0601143F	552
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL	0x8002C02F0601143F	738
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x8002282F0601143F	563
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL	0x8002C82F0601143F	756
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x8002302F0601143F	574
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x8002682F0601143F	688
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x8002702F0601143F	704
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x8002782F0601143F	715

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IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x8002182F0601143F	531
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x8002102F0601143F	522
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_FIR_PL	0x8002082F0601143F	513
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x8002002F0601143F	503
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x8000082F0601143F	293
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL	0x8000802F0601143F	393
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x8000102F0601143F	311
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL	0x8000882F0601143F	405
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x8000182F0601143F	324
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL	0x8000902F0601143F	417
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x8000202F0601143F	336
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL	0x8000982F0601143F	429
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x8000282F0601143F	349
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL	0x8000A02F0601143F	441
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x8000302F0601143F	360
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL	0x8000A82F0601143F	453
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x8000382F0601143F	372
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL	0x8000B02F0601143F	465
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x8000402F0601143F	382
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL	0x8000B82F0601143F	475
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL	0x8000C02F0601143F	488
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x8000002F0601143F	276
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL	0x800300300601143F	779
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x800248300601143F	631
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL	0x800308300601143F	790
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x800250300601143F	645
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL	0x800310300601143F	806
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x800258300601143F	660
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x800260300601143F	671

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IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x800240300601143F	607
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x800220300601143F	553
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL	0x8002C0300601143F	738
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x800228300601143F	563
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL	0x8002C8300601143F	756
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x800230300601143F	575
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x800268300601143F	688
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x800270300601143F	705
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x800278300601143F	715
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x800218300601143F	532
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x800210300601143F	522
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_FIR_PL	0x800208300601143F	513
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x800200300601143F	504
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x800008300601143F	294
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL	0x800080300601143F	394
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x800010300601143F	312
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL	0x800088300601143F	406
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x800018300601143F	324
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL	0x800090300601143F	418
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x800020300601143F	336
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL	0x800098300601143F	430
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x800028300601143F	350
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL	0x8000A0300601143F	442
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x800030300601143F	360
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL	0x8000A8300601143F	454
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x800038300601143F	372
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL	0x8000B0300601143F	466

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IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x800040300601143F	382
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL	0x8000B8300601143F	476
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL	0x8000C0300601143F	488
IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x800000300601143F	276
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#0.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL	0x800380210601143F	818
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#0.RX_WORK_REGS.RX_WORK_STAT1_EO_PL	0x800388210601143F	852
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#0.RX_WORK_REGS.RX_WORK_STAT2_EO_PL	0x800390210601143F	885
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#0.RX_WORK_REGS.RX_WORK_STAT3_EO_PL	0x800398210601143F	901
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#1.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL	0x800380230601143F	819
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#1.RX_WORK_REGS.RX_WORK_STAT1_EO_PL	0x800388230601143F	854
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#1.RX_WORK_REGS.RX_WORK_STAT2_EO_PL	0x800390230601143F	886
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#1.RX_WORK_REGS.RX_WORK_STAT3_EO_PL	0x800398230601143F	902
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#10.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL	0x800380290601143F	821
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#10.RX_WORK_REGS.RX_WORK_STAT1_EO_PL	0x800388290601143F	860
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#10.RX_WORK_REGS.RX_WORK_STAT2_EO_PL	0x800390290601143F	888
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#10.RX_WORK_REGS.RX_WORK_STAT3_EO_PL	0x800398290601143F	904
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#11.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL	0x800380310601143F	825
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#11.RX_WORK_REGS.RX_WORK_STAT1_EO_PL	0x800388310601143F	868
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#11.RX_WORK_REGS.RX_WORK_STAT2_EO_PL	0x800390310601143F	891
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#11.RX_WORK_REGS.RX_WORK_STAT3_EO_PL	0x800398310601143F	906
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#12.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL	0x8003802E0601143F	823
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#12.RX_WORK_REGS.RX_WORK_STAT1_EO_PL	0x8003882E0601143F	865
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#12.RX_WORK_REGS.RX_WORK_STAT2_EO_PL	0x8003902E0601143F	890
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#12.RX_WORK_REGS.RX_WORK_STAT3_EO_PL	0x8003982E0601143F	905
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#13.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL	0x8003802C0601143F	823
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#13.RX_WORK_REGS.RX_WORK_STAT1_EO_PL	0x8003882C0601143F	863
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#13.RX_WORK_REGS.RX_WORK_STAT2_EO_PL	0x8003902C0601143F	889

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IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#13.RX_WORK_REGS.RX_WORK_STAT3_EO_PL	0x8003982C0601143F	904
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#14.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL	0x8003802D0601143F	823
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#14.RX_WORK_REGS.RX_WORK_STAT1_EO_PL	0x8003882D0601143F	864
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#14.RX_WORK_REGS.RX_WORK_STAT2_EO_PL	0x8003902D0601143F	890
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#14.RX_WORK_REGS.RX_WORK_STAT3_EO_PL	0x8003982D0601143F	905
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#15.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL	0x8003802B0601143F	822
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#15.RX_WORK_REGS.RX_WORK_STAT1_EO_PL	0x8003882B0601143F	862
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#15.RX_WORK_REGS.RX_WORK_STAT2_EO_PL	0x8003902B0601143F	889
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#15.RX_WORK_REGS.RX_WORK_STAT3_EO_PL	0x8003982B0601143F	904
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#16.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL	0x8003802F0601143F	824
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#16.RX_WORK_REGS.RX_WORK_STAT1_EO_PL	0x8003882F0601143F	866
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#16.RX_WORK_REGS.RX_WORK_STAT2_EO_PL	0x8003902F0601143F	891
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#16.RX_WORK_REGS.RX_WORK_STAT3_EO_PL	0x8003982F0601143F	905
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#17.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL	0x800380300601143F	824
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#17.RX_WORK_REGS.RX_WORK_STAT1_EO_PL	0x800388300601143F	867
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#17.RX_WORK_REGS.RX_WORK_STAT2_EO_PL	0x800390300601143F	891
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#17.RX_WORK_REGS.RX_WORK_STAT3_EO_PL	0x800398300601143F	906
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#18.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL	0x800380320601143F	825
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#18.RX_WORK_REGS.RX_WORK_STAT1_EO_PL	0x800388320601143F	869
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#18.RX_WORK_REGS.RX_WORK_STAT2_EO_PL	0x800390320601143F	892
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#18.RX_WORK_REGS.RX_WORK_STAT3_EO_PL	0x800398320601143F	906
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#19.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL	0x800380330601143F	826
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#19.RX_WORK_REGS.RX_WORK_STAT1_EO_PL	0x800388330601143F	870
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#19.RX_WORK_REGS.RX_WORK_STAT2_EO_PL	0x800390330601143F	892
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#19.RX_WORK_REGS.RX_WORK_STAT3_EO_PL	0x800398330601143F	906
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#2.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL	0x800380200601143F	817
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#2.RX_WORK_REGS.RX_WORK_STAT1_EO_PL	0x800388200601143F	851

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IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#2.RX_WORK_REGS.RX_WORK_STAT2_EO_PL	0x800390200601143F	885
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#2.RX_WORK_REGS.RX_WORK_STAT3_EO_PL	0x800398200601143F	901
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#20.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL	0x800380340601143F	826
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#20.RX_WORK_REGS.RX_WORK_STAT1_EO_PL	0x800388340601143F	871
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#20.RX_WORK_REGS.RX_WORK_STAT2_EO_PL	0x800390340601143F	893
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#20.RX_WORK_REGS.RX_WORK_STAT3_EO_PL	0x800398340601143F	907
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IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#21.RX_WORK_REGS.RX_WORK_STAT2_EO_PL	0x800390350601143F	893
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#21.RX_WORK_REGS.RX_WORK_STAT3_EO_PL	0x800398350601143F	907
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#22.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL	0x800380360601143F	827
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#22.RX_WORK_REGS.RX_WORK_STAT1_EO_PL	0x800388360601143F	873
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#22.RX_WORK_REGS.RX_WORK_STAT2_EO_PL	0x800390360601143F	893
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#22.RX_WORK_REGS.RX_WORK_STAT3_EO_PL	0x800398360601143F	907
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#23.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL	0x800380370601143F	827
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#23.RX_WORK_REGS.RX_WORK_STAT1_EO_PL	0x800388370601143F	874
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#23.RX_WORK_REGS.RX_WORK_STAT2_EO_PL	0x800390370601143F	894
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#23.RX_WORK_REGS.RX_WORK_STAT3_EO_PL	0x800398370601143F	908
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#3.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL	0x800380220601143F	818
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#3.RX_WORK_REGS.RX_WORK_STAT1_EO_PL	0x800388220601143F	853
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#3.RX_WORK_REGS.RX_WORK_STAT2_EO_PL	0x800390220601143F	885
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#3.RX_WORK_REGS.RX_WORK_STAT3_EO_PL	0x800398220601143F	902
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#4.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL	0x800380270601143F	820
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#4.RX_WORK_REGS.RX_WORK_STAT1_EO_PL	0x800388270601143F	858
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#4.RX_WORK_REGS.RX_WORK_STAT2_EO_PL	0x800390270601143F	887
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#4.RX_WORK_REGS.RX_WORK_STAT3_EO_PL	0x800398270601143F	903
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#5.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL	0x800380250601143F	819

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IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#5.RX_WORK_REGS.RX_WORK_STAT1_EO_PL	0x800388250601143F	856
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IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#5.RX_WORK_REGS.RX_WORK_STAT3_EO_PL	0x800398250601143F	902
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#6.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL	0x800380260601143F	820
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#6.RX_WORK_REGS.RX_WORK_STAT1_EO_PL	0x800388260601143F	857
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#6.RX_WORK_REGS.RX_WORK_STAT2_EO_PL	0x800390260601143F	887
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#6.RX_WORK_REGS.RX_WORK_STAT3_EO_PL	0x800398260601143F	903
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IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#7.RX_WORK_REGS.RX_WORK_STAT1_EO_PL	0x800388240601143F	855
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#7.RX_WORK_REGS.RX_WORK_STAT2_EO_PL	0x800390240601143F	886
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#7.RX_WORK_REGS.RX_WORK_STAT3_EO_PL	0x800398240601143F	902
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#8.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL	0x800380280601143F	821
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#8.RX_WORK_REGS.RX_WORK_STAT1_EO_PL	0x800388280601143F	859
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#8.RX_WORK_REGS.RX_WORK_STAT2_EO_PL	0x800390280601143F	888
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#8.RX_WORK_REGS.RX_WORK_STAT3_EO_PL	0x800398280601143F	903
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IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#9.RX_WORK_REGS.RX_WORK_STAT1_EO_PL	0x8003882A0601143F	861
IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#9.RX_WORK_REGS.RX_WORK_STAT2_EO_PL	0x8003902A0601143F	889
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IOF2.TX_WRAP.TX0.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_CNTL2_EO_PG	0x800C2C000601143F	1153
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IOF2.TX_WRAP.TX0.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_CNTL9_EO_PG	0x800CD4000601143F	1163
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IOF2.TX_WRAP.TX0.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_CNTLG4_E_PG	0x800CAC000601143F	1159
IOF2.TX_WRAP.TX0.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_CNTLG5_E_PG	0x800CB4000601143F	1159
IOF2.TX_WRAP.TX0.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_CNTLG6_E_PG	0x800CBC000601143F	1160
IOF2.TX_WRAP.TX0.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_CNTLG7_E_PG	0x800CC4000601143F	1162
IOF2.TX_WRAP.TX0.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_MODE1_EO_PG	0x800C14000601143F	1149
IOF2.TX_WRAP.TX0.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_MODE1_E_PG	0x800C8C000601143F	1155

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IOF2.TX_WRAP.TX0.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_MODE2_EO_PG	0x800C1C000601143F	1150
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IOF2.TX_WRAP.TX0.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_MODE3_E_PG	0x800CF4000601143F	1165
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IOF2.TX_WRAP.TX0.TXCTL.CTL_REGS.TX_CTL_REGS.TX_ID2_PG	0x800C84000601143F	1155
IOF2.TX_WRAP.TX0.TXCTL.CTL_REGS.TX_CTL_REGS.TX_SPARE_MODE_PG	0x800C04000601143F	1147
IOF2.TX_WRAP.TX0.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_CNTL1_EO_PG	0x800D34000601143F	1170
IOF2.TX_WRAP.TX0.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_CNTL2_EO_PG	0x800D3C000601143F	1171
IOF2.TX_WRAP.TX0.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_CNTL3_EO_PG	0x800D44000601143F	1171
IOF2.TX_WRAP.TX0.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_CNTL4_EO_PG	0x800D4C000601143F	1172
IOF2.TX_WRAP.TX0.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_CNTL5_EO_PG	0x800D54000601143F	1172
IOF2.TX_WRAP.TX0.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_CNTL6_EO_PG	0x800D5C000601143F	1173
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IOF2.TX_WRAP.TX0.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_SPARE_MODE_PG	0x800D24000601143F	1168
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IOF2.TX_WRAP.TX0.TXCTL.TX_CTL_SM.REGS.TX_FIR_ERROR_INJECT_PG	0x800D1C000601143F	1168
IOF2.TX_WRAP.TX0.TXCTL.TX_CTL_SM.REGS.TX_FIR_MASK_PG	0x800D0C000601143F	1166
IOF2.TX_WRAP.TX0.TXCTL.TX_CTL_SM.REGS.TX_FIR_PG	0x800D04000601143F	1166
IOF2.TX_WRAP.TX0.TXCTL.TX_CTL_SM.REGS.TX_FIR_RESET_PG	0x800D14000601143F	1167
IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL	0x80043C000601143F	1017
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IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_CNTL3_EO_PL	0x800454000601143F	1051
IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL	0x800434000601143F	1008
IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_MASK_PL	0x80042C000601143F	998
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IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_MODE1_PL	0x800404000601143F	908
IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_MODE2_PL	0x80040C000601143F	935
IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_STAT1_PL	0x80041C000601143F	975
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IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_CNTL3_EO_PL	0x800454010601143F	1051
IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL	0x800434010601143F	1008
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IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_PL	0x800424010601143F	990

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IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_MODE1_PL	0x800404010601143F	909
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IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_STAT1_PL	0x80041C010601143F	976
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Mnemonic	Address	Page
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IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_MASK_PL	0x80042C280601143F	1005
IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_PL	0x800424280601143F	996
IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_MODE1_PL	0x800404280601143F	928
IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_MODE2_PL	0x80040C280601143F	954
IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_STAT1_PL	0x80041C280601143F	986
IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL	0x80043C290601143F	1030
IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_BIT_MODE2_E_PL	0x800444290601143F	1047
IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_CNTL1G_PL	0x800414290601143F	972
IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_CNTL3_EO_PL	0x800454290601143F	1057

Mnemonic	Address	Page
IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL	0x800434290601143F	1015
IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_MASK_PL	0x80042C290601143F	1005
IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_PL	0x800424290601143F	996
IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_MODE1_PL	0x800404290601143F	929
IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_MODE2_PL	0x80040C290601143F	955
IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_STAT1_PL	0x80041C290601143F	986
IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL	0x80043C2A0601143F	1030
IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_BIT_MODE2_E_PL	0x8004442A0601143F	1047
IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_CNTL1G_PL	0x8004142A0601143F	972
IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_CNTL3_EO_PL	0x8004542A0601143F	1058
IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL	0x8004342A0601143F	1015
IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_MASK_PL	0x80042C2A0601143F	1006
IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_PL	0x8004242A0601143F	997
IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_MODE1_PL	0x8004042A0601143F	929
IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_MODE2_PL	0x80040C2A0601143F	955
IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_STAT1_PL	0x80041C2A0601143F	987
IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL	0x80043C2B0601143F	1031
IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_BIT_MODE2_E_PL	0x8004442B0601143F	1048
IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_CNTL1G_PL	0x8004142B0601143F	973
IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_CNTL3_EO_PL	0x8004542B0601143F	1058
IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL	0x8004342B0601143F	1015
IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_MASK_PL	0x80042C2B0601143F	1006
IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_PL	0x8004242B0601143F	997
IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_MODE1_PL	0x8004042B0601143F	930
IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_MODE2_PL	0x80040C2B0601143F	956
IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_STAT1_PL	0x80041C2B0601143F	987
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL	0x80043C2C0601143F	1031
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_BIT_MODE2_E_PL	0x8004442C0601143F	1048
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_CNTL1G_PL	0x8004142C0601143F	973
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_CNTL3_EO_PL	0x8004542C0601143F	1058
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL	0x8004342C0601143F	1015
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_MASK_PL	0x80042C2C0601143F	1006
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_PL	0x8004242C0601143F	997
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_MODE1_PL	0x8004042C0601143F	931

Mnemonic	Address	Page
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_MODE2_PL	0x80040C2C0601143F	957
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_STAT1_PL	0x80041C2C0601143F	988
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL	0x80043C2D0601143F	1032
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_BIT_MODE2_E_PL	0x8004442D0601143F	1049
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_CNTL1G_PL	0x8004142D0601143F	974
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_CNTL3_EO_PL	0x8004542D0601143F	1058
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL	0x8004342D0601143F	1016
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_MASK_PL	0x80042C2D0601143F	1006
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_PL	0x8004242D0601143F	997
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_MODE1_PL	0x8004042D0601143F	932
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_MODE2_PL	0x80040C2D0601143F	958
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_STAT1_PL	0x80041C2D0601143F	988
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL	0x80043C2E0601143F	1032
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_BIT_MODE2_E_PL	0x8004442E0601143F	1049
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_CNTL1G_PL	0x8004142E0601143F	974
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_CNTL3_EO_PL	0x8004542E0601143F	1059
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL	0x8004342E0601143F	1016
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_MASK_PL	0x80042C2E0601143F	1007
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_PL	0x8004242E0601143F	998
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_MODE1_PL	0x8004042E0601143F	933
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_MODE2_PL	0x80040C2E0601143F	958
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_STAT1_PL	0x80041C2E0601143F	989
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL	0x80043C2F0601143F	1033
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_BIT_MODE2_E_PL	0x8004442F0601143F	1050
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_CNTL1G_PL	0x8004142F0601143F	974
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_CNTL3_EO_PL	0x8004542F0601143F	1059
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL	0x8004342F0601143F	1016
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_MASK_PL	0x80042C2F0601143F	1007
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_PL	0x8004242F0601143F	998
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_MODE1_PL	0x8004042F0601143F	933
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_MODE2_PL	0x80040C2F0601143F	959
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_STAT1_PL	0x80041C2F0601143F	989
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#4.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL	0x80043C300601143F	1033
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#4.DD.TX_BIT_REGS.TX_BIT_MODE2_E_PL	0x800444300601143F	1050

Mnemonic	Address	Page
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#4.DD.TX_BIT_REGS.TX_CNTL1G_PL	0x800414300601143F	975
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#4.DD.TX_BIT_REGS.TX_CNTL3_EO_PL	0x800454300601143F	1059
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#4.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL	0x800434300601143F	1017
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#4.DD.TX_BIT_REGS.TX_FIR_MASK_PL	0x80042C300601143F	1007
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#4.DD.TX_BIT_REGS.TX_FIR_PL	0x800424300601143F	998
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#4.DD.TX_BIT_REGS.TX_MODE1_PL	0x800404300601143F	934
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#4.DD.TX_BIT_REGS.TX_MODE2_PL	0x80040C300601143F	960
IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#4.DD.TX_BIT_REGS.TX_STAT1_PL	0x80041C300601143F	989

The POWER9 processor registers are listed in the following tables.

Register Name	**Receive Data DAC Spare Mode Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	800000000601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Data DAC Spare Mode Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	800000010601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	800000020601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	800000030601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	800000040601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	800000050601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	800000060601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	800000070601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	800000080601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	800000090601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	8000000A0601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	8000000B0601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	8000000C0601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	8000000D0601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	8000000E0601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Data DAC Spare Mode Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	8000000F0601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Data DAC Spare Mode Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	800000100601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	800000110601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	800000200601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	800000210601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Data DAC Spare Mode Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	800000220601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Data DAC Spare Mode Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	800000230601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	800000240601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	800000250601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	800000260601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	800000270601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	800000280601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	800000290601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	8000002A0601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Data DAC Spare Mode Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	8000002B0601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Data DAC Spare Mode Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	8000002C0601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	8000002D0601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	8000002E0601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Data DAC Spare Mode Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	8000002F0601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Data DAC Spare Mode Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	800000300601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	800000310601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	800008000601143F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PDWN_LITE_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RO	constant = 0b000000

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	800008010601143F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PDWN_LITE_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RO	constant = 0b000000

Register Name	**Receive DAC Control 1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	800008020601143F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PDWN_LITE_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RO	constant = 0b000000

Register Name	**Receive DAC Control 1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	800008030601143F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_PDWN_LITE_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RO	constant = 0b000000

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	800008040601143F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PDWN_LITE_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RO	constant = 0b000000

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	800008050601143F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_PDWN_LITE_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RO	constant = 0b000000

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	800008060601143F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PDWN_LITE_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RO	constant = 0b000000

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	800008070601143F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_PDWN_LITE_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RO	constant = 0b000000

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	800008080601143F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PDWN_LITE_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RO	constant = 0b000000

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	800008090601143F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_PDWN_LITE_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RO	constant = 0b000000

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	8000080A0601143F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PDWN_LITE_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RO	constant = 0b000000

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	8000080B0601143F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_PDWN_LITE_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RO	constant = 0b000000

Register Name	**Receive DAC Control 1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	8000080C0601143F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PDWN_LITE_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RO	constant = 0b000000

Register Name	**Receive DAC Control 1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	8000080D0601143F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_PDWN_LITE_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RO	constant = 0b000000

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	8000080E0601143F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PDWN_LITE_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RO	constant = 0b000000

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	8000080F0601143F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_PDWN_LITE_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RO	constant = 0b000000

Register Name	**Receive DAC Control 1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	800008100601143F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PDWN_LITE_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RO	constant = 0b000000

Register Name	**Receive DAC Control 1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	800008110601143F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_PDWN_LITE_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RO	constant = 0b000000

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	800008200601143F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PDWN_LITE_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RO	constant = 0b000000

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	800008210601143F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_PDWN_LITE_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RO	constant = 0b000000

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	800008220601143F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PDWN_LITE_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RO	constant = 0b000000

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	800008230601143F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_PDWN_LITE_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RO	constant = 0b000000

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	800008240601143F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PDWN_LITE_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RO	constant = 0b000000

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	800008250601143F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_PDWN_LITE_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RO	constant = 0b000000

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	800008260601143F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PDWN_LITE_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RO	constant = 0b000000

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	800008270601143F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_PDWN_LITE_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RO	constant = 0b000000

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	800008280601143F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PDWN_LITE_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RO	constant = 0b000000

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	800008290601143F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_PDWN_LITE_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RO	constant = 0b000000

Register Name	**Receive DAC Control 1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	8000082A0601143F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PDWN_LITE_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RO	constant = 0b000000

Register Name	**Receive DAC Control 1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	8000082B0601143F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_PDWN_LITE_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RO	constant = 0b000000

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	8000082C0601143F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PDWN_LITE_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RO	constant = 0b000000

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	8000082D0601143F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_PDWN_LITE_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RO	constant = 0b000000

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	8000082E0601143F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PDWN_LITE_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RO	constant = 0b000000

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	8000082F0601143F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_PDWN_LITE_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RO	constant = 0b000000

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	800008300601143F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PDWN_LITE_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RO	constant = 0b000000

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	800008310601143F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_PDWN_LITE_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RO	constant = 0b000000

Register Name	**Receive DAC Control 2 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	800010000601143F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	**Receive DAC Control 2 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	800010010601143F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	800010020601143F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	800010030601143F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	800010040601143F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	800010050601143F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	800010060601143F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	800010070601143F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	800010080601143F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	800010090601143F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	8000100A0601143F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	8000100B0601143F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	8000100C0601143F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	8000100D0601143F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	8000100E0601143F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	8000100F0601143F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	800010100601143F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	800010110601143F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	800010200601143F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	800010210601143F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	800010220601143F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	800010230601143F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	800010240601143F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	800010250601143F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	800010260601143F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	800010270601143F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	800010280601143F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	800010290601143F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	8000102A0601143F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	8000102B0601143F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	8000102C0601143F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	8000102D0601143F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	8000102E0601143F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	8000102F0601143F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	800010300601143F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	800010310601143F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	800018000601143F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	800018010601143F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	800018020601143F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	800018030601143F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	800018040601143F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	800018050601143F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	800018060601143F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	800018070601143F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	**Receive DAC Control 3 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	800018080601143F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	**Receive DAC Control 3 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	800018090601143F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	**Receive DAC Control 3 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	8000180A0601143F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	8000180B0601143F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	8000180C0601143F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	8000180D0601143F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	8000180E0601143F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	8000180F0601143F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	800018100601143F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	800018110601143F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	800018200601143F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	800018210601143F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	800018220601143F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	800018230601143F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	800018240601143F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	800018250601143F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	800018260601143F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	800018270601143F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	800018280601143F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	800018290601143F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	8000182A0601143F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	8000182B0601143F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	8000182C0601143F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	8000182D0601143F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	8000182E0601143F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	8000182F0601143F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	800018300601143F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	800018310601143F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	800020000601143F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	800020010601143F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	800020020601143F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	800020030601143F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	800020040601143F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	800020050601143F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	800020060601143F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	800020070601143F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	800020080601143F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	800020090601143F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	8000200A0601143F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	8000200B0601143F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	8000200C0601143F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	8000200D0601143F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	8000200E0601143F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	8000200F0601143F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	800020100601143F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	800020110601143F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	800020200601143F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	800020210601143F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	800020220601143F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	800020230601143F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	800020240601143F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	**Receive DAC Control 4 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	800020250601143F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	**Receive DAC Control 4 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	800020260601143F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	**Receive DAC Control 4 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	800020270601143F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	800020280601143F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	800020290601143F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	8000202A0601143F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	8000202B0601143F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	8000202C0601143F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	8000202D0601143F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	8000202E0601143F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	8000202F0601143F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	800020300601143F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	800020310601143F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	800028000601143F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	800028010601143F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	**Receive DAC Control 5 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	800028020601143F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	**Receive DAC Control 5 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	800028030601143F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	**Receive DAC Control 5 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	800028040601143F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.

Bits	SCOM	Field Mnemonic: Description
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	800028050601143F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	800028060601143F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	800028070601143F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	800028080601143F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	800028090601143F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	8000280A0601143F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	8000280B0601143F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	8000280C0601143F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.

Bits	SCOM	Field Mnemonic: Description
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	8000280D0601143F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	8000280E0601143F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	8000280F0601143F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	800028100601143F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	800028110601143F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	800028200601143F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	800028210601143F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	800028220601143F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.

Bits	SCOM	Field Mnemonic: Description
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	800028230601143F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	800028240601143F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	800028250601143F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	800028260601143F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	800028270601143F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	800028280601143F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	800028290601143F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	8000282A0601143F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.

Bits	SCOM	Field Mnemonic: Description
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	8000282B0601143F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	8000282C0601143F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	8000282D0601143F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	8000282E0601143F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	8000282F0601143F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	800028300601143F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	800028310601143F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	800030000601143F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_CTLE_PEAK: This is the CTLE coarse peak value. Only 4 bits are currently used.
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	800030010601143F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_CTLE_PEAK: This is the CTLE coarse peak value. Only 4 bits are currently used.
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	800030020601143F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_CTLE_PEAK: This is the CTLE coarse peak value. Only 4 bits are currently used.
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	800030030601143F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_CTLE_PEAK: This is the CTLE coarse peak value. Only 4 bits are currently used.
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	800030040601143F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_CTLE_PEAK: This is the CTLE coarse peak value. Only 4 bits are currently used.
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	800030050601143F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_CTLE_PEAK: This is the CTLE coarse peak value. Only 4 bits are currently used.
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	800030060601143F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_CTLE_PEAK: This is the CTLE coarse peak value. Only 4 bits are currently used.
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	800030070601143F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_CTLE_PEAK: This is the CTLE coarse peak value. Only 4 bits are currently used.
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	800030080601143F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_CTLE_PEAK: This is the CTLE coarse peak value. Only 4 bits are currently used.
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	800030090601143F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_CTLE_PEAK: This is the CTLE coarse peak value. Only 4 bits are currently used.
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	8000300A0601143F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_CTLE_PEAK: This is the CTLE coarse peak value. Only 4 bits are currently used.
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	8000300B0601143F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_CTLE_PEAK: This is the CTLE coarse peak value. Only 4 bits are currently used.
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	8000300C0601143F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_CTLE_PEAK: This is the CTLE coarse peak value. Only 4 bits are currently used.
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	8000300D0601143F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_CTLE_PEAK: This is the CTLE coarse peak value. Only 4 bits are currently used.
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	8000300E0601143F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_CTLE_PEAK: This is the CTLE coarse peak value. Only 4 bits are currently used.
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	8000300F0601143F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_CTLE_PEAK: This is the CTLE coarse peak value. Only 4 bits are currently used.
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	800030100601143F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_CTLE_PEAK: This is the CTLE coarse peak value. Only 4 bits are currently used.
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	800030110601143F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_CTLE_PEAK: This is the CTLE coarse peak value. Only 4 bits are currently used.
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	800030200601143F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_CTLE_PEAK: This is the CTLE coarse peak value. Only 4 bits are currently used.
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	800030210601143F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_CTLE_PEAK: This is the CTLE coarse peak value. Only 4 bits are currently used.
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	800030220601143F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_CTLE_PEAK: This is the CTLE coarse peak value. Only 4 bits are currently used.
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	800030230601143F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_CTLE_PEAK: This is the CTLE coarse peak value. Only 4 bits are currently used.
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	**Receive DAC Control 6 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	800030240601143F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	**SCOM**	**Field Mnemonic: Description**
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_CTLE_PEAK: This is the CTLE coarse peak value. Only 4 bits are currently used.
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	**Receive DAC Control 6 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	800030250601143F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	**SCOM**	**Field Mnemonic: Description**
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_CTLE_PEAK: This is the CTLE coarse peak value. Only 4 bits are currently used.
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	**Receive DAC Control 6 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	800030260601143F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	**SCOM**	**Field Mnemonic: Description**
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_CTLE_PEAK: This is the CTLE coarse peak value. Only 4 bits are currently used.
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	**Receive DAC Control 6 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	800030270601143F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_CTLE_PEAK: This is the CTLE coarse peak value. Only 4 bits are currently used.
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	800030280601143F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_CTLE_PEAK: This is the CTLE coarse peak value. Only 4 bits are currently used.
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	800030290601143F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_CTLE_PEAK: This is the CTLE coarse peak value. Only 4 bits are currently used.
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	8000302A0601143F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_CTLE_PEAK: This is the CTLE coarse peak value. Only 4 bits are currently used.
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	8000302B0601143F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_CTLE_PEAK: This is the CTLE coarse peak value. Only 4 bits are currently used.
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	8000302C0601143F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_CTLE_PEAK: This is the CTLE coarse peak value. Only 4 bits are currently used.
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	8000302D0601143F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_CTLE_PEAK: This is the CTLE coarse peak value. Only 4 bits are currently used.
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	8000302E0601143F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_CTLE_PEAK: This is the CTLE coarse peak value. Only 4 bits are currently used.
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	8000302F0601143F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_CTLE_PEAK: This is the CTLE coarse peak value. Only 4 bits are currently used.
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	800030300601143F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_CTLE_PEAK: This is the CTLE coarse peak value. Only 4 bits are currently used.
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	800030310601143F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_CTLE_PEAK: This is the CTLE coarse peak value. Only 4 bits are currently used.
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	800038000601143F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	800038010601143F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	800038020601143F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	800038030601143F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	800038040601143F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	800038050601143F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	800038060601143F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	800038070601143F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	800038080601143F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	800038090601143F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	8000380A0601143F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	8000380B0601143F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	8000380C0601143F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	8000380D0601143F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	8000380E0601143F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	**Receive DAC Control 7 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	8000380F0601143F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	**Receive DAC Control 7 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	800038100601143F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	**Receive DAC Control 7 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	800038110601143F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	800038200601143F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	800038210601143F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	800038220601143F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	800038230601143F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	800038240601143F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	800038250601143F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	800038260601143F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	800038270601143F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	800038280601143F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	800038290601143F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	8000382A0601143F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	8000382B0601143F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	8000382C0601143F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	8000382D0601143F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	8000382E0601143F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	8000382F0601143F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	800038300601143F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	800038310601143F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	800040000601143F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	800040010601143F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	800040020601143F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	800040030601143F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.

Bits	SCOM	Field Mnemonic: Description
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	800040040601143F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	800040050601143F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	800040060601143F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	800040070601143F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	800040080601143F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	800040090601143F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	8000400A0601143F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	8000400B0601143F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	8000400C0601143F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	8000400D0601143F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	8000400E0601143F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.

Bits	SCOM	Field Mnemonic: Description
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	8000400F0601143F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	800040100601143F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	800040110601143F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	800040200601143F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	800040210601143F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	800040220601143F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	800040230601143F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	**Receive DAC Control 8 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	800040240601143F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	**Receive DAC Control 8 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	800040250601143F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	**Receive DAC Control 8 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	800040260601143F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	**Receive DAC Control 8 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	800040270601143F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.

Bits	SCOM	Field Mnemonic: Description
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	800040280601143F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	800040290601143F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	8000402A0601143F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	8000402B0601143F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	8000402C0601143F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	8000402D0601143F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	8000402E0601143F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	8000402F0601143F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	800040300601143F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	800040310601143F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL
Address	800080000601143F (SCOM)
Description	This register contains the first set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_H2E_VAL: This field contains the DFE H1 value for even sampler 1.

Bits	SCOM	Field Mnemonic: Description
54:55	RO	constant = 0b00
56:61	RWX	RX_A_H2O_VAL: This field contains the DFE H1 value for even sampler 0.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL
Address	800080010601143F (SCOM)
Description	This register contains the first set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_H2E_VAL: This field contains the DFE H1 value for even sampler 1.
54:55	RO	constant = 0b00
56:61	RWX	RX_A_H2O_VAL: This field contains the DFE H1 value for even sampler 0.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL
Address	800080020601143F (SCOM)
Description	This register contains the first set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_H2E_VAL: This field contains the DFE H1 value for even sampler 1.
54:55	RO	constant = 0b00
56:61	RWX	RX_A_H2O_VAL: This field contains the DFE H1 value for even sampler 0.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL
Address	800080030601143F (SCOM)
Description	This register contains the first set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_H2E_VAL: This field contains the DFE H1 value for even sampler 1.
54:55	RO	constant = 0b00

Bits	SCOM	Field Mnemonic: Description
56:61	RWX	RX_A_H2O_VAL: This field contains the DFE H1 value for even sampler 0.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL
Address	800080040601143F (SCOM)
Description	This register contains the first set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_H2E_VAL: This field contains the DFE H1 value for even sampler 1.
54:55	RO	constant = 0b00
56:61	RWX	RX_A_H2O_VAL: This field contains the DFE H1 value for even sampler 0.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL
Address	800080050601143F (SCOM)
Description	This register contains the first set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_H2E_VAL: This field contains the DFE H1 value for even sampler 1.
54:55	RO	constant = 0b00
56:61	RWX	RX_A_H2O_VAL: This field contains the DFE H1 value for even sampler 0.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL
Address	800080060601143F (SCOM)
Description	This register contains the first set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_H2E_VAL: This field contains the DFE H1 value for even sampler 1.
54:55	RO	constant = 0b00
56:61	RWX	RX_A_H2O_VAL: This field contains the DFE H1 value for even sampler 0.

Bits	SCOM	Field Mnemonic: Description
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL
Address	800080070601143F (SCOM)
Description	This register contains the first set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_H2E_VAL: This field contains the DFE H1 value for even sampler 1.
54:55	RO	constant = 0b00
56:61	RWX	RX_A_H2O_VAL: This field contains the DFE H1 value for even sampler 0.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL
Address	800080080601143F (SCOM)
Description	This register contains the first set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_H2E_VAL: This field contains the DFE H1 value for even sampler 1.
54:55	RO	constant = 0b00
56:61	RWX	RX_A_H2O_VAL: This field contains the DFE H1 value for even sampler 0.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL
Address	800080090601143F (SCOM)
Description	This register contains the first set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_H2E_VAL: This field contains the DFE H1 value for even sampler 1.
54:55	RO	constant = 0b00
56:61	RWX	RX_A_H2O_VAL: This field contains the DFE H1 value for even sampler 0.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL
Address	8000800A0601143F (SCOM)
Description	This register contains the first set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_H2E_VAL: This field contains the DFE H1 value for even sampler 1.
54:55	RO	constant = 0b00
56:61	RWX	RX_A_H2O_VAL: This field contains the DFE H1 value for even sampler 0.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL
Address	8000800B0601143F (SCOM)
Description	This register contains the first set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_H2E_VAL: This field contains the DFE H1 value for even sampler 1.
54:55	RO	constant = 0b00
56:61	RWX	RX_A_H2O_VAL: This field contains the DFE H1 value for even sampler 0.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL
Address	8000800C0601143F (SCOM)
Description	This register contains the first set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_H2E_VAL: This field contains the DFE H1 value for even sampler 1.
54:55	RO	constant = 0b00
56:61	RWX	RX_A_H2O_VAL: This field contains the DFE H1 value for even sampler 0.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL
Address	8000800D0601143F (SCOM)
Description	This register contains the first set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_H2E_VAL: This field contains the DFE H1 value for even sampler 1.
54:55	RO	constant = 0b00
56:61	RWX	RX_A_H2O_VAL: This field contains the DFE H1 value for even sampler 0.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL
Address	8000800E0601143F (SCOM)
Description	This register contains the first set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_H2E_VAL: This field contains the DFE H1 value for even sampler 1.
54:55	RO	constant = 0b00
56:61	RWX	RX_A_H2O_VAL: This field contains the DFE H1 value for even sampler 0.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL
Address	8000800F0601143F (SCOM)
Description	This register contains the first set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_H2E_VAL: This field contains the DFE H1 value for even sampler 1.
54:55	RO	constant = 0b00
56:61	RWX	RX_A_H2O_VAL: This field contains the DFE H1 value for even sampler 0.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL
Address	800080100601143F (SCOM)
Description	This register contains the first set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_H2E_VAL: This field contains the DFE H1 value for even sampler 1.
54:55	RO	constant = 0b00
56:61	RWX	RX_A_H2O_VAL: This field contains the DFE H1 value for even sampler 0.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL
Address	800080110601143F (SCOM)
Description	This register contains the first set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_H2E_VAL: This field contains the DFE H1 value for even sampler 1.
54:55	RO	constant = 0b00
56:61	RWX	RX_A_H2O_VAL: This field contains the DFE H1 value for even sampler 0.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL
Address	800080200601143F (SCOM)
Description	This register contains the first set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_H2E_VAL: This field contains the DFE H1 value for even sampler 1.
54:55	RO	constant = 0b00
56:61	RWX	RX_A_H2O_VAL: This field contains the DFE H1 value for even sampler 0.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL
Address	800080210601143F (SCOM)
Description	This register contains the first set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_H2E_VAL: This field contains the DFE H1 value for even sampler 1.
54:55	RO	constant = 0b00
56:61	RWX	RX_A_H2O_VAL: This field contains the DFE H1 value for even sampler 0.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL
Address	800080220601143F (SCOM)
Description	This register contains the first set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_H2E_VAL: This field contains the DFE H1 value for even sampler 1.
54:55	RO	constant = 0b00
56:61	RWX	RX_A_H2O_VAL: This field contains the DFE H1 value for even sampler 0.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL
Address	800080230601143F (SCOM)
Description	This register contains the first set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_H2E_VAL: This field contains the DFE H1 value for even sampler 1.
54:55	RO	constant = 0b00
56:61	RWX	RX_A_H2O_VAL: This field contains the DFE H1 value for even sampler 0.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL
Address	800080240601143F (SCOM)
Description	This register contains the first set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_H2E_VAL: This field contains the DFE H1 value for even sampler 1.
54:55	RO	constant = 0b00
56:61	RWX	RX_A_H2O_VAL: This field contains the DFE H1 value for even sampler 0.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL
Address	800080250601143F (SCOM)
Description	This register contains the first set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_H2E_VAL: This field contains the DFE H1 value for even sampler 1.
54:55	RO	constant = 0b00
56:61	RWX	RX_A_H2O_VAL: This field contains the DFE H1 value for even sampler 0.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL
Address	800080260601143F (SCOM)
Description	This register contains the first set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_H2E_VAL: This field contains the DFE H1 value for even sampler 1.
54:55	RO	constant = 0b00
56:61	RWX	RX_A_H2O_VAL: This field contains the DFE H1 value for even sampler 0.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL
Address	800080270601143F (SCOM)
Description	This register contains the first set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_H2E_VAL: This field contains the DFE H1 value for even sampler 1.
54:55	RO	constant = 0b00
56:61	RWX	RX_A_H2O_VAL: This field contains the DFE H1 value for even sampler 0.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL
Address	800080280601143F (SCOM)
Description	This register contains the first set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_H2E_VAL: This field contains the DFE H1 value for even sampler 1.
54:55	RO	constant = 0b00
56:61	RWX	RX_A_H2O_VAL: This field contains the DFE H1 value for even sampler 0.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL
Address	800080290601143F (SCOM)
Description	This register contains the first set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_H2E_VAL: This field contains the DFE H1 value for even sampler 1.
54:55	RO	constant = 0b00
56:61	RWX	RX_A_H2O_VAL: This field contains the DFE H1 value for even sampler 0.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL
Address	8000802A0601143F (SCOM)
Description	This register contains the first set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_H2E_VAL: This field contains the DFE H1 value for even sampler 1.
54:55	RO	constant = 0b00
56:61	RWX	RX_A_H2O_VAL: This field contains the DFE H1 value for even sampler 0.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL
Address	8000802B0601143F (SCOM)
Description	This register contains the first set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_H2E_VAL: This field contains the DFE H1 value for even sampler 1.
54:55	RO	constant = 0b00
56:61	RWX	RX_A_H2O_VAL: This field contains the DFE H1 value for even sampler 0.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL
Address	8000802C0601143F (SCOM)
Description	This register contains the first set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_H2E_VAL: This field contains the DFE H1 value for even sampler 1.
54:55	RO	constant = 0b00
56:61	RWX	RX_A_H2O_VAL: This field contains the DFE H1 value for even sampler 0.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL
Address	8000802D0601143F (SCOM)
Description	This register contains the first set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_H2E_VAL: This field contains the DFE H1 value for even sampler 1.
54:55	RO	constant = 0b00
56:61	RWX	RX_A_H2O_VAL: This field contains the DFE H1 value for even sampler 0.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL
Address	8000802E0601143F (SCOM)
Description	This register contains the first set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_H2E_VAL: This field contains the DFE H1 value for even sampler 1.
54:55	RO	constant = 0b00
56:61	RWX	RX_A_H2O_VAL: This field contains the DFE H1 value for even sampler 0.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL
Address	8000802F0601143F (SCOM)
Description	This register contains the first set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_H2E_VAL: This field contains the DFE H1 value for even sampler 1.
54:55	RO	constant = 0b00
56:61	RWX	RX_A_H2O_VAL: This field contains the DFE H1 value for even sampler 0.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL
Address	800080300601143F (SCOM)
Description	This register contains the first set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_H2E_VAL: This field contains the DFE H1 value for even sampler 1.
54:55	RO	constant = 0b00
56:61	RWX	RX_A_H2O_VAL: This field contains the DFE H1 value for even sampler 0.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_E_PL
Address	800080310601143F (SCOM)
Description	This register contains the first set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_H2E_VAL: This field contains the DFE H1 value for even sampler 1.
54:55	RO	constant = 0b00
56:61	RWX	RX_A_H2O_VAL: This field contains the DFE H1 value for even sampler 0.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL
Address	800088000601143F (SCOM)
Description	This register contains the second set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H3E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H3O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL
Address	800088010601143F (SCOM)
Description	This register contains the second set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H3E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H3O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL
Address	800088020601143F (SCOM)
Description	This register contains the second set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H3E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H3O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL
Address	800088030601143F (SCOM)
Description	This register contains the second set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H3E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H3O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL
Address	800088040601143F (SCOM)
Description	This register contains the second set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H3E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H3O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL
Address	800088050601143F (SCOM)
Description	This register contains the second set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H3E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H3O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL
Address	800088060601143F (SCOM)
Description	This register contains the second set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H3E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H3O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL
Address	800088070601143F (SCOM)
Description	This register contains the second set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H3E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H3O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL
Address	800088080601143F (SCOM)
Description	This register contains the second set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H3E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H3O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL
Address	800088090601143F (SCOM)
Description	This register contains the second set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H3E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H3O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL
Address	8000880A0601143F (SCOM)
Description	This register contains the second set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H3E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H3O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL
Address	8000880B0601143F (SCOM)
Description	This register contains the second set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H3E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H3O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL
Address	8000880C0601143F (SCOM)
Description	This register contains the second set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H3E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H3O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL
Address	8000880D0601143F (SCOM)
Description	This register contains the second set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H3E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H3O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL
Address	8000880E0601143F (SCOM)
Description	This register contains the second set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H3E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H3O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL
Address	8000880F0601143F (SCOM)
Description	This register contains the second set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H3E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H3O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL
Address	800088100601143F (SCOM)
Description	This register contains the second set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H3E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H3O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL
Address	800088110601143F (SCOM)
Description	This register contains the second set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H3E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H3O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL
Address	800088200601143F (SCOM)
Description	This register contains the second set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H3E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H3O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL
Address	800088210601143F (SCOM)
Description	This register contains the second set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H3E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H3O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL
Address	800088220601143F (SCOM)
Description	This register contains the second set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H3E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H3O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL
Address	800088230601143F (SCOM)
Description	This register contains the second set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H3E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H3O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL
Address	800088240601143F (SCOM)
Description	This register contains the second set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H3E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H3O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL
Address	800088250601143F (SCOM)
Description	This register contains the second set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H3E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H3O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL
Address	800088260601143F (SCOM)
Description	This register contains the second set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H3E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H3O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL
Address	800088270601143F (SCOM)
Description	This register contains the second set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H3E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H3O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL
Address	800088280601143F (SCOM)
Description	This register contains the second set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H3E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H3O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL
Address	800088290601143F (SCOM)
Description	This register contains the second set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H3E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H3O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL
Address	8000882A0601143F (SCOM)
Description	This register contains the second set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H3E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H3O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL
Address	8000882B0601143F (SCOM)
Description	This register contains the second set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H3E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H3O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL
Address	8000882C0601143F (SCOM)
Description	This register contains the second set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H3E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H3O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL
Address	8000882D0601143F (SCOM)
Description	This register contains the second set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H3E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H3O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL
Address	8000882E0601143F (SCOM)
Description	This register contains the second set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H3E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H3O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL
Address	8000882F0601143F (SCOM)
Description	This register contains the second set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H3E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H3O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL
Address	800088300601143F (SCOM)
Description	This register contains the second set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H3E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H3O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_E_PL
Address	800088310601143F (SCOM)
Description	This register contains the second set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H3E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H3O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL
Address	800090000601143F (SCOM)
Description	This register contains the third set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H4E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H4O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL
Address	800090010601143F (SCOM)
Description	This register contains the third set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H4E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H4O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL
Address	800090020601143F (SCOM)
Description	This register contains the third set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H4E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H4O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL
Address	800090030601143F (SCOM)
Description	This register contains the third set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H4E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H4O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL
Address	800090040601143F (SCOM)
Description	This register contains the third set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H4E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H4O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL
Address	800090050601143F (SCOM)
Description	This register contains the third set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H4E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H4O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL
Address	800090060601143F (SCOM)
Description	This register contains the third set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H4E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H4O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL
Address	800090070601143F (SCOM)
Description	This register contains the third set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H4E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H4O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL
Address	800090080601143F (SCOM)
Description	This register contains the third set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H4E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H4O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL
Address	800090090601143F (SCOM)
Description	This register contains the third set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H4E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H4O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL
Address	8000900A0601143F (SCOM)
Description	This register contains the third set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H4E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H4O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL
Address	8000900B0601143F (SCOM)
Description	This register contains the third set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H4E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H4O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL
Address	8000900C0601143F (SCOM)
Description	This register contains the third set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H4E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H4O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL
Address	8000900D0601143F (SCOM)
Description	This register contains the third set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H4E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H4O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL
Address	8000900E0601143F (SCOM)
Description	This register contains the third set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H4E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H4O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL
Address	8000900F0601143F (SCOM)
Description	This register contains the third set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H4E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H4O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	**Receive DAC Control 3 E Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL
Address	800090100601143F (SCOM)
Description	This register contains the third set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H4E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H4O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	**Receive DAC Control 3 E Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL
Address	800090110601143F (SCOM)
Description	This register contains the third set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H4E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H4O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	**Receive DAC Control 3 E Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL
Address	800090200601143F (SCOM)
Description	This register contains the third set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H4E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H4O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL
Address	800090210601143F (SCOM)
Description	This register contains the third set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H4E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H4O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL
Address	800090220601143F (SCOM)
Description	This register contains the third set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H4E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H4O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL
Address	800090230601143F (SCOM)
Description	This register contains the third set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H4E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H4O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL
Address	800090240601143F (SCOM)
Description	This register contains the third set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H4E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H4O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL
Address	800090250601143F (SCOM)
Description	This register contains the third set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H4E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H4O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL
Address	800090260601143F (SCOM)
Description	This register contains the third set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H4E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H4O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL
Address	800090270601143F (SCOM)
Description	This register contains the third set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H4E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H4O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL
Address	800090280601143F (SCOM)
Description	This register contains the third set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H4E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H4O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL
Address	800090290601143F (SCOM)
Description	This register contains the third set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H4E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H4O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL
Address	8000902A0601143F (SCOM)
Description	This register contains the third set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H4E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H4O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL
Address	8000902B0601143F (SCOM)
Description	This register contains the third set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H4E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H4O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL
Address	8000902C0601143F (SCOM)
Description	This register contains the third set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H4E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H4O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL
Address	8000902D0601143F (SCOM)
Description	This register contains the third set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H4E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H4O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL
Address	8000902E0601143F (SCOM)
Description	This register contains the third set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H4E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H4O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL
Address	8000902F0601143F (SCOM)
Description	This register contains the third set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H4E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H4O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL
Address	800090300601143F (SCOM)
Description	This register contains the third set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H4E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H4O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_E_PL
Address	800090310601143F (SCOM)
Description	This register contains the third set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H4E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H4O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 4 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL
Address	800098000601143F (SCOM)
Description	This register contains the fourth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H5E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H5O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 4 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL
Address	800098010601143F (SCOM)
Description	This register contains the fourth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H5E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H5O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 4 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL
Address	800098020601143F (SCOM)
Description	This register contains the fourth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H5E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H5O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 4 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL
Address	800098030601143F (SCOM)
Description	This register contains the fourth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H5E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H5O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 4 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL
Address	800098040601143F (SCOM)
Description	This register contains the fourth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H5E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H5O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 4 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL
Address	800098050601143F (SCOM)
Description	This register contains the fourth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H5E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H5O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 4 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL
Address	800098060601143F (SCOM)
Description	This register contains the fourth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H5E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H5O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 4 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL
Address	800098070601143F (SCOM)
Description	This register contains the fourth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H5E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H5O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 4 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL
Address	800098080601143F (SCOM)
Description	This register contains the fourth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H5E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H5O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 4 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL
Address	800098090601143F (SCOM)
Description	This register contains the fourth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H5E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H5O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 4 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL
Address	8000980A0601143F (SCOM)
Description	This register contains the fourth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H5E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H5O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 4 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL
Address	8000980B0601143F (SCOM)
Description	This register contains the fourth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H5E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H5O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 4 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL
Address	8000980C0601143F (SCOM)
Description	This register contains the fourth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H5E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H5O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 4 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL
Address	8000980D0601143F (SCOM)
Description	This register contains the fourth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H5E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H5O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 4 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL
Address	8000980E0601143F (SCOM)
Description	This register contains the fourth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H5E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H5O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 4 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL
Address	8000980F0601143F (SCOM)
Description	This register contains the fourth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H5E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H5O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 4 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL
Address	800098100601143F (SCOM)
Description	This register contains the fourth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H5E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H5O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 4 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL
Address	800098110601143F (SCOM)
Description	This register contains the fourth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H5E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H5O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 4 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL
Address	800098200601143F (SCOM)
Description	This register contains the fourth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H5E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H5O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 4 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL
Address	800098210601143F (SCOM)
Description	This register contains the fourth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H5E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H5O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 4 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL
Address	800098220601143F (SCOM)
Description	This register contains the fourth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H5E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H5O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 4 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL
Address	800098230601143F (SCOM)
Description	This register contains the fourth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H5E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H5O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 4 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL
Address	800098240601143F (SCOM)
Description	This register contains the fourth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H5E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H5O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 4 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL
Address	800098250601143F (SCOM)
Description	This register contains the fourth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H5E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H5O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 4 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL
Address	800098260601143F (SCOM)
Description	This register contains the fourth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H5E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H5O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 4 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL
Address	800098270601143F (SCOM)
Description	This register contains the fourth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H5E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H5O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 4 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL
Address	800098280601143F (SCOM)
Description	This register contains the fourth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H5E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H5O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 4 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL
Address	800098290601143F (SCOM)
Description	This register contains the fourth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H5E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H5O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 4 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL
Address	8000982A0601143F (SCOM)
Description	This register contains the fourth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H5E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H5O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 4 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL
Address	8000982B0601143F (SCOM)
Description	This register contains the fourth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H5E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H5O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 4 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL
Address	8000982C0601143F (SCOM)
Description	This register contains the fourth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H5E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H5O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 4 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL
Address	8000982D0601143F (SCOM)
Description	This register contains the fourth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H5E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H5O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 4 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL
Address	8000982E0601143F (SCOM)
Description	This register contains the fourth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H5E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H5O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 4 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL
Address	8000982F0601143F (SCOM)
Description	This register contains the fourth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H5E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H5O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 4 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL
Address	800098300601143F (SCOM)
Description	This register contains the fourth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H5E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H5O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 4 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_E_PL
Address	800098310601143F (SCOM)
Description	This register contains the fourth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H5E_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H5O_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 5 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL
Address	8000A0000601143F (SCOM)
Description	This register contains the fifth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H6_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H7_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 5 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL
Address	8000A0010601143F (SCOM)
Description	This register contains the fifth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H6_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H7_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 5 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL
Address	8000A0020601143F (SCOM)
Description	This register contains the fifth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H6_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H7_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 5 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL
Address	8000A0030601143F (SCOM)
Description	This register contains the fifth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H6_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H7_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 5 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL
Address	8000A0040601143F (SCOM)
Description	This register contains the fifth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H6_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H7_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 5 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL
Address	8000A0050601143F (SCOM)
Description	This register contains the fifth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H6_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H7_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 5 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL
Address	8000A0060601143F (SCOM)
Description	This register contains the fifth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H6_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H7_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 5 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL
Address	8000A0070601143F (SCOM)
Description	This register contains the fifth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H6_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H7_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 5 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL
Address	8000A0080601143F (SCOM)
Description	This register contains the fifth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H6_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H7_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 5 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL
Address	8000A0090601143F (SCOM)
Description	This register contains the fifth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H6_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H7_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 5 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL
Address	8000A00A0601143F (SCOM)
Description	This register contains the fifth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H6_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H7_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 5 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL
Address	8000A00B0601143F (SCOM)
Description	This register contains the fifth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H6_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H7_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 5 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL
Address	8000A00C0601143F (SCOM)
Description	This register contains the fifth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H6_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H7_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	**Receive DAC Control 5 E Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL
Address	8000A00D0601143F (SCOM)
Description	This register contains the fifth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H6_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H7_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	**Receive DAC Control 5 E Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL
Address	8000A00E0601143F (SCOM)
Description	This register contains the fifth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H6_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H7_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	**Receive DAC Control 5 E Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL
Address	8000A00F0601143F (SCOM)
Description	This register contains the fifth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H6_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H7_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 5 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL
Address	8000A0100601143F (SCOM)
Description	This register contains the fifth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H6_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H7_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 5 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL
Address	8000A0110601143F (SCOM)
Description	This register contains the fifth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H6_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H7_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 5 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL
Address	8000A0200601143F (SCOM)
Description	This register contains the fifth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H6_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H7_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 5 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL
Address	8000A0210601143F (SCOM)
Description	This register contains the fifth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H6_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H7_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 5 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL
Address	8000A0220601143F (SCOM)
Description	This register contains the fifth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H6_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H7_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 5 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL
Address	8000A0230601143F (SCOM)
Description	This register contains the fifth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H6_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H7_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	**Receive DAC Control 5 E Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL
Address	8000A0240601143F (SCOM)
Description	This register contains the fifth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H6_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H7_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	**Receive DAC Control 5 E Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL
Address	8000A0250601143F (SCOM)
Description	This register contains the fifth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H6_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H7_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	**Receive DAC Control 5 E Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL
Address	8000A0260601143F (SCOM)
Description	This register contains the fifth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H6_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H7_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 5 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL
Address	8000A0270601143F (SCOM)
Description	This register contains the fifth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H6_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H7_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 5 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL
Address	8000A0280601143F (SCOM)
Description	This register contains the fifth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H6_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H7_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 5 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL
Address	8000A0290601143F (SCOM)
Description	This register contains the fifth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H6_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H7_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 5 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL
Address	8000A02A0601143F (SCOM)
Description	This register contains the fifth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H6_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H7_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 5 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL
Address	8000A02B0601143F (SCOM)
Description	This register contains the fifth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H6_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H7_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 5 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL
Address	8000A02C0601143F (SCOM)
Description	This register contains the fifth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H6_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H7_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 5 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL
Address	8000A02D0601143F (SCOM)
Description	This register contains the fifth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H6_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H7_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 5 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL
Address	8000A02E0601143F (SCOM)
Description	This register contains the fifth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H6_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H7_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 5 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL
Address	8000A02F0601143F (SCOM)
Description	This register contains the fifth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H6_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H7_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 5 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL
Address	8000A0300601143F (SCOM)
Description	This register contains the fifth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H6_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H7_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 5 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_E_PL
Address	8000A0310601143F (SCOM)
Description	This register contains the fifth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H6_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H7_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 6 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL
Address	8000A8000601143F (SCOM)
Description	This register contains the sixth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H8_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H9_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 6 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL
Address	8000A8010601143F (SCOM)
Description	This register contains the sixth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H8_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H9_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 6 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL
Address	8000A8020601143F (SCOM)
Description	This register contains the sixth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H8_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H9_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 6 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL
Address	8000A8030601143F (SCOM)
Description	This register contains the sixth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H8_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H9_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 6 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL
Address	8000A8040601143F (SCOM)
Description	This register contains the sixth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H8_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H9_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 6 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL
Address	8000A8050601143F (SCOM)
Description	This register contains the sixth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H8_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H9_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 6 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL
Address	8000A8060601143F (SCOM)
Description	This register contains the sixth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H8_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H9_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 6 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL
Address	8000A8070601143F (SCOM)
Description	This register contains the sixth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H8_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H9_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 6 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL
Address	8000A8080601143F (SCOM)
Description	This register contains the sixth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H8_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H9_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 6 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL
Address	8000A8090601143F (SCOM)
Description	This register contains the sixth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H8_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H9_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 6 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL
Address	8000A80A0601143F (SCOM)
Description	This register contains the sixth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H8_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H9_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 6 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL
Address	8000A80B0601143F (SCOM)
Description	This register contains the sixth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H8_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H9_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 6 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL
Address	8000A80C0601143F (SCOM)
Description	This register contains the sixth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H8_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H9_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 6 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL
Address	8000A80D0601143F (SCOM)
Description	This register contains the sixth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H8_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H9_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 6 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL
Address	8000A80E0601143F (SCOM)
Description	This register contains the sixth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H8_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H9_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 6 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL
Address	8000A80F0601143F (SCOM)
Description	This register contains the sixth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H8_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H9_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	**Receive DAC Control 6 E Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL
Address	8000A8100601143F (SCOM)
Description	This register contains the sixth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H8_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H9_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	**Receive DAC Control 6 E Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL
Address	8000A8110601143F (SCOM)
Description	This register contains the sixth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H8_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H9_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	**Receive DAC Control 6 E Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL
Address	8000A8200601143F (SCOM)
Description	This register contains the sixth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H8_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H9_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 6 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL
Address	8000A8210601143F (SCOM)
Description	This register contains the sixth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H8_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H9_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 6 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL
Address	8000A8220601143F (SCOM)
Description	This register contains the sixth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H8_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H9_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 6 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL
Address	8000A8230601143F (SCOM)
Description	This register contains the sixth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H8_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H9_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 6 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL
Address	8000A8240601143F (SCOM)
Description	This register contains the sixth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H8_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H9_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 6 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL
Address	8000A8250601143F (SCOM)
Description	This register contains the sixth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H8_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H9_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 6 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL
Address	8000A8260601143F (SCOM)
Description	This register contains the sixth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H8_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H9_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 6 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL
Address	8000A8270601143F (SCOM)
Description	This register contains the sixth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H8_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H9_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 6 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL
Address	8000A8280601143F (SCOM)
Description	This register contains the sixth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H8_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H9_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 6 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL
Address	8000A8290601143F (SCOM)
Description	This register contains the sixth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H8_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H9_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 6 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL
Address	8000A82A0601143F (SCOM)
Description	This register contains the sixth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H8_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H9_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 6 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL
Address	8000A82B0601143F (SCOM)
Description	This register contains the sixth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H8_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H9_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 6 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL
Address	8000A82C0601143F (SCOM)
Description	This register contains the sixth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H8_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H9_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 6 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL
Address	8000A82D0601143F (SCOM)
Description	This register contains the sixth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H8_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H9_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 6 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL
Address	8000A82E0601143F (SCOM)
Description	This register contains the sixth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H8_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H9_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 6 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL
Address	8000A82F0601143F (SCOM)
Description	This register contains the sixth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H8_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H9_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 6 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL
Address	8000A8300601143F (SCOM)
Description	This register contains the sixth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H8_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H9_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 6 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_E_PL
Address	8000A8310601143F (SCOM)
Description	This register contains the sixth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H8_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H9_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 7 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL
Address	8000B0000601143F (SCOM)
Description	This register contains the seventh set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H10_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H11_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	**Receive DAC Control 7 E Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL
Address	8000B0010601143F (SCOM)
Description	This register contains the seventh set of E DAC controls.

Bits	**SCOM**	**Field Mnemonic: Description**
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H10_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H11_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	**Receive DAC Control 7 E Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL
Address	8000B0020601143F (SCOM)
Description	This register contains the seventh set of E DAC controls.

Bits	**SCOM**	**Field Mnemonic: Description**
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H10_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H11_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	**Receive DAC Control 7 E Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL
Address	8000B0030601143F (SCOM)
Description	This register contains the seventh set of E DAC controls.

Bits	**SCOM**	**Field Mnemonic: Description**
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H10_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H11_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 7 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL
Address	8000B0040601143F (SCOM)
Description	This register contains the seventh set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H10_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H11_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 7 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL
Address	8000B0050601143F (SCOM)
Description	This register contains the seventh set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H10_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H11_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 7 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL
Address	8000B0060601143F (SCOM)
Description	This register contains the seventh set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H10_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H11_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 7 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL
Address	8000B0070601143F (SCOM)
Description	This register contains the seventh set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H10_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H11_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 7 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL
Address	8000B0080601143F (SCOM)
Description	This register contains the seventh set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H10_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H11_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 7 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL
Address	8000B0090601143F (SCOM)
Description	This register contains the seventh set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H10_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H11_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 7 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL
Address	8000B00A0601143F (SCOM)
Description	This register contains the seventh set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H10_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H11_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 7 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL
Address	8000B00B0601143F (SCOM)
Description	This register contains the seventh set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H10_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H11_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 7 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL
Address	8000B00C0601143F (SCOM)
Description	This register contains the seventh set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H10_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H11_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 7 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL
Address	8000B00D0601143F (SCOM)
Description	This register contains the seventh set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H10_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H11_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 7 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL
Address	8000B00E0601143F (SCOM)
Description	This register contains the seventh set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H10_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H11_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 7 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL
Address	8000B00F0601143F (SCOM)
Description	This register contains the seventh set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H10_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H11_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 7 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL
Address	8000B0100601143F (SCOM)
Description	This register contains the seventh set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H10_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H11_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 7 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL
Address	8000B0110601143F (SCOM)
Description	This register contains the seventh set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H10_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H11_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 7 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL
Address	8000B0200601143F (SCOM)
Description	This register contains the seventh set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H10_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H11_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 7 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL
Address	8000B0210601143F (SCOM)
Description	This register contains the seventh set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H10_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H11_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 7 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL
Address	8000B0220601143F (SCOM)
Description	This register contains the seventh set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H10_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H11_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 7 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL
Address	8000B0230601143F (SCOM)
Description	This register contains the seventh set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H10_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H11_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 7 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL
Address	8000B0240601143F (SCOM)
Description	This register contains the seventh set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H10_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H11_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 7 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL
Address	8000B0250601143F (SCOM)
Description	This register contains the seventh set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H10_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H11_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 7 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL
Address	8000B0260601143F (SCOM)
Description	This register contains the seventh set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H10_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H11_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 7 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL
Address	8000B0270601143F (SCOM)
Description	This register contains the seventh set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H10_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H11_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 7 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL
Address	8000B0280601143F (SCOM)
Description	This register contains the seventh set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H10_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H11_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 7 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL
Address	8000B0290601143F (SCOM)
Description	This register contains the seventh set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H10_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H11_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 7 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL
Address	8000B02A0601143F (SCOM)
Description	This register contains the seventh set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H10_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H11_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 7 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL
Address	8000B02B0601143F (SCOM)
Description	This register contains the seventh set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H10_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H11_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 7 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL
Address	8000B02C0601143F (SCOM)
Description	This register contains the seventh set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H10_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H11_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 7 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL
Address	8000B02D0601143F (SCOM)
Description	This register contains the seventh set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H10_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H11_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 7 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL
Address	8000B02E0601143F (SCOM)
Description	This register contains the seventh set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H10_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H11_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 7 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL
Address	8000B02F0601143F (SCOM)
Description	This register contains the seventh set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H10_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H11_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 7 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL
Address	8000B0300601143F (SCOM)
Description	This register contains the seventh set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H10_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H11_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 7 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_E_PL
Address	8000B0310601143F (SCOM)
Description	This register contains the seventh set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H10_VAL: This field contains the DFE H1 value for even sampler 1.
53:55	RO	constant = 0b000
56:60	RWX	RX_A_H11_VAL: This field contains the DFE H1 value for even sampler 0.
61:63	RO	constant = 0b000

Register Name	Receive DAC Control 8 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL
Address	8000B8000601143F (SCOM)
Description	This register contains the eighth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H12_VAL: This field contains the DFE H1 value for even sampler 0.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 8 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL
Address	8000B8010601143F (SCOM)
Description	This register contains the eighth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H12_VAL: This field contains the DFE H1 value for even sampler 0.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 8 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL
Address	8000B8020601143F (SCOM)
Description	This register contains the eighth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H12_VAL: This field contains the DFE H1 value for even sampler 0.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 8 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL
Address	8000B8030601143F (SCOM)
Description	This register contains the eighth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H12_VAL: This field contains the DFE H1 value for even sampler 0.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 8 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL
Address	8000B8040601143F (SCOM)
Description	This register contains the eighth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H12_VAL: This field contains the DFE H1 value for even sampler 0.

Bits	SCOM	Field Mnemonic: Description
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 8 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL
Address	8000B8050601143F (SCOM)
Description	This register contains the eighth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H12_VAL: This field contains the DFE H1 value for even sampler 0.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 8 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL
Address	8000B8060601143F (SCOM)
Description	This register contains the eighth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H12_VAL: This field contains the DFE H1 value for even sampler 0.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 8 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL
Address	8000B8070601143F (SCOM)
Description	This register contains the eighth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H12_VAL: This field contains the DFE H1 value for even sampler 0.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 8 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL
Address	8000B8080601143F (SCOM)
Description	This register contains the eighth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H12_VAL: This field contains the DFE H1 value for even sampler 0.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 8 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL
Address	8000B8090601143F (SCOM)
Description	This register contains the eighth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H12_VAL: This field contains the DFE H1 value for even sampler 0.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 8 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL
Address	8000B80A0601143F (SCOM)
Description	This register contains the eighth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H12_VAL: This field contains the DFE H1 value for even sampler 0.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 8 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL
Address	8000B80B0601143F (SCOM)
Description	This register contains the eighth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H12_VAL: This field contains the DFE H1 value for even sampler 0.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 8 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL
Address	8000B80C0601143F (SCOM)
Description	This register contains the eighth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H12_VAL: This field contains the DFE H1 value for even sampler 0.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 8 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL
Address	8000B80D0601143F (SCOM)
Description	This register contains the eighth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H12_VAL: This field contains the DFE H1 value for even sampler 0.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 8 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL
Address	8000B80E0601143F (SCOM)
Description	This register contains the eighth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H12_VAL: This field contains the DFE H1 value for even sampler 0.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 8 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL
Address	8000B80F0601143F (SCOM)
Description	This register contains the eighth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H12_VAL: This field contains the DFE H1 value for even sampler 0.

Bits	SCOM	Field Mnemonic: Description
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 8 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL
Address	8000B8100601143F (SCOM)
Description	This register contains the eighth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H12_VAL: This field contains the DFE H1 value for even sampler 0.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 8 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL
Address	8000B8110601143F (SCOM)
Description	This register contains the eighth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H12_VAL: This field contains the DFE H1 value for even sampler 0.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 8 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL
Address	8000B8200601143F (SCOM)
Description	This register contains the eighth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H12_VAL: This field contains the DFE H1 value for even sampler 0.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 8 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL
Address	8000B8210601143F (SCOM)
Description	This register contains the eighth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H12_VAL: This field contains the DFE H1 value for even sampler 0.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 8 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL
Address	8000B8220601143F (SCOM)
Description	This register contains the eighth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H12_VAL: This field contains the DFE H1 value for even sampler 0.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 8 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL
Address	8000B8230601143F (SCOM)
Description	This register contains the eighth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H12_VAL: This field contains the DFE H1 value for even sampler 0.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 8 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL
Address	8000B8240601143F (SCOM)
Description	This register contains the eighth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H12_VAL: This field contains the DFE H1 value for even sampler 0.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 8 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL
Address	8000B8250601143F (SCOM)
Description	This register contains the eighth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H12_VAL: This field contains the DFE H1 value for even sampler 0.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 8 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL
Address	8000B8260601143F (SCOM)
Description	This register contains the eighth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H12_VAL: This field contains the DFE H1 value for even sampler 0.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 8 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL
Address	8000B8270601143F (SCOM)
Description	This register contains the eighth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H12_VAL: This field contains the DFE H1 value for even sampler 0.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 8 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL
Address	8000B8280601143F (SCOM)
Description	This register contains the eighth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H12_VAL: This field contains the DFE H1 value for even sampler 0.

Bits	SCOM	Field Mnemonic: Description
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 8 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL
Address	8000B8290601143F (SCOM)
Description	This register contains the eighth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H12_VAL: This field contains the DFE H1 value for even sampler 0.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 8 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL
Address	8000B82A0601143F (SCOM)
Description	This register contains the eighth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H12_VAL: This field contains the DFE H1 value for even sampler 0.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 8 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL
Address	8000B82B0601143F (SCOM)
Description	This register contains the eighth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H12_VAL: This field contains the DFE H1 value for even sampler 0.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 8 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL
Address	8000B82C0601143F (SCOM)
Description	This register contains the eighth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H12_VAL: This field contains the DFE H1 value for even sampler 0.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 8 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL
Address	8000B82D0601143F (SCOM)
Description	This register contains the eighth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H12_VAL: This field contains the DFE H1 value for even sampler 0.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 8 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL
Address	8000B82E0601143F (SCOM)
Description	This register contains the eighth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H12_VAL: This field contains the DFE H1 value for even sampler 0.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 8 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL
Address	8000B82F0601143F (SCOM)
Description	This register contains the eighth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H12_VAL: This field contains the DFE H1 value for even sampler 0.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 8 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL
Address	8000B8300601143F (SCOM)
Description	This register contains the eighth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H12_VAL: This field contains the DFE H1 value for even sampler 0.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 8 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_E_PL
Address	8000B8310601143F (SCOM)
Description	This register contains the eighth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_A_H12_VAL: This field contains the DFE H1 value for even sampler 0.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 9 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL
Address	8000C0000601143F (SCOM)
Description	This register contains the ninth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1ARATIO_VAL: This field feeds the DAC that is used to make the H1 DAC and offset DAC match the rest of the DACs.
55:60	RWX	RX_A_H1CAL_VAL: This field feeds the DAC that is used to make the H1 DAC match a precision reference current.
61	RWX	RX_A_H1CAL_EN: This field goes to the analog to set its circuits in a mode for calibrating the H1 DAC.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL
Address	8000C0010601143F (SCOM)
Description	This register contains the ninth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1ARATIO_VAL: This field feeds the DAC that is used to make the H1 DAC and offset DAC match the rest of the DACs.
55:60	RWX	RX_A_H1CAL_VAL: This field feeds the DAC that is used to make the H1 DAC match a precision reference current.
61	RWX	RX_A_H1CAL_EN: This field goes to the analog to set its circuits in a mode for calibrating the H1 DAC.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL
Address	8000C0020601143F (SCOM)
Description	This register contains the ninth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1ARATIO_VAL: This field feeds the DAC that is used to make the H1 DAC and offset DAC match the rest of the DACs.
55:60	RWX	RX_A_H1CAL_VAL: This field feeds the DAC that is used to make the H1 DAC match a precision reference current.
61	RWX	RX_A_H1CAL_EN: This field goes to the analog to set its circuits in a mode for calibrating the H1 DAC.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL
Address	8000C0030601143F (SCOM)
Description	This register contains the ninth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1ARATIO_VAL: This field feeds the DAC that is used to make the H1 DAC and offset DAC match the rest of the DACs.
55:60	RWX	RX_A_H1CAL_VAL: This field feeds the DAC that is used to make the H1 DAC match a precision reference current.
61	RWX	RX_A_H1CAL_EN: This field goes to the analog to set its circuits in a mode for calibrating the H1 DAC.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL
Address	8000C0040601143F (SCOM)
Description	This register contains the ninth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1ARATIO_VAL: This field feeds the DAC that is used to make the H1 DAC and offset DAC match the rest of the DACs.
55:60	RWX	RX_A_H1CAL_VAL: This field feeds the DAC that is used to make the H1 DAC match a precision reference current.
61	RWX	RX_A_H1CAL_EN: This field goes to the analog to set its circuits in a mode for calibrating the H1 DAC.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL
Address	8000C0050601143F (SCOM)
Description	This register contains the ninth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1ARATIO_VAL: This field feeds the DAC that is used to make the H1 DAC and offset DAC match the rest of the DACs.
55:60	RWX	RX_A_H1CAL_VAL: This field feeds the DAC that is used to make the H1 DAC match a precision reference current.
61	RWX	RX_A_H1CAL_EN: This field goes to the analog to set its circuits in a mode for calibrating the H1 DAC.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL
Address	8000C0060601143F (SCOM)
Description	This register contains the ninth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1ARATIO_VAL: This field feeds the DAC that is used to make the H1 DAC and offset DAC match the rest of the DACs.
55:60	RWX	RX_A_H1CAL_VAL: This field feeds the DAC that is used to make the H1 DAC match a precision reference current.
61	RWX	RX_A_H1CAL_EN: This field goes to the analog to set its circuits in a mode for calibrating the H1 DAC.
62:63	RO	constant = 0b00

Register Name	**Receive DAC Control 9 E Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL
Address	8000C0070601143F (SCOM)
Description	This register contains the ninth set of E DAC controls.

Bits	**SCOM**	**Field Mnemonic: Description**
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1ARATIO_VAL: This field feeds the DAC that is used to make the H1 DAC and offset DAC match the rest of the DACs.
55:60	RWX	RX_A_H1CAL_VAL: This field feeds the DAC that is used to make the H1 DAC match a precision reference current.
61	RWX	RX_A_H1CAL_EN: This field goes to the analog to set its circuits in a mode for calibrating the H1 DAC.
62:63	RO	constant = 0b00

Register Name	**Receive DAC Control 9 E Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL
Address	8000C0080601143F (SCOM)
Description	This register contains the ninth set of E DAC controls.

Bits	**SCOM**	**Field Mnemonic: Description**
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1ARATIO_VAL: This field feeds the DAC that is used to make the H1 DAC and offset DAC match the rest of the DACs.
55:60	RWX	RX_A_H1CAL_VAL: This field feeds the DAC that is used to make the H1 DAC match a precision reference current.
61	RWX	RX_A_H1CAL_EN: This field goes to the analog to set its circuits in a mode for calibrating the H1 DAC.
62:63	RO	constant = 0b00

Register Name	**Receive DAC Control 9 E Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL
Address	8000C0090601143F (SCOM)
Description	This register contains the ninth set of E DAC controls.

Bits	**SCOM**	**Field Mnemonic: Description**
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1ARATIO_VAL: This field feeds the DAC that is used to make the H1 DAC and offset DAC match the rest of the DACs.
55:60	RWX	RX_A_H1CAL_VAL: This field feeds the DAC that is used to make the H1 DAC match a precision reference current.
61	RWX	RX_A_H1CAL_EN: This field goes to the analog to set its circuits in a mode for calibrating the H1 DAC.

Bits	SCOM	Field Mnemonic: Description
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL
Address	8000C00A0601143F (SCOM)
Description	This register contains the ninth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1ARATIO_VAL: This field feeds the DAC that is used to make the H1 DAC and offset DAC match the rest of the DACs.
55:60	RWX	RX_A_H1CAL_VAL: This field feeds the DAC that is used to make the H1 DAC match a precision reference current.
61	RWX	RX_A_H1CAL_EN: This field goes to the analog to set its circuits in a mode for calibrating the H1 DAC.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL
Address	8000C00B0601143F (SCOM)
Description	This register contains the ninth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1ARATIO_VAL: This field feeds the DAC that is used to make the H1 DAC and offset DAC match the rest of the DACs.
55:60	RWX	RX_A_H1CAL_VAL: This field feeds the DAC that is used to make the H1 DAC match a precision reference current.
61	RWX	RX_A_H1CAL_EN: This field goes to the analog to set its circuits in a mode for calibrating the H1 DAC.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL
Address	8000C00C0601143F (SCOM)
Description	This register contains the ninth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1ARATIO_VAL: This field feeds the DAC that is used to make the H1 DAC and offset DAC match the rest of the DACs.

Bits	SCOM	Field Mnemonic: Description
55:60	RWX	RX_A_H1CAL_VAL: This field feeds the DAC that is used to make the H1 DAC match a precision reference current.
61	RWX	RX_A_H1CAL_EN: This field goes to the analog to set its circuits in a mode for calibrating the H1 DAC.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL
Address	8000C00D0601143F (SCOM)
Description	This register contains the ninth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1ARATIO_VAL: This field feeds the DAC that is used to make the H1 DAC and offset DAC match the rest of the DACs.
55:60	RWX	RX_A_H1CAL_VAL: This field feeds the DAC that is used to make the H1 DAC match a precision reference current.
61	RWX	RX_A_H1CAL_EN: This field goes to the analog to set its circuits in a mode for calibrating the H1 DAC.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL
Address	8000C00E0601143F (SCOM)
Description	This register contains the ninth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1ARATIO_VAL: This field feeds the DAC that is used to make the H1 DAC and offset DAC match the rest of the DACs.
55:60	RWX	RX_A_H1CAL_VAL: This field feeds the DAC that is used to make the H1 DAC match a precision reference current.
61	RWX	RX_A_H1CAL_EN: This field goes to the analog to set its circuits in a mode for calibrating the H1 DAC.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL
Address	8000C00F0601143F (SCOM)
Description	This register contains the ninth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1ARATIO_VAL: This field feeds the DAC that is used to make the H1 DAC and offset DAC match the rest of the DACs.
55:60	RWX	RX_A_H1CAL_VAL: This field feeds the DAC that is used to make the H1 DAC match a precision reference current.
61	RWX	RX_A_H1CAL_EN: This field goes to the analog to set its circuits in a mode for calibrating the H1 DAC.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL
Address	8000C0100601143F (SCOM)
Description	This register contains the ninth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1ARATIO_VAL: This field feeds the DAC that is used to make the H1 DAC and offset DAC match the rest of the DACs.
55:60	RWX	RX_A_H1CAL_VAL: This field feeds the DAC that is used to make the H1 DAC match a precision reference current.
61	RWX	RX_A_H1CAL_EN: This field goes to the analog to set its circuits in a mode for calibrating the H1 DAC.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL
Address	8000C0110601143F (SCOM)
Description	This register contains the ninth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1ARATIO_VAL: This field feeds the DAC that is used to make the H1 DAC and offset DAC match the rest of the DACs.
55:60	RWX	RX_A_H1CAL_VAL: This field feeds the DAC that is used to make the H1 DAC match a precision reference current.
61	RWX	RX_A_H1CAL_EN: This field goes to the analog to set its circuits in a mode for calibrating the H1 DAC.
62:63	RO	constant = 0b00

Register Name	**Receive DAC Control 9 E Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL
Address	8000C0200601143F (SCOM)
Description	This register contains the ninth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1ARATIO_VAL: This field feeds the DAC that is used to make the H1 DAC and offset DAC match the rest of the DACs.
55:60	RWX	RX_A_H1CAL_VAL: This field feeds the DAC that is used to make the H1 DAC match a precision reference current.
61	RWX	RX_A_H1CAL_EN: This field goes to the analog to set its circuits in a mode for calibrating the H1 DAC.
62:63	RO	constant = 0b00

Register Name	**Receive DAC Control 9 E Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL
Address	8000C0210601143F (SCOM)
Description	This register contains the ninth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1ARATIO_VAL: This field feeds the DAC that is used to make the H1 DAC and offset DAC match the rest of the DACs.
55:60	RWX	RX_A_H1CAL_VAL: This field feeds the DAC that is used to make the H1 DAC match a precision reference current.
61	RWX	RX_A_H1CAL_EN: This field goes to the analog to set its circuits in a mode for calibrating the H1 DAC.
62:63	RO	constant = 0b00

Register Name	**Receive DAC Control 9 E Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL
Address	8000C0220601143F (SCOM)
Description	This register contains the ninth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1ARATIO_VAL: This field feeds the DAC that is used to make the H1 DAC and offset DAC match the rest of the DACs.
55:60	RWX	RX_A_H1CAL_VAL: This field feeds the DAC that is used to make the H1 DAC match a precision reference current.
61	RWX	RX_A_H1CAL_EN: This field goes to the analog to set its circuits in a mode for calibrating the H1 DAC.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL
Address	8000C0230601143F (SCOM)
Description	This register contains the ninth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1ARATIO_VAL: This field feeds the DAC that is used to make the H1 DAC and offset DAC match the rest of the DACs.
55:60	RWX	RX_A_H1CAL_VAL: This field feeds the DAC that is used to make the H1 DAC match a precision reference current.
61	RWX	RX_A_H1CAL_EN: This field goes to the analog to set its circuits in a mode for calibrating the H1 DAC.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL
Address	8000C0240601143F (SCOM)
Description	This register contains the ninth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1ARATIO_VAL: This field feeds the DAC that is used to make the H1 DAC and offset DAC match the rest of the DACs.
55:60	RWX	RX_A_H1CAL_VAL: This field feeds the DAC that is used to make the H1 DAC match a precision reference current.
61	RWX	RX_A_H1CAL_EN: This field goes to the analog to set its circuits in a mode for calibrating the H1 DAC.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL
Address	8000C0250601143F (SCOM)
Description	This register contains the ninth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1ARATIO_VAL: This field feeds the DAC that is used to make the H1 DAC and offset DAC match the rest of the DACs.
55:60	RWX	RX_A_H1CAL_VAL: This field feeds the DAC that is used to make the H1 DAC match a precision reference current.
61	RWX	RX_A_H1CAL_EN: This field goes to the analog to set its circuits in a mode for calibrating the H1 DAC.

Bits	SCOM	Field Mnemonic: Description
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL
Address	8000C0260601143F (SCOM)
Description	This register contains the ninth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1ARATIO_VAL: This field feeds the DAC that is used to make the H1 DAC and offset DAC match the rest of the DACs.
55:60	RWX	RX_A_H1CAL_VAL: This field feeds the DAC that is used to make the H1 DAC match a precision reference current.
61	RWX	RX_A_H1CAL_EN: This field goes to the analog to set its circuits in a mode for calibrating the H1 DAC.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL
Address	8000C0270601143F (SCOM)
Description	This register contains the ninth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1ARATIO_VAL: This field feeds the DAC that is used to make the H1 DAC and offset DAC match the rest of the DACs.
55:60	RWX	RX_A_H1CAL_VAL: This field feeds the DAC that is used to make the H1 DAC match a precision reference current.
61	RWX	RX_A_H1CAL_EN: This field goes to the analog to set its circuits in a mode for calibrating the H1 DAC.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL
Address	8000C0280601143F (SCOM)
Description	This register contains the ninth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1ARATIO_VAL: This field feeds the DAC that is used to make the H1 DAC and offset DAC match the rest of the DACs.

Bits	SCOM	Field Mnemonic: Description
55:60	RWX	RX_A_H1CAL_VAL: This field feeds the DAC that is used to make the H1 DAC match a precision reference current.
61	RWX	RX_A_H1CAL_EN: This field goes to the analog to set its circuits in a mode for calibrating the H1 DAC.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL
Address	8000C0290601143F (SCOM)
Description	This register contains the ninth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1ARATIO_VAL: This field feeds the DAC that is used to make the H1 DAC and offset DAC match the rest of the DACs.
55:60	RWX	RX_A_H1CAL_VAL: This field feeds the DAC that is used to make the H1 DAC match a precision reference current.
61	RWX	RX_A_H1CAL_EN: This field goes to the analog to set its circuits in a mode for calibrating the H1 DAC.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL
Address	8000C02A0601143F (SCOM)
Description	This register contains the ninth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1ARATIO_VAL: This field feeds the DAC that is used to make the H1 DAC and offset DAC match the rest of the DACs.
55:60	RWX	RX_A_H1CAL_VAL: This field feeds the DAC that is used to make the H1 DAC match a precision reference current.
61	RWX	RX_A_H1CAL_EN: This field goes to the analog to set its circuits in a mode for calibrating the H1 DAC.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL
Address	8000C02B0601143F (SCOM)
Description	This register contains the ninth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1ARATIO_VAL: This field feeds the DAC that is used to make the H1 DAC and offset DAC match the rest of the DACs.
55:60	RWX	RX_A_H1CAL_VAL: This field feeds the DAC that is used to make the H1 DAC match a precision reference current.
61	RWX	RX_A_H1CAL_EN: This field goes to the analog to set its circuits in a mode for calibrating the H1 DAC.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL
Address	8000C02C0601143F (SCOM)
Description	This register contains the ninth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1ARATIO_VAL: This field feeds the DAC that is used to make the H1 DAC and offset DAC match the rest of the DACs.
55:60	RWX	RX_A_H1CAL_VAL: This field feeds the DAC that is used to make the H1 DAC match a precision reference current.
61	RWX	RX_A_H1CAL_EN: This field goes to the analog to set its circuits in a mode for calibrating the H1 DAC.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL
Address	8000C02D0601143F (SCOM)
Description	This register contains the ninth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1ARATIO_VAL: This field feeds the DAC that is used to make the H1 DAC and offset DAC match the rest of the DACs.
55:60	RWX	RX_A_H1CAL_VAL: This field feeds the DAC that is used to make the H1 DAC match a precision reference current.
61	RWX	RX_A_H1CAL_EN: This field goes to the analog to set its circuits in a mode for calibrating the H1 DAC.
62:63	RO	constant = 0b00

Register Name	**Receive DAC Control 9 E Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL
Address	8000C02E0601143F (SCOM)
Description	This register contains the ninth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1ARATIO_VAL: This field feeds the DAC that is used to make the H1 DAC and offset DAC match the rest of the DACs.
55:60	RWX	RX_A_H1CAL_VAL: This field feeds the DAC that is used to make the H1 DAC match a precision reference current.
61	RWX	RX_A_H1CAL_EN: This field goes to the analog to set its circuits in a mode for calibrating the H1 DAC.
62:63	RO	constant = 0b00

Register Name	**Receive DAC Control 9 E Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL
Address	8000C02F0601143F (SCOM)
Description	This register contains the ninth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1ARATIO_VAL: This field feeds the DAC that is used to make the H1 DAC and offset DAC match the rest of the DACs.
55:60	RWX	RX_A_H1CAL_VAL: This field feeds the DAC that is used to make the H1 DAC match a precision reference current.
61	RWX	RX_A_H1CAL_EN: This field goes to the analog to set its circuits in a mode for calibrating the H1 DAC.
62:63	RO	constant = 0b00

Register Name	**Receive DAC Control 9 E Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL
Address	8000C0300601143F (SCOM)
Description	This register contains the ninth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1ARATIO_VAL: This field feeds the DAC that is used to make the H1 DAC and offset DAC match the rest of the DACs.
55:60	RWX	RX_A_H1CAL_VAL: This field feeds the DAC that is used to make the H1 DAC match a precision reference current.
61	RWX	RX_A_H1CAL_EN: This field goes to the analog to set its circuits in a mode for calibrating the H1 DAC.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_E_PL
Address	8000C0310601143F (SCOM)
Description	This register contains the ninth set of E DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1ARATIO_VAL: This field feeds the DAC that is used to make the H1 DAC and offset DAC match the rest of the DACs.
55:60	RWX	RX_A_H1CAL_VAL: This field feeds the DAC that is used to make the H1 DAC match a precision reference current.
61	RWX	RX_A_H1CAL_EN: This field goes to the analog to set its circuits in a mode for calibrating the H1 DAC.
62:63	RO	constant = 0b00

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	800200000601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	800200010601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Spare Mode Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	800200020601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Spare Mode Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	800200030601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	800200040601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	800200050601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	800200060601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	800200070601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	800200080601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	800200090601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	8002000A0601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	8002000B0601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	8002000C0601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Spare Mode Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	8002000D0601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Spare Mode Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	8002000E0601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Spare Mode Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	8002000F0601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	800200100601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	800200110601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	800200200601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	800200210601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Spare Mode Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	800200220601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Spare Mode Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	800200230601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Spare Mode Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	800200240601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	800200250601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	800200260601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	800200270601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	800200280601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Spare Mode Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	800200290601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	**SCOM**	**Field Mnemonic: Description**
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Spare Mode Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	8002002A0601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	**SCOM**	**Field Mnemonic: Description**
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Spare Mode Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	8002002B0601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	8002002C0601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	8002002D0601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	8002002E0601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	8002002F0601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	800200300601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	800200310601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_FIR_PL
Address	800208000601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_FIR_PL
Address	800208010601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_PL
Address	800208020601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_PL
Address	800208030601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_PL
Address	800208040601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_PL
Address	800208050601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_PL
Address	800208060601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_PL
Address	800208070601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_PL
Address	800208080601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_PL
Address	800208090601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_PL
Address	8002080A0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_PL
Address	8002080B0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_PL
Address	8002080C0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_PL
Address	8002080D0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_PL
Address	8002080E0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_PL
Address	8002080F0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_PL
Address	800208100601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_PL
Address	800208110601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_PL
Address	800208200601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_PL
Address	800208210601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_PL
Address	800208220601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	**Receive FIR Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_PL
Address	800208230601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	**Receive FIR Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_PL
Address	800208240601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	**Receive FIR Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_PL
Address	800208250601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	**Receive FIR Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_PL
Address	800208260601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_PL
Address	800208270601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_PL
Address	800208280601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_PL
Address	800208290601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_PL
Address	8002082A0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_PL
Address	8002082B0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_PL
Address	8002082C0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_PL
Address	8002082D0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_PL
Address	8002082E0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_FIR_PL
Address	8002082F0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_FIR_PL
Address	800208300601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_PL
Address	800208310601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	800210000601143F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	800210010601143F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	800210020601143F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	800210030601143F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	800210040601143F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	800210050601143F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	800210060601143F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	800210070601143F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	800210080601143F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	800210090601143F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8002100A0601143F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8002100B0601143F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8002100C0601143F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8002100D0601143F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8002100E0601143F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8002100F0601143F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	800210100601143F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	800210110601143F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	800210200601143F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	800210210601143F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	800210220601143F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	800210230601143F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	800210240601143F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	800210250601143F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	800210260601143F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	800210270601143F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	800210280601143F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	800210290601143F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8002102A0601143F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8002102B0601143F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8002102C0601143F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8002102D0601143F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8002102E0601143F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8002102F0601143F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	800210300601143F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	800210310601143F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	800218000601143F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	800218010601143F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	800218020601143F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	800218030601143F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	800218040601143F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	800218050601143F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	800218060601143F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	800218070601143F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	800218080601143F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	800218090601143F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8002180A0601143F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8002180B0601143F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8002180C0601143F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8002180D0601143F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8002180E0601143F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8002180F0601143F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	800218100601143F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	800218110601143F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	800218200601143F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	800218210601143F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	800218220601143F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	800218230601143F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	800218240601143F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	800218250601143F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	800218260601143F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	800218270601143F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	800218280601143F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	800218290601143F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8002182A0601143F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8002182B0601143F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8002182C0601143F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8002182D0601143F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8002182E0601143F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8002182F0601143F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	800218300601143F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	800218310601143F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	800220000601143F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50:51	RO	constant = 0b00
52	RWX	RX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the receive descrambler on a specific lane, or all lanes, by using a per-lane/per-group global write.
53:55	RO	constant = 0b000

Bits	SCOM	Field Mnemonic: Description
56:57	RWX	RX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by RX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
58	RWX	RX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the receive FIFO for slower frequency connections.
59	RO	constant = 0b0
60	RWX	RX_PRBS_SYNC_MODE: This bit selects the PRBS synchronization sequence length.
61	RWX	RX_PRBS_RXBIST_MODE: This bit forces prbs_en on for running edi+ rx_bist.
62:63	RO	constant = 0b00

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	800220010601143F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50:51	RO	constant = 0b00
52	RWX	RX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the receive descrambler on a specific lane, or all lanes, by using a per-lane/per-group global write.
53:55	RO	constant = 0b000
56:57	RWX	RX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by RX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
58	RWX	RX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the receive FIFO for slower frequency connections.
59	RO	constant = 0b0
60	RWX	RX_PRBS_SYNC_MODE: This bit selects the PRBS synchronization sequence length.
61	RWX	RX_PRBS_RXBIST_MODE: This bit forces prbs_en on for running edi+ rx_bist.
62:63	RO	constant = 0b00

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	800220020601143F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50:51	RO	constant = 0b00
52	RWX	RX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the receive descrambler on a specific lane, or all lanes, by using a per-lane/per-group global write.
53:55	RO	constant = 0b000
56:57	RWX	RX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by RX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
58	RWX	RX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the receive FIFO for slower frequency connections.
59	RO	constant = 0b0
60	RWX	RX_PRBS_SYNC_MODE: This bit selects the PRBS synchronization sequence length.
61	RWX	RX_PRBS_RXBIST_MODE: This bit forces prbs_en on for running edi+ rx_bist.
62:63	RO	constant = 0b00

Register Name	**Receive Bit Mode 1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	800220030601143F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50:51	RO	constant = 0b00
52	RWX	RX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the receive descrambler on a specific lane, or all lanes, by using a per-lane/per-group global write.
53:55	RO	constant = 0b000
56:57	RWX	RX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by RX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
58	RWX	RX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the receive FIFO for slower frequency connections.
59	RO	constant = 0b0
60	RWX	RX_PRBS_SYNC_MODE: This bit selects the PRBS synchronization sequence length.
61	RWX	RX_PRBS_RXBIST_MODE: This bit forces prbs_en on for running edi+ rx_bist.

Bits	SCOM	Field Mnemonic: Description
62:63	RO	constant = 0b00

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	800220040601143F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50:51	RO	constant = 0b00
52	RWX	RX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the receive descrambler on a specific lane, or all lanes, by using a per-lane/per-group global write.
53:55	RO	constant = 0b000
56:57	RWX	RX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by RX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
58	RWX	RX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the receive FIFO for slower frequency connections.
59	RO	constant = 0b0
60	RWX	RX_PRBS_SYNC_MODE: This bit selects the PRBS synchronization sequence length.
61	RWX	RX_PRBS_RXBIST_MODE: This bit forces prbs_en on for running edi+ rx_bist.
62:63	RO	constant = 0b00

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	800220050601143F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50:51	RO	constant = 0b00
52	RWX	RX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the receive descrambler on a specific lane, or all lanes, by using a per-lane/per-group global write.
53:55	RO	constant = 0b000

Bits	SCOM	Field Mnemonic: Description
56:57	RWX	RX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by RX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
58	RWX	RX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the receive FIFO for slower frequency connections.
59	RO	constant = 0b0
60	RWX	RX_PRBS_SYNC_MODE: This bit selects the PRBS synchronization sequence length.
61	RWX	RX_PRBS_RXBIST_MODE: This bit forces prbs_en on for running edi+ rx_bist.
62:63	RO	constant = 0b00

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	800220060601143F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50:51	RO	constant = 0b00
52	RWX	RX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the receive descrambler on a specific lane, or all lanes, by using a per-lane/per-group global write.
53:55	RO	constant = 0b000
56:57	RWX	RX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by RX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
58	RWX	RX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the receive FIFO for slower frequency connections.
59	RO	constant = 0b0
60	RWX	RX_PRBS_SYNC_MODE: This bit selects the PRBS synchronization sequence length.
61	RWX	RX_PRBS_RXBIST_MODE: This bit forces prbs_en on for running edi+ rx_bist.
62:63	RO	constant = 0b00

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	800220070601143F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50:51	RO	constant = 0b00
52	RWX	RX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the receive descrambler on a specific lane, or all lanes, by using a per-lane/per-group global write.
53:55	RO	constant = 0b000
56:57	RWX	RX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by RX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
58	RWX	RX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the receive FIFO for slower frequency connections.
59	RO	constant = 0b0
60	RWX	RX_PRBS_SYNC_MODE: This bit selects the PRBS synchronization sequence length.
61	RWX	RX_PRBS_RXBIST_MODE: This bit forces prbs_en on for running edi+ rx_bist.
62:63	RO	constant = 0b00

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	800220080601143F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50:51	RO	constant = 0b00
52	RWX	RX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the receive descrambler on a specific lane, or all lanes, by using a per-lane/per-group global write.
53:55	RO	constant = 0b000
56:57	RWX	RX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by RX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
58	RWX	RX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the receive FIFO for slower frequency connections.
59	RO	constant = 0b0
60	RWX	RX_PRBS_SYNC_MODE: This bit selects the PRBS synchronization sequence length.
61	RWX	RX_PRBS_RXBIST_MODE: This bit forces prbs_en on for running edi+ rx_bist.

Bits	SCOM	Field Mnemonic: Description
62:63	RO	constant = 0b00

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	800220090601143F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50:51	RO	constant = 0b00
52	RWX	RX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the receive descrambler on a specific lane, or all lanes, by using a per-lane/per-group global write.
53:55	RO	constant = 0b000
56:57	RWX	RX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by RX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
58	RWX	RX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the receive FIFO for slower frequency connections.
59	RO	constant = 0b0
60	RWX	RX_PRBS_SYNC_MODE: This bit selects the PRBS synchronization sequence length.
61	RWX	RX_PRBS_RXBIST_MODE: This bit forces prbs_en on for running edi+ rx_bist.
62:63	RO	constant = 0b00

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	8002200A0601143F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50:51	RO	constant = 0b00
52	RWX	RX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the receive descrambler on a specific lane, or all lanes, by using a per-lane/per-group global write.
53:55	RO	constant = 0b000

Bits	SCOM	Field Mnemonic: Description
56:57	RWX	RX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by RX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
58	RWX	RX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the receive FIFO for slower frequency connections.
59	RO	constant = 0b0
60	RWX	RX_PRBS_SYNC_MODE: This bit selects the PRBS synchronization sequence length.
61	RWX	RX_PRBS_RXBIST_MODE: This bit forces prbs_en on for running edi+ rx_bist.
62:63	RO	constant = 0b00

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	8002200B0601143F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50:51	RO	constant = 0b00
52	RWX	RX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the receive descrambler on a specific lane, or all lanes, by using a per-lane/per-group global write.
53:55	RO	constant = 0b000
56:57	RWX	RX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by RX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
58	RWX	RX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the receive FIFO for slower frequency connections.
59	RO	constant = 0b0
60	RWX	RX_PRBS_SYNC_MODE: This bit selects the PRBS synchronization sequence length.
61	RWX	RX_PRBS_RXBIST_MODE: This bit forces prbs_en on for running edi+ rx_bist.
62:63	RO	constant = 0b00

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	8002200C0601143F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50:51	RO	constant = 0b00
52	RWX	RX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the receive descrambler on a specific lane, or all lanes, by using a per-lane/per-group global write.
53:55	RO	constant = 0b000
56:57	RWX	RX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by RX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
58	RWX	RX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the receive FIFO for slower frequency connections.
59	RO	constant = 0b0
60	RWX	RX_PRBS_SYNC_MODE: This bit selects the PRBS synchronization sequence length.
61	RWX	RX_PRBS_RXBIST_MODE: This bit forces prbs_en on for running edi+ rx_bist.
62:63	RO	constant = 0b00

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	8002200D0601143F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50:51	RO	constant = 0b00
52	RWX	RX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the receive descrambler on a specific lane, or all lanes, by using a per-lane/per-group global write.
53:55	RO	constant = 0b000
56:57	RWX	RX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by RX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
58	RWX	RX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the receive FIFO for slower frequency connections.
59	RO	constant = 0b0
60	RWX	RX_PRBS_SYNC_MODE: This bit selects the PRBS synchronization sequence length.
61	RWX	RX_PRBS_RXBIST_MODE: This bit forces prbs_en on for running edi+ rx_bist.

Bits	SCOM	Field Mnemonic: Description
62:63	RO	constant = 0b00

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	8002200E0601143F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50:51	RO	constant = 0b00
52	RWX	RX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the receive descrambler on a specific lane, or all lanes, by using a per-lane/per-group global write.
53:55	RO	constant = 0b000
56:57	RWX	RX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by RX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
58	RWX	RX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the receive FIFO for slower frequency connections.
59	RO	constant = 0b0
60	RWX	RX_PRBS_SYNC_MODE: This bit selects the PRBS synchronization sequence length.
61	RWX	RX_PRBS_RXBIST_MODE: This bit forces prbs_en on for running edi+ rx_bist.
62:63	RO	constant = 0b00

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	8002200F0601143F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50:51	RO	constant = 0b00
52	RWX	RX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the receive descrambler on a specific lane, or all lanes, by using a per-lane/per-group global write.
53:55	RO	constant = 0b000

Bits	SCOM	Field Mnemonic: Description
56:57	RWX	RX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by RX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
58	RWX	RX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the receive FIFO for slower frequency connections.
59	RO	constant = 0b0
60	RWX	RX_PRBS_SYNC_MODE: This bit selects the PRBS synchronization sequence length.
61	RWX	RX_PRBS_RXBIST_MODE: This bit forces prbs_en on for running edi+ rx_bist.
62:63	RO	constant = 0b00

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	800220100601143F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50:51	RO	constant = 0b00
52	RWX	RX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the receive descrambler on a specific lane, or all lanes, by using a per-lane/per-group global write.
53:55	RO	constant = 0b000
56:57	RWX	RX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by RX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
58	RWX	RX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the receive FIFO for slower frequency connections.
59	RO	constant = 0b0
60	RWX	RX_PRBS_SYNC_MODE: This bit selects the PRBS synchronization sequence length.
61	RWX	RX_PRBS_RXBIST_MODE: This bit forces prbs_en on for running edi+ rx_bist.
62:63	RO	constant = 0b00

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	800220110601143F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50:51	RO	constant = 0b00
52	RWX	RX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the receive descrambler on a specific lane, or all lanes, by using a per-lane/per-group global write.
53:55	RO	constant = 0b000
56:57	RWX	RX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by RX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
58	RWX	RX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the receive FIFO for slower frequency connections.
59	RO	constant = 0b0
60	RWX	RX_PRBS_SYNC_MODE: This bit selects the PRBS synchronization sequence length.
61	RWX	RX_PRBS_RXBIST_MODE: This bit forces prbs_en on for running edi+ rx_bist.
62:63	RO	constant = 0b00

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	800220200601143F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50:51	RO	constant = 0b00
52	RWX	RX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the receive descrambler on a specific lane, or all lanes, by using a per-lane/per-group global write.
53:55	RO	constant = 0b000
56:57	RWX	RX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by RX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
58	RWX	RX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the receive FIFO for slower frequency connections.
59	RO	constant = 0b0
60	RWX	RX_PRBS_SYNC_MODE: This bit selects the PRBS synchronization sequence length.
61	RWX	RX_PRBS_RXBIST_MODE: This bit forces prbs_en on for running edi+ rx_bist.

Bits	SCOM	Field Mnemonic: Description
62:63	RO	constant = 0b00

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	800220210601143F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50:51	RO	constant = 0b00
52	RWX	RX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the receive descrambler on a specific lane, or all lanes, by using a per-lane/per-group global write.
53:55	RO	constant = 0b000
56:57	RWX	RX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by RX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
58	RWX	RX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the receive FIFO for slower frequency connections.
59	RO	constant = 0b0
60	RWX	RX_PRBS_SYNC_MODE: This bit selects the PRBS synchronization sequence length.
61	RWX	RX_PRBS_RXBIST_MODE: This bit forces prbs_en on for running edi+ rx_bist.
62:63	RO	constant = 0b00

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	800220220601143F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50:51	RO	constant = 0b00
52	RWX	RX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the receive descrambler on a specific lane, or all lanes, by using a per-lane/per-group global write.
53:55	RO	constant = 0b000

Bits	SCOM	Field Mnemonic: Description
56:57	RWX	RX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by RX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
58	RWX	RX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the receive FIFO for slower frequency connections.
59	RO	constant = 0b0
60	RWX	RX_PRBS_SYNC_MODE: This bit selects the PRBS synchronization sequence length.
61	RWX	RX_PRBS_RXBIST_MODE: This bit forces prbs_en on for running edi+ rx_bist.
62:63	RO	constant = 0b00

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	800220230601143F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50:51	RO	constant = 0b00
52	RWX	RX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the receive descrambler on a specific lane, or all lanes, by using a per-lane/per-group global write.
53:55	RO	constant = 0b000
56:57	RWX	RX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by RX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
58	RWX	RX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the receive FIFO for slower frequency connections.
59	RO	constant = 0b0
60	RWX	RX_PRBS_SYNC_MODE: This bit selects the PRBS synchronization sequence length.
61	RWX	RX_PRBS_RXBIST_MODE: This bit forces prbs_en on for running edi+ rx_bist.
62:63	RO	constant = 0b00

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	800220240601143F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50:51	RO	constant = 0b00
52	RWX	RX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the receive descrambler on a specific lane, or all lanes, by using a per-lane/per-group global write.
53:55	RO	constant = 0b000
56:57	RWX	RX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by RX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
58	RWX	RX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the receive FIFO for slower frequency connections.
59	RO	constant = 0b0
60	RWX	RX_PRBS_SYNC_MODE: This bit selects the PRBS synchronization sequence length.
61	RWX	RX_PRBS_RXBIST_MODE: This bit forces prbs_en on for running edi+ rx_bist.
62:63	RO	constant = 0b00

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	800220250601143F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50:51	RO	constant = 0b00
52	RWX	RX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the receive descrambler on a specific lane, or all lanes, by using a per-lane/per-group global write.
53:55	RO	constant = 0b000
56:57	RWX	RX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by RX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
58	RWX	RX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the receive FIFO for slower frequency connections.
59	RO	constant = 0b0
60	RWX	RX_PRBS_SYNC_MODE: This bit selects the PRBS synchronization sequence length.
61	RWX	RX_PRBS_RXBIST_MODE: This bit forces prbs_en on for running edi+ rx_bist.

Bits	SCOM	Field Mnemonic: Description
62:63	RO	constant = 0b00

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	800220260601143F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50:51	RO	constant = 0b00
52	RWX	RX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the receive descrambler on a specific lane, or all lanes, by using a per-lane/per-group global write.
53:55	RO	constant = 0b000
56:57	RWX	RX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by RX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
58	RWX	RX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the receive FIFO for slower frequency connections.
59	RO	constant = 0b0
60	RWX	RX_PRBS_SYNC_MODE: This bit selects the PRBS synchronization sequence length.
61	RWX	RX_PRBS_RXBIST_MODE: This bit forces prbs_en on for running edi+ rx_bist.
62:63	RO	constant = 0b00

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	800220270601143F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50:51	RO	constant = 0b00
52	RWX	RX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the receive descrambler on a specific lane, or all lanes, by using a per-lane/per-group global write.
53:55	RO	constant = 0b000

Bits	SCOM	Field Mnemonic: Description
56:57	RWX	RX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by RX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
58	RWX	RX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the receive FIFO for slower frequency connections.
59	RO	constant = 0b0
60	RWX	RX_PRBS_SYNC_MODE: This bit selects the PRBS synchronization sequence length.
61	RWX	RX_PRBS_RXBIST_MODE: This bit forces prbs_en on for running edi+ rx_bist.
62:63	RO	constant = 0b00

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	800220280601143F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50:51	RO	constant = 0b00
52	RWX	RX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the receive descrambler on a specific lane, or all lanes, by using a per-lane/per-group global write.
53:55	RO	constant = 0b000
56:57	RWX	RX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by RX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
58	RWX	RX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the receive FIFO for slower frequency connections.
59	RO	constant = 0b0
60	RWX	RX_PRBS_SYNC_MODE: This bit selects the PRBS synchronization sequence length.
61	RWX	RX_PRBS_RXBIST_MODE: This bit forces prbs_en on for running edi+ rx_bist.
62:63	RO	constant = 0b00

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	800220290601143F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50:51	RO	constant = 0b00
52	RWX	RX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the receive descrambler on a specific lane, or all lanes, by using a per-lane/per-group global write.
53:55	RO	constant = 0b000
56:57	RWX	RX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by RX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
58	RWX	RX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the receive FIFO for slower frequency connections.
59	RO	constant = 0b0
60	RWX	RX_PRBS_SYNC_MODE: This bit selects the PRBS synchronization sequence length.
61	RWX	RX_PRBS_RXBIST_MODE: This bit forces prbs_en on for running edi+ rx_bist.
62:63	RO	constant = 0b00

Register Name	**Receive Bit Mode 1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	8002202A0601143F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50:51	RO	constant = 0b00
52	RWX	RX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the receive descrambler on a specific lane, or all lanes, by using a per-lane/per-group global write.
53:55	RO	constant = 0b000
56:57	RWX	RX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by RX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
58	RWX	RX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the receive FIFO for slower frequency connections.
59	RO	constant = 0b0
60	RWX	RX_PRBS_SYNC_MODE: This bit selects the PRBS synchronization sequence length.
61	RWX	RX_PRBS_RXBIST_MODE: This bit forces prbs_en on for running edi+ rx_bist.

Bits	SCOM	Field Mnemonic: Description
62:63	RO	constant = 0b00

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	8002202B0601143F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50:51	RO	constant = 0b00
52	RWX	RX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the receive descrambler on a specific lane, or all lanes, by using a per-lane/per-group global write.
53:55	RO	constant = 0b000
56:57	RWX	RX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by RX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
58	RWX	RX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the receive FIFO for slower frequency connections.
59	RO	constant = 0b0
60	RWX	RX_PRBS_SYNC_MODE: This bit selects the PRBS synchronization sequence length.
61	RWX	RX_PRBS_RXBIST_MODE: This bit forces prbs_en on for running edi+ rx_bist.
62:63	RO	constant = 0b00

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	8002202C0601143F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50:51	RO	constant = 0b00
52	RWX	RX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the receive descrambler on a specific lane, or all lanes, by using a per-lane/per-group global write.
53:55	RO	constant = 0b000

Bits	SCOM	Field Mnemonic: Description
56:57	RWX	RX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by RX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
58	RWX	RX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the receive FIFO for slower frequency connections.
59	RO	constant = 0b0
60	RWX	RX_PRBS_SYNC_MODE: This bit selects the PRBS synchronization sequence length.
61	RWX	RX_PRBS_RXBIST_MODE: This bit forces prbs_en on for running edi+ rx_bist.
62:63	RO	constant = 0b00

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	8002202D0601143F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50:51	RO	constant = 0b00
52	RWX	RX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the receive descrambler on a specific lane, or all lanes, by using a per-lane/per-group global write.
53:55	RO	constant = 0b000
56:57	RWX	RX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by RX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
58	RWX	RX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the receive FIFO for slower frequency connections.
59	RO	constant = 0b0
60	RWX	RX_PRBS_SYNC_MODE: This bit selects the PRBS synchronization sequence length.
61	RWX	RX_PRBS_RXBIST_MODE: This bit forces prbs_en on for running edi+ rx_bist.
62:63	RO	constant = 0b00

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	8002202E0601143F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50:51	RO	constant = 0b00
52	RWX	RX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the receive descrambler on a specific lane, or all lanes, by using a per-lane/per-group global write.
53:55	RO	constant = 0b000
56:57	RWX	RX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by RX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
58	RWX	RX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the receive FIFO for slower frequency connections.
59	RO	constant = 0b0
60	RWX	RX_PRBS_SYNC_MODE: This bit selects the PRBS synchronization sequence length.
61	RWX	RX_PRBS_RXBIST_MODE: This bit forces prbs_en on for running edi+ rx_bist.
62:63	RO	constant = 0b00

Register Name	**Receive Bit Mode 1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	8002202F0601143F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50:51	RO	constant = 0b00
52	RWX	RX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the receive descrambler on a specific lane, or all lanes, by using a per-lane/per-group global write.
53:55	RO	constant = 0b000
56:57	RWX	RX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by RX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
58	RWX	RX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the receive FIFO for slower frequency connections.
59	RO	constant = 0b0
60	RWX	RX_PRBS_SYNC_MODE: This bit selects the PRBS synchronization sequence length.
61	RWX	RX_PRBS_RXBIST_MODE: This bit forces prbs_en on for running edi+ rx_bist.

Bits	SCOM	Field Mnemonic: Description
62:63	RO	constant = 0b00

Register Name	**Receive Bit Mode 1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	800220300601143F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50:51	RO	constant = 0b00
52	RWX	RX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the receive descrambler on a specific lane, or all lanes, by using a per-lane/per-group global write.
53:55	RO	constant = 0b000
56:57	RWX	RX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by RX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
58	RWX	RX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the receive FIFO for slower frequency connections.
59	RO	constant = 0b0
60	RWX	RX_PRBS_SYNC_MODE: This bit selects the PRBS synchronization sequence length.
61	RWX	RX_PRBS_RXBIST_MODE: This bit forces prbs_en on for running edi+ rx_bist.
62:63	RO	constant = 0b00

Register Name	**Receive Bit Mode 1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	800220310601143F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50:51	RO	constant = 0b00
52	RWX	RX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the receive descrambler on a specific lane, or all lanes, by using a per-lane/per-group global write.
53:55	RO	constant = 0b000

Bits	SCOM	Field Mnemonic: Description
56:57	RWX	RX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by RX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
58	RWX	RX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the receive FIFO for slower frequency connections.
59	RO	constant = 0b0
60	RWX	RX_PRBS_SYNC_MODE: This bit selects the PRBS synchronization sequence length.
61	RWX	RX_PRBS_RXBIST_MODE: This bit forces prbs_en on for running edi+ rx_bist.
62:63	RO	constant = 0b00

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	800228000601143F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:59	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	800228010601143F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:59	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	800228020601143F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:59	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	800228030601143F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:59	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	800228040601143F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:59	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	800228050601143F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:59	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	800228060601143F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:59	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	800228070601143F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:59	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	800228080601143F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:59	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	800228090601143F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:59	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	8002280A0601143F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:59	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	8002280B0601143F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:59	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	8002280C0601143F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:59	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	8002280D0601143F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:59	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	8002280E0601143F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:59	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	8002280F0601143F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:59	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	800228100601143F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:59	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	800228110601143F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:59	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	800228200601143F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:59	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	800228210601143F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:59	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	800228220601143F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:59	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	800228230601143F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:59	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	800228240601143F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:59	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	800228250601143F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:59	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	800228260601143F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:59	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	800228270601143F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:59	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	800228280601143F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:59	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	800228290601143F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:59	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	8002282A0601143F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:59	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	8002282B0601143F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:59	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	8002282C0601143F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:59	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	8002282D0601143F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:59	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	8002282E0601143F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:59	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	8002282F0601143F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:59	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	800228300601143F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:59	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	800228310601143F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:59	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	800230000601143F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	800230010601143F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	800230020601143F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	800230030601143F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	800230040601143F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	800230050601143F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	800230060601143F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	800230070601143F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	800230080601143F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	800230090601143F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	8002300A0601143F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	8002300B0601143F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	8002300C0601143F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	8002300D0601143F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	8002300E0601143F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	8002300F0601143F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	800230100601143F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	800230110601143F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	800230200601143F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	800230210601143F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	800230220601143F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	800230230601143F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	800230240601143F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	800230250601143F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	800230260601143F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	800230270601143F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	800230280601143F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	800230290601143F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	8002302A0601143F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	8002302B0601143F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	8002302C0601143F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	8002302D0601143F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	8002302E0601143F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	8002302F0601143F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	800230300601143F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	800230310601143F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit CNTLX1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	800240000601143F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49	RWX	RX_LANE_INVERT: This bit inverts the receive lane data.
50	RWX	RX_LANE_INVALID: This bit marks this receive slice as invalid and fences other operations. Use this bit, for example, to broadcast a setting to all good lanes but not bad or disabled ones.
51	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic. 0b0 = Data. 0b1 = Descrambler output.
52	RO	constant = 0b0
53	RWX	RX_PDWN_LITE: When set, this bit partially powers down unused spare lanes when not being recalibrated.
54	RWX	RX_PRBS_CHECK_SYNC: This bit enables checking for the 12/24 UI scramble synchronization pulse in the descramble PRBS block. 0b0 = Disable checking (forces prbs_sync_done to 0). 0b1 = Enable checking (prbs_sync_done may go to 1 after identifying the sync pulse).
55	RWX	RX_PRBS_SEED_DDC: Set this bit to enable seeding of the DDC PRBS block from the data pipe output (either the data stream or the descramble PRBS block depending on the value of rx_pipe_sel).
56	RWX	RX_PRBS_SEED_DFE: Set this bit to enable seeding of the DFE PRBS block. Related to this is rx_dfe_force_load_seed, which loads from the incoming data stream when 0 or from the rx_prbs_seed_value_* when 1.
57	RWX	RX_DFE_FORCE_LOAD_SEED: Set this bit to force rx_prbs_seed_value_0_15 and rx_prbs_seed_value_16_22 to load directly into the DFE history vector in the analog front-end for this lane. **Note:** The rx_prbs_seed_value_* bits are extended by 1 bit and shifted by a fixed value to match the pipeline delays between the analog front end and the receive PRBS descrambler. To set the DFE history vector to a specific value, the user must reverse that transformation to determine the value to write to the rx_prbs_seed_value_* to get the desired result in the vector.
58	RWX	RX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
59:60	RWX	RX_IOCLK_SLIP: This field provides software control of the receive slice deserializer IOCLK slip control. Use this to slip the deserilizer by 2N beats.
61	RWX	RX_IOCLK_SLIP_STROBE: This bit provides software control to execute IOCLK slip control.
62	RWX	RX_HISTORY_PRBS_POWER_UP: This bit forces the power up of the additional analog history latches used for PRBS generation when performing H2 - 12 calibration.
63	RWX	RX_PSAVE_RESYNC_DISABLE: This bit disables the resynchronize machine for this physical lane without disabling psave mode entirely.

Register Name	**Receive Bit CNTLX1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	800240010601143F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49	RWX	RX_LANE_INVERT: This bit inverts the receive lane data.
50	RWX	RX_LANE_INVALID: This bit marks this receive slice as invalid and fences other operations. Use this bit, for example, to broadcast a setting to all good lanes but not bad or disabled ones.

Bits	SCOM	Field Mnemonic: Description
51	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic. 0b0 = Data. 0b1 = Descrambler output.
52	RO	constant = 0b0
53	RWX	RX_PDWN_LITE: When set, this bit partially powers down unused spare lanes when not being recalibrated.
54	RWX	RX_PRBS_CHECK_SYNC: This bit enables checking for the 12/24 UI scramble synchronization pulse in the descramble PRBS block. 0b0 = Disable checking (forces prbs_sync_done to 0). 0b1 = Enable checking (prbs_sync_done may go to 1 after identifying the sync pulse).
55	RWX	RX_PRBS_SEED_DDC: Set this bit to enable seeding of the DDC PRBS block from the data pipe output (either the data stream or the descramble PRBS block depending on the value of rx_pipe_sel).
56	RWX	RX_PRBS_SEED_DFE: Set this bit to enable seeding of the DFE PRBS block. Related to this is rx_dfe_force_load_seed, which loads from the incoming data stream when 0 or from the rx_prbs_seed_value_* when 1.
57	RWX	RX_DFE_FORCE_LOAD_SEED: Set this bit to force rx_prbs_seed_value_0_15 and rx_prbs_seed_value_16_22 to load directly into the DFE history vector in the analog front-end for this lane. **Note:** The rx_prbs_seed_value_* bits are extended by 1 bit and shifted by a fixed value to match the pipeline delays between the analog front end and the receive PRBS descrambler. To set the DFE history vector to a specific value, the user must reverse that transformation to determine the value to write to the rx_prbs_seed_value_* to get the desired result in the vector.
58	RWX	RX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
59:60	RWX	RX_IOCLK_SLIP: This field provides software control of the receive slice deserializer IOCLK slip control. Use this to slip the deserilizer by 2N beats.
61	RWX	RX_IOCLK_SLIP_STROBE: This bit provides software control to execute IOCLK slip control.
62	RWX	RX_HISTORY_PRBS_POWER_UP: This bit forces the power up of the additional analog history latches used for PRBS generation when performing H2 - 12 calibration.
63	RWX	RX_PSAVE_RESYNC_DISABLE: This bit disables the resynchronize machine for this physical lane without disabling psave mode entirely.

Register Name	Receive Bit CNTLX1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	800240020601143F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49	RWX	RX_LANE_INVERT: This bit inverts the receive lane data.
50	RWX	RX_LANE_INVALID: This bit marks this receive slice as invalid and fences other operations. Use this bit, for example, to broadcast a setting to all good lanes but not bad or disabled ones.
51	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic. 0b0 = Data. 0b1 = Descrambler output.
52	RO	constant = 0b0
53	RWX	RX_PDWN_LITE: When set, this bit partially powers down unused spare lanes when not being recalibrated.

Bits	SCOM	Field Mnemonic: Description
54	RWX	RX_PRBS_CHECK_SYNC: This bit enables checking for the 12/24 UI scramble synchronization pulse in the descramble PRBS block. 0b0 = Disable checking (forces prbs_sync_done to 0). 0b1 = Enable checking (prbs_sync_done may go to 1 after identifying the sync pulse).
55	RWX	RX_PRBS_SEED_DDC: Set this bit to enable seeding of the DDC PRBS block from the data pipe output (either the data stream or the descramble PRBS block depending on the value of rx_pipe_sel).
56	RWX	RX_PRBS_SEED_DFE: Set this bit to enable seeding of the DFE PRBS block. Related to this is rx_dfe_force_load_seed, which loads from the incoming data stream when 0 or from the rx_prbs_seed_value_* when 1.
57	RWX	RX_DFE_FORCE_LOAD_SEED: Set this bit to force rx_prbs_seed_value_0_15 and rx_prbs_seed_value_16_22 to load directly into the DFE history vector in the analog front-end for this lane. **Note:** The rx_prbs_seed_value_* bits are extended by 1 bit and shifted by a fixed value to match the pipeline delays between the analog front end and the receive PRBS descrambler. To set the DFE history vector to a specific value, the user must reverse that transformation to determine the value to write to the rx_prbs_seed_value_* to get the desired result in the vector.
58	RWX	RX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
59:60	RWX	RX_IOCLK_SLIP: This field provides software control of the receive slice deserializer IOCLK slip control. Use this to slip the deserilizer by 2N beats.
61	RWX	RX_IOCLK_SLIP_STROBE: This bit provides software control to execute IOCLK slip control.
62	RWX	RX_HISTORY_PRBS_POWER_UP: This bit forces the power up of the additional analog history latches used for PRBS generation when performing H2 - 12 calibration.
63	RWX	RX_PSAVE_RESYNC_DISABLE: This bit disables the resynchronize machine for this physical lane without disabling psave mode entirely.

Register Name	**Receive Bit CNTLX1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	800240030601143F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49	RWX	RX_LANE_INVERT: This bit inverts the receive lane data.
50	RWX	RX_LANE_INVALID: This bit marks this receive slice as invalid and fences other operations. Use this bit, for example, to broadcast a setting to all good lanes but not bad or disabled ones.
51	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic. 0b0 = Data. 0b1 = Descrambler output.
52	RO	constant = 0b0
53	RWX	RX_PDWN_LITE: When set, this bit partially powers down unused spare lanes when not being recalibrated.
54	RWX	RX_PRBS_CHECK_SYNC: This bit enables checking for the 12/24 UI scramble synchronization pulse in the descramble PRBS block. 0b0 = Disable checking (forces prbs_sync_done to 0). 0b1 = Enable checking (prbs_sync_done may go to 1 after identifying the sync pulse).
55	RWX	RX_PRBS_SEED_DDC: Set this bit to enable seeding of the DDC PRBS block from the data pipe output (either the data stream or the descramble PRBS block depending on the value of rx_pipe_sel).

Bits	SCOM	Field Mnemonic: Description
56	RWX	RX_PRBS_SEED_DFE: Set this bit to enable seeding of the DFE PRBS block. Related to this is rx_dfe_force_load_seed, which loads from the incoming data stream when 0 or from the rx_prbs_seed_value_* when 1.
57	RWX	RX_DFE_FORCE_LOAD_SEED: Set this bit to force rx_prbs_seed_value_0_15 and rx_prbs_seed_value_16_22 to load directly into the DFE history vector in the analog front-end for this lane. **Note:** The rx_prbs_seed_value_* bits are extended by 1 bit and shifted by a fixed value to match the pipeline delays between the analog front end and the receive PRBS descrambler. To set the DFE history vector to a specific value, the user must reverse that transformation to determine the value to write to the rx_prbs_seed_value_* to get the desired result in the vector.
58	RWX	RX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
59:60	RWX	RX_IOCLK_SLIP: This field provides software control of the receive slice deserializer IOCLK slip control. Use this to slip the deserilizer by 2N beats.
61	RWX	RX_IOCLK_SLIP_STROBE: This bit provides software control to execute IOCLK slip control.
62	RWX	RX_HISTORY_PRBS_POWER_UP: This bit forces the power up of the additional analog history latches used for PRBS generation when performing H2 - 12 calibration.
63	RWX	RX_PSAVE_RESYNC_DISABLE: This bit disables the resynchronize machine for this physical lane without disabling psave mode entirely.

Register Name	**Receive Bit CNTLX1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	800240040601143F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49	RWX	RX_LANE_INVERT: This bit inverts the receive lane data.
50	RWX	RX_LANE_INVALID: This bit marks this receive slice as invalid and fences other operations. Use this bit, for example, to broadcast a setting to all good lanes but not bad or disabled ones.
51	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic. 0b0 = Data. 0b1 = Descrambler output.
52	RO	constant = 0b0
53	RWX	RX_PDWN_LITE: When set, this bit partially powers down unused spare lanes when not being recalibrated.
54	RWX	RX_PRBS_CHECK_SYNC: This bit enables checking for the 12/24 UI scramble synchronization pulse in the descramble PRBS block. 0b0 = Disable checking (forces prbs_sync_done to 0). 0b1 = Enable checking (prbs_sync_done may go to 1 after identifying the sync pulse).
55	RWX	RX_PRBS_SEED_DDC: Set this bit to enable seeding of the DDC PRBS block from the data pipe output (either the data stream or the descramble PRBS block depending on the value of rx_pipe_sel).
56	RWX	RX_PRBS_SEED_DFE: Set this bit to enable seeding of the DFE PRBS block. Related to this is rx_dfe_force_load_seed, which loads from the incoming data stream when 0 or from the rx_prbs_seed_value_* when 1.

Bits	SCOM	Field Mnemonic: Description
57	RWX	RX_DFE_FORCE_LOAD_SEED: Set this bit to force rx_prbs_seed_value_0_15 and rx_prbs_seed_value_16_22 to load directly into the DFE history vector in the analog front-end for this lane. **Note:** The rx_prbs_seed_value_* bits are extended by 1 bit and shifted by a fixed value to match the pipeline delays between the analog front end and the receive PRBS descrambler. To set the DFE history vector to a specific value, the user must reverse that transformation to determine the value to write to the rx_prbs_seed_value_* to get the desired result in the vector.
58	RWX	RX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
59:60	RWX	RX_IOCLK_SLIP: This field provides software control of the receive slice deserializer IOCLK slip control. Use this to slip the deserilizer by 2N beats.
61	RWX	RX_IOCLK_SLIP_STROBE: This bit provides software control to execute IOCLK slip control.
62	RWX	RX_HISTORY_PRBS_POWER_UP: This bit forces the power up of the additional analog history latches used for PRBS generation when performing H2 - 12 calibration.
63	RWX	RX_PSAVE_RESYNC_DISABLE: This bit disables the resynchronize machine for this physical lane without disabling psave mode entirely.

Register Name	Receive Bit CNTLX1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	800240050601143F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49	RWX	RX_LANE_INVERT: This bit inverts the receive lane data.
50	RWX	RX_LANE_INVALID: This bit marks this receive slice as invalid and fences other operations. Use this bit, for example, to broadcast a setting to all good lanes but not bad or disabled ones.
51	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic. 0b0 = Data. 0b1 = Descrambler output.
52	RO	constant = 0b0
53	RWX	RX_PDWN_LITE: When set, this bit partially powers down unused spare lanes when not being recalibrated.
54	RWX	RX_PRBS_CHECK_SYNC: This bit enables checking for the 12/24 UI scramble synchronization pulse in the descramble PRBS block. 0b0 = Disable checking (forces prbs_sync_done to 0). 0b1 = Enable checking (prbs_sync_done may go to 1 after identifying the sync pulse).
55	RWX	RX_PRBS_SEED_DDC: Set this bit to enable seeding of the DDC PRBS block from the data pipe output (either the data stream or the descramble PRBS block depending on the value of rx_pipe_sel).
56	RWX	RX_PRBS_SEED_DFE: Set this bit to enable seeding of the DFE PRBS block. Related to this is rx_dfe_force_load_seed, which loads from the incoming data stream when 0 or from the rx_prbs_seed_value_* when 1.
57	RWX	RX_DFE_FORCE_LOAD_SEED: Set this bit to force rx_prbs_seed_value_0_15 and rx_prbs_seed_value_16_22 to load directly into the DFE history vector in the analog front-end for this lane. **Note:** The rx_prbs_seed_value_* bits are extended by 1 bit and shifted by a fixed value to match the pipeline delays between the analog front end and the receive PRBS descrambler. To set the DFE history vector to a specific value, the user must reverse that transformation to determine the value to write to the rx_prbs_seed_value_* to get the desired result in the vector.
58	RWX	RX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.

Bits	SCOM	Field Mnemonic: Description
59:60	RWX	RX_IOCLK_SLIP: This field provides software control of the receive slice deserializer IOCLK slip control. Use this to slip the deserilizer by 2N beats.
61	RWX	RX_IOCLK_SLIP_STROBE: This bit provides software control to execute IOCLK slip control.
62	RWX	RX_HISTORY_PRBS_POWER_UP: This bit forces the power up of the additional analog history latches used for PRBS generation when performing H2 - 12 calibration.
63	RWX	RX_PSAVE_RESYNC_DISABLE: This bit disables the resynchronize machine for this physical lane without disabling psave mode entirely.

Register Name	Receive Bit CNTLX1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	800240060601143F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49	RWX	RX_LANE_INVERT: This bit inverts the receive lane data.
50	RWX	RX_LANE_INVALID: This bit marks this receive slice as invalid and fences other operations. Use this bit, for example, to broadcast a setting to all good lanes but not bad or disabled ones.
51	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic. 0b0 = Data. 0b1 = Descrambler output.
52	RO	constant = 0b0
53	RWX	RX_PDWN_LITE: When set, this bit partially powers down unused spare lanes when not being recalibrated.
54	RWX	RX_PRBS_CHECK_SYNC: This bit enables checking for the 12/24 UI scramble synchronization pulse in the descramble PRBS block. 0b0 = Disable checking (forces prbs_sync_done to 0). 0b1 = Enable checking (prbs_sync_done may go to 1 after identifying the sync pulse).
55	RWX	RX_PRBS_SEED_DDC: Set this bit to enable seeding of the DDC PRBS block from the data pipe output (either the data stream or the descramble PRBS block depending on the value of rx_pipe_sel).
56	RWX	RX_PRBS_SEED_DFE: Set this bit to enable seeding of the DFE PRBS block. Related to this is rx_dfe_force_load_seed, which loads from the incoming data stream when 0 or from the rx_prbs_seed_value_* when 1.
57	RWX	RX_DFE_FORCE_LOAD_SEED: Set this bit to force rx_prbs_seed_value_0_15 and rx_prbs_seed_value_16_22 to load directly into the DFE history vector in the analog front-end for this lane. **Note:** The rx_prbs_seed_value_* bits are extended by 1 bit and shifted by a fixed value to match the pipeline delays between the analog front end and the receive PRBS descrambler. To set the DFE history vector to a specific value, the user must reverse that transformation to determine the value to write to the rx_prbs_seed_value_* to get the desired result in the vector.
58	RWX	RX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
59:60	RWX	RX_IOCLK_SLIP: This field provides software control of the receive slice deserializer IOCLK slip control. Use this to slip the deserilizer by 2N beats.
61	RWX	RX_IOCLK_SLIP_STROBE: This bit provides software control to execute IOCLK slip control.
62	RWX	RX_HISTORY_PRBS_POWER_UP: This bit forces the power up of the additional analog history latches used for PRBS generation when performing H2 - 12 calibration.

Bits	SCOM	Field Mnemonic: Description
63	RWX	RX_PSAVE_RESYNC_DISABLE: This bit disables the resynchronize machine for this physical lane without disabling psave mode entirely.

Register Name	Receive Bit CNTLX1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	800240070601143F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49	RWX	RX_LANE_INVERT: This bit inverts the receive lane data.
50	RWX	RX_LANE_INVALID: This bit marks this receive slice as invalid and fences other operations. Use this bit, for example, to broadcast a setting to all good lanes but not bad or disabled ones.
51	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic. 0b0 = Data. 0b1 = Descrambler output.
52	RO	constant = 0b0
53	RWX	RX_PDWN_LITE: When set, this bit partially powers down unused spare lanes when not being recalibrated.
54	RWX	RX_PRBS_CHECK_SYNC: This bit enables checking for the 12/24 UI scramble synchronization pulse in the descramble PRBS block. 0b0 = Disable checking (forces prbs_sync_done to 0). 0b1 = Enable checking (prbs_sync_done may go to 1 after identifying the sync pulse).
55	RWX	RX_PRBS_SEED_DDC: Set this bit to enable seeding of the DDC PRBS block from the data pipe output (either the data stream or the descramble PRBS block depending on the value of rx_pipe_sel).
56	RWX	RX_PRBS_SEED_DFE: Set this bit to enable seeding of the DFE PRBS block. Related to this is rx_dfe_force_load_seed, which loads from the incoming data stream when 0 or from the rx_prbs_seed_value_* when 1.
57	RWX	RX_DFE_FORCE_LOAD_SEED: Set this bit to force rx_prbs_seed_value_0_15 and rx_prbs_seed_value_16_22 to load directly into the DFE history vector in the analog front-end for this lane. **Note:** The rx_prbs_seed_value_* bits are extended by 1 bit and shifted by a fixed value to match the pipeline delays between the analog front end and the receive PRBS descrambler. To set the DFE history vector to a specific value, the user must reverse that transformation to determine the value to write to the rx_prbs_seed_value_* to get the desired result in the vector.
58	RWX	RX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
59:60	RWX	RX_IOCLK_SLIP: This field provides software control of the receive slice deserializer IOCLK slip control. Use this to slip the deserilizer by 2N beats.
61	RWX	RX_IOCLK_SLIP_STROBE: This bit provides software control to execute IOCLK slip control.
62	RWX	RX_HISTORY_PRBS_POWER_UP: This bit forces the power up of the additional analog history latches used for PRBS generation when performing H2 - 12 calibration.
63	RWX	RX_PSAVE_RESYNC_DISABLE: This bit disables the resynchronize machine for this physical lane without disabling psave mode entirely.

Register Name	Receive Bit CNTLX1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	800240080601143F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49	RWX	RX_LANE_INVERT: This bit inverts the receive lane data.
50	RWX	RX_LANE_INVALID: This bit marks this receive slice as invalid and fences other operations. Use this bit, for example, to broadcast a setting to all good lanes but not bad or disabled ones.
51	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic. 0b0 = Data. 0b1 = Descrambler output.
52	RO	constant = 0b0
53	RWX	RX_PDWN_LITE: When set, this bit partially powers down unused spare lanes when not being recalibrated.
54	RWX	RX_PRBS_CHECK_SYNC: This bit enables checking for the 12/24 UI scramble synchronization pulse in the descramble PRBS block. 0b0 = Disable checking (forces prbs_sync_done to 0). 0b1 = Enable checking (prbs_sync_done may go to 1 after identifying the sync pulse).
55	RWX	RX_PRBS_SEED_DDC: Set this bit to enable seeding of the DDC PRBS block from the data pipe output (either the data stream or the descramble PRBS block depending on the value of rx_pipe_sel).
56	RWX	RX_PRBS_SEED_DFE: Set this bit to enable seeding of the DFE PRBS block. Related to this is rx_dfe_force_load_seed, which loads from the incoming data stream when 0 or from the rx_prbs_seed_value_* when 1.
57	RWX	RX_DFE_FORCE_LOAD_SEED: Set this bit to force rx_prbs_seed_value_0_15 and rx_prbs_seed_value_16_22 to load directly into the DFE history vector in the analog front-end for this lane. **Note:** The rx_prbs_seed_value_* bits are extended by 1 bit and shifted by a fixed value to match the pipeline delays between the analog front end and the receive PRBS descrambler. To set the DFE history vector to a specific value, the user must reverse that transformation to determine the value to write to the rx_prbs_seed_value_* to get the desired result in the vector.
58	RWX	RX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
59:60	RWX	RX_IOCLK_SLIP: This field provides software control of the receive slice deserializer IOCLK slip control. Use this to slip the deserilizer by 2N beats.
61	RWX	RX_IOCLK_SLIP_STROBE: This bit provides software control to execute IOCLK slip control.
62	RWX	RX_HISTORY_PRBS_POWER_UP: This bit forces the power up of the additional analog history latches used for PRBS generation when performing H2 - 12 calibration.
63	RWX	RX_PSAVE_RESYNC_DISABLE: This bit disables the resynchronize machine for this physical lane without disabling psave mode entirely.

Register Name	Receive Bit CNTLX1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	800240090601143F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49	RWX	RX_LANE_INVERT: This bit inverts the receive lane data.
50	RWX	RX_LANE_INVALID: This bit marks this receive slice as invalid and fences other operations. Use this bit, for example, to broadcast a setting to all good lanes but not bad or disabled ones.
51	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic. 0b0 = Data. 0b1 = Descrambler output.
52	RO	constant = 0b0
53	RWX	RX_PDWN_LITE: When set, this bit partially powers down unused spare lanes when not being recalibrated.
54	RWX	RX_PRBS_CHECK_SYNC: This bit enables checking for the 12/24 UI scramble synchronization pulse in the descramble PRBS block. 0b0 = Disable checking (forces prbs_sync_done to 0). 0b1 = Enable checking (prbs_sync_done may go to 1 after identifying the sync pulse).
55	RWX	RX_PRBS_SEED_DDC: Set this bit to enable seeding of the DDC PRBS block from the data pipe output (either the data stream or the descramble PRBS block depending on the value of rx_pipe_sel).
56	RWX	RX_PRBS_SEED_DFE: Set this bit to enable seeding of the DFE PRBS block. Related to this is rx_dfe_force_load_seed, which loads from the incoming data stream when 0 or from the rx_prbs_seed_value_* when 1.
57	RWX	RX_DFE_FORCE_LOAD_SEED: Set this bit to force rx_prbs_seed_value_0_15 and rx_prbs_seed_value_16_22 to load directly into the DFE history vector in the analog front-end for this lane. **Note:** The rx_prbs_seed_value_* bits are extended by 1 bit and shifted by a fixed value to match the pipeline delays between the analog front end and the receive PRBS descrambler. To set the DFE history vector to a specific value, the user must reverse that transformation to determine the value to write to the rx_prbs_seed_value_* to get the desired result in the vector.
58	RWX	RX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
59:60	RWX	RX_IOCLK_SLIP: This field provides software control of the receive slice deserializer IOCLK slip control. Use this to slip the deserilizer by 2N beats.
61	RWX	RX_IOCLK_SLIP_STROBE: This bit provides software control to execute IOCLK slip control.
62	RWX	RX_HISTORY_PRBS_POWER_UP: This bit forces the power up of the additional analog history latches used for PRBS generation when performing H2 - 12 calibration.
63	RWX	RX_PSAVE_RESYNC_DISABLE: This bit disables the resynchronize machine for this physical lane without disabling psave mode entirely.

Register Name	**Receive Bit CNTLX1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	8002400A0601143F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49	RWX	RX_LANE_INVERT: This bit inverts the receive lane data.
50	RWX	RX_LANE_INVALID: This bit marks this receive slice as invalid and fences other operations. Use this bit, for example, to broadcast a setting to all good lanes but not bad or disabled ones.

Bits	SCOM	Field Mnemonic: Description
51	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic. 0b0 = Data. 0b1 = Descrambler output.
52	RO	constant = 0b0
53	RWX	RX_PDWN_LITE: When set, this bit partially powers down unused spare lanes when not being recalibrated.
54	RWX	RX_PRBS_CHECK_SYNC: This bit enables checking for the 12/24 UI scramble synchronization pulse in the descramble PRBS block. 0b0 = Disable checking (forces prbs_sync_done to 0). 0b1 = Enable checking (prbs_sync_done may go to 1 after identifying the sync pulse).
55	RWX	RX_PRBS_SEED_DDC: Set this bit to enable seeding of the DDC PRBS block from the data pipe output (either the data stream or the descramble PRBS block depending on the value of rx_pipe_sel).
56	RWX	RX_PRBS_SEED_DFE: Set this bit to enable seeding of the DFE PRBS block. Related to this is rx_dfe_force_load_seed, which loads from the incoming data stream when 0 or from the rx_prbs_seed_value_* when 1.
57	RWX	RX_DFE_FORCE_LOAD_SEED: Set this bit to force rx_prbs_seed_value_0_15 and rx_prbs_seed_value_16_22 to load directly into the DFE history vector in the analog front-end for this lane. **Note:** The rx_prbs_seed_value_* bits are extended by 1 bit and shifted by a fixed value to match the pipeline delays between the analog front end and the receive PRBS descrambler. To set the DFE history vector to a specific value, the user must reverse that transformation to determine the value to write to the rx_prbs_seed_value_* to get the desired result in the vector.
58	RWX	RX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
59:60	RWX	RX_IOCLK_SLIP: This field provides software control of the receive slice deserializer IOCLK slip control. Use this to slip the deserilizer by 2N beats.
61	RWX	RX_IOCLK_SLIP_STROBE: This bit provides software control to execute IOCLK slip control.
62	RWX	RX_HISTORY_PRBS_POWER_UP: This bit forces the power up of the additional analog history latches used for PRBS generation when performing H2 - 12 calibration.
63	RWX	RX_PSAVE_RESYNC_DISABLE: This bit disables the resynchronize machine for this physical lane without disabling psave mode entirely.

Register Name	**Receive Bit CNTLX1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	8002400B0601143F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49	RWX	RX_LANE_INVERT: This bit inverts the receive lane data.
50	RWX	RX_LANE_INVALID: This bit marks this receive slice as invalid and fences other operations. Use this bit, for example, to broadcast a setting to all good lanes but not bad or disabled ones.
51	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic. 0b0 = Data. 0b1 = Descrambler output.
52	RO	constant = 0b0
53	RWX	RX_PDWN_LITE: When set, this bit partially powers down unused spare lanes when not being recalibrated.

Bits	SCOM	Field Mnemonic: Description
54	RWX	RX_PRBS_CHECK_SYNC: This bit enables checking for the 12/24 UI scramble synchronization pulse in the descramble PRBS block. 0b0 = Disable checking (forces prbs_sync_done to 0). 0b1 = Enable checking (prbs_sync_done may go to 1 after identifying the sync pulse).
55	RWX	RX_PRBS_SEED_DDC: Set this bit to enable seeding of the DDC PRBS block from the data pipe output (either the data stream or the descramble PRBS block depending on the value of rx_pipe_sel).
56	RWX	RX_PRBS_SEED_DFE: Set this bit to enable seeding of the DFE PRBS block. Related to this is rx_dfe_force_load_seed, which loads from the incoming data stream when 0 or from the rx_prbs_seed_value_* when 1.
57	RWX	RX_DFE_FORCE_LOAD_SEED: Set this bit to force rx_prbs_seed_value_0_15 and rx_prbs_seed_value_16_22 to load directly into the DFE history vector in the analog front-end for this lane. **Note:** The rx_prbs_seed_value_* bits are extended by 1 bit and shifted by a fixed value to match the pipeline delays between the analog front end and the receive PRBS descrambler. To set the DFE history vector to a specific value, the user must reverse that transformation to determine the value to write to the rx_prbs_seed_value_* to get the desired result in the vector.
58	RWX	RX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
59:60	RWX	RX_IOCLK_SLIP: This field provides software control of the receive slice deserializer IOCLK slip control. Use this to slip the deserilizer by 2N beats.
61	RWX	RX_IOCLK_SLIP_STROBE: This bit provides software control to execute IOCLK slip control.
62	RWX	RX_HISTORY_PRBS_POWER_UP: This bit forces the power up of the additional analog history latches used for PRBS generation when performing H2 - 12 calibration.
63	RWX	RX_PSAVE_RESYNC_DISABLE: This bit disables the resynchronize machine for this physical lane without disabling psave mode entirely.

Register Name	Receive Bit CNTLX1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	8002400C0601143F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49	RWX	RX_LANE_INVERT: This bit inverts the receive lane data.
50	RWX	RX_LANE_INVALID: This bit marks this receive slice as invalid and fences other operations. Use this bit, for example, to broadcast a setting to all good lanes but not bad or disabled ones.
51	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic. 0b0 = Data. 0b1 = Descrambler output.
52	RO	constant = 0b0
53	RWX	RX_PDWN_LITE: When set, this bit partially powers down unused spare lanes when not being recalibrated.
54	RWX	RX_PRBS_CHECK_SYNC: This bit enables checking for the 12/24 UI scramble synchronization pulse in the descramble PRBS block. 0b0 = Disable checking (forces prbs_sync_done to 0). 0b1 = Enable checking (prbs_sync_done may go to 1 after identifying the sync pulse).
55	RWX	RX_PRBS_SEED_DDC: Set this bit to enable seeding of the DDC PRBS block from the data pipe output (either the data stream or the descramble PRBS block depending on the value of rx_pipe_sel).

Bits	SCOM	Field Mnemonic: Description
56	RWX	RX_PRBS_SEED_DFE: Set this bit to enable seeding of the DFE PRBS block. Related to this is rx_dfe_force_load_seed, which loads from the incoming data stream when 0 or from the rx_prbs_seed_value_* when 1.
57	RWX	RX_DFE_FORCE_LOAD_SEED: Set this bit to force rx_prbs_seed_value_0_15 and rx_prbs_seed_value_16_22 to load directly into the DFE history vector in the analog front-end for this lane. **Note:** The rx_prbs_seed_value_* bits are extended by 1 bit and shifted by a fixed value to match the pipeline delays between the analog front end and the receive PRBS descrambler. To set the DFE history vector to a specific value, the user must reverse that transformation to determine the value to write to the rx_prbs_seed_value_* to get the desired result in the vector.
58	RWX	RX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
59:60	RWX	RX_IOCLK_SLIP: This field provides software control of the receive slice deserializer IOCLK slip control. Use this to slip the deserilizer by 2N beats.
61	RWX	RX_IOCLK_SLIP_STROBE: This bit provides software control to execute IOCLK slip control.
62	RWX	RX_HISTORY_PRBS_POWER_UP: This bit forces the power up of the additional analog history latches used for PRBS generation when performing H2 - 12 calibration.
63	RWX	RX_PSAVE_RESYNC_DISABLE: This bit disables the resynchronize machine for this physical lane without disabling psave mode entirely.

Register Name	**Receive Bit CNTLX1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	8002400D0601143F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49	RWX	RX_LANE_INVERT: This bit inverts the receive lane data.
50	RWX	RX_LANE_INVALID: This bit marks this receive slice as invalid and fences other operations. Use this bit, for example, to broadcast a setting to all good lanes but not bad or disabled ones.
51	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic. 0b0 = Data. 0b1 = Descrambler output.
52	RO	constant = 0b0
53	RWX	RX_PDWN_LITE: When set, this bit partially powers down unused spare lanes when not being recalibrated.
54	RWX	RX_PRBS_CHECK_SYNC: This bit enables checking for the 12/24 UI scramble synchronization pulse in the descramble PRBS block. 0b0 = Disable checking (forces prbs_sync_done to 0). 0b1 = Enable checking (prbs_sync_done may go to 1 after identifying the sync pulse).
55	RWX	RX_PRBS_SEED_DDC: Set this bit to enable seeding of the DDC PRBS block from the data pipe output (either the data stream or the descramble PRBS block depending on the value of rx_pipe_sel).
56	RWX	RX_PRBS_SEED_DFE: Set this bit to enable seeding of the DFE PRBS block. Related to this is rx_dfe_force_load_seed, which loads from the incoming data stream when 0 or from the rx_prbs_seed_value_* when 1.

Bits	SCOM	Field Mnemonic: Description
57	RWX	RX_DFE_FORCE_LOAD_SEED: Set this bit to force rx_prbs_seed_value_0_15 and rx_prbs_seed_value_16_22 to load directly into the DFE history vector in the analog front-end for this lane. **Note:** The rx_prbs_seed_value_* bits are extended by 1 bit and shifted by a fixed value to match the pipeline delays between the analog front end and the receive PRBS descrambler. To set the DFE history vector to a specific value, the user must reverse that transformation to determine the value to write to the rx_prbs_seed_value_* to get the desired result in the vector.
58	RWX	RX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
59:60	RWX	RX_IOCLK_SLIP: This field provides software control of the receive slice deserializer IOCLK slip control. Use this to slip the deserilizer by 2N beats.
61	RWX	RX_IOCLK_SLIP_STROBE: This bit provides software control to execute IOCLK slip control.
62	RWX	RX_HISTORY_PRBS_POWER_UP: This bit forces the power up of the additional analog history latches used for PRBS generation when performing H2 - 12 calibration.
63	RWX	RX_PSAVE_RESYNC_DISABLE: This bit disables the resynchronize machine for this physical lane without disabling psave mode entirely.

Register Name	Receive Bit CNTLX1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	8002400E0601143F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49	RWX	RX_LANE_INVERT: This bit inverts the receive lane data.
50	RWX	RX_LANE_INVALID: This bit marks this receive slice as invalid and fences other operations. Use this bit, for example, to broadcast a setting to all good lanes but not bad or disabled ones.
51	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic. 0b0 = Data. 0b1 = Descrambler output.
52	RO	constant = 0b0
53	RWX	RX_PDWN_LITE: When set, this bit partially powers down unused spare lanes when not being recalibrated.
54	RWX	RX_PRBS_CHECK_SYNC: This bit enables checking for the 12/24 UI scramble synchronization pulse in the descramble PRBS block. 0b0 = Disable checking (forces prbs_sync_done to 0). 0b1 = Enable checking (prbs_sync_done may go to 1 after identifying the sync pulse).
55	RWX	RX_PRBS_SEED_DDC: Set this bit to enable seeding of the DDC PRBS block from the data pipe output (either the data stream or the descramble PRBS block depending on the value of rx_pipe_sel).
56	RWX	RX_PRBS_SEED_DFE: Set this bit to enable seeding of the DFE PRBS block. Related to this is rx_dfe_force_load_seed, which loads from the incoming data stream when 0 or from the rx_prbs_seed_value_* when 1.
57	RWX	RX_DFE_FORCE_LOAD_SEED: Set this bit to force rx_prbs_seed_value_0_15 and rx_prbs_seed_value_16_22 to load directly into the DFE history vector in the analog front-end for this lane. **Note:** The rx_prbs_seed_value_* bits are extended by 1 bit and shifted by a fixed value to match the pipeline delays between the analog front end and the receive PRBS descrambler. To set the DFE history vector to a specific value, the user must reverse that transformation to determine the value to write to the rx_prbs_seed_value_* to get the desired result in the vector.
58	RWX	RX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.

Bits	SCOM	Field Mnemonic: Description
59:60	RWX	RX_IOCLK_SLIP: This field provides software control of the receive slice deserializer IOCLK slip control. Use this to slip the deserilizer by 2N beats.
61	RWX	RX_IOCLK_SLIP_STROBE: This bit provides software control to execute IOCLK slip control.
62	RWX	RX_HISTORY_PRBS_POWER_UP: This bit forces the power up of the additional analog history latches used for PRBS generation when performing H2 - 12 calibration.
63	RWX	RX_PSAVE_RESYNC_DISABLE: This bit disables the resynchronize machine for this physical lane without disabling psave mode entirely.

Register Name	**Receive Bit CNTLX1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	8002400F0601143F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49	RWX	RX_LANE_INVERT: This bit inverts the receive lane data.
50	RWX	RX_LANE_INVALID: This bit marks this receive slice as invalid and fences other operations. Use this bit, for example, to broadcast a setting to all good lanes but not bad or disabled ones.
51	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic. 0b0 = Data. 0b1 = Descrambler output.
52	RO	constant = 0b0
53	RWX	RX_PDWN_LITE: When set, this bit partially powers down unused spare lanes when not being recalibrated.
54	RWX	RX_PRBS_CHECK_SYNC: This bit enables checking for the 12/24 UI scramble synchronization pulse in the descramble PRBS block. 0b0 = Disable checking (forces prbs_sync_done to 0). 0b1 = Enable checking (prbs_sync_done may go to 1 after identifying the sync pulse).
55	RWX	RX_PRBS_SEED_DDC: Set this bit to enable seeding of the DDC PRBS block from the data pipe output (either the data stream or the descramble PRBS block depending on the value of rx_pipe_sel).
56	RWX	RX_PRBS_SEED_DFE: Set this bit to enable seeding of the DFE PRBS block. Related to this is rx_dfe_force_load_seed, which loads from the incoming data stream when 0 or from the rx_prbs_seed_value_* when 1.
57	RWX	RX_DFE_FORCE_LOAD_SEED: Set this bit to force rx_prbs_seed_value_0_15 and rx_prbs_seed_value_16_22 to load directly into the DFE history vector in the analog front-end for this lane. **Note:** The rx_prbs_seed_value_* bits are extended by 1 bit and shifted by a fixed value to match the pipeline delays between the analog front end and the receive PRBS descrambler. To set the DFE history vector to a specific value, the user must reverse that transformation to determine the value to write to the rx_prbs_seed_value_* to get the desired result in the vector.
58	RWX	RX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
59:60	RWX	RX_IOCLK_SLIP: This field provides software control of the receive slice deserializer IOCLK slip control. Use this to slip the deserilizer by 2N beats.
61	RWX	RX_IOCLK_SLIP_STROBE: This bit provides software control to execute IOCLK slip control.
62	RWX	RX_HISTORY_PRBS_POWER_UP: This bit forces the power up of the additional analog history latches used for PRBS generation when performing H2 - 12 calibration.

Bits	SCOM	Field Mnemonic: Description
63	RWX	RX_PSAVE_RESYNC_DISABLE: This bit disables the resynchronize machine for this physical lane without disabling psave mode entirely.

Register Name	Receive Bit CNTLX1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	800240100601143F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49	RWX	RX_LANE_INVERT: This bit inverts the receive lane data.
50	RWX	RX_LANE_INVALID: This bit marks this receive slice as invalid and fences other operations. Use this bit, for example, to broadcast a setting to all good lanes but not bad or disabled ones.
51	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic. 0b0 = Data. 0b1 = Descrambler output.
52	RO	constant = 0b0
53	RWX	RX_PDWN_LITE: When set, this bit partially powers down unused spare lanes when not being recalibrated.
54	RWX	RX_PRBS_CHECK_SYNC: This bit enables checking for the 12/24 UI scramble synchronization pulse in the descramble PRBS block. 0b0 = Disable checking (forces prbs_sync_done to 0). 0b1 = Enable checking (prbs_sync_done may go to 1 after identifying the sync pulse).
55	RWX	RX_PRBS_SEED_DDC: Set this bit to enable seeding of the DDC PRBS block from the data pipe output (either the data stream or the descramble PRBS block depending on the value of rx_pipe_sel).
56	RWX	RX_PRBS_SEED_DFE: Set this bit to enable seeding of the DFE PRBS block. Related to this is rx_dfe_force_load_seed, which loads from the incoming data stream when 0 or from the rx_prbs_seed_value_* when 1.
57	RWX	RX_DFE_FORCE_LOAD_SEED: Set this bit to force rx_prbs_seed_value_0_15 and rx_prbs_seed_value_16_22 to load directly into the DFE history vector in the analog front-end for this lane. **Note:** The rx_prbs_seed_value_* bits are extended by 1 bit and shifted by a fixed value to match the pipeline delays between the analog front end and the receive PRBS descrambler. To set the DFE history vector to a specific value, the user must reverse that transformation to determine the value to write to the rx_prbs_seed_value_* to get the desired result in the vector.
58	RWX	RX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
59:60	RWX	RX_IOCLK_SLIP: This field provides software control of the receive slice deserializer IOCLK slip control. Use this to slip the deserilizer by 2N beats.
61	RWX	RX_IOCLK_SLIP_STROBE: This bit provides software control to execute IOCLK slip control.
62	RWX	RX_HISTORY_PRBS_POWER_UP: This bit forces the power up of the additional analog history latches used for PRBS generation when performing H2 - 12 calibration.
63	RWX	RX_PSAVE_RESYNC_DISABLE: This bit disables the resynchronize machine for this physical lane without disabling psave mode entirely.

Register Name	Receive Bit CNTLX1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	800240110601143F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49	RWX	RX_LANE_INVERT: This bit inverts the receive lane data.
50	RWX	RX_LANE_INVALID: This bit marks this receive slice as invalid and fences other operations. Use this bit, for example, to broadcast a setting to all good lanes but not bad or disabled ones.
51	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic. 0b0 = Data. 0b1 = Descrambler output.
52	RO	constant = 0b0
53	RWX	RX_PDWN_LITE: When set, this bit partially powers down unused spare lanes when not being recalibrated.
54	RWX	RX_PRBS_CHECK_SYNC: This bit enables checking for the 12/24 UI scramble synchronization pulse in the descramble PRBS block. 0b0 = Disable checking (forces prbs_sync_done to 0). 0b1 = Enable checking (prbs_sync_done may go to 1 after identifying the sync pulse).
55	RWX	RX_PRBS_SEED_DDC: Set this bit to enable seeding of the DDC PRBS block from the data pipe output (either the data stream or the descramble PRBS block depending on the value of rx_pipe_sel).
56	RWX	RX_PRBS_SEED_DFE: Set this bit to enable seeding of the DFE PRBS block. Related to this is rx_dfe_force_load_seed, which loads from the incoming data stream when 0 or from the rx_prbs_seed_value_* when 1.
57	RWX	RX_DFE_FORCE_LOAD_SEED: Set this bit to force rx_prbs_seed_value_0_15 and rx_prbs_seed_value_16_22 to load directly into the DFE history vector in the analog front-end for this lane. **Note:** The rx_prbs_seed_value_* bits are extended by 1 bit and shifted by a fixed value to match the pipeline delays between the analog front end and the receive PRBS descrambler. To set the DFE history vector to a specific value, the user must reverse that transformation to determine the value to write to the rx_prbs_seed_value_* to get the desired result in the vector.
58	RWX	RX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
59:60	RWX	RX_IOCLK_SLIP: This field provides software control of the receive slice deserializer IOCLK slip control. Use this to slip the deserilizer by 2N beats.
61	RWX	RX_IOCLK_SLIP_STROBE: This bit provides software control to execute IOCLK slip control.
62	RWX	RX_HISTORY_PRBS_POWER_UP: This bit forces the power up of the additional analog history latches used for PRBS generation when performing H2 - 12 calibration.
63	RWX	RX_PSAVE_RESYNC_DISABLE: This bit disables the resynchronize machine for this physical lane without disabling psave mode entirely.

Register Name	Receive Bit CNTLX1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	800240200601143F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49	RWX	RX_LANE_INVERT: This bit inverts the receive lane data.
50	RWX	RX_LANE_INVALID: This bit marks this receive slice as invalid and fences other operations. Use this bit, for example, to broadcast a setting to all good lanes but not bad or disabled ones.
51	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic. 0b0 = Data. 0b1 = Descrambler output.
52	RO	constant = 0b0
53	RWX	RX_PDWN_LITE: When set, this bit partially powers down unused spare lanes when not being recalibrated.
54	RWX	RX_PRBS_CHECK_SYNC: This bit enables checking for the 12/24 UI scramble synchronization pulse in the descramble PRBS block. 0b0 = Disable checking (forces prbs_sync_done to 0). 0b1 = Enable checking (prbs_sync_done may go to 1 after identifying the sync pulse).
55	RWX	RX_PRBS_SEED_DDC: Set this bit to enable seeding of the DDC PRBS block from the data pipe output (either the data stream or the descramble PRBS block depending on the value of rx_pipe_sel).
56	RWX	RX_PRBS_SEED_DFE: Set this bit to enable seeding of the DFE PRBS block. Related to this is rx_dfe_force_load_seed, which loads from the incoming data stream when 0 or from the rx_prbs_seed_value_* when 1.
57	RWX	RX_DFE_FORCE_LOAD_SEED: Set this bit to force rx_prbs_seed_value_0_15 and rx_prbs_seed_value_16_22 to load directly into the DFE history vector in the analog front-end for this lane. **Note:** The rx_prbs_seed_value_* bits are extended by 1 bit and shifted by a fixed value to match the pipeline delays between the analog front end and the receive PRBS descrambler. To set the DFE history vector to a specific value, the user must reverse that transformation to determine the value to write to the rx_prbs_seed_value_* to get the desired result in the vector.
58	RWX	RX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
59:60	RWX	RX_IOCLK_SLIP: This field provides software control of the receive slice deserializer IOCLK slip control. Use this to slip the deserilizer by 2N beats.
61	RWX	RX_IOCLK_SLIP_STROBE: This bit provides software control to execute IOCLK slip control.
62	RWX	RX_HISTORY_PRBS_POWER_UP: This bit forces the power up of the additional analog history latches used for PRBS generation when performing H2 - 12 calibration.
63	RWX	RX_PSAVE_RESYNC_DISABLE: This bit disables the resynchronize machine for this physical lane without disabling psave mode entirely.

Register Name	**Receive Bit CNTLX1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	800240210601143F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49	RWX	RX_LANE_INVERT: This bit inverts the receive lane data.
50	RWX	RX_LANE_INVALID: This bit marks this receive slice as invalid and fences other operations. Use this bit, for example, to broadcast a setting to all good lanes but not bad or disabled ones.

Bits	SCOM	Field Mnemonic: Description
51	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic. 0b0 = Data. 0b1 = Descrambler output.
52	RO	constant = 0b0
53	RWX	RX_PDWN_LITE: When set, this bit partially powers down unused spare lanes when not being recalibrated.
54	RWX	RX_PRBS_CHECK_SYNC: This bit enables checking for the 12/24 UI scramble synchronization pulse in the descramble PRBS block. 0b0 = Disable checking (forces prbs_sync_done to 0). 0b1 = Enable checking (prbs_sync_done may go to 1 after identifying the sync pulse).
55	RWX	RX_PRBS_SEED_DDC: Set this bit to enable seeding of the DDC PRBS block from the data pipe output (either the data stream or the descramble PRBS block depending on the value of rx_pipe_sel).
56	RWX	RX_PRBS_SEED_DFE: Set this bit to enable seeding of the DFE PRBS block. Related to this is rx_dfe_force_load_seed, which loads from the incoming data stream when 0 or from the rx_prbs_seed_value_* when 1.
57	RWX	RX_DFE_FORCE_LOAD_SEED: Set this bit to force rx_prbs_seed_value_0_15 and rx_prbs_seed_value_16_22 to load directly into the DFE history vector in the analog front-end for this lane. **Note:** The rx_prbs_seed_value_* bits are extended by 1 bit and shifted by a fixed value to match the pipeline delays between the analog front end and the receive PRBS descrambler. To set the DFE history vector to a specific value, the user must reverse that transformation to determine the value to write to the rx_prbs_seed_value_* to get the desired result in the vector.
58	RWX	RX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
59:60	RWX	RX_IOCLK_SLIP: This field provides software control of the receive slice deserializer IOCLK slip control. Use this to slip the deserilizer by 2N beats.
61	RWX	RX_IOCLK_SLIP_STROBE: This bit provides software control to execute IOCLK slip control.
62	RWX	RX_HISTORY_PRBS_POWER_UP: This bit forces the power up of the additional analog history latches used for PRBS generation when performing H2 - 12 calibration.
63	RWX	RX_PSAVE_RESYNC_DISABLE: This bit disables the resynchronize machine for this physical lane without disabling psave mode entirely.

Register Name	**Receive Bit CNTLX1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	800240220601143F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49	RWX	RX_LANE_INVERT: This bit inverts the receive lane data.
50	RWX	RX_LANE_INVALID: This bit marks this receive slice as invalid and fences other operations. Use this bit, for example, to broadcast a setting to all good lanes but not bad or disabled ones.
51	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic. 0b0 = Data. 0b1 = Descrambler output.
52	RO	constant = 0b0
53	RWX	RX_PDWN_LITE: When set, this bit partially powers down unused spare lanes when not being recalibrated.

Bits	SCOM	Field Mnemonic: Description
54	RWX	RX_PRBS_CHECK_SYNC: This bit enables checking for the 12/24 UI scramble synchronization pulse in the descramble PRBS block. 0b0 = Disable checking (forces prbs_sync_done to 0). 0b1 = Enable checking (prbs_sync_done may go to 1 after identifying the sync pulse).
55	RWX	RX_PRBS_SEED_DDC: Set this bit to enable seeding of the DDC PRBS block from the data pipe output (either the data stream or the descramble PRBS block depending on the value of rx_pipe_sel).
56	RWX	RX_PRBS_SEED_DFE: Set this bit to enable seeding of the DFE PRBS block. Related to this is rx_dfe_force_load_seed, which loads from the incoming data stream when 0 or from the rx_prbs_seed_value_* when 1.
57	RWX	RX_DFE_FORCE_LOAD_SEED: Set this bit to force rx_prbs_seed_value_0_15 and rx_prbs_seed_value_16_22 to load directly into the DFE history vector in the analog front-end for this lane. **Note:** The rx_prbs_seed_value_* bits are extended by 1 bit and shifted by a fixed value to match the pipeline delays between the analog front end and the receive PRBS descrambler. To set the DFE history vector to a specific value, the user must reverse that transformation to determine the value to write to the rx_prbs_seed_value_* to get the desired result in the vector.
58	RWX	RX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
59:60	RWX	RX_IOCLK_SLIP: This field provides software control of the receive slice deserializer IOCLK slip control. Use this to slip the deserilizer by 2N beats.
61	RWX	RX_IOCLK_SLIP_STROBE: This bit provides software control to execute IOCLK slip control.
62	RWX	RX_HISTORY_PRBS_POWER_UP: This bit forces the power up of the additional analog history latches used for PRBS generation when performing H2 - 12 calibration.
63	RWX	RX_PSAVE_RESYNC_DISABLE: This bit disables the resynchronize machine for this physical lane without disabling psave mode entirely.

Register Name	**Receive Bit CNTLX1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	800240230601143F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49	RWX	RX_LANE_INVERT: This bit inverts the receive lane data.
50	RWX	RX_LANE_INVALID: This bit marks this receive slice as invalid and fences other operations. Use this bit, for example, to broadcast a setting to all good lanes but not bad or disabled ones.
51	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic. 0b0 = Data. 0b1 = Descrambler output.
52	RO	constant = 0b0
53	RWX	RX_PDWN_LITE: When set, this bit partially powers down unused spare lanes when not being recalibrated.
54	RWX	RX_PRBS_CHECK_SYNC: This bit enables checking for the 12/24 UI scramble synchronization pulse in the descramble PRBS block. 0b0 = Disable checking (forces prbs_sync_done to 0). 0b1 = Enable checking (prbs_sync_done may go to 1 after identifying the sync pulse).
55	RWX	RX_PRBS_SEED_DDC: Set this bit to enable seeding of the DDC PRBS block from the data pipe output (either the data stream or the descramble PRBS block depending on the value of rx_pipe_sel).

Bits	SCOM	Field Mnemonic: Description
56	RWX	RX_PRBS_SEED_DFE: Set this bit to enable seeding of the DFE PRBS block. Related to this is rx_dfe_force_load_seed, which loads from the incoming data stream when 0 or from the rx_prbs_seed_value_* when 1.
57	RWX	RX_DFE_FORCE_LOAD_SEED: Set this bit to force rx_prbs_seed_value_0_15 and rx_prbs_seed_value_16_22 to load directly into the DFE history vector in the analog front-end for this lane. **Note:** The rx_prbs_seed_value_* bits are extended by 1 bit and shifted by a fixed value to match the pipeline delays between the analog front end and the receive PRBS descrambler. To set the DFE history vector to a specific value, the user must reverse that transformation to determine the value to write to the rx_prbs_seed_value_* to get the desired result in the vector.
58	RWX	RX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
59:60	RWX	RX_IOCLK_SLIP: This field provides software control of the receive slice deserializer IOCLK slip control. Use this to slip the deserilizer by 2N beats.
61	RWX	RX_IOCLK_SLIP_STROBE: This bit provides software control to execute IOCLK slip control.
62	RWX	RX_HISTORY_PRBS_POWER_UP: This bit forces the power up of the additional analog history latches used for PRBS generation when performing H2 - 12 calibration.
63	RWX	RX_PSAVE_RESYNC_DISABLE: This bit disables the resynchronize machine for this physical lane without disabling psave mode entirely.

Register Name	Receive Bit CNTLX1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	800240240601143F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49	RWX	RX_LANE_INVERT: This bit inverts the receive lane data.
50	RWX	RX_LANE_INVALID: This bit marks this receive slice as invalid and fences other operations. Use this bit, for example, to broadcast a setting to all good lanes but not bad or disabled ones.
51	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic. 0b0 = Data. 0b1 = Descrambler output.
52	RO	constant = 0b0
53	RWX	RX_PDWN_LITE: When set, this bit partially powers down unused spare lanes when not being recalibrated.
54	RWX	RX_PRBS_CHECK_SYNC: This bit enables checking for the 12/24 UI scramble synchronization pulse in the descramble PRBS block. 0b0 = Disable checking (forces prbs_sync_done to 0). 0b1 = Enable checking (prbs_sync_done may go to 1 after identifying the sync pulse).
55	RWX	RX_PRBS_SEED_DDC: Set this bit to enable seeding of the DDC PRBS block from the data pipe output (either the data stream or the descramble PRBS block depending on the value of rx_pipe_sel).
56	RWX	RX_PRBS_SEED_DFE: Set this bit to enable seeding of the DFE PRBS block. Related to this is rx_dfe_force_load_seed, which loads from the incoming data stream when 0 or from the rx_prbs_seed_value_* when 1.

Bits	SCOM	Field Mnemonic: Description
57	RWX	RX_DFE_FORCE_LOAD_SEED: Set this bit to force rx_prbs_seed_value_0_15 and rx_prbs_seed_value_16_22 to load directly into the DFE history vector in the analog front-end for this lane. **Note:** The rx_prbs_seed_value_* bits are extended by 1 bit and shifted by a fixed value to match the pipeline delays between the analog front end and the receive PRBS descrambler. To set the DFE history vector to a specific value, the user must reverse that transformation to determine the value to write to the rx_prbs_seed_value_* to get the desired result in the vector.
58	RWX	RX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
59:60	RWX	RX_IOCLK_SLIP: This field provides software control of the receive slice deserializer IOCLK slip control. Use this to slip the deserilizer by 2N beats.
61	RWX	RX_IOCLK_SLIP_STROBE: This bit provides software control to execute IOCLK slip control.
62	RWX	RX_HISTORY_PRBS_POWER_UP: This bit forces the power up of the additional analog history latches used for PRBS generation when performing H2 - 12 calibration.
63	RWX	RX_PSAVE_RESYNC_DISABLE: This bit disables the resynchronize machine for this physical lane without disabling psave mode entirely.

Register Name	Receive Bit CNTLX1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	800240250601143F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49	RWX	RX_LANE_INVERT: This bit inverts the receive lane data.
50	RWX	RX_LANE_INVALID: This bit marks this receive slice as invalid and fences other operations. Use this bit, for example, to broadcast a setting to all good lanes but not bad or disabled ones.
51	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic. 0b0 = Data. 0b1 = Descrambler output.
52	RO	constant = 0b0
53	RWX	RX_PDWN_LITE: When set, this bit partially powers down unused spare lanes when not being recalibrated.
54	RWX	RX_PRBS_CHECK_SYNC: This bit enables checking for the 12/24 UI scramble synchronization pulse in the descramble PRBS block. 0b0 = Disable checking (forces prbs_sync_done to 0). 0b1 = Enable checking (prbs_sync_done may go to 1 after identifying the sync pulse).
55	RWX	RX_PRBS_SEED_DDC: Set this bit to enable seeding of the DDC PRBS block from the data pipe output (either the data stream or the descramble PRBS block depending on the value of rx_pipe_sel).
56	RWX	RX_PRBS_SEED_DFE: Set this bit to enable seeding of the DFE PRBS block. Related to this is rx_dfe_force_load_seed, which loads from the incoming data stream when 0 or from the rx_prbs_seed_value_* when 1.
57	RWX	RX_DFE_FORCE_LOAD_SEED: Set this bit to force rx_prbs_seed_value_0_15 and rx_prbs_seed_value_16_22 to load directly into the DFE history vector in the analog front-end for this lane. **Note:** The rx_prbs_seed_value_* bits are extended by 1 bit and shifted by a fixed value to match the pipeline delays between the analog front end and the receive PRBS descrambler. To set the DFE history vector to a specific value, the user must reverse that transformation to determine the value to write to the rx_prbs_seed_value_* to get the desired result in the vector.
58	RWX	RX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.

Bits	SCOM	Field Mnemonic: Description
59:60	RWX	RX_IOCLK_SLIP: This field provides software control of the receive slice deserializer IOCLK slip control. Use this to slip the deserilizer by 2N beats.
61	RWX	RX_IOCLK_SLIP_STROBE: This bit provides software control to execute IOCLK slip control.
62	RWX	RX_HISTORY_PRBS_POWER_UP: This bit forces the power up of the additional analog history latches used for PRBS generation when performing H2 - 12 calibration.
63	RWX	RX_PSAVE_RESYNC_DISABLE: This bit disables the resynchronize machine for this physical lane without disabling psave mode entirely.

Register Name	Receive Bit CNTLX1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	800240260601143F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49	RWX	RX_LANE_INVERT: This bit inverts the receive lane data.
50	RWX	RX_LANE_INVALID: This bit marks this receive slice as invalid and fences other operations. Use this bit, for example, to broadcast a setting to all good lanes but not bad or disabled ones.
51	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic. 0b0 = Data. 0b1 = Descrambler output.
52	RO	constant = 0b0
53	RWX	RX_PDWN_LITE: When set, this bit partially powers down unused spare lanes when not being recalibrated.
54	RWX	RX_PRBS_CHECK_SYNC: This bit enables checking for the 12/24 UI scramble synchronization pulse in the descramble PRBS block. 0b0 = Disable checking (forces prbs_sync_done to 0). 0b1 = Enable checking (prbs_sync_done may go to 1 after identifying the sync pulse).
55	RWX	RX_PRBS_SEED_DDC: Set this bit to enable seeding of the DDC PRBS block from the data pipe output (either the data stream or the descramble PRBS block depending on the value of rx_pipe_sel).
56	RWX	RX_PRBS_SEED_DFE: Set this bit to enable seeding of the DFE PRBS block. Related to this is rx_dfe_force_load_seed, which loads from the incoming data stream when 0 or from the rx_prbs_seed_value_* when 1.
57	RWX	RX_DFE_FORCE_LOAD_SEED: Set this bit to force rx_prbs_seed_value_0_15 and rx_prbs_seed_value_16_22 to load directly into the DFE history vector in the analog front-end for this lane. **Note:** The rx_prbs_seed_value_* bits are extended by 1 bit and shifted by a fixed value to match the pipeline delays between the analog front end and the receive PRBS descrambler. To set the DFE history vector to a specific value, the user must reverse that transformation to determine the value to write to the rx_prbs_seed_value_* to get the desired result in the vector.
58	RWX	RX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
59:60	RWX	RX_IOCLK_SLIP: This field provides software control of the receive slice deserializer IOCLK slip control. Use this to slip the deserilizer by 2N beats.
61	RWX	RX_IOCLK_SLIP_STROBE: This bit provides software control to execute IOCLK slip control.
62	RWX	RX_HISTORY_PRBS_POWER_UP: This bit forces the power up of the additional analog history latches used for PRBS generation when performing H2 - 12 calibration.

Bits	SCOM	Field Mnemonic: Description
63	RWX	RX_PSAVE_RESYNC_DISABLE: This bit disables the resynchronize machine for this physical lane without disabling psave mode entirely.

Register Name	**Receive Bit CNTLX1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	800240270601143F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49	RWX	RX_LANE_INVERT: This bit inverts the receive lane data.
50	RWX	RX_LANE_INVALID: This bit marks this receive slice as invalid and fences other operations. Use this bit, for example, to broadcast a setting to all good lanes but not bad or disabled ones.
51	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic. 0b0 = Data. 0b1 = Descrambler output.
52	RO	constant = 0b0
53	RWX	RX_PDWN_LITE: When set, this bit partially powers down unused spare lanes when not being recalibrated.
54	RWX	RX_PRBS_CHECK_SYNC: This bit enables checking for the 12/24 UI scramble synchronization pulse in the descramble PRBS block. 0b0 = Disable checking (forces prbs_sync_done to 0). 0b1 = Enable checking (prbs_sync_done may go to 1 after identifying the sync pulse).
55	RWX	RX_PRBS_SEED_DDC: Set this bit to enable seeding of the DDC PRBS block from the data pipe output (either the data stream or the descramble PRBS block depending on the value of rx_pipe_sel).
56	RWX	RX_PRBS_SEED_DFE: Set this bit to enable seeding of the DFE PRBS block. Related to this is rx_dfe_force_load_seed, which loads from the incoming data stream when 0 or from the rx_prbs_seed_value_* when 1.
57	RWX	RX_DFE_FORCE_LOAD_SEED: Set this bit to force rx_prbs_seed_value_0_15 and rx_prbs_seed_value_16_22 to load directly into the DFE history vector in the analog front-end for this lane. **Note:** The rx_prbs_seed_value_* bits are extended by 1 bit and shifted by a fixed value to match the pipeline delays between the analog front end and the receive PRBS descrambler. To set the DFE history vector to a specific value, the user must reverse that transformation to determine the value to write to the rx_prbs_seed_value_* to get the desired result in the vector.
58	RWX	RX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
59:60	RWX	RX_IOCLK_SLIP: This field provides software control of the receive slice deserializer IOCLK slip control. Use this to slip the deserilizer by 2N beats.
61	RWX	RX_IOCLK_SLIP_STROBE: This bit provides software control to execute IOCLK slip control.
62	RWX	RX_HISTORY_PRBS_POWER_UP: This bit forces the power up of the additional analog history latches used for PRBS generation when performing H2 - 12 calibration.
63	RWX	RX_PSAVE_RESYNC_DISABLE: This bit disables the resynchronize machine for this physical lane without disabling psave mode entirely.

Register Name	Receive Bit CNTLX1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	800240280601143F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49	RWX	RX_LANE_INVERT: This bit inverts the receive lane data.
50	RWX	RX_LANE_INVALID: This bit marks this receive slice as invalid and fences other operations. Use this bit, for example, to broadcast a setting to all good lanes but not bad or disabled ones.
51	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic. 0b0 = Data. 0b1 = Descrambler output.
52	RO	constant = 0b0
53	RWX	RX_PDWN_LITE: When set, this bit partially powers down unused spare lanes when not being recalibrated.
54	RWX	RX_PRBS_CHECK_SYNC: This bit enables checking for the 12/24 UI scramble synchronization pulse in the descramble PRBS block. 0b0 = Disable checking (forces prbs_sync_done to 0). 0b1 = Enable checking (prbs_sync_done may go to 1 after identifying the sync pulse).
55	RWX	RX_PRBS_SEED_DDC: Set this bit to enable seeding of the DDC PRBS block from the data pipe output (either the data stream or the descramble PRBS block depending on the value of rx_pipe_sel).
56	RWX	RX_PRBS_SEED_DFE: Set this bit to enable seeding of the DFE PRBS block. Related to this is rx_dfe_force_load_seed, which loads from the incoming data stream when 0 or from the rx_prbs_seed_value_* when 1.
57	RWX	RX_DFE_FORCE_LOAD_SEED: Set this bit to force rx_prbs_seed_value_0_15 and rx_prbs_seed_value_16_22 to load directly into the DFE history vector in the analog front-end for this lane. **Note:** The rx_prbs_seed_value_* bits are extended by 1 bit and shifted by a fixed value to match the pipeline delays between the analog front end and the receive PRBS descrambler. To set the DFE history vector to a specific value, the user must reverse that transformation to determine the value to write to the rx_prbs_seed_value_* to get the desired result in the vector.
58	RWX	RX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
59:60	RWX	RX_IOCLK_SLIP: This field provides software control of the receive slice deserializer IOCLK slip control. Use this to slip the deserilizer by 2N beats.
61	RWX	RX_IOCLK_SLIP_STROBE: This bit provides software control to execute IOCLK slip control.
62	RWX	RX_HISTORY_PRBS_POWER_UP: This bit forces the power up of the additional analog history latches used for PRBS generation when performing H2 - 12 calibration.
63	RWX	RX_PSAVE_RESYNC_DISABLE: This bit disables the resynchronize machine for this physical lane without disabling psave mode entirely.

Register Name	Receive Bit CNTLX1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	800240290601143F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49	RWX	RX_LANE_INVERT: This bit inverts the receive lane data.
50	RWX	RX_LANE_INVALID: This bit marks this receive slice as invalid and fences other operations. Use this bit, for example, to broadcast a setting to all good lanes but not bad or disabled ones.
51	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic. 0b0 = Data. 0b1 = Descrambler output.
52	RO	constant = 0b0
53	RWX	RX_PDWN_LITE: When set, this bit partially powers down unused spare lanes when not being recalibrated.
54	RWX	RX_PRBS_CHECK_SYNC: This bit enables checking for the 12/24 UI scramble synchronization pulse in the descramble PRBS block. 0b0 = Disable checking (forces prbs_sync_done to 0). 0b1 = Enable checking (prbs_sync_done may go to 1 after identifying the sync pulse).
55	RWX	RX_PRBS_SEED_DDC: Set this bit to enable seeding of the DDC PRBS block from the data pipe output (either the data stream or the descramble PRBS block depending on the value of rx_pipe_sel).
56	RWX	RX_PRBS_SEED_DFE: Set this bit to enable seeding of the DFE PRBS block. Related to this is rx_dfe_force_load_seed, which loads from the incoming data stream when 0 or from the rx_prbs_seed_value_* when 1.
57	RWX	RX_DFE_FORCE_LOAD_SEED: Set this bit to force rx_prbs_seed_value_0_15 and rx_prbs_seed_value_16_22 to load directly into the DFE history vector in the analog front-end for this lane. **Note:** The rx_prbs_seed_value_* bits are extended by 1 bit and shifted by a fixed value to match the pipeline delays between the analog front end and the receive PRBS descrambler. To set the DFE history vector to a specific value, the user must reverse that transformation to determine the value to write to the rx_prbs_seed_value_* to get the desired result in the vector.
58	RWX	RX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
59:60	RWX	RX_IOCLK_SLIP: This field provides software control of the receive slice deserializer IOCLK slip control. Use this to slip the deserilizer by 2N beats.
61	RWX	RX_IOCLK_SLIP_STROBE: This bit provides software control to execute IOCLK slip control.

Bits	SCOM	Field Mnemonic: Description
62	RWX	RX_HISTORY_PRBS_POWER_UP: This bit forces the power up of the additional analog history latches used for PRBS generation when performing H2 - 12 calibration.
63	RWX	RX_PSAVE_RESYNC_DISABLE: This bit disables the resynchronize machine for this physical lane without disabling psave mode entirely.

Register Name	Receive Bit CNTLX1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	8002402A0601143F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49	RWX	RX_LANE_INVERT: This bit inverts the receive lane data.
50	RWX	RX_LANE_INVALID: This bit marks this receive slice as invalid and fences other operations. Use this bit, for example, to broadcast a setting to all good lanes but not bad or disabled ones.
51	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic. 0b0 = Data. 0b1 = Descrambler output.
52	RO	constant = 0b0
53	RWX	RX_PDWN_LITE: When set, this bit partially powers down unused spare lanes when not being recalibrated.
54	RWX	RX_PRBS_CHECK_SYNC: This bit enables checking for the 12/24 UI scramble synchronization pulse in the descramble PRBS block. 0b0 = Disable checking (forces prbs_sync_done to 0). 0b1 = Enable checking (prbs_sync_done may go to 1 after identifying the sync pulse).
55	RWX	RX_PRBS_SEED_DDC: Set this bit to enable seeding of the DDC PRBS block from the data pipe output (either the data stream or the descramble PRBS block depending on the value of rx_pipe_sel).
56	RWX	RX_PRBS_SEED_DFE: Set this bit to enable seeding of the DFE PRBS block. Related to this is rx_dfe_force_load_seed, which loads from the incoming data stream when 0 or from the rx_prbs_seed_value_* when 1.
57	RWX	RX_DFE_FORCE_LOAD_SEED: Set this bit to force rx_prbs_seed_value_0_15 and rx_prbs_seed_value_16_22 to load directly into the DFE history vector in the analog front-end for this lane. **Note:** The rx_prbs_seed_value_* bits are extended by 1 bit and shifted by a fixed value to match the pipeline delays between the analog front end and the receive PRBS descrambler. To set the DFE history vector to a specific value, the user must reverse that transformation to determine the value to write to the rx_prbs_seed_value_* to get the desired result in the vector.
58	RWX	RX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
59:60	RWX	RX_IOCLK_SLIP: This field provides software control of the receive slice deserializer IOCLK slip control. Use this to slip the deserilizer by 2N beats.
61	RWX	RX_IOCLK_SLIP_STROBE: This bit provides software control to execute IOCLK slip control.
62	RWX	RX_HISTORY_PRBS_POWER_UP: This bit forces the power up of the additional analog history latches used for PRBS generation when performing H2 - 12 calibration.
63	RWX	RX_PSAVE_RESYNC_DISABLE: This bit disables the resynchronize machine for this physical lane without disabling psave mode entirely.

Register Name	Receive Bit CNTLX1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	8002402B0601143F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49	RWX	RX_LANE_INVERT: This bit inverts the receive lane data.
50	RWX	RX_LANE_INVALID: This bit marks this receive slice as invalid and fences other operations. Use this bit, for example, to broadcast a setting to all good lanes but not bad or disabled ones.
51	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic. 0b0 = Data. 0b1 = Descrambler output.
52	RO	constant = 0b0
53	RWX	RX_PDWN_LITE: When set, this bit partially powers down unused spare lanes when not being recalibrated.
54	RWX	RX_PRBS_CHECK_SYNC: This bit enables checking for the 12/24 UI scramble synchronization pulse in the descramble PRBS block. 0b0 = Disable checking (forces prbs_sync_done to 0). 0b1 = Enable checking (prbs_sync_done may go to 1 after identifying the sync pulse).
55	RWX	RX_PRBS_SEED_DDC: Set this bit to enable seeding of the DDC PRBS block from the data pipe output (either the data stream or the descramble PRBS block depending on the value of rx_pipe_sel).
56	RWX	RX_PRBS_SEED_DFE: Set this bit to enable seeding of the DFE PRBS block. Related to this is rx_dfe_force_load_seed, which loads from the incoming data stream when 0 or from the rx_prbs_seed_value_* when 1.
57	RWX	RX_DFE_FORCE_LOAD_SEED: Set this bit to force rx_prbs_seed_value_0_15 and rx_prbs_seed_value_16_22 to load directly into the DFE history vector in the analog front-end for this lane. **Note:** The rx_prbs_seed_value_* bits are extended by 1 bit and shifted by a fixed value to match the pipeline delays between the analog front end and the receive PRBS descrambler. To set the DFE history vector to a specific value, the user must reverse that transformation to determine the value to write to the rx_prbs_seed_value_* to get the desired result in the vector.
58	RWX	RX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
59:60	RWX	RX_IOCLK_SLIP: This field provides software control of the receive slice deserializer IOCLK slip control. Use this to slip the deserilizer by 2N beats.
61	RWX	RX_IOCLK_SLIP_STROBE: This bit provides software control to execute IOCLK slip control.
62	RWX	RX_HISTORY_PRBS_POWER_UP: This bit forces the power up of the additional analog history latches used for PRBS generation when performing H2 - 12 calibration.
63	RWX	RX_PSAVE_RESYNC_DISABLE: This bit disables the resynchronize machine for this physical lane without disabling psave mode entirely.

Register Name	Receive Bit CNTLX1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	8002402C0601143F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49	RWX	RX_LANE_INVERT: This bit inverts the receive lane data.
50	RWX	RX_LANE_INVALID: This bit marks this receive slice as invalid and fences other operations. Use this bit, for example, to broadcast a setting to all good lanes but not bad or disabled ones.
51	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic. 0b0 = Data. 0b1 = Descrambler output.
52	RO	constant = 0b0
53	RWX	RX_PDWN_LITE: When set, this bit partially powers down unused spare lanes when not being recalibrated.

Bits	SCOM	Field Mnemonic: Description
54	RWX	RX_PRBS_CHECK_SYNC: This bit enables checking for the 12/24 UI scramble synchronization pulse in the descramble PRBS block. 0b0 = Disable checking (forces prbs_sync_done to 0). 0b1 = Enable checking (prbs_sync_done may go to 1 after identifying the sync pulse).
55	RWX	RX_PRBS_SEED_DDC: Set this bit to enable seeding of the DDC PRBS block from the data pipe output (either the data stream or the descramble PRBS block depending on the value of rx_pipe_sel).
56	RWX	RX_PRBS_SEED_DFE: Set this bit to enable seeding of the DFE PRBS block. Related to this is rx_dfe_force_load_seed, which loads from the incoming data stream when 0 or from the rx_prbs_seed_value_* when 1.
57	RWX	RX_DFE_FORCE_LOAD_SEED: Set this bit to force rx_prbs_seed_value_0_15 and rx_prbs_seed_value_16_22 to load directly into the DFE history vector in the analog front-end for this lane. **Note:** The rx_prbs_seed_value_* bits are extended by 1 bit and shifted by a fixed value to match the pipeline delays between the analog front end and the receive PRBS descrambler. To set the DFE history vector to a specific value, the user must reverse that transformation to determine the value to write to the rx_prbs_seed_value_* to get the desired result in the vector.
58	RWX	RX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
59:60	RWX	RX_IOCLK_SLIP: This field provides software control of the receive slice deserializer IOCLK slip control. Use this to slip the deserilizer by 2N beats.
61	RWX	RX_IOCLK_SLIP_STROBE: This bit provides software control to execute IOCLK slip control.
62	RWX	RX_HISTORY_PRBS_POWER_UP: This bit forces the power up of the additional analog history latches used for PRBS generation when performing H2 - 12 calibration.
63	RWX	RX_PSAVE_RESYNC_DISABLE: This bit disables the resynchronize machine for this physical lane without disabling psave mode entirely.

Register Name	**Receive Bit CNTLX1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	8002402D0601143F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49	RWX	RX_LANE_INVERT: This bit inverts the receive lane data.
50	RWX	RX_LANE_INVALID: This bit marks this receive slice as invalid and fences other operations. Use this bit, for example, to broadcast a setting to all good lanes but not bad or disabled ones.
51	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic. 0b0 = Data. 0b1 = Descrambler output.
52	RO	constant = 0b0
53	RWX	RX_PDWN_LITE: When set, this bit partially powers down unused spare lanes when not being recalibrated.
54	RWX	RX_PRBS_CHECK_SYNC: This bit enables checking for the 12/24 UI scramble synchronization pulse in the descramble PRBS block. 0b0 = Disable checking (forces prbs_sync_done to 0). 0b1 = Enable checking (prbs_sync_done may go to 1 after identifying the sync pulse).
55	RWX	RX_PRBS_SEED_DDC: Set this bit to enable seeding of the DDC PRBS block from the data pipe output (either the data stream or the descramble PRBS block depending on the value of rx_pipe_sel).

Bits	SCOM	Field Mnemonic: Description
56	RWX	RX_PRBS_SEED_DFE: Set this bit to enable seeding of the DFE PRBS block. Related to this is rx_dfe_force_load_seed, which loads from the incoming data stream when 0 or from the rx_prbs_seed_value_* when 1.
57	RWX	RX_DFE_FORCE_LOAD_SEED: Set this bit to force rx_prbs_seed_value_0_15 and rx_prbs_seed_value_16_22 to load directly into the DFE history vector in the analog front-end for this lane. **Note:** The rx_prbs_seed_value_* bits are extended by 1 bit and shifted by a fixed value to match the pipeline delays between the analog front end and the receive PRBS descrambler. To set the DFE history vector to a specific value, the user must reverse that transformation to determine the value to write to the rx_prbs_seed_value_* to get the desired result in the vector.
58	RWX	RX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
59:60	RWX	RX_IOCLK_SLIP: This field provides software control of the receive slice deserializer IOCLK slip control. Use this to slip the deserilizer by 2N beats.
61	RWX	RX_IOCLK_SLIP_STROBE: This bit provides software control to execute IOCLK slip control.
62	RWX	RX_HISTORY_PRBS_POWER_UP: This bit forces the power up of the additional analog history latches used for PRBS generation when performing H2 - 12 calibration.
63	RWX	RX_PSAVE_RESYNC_DISABLE: This bit disables the resynchronize machine for this physical lane without disabling psave mode entirely.

Register Name	Receive Bit CNTLX1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	8002402E0601143F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49	RWX	RX_LANE_INVERT: This bit inverts the receive lane data.
50	RWX	RX_LANE_INVALID: This bit marks this receive slice as invalid and fences other operations. Use this bit, for example, to broadcast a setting to all good lanes but not bad or disabled ones.
51	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic. 0b0 = Data. 0b1 = Descrambler output.
52	RO	constant = 0b0
53	RWX	RX_PDWN_LITE: When set, this bit partially powers down unused spare lanes when not being recalibrated.
54	RWX	RX_PRBS_CHECK_SYNC: This bit enables checking for the 12/24 UI scramble synchronization pulse in the descramble PRBS block. 0b0 = Disable checking (forces prbs_sync_done to 0). 0b1 = Enable checking (prbs_sync_done may go to 1 after identifying the sync pulse).
55	RWX	RX_PRBS_SEED_DDC: Set this bit to enable seeding of the DDC PRBS block from the data pipe output (either the data stream or the descramble PRBS block depending on the value of rx_pipe_sel).
56	RWX	RX_PRBS_SEED_DFE: Set this bit to enable seeding of the DFE PRBS block. Related to this is rx_dfe_force_load_seed, which loads from the incoming data stream when 0 or from the rx_prbs_seed_value_* when 1.

Bits	SCOM	Field Mnemonic: Description
57	RWX	RX_DFE_FORCE_LOAD_SEED: Set this bit to force rx_prbs_seed_value_0_15 and rx_prbs_seed_value_16_22 to load directly into the DFE history vector in the analog front-end for this lane. **Note:** The rx_prbs_seed_value_* bits are extended by 1 bit and shifted by a fixed value to match the pipeline delays between the analog front end and the receive PRBS descrambler. To set the DFE history vector to a specific value, the user must reverse that transformation to determine the value to write to the rx_prbs_seed_value_* to get the desired result in the vector.
58	RWX	RX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
59:60	RWX	RX_IOCLK_SLIP: This field provides software control of the receive slice deserializer IOCLK slip control. Use this to slip the deserilizer by 2N beats.
61	RWX	RX_IOCLK_SLIP_STROBE: This bit provides software control to execute IOCLK slip control.
62	RWX	RX_HISTORY_PRBS_POWER_UP: This bit forces the power up of the additional analog history latches used for PRBS generation when performing H2 - 12 calibration.
63	RWX	RX_PSAVE_RESYNC_DISABLE: This bit disables the resynchronize machine for this physical lane without disabling psave mode entirely.

Register Name	**Receive Bit CNTLX1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	8002402F0601143F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49	RWX	RX_LANE_INVERT: This bit inverts the receive lane data.
50	RWX	RX_LANE_INVALID: This bit marks this receive slice as invalid and fences other operations. Use this bit, for example, to broadcast a setting to all good lanes but not bad or disabled ones.
51	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic. 0b0 = Data. 0b1 = Descrambler output.
52	RO	constant = 0b0
53	RWX	RX_PDWN_LITE: When set, this bit partially powers down unused spare lanes when not being recalibrated.
54	RWX	RX_PRBS_CHECK_SYNC: This bit enables checking for the 12/24 UI scramble synchronization pulse in the descramble PRBS block. 0b0 = Disable checking (forces prbs_sync_done to 0). 0b1 = Enable checking (prbs_sync_done may go to 1 after identifying the sync pulse).
55	RWX	RX_PRBS_SEED_DDC: Set this bit to enable seeding of the DDC PRBS block from the data pipe output (either the data stream or the descramble PRBS block depending on the value of rx_pipe_sel).
56	RWX	RX_PRBS_SEED_DFE: Set this bit to enable seeding of the DFE PRBS block. Related to this is rx_dfe_force_load_seed, which loads from the incoming data stream when 0 or from the rx_prbs_seed_value_* when 1.
57	RWX	RX_DFE_FORCE_LOAD_SEED: Set this bit to force rx_prbs_seed_value_0_15 and rx_prbs_seed_value_16_22 to load directly into the DFE history vector in the analog front-end for this lane. **Note:** The rx_prbs_seed_value_* bits are extended by 1 bit and shifted by a fixed value to match the pipeline delays between the analog front end and the receive PRBS descrambler. To set the DFE history vector to a specific value, the user must reverse that transformation to determine the value to write to the rx_prbs_seed_value_* to get the desired result in the vector.
58	RWX	RX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.

Bits	SCOM	Field Mnemonic: Description
59:60	RWX	RX_IOCLK_SLIP: This field provides software control of the receive slice deserializer IOCLK slip control. Use this to slip the deserilizer by 2N beats.
61	RWX	RX_IOCLK_SLIP_STROBE: This bit provides software control to execute IOCLK slip control.
62	RWX	RX_HISTORY_PRBS_POWER_UP: This bit forces the power up of the additional analog history latches used for PRBS generation when performing H2 - 12 calibration.
63	RWX	RX_PSAVE_RESYNC_DISABLE: This bit disables the resynchronize machine for this physical lane without disabling psave mode entirely.

Register Name	Receive Bit CNTLX1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	800240300601143F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49	RWX	RX_LANE_INVERT: This bit inverts the receive lane data.
50	RWX	RX_LANE_INVALID: This bit marks this receive slice as invalid and fences other operations. Use this bit, for example, to broadcast a setting to all good lanes but not bad or disabled ones.
51	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic. 0b0 = Data. 0b1 = Descrambler output.
52	RO	constant = 0b0
53	RWX	RX_PDWN_LITE: When set, this bit partially powers down unused spare lanes when not being recalibrated.
54	RWX	RX_PRBS_CHECK_SYNC: This bit enables checking for the 12/24 UI scramble synchronization pulse in the descramble PRBS block. 0b0 = Disable checking (forces prbs_sync_done to 0). 0b1 = Enable checking (prbs_sync_done may go to 1 after identifying the sync pulse).
55	RWX	RX_PRBS_SEED_DDC: Set this bit to enable seeding of the DDC PRBS block from the data pipe output (either the data stream or the descramble PRBS block depending on the value of rx_pipe_sel).
56	RWX	RX_PRBS_SEED_DFE: Set this bit to enable seeding of the DFE PRBS block. Related to this is rx_dfe_force_load_seed, which loads from the incoming data stream when 0 or from the rx_prbs_seed_value_* when 1.
57	RWX	RX_DFE_FORCE_LOAD_SEED: Set this bit to force rx_prbs_seed_value_0_15 and rx_prbs_seed_value_16_22 to load directly into the DFE history vector in the analog front-end for this lane. **Note:** The rx_prbs_seed_value_* bits are extended by 1 bit and shifted by a fixed value to match the pipeline delays between the analog front end and the receive PRBS descrambler. To set the DFE history vector to a specific value, the user must reverse that transformation to determine the value to write to the rx_prbs_seed_value_* to get the desired result in the vector.
58	RWX	RX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
59:60	RWX	RX_IOCLK_SLIP: This field provides software control of the receive slice deserializer IOCLK slip control. Use this to slip the deserilizer by 2N beats.
61	RWX	RX_IOCLK_SLIP_STROBE: This bit provides software control to execute IOCLK slip control.
62	RWX	RX_HISTORY_PRBS_POWER_UP: This bit forces the power up of the additional analog history latches used for PRBS generation when performing H2 - 12 calibration.

Bits	SCOM	Field Mnemonic: Description
63	RWX	RX_PSAVE_RESYNC_DISABLE: This bit disables the resynchronize machine for this physical lane without disabling psave mode entirely.

Register Name	**Receive Bit CNTLX1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	800240310601143F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49	RWX	RX_LANE_INVERT: This bit inverts the receive lane data.
50	RWX	RX_LANE_INVALID: This bit marks this receive slice as invalid and fences other operations. Use this bit, for example, to broadcast a setting to all good lanes but not bad or disabled ones.
51	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic. 0b0 = Data. 0b1 = Descrambler output.
52	RO	constant = 0b0
53	RWX	RX_PDWN_LITE: When set, this bit partially powers down unused spare lanes when not being recalibrated.
54	RWX	RX_PRBS_CHECK_SYNC: This bit enables checking for the 12/24 UI scramble synchronization pulse in the descramble PRBS block. 0b0 = Disable checking (forces prbs_sync_done to 0). 0b1 = Enable checking (prbs_sync_done may go to 1 after identifying the sync pulse).
55	RWX	RX_PRBS_SEED_DDC: Set this bit to enable seeding of the DDC PRBS block from the data pipe output (either the data stream or the descramble PRBS block depending on the value of rx_pipe_sel).
56	RWX	RX_PRBS_SEED_DFE: Set this bit to enable seeding of the DFE PRBS block. Related to this is rx_dfe_force_load_seed, which loads from the incoming data stream when 0 or from the rx_prbs_seed_value_* when 1.
57	RWX	RX_DFE_FORCE_LOAD_SEED: Set this bit to force rx_prbs_seed_value_0_15 and rx_prbs_seed_value_16_22 to load directly into the DFE history vector in the analog front-end for this lane. **Note:** The rx_prbs_seed_value_* bits are extended by 1 bit and shifted by a fixed value to match the pipeline delays between the analog front end and the receive PRBS descrambler. To set the DFE history vector to a specific value, the user must reverse that transformation to determine the value to write to the rx_prbs_seed_value_* to get the desired result in the vector.
58	RWX	RX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
59:60	RWX	RX_IOCLK_SLIP: This field provides software control of the receive slice deserializer IOCLK slip control. Use this to slip the deserilizer by 2N beats.
61	RWX	RX_IOCLK_SLIP_STROBE: This bit provides software control to execute IOCLK slip control.
62	RWX	RX_HISTORY_PRBS_POWER_UP: This bit forces the power up of the additional analog history latches used for PRBS generation when performing H2 - 12 calibration.
63	RWX	RX_PSAVE_RESYNC_DISABLE: This bit disables the resynchronize machine for this physical lane without disabling psave mode entirely.

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	800248000601143F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51:52	RO	constant = 0b00
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RO	constant = 0b0
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_CENTER: This bumps PR A position to the center => -(16 - clkadj).
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported).
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported).
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	800248010601143F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51:52	RO	constant = 0b00

Bits	SCOM	Field Mnemonic: Description
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RO	constant = 0b0
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_CENTER: This bumps PR A position to the center => -(16 - clkadj).
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported).
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported).
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	800248020601143F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51:52	RO	constant = 0b00
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RO	constant = 0b0
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_CENTER: This bumps PR A position to the center => -(16 - clkadj).
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported).
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported).
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	800248030601143F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51:52	RO	constant = 0b00
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RO	constant = 0b0
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_CENTER: This bumps PR A position to the center => -(16 - clkadj).
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported).
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported).
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	800248040601143F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51:52	RO	constant = 0b00

Bits	SCOM	Field Mnemonic: Description
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RO	constant = 0b0
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_CENTER: This bumps PR A position to the center => -(16 - clkadj).
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported).
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported).
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	800248050601143F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51:52	RO	constant = 0b00
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RO	constant = 0b0
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_CENTER: This bumps PR A position to the center => -(16 - clkadj).
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported).
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported).
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	800248060601143F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51:52	RO	constant = 0b00
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RO	constant = 0b0
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_CENTER: This bumps PR A position to the center => -(16 - clkadj).
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported).
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported).
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	800248070601143F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51:52	RO	constant = 0b00

Bits	SCOM	Field Mnemonic: Description
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RO	constant = 0b0
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_CENTER: This bumps PR A position to the center => -(16 - clkadj).
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported).
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported).
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	800248080601143F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51:52	RO	constant = 0b00
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RO	constant = 0b0
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_CENTER: This bumps PR A position to the center => -(16 - clkadj).
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported).
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported).
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	800248090601143F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51:52	RO	constant = 0b00
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RO	constant = 0b0
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_CENTER: This bumps PR A position to the center => -(16 - clkadj).
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported).
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported).
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	8002480A0601143F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51:52	RO	constant = 0b00

Bits	SCOM	Field Mnemonic: Description
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RO	constant = 0b0
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_CENTER: This bumps PR A position to the center => -(16 - clkadj).
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported).
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported).
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62:63	RO	constant = 0b00

Register Name	**Receive Bit CNTL2 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	8002480B0601143F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51:52	RO	constant = 0b00
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RO	constant = 0b0
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_CENTER: This bumps PR A position to the center => -(16 - clkadj).
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported).
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported).
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	8002480C0601143F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51:52	RO	constant = 0b00
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RO	constant = 0b0
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_CENTER: This bumps PR A position to the center => -(16 - clkadj).
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported).
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported).
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	8002480D0601143F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51:52	RO	constant = 0b00

Bits	SCOM	Field Mnemonic: Description
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RO	constant = 0b0
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_CENTER: This bumps PR A position to the center => -(16 - clkadj).
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported).
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported).
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	8002480E0601143F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51:52	RO	constant = 0b00
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RO	constant = 0b0
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_CENTER: This bumps PR A position to the center => -(16 - clkadj).
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported).
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported).
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	8002480F0601143F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51:52	RO	constant = 0b00
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RO	constant = 0b0
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_CENTER: This bumps PR A position to the center => -(16 - clkadj).
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported).
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported).
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	800248100601143F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51:52	RO	constant = 0b00

Bits	SCOM	Field Mnemonic: Description
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RO	constant = 0b0
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_CENTER: This bumps PR A position to the center => -(16 - clkadj).
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported).
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported).
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	800248110601143F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51:52	RO	constant = 0b00
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RO	constant = 0b0
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_CENTER: This bumps PR A position to the center => -(16 - clkadj).
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported).
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported).
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	800248200601143F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51:52	RO	constant = 0b00
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RO	constant = 0b0
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_CENTER: This bumps PR A position to the center => -(16 - clkadj).
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported).
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported).
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	800248210601143F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51:52	RO	constant = 0b00

Bits	SCOM	Field Mnemonic: Description
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RO	constant = 0b0
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_CENTER: This bumps PR A position to the center => -(16 - clkadj).
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported).
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported).
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	800248220601143F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51:52	RO	constant = 0b00
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RO	constant = 0b0
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_CENTER: This bumps PR A position to the center => -(16 - clkadj).
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported).
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported).
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	800248230601143F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51:52	RO	constant = 0b00
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RO	constant = 0b0
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_CENTER: This bumps PR A position to the center => -(16 - clkadj).
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported).
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported).
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	800248240601143F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51:52	RO	constant = 0b00

Bits	SCOM	Field Mnemonic: Description
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RO	constant = 0b0
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_CENTER: This bumps PR A position to the center => -(16 - clkadj).
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported).
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported).
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62:63	RO	constant = 0b00

Register Name	**Receive Bit CNTL2 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	800248250601143F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51:52	RO	constant = 0b00
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RO	constant = 0b0
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_CENTER: This bumps PR A position to the center => -(16 - clkadj).
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported).
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported).
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	800248260601143F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51:52	RO	constant = 0b00
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RO	constant = 0b0
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_CENTER: This bumps PR A position to the center => -(16 - clkadj).
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported).
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported).
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	800248270601143F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51:52	RO	constant = 0b00

Bits	SCOM	Field Mnemonic: Description
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RO	constant = 0b0
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_CENTER: This bumps PR A position to the center => -(16 - clkadj).
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported).
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported).
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62:63	RO	constant = 0b00

Register Name	**Receive Bit CNTL2 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	800248280601143F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51:52	RO	constant = 0b00
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RO	constant = 0b0
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_CENTER: This bumps PR A position to the center => -(16 - clkadj).
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported).
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported).
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	800248290601143F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51:52	RO	constant = 0b00
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RO	constant = 0b0
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_CENTER: This bumps PR A position to the center => -(16 - clkadj).
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported).
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported).
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	8002482A0601143F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51:52	RO	constant = 0b00

Bits	SCOM	Field Mnemonic: Description
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RO	constant = 0b0
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_CENTER: This bumps PR A position to the center => -(16 - clkadj).
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported).
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported).
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62:63	RO	constant = 0b00

Register Name	**Receive Bit CNTL2 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	8002482B0601143F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51:52	RO	constant = 0b00
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RO	constant = 0b0
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_CENTER: This bumps PR A position to the center => -(16 - clkadj).
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported).
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported).
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	8002482C0601143F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51:52	RO	constant = 0b00
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RO	constant = 0b0
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_CENTER: This bumps PR A position to the center => -(16 - clkadj).
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported).
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported).
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	8002482D0601143F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51:52	RO	constant = 0b00

Bits	SCOM	Field Mnemonic: Description
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RO	constant = 0b0
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_CENTER: This bumps PR A position to the center => -(16 - clkadj).
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported).
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported).
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62:63	RO	constant = 0b00

Register Name	**Receive Bit CNTL2 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	8002482E0601143F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51:52	RO	constant = 0b00
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RO	constant = 0b0
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_CENTER: This bumps PR A position to the center => -(16 - clkadj).
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported).
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported).
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	8002482F0601143F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51:52	RO	constant = 0b00
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RO	constant = 0b0
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_CENTER: This bumps PR A position to the center => -(16 - clkadj).
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported).
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported).
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	800248300601143F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51:52	RO	constant = 0b00

Bits	SCOM	Field Mnemonic: Description
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RO	constant = 0b0
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_CENTER: This bumps PR A position to the center => -(16 - clkadj).
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported).
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported).
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62:63	RO	constant = 0b00

Register Name	**Receive Bit CNTL2 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	800248310601143F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51:52	RO	constant = 0b00
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RO	constant = 0b0
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_CENTER: This bumps PR A position to the center => -(16 - clkadj).
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported).
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported).
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	800250000601143F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RO	constant = 0b000000
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	800250010601143F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RO	constant = 0b000000
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	800250020601143F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RO	constant = 0b000000
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.

Bits	SCOM	Field Mnemonic: Description
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	800250030601143F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RO	constant = 0b000000
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	800250040601143F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RO	constant = 0b000000
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	800250050601143F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RO	constant = 0b000000

Bits	SCOM	Field Mnemonic: Description
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	800250060601143F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RO	constant = 0b000000
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	800250070601143F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RO	constant = 0b000000
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	800250080601143F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RO	constant = 0b000000
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	800250090601143F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RO	constant = 0b000000
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	8002500A0601143F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RO	constant = 0b000000
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	8002500B0601143F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RO	constant = 0b000000
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	8002500C0601143F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RO	constant = 0b000000
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	8002500D0601143F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RO	constant = 0b000000
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.

Bits	SCOM	Field Mnemonic: Description
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	8002500E0601143F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RO	constant = 0b000000
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	8002500F0601143F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RO	constant = 0b000000
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	800250100601143F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RO	constant = 0b000000

Bits	SCOM	Field Mnemonic: Description
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	800250110601143F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RO	constant = 0b000000
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	800250200601143F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RO	constant = 0b000000
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	800250210601143F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RO	constant = 0b000000
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	800250220601143F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RO	constant = 0b000000
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	800250230601143F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RO	constant = 0b000000
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	800250240601143F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RO	constant = 0b000000
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	800250250601143F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RO	constant = 0b000000
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	800250260601143F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RO	constant = 0b000000
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.

Bits	SCOM	Field Mnemonic: Description
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	800250270601143F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RO	constant = 0b000000
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	800250280601143F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RO	constant = 0b000000
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	800250290601143F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RO	constant = 0b000000

Bits	SCOM	Field Mnemonic: Description
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	8002502A0601143F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RO	constant = 0b000000
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	8002502B0601143F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RO	constant = 0b000000
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	8002502C0601143F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RO	constant = 0b000000
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	8002502D0601143F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RO	constant = 0b000000
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	8002502E0601143F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RO	constant = 0b000000
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	8002502F0601143F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RO	constant = 0b000000
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	800250300601143F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RO	constant = 0b000000
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	800250310601143F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RO	constant = 0b000000
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.

Bits	SCOM	Field Mnemonic: Description
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	800258000601143F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58	RWX	RX_DDC_DFE_OFFSET_SWITCH_STOP: This bit enables the trace debug DDC-DFE offset switch state to stop the state machines.
59:61	RWX	RX_DDC_DFE_OFFSET_SWITCH_SM: This field determines when to stop the state machine for trace debug.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	800258010601143F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58	RWX	RX_DDC_DFE_OFFSET_SWITCH_STOP: This bit enables the trace debug DDC-DFE offset switch state to stop the state machines.
59:61	RWX	RX_DDC_DFE_OFFSET_SWITCH_SM: This field determines when to stop the state machine for trace debug.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	800258020601143F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58	RWX	RX_DDC_DFE_OFFSET_SWITCH_STOP: This bit enables the trace debug DDC-DFE offset switch state to stop the state machines.
59:61	RWX	RX_DDC_DFE_OFFSET_SWITCH_SM: This field determines when to stop the state machine for trace debug.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	800258030601143F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58	RWX	RX_DDC_DFE_OFFSET_SWITCH_STOP: This bit enables the trace debug DDC-DFE offset switch state to stop the state machines.
59:61	RWX	RX_DDC_DFE_OFFSET_SWITCH_SM: This field determines when to stop the state machine for trace debug.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	800258040601143F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58	RWX	RX_DDC_DFE_OFFSET_SWITCH_STOP: This bit enables the trace debug DDC-DFE offset switch state to stop the state machines.
59:61	RWX	RX_DDC_DFE_OFFSET_SWITCH_SM: This field determines when to stop the state machine for trace debug.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	800258050601143F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58	RWX	RX_DDC_DFE_OFFSET_SWITCH_STOP: This bit enables the trace debug DDC-DFE offset switch state to stop the state machines.
59:61	RWX	RX_DDC_DFE_OFFSET_SWITCH_SM: This field determines when to stop the state machine for trace debug.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	800258060601143F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.

Bits	SCOM	Field Mnemonic: Description
58	RWX	RX_DDC_DFE_OFFSET_SWITCH_STOP: This bit enables the trace debug DDC-DFE offset switch state to stop the state machines.
59:61	RWX	RX_DDC_DFE_OFFSET_SWITCH_SM: This field determines when to stop the state machine for trace debug.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	800258070601143F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58	RWX	RX_DDC_DFE_OFFSET_SWITCH_STOP: This bit enables the trace debug DDC-DFE offset switch state to stop the state machines.
59:61	RWX	RX_DDC_DFE_OFFSET_SWITCH_SM: This field determines when to stop the state machine for trace debug.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	800258080601143F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58	RWX	RX_DDC_DFE_OFFSET_SWITCH_STOP: This bit enables the trace debug DDC-DFE offset switch state to stop the state machines.
59:61	RWX	RX_DDC_DFE_OFFSET_SWITCH_SM: This field determines when to stop the state machine for trace debug.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	800258090601143F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58	RWX	RX_DDC_DFE_OFFSET_SWITCH_STOP: This bit enables the trace debug DDC-DFE offset switch state to stop the state machines.
59:61	RWX	RX_DDC_DFE_OFFSET_SWITCH_SM: This field determines when to stop the state machine for trace debug.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	8002580A0601143F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58	RWX	RX_DDC_DFE_OFFSET_SWITCH_STOP: This bit enables the trace debug DDC-DFE offset switch state to stop the state machines.
59:61	RWX	RX_DDC_DFE_OFFSET_SWITCH_SM: This field determines when to stop the state machine for trace debug.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	8002580B0601143F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58	RWX	RX_DDC_DFE_OFFSET_SWITCH_STOP: This bit enables the trace debug DDC-DFE offset switch state to stop the state machines.
59:61	RWX	RX_DDC_DFE_OFFSET_SWITCH_SM: This field determines when to stop the state machine for trace debug.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	8002580C0601143F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58	RWX	RX_DDC_DFE_OFFSET_SWITCH_STOP: This bit enables the trace debug DDC-DFE offset switch state to stop the state machines.
59:61	RWX	RX_DDC_DFE_OFFSET_SWITCH_SM: This field determines when to stop the state machine for trace debug.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	8002580D0601143F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.

Bits	SCOM	Field Mnemonic: Description
58	RWX	RX_DDC_DFE_OFFSET_SWITCH_STOP: This bit enables the trace debug DDC-DFE offset switch state to stop the state machines.
59:61	RWX	RX_DDC_DFE_OFFSET_SWITCH_SM: This field determines when to stop the state machine for trace debug.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	8002580E0601143F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58	RWX	RX_DDC_DFE_OFFSET_SWITCH_STOP: This bit enables the trace debug DDC-DFE offset switch state to stop the state machines.
59:61	RWX	RX_DDC_DFE_OFFSET_SWITCH_SM: This field determines when to stop the state machine for trace debug.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	8002580F0601143F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58	RWX	RX_DDC_DFE_OFFSET_SWITCH_STOP: This bit enables the trace debug DDC-DFE offset switch state to stop the state machines.
59:61	RWX	RX_DDC_DFE_OFFSET_SWITCH_SM: This field determines when to stop the state machine for trace debug.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	800258100601143F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58	RWX	RX_DDC_DFE_OFFSET_SWITCH_STOP: This bit enables the trace debug DDC-DFE offset switch state to stop the state machines.
59:61	RWX	RX_DDC_DFE_OFFSET_SWITCH_SM: This field determines when to stop the state machine for trace debug.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	800258110601143F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58	RWX	RX_DDC_DFE_OFFSET_SWITCH_STOP: This bit enables the trace debug DDC-DFE offset switch state to stop the state machines.
59:61	RWX	RX_DDC_DFE_OFFSET_SWITCH_SM: This field determines when to stop the state machine for trace debug.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	800258200601143F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58	RWX	RX_DDC_DFE_OFFSET_SWITCH_STOP: This bit enables the trace debug DDC-DFE offset switch state to stop the state machines.
59:61	RWX	RX_DDC_DFE_OFFSET_SWITCH_SM: This field determines when to stop the state machine for trace debug.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	800258210601143F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58	RWX	RX_DDC_DFE_OFFSET_SWITCH_STOP: This bit enables the trace debug DDC-DFE offset switch state to stop the state machines.
59:61	RWX	RX_DDC_DFE_OFFSET_SWITCH_SM: This field determines when to stop the state machine for trace debug.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	800258220601143F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.

Bits	SCOM	Field Mnemonic: Description
58	RWX	RX_DDC_DFE_OFFSET_SWITCH_STOP: This bit enables the trace debug DDC-DFE offset switch state to stop the state machines.
59:61	RWX	RX_DDC_DFE_OFFSET_SWITCH_SM: This field determines when to stop the state machine for trace debug.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	800258230601143F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58	RWX	RX_DDC_DFE_OFFSET_SWITCH_STOP: This bit enables the trace debug DDC-DFE offset switch state to stop the state machines.
59:61	RWX	RX_DDC_DFE_OFFSET_SWITCH_SM: This field determines when to stop the state machine for trace debug.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	800258240601143F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58	RWX	RX_DDC_DFE_OFFSET_SWITCH_STOP: This bit enables the trace debug DDC-DFE offset switch state to stop the state machines.
59:61	RWX	RX_DDC_DFE_OFFSET_SWITCH_SM: This field determines when to stop the state machine for trace debug.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	800258250601143F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58	RWX	RX_DDC_DFE_OFFSET_SWITCH_STOP: This bit enables the trace debug DDC-DFE offset switch state to stop the state machines.
59:61	RWX	RX_DDC_DFE_OFFSET_SWITCH_SM: This field determines when to stop the state machine for trace debug.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	800258260601143F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58	RWX	RX_DDC_DFE_OFFSET_SWITCH_STOP: This bit enables the trace debug DDC-DFE offset switch state to stop the state machines.
59:61	RWX	RX_DDC_DFE_OFFSET_SWITCH_SM: This field determines when to stop the state machine for trace debug.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	800258270601143F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58	RWX	RX_DDC_DFE_OFFSET_SWITCH_STOP: This bit enables the trace debug DDC-DFE offset switch state to stop the state machines.
59:61	RWX	RX_DDC_DFE_OFFSET_SWITCH_SM: This field determines when to stop the state machine for trace debug.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	800258280601143F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58	RWX	RX_DDC_DFE_OFFSET_SWITCH_STOP: This bit enables the trace debug DDC-DFE offset switch state to stop the state machines.
59:61	RWX	RX_DDC_DFE_OFFSET_SWITCH_SM: This field determines when to stop the state machine for trace debug.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	800258290601143F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.

Bits	SCOM	Field Mnemonic: Description
58	RWX	RX_DDC_DFE_OFFSET_SWITCH_STOP: This bit enables the trace debug DDC-DFE offset switch state to stop the state machines.
59:61	RWX	RX_DDC_DFE_OFFSET_SWITCH_SM: This field determines when to stop the state machine for trace debug.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	8002582A0601143F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58	RWX	RX_DDC_DFE_OFFSET_SWITCH_STOP: This bit enables the trace debug DDC-DFE offset switch state to stop the state machines.
59:61	RWX	RX_DDC_DFE_OFFSET_SWITCH_SM: This field determines when to stop the state machine for trace debug.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	8002582B0601143F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58	RWX	RX_DDC_DFE_OFFSET_SWITCH_STOP: This bit enables the trace debug DDC-DFE offset switch state to stop the state machines.
59:61	RWX	RX_DDC_DFE_OFFSET_SWITCH_SM: This field determines when to stop the state machine for trace debug.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	8002582C0601143F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58	RWX	RX_DDC_DFE_OFFSET_SWITCH_STOP: This bit enables the trace debug DDC-DFE offset switch state to stop the state machines.
59:61	RWX	RX_DDC_DFE_OFFSET_SWITCH_SM: This field determines when to stop the state machine for trace debug.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	8002582D0601143F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58	RWX	RX_DDC_DFE_OFFSET_SWITCH_STOP: This bit enables the trace debug DDC-DFE offset switch state to stop the state machines.
59:61	RWX	RX_DDC_DFE_OFFSET_SWITCH_SM: This field determines when to stop the state machine for trace debug.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	8002582E0601143F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58	RWX	RX_DDC_DFE_OFFSET_SWITCH_STOP: This bit enables the trace debug DDC-DFE offset switch state to stop the state machines.
59:61	RWX	RX_DDC_DFE_OFFSET_SWITCH_SM: This field determines when to stop the state machine for trace debug.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	8002582F0601143F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58	RWX	RX_DDC_DFE_OFFSET_SWITCH_STOP: This bit enables the trace debug DDC-DFE offset switch state to stop the state machines.
59:61	RWX	RX_DDC_DFE_OFFSET_SWITCH_SM: This field determines when to stop the state machine for trace debug.
62:63	RO	constant = 0b00

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	800258300601143F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.

Bits	SCOM	Field Mnemonic: Description
58	RWX	RX_DDC_DFE_OFFSET_SWITCH_STOP: This bit enables the trace debug DDC-DFE offset switch state to stop the state machines.
59:61	RWX	RX_DDC_DFE_OFFSET_SWITCH_SM: This field determines when to stop the state machine for trace debug.
62:63	RO	constant = 0b00

Register Name	**Receive Bit CNTL4 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	800258310601143F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58	RWX	RX_DDC_DFE_OFFSET_SWITCH_STOP: This bit enables the trace debug DDC-DFE offset switch state to stop the state machines.
59:61	RWX	RX_DDC_DFE_OFFSET_SWITCH_SM: This field determines when to stop the state machine for trace debug.
62:63	RO	constant = 0b00

Register Name	**Receive Bit CNTL5 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	800260000601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50:63	RO	constant = 0b00000000000000

Register Name	**Receive Bit CNTL5 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	800260010601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50:63	RO	constant = 0b00000000000000

Register Name	**Receive Bit CNTL5 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	800260020601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50:63	RO	constant = 0b00000000000000

Register Name	**Receive Bit CNTL5 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	800260030601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50:63	RO	constant = 0b00000000000000

Register Name	**Receive Bit CNTL5 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	800260040601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50:63	RO	constant = 0b00000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	800260050601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50:63	RO	constant = 0b00000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	800260060601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50:63	RO	constant = 0b00000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	800260070601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50:63	RO	constant = 0b00000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	800260080601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	NCX	Reserved field.
49	NCX	Reserved field.
50:63	RO	constant = 0b00000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	800260090601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50:63	RO	constant = 0b00000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	8002600A0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50:63	RO	constant = 0b00000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	8002600B0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50:63	RO	constant = 0b00000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	8002600C0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50:63	RO	constant = 0b00000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	8002600D0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50:63	RO	constant = 0b00000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	8002600E0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50:63	RO	constant = 0b00000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	8002600F0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	NCX	Reserved field.
49	NCX	Reserved field.
50:63	RO	constant = 0b00000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	800260100601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50:63	RO	constant = 0b00000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	800260110601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50:63	RO	constant = 0b00000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	800260200601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50:63	RO	constant = 0b00000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	800260210601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50:63	RO	constant = 0b00000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	800260220601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50:63	RO	constant = 0b00000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	800260230601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50:63	RO	constant = 0b00000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	800260240601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	NCX	Reserved field.
49	NCX	Reserved field.
50:63	RO	constant = 0b00000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	800260250601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50:63	RO	constant = 0b00000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	800260260601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50:63	RO	constant = 0b00000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	800260270601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50:63	RO	constant = 0b00000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	800260280601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50:63	RO	constant = 0b00000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	800260290601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50:63	RO	constant = 0b00000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	8002602A0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50:63	RO	constant = 0b00000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	8002602B0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	NCX	Reserved field.
49	NCX	Reserved field.
50:63	RO	constant = 0b00000000000000

Register Name	**Receive Bit CNTL5 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	8002602C0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50:63	RO	constant = 0b00000000000000

Register Name	**Receive Bit CNTL5 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	8002602D0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50:63	RO	constant = 0b00000000000000

Register Name	**Receive Bit CNTL5 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	8002602E0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50:63	RO	constant = 0b00000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	8002602F0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50:63	RO	constant = 0b00000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	800260300601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50:63	RO	constant = 0b00000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	800260310601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50:63	RO	constant = 0b00000000000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	800268000601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	RO	constant = 0b0
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	**Receive Bit STAT1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	800268010601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	RO	constant = 0b0
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	**Receive Bit STAT1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	800268020601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	RO	constant = 0b0
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	**Receive Bit STAT1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	800268030601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	RO	constant = 0b0
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	**Receive Bit STAT1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	800268040601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	RO	constant = 0b0
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	800268050601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	RO	constant = 0b0
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	800268060601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
51	ROX	Reserved field.
52	ROX	Reserved field.
53	RO	constant = 0b0
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	**Receive Bit STAT1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	800268070601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	RO	constant = 0b0
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	**Receive Bit STAT1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	800268080601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
52	ROX	Reserved field.
53	RO	constant = 0b0
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	800268090601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	RO	constant = 0b0
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	8002680A0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
53	RO	constant = 0b0
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	8002680B0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	RO	constant = 0b0
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	8002680C0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	8002680D0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	RO	constant = 0b0
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	8002680E0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	RO	constant = 0b0
54	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	8002680F0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	RO	constant = 0b0
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	800268100601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	RO	constant = 0b0
54	ROX	Reserved field.
55	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
56	ROX	Reserved field.
57	ROX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	800268110601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	RO	constant = 0b0
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	800268200601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	RO	constant = 0b0
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
57	ROX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	800268210601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	RO	constant = 0b0
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	800268220601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	RO	constant = 0b0
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant = 0b000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	800268230601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	RO	constant = 0b0
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	800268240601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	RO	constant = 0b0
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	800268250601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	RO	constant = 0b0
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	800268260601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	RO	constant = 0b0
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	800268270601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	RO	constant = 0b0
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	800268280601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	RO	constant = 0b0
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	800268290601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	RO	constant = 0b0
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	8002682A0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	RO	constant = 0b0
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	8002682B0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	RO	constant = 0b0
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	8002682C0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	RO	constant = 0b0
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	8002682D0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	RO	constant = 0b0
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	8002682E0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	RO	constant = 0b0
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	8002682F0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	RO	constant = 0b0
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	800268300601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	RO	constant = 0b0
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	800268310601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	RO	constant = 0b0
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	800270000601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51:52	RO	constant = 0b00
53	ROX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	800270010601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51:52	RO	constant = 0b00
53	ROX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	800270020601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51:52	RO	constant = 0b00
53	ROX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	800270030601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51:52	RO	constant = 0b00
53	ROX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	800270040601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51:52	RO	constant = 0b00
53	ROX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	800270050601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51:52	RO	constant = 0b00

Bits	SCOM	Field Mnemonic: Description
53	ROX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	800270060601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51:52	RO	constant = 0b00
53	ROX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	800270070601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51:52	RO	constant = 0b00
53	ROX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	800270080601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51:52	RO	constant = 0b00
53	ROX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	800270090601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51:52	RO	constant = 0b00
53	ROX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	8002700A0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51:52	RO	constant = 0b00
53	ROX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	8002700B0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51:52	RO	constant = 0b00
53	ROX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	8002700C0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51:52	RO	constant = 0b00
53	ROX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	8002700D0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51:52	RO	constant = 0b00
53	ROX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	8002700E0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51:52	RO	constant = 0b00
53	ROX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	8002700F0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51:52	RO	constant = 0b00
53	ROX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	800270100601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51:52	RO	constant = 0b00

Bits	SCOM	Field Mnemonic: Description
53	ROX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	**Receive Bit STAT2 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	800270110601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51:52	RO	constant = 0b00
53	ROX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	**Receive Bit STAT2 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	800270200601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51:52	RO	constant = 0b00
53	ROX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	800270210601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51:52	RO	constant = 0b00
53	ROX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	800270220601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51:52	RO	constant = 0b00
53	ROX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	800270230601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51:52	RO	constant = 0b00
53	ROX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	800270240601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51:52	RO	constant = 0b00
53	ROX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	**Receive Bit STAT2 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	800270250601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51:52	RO	constant = 0b00
53	ROX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	**Receive Bit STAT2 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	800270260601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51:52	RO	constant = 0b00
53	ROX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	**Receive Bit STAT2 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	800270270601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51:52	RO	constant = 0b00
53	ROX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	800270280601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51:52	RO	constant = 0b00
53	ROX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	800270290601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51:52	RO	constant = 0b00

Bits	SCOM	Field Mnemonic: Description
53	ROX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	8002702A0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51:52	RO	constant = 0b00
53	ROX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	8002702B0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51:52	RO	constant = 0b00
53	ROX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	8002702C0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51:52	RO	constant = 0b00
53	ROX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	8002702D0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51:52	RO	constant = 0b00
53	ROX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	8002702E0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51:52	RO	constant = 0b00
53	ROX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	8002702F0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51:52	RO	constant = 0b00
53	ROX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	**Receive Bit STAT2 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	800270300601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51:52	RO	constant = 0b00
53	ROX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	**Receive Bit STAT2 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	800270310601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51:52	RO	constant = 0b00
53	ROX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	**Receive Bit STAT3 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	800278000601143F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	800278010601143F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	800278020601143F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	800278030601143F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	800278040601143F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	800278050601143F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	800278060601143F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	800278070601143F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	800278080601143F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	800278090601143F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	8002780A0601143F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	8002780B0601143F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	8002780C0601143F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	8002780D0601143F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	8002780E0601143F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	8002780F0601143F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	800278100601143F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	800278110601143F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	800278200601143F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	800278210601143F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	800278220601143F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	800278230601143F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	800278240601143F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	800278250601143F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	800278260601143F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	800278270601143F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	800278280601143F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	800278290601143F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	8002782A0601143F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	8002782B0601143F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	8002782C0601143F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	8002782D0601143F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	8002782E0601143F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	8002782F0601143F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	800278300601143F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	800278310601143F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL
Address	8002C0000601143F (SCOM)
Description	This register contains the first set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	RX_PRBS_SEED_VALUE_0_15: Receive per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This setting must be set consistent with tx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in 12-bit or 24-bit synchronous mode. 0b0001000000000000 = 24-bit PRBS tap point A. 0b1111000000111110 = 24-bit PRBS tap point B. 0b0000011110111100 = 24-bit PRBS tap point C. 0b0000011111000111 = 24-bit PRBS tap point D. 0b0000001111101111 = 24-bit PRBS tap point E. 0b0001111100001111 = 24-bit PRBS tap point F. 0b0001100000000000 = 24-bit PRBS tap point G. 0b1001110000000000 = 24-bit PRBS tap point H. 0b1000010000000000 = 12-bit PRBS tap point A. 0b0111110000000000 = 12-bit PRBS tap point B. 0b0000000000001111 = 12-bit PRBS tap point C. 0b1100000000001111 = 12-bit PRBS tap point D. 0b1000000000000111 = 12-bit PRBS tap point E. 0b1000000000111111 = 12-bit PRBS tap point F. 0b0000011000000000 = 12-bit PRBS tap point G. 0b0000011100000000 = 12-bit PRBS tap point H.

Register Name	Receive Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL
Address	8002C0010601143F (SCOM)
Description	This register contains the first set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	RX_PRBS_SEED_VALUE_0_15: Receive per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This setting must be set consistent with tx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in 12-bit or 24-bit synchronous mode. 0b0001000000000000 = 24-bit PRBS tap point A. 0b1111000000111110 = 24-bit PRBS tap point B. 0b0000011110111100 = 24-bit PRBS tap point C. 0b0000011111000111 = 24-bit PRBS tap point D. 0b0000001111101111 = 24-bit PRBS tap point E. 0b0001111100001111 = 24-bit PRBS tap point F. 0b0001100000000000 = 24-bit PRBS tap point G. 0b1001110000000000 = 24-bit PRBS tap point H. 0b1000010000000000 = 12-bit PRBS tap point A. 0b0111110000000000 = 12-bit PRBS tap point B. 0b0000000000001111 = 12-bit PRBS tap point C. 0b1100000000001111 = 12-bit PRBS tap point D. 0b1000000000000111 = 12-bit PRBS tap point E. 0b1000000000111111 = 12-bit PRBS tap point F. 0b0000011000000000 = 12-bit PRBS tap point G. 0b0000011100000000 = 12-bit PRBS tap point H.

Register Name	Receive Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL
Address	8002C0020601143F (SCOM)
Description	This register contains the first set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	RX_PRBS_SEED_VALUE_0_15: Receive per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This setting must be set consistent with tx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in 12-bit or 24-bit synchronous mode. 0b0001000000000000 = 24-bit PRBS tap point A. 0b1111000000111110 = 24-bit PRBS tap point B. 0b0000011110111100 = 24-bit PRBS tap point C. 0b0000011111000111 = 24-bit PRBS tap point D. 0b0000001111101111 = 24-bit PRBS tap point E. 0b0001111100001111 = 24-bit PRBS tap point F. 0b0001100000000000 = 24-bit PRBS tap point G. 0b1001110000000000 = 24-bit PRBS tap point H. 0b1000010000000000 = 12-bit PRBS tap point A. 0b0111110000000000 = 12-bit PRBS tap point B. 0b0000000000001111 = 12-bit PRBS tap point C. 0b1100000000001111 = 12-bit PRBS tap point D. 0b1000000000000111 = 12-bit PRBS tap point E. 0b1000000000111111 = 12-bit PRBS tap point F. 0b0000011000000000 = 12-bit PRBS tap point G. 0b0000011100000000 = 12-bit PRBS tap point H.

Register Name	Receive Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL
Address	8002C0030601143F (SCOM)
Description	This register contains the first set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	RX_PRBS_SEED_VALUE_0_15: Receive per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This setting must be set consistent with tx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in 12-bit or 24-bit synchronous mode. 0b0001000000000000 = 24-bit PRBS tap point A. 0b1111000000111110 = 24-bit PRBS tap point B. 0b0000011110111100 = 24-bit PRBS tap point C. 0b0000011111000111 = 24-bit PRBS tap point D. 0b0000001111101111 = 24-bit PRBS tap point E. 0b0001111100001111 = 24-bit PRBS tap point F. 0b0001100000000000 = 24-bit PRBS tap point G. 0b1001110000000000 = 24-bit PRBS tap point H. 0b1000010000000000 = 12-bit PRBS tap point A. 0b0111110000000000 = 12-bit PRBS tap point B. 0b0000000000001111 = 12-bit PRBS tap point C. 0b1100000000001111 = 12-bit PRBS tap point D. 0b1000000000000111 = 12-bit PRBS tap point E. 0b1000000000111111 = 12-bit PRBS tap point F. 0b0000011000000000 = 12-bit PRBS tap point G. 0b0000011100000000 = 12-bit PRBS tap point H.

Register Name	Receive Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL
Address	8002C0040601143F (SCOM)
Description	This register contains the first set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	RX_PRBS_SEED_VALUE_0_15: Receive per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This setting must be set consistent with tx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in 12-bit or 24-bit synchronous mode. 0b0001000000000000 = 24-bit PRBS tap point A. 0b1111000000111110 = 24-bit PRBS tap point B. 0b0000011110111100 = 24-bit PRBS tap point C. 0b0000011111000111 = 24-bit PRBS tap point D. 0b0000001111101111 = 24-bit PRBS tap point E. 0b0001111100001111 = 24-bit PRBS tap point F. 0b0001100000000000 = 24-bit PRBS tap point G. 0b1001110000000000 = 24-bit PRBS tap point H. 0b1000010000000000 = 12-bit PRBS tap point A. 0b0111110000000000 = 12-bit PRBS tap point B. 0b0000000000001111 = 12-bit PRBS tap point C. 0b1100000000001111 = 12-bit PRBS tap point D. 0b1000000000000111 = 12-bit PRBS tap point E. 0b1000000000111111 = 12-bit PRBS tap point F. 0b0000011000000000 = 12-bit PRBS tap point G. 0b0000011100000000 = 12-bit PRBS tap point H.

Register Name	Receive Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL
Address	8002C0050601143F (SCOM)
Description	This register contains the first set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	RX_PRBS_SEED_VALUE_0_15: Receive per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This setting must be set consistent with tx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in 12-bit or 24-bit synchronous mode. 0b0001000000000000 = 24-bit PRBS tap point A. 0b1111000000111110 = 24-bit PRBS tap point B. 0b0000011110111100 = 24-bit PRBS tap point C. 0b0000011111000111 = 24-bit PRBS tap point D. 0b0000001111101111 = 24-bit PRBS tap point E. 0b0001111100001111 = 24-bit PRBS tap point F. 0b0001100000000000 = 24-bit PRBS tap point G. 0b1001110000000000 = 24-bit PRBS tap point H. 0b1000010000000000 = 12-bit PRBS tap point A. 0b0111110000000000 = 12-bit PRBS tap point B. 0b0000000000001111 = 12-bit PRBS tap point C. 0b1100000000001111 = 12-bit PRBS tap point D. 0b1000000000000111 = 12-bit PRBS tap point E. 0b1000000000111111 = 12-bit PRBS tap point F. 0b0000011000000000 = 12-bit PRBS tap point G. 0b0000011100000000 = 12-bit PRBS tap point H.

Register Name	Receive Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL
Address	8002C0060601143F (SCOM)
Description	This register contains the first set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	RX_PRBS_SEED_VALUE_0_15: Receive per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This setting must be set consistent with tx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in 12-bit or 24-bit synchronous mode. 0b0001000000000000 = 24-bit PRBS tap point A. 0b1111000000111110 = 24-bit PRBS tap point B. 0b0000011110111100 = 24-bit PRBS tap point C. 0b0000011111000111 = 24-bit PRBS tap point D. 0b0000001111101111 = 24-bit PRBS tap point E. 0b0001111100001111 = 24-bit PRBS tap point F. 0b0001100000000000 = 24-bit PRBS tap point G. 0b1001110000000000 = 24-bit PRBS tap point H. 0b1000010000000000 = 12-bit PRBS tap point A. 0b0111110000000000 = 12-bit PRBS tap point B. 0b0000000000001111 = 12-bit PRBS tap point C. 0b1100000000001111 = 12-bit PRBS tap point D. 0b1000000000000111 = 12-bit PRBS tap point E. 0b1000000000111111 = 12-bit PRBS tap point F. 0b0000011000000000 = 12-bit PRBS tap point G. 0b0000011100000000 = 12-bit PRBS tap point H.

Register Name	Receive Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL
Address	8002C0070601143F (SCOM)
Description	This register contains the first set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	RX_PRBS_SEED_VALUE_0_15: Receive per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This setting must be set consistent with tx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in 12-bit or 24-bit synchronous mode. 0b0001000000000000 = 24-bit PRBS tap point A. 0b1111000000111110 = 24-bit PRBS tap point B. 0b0000011110111100 = 24-bit PRBS tap point C. 0b0000011111000111 = 24-bit PRBS tap point D. 0b0000001111101111 = 24-bit PRBS tap point E. 0b0001111100001111 = 24-bit PRBS tap point F. 0b0001100000000000 = 24-bit PRBS tap point G. 0b1001110000000000 = 24-bit PRBS tap point H. 0b1000010000000000 = 12-bit PRBS tap point A. 0b0111110000000000 = 12-bit PRBS tap point B. 0b0000000000001111 = 12-bit PRBS tap point C. 0b1100000000001111 = 12-bit PRBS tap point D. 0b1000000000000111 = 12-bit PRBS tap point E. 0b1000000000111111 = 12-bit PRBS tap point F. 0b0000011000000000 = 12-bit PRBS tap point G. 0b0000011100000000 = 12-bit PRBS tap point H.

Register Name	Receive Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL
Address	8002C0080601143F (SCOM)
Description	This register contains the first set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	RX_PRBS_SEED_VALUE_0_15: Receive per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This setting must be set consistent with tx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in 12-bit or 24-bit synchronous mode. 0b0001000000000000 = 24-bit PRBS tap point A. 0b1111000000111110 = 24-bit PRBS tap point B. 0b0000011110111100 = 24-bit PRBS tap point C. 0b0000011111000111 = 24-bit PRBS tap point D. 0b0000001111101111 = 24-bit PRBS tap point E. 0b0001111100001111 = 24-bit PRBS tap point F. 0b0001100000000000 = 24-bit PRBS tap point G. 0b1001110000000000 = 24-bit PRBS tap point H. 0b1000010000000000 = 12-bit PRBS tap point A. 0b0111110000000000 = 12-bit PRBS tap point B. 0b0000000000001111 = 12-bit PRBS tap point C. 0b1100000000001111 = 12-bit PRBS tap point D. 0b1000000000000111 = 12-bit PRBS tap point E. 0b1000000000111111 = 12-bit PRBS tap point F. 0b0000011000000000 = 12-bit PRBS tap point G. 0b0000011100000000 = 12-bit PRBS tap point H.

Register Name	Receive Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL
Address	8002C0090601143F (SCOM)
Description	This register contains the first set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	RX_PRBS_SEED_VALUE_0_15: Receive per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This setting must be set consistent with tx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in 12-bit or 24-bit synchronous mode. 0b0001000000000000 = 24-bit PRBS tap point A. 0b1111000000111110 = 24-bit PRBS tap point B. 0b0000011110111100 = 24-bit PRBS tap point C. 0b0000011111000111 = 24-bit PRBS tap point D. 0b0000001111101111 = 24-bit PRBS tap point E. 0b0001111100001111 = 24-bit PRBS tap point F. 0b0001100000000000 = 24-bit PRBS tap point G. 0b1001110000000000 = 24-bit PRBS tap point H. 0b1000010000000000 = 12-bit PRBS tap point A. 0b0111110000000000 = 12-bit PRBS tap point B. 0b0000000000001111 = 12-bit PRBS tap point C. 0b1100000000001111 = 12-bit PRBS tap point D. 0b1000000000000111 = 12-bit PRBS tap point E. 0b1000000000111111 = 12-bit PRBS tap point F. 0b0000011000000000 = 12-bit PRBS tap point G. 0b0000011100000000 = 12-bit PRBS tap point H.

Register Name	Receive Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL
Address	8002C00A0601143F (SCOM)
Description	This register contains the first set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	RX_PRBS_SEED_VALUE_0_15: Receive per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This setting must be set consistent with tx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in 12-bit or 24-bit synchronous mode. 0b0001000000000000 = 24-bit PRBS tap point A. 0b1111000000111110 = 24-bit PRBS tap point B. 0b0000011110111100 = 24-bit PRBS tap point C. 0b0000011111000111 = 24-bit PRBS tap point D. 0b0000001111101111 = 24-bit PRBS tap point E. 0b0001111100001111 = 24-bit PRBS tap point F. 0b0001100000000000 = 24-bit PRBS tap point G. 0b1001110000000000 = 24-bit PRBS tap point H. 0b1000010000000000 = 12-bit PRBS tap point A. 0b0111110000000000 = 12-bit PRBS tap point B. 0b0000000000001111 = 12-bit PRBS tap point C. 0b1100000000001111 = 12-bit PRBS tap point D. 0b1000000000000111 = 12-bit PRBS tap point E. 0b1000000000111111 = 12-bit PRBS tap point F. 0b0000011000000000 = 12-bit PRBS tap point G. 0b0000011100000000 = 12-bit PRBS tap point H.

Register Name	Receive Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL
Address	8002C00B0601143F (SCOM)
Description	This register contains the first set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	RX_PRBS_SEED_VALUE_0_15: Receive per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This setting must be set consistent with tx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in 12-bit or 24-bit synchronous mode. 0b0001000000000000 = 24-bit PRBS tap point A. 0b1111000000111110 = 24-bit PRBS tap point B. 0b0000011110111100 = 24-bit PRBS tap point C. 0b0000011111000111 = 24-bit PRBS tap point D. 0b0000001111101111 = 24-bit PRBS tap point E. 0b0001111100001111 = 24-bit PRBS tap point F. 0b0001100000000000 = 24-bit PRBS tap point G. 0b1001110000000000 = 24-bit PRBS tap point H. 0b1000010000000000 = 12-bit PRBS tap point A. 0b0111110000000000 = 12-bit PRBS tap point B. 0b0000000000001111 = 12-bit PRBS tap point C. 0b1100000000001111 = 12-bit PRBS tap point D. 0b1000000000000111 = 12-bit PRBS tap point E. 0b1000000000111111 = 12-bit PRBS tap point F. 0b0000011000000000 = 12-bit PRBS tap point G. 0b0000011100000000 = 12-bit PRBS tap point H.

Register Name	Receive Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL
Address	8002C00C0601143F (SCOM)
Description	This register contains the first set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	RX_PRBS_SEED_VALUE_0_15: Receive per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This setting must be set consistent with tx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in 12-bit or 24-bit synchronous mode. 0b0001000000000000 = 24-bit PRBS tap point A. 0b1111000000111110 = 24-bit PRBS tap point B. 0b0000011110111100 = 24-bit PRBS tap point C. 0b0000011111000111 = 24-bit PRBS tap point D. 0b0000001111101111 = 24-bit PRBS tap point E. 0b0001111100001111 = 24-bit PRBS tap point F. 0b0001100000000000 = 24-bit PRBS tap point G. 0b1001110000000000 = 24-bit PRBS tap point H. 0b1000010000000000 = 12-bit PRBS tap point A. 0b0111110000000000 = 12-bit PRBS tap point B. 0b0000000000001111 = 12-bit PRBS tap point C. 0b1100000000001111 = 12-bit PRBS tap point D. 0b1000000000000111 = 12-bit PRBS tap point E. 0b1000000000111111 = 12-bit PRBS tap point F. 0b0000011000000000 = 12-bit PRBS tap point G. 0b0000011100000000 = 12-bit PRBS tap point H.

Register Name	Receive Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL
Address	8002C00D0601143F (SCOM)
Description	This register contains the first set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	RX_PRBS_SEED_VALUE_0_15: Receive per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This setting must be set consistent with tx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in 12-bit or 24-bit synchronous mode. 0b0001000000000000 = 24-bit PRBS tap point A. 0b1111000000111110 = 24-bit PRBS tap point B. 0b0000011110111100 = 24-bit PRBS tap point C. 0b0000011111000111 = 24-bit PRBS tap point D. 0b0000001111101111 = 24-bit PRBS tap point E. 0b0001111100001111 = 24-bit PRBS tap point F. 0b0001100000000000 = 24-bit PRBS tap point G. 0b1001110000000000 = 24-bit PRBS tap point H. 0b1000010000000000 = 12-bit PRBS tap point A. 0b0111110000000000 = 12-bit PRBS tap point B. 0b0000000000001111 = 12-bit PRBS tap point C. 0b1100000000001111 = 12-bit PRBS tap point D. 0b1000000000000111 = 12-bit PRBS tap point E. 0b1000000000111111 = 12-bit PRBS tap point F. 0b0000011000000000 = 12-bit PRBS tap point G. 0b0000011100000000 = 12-bit PRBS tap point H.

Register Name	Receive Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL
Address	8002C00E0601143F (SCOM)
Description	This register contains the first set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	RX_PRBS_SEED_VALUE_0_15: Receive per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This setting must be set consistent with tx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in 12-bit or 24-bit synchronous mode. 0b0001000000000000 = 24-bit PRBS tap point A. 0b1111000000111110 = 24-bit PRBS tap point B. 0b0000011110111100 = 24-bit PRBS tap point C. 0b0000011111000111 = 24-bit PRBS tap point D. 0b0000001111101111 = 24-bit PRBS tap point E. 0b0001111100001111 = 24-bit PRBS tap point F. 0b0001100000000000 = 24-bit PRBS tap point G. 0b1001110000000000 = 24-bit PRBS tap point H. 0b1000010000000000 = 12-bit PRBS tap point A. 0b0111110000000000 = 12-bit PRBS tap point B. 0b0000000000001111 = 12-bit PRBS tap point C. 0b1100000000001111 = 12-bit PRBS tap point D. 0b1000000000000111 = 12-bit PRBS tap point E. 0b1000000000111111 = 12-bit PRBS tap point F. 0b0000011000000000 = 12-bit PRBS tap point G. 0b0000011100000000 = 12-bit PRBS tap point H.

Register Name	Receive Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL
Address	8002C00F0601143F (SCOM)
Description	This register contains the first set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	RX_PRBS_SEED_VALUE_0_15: Receive per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This setting must be set consistent with tx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in 12-bit or 24-bit synchronous mode. 0b0001000000000000 = 24-bit PRBS tap point A. 0b1111000000111110 = 24-bit PRBS tap point B. 0b0000011110111100 = 24-bit PRBS tap point C. 0b0000011111000111 = 24-bit PRBS tap point D. 0b0000001111101111 = 24-bit PRBS tap point E. 0b0001111100001111 = 24-bit PRBS tap point F. 0b0001100000000000 = 24-bit PRBS tap point G. 0b1001110000000000 = 24-bit PRBS tap point H. 0b1000010000000000 = 12-bit PRBS tap point A. 0b0111110000000000 = 12-bit PRBS tap point B. 0b0000000000001111 = 12-bit PRBS tap point C. 0b1100000000001111 = 12-bit PRBS tap point D. 0b1000000000000111 = 12-bit PRBS tap point E. 0b1000000000111111 = 12-bit PRBS tap point F. 0b0000011000000000 = 12-bit PRBS tap point G. 0b0000011100000000 = 12-bit PRBS tap point H.

Register Name	Receive Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL
Address	8002C0100601143F (SCOM)
Description	This register contains the first set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	RX_PRBS_SEED_VALUE_0_15: Receive per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This setting must be set consistent with tx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in 12-bit or 24-bit synchronous mode. 0b0001000000000000 = 24-bit PRBS tap point A. 0b1111000000111110 = 24-bit PRBS tap point B. 0b0000011110111100 = 24-bit PRBS tap point C. 0b0000011111000111 = 24-bit PRBS tap point D. 0b0000001111101111 = 24-bit PRBS tap point E. 0b0001111100001111 = 24-bit PRBS tap point F. 0b0001100000000000 = 24-bit PRBS tap point G. 0b1001110000000000 = 24-bit PRBS tap point H. 0b1000010000000000 = 12-bit PRBS tap point A. 0b0111110000000000 = 12-bit PRBS tap point B. 0b0000000000001111 = 12-bit PRBS tap point C. 0b1100000000001111 = 12-bit PRBS tap point D. 0b1000000000000111 = 12-bit PRBS tap point E. 0b1000000000111111 = 12-bit PRBS tap point F. 0b0000011000000000 = 12-bit PRBS tap point G. 0b0000011100000000 = 12-bit PRBS tap point H.

Register Name	Receive Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL
Address	8002C0110601143F (SCOM)
Description	This register contains the first set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	RX_PRBS_SEED_VALUE_0_15: Receive per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This setting must be set consistent with tx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in 12-bit or 24-bit synchronous mode. 0b0001000000000000 = 24-bit PRBS tap point A. 0b1111000000111110 = 24-bit PRBS tap point B. 0b0000011110111100 = 24-bit PRBS tap point C. 0b0000011111000111 = 24-bit PRBS tap point D. 0b0000001111101111 = 24-bit PRBS tap point E. 0b0001111100001111 = 24-bit PRBS tap point F. 0b0001100000000000 = 24-bit PRBS tap point G. 0b1001110000000000 = 24-bit PRBS tap point H. 0b1000010000000000 = 12-bit PRBS tap point A. 0b0111110000000000 = 12-bit PRBS tap point B. 0b0000000000001111 = 12-bit PRBS tap point C. 0b1100000000001111 = 12-bit PRBS tap point D. 0b1000000000000111 = 12-bit PRBS tap point E. 0b1000000000111111 = 12-bit PRBS tap point F. 0b0000011000000000 = 12-bit PRBS tap point G. 0b0000011100000000 = 12-bit PRBS tap point H.

Register Name	Receive Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL
Address	8002C0200601143F (SCOM)
Description	This register contains the first set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	RX_PRBS_SEED_VALUE_0_15: Receive per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This setting must be set consistent with tx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in 12-bit or 24-bit synchronous mode. 0b0001000000000000 = 24-bit PRBS tap point A. 0b1111000000111110 = 24-bit PRBS tap point B. 0b0000011110111100 = 24-bit PRBS tap point C. 0b0000011111000111 = 24-bit PRBS tap point D. 0b0000001111101111 = 24-bit PRBS tap point E. 0b0001111100001111 = 24-bit PRBS tap point F. 0b0001100000000000 = 24-bit PRBS tap point G. 0b1001110000000000 = 24-bit PRBS tap point H. 0b1000010000000000 = 12-bit PRBS tap point A. 0b0111110000000000 = 12-bit PRBS tap point B. 0b0000000000001111 = 12-bit PRBS tap point C. 0b1100000000001111 = 12-bit PRBS tap point D. 0b1000000000000111 = 12-bit PRBS tap point E. 0b1000000000111111 = 12-bit PRBS tap point F. 0b0000011000000000 = 12-bit PRBS tap point G. 0b0000011100000000 = 12-bit PRBS tap point H.

Register Name	Receive Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL
Address	8002C0210601143F (SCOM)
Description	This register contains the first set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	RX_PRBS_SEED_VALUE_0_15: Receive per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This setting must be set consistent with tx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in 12-bit or 24-bit synchronous mode. 0b0001000000000000 = 24-bit PRBS tap point A. 0b1111000000111110 = 24-bit PRBS tap point B. 0b0000011110111100 = 24-bit PRBS tap point C. 0b0000011111000111 = 24-bit PRBS tap point D. 0b0000001111101111 = 24-bit PRBS tap point E. 0b0001111100001111 = 24-bit PRBS tap point F. 0b0001100000000000 = 24-bit PRBS tap point G. 0b1001110000000000 = 24-bit PRBS tap point H. 0b1000010000000000 = 12-bit PRBS tap point A. 0b0111110000000000 = 12-bit PRBS tap point B. 0b0000000000001111 = 12-bit PRBS tap point C. 0b1100000000001111 = 12-bit PRBS tap point D. 0b1000000000000111 = 12-bit PRBS tap point E. 0b1000000000111111 = 12-bit PRBS tap point F. 0b0000011000000000 = 12-bit PRBS tap point G. 0b0000011100000000 = 12-bit PRBS tap point H.

Register Name	Receive Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL
Address	8002C0220601143F (SCOM)
Description	This register contains the first set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	RX_PRBS_SEED_VALUE_0_15: Receive per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This setting must be set consistent with tx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in 12-bit or 24-bit synchronous mode. 0b0001000000000000 = 24-bit PRBS tap point A. 0b1111000000111110 = 24-bit PRBS tap point B. 0b0000011110111100 = 24-bit PRBS tap point C. 0b0000011111000111 = 24-bit PRBS tap point D. 0b0000001111101111 = 24-bit PRBS tap point E. 0b0001111100001111 = 24-bit PRBS tap point F. 0b0001100000000000 = 24-bit PRBS tap point G. 0b1001110000000000 = 24-bit PRBS tap point H. 0b1000010000000000 = 12-bit PRBS tap point A. 0b0111110000000000 = 12-bit PRBS tap point B. 0b0000000000001111 = 12-bit PRBS tap point C. 0b1100000000001111 = 12-bit PRBS tap point D. 0b1000000000000111 = 12-bit PRBS tap point E. 0b1000000000111111 = 12-bit PRBS tap point F. 0b0000011000000000 = 12-bit PRBS tap point G. 0b0000011100000000 = 12-bit PRBS tap point H.

Register Name	Receive Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL
Address	8002C0230601143F (SCOM)
Description	This register contains the first set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	RX_PRBS_SEED_VALUE_0_15: Receive per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This setting must be set consistent with tx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in 12-bit or 24-bit synchronous mode. 0b0001000000000000 = 24-bit PRBS tap point A. 0b1111000000111110 = 24-bit PRBS tap point B. 0b0000011110111100 = 24-bit PRBS tap point C. 0b0000011111000111 = 24-bit PRBS tap point D. 0b0000001111101111 = 24-bit PRBS tap point E. 0b0001111100001111 = 24-bit PRBS tap point F. 0b0001100000000000 = 24-bit PRBS tap point G. 0b1001110000000000 = 24-bit PRBS tap point H. 0b1000010000000000 = 12-bit PRBS tap point A. 0b0111110000000000 = 12-bit PRBS tap point B. 0b0000000000001111 = 12-bit PRBS tap point C. 0b1100000000001111 = 12-bit PRBS tap point D. 0b1000000000000111 = 12-bit PRBS tap point E. 0b1000000000111111 = 12-bit PRBS tap point F. 0b0000011000000000 = 12-bit PRBS tap point G. 0b0000011100000000 = 12-bit PRBS tap point H.

Register Name	Receive Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL
Address	8002C0240601143F (SCOM)
Description	This register contains the first set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	RX_PRBS_SEED_VALUE_0_15: Receive per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This setting must be set consistent with tx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in 12-bit or 24-bit synchronous mode. 0b0001000000000000 = 24-bit PRBS tap point A. 0b1111000000111110 = 24-bit PRBS tap point B. 0b0000011110111100 = 24-bit PRBS tap point C. 0b0000011111000111 = 24-bit PRBS tap point D. 0b0000001111101111 = 24-bit PRBS tap point E. 0b0001111100001111 = 24-bit PRBS tap point F. 0b0001100000000000 = 24-bit PRBS tap point G. 0b1001110000000000 = 24-bit PRBS tap point H. 0b1000010000000000 = 12-bit PRBS tap point A. 0b0111110000000000 = 12-bit PRBS tap point B. 0b0000000000001111 = 12-bit PRBS tap point C. 0b1100000000001111 = 12-bit PRBS tap point D. 0b1000000000000111 = 12-bit PRBS tap point E. 0b1000000000111111 = 12-bit PRBS tap point F. 0b0000011000000000 = 12-bit PRBS tap point G. 0b0000011100000000 = 12-bit PRBS tap point H.

Register Name	Receive Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL
Address	8002C0250601143F (SCOM)
Description	This register contains the first set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	RX_PRBS_SEED_VALUE_0_15: Receive per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This setting must be set consistent with tx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in 12-bit or 24-bit synchronous mode. 0b0001000000000000 = 24-bit PRBS tap point A. 0b1111000000111110 = 24-bit PRBS tap point B. 0b0000011110111100 = 24-bit PRBS tap point C. 0b0000011111000111 = 24-bit PRBS tap point D. 0b0000001111101111 = 24-bit PRBS tap point E. 0b0001111100001111 = 24-bit PRBS tap point F. 0b0001100000000000 = 24-bit PRBS tap point G. 0b1001110000000000 = 24-bit PRBS tap point H. 0b1000010000000000 = 12-bit PRBS tap point A. 0b0111110000000000 = 12-bit PRBS tap point B. 0b0000000000001111 = 12-bit PRBS tap point C. 0b1100000000001111 = 12-bit PRBS tap point D. 0b1000000000000111 = 12-bit PRBS tap point E. 0b1000000000111111 = 12-bit PRBS tap point F. 0b0000011000000000 = 12-bit PRBS tap point G. 0b0000011100000000 = 12-bit PRBS tap point H.

Register Name	Receive Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL
Address	8002C0260601143F (SCOM)
Description	This register contains the first set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	RX_PRBS_SEED_VALUE_0_15: Receive per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This setting must be set consistent with tx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in 12-bit or 24-bit synchronous mode. 0b0001000000000000 = 24-bit PRBS tap point A. 0b1111000000111110 = 24-bit PRBS tap point B. 0b0000011110111100 = 24-bit PRBS tap point C. 0b0000011111000111 = 24-bit PRBS tap point D. 0b0000001111101111 = 24-bit PRBS tap point E. 0b0001111100001111 = 24-bit PRBS tap point F. 0b0001100000000000 = 24-bit PRBS tap point G. 0b1001110000000000 = 24-bit PRBS tap point H. 0b1000010000000000 = 12-bit PRBS tap point A. 0b0111110000000000 = 12-bit PRBS tap point B. 0b0000000000001111 = 12-bit PRBS tap point C. 0b1100000000001111 = 12-bit PRBS tap point D. 0b1000000000000111 = 12-bit PRBS tap point E. 0b1000000000111111 = 12-bit PRBS tap point F. 0b0000011000000000 = 12-bit PRBS tap point G. 0b0000011100000000 = 12-bit PRBS tap point H.

Register Name	Receive Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL
Address	8002C0270601143F (SCOM)
Description	This register contains the first set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	RX_PRBS_SEED_VALUE_0_15: Receive per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This setting must be set consistent with tx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in 12-bit or 24-bit synchronous mode. 0b0001000000000000 = 24-bit PRBS tap point A. 0b1111000000111110 = 24-bit PRBS tap point B. 0b0000011110111100 = 24-bit PRBS tap point C. 0b0000011111000111 = 24-bit PRBS tap point D. 0b0000001111101111 = 24-bit PRBS tap point E. 0b0001111100001111 = 24-bit PRBS tap point F. 0b0001100000000000 = 24-bit PRBS tap point G. 0b1001110000000000 = 24-bit PRBS tap point H. 0b1000010000000000 = 12-bit PRBS tap point A. 0b0111110000000000 = 12-bit PRBS tap point B. 0b0000000000001111 = 12-bit PRBS tap point C. 0b1100000000001111 = 12-bit PRBS tap point D. 0b1000000000000111 = 12-bit PRBS tap point E. 0b1000000000111111 = 12-bit PRBS tap point F. 0b0000011000000000 = 12-bit PRBS tap point G. 0b0000011100000000 = 12-bit PRBS tap point H.

Register Name	Receive Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL
Address	8002C0280601143F (SCOM)
Description	This register contains the first set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	RX_PRBS_SEED_VALUE_0_15: Receive per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This setting must be set consistent with tx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in 12-bit or 24-bit synchronous mode. 0b0001000000000000 = 24-bit PRBS tap point A. 0b1111000000111110 = 24-bit PRBS tap point B. 0b0000011110111100 = 24-bit PRBS tap point C. 0b0000011111000111 = 24-bit PRBS tap point D. 0b0000001111101111 = 24-bit PRBS tap point E. 0b0001111100001111 = 24-bit PRBS tap point F. 0b0001100000000000 = 24-bit PRBS tap point G. 0b1001110000000000 = 24-bit PRBS tap point H. 0b1000010000000000 = 12-bit PRBS tap point A. 0b0111110000000000 = 12-bit PRBS tap point B. 0b0000000000001111 = 12-bit PRBS tap point C. 0b1100000000001111 = 12-bit PRBS tap point D. 0b1000000000000111 = 12-bit PRBS tap point E. 0b1000000000111111 = 12-bit PRBS tap point F. 0b0000011000000000 = 12-bit PRBS tap point G. 0b0000011100000000 = 12-bit PRBS tap point H.

Register Name	Receive Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL
Address	8002C0290601143F (SCOM)
Description	This register contains the first set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	RX_PRBS_SEED_VALUE_0_15: Receive per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This setting must be set consistent with tx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in 12-bit or 24-bit synchronous mode. 0b0001000000000000 = 24-bit PRBS tap point A. 0b1111000000111110 = 24-bit PRBS tap point B. 0b0000011110111100 = 24-bit PRBS tap point C. 0b0000011111000111 = 24-bit PRBS tap point D. 0b0000001111101111 = 24-bit PRBS tap point E. 0b0001111100001111 = 24-bit PRBS tap point F. 0b0001100000000000 = 24-bit PRBS tap point G. 0b1001110000000000 = 24-bit PRBS tap point H. 0b1000010000000000 = 12-bit PRBS tap point A. 0b0111110000000000 = 12-bit PRBS tap point B. 0b0000000000001111 = 12-bit PRBS tap point C. 0b1100000000001111 = 12-bit PRBS tap point D. 0b1000000000000111 = 12-bit PRBS tap point E. 0b1000000000111111 = 12-bit PRBS tap point F. 0b0000011000000000 = 12-bit PRBS tap point G. 0b0000011100000000 = 12-bit PRBS tap point H.

Register Name	Receive Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL
Address	8002C02A0601143F (SCOM)
Description	This register contains the first set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	RX_PRBS_SEED_VALUE_0_15: Receive per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This setting must be set consistent with tx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in 12-bit or 24-bit synchronous mode. 0b0001000000000000 = 24-bit PRBS tap point A. 0b1111000000111110 = 24-bit PRBS tap point B. 0b0000011110111100 = 24-bit PRBS tap point C. 0b0000011111000111 = 24-bit PRBS tap point D. 0b0000001111101111 = 24-bit PRBS tap point E. 0b0001111100001111 = 24-bit PRBS tap point F. 0b0001100000000000 = 24-bit PRBS tap point G. 0b1001110000000000 = 24-bit PRBS tap point H. 0b1000010000000000 = 12-bit PRBS tap point A. 0b0111110000000000 = 12-bit PRBS tap point B. 0b0000000000001111 = 12-bit PRBS tap point C. 0b1100000000001111 = 12-bit PRBS tap point D. 0b1000000000000111 = 12-bit PRBS tap point E. 0b1000000000111111 = 12-bit PRBS tap point F. 0b0000011000000000 = 12-bit PRBS tap point G. 0b0000011100000000 = 12-bit PRBS tap point H.

Register Name	Receive Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL
Address	8002C02B0601143F (SCOM)
Description	This register contains the first set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	RX_PRBS_SEED_VALUE_0_15: Receive per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This setting must be set consistent with tx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in 12-bit or 24-bit synchronous mode. 0b0001000000000000 = 24-bit PRBS tap point A. 0b1111000000111110 = 24-bit PRBS tap point B. 0b0000011110111100 = 24-bit PRBS tap point C. 0b0000011111000111 = 24-bit PRBS tap point D. 0b0000001111101111 = 24-bit PRBS tap point E. 0b0001111100001111 = 24-bit PRBS tap point F. 0b0001100000000000 = 24-bit PRBS tap point G. 0b1001110000000000 = 24-bit PRBS tap point H. 0b1000010000000000 = 12-bit PRBS tap point A. 0b0111110000000000 = 12-bit PRBS tap point B. 0b0000000000001111 = 12-bit PRBS tap point C. 0b1100000000001111 = 12-bit PRBS tap point D. 0b1000000000000111 = 12-bit PRBS tap point E. 0b1000000000111111 = 12-bit PRBS tap point F. 0b0000011000000000 = 12-bit PRBS tap point G. 0b0000011100000000 = 12-bit PRBS tap point H.

Register Name	Receive Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL
Address	8002C02C0601143F (SCOM)
Description	This register contains the first set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	RX_PRBS_SEED_VALUE_0_15: Receive per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This setting must be set consistent with tx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in 12-bit or 24-bit synchronous mode. 0b0001000000000000 = 24-bit PRBS tap point A. 0b1111000000111110 = 24-bit PRBS tap point B. 0b0000011110111100 = 24-bit PRBS tap point C. 0b0000011111000111 = 24-bit PRBS tap point D. 0b0000001111101111 = 24-bit PRBS tap point E. 0b0001111100001111 = 24-bit PRBS tap point F. 0b0001100000000000 = 24-bit PRBS tap point G. 0b1001110000000000 = 24-bit PRBS tap point H. 0b1000010000000000 = 12-bit PRBS tap point A. 0b0111110000000000 = 12-bit PRBS tap point B. 0b0000000000001111 = 12-bit PRBS tap point C. 0b1100000000001111 = 12-bit PRBS tap point D. 0b1000000000000111 = 12-bit PRBS tap point E. 0b1000000000111111 = 12-bit PRBS tap point F. 0b0000011000000000 = 12-bit PRBS tap point G. 0b0000011100000000 = 12-bit PRBS tap point H.

Register Name	Receive Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL
Address	8002C02D0601143F (SCOM)
Description	This register contains the first set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	RX_PRBS_SEED_VALUE_0_15: Receive per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This setting must be set consistent with tx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in 12-bit or 24-bit synchronous mode. 0b0001000000000000 = 24-bit PRBS tap point A. 0b1111000000111110 = 24-bit PRBS tap point B. 0b0000011110111100 = 24-bit PRBS tap point C. 0b0000011111000111 = 24-bit PRBS tap point D. 0b0000001111101111 = 24-bit PRBS tap point E. 0b0001111100001111 = 24-bit PRBS tap point F. 0b0001100000000000 = 24-bit PRBS tap point G. 0b1001110000000000 = 24-bit PRBS tap point H. 0b1000010000000000 = 12-bit PRBS tap point A. 0b0111110000000000 = 12-bit PRBS tap point B. 0b0000000000001111 = 12-bit PRBS tap point C. 0b1100000000001111 = 12-bit PRBS tap point D. 0b1000000000000111 = 12-bit PRBS tap point E. 0b1000000000111111 = 12-bit PRBS tap point F. 0b0000011000000000 = 12-bit PRBS tap point G. 0b0000011100000000 = 12-bit PRBS tap point H.

Register Name	Receive Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL
Address	8002C02E0601143F (SCOM)
Description	This register contains the first set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	RX_PRBS_SEED_VALUE_0_15: Receive per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This setting must be set consistent with tx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in 12-bit or 24-bit synchronous mode. 0b0001000000000000 = 24-bit PRBS tap point A. 0b1111000000111110 = 24-bit PRBS tap point B. 0b0000011110111100 = 24-bit PRBS tap point C. 0b0000011111000111 = 24-bit PRBS tap point D. 0b0000001111101111 = 24-bit PRBS tap point E. 0b0001111100001111 = 24-bit PRBS tap point F. 0b0001100000000000 = 24-bit PRBS tap point G. 0b1001110000000000 = 24-bit PRBS tap point H. 0b1000010000000000 = 12-bit PRBS tap point A. 0b0111110000000000 = 12-bit PRBS tap point B. 0b0000000000001111 = 12-bit PRBS tap point C. 0b1100000000001111 = 12-bit PRBS tap point D. 0b1000000000000111 = 12-bit PRBS tap point E. 0b1000000000111111 = 12-bit PRBS tap point F. 0b0000011000000000 = 12-bit PRBS tap point G. 0b0000011100000000 = 12-bit PRBS tap point H.

Register Name	Receive Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL
Address	8002C02F0601143F (SCOM)
Description	This register contains the first set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	RX_PRBS_SEED_VALUE_0_15: Receive per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This setting must be set consistent with tx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in 12-bit or 24-bit synchronous mode. 0b0001000000000000 = 24-bit PRBS tap point A. 0b1111000000111110 = 24-bit PRBS tap point B. 0b0000011110111100 = 24-bit PRBS tap point C. 0b0000011111000111 = 24-bit PRBS tap point D. 0b0000001111101111 = 24-bit PRBS tap point E. 0b0001111100001111 = 24-bit PRBS tap point F. 0b0001100000000000 = 24-bit PRBS tap point G. 0b1001110000000000 = 24-bit PRBS tap point H. 0b1000010000000000 = 12-bit PRBS tap point A. 0b0111110000000000 = 12-bit PRBS tap point B. 0b0000000000001111 = 12-bit PRBS tap point C. 0b1100000000001111 = 12-bit PRBS tap point D. 0b1000000000000111 = 12-bit PRBS tap point E. 0b1000000000111111 = 12-bit PRBS tap point F. 0b0000011000000000 = 12-bit PRBS tap point G. 0b0000011100000000 = 12-bit PRBS tap point H.

Register Name	Receive Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL
Address	8002C0300601143F (SCOM)
Description	This register contains the first set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	RX_PRBS_SEED_VALUE_0_15: Receive per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This setting must be set consistent with tx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in 12-bit or 24-bit synchronous mode. 0b0001000000000000 = 24-bit PRBS tap point A. 0b1111000000111110 = 24-bit PRBS tap point B. 0b0000011110111100 = 24-bit PRBS tap point C. 0b0000011111000111 = 24-bit PRBS tap point D. 0b0000001111101111 = 24-bit PRBS tap point E. 0b0001111100001111 = 24-bit PRBS tap point F. 0b0001100000000000 = 24-bit PRBS tap point G. 0b1001110000000000 = 24-bit PRBS tap point H. 0b1000010000000000 = 12-bit PRBS tap point A. 0b0111110000000000 = 12-bit PRBS tap point B. 0b0000000000001111 = 12-bit PRBS tap point C. 0b1100000000001111 = 12-bit PRBS tap point D. 0b1000000000000111 = 12-bit PRBS tap point E. 0b1000000000111111 = 12-bit PRBS tap point F. 0b0000011000000000 = 12-bit PRBS tap point G. 0b0000011100000000 = 12-bit PRBS tap point H.

Register Name	**Receive Bit Mode 1 E Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_E_PL
Address	8002C0310601143F (SCOM)
Description	This register contains the first set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	RX_PRBS_SEED_VALUE_0_15: Receive per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This setting must be set consistent with tx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in 12-bit or 24-bit synchronous mode. 0b0001000000000000 = 24-bit PRBS tap point A. 0b1111000000111110 = 24-bit PRBS tap point B. 0b0000011110111100 = 24-bit PRBS tap point C. 0b0000011111000111 = 24-bit PRBS tap point D. 0b0000001111101111 = 24-bit PRBS tap point E. 0b0001111100001111 = 24-bit PRBS tap point F. 0b0001100000000000 = 24-bit PRBS tap point G. 0b1001110000000000 = 24-bit PRBS tap point H. 0b1000010000000000 = 12-bit PRBS tap point A. 0b0111110000000000 = 12-bit PRBS tap point B. 0b0000000000001111 = 12-bit PRBS tap point C. 0b1100000000001111 = 12-bit PRBS tap point D. 0b1000000000000111 = 12-bit PRBS tap point E. 0b1000000000111111 = 12-bit PRBS tap point F. 0b0000011000000000 = 12-bit PRBS tap point G. 0b0000011100000000 = 12-bit PRBS tap point H.

Register Name	Receive Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL
Address	8002C8000601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RX_PRBS_SEED_VALUE_16_22: Least significant bits of the receive per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b1000010 = 24-bit PRBS tap point A. 0b0111110 = 24-bit PRBS tap point B. 0b0000000 = 24-bit PRBS tap point C, and 12-bit PRBS tap points A, C, G, and H. 0b1100000 = 24-bit PRBS tap point D. 0b1000000 = 24-bit PRBS tap points E and F. 0b0000011 = 24-bit PRBS tap points G and H. 0b0111111 = 12-bit PRBS tap point B. 0b1111000 = 12-bit PRBS tap point D. 0b1110000 = 12-bit PRBS tap points E and F.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL
Address	8002C8010601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the receive per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b1000010 = 24-bit PRBS tap point A. 0b0111110 = 24-bit PRBS tap point B. 0b0000000 = 24-bit PRBS tap point C, and 12-bit PRBS tap points A, C, G, and H. 0b1100000 = 24-bit PRBS tap point D. 0b1000000 = 24-bit PRBS tap points E and F. 0b0000011 = 24-bit PRBS tap points G and H. 0b0111111 = 12-bit PRBS tap point B. 0b1111000 = 12-bit PRBS tap point D. 0b1110000 = 12-bit PRBS tap points E and F.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL
Address	8002C8020601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	RX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the receive per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b1000010 = 24-bit PRBS tap point A. 0b0111110 = 24-bit PRBS tap point B. 0b0000000 = 24-bit PRBS tap point C, and 12-bit PRBS tap points A, C, G, and H. 0b1100000 = 24-bit PRBS tap point D. 0b1000000 = 24-bit PRBS tap points E and F. 0b0000011 = 24-bit PRBS tap points G and H. 0b0111111 = 12-bit PRBS tap point B. 0b1111000 = 12-bit PRBS tap point D. 0b1110000 = 12-bit PRBS tap points E and F.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL
Address	8002C8030601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the receive per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b1000010 = 24-bit PRBS tap point A. 0b0111110 = 24-bit PRBS tap point B. 0b0000000 = 24-bit PRBS tap point C, and 12-bit PRBS tap points A, C, G, and H. 0b1100000 = 24-bit PRBS tap point D. 0b1000000 = 24-bit PRBS tap points E and F. 0b0000011 = 24-bit PRBS tap points G and H. 0b0111111 = 12-bit PRBS tap point B. 0b1111000 = 12-bit PRBS tap point D. 0b1110000 = 12-bit PRBS tap points E and F.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL
Address	8002C8040601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	RX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the receive per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b1000010 = 24-bit PRBS tap point A. 0b0111110 = 24-bit PRBS tap point B. 0b0000000 = 24-bit PRBS tap point C, and 12-bit PRBS tap points A, C, G, and H. 0b1100000 = 24-bit PRBS tap point D. 0b1000000 = 24-bit PRBS tap points E and F. 0b0000011 = 24-bit PRBS tap points G and H. 0b0111111 = 12-bit PRBS tap point B. 0b1111000 = 12-bit PRBS tap point D. 0b1110000 = 12-bit PRBS tap points E and F.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL
Address	8002C8050601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the receive per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b1000010 = 24-bit PRBS tap point A. 0b0111110 = 24-bit PRBS tap point B. 0b0000000 = 24-bit PRBS tap point C, and 12-bit PRBS tap points A, C, G, and H. 0b1100000 = 24-bit PRBS tap point D. 0b1000000 = 24-bit PRBS tap points E and F. 0b0000011 = 24-bit PRBS tap points G and H. 0b0111111 = 12-bit PRBS tap point B. 0b1111000 = 12-bit PRBS tap point D. 0b1110000 = 12-bit PRBS tap points E and F.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL
Address	8002C8060601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	RX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the receive per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b1000010 = 24-bit PRBS tap point A. 0b0111110 = 24-bit PRBS tap point B. 0b0000000 = 24-bit PRBS tap point C, and 12-bit PRBS tap points A, C, G, and H. 0b1100000 = 24-bit PRBS tap point D. 0b1000000 = 24-bit PRBS tap points E and F. 0b0000011 = 24-bit PRBS tap points G and H. 0b0111111 = 12-bit PRBS tap point B. 0b1111000 = 12-bit PRBS tap point D. 0b1110000 = 12-bit PRBS tap points E and F.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL
Address	8002C8070601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the receive per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b1000010 = 24-bit PRBS tap point A. 0b0111110 = 24-bit PRBS tap point B. 0b0000000 = 24-bit PRBS tap point C, and 12-bit PRBS tap points A, C, G, and H. 0b1100000 = 24-bit PRBS tap point D. 0b1000000 = 24-bit PRBS tap points E and F. 0b0000011 = 24-bit PRBS tap points G and H. 0b0111111 = 12-bit PRBS tap point B. 0b1111000 = 12-bit PRBS tap point D. 0b1110000 = 12-bit PRBS tap points E and F.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL
Address	8002C8080601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	RX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the receive per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b1000010 = 24-bit PRBS tap point A. 0b0111110 = 24-bit PRBS tap point B. 0b0000000 = 24-bit PRBS tap point C, and 12-bit PRBS tap points A, C, G, and H. 0b1100000 = 24-bit PRBS tap point D. 0b1000000 = 24-bit PRBS tap points E and F. 0b0000011 = 24-bit PRBS tap points G and H. 0b0111111 = 12-bit PRBS tap point B. 0b1111000 = 12-bit PRBS tap point D. 0b1110000 = 12-bit PRBS tap points E and F.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL
Address	8002C8090601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the receive per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b1000010 = 24-bit PRBS tap point A. 0b0111110 = 24-bit PRBS tap point B. 0b0000000 = 24-bit PRBS tap point C, and 12-bit PRBS tap points A, C, G, and H. 0b1100000 = 24-bit PRBS tap point D. 0b1000000 = 24-bit PRBS tap points E and F. 0b0000011 = 24-bit PRBS tap points G and H. 0b0111111 = 12-bit PRBS tap point B. 0b1111000 = 12-bit PRBS tap point D. 0b1110000 = 12-bit PRBS tap points E and F.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL
Address	8002C80A0601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	RX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the receive per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b1000010 = 24-bit PRBS tap point A. 0b0111110 = 24-bit PRBS tap point B. 0b0000000 = 24-bit PRBS tap point C, and 12-bit PRBS tap points A, C, G, and H. 0b1100000 = 24-bit PRBS tap point D. 0b1000000 = 24-bit PRBS tap points E and F. 0b0000011 = 24-bit PRBS tap points G and H. 0b0111111 = 12-bit PRBS tap point B. 0b1111000 = 12-bit PRBS tap point D. 0b1110000 = 12-bit PRBS tap points E and F.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL
Address	8002C80B0601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the receive per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b1000010 = 24-bit PRBS tap point A. 0b0111110 = 24-bit PRBS tap point B. 0b0000000 = 24-bit PRBS tap point C, and 12-bit PRBS tap points A, C, G, and H. 0b1100000 = 24-bit PRBS tap point D. 0b1000000 = 24-bit PRBS tap points E and F. 0b0000011 = 24-bit PRBS tap points G and H. 0b0111111 = 12-bit PRBS tap point B. 0b1111000 = 12-bit PRBS tap point D. 0b1110000 = 12-bit PRBS tap points E and F.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL
Address	8002C80C0601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	RX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the receive per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b1000010 = 24-bit PRBS tap point A. 0b0111110 = 24-bit PRBS tap point B. 0b0000000 = 24-bit PRBS tap point C, and 12-bit PRBS tap points A, C, G, and H. 0b1100000 = 24-bit PRBS tap point D. 0b1000000 = 24-bit PRBS tap points E and F. 0b0000011 = 24-bit PRBS tap points G and H. 0b0111111 = 12-bit PRBS tap point B. 0b1111000 = 12-bit PRBS tap point D. 0b1110000 = 12-bit PRBS tap points E and F.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL
Address	8002C80D0601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the receive per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b1000010 = 24-bit PRBS tap point A. 0b0111110 = 24-bit PRBS tap point B. 0b0000000 = 24-bit PRBS tap point C, and 12-bit PRBS tap points A, C, G, and H. 0b1100000 = 24-bit PRBS tap point D. 0b1000000 = 24-bit PRBS tap points E and F. 0b0000011 = 24-bit PRBS tap points G and H. 0b0111111 = 12-bit PRBS tap point B. 0b1111000 = 12-bit PRBS tap point D. 0b1110000 = 12-bit PRBS tap points E and F.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL
Address	8002C80E0601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	RX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the receive per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b1000010 = 24-bit PRBS tap point A. 0b0111110 = 24-bit PRBS tap point B. 0b0000000 = 24-bit PRBS tap point C, and 12-bit PRBS tap points A, C, G, and H. 0b1100000 = 24-bit PRBS tap point D. 0b1000000 = 24-bit PRBS tap points E and F. 0b0000011 = 24-bit PRBS tap points G and H. 0b0111111 = 12-bit PRBS tap point B. 0b1111000 = 12-bit PRBS tap point D. 0b1110000 = 12-bit PRBS tap points E and F.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL
Address	8002C80F0601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the receive per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b1000010 = 24-bit PRBS tap point A. 0b0111110 = 24-bit PRBS tap point B. 0b0000000 = 24-bit PRBS tap point C, and 12-bit PRBS tap points A, C, G, and H. 0b1100000 = 24-bit PRBS tap point D. 0b1000000 = 24-bit PRBS tap points E and F. 0b0000011 = 24-bit PRBS tap points G and H. 0b0111111 = 12-bit PRBS tap point B. 0b1111000 = 12-bit PRBS tap point D. 0b1110000 = 12-bit PRBS tap points E and F.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL
Address	8002C8100601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	RX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the receive per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b1000010 = 24-bit PRBS tap point A. 0b0111110 = 24-bit PRBS tap point B. 0b0000000 = 24-bit PRBS tap point C, and 12-bit PRBS tap points A, C, G, and H. 0b1100000 = 24-bit PRBS tap point D. 0b1000000 = 24-bit PRBS tap points E and F. 0b0000011 = 24-bit PRBS tap points G and H. 0b0111111 = 12-bit PRBS tap point B. 0b1111000 = 12-bit PRBS tap point D. 0b1110000 = 12-bit PRBS tap points E and F.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL
Address	8002C8110601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the receive per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b1000010 = 24-bit PRBS tap point A. 0b0111110 = 24-bit PRBS tap point B. 0b0000000 = 24-bit PRBS tap point C, and 12-bit PRBS tap points A, C, G, and H. 0b1100000 = 24-bit PRBS tap point D. 0b1000000 = 24-bit PRBS tap points E and F. 0b0000011 = 24-bit PRBS tap points G and H. 0b0111111 = 12-bit PRBS tap point B. 0b1111000 = 12-bit PRBS tap point D. 0b1110000 = 12-bit PRBS tap points E and F.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL
Address	8002C8200601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	RX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the receive per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b1000010 = 24-bit PRBS tap point A. 0b0111110 = 24-bit PRBS tap point B. 0b0000000 = 24-bit PRBS tap point C, and 12-bit PRBS tap points A, C, G, and H. 0b1100000 = 24-bit PRBS tap point D. 0b1000000 = 24-bit PRBS tap points E and F. 0b0000011 = 24-bit PRBS tap points G and H. 0b0111111 = 12-bit PRBS tap point B. 0b1111000 = 12-bit PRBS tap point D. 0b1110000 = 12-bit PRBS tap points E and F.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL
Address	8002C8210601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the receive per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b1000010 = 24-bit PRBS tap point A. 0b0111110 = 24-bit PRBS tap point B. 0b0000000 = 24-bit PRBS tap point C, and 12-bit PRBS tap points A, C, G, and H. 0b1100000 = 24-bit PRBS tap point D. 0b1000000 = 24-bit PRBS tap points E and F. 0b0000011 = 24-bit PRBS tap points G and H. 0b0111111 = 12-bit PRBS tap point B. 0b1111000 = 12-bit PRBS tap point D. 0b1110000 = 12-bit PRBS tap points E and F.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL
Address	8002C8220601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	RX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the receive per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b1000010 = 24-bit PRBS tap point A. 0b0111110 = 24-bit PRBS tap point B. 0b0000000 = 24-bit PRBS tap point C, and 12-bit PRBS tap points A, C, G, and H. 0b1100000 = 24-bit PRBS tap point D. 0b1000000 = 24-bit PRBS tap points E and F. 0b0000011 = 24-bit PRBS tap points G and H. 0b0111111 = 12-bit PRBS tap point B. 0b1111000 = 12-bit PRBS tap point D. 0b1110000 = 12-bit PRBS tap points E and F.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL
Address	8002C8230601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the receive per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b1000010 = 24-bit PRBS tap point A. 0b0111110 = 24-bit PRBS tap point B. 0b0000000 = 24-bit PRBS tap point C, and 12-bit PRBS tap points A, C, G, and H. 0b1100000 = 24-bit PRBS tap point D. 0b1000000 = 24-bit PRBS tap points E and F. 0b0000011 = 24-bit PRBS tap points G and H. 0b0111111 = 12-bit PRBS tap point B. 0b1111000 = 12-bit PRBS tap point D. 0b1110000 = 12-bit PRBS tap points E and F.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL
Address	8002C8240601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	RX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the receive per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b1000010 = 24-bit PRBS tap point A. 0b0111110 = 24-bit PRBS tap point B. 0b0000000 = 24-bit PRBS tap point C, and 12-bit PRBS tap points A, C, G, and H. 0b1100000 = 24-bit PRBS tap point D. 0b1000000 = 24-bit PRBS tap points E and F. 0b0000011 = 24-bit PRBS tap points G and H. 0b0111111 = 12-bit PRBS tap point B. 0b1111000 = 12-bit PRBS tap point D. 0b1110000 = 12-bit PRBS tap points E and F.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL
Address	8002C8250601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the receive per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b1000010 = 24-bit PRBS tap point A. 0b0111110 = 24-bit PRBS tap point B. 0b0000000 = 24-bit PRBS tap point C, and 12-bit PRBS tap points A, C, G, and H. 0b1100000 = 24-bit PRBS tap point D. 0b1000000 = 24-bit PRBS tap points E and F. 0b0000011 = 24-bit PRBS tap points G and H. 0b0111111 = 12-bit PRBS tap point B. 0b1111000 = 12-bit PRBS tap point D. 0b1110000 = 12-bit PRBS tap points E and F.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL
Address	8002C8260601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	RX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the receive per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b1000010 = 24-bit PRBS tap point A. 0b0111110 = 24-bit PRBS tap point B. 0b0000000 = 24-bit PRBS tap point C, and 12-bit PRBS tap points A, C, G, and H. 0b1100000 = 24-bit PRBS tap point D. 0b1000000 = 24-bit PRBS tap points E and F. 0b0000011 = 24-bit PRBS tap points G and H. 0b0111111 = 12-bit PRBS tap point B. 0b1111000 = 12-bit PRBS tap point D. 0b1110000 = 12-bit PRBS tap points E and F.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL
Address	8002C8270601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the receive per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b1000010 = 24-bit PRBS tap point A. 0b0111110 = 24-bit PRBS tap point B. 0b0000000 = 24-bit PRBS tap point C, and 12-bit PRBS tap points A, C, G, and H. 0b1100000 = 24-bit PRBS tap point D. 0b1000000 = 24-bit PRBS tap points E and F. 0b0000011 = 24-bit PRBS tap points G and H. 0b0111111 = 12-bit PRBS tap point B. 0b1111000 = 12-bit PRBS tap point D. 0b1110000 = 12-bit PRBS tap points E and F.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL
Address	8002C8280601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	RX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the receive per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b1000010 = 24-bit PRBS tap point A. 0b0111110 = 24-bit PRBS tap point B. 0b0000000 = 24-bit PRBS tap point C, and 12-bit PRBS tap points A, C, G, and H. 0b1100000 = 24-bit PRBS tap point D. 0b1000000 = 24-bit PRBS tap points E and F. 0b0000011 = 24-bit PRBS tap points G and H. 0b0111111 = 12-bit PRBS tap point B. 0b1111000 = 12-bit PRBS tap point D. 0b1110000 = 12-bit PRBS tap points E and F.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL
Address	8002C8290601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the receive per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b1000010 = 24-bit PRBS tap point A. 0b0111110 = 24-bit PRBS tap point B. 0b0000000 = 24-bit PRBS tap point C, and 12-bit PRBS tap points A, C, G, and H. 0b1100000 = 24-bit PRBS tap point D. 0b1000000 = 24-bit PRBS tap points E and F. 0b0000011 = 24-bit PRBS tap points G and H. 0b0111111 = 12-bit PRBS tap point B. 0b1111000 = 12-bit PRBS tap point D. 0b1110000 = 12-bit PRBS tap points E and F.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL
Address	8002C82A0601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	RX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the receive per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b1000010 = 24-bit PRBS tap point A. 0b0111110 = 24-bit PRBS tap point B. 0b0000000 = 24-bit PRBS tap point C, and 12-bit PRBS tap points A, C, G, and H. 0b1100000 = 24-bit PRBS tap point D. 0b1000000 = 24-bit PRBS tap points E and F. 0b0000011 = 24-bit PRBS tap points G and H. 0b0111111 = 12-bit PRBS tap point B. 0b1111000 = 12-bit PRBS tap point D. 0b1110000 = 12-bit PRBS tap points E and F.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL
Address	8002C82B0601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the receive per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b1000010 = 24-bit PRBS tap point A. 0b0111110 = 24-bit PRBS tap point B. 0b0000000 = 24-bit PRBS tap point C, and 12-bit PRBS tap points A, C, G, and H. 0b1100000 = 24-bit PRBS tap point D. 0b1000000 = 24-bit PRBS tap points E and F. 0b0000011 = 24-bit PRBS tap points G and H. 0b0111111 = 12-bit PRBS tap point B. 0b1111000 = 12-bit PRBS tap point D. 0b1110000 = 12-bit PRBS tap points E and F.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL
Address	8002C82C0601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	RX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the receive per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b1000010 = 24-bit PRBS tap point A. 0b0111110 = 24-bit PRBS tap point B. 0b0000000 = 24-bit PRBS tap point C, and 12-bit PRBS tap points A, C, G, and H. 0b1100000 = 24-bit PRBS tap point D. 0b1000000 = 24-bit PRBS tap points E and F. 0b0000011 = 24-bit PRBS tap points G and H. 0b0111111 = 12-bit PRBS tap point B. 0b1111000 = 12-bit PRBS tap point D. 0b1110000 = 12-bit PRBS tap points E and F.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL
Address	8002C82D0601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the receive per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b1000010 = 24-bit PRBS tap point A. 0b0111110 = 24-bit PRBS tap point B. 0b0000000 = 24-bit PRBS tap point C, and 12-bit PRBS tap points A, C, G, and H. 0b1100000 = 24-bit PRBS tap point D. 0b1000000 = 24-bit PRBS tap points E and F. 0b0000011 = 24-bit PRBS tap points G and H. 0b0111111 = 12-bit PRBS tap point B. 0b1111000 = 12-bit PRBS tap point D. 0b1110000 = 12-bit PRBS tap points E and F.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL
Address	8002C82E0601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	RX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the receive per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b1000010 = 24-bit PRBS tap point A. 0b0111110 = 24-bit PRBS tap point B. 0b0000000 = 24-bit PRBS tap point C, and 12-bit PRBS tap points A, C, G, and H. 0b1100000 = 24-bit PRBS tap point D. 0b1000000 = 24-bit PRBS tap points E and F. 0b0000011 = 24-bit PRBS tap points G and H. 0b0111111 = 12-bit PRBS tap point B. 0b1111000 = 12-bit PRBS tap point D. 0b1110000 = 12-bit PRBS tap points E and F.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL
Address	8002C82F0601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the receive per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b1000010 = 24-bit PRBS tap point A. 0b0111110 = 24-bit PRBS tap point B. 0b0000000 = 24-bit PRBS tap point C, and 12-bit PRBS tap points A, C, G, and H. 0b1100000 = 24-bit PRBS tap point D. 0b1000000 = 24-bit PRBS tap points E and F. 0b0000011 = 24-bit PRBS tap points G and H. 0b0111111 = 12-bit PRBS tap point B. 0b1111000 = 12-bit PRBS tap point D. 0b1110000 = 12-bit PRBS tap points E and F.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL
Address	8002C8300601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	RX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the receive per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b1000010 = 24-bit PRBS tap point A. 0b0111110 = 24-bit PRBS tap point B. 0b0000000 = 24-bit PRBS tap point C, and 12-bit PRBS tap points A, C, G, and H. 0b1100000 = 24-bit PRBS tap point D. 0b1000000 = 24-bit PRBS tap points E and F. 0b0000011 = 24-bit PRBS tap points G and H. 0b0111111 = 12-bit PRBS tap point B. 0b1111000 = 12-bit PRBS tap point D. 0b1110000 = 12-bit PRBS tap points E and F.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_E_PL
Address	8002C8310601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the receive per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b1000010 = 24-bit PRBS tap point A. 0b0111110 = 24-bit PRBS tap point B. 0b0000000 = 24-bit PRBS tap point C, and 12-bit PRBS tap points A, C, G, and H. 0b1100000 = 24-bit PRBS tap point D. 0b1000000 = 24-bit PRBS tap points E and F. 0b0000011 = 24-bit PRBS tap points G and H. 0b0111111 = 12-bit PRBS tap point B. 0b1111000 = 12-bit PRBS tap point D. 0b1110000 = 12-bit PRBS tap points E and F.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL
Address	800300000601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60	NCX	Reserved field.
61	NCX	Reserved field.
62	NCX	Reserved field.
63	RO	constant = 0b0

Register Name	**Receive Bit Control 1 E Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL
Address	800300010601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60	NCX	Reserved field.
61	NCX	Reserved field.
62	NCX	Reserved field.
63	RO	constant = 0b0

Register Name	Receive Bit Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL
Address	800300020601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60	NCX	Reserved field.
61	NCX	Reserved field.
62	NCX	Reserved field.
63	RO	constant = 0b0

Register Name	Receive Bit Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL
Address	800300030601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60	NCX	Reserved field.
61	NCX	Reserved field.
62	NCX	Reserved field.
63	RO	constant = 0b0

Register Name	**Receive Bit Control 1 E Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL
Address	800300040601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60	NCX	Reserved field.
61	NCX	Reserved field.
62	NCX	Reserved field.
63	RO	constant = 0b0

Register Name	**Receive Bit Control 1 E Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL
Address	800300050601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60	NCX	Reserved field.
61	NCX	Reserved field.
62	NCX	Reserved field.
63	RO	constant = 0b0

Register Name	Receive Bit Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL
Address	800300060601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60	NCX	Reserved field.
61	NCX	Reserved field.
62	NCX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
63	RO	constant = 0b0

Register Name	Receive Bit Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL
Address	800300070601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60	NCX	Reserved field.
61	NCX	Reserved field.
62	NCX	Reserved field.
63	RO	constant = 0b0

Register Name	Receive Bit Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL
Address	800300080601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60	NCX	Reserved field.
61	NCX	Reserved field.
62	NCX	Reserved field.
63	RO	constant = 0b0

Register Name	Receive Bit Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL
Address	800300090601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60	NCX	Reserved field.
61	NCX	Reserved field.
62	NCX	Reserved field.
63	RO	constant = 0b0

Register Name	Receive Bit Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL
Address	8003000A0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60	NCX	Reserved field.
61	NCX	Reserved field.
62	NCX	Reserved field.
63	RO	constant = 0b0

Register Name	Receive Bit Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL
Address	8003000B0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60	NCX	Reserved field.
61	NCX	Reserved field.
62	NCX	Reserved field.
63	RO	constant = 0b0

Register Name	Receive Bit Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL
Address	8003000C0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60	NCX	Reserved field.
61	NCX	Reserved field.
62	NCX	Reserved field.
63	RO	constant = 0b0

Register Name	Receive Bit Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL
Address	8003000D0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60	NCX	Reserved field.
61	NCX	Reserved field.
62	NCX	Reserved field.
63	RO	constant = 0b0

Register Name	**Receive Bit Control 1 E Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL
Address	8003000E0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60	NCX	Reserved field.
61	NCX	Reserved field.
62	NCX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
63	RO	constant = 0b0

Register Name	Receive Bit Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL
Address	8003000F0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60	NCX	Reserved field.
61	NCX	Reserved field.
62	NCX	Reserved field.
63	RO	constant = 0b0

Register Name	Receive Bit Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL
Address	800300100601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60	NCX	Reserved field.
61	NCX	Reserved field.
62	NCX	Reserved field.
63	RO	constant = 0b0

Register Name	Receive Bit Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL
Address	800300110601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60	NCX	Reserved field.
61	NCX	Reserved field.
62	NCX	Reserved field.
63	RO	constant = 0b0

Register Name	Receive Bit Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL
Address	800300200601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60	NCX	Reserved field.
61	NCX	Reserved field.
62	NCX	Reserved field.
63	RO	constant = 0b0

Register Name	Receive Bit Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL
Address	800300210601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60	NCX	Reserved field.
61	NCX	Reserved field.
62	NCX	Reserved field.
63	RO	constant = 0b0

Register Name	Receive Bit Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS. Receive Bit Control 1 E Per-Lane Register
Address	800300220601143F (SCOM)
Description	Register

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60	NCX	Reserved field.
61	NCX	Reserved field.
62	NCX	Reserved field.
63	RO	constant = 0b0

Register Name	Receive Bit Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL
Address	800300230601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60	NCX	Reserved field.
61	NCX	Reserved field.
62	NCX	Reserved field.
63	RO	constant = 0b0

Register Name	Receive Bit Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL
Address	800300240601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60	NCX	Reserved field.
61	NCX	Reserved field.
62	NCX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
63	RO	constant = 0b0

Register Name	Receive Bit Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL
Address	800300250601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60	NCX	Reserved field.
61	NCX	Reserved field.
62	NCX	Reserved field.
63	RO	constant = 0b0

Register Name	Receive Bit Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL
Address	800300260601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60	NCX	Reserved field.
61	NCX	Reserved field.
62	NCX	Reserved field.
63	RO	constant = 0b0

Register Name	Receive Bit Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL
Address	800300270601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60	NCX	Reserved field.
61	NCX	Reserved field.
62	NCX	Reserved field.
63	RO	constant = 0b0

Register Name	Receive Bit Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL
Address	800300280601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60	NCX	Reserved field.
61	NCX	Reserved field.
62	NCX	Reserved field.
63	RO	constant = 0b0

Register Name	Receive Bit Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL
Address	800300290601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60	NCX	Reserved field.
61	NCX	Reserved field.
62	NCX	Reserved field.
63	RO	constant = 0b0

Register Name	Receive Bit Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL
Address	8003002A0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60	NCX	Reserved field.
61	NCX	Reserved field.
62	NCX	Reserved field.
63	RO	constant = 0b0

Register Name	Receive Bit Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL
Address	8003002B0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60	NCX	Reserved field.
61	NCX	Reserved field.
62	NCX	Reserved field.
63	RO	constant = 0b0

Register Name	Receive Bit Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL
Address	8003002C0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60	NCX	Reserved field.
61	NCX	Reserved field.
62	NCX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
63	RO	constant = 0b0

Register Name	Receive Bit Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL
Address	8003002D0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60	NCX	Reserved field.
61	NCX	Reserved field.
62	NCX	Reserved field.
63	RO	constant = 0b0

Register Name	Receive Bit Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL
Address	8003002E0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60	NCX	Reserved field.
61	NCX	Reserved field.
62	NCX	Reserved field.
63	RO	constant = 0b0

Register Name	**Receive Bit Control 1 E Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL
Address	8003002F0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60	NCX	Reserved field.
61	NCX	Reserved field.
62	NCX	Reserved field.
63	RO	constant = 0b0

Register Name	Receive Bit Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL
Address	800300300601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60	NCX	Reserved field.
61	NCX	Reserved field.
62	NCX	Reserved field.
63	RO	constant = 0b0

Register Name	Receive Bit Control 1 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL1_E_PL
Address	800300310601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60	NCX	Reserved field.
61	NCX	Reserved field.
62	NCX	Reserved field.
63	RO	constant = 0b0

Register Name	**Receive Bit Control 2 E Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL
Address	800308000601143F (SCOM)
Description	This register contains the second set of E control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: Receive FIFO load-to-unload delay. This field is initialized during FIFO initialization. It is modified thereafter by the deskew machine. For setting X, the latency is 4 x X to 4 x X + 4 UI. The default is 20 - 24 UI.
52:63	RO	constant = 0b000000000000

Register Name	**Receive Bit Control 2 E Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL
Address	800308010601143F (SCOM)
Description	This register contains the second set of E control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: Receive FIFO load-to-unload delay. This field is initialized during FIFO initialization. It is modified thereafter by the deskew machine. For setting X, the latency is 4 x X to 4 x X + 4 UI. The default is 20 - 24 UI.
52:63	RO	constant = 0b000000000000

Register Name	**Receive Bit Control 2 E Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL
Address	800308020601143F (SCOM)
Description	This register contains the second set of E control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RWX	RX_FIFO_L2U_DLY: Receive FIFO load-to-unload delay. This field is initialized during FIFO initialization. It is modified thereafter by the deskew machine. For setting X, the latency is 4 x X to 4 x X + 4 UI. The default is 20 - 24 UI.
52:63	RO	constant = 0b000000000000

Register Name	Receive Bit Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL
Address	800308030601143F (SCOM)
Description	This register contains the second set of E control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: Receive FIFO load-to-unload delay. This field is initialized during FIFO initialization. It is modified thereafter by the deskew machine. For setting X, the latency is 4 x X to 4 x X + 4 UI. The default is 20 - 24 UI.
52:63	RO	constant = 0b000000000000

Register Name	Receive Bit Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL
Address	800308040601143F (SCOM)
Description	This register contains the second set of E control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: Receive FIFO load-to-unload delay. This field is initialized during FIFO initialization. It is modified thereafter by the deskew machine. For setting X, the latency is 4 x X to 4 x X + 4 UI. The default is 20 - 24 UI.
52:63	RO	constant = 0b000000000000

Register Name	Receive Bit Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL
Address	800308050601143F (SCOM)
Description	This register contains the second set of E control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: Receive FIFO load-to-unload delay. This field is initialized during FIFO initialization. It is modified thereafter by the deskew machine. For setting X, the latency is 4 x X to 4 x X + 4 UI. The default is 20 - 24 UI.
52:63	RO	constant = 0b000000000000

Register Name	Receive Bit Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL
Address	800308060601143F (SCOM)
Description	This register contains the second set of E control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: Receive FIFO load-to-unload delay. This field is initialized during FIFO initialization. It is modified thereafter by the deskew machine. For setting X, the latency is 4 x X to 4 x X + 4 UI. The default is 20 - 24 UI.
52:63	RO	constant = 0b000000000000

Register Name	Receive Bit Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL
Address	800308070601143F (SCOM)
Description	This register contains the second set of E control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: Receive FIFO load-to-unload delay. This field is initialized during FIFO initialization. It is modified thereafter by the deskew machine. For setting X, the latency is 4 x X to 4 x X + 4 UI. The default is 20 - 24 UI.
52:63	RO	constant = 0b000000000000

Register Name	Receive Bit Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL
Address	800308080601143F (SCOM)
Description	This register contains the second set of E control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: Receive FIFO load-to-unload delay. This field is initialized during FIFO initialization. It is modified thereafter by the deskew machine. For setting X, the latency is 4 x X to 4 x X + 4 UI. The default is 20 - 24 UI.
52:63	RO	constant = 0b000000000000

Register Name	Receive Bit Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL
Address	800308090601143F (SCOM)
Description	This register contains the second set of E control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RWX	RX_FIFO_L2U_DLY: Receive FIFO load-to-unload delay. This field is initialized during FIFO initialization. It is modified thereafter by the deskew machine. For setting X, the latency is 4 x X to 4 x X + 4 UI. The default is 20 - 24 UI.
52:63	RO	constant = 0b000000000000

Register Name	Receive Bit Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL
Address	8003080A0601143F (SCOM)
Description	This register contains the second set of E control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: Receive FIFO load-to-unload delay. This field is initialized during FIFO initialization. It is modified thereafter by the deskew machine. For setting X, the latency is 4 x X to 4 x X + 4 UI. The default is 20 - 24 UI.
52:63	RO	constant = 0b000000000000

Register Name	Receive Bit Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL
Address	8003080B0601143F (SCOM)
Description	This register contains the second set of E control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: Receive FIFO load-to-unload delay. This field is initialized during FIFO initialization. It is modified thereafter by the deskew machine. For setting X, the latency is 4 x X to 4 x X + 4 UI. The default is 20 - 24 UI.
52:63	RO	constant = 0b000000000000

Register Name	Receive Bit Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL
Address	8003080C0601143F (SCOM)
Description	This register contains the second set of E control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: Receive FIFO load-to-unload delay. This field is initialized during FIFO initialization. It is modified thereafter by the deskew machine. For setting X, the latency is 4 x X to 4 x X + 4 UI. The default is 20 - 24 UI.
52:63	RO	constant = 0b000000000000

Register Name	Receive Bit Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL
Address	8003080D0601143F (SCOM)
Description	This register contains the second set of E control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: Receive FIFO load-to-unload delay. This field is initialized during FIFO initialization. It is modified thereafter by the deskew machine. For setting X, the latency is 4 x X to 4 x X + 4 UI. The default is 20 - 24 UI.
52:63	RO	constant = 0b000000000000

Register Name	Receive Bit Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL
Address	8003080E0601143F (SCOM)
Description	This register contains the second set of E control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: Receive FIFO load-to-unload delay. This field is initialized during FIFO initialization. It is modified thereafter by the deskew machine. For setting X, the latency is 4 x X to 4 x X + 4 UI. The default is 20 - 24 UI.
52:63	RO	constant = 0b000000000000

Register Name	Receive Bit Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL
Address	8003080F0601143F (SCOM)
Description	This register contains the second set of E control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: Receive FIFO load-to-unload delay. This field is initialized during FIFO initialization. It is modified thereafter by the deskew machine. For setting X, the latency is 4 x X to 4 x X + 4 UI. The default is 20 - 24 UI.
52:63	RO	constant = 0b000000000000

Register Name	Receive Bit Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL
Address	800308100601143F (SCOM)
Description	This register contains the second set of E control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RWX	RX_FIFO_L2U_DLY: Receive FIFO load-to-unload delay. This field is initialized during FIFO initialization. It is modified thereafter by the deskew machine. For setting X, the latency is 4 x X to 4 x X + 4 UI. The default is 20 - 24 UI.
52:63	RO	constant = 0b000000000000

Register Name	Receive Bit Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL
Address	800308110601143F (SCOM)
Description	This register contains the second set of E control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: Receive FIFO load-to-unload delay. This field is initialized during FIFO initialization. It is modified thereafter by the deskew machine. For setting X, the latency is 4 x X to 4 x X + 4 UI. The default is 20 - 24 UI.
52:63	RO	constant = 0b000000000000

Register Name	Receive Bit Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL
Address	800308200601143F (SCOM)
Description	This register contains the second set of E control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: Receive FIFO load-to-unload delay. This field is initialized during FIFO initialization. It is modified thereafter by the deskew machine. For setting X, the latency is 4 x X to 4 x X + 4 UI. The default is 20 - 24 UI.
52:63	RO	constant = 0b000000000000

Register Name	Receive Bit Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL
Address	800308210601143F (SCOM)
Description	This register contains the second set of E control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: Receive FIFO load-to-unload delay. This field is initialized during FIFO initialization. It is modified thereafter by the deskew machine. For setting X, the latency is 4 x X to 4 x X + 4 UI. The default is 20 - 24 UI.
52:63	RO	constant = 0b000000000000

Register Name	Receive Bit Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL
Address	800308220601143F (SCOM)
Description	This register contains the second set of E control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: Receive FIFO load-to-unload delay. This field is initialized during FIFO initialization. It is modified thereafter by the deskew machine. For setting X, the latency is 4 x X to 4 x X + 4 UI. The default is 20 - 24 UI.
52:63	RO	constant = 0b000000000000

Register Name	Receive Bit Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL
Address	800308230601143F (SCOM)
Description	This register contains the second set of E control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: Receive FIFO load-to-unload delay. This field is initialized during FIFO initialization. It is modified thereafter by the deskew machine. For setting X, the latency is 4 x X to 4 x X + 4 UI. The default is 20 - 24 UI.
52:63	RO	constant = 0b000000000000

Register Name	Receive Bit Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL
Address	800308240601143F (SCOM)
Description	This register contains the second set of E control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: Receive FIFO load-to-unload delay. This field is initialized during FIFO initialization. It is modified thereafter by the deskew machine. For setting X, the latency is 4 x X to 4 x X + 4 UI. The default is 20 - 24 UI.
52:63	RO	constant = 0b000000000000

Register Name	Receive Bit Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL
Address	800308250601143F (SCOM)
Description	This register contains the second set of E control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RWX	RX_FIFO_L2U_DLY: Receive FIFO load-to-unload delay. This field is initialized during FIFO initialization. It is modified thereafter by the deskew machine. For setting X, the latency is 4 x X to 4 x X + 4 UI. The default is 20 - 24 UI.
52:63	RO	constant = 0b000000000000

Register Name	Receive Bit Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL
Address	800308260601143F (SCOM)
Description	This register contains the second set of E control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: Receive FIFO load-to-unload delay. This field is initialized during FIFO initialization. It is modified thereafter by the deskew machine. For setting X, the latency is 4 x X to 4 x X + 4 UI. The default is 20 - 24 UI.
52:63	RO	constant = 0b000000000000

Register Name	Receive Bit Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL
Address	800308270601143F (SCOM)
Description	This register contains the second set of E control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: Receive FIFO load-to-unload delay. This field is initialized during FIFO initialization. It is modified thereafter by the deskew machine. For setting X, the latency is 4 x X to 4 x X + 4 UI. The default is 20 - 24 UI.
52:63	RO	constant = 0b000000000000

Register Name	Receive Bit Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL
Address	800308280601143F (SCOM)
Description	This register contains the second set of E control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: Receive FIFO load-to-unload delay. This field is initialized during FIFO initialization. It is modified thereafter by the deskew machine. For setting X, the latency is 4 x X to 4 x X + 4 UI. The default is 20 - 24 UI.
52:63	RO	constant = 0b000000000000

Register Name	Receive Bit Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL
Address	800308290601143F (SCOM)
Description	This register contains the second set of E control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: Receive FIFO load-to-unload delay. This field is initialized during FIFO initialization. It is modified thereafter by the deskew machine. For setting X, the latency is 4 x X to 4 x X + 4 UI. The default is 20 - 24 UI.
52:63	RO	constant = 0b000000000000

Register Name	Receive Bit Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL
Address	8003082A0601143F (SCOM)
Description	This register contains the second set of E control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: Receive FIFO load-to-unload delay. This field is initialized during FIFO initialization. It is modified thereafter by the deskew machine. For setting X, the latency is 4 x X to 4 x X + 4 UI. The default is 20 - 24 UI.
52:63	RO	constant = 0b000000000000

Register Name	Receive Bit Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL
Address	8003082B0601143F (SCOM)
Description	This register contains the second set of E control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: Receive FIFO load-to-unload delay. This field is initialized during FIFO initialization. It is modified thereafter by the deskew machine. For setting X, the latency is 4 x X to 4 x X + 4 UI. The default is 20 - 24 UI.
52:63	RO	constant = 0b000000000000

Register Name	Receive Bit Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL
Address	8003082C0601143F (SCOM)
Description	This register contains the second set of E control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RWX	RX_FIFO_L2U_DLY: Receive FIFO load-to-unload delay. This field is initialized during FIFO initialization. It is modified thereafter by the deskew machine. For setting X, the latency is 4 x X to 4 x X + 4 UI. The default is 20 - 24 UI.
52:63	RO	constant = 0b000000000000

Register Name	Receive Bit Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL
Address	8003082D0601143F (SCOM)
Description	This register contains the second set of E control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: Receive FIFO load-to-unload delay. This field is initialized during FIFO initialization. It is modified thereafter by the deskew machine. For setting X, the latency is 4 x X to 4 x X + 4 UI. The default is 20 - 24 UI.
52:63	RO	constant = 0b000000000000

Register Name	Receive Bit Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL
Address	8003082E0601143F (SCOM)
Description	This register contains the second set of E control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: Receive FIFO load-to-unload delay. This field is initialized during FIFO initialization. It is modified thereafter by the deskew machine. For setting X, the latency is 4 x X to 4 x X + 4 UI. The default is 20 - 24 UI.
52:63	RO	constant = 0b000000000000

Register Name	Receive Bit Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL
Address	8003082F0601143F (SCOM)
Description	This register contains the second set of E control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: Receive FIFO load-to-unload delay. This field is initialized during FIFO initialization. It is modified thereafter by the deskew machine. For setting X, the latency is 4 x X to 4 x X + 4 UI. The default is 20 - 24 UI.
52:63	RO	constant = 0b000000000000

Register Name	Receive Bit Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL
Address	800308300601143F (SCOM)
Description	This register contains the second set of E control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: Receive FIFO load-to-unload delay. This field is initialized during FIFO initialization. It is modified thereafter by the deskew machine. For setting X, the latency is 4 x X to 4 x X + 4 UI. The default is 20 - 24 UI.
52:63	RO	constant = 0b000000000000

Register Name	Receive Bit Control 2 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_E_PL
Address	800308310601143F (SCOM)
Description	This register contains the second set of E control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: Receive FIFO load-to-unload delay. This field is initialized during FIFO initialization. It is modified thereafter by the deskew machine. For setting X, the latency is 4 x X to 4 x X + 4 UI. The default is 20 - 24 UI.
52:63	RO	constant = 0b000000000000

Register Name	Receive Bit Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL
Address	800310000601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54:55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL
Address	800310010601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54:55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL
Address	800310020601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54:55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL
Address	800310030601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54:55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL
Address	800310040601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54:55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL
Address	800310050601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54:55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL
Address	800310060601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54:55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL
Address	800310070601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
53	NCX	Reserved field.
54:55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL
Address	800310080601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54:55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL
Address	800310090601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54:55	NCX	Reserved field.
56	NCX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
57	NCX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL
Address	8003100A0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54:55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL
Address	8003100B0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54:55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL
Address	8003100C0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54:55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL
Address	8003100D0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54:55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL
Address	8003100E0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54:55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL
Address	8003100F0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54:55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL
Address	800310100601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54:55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL
Address	800310110601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54:55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL
Address	800310200601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
53	NCX	Reserved field.
54:55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL
Address	800310210601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54:55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL
Address	800310220601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54:55	NCX	Reserved field.
56	NCX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
57	NCX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL
Address	800310230601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54:55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL
Address	800310240601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54:55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	**Receive Bit Control 3 E Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL
Address	800310250601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54:55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	**Receive Bit Control 3 E Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL
Address	800310260601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54:55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	**Receive Bit Control 3 E Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL
Address	800310270601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54:55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	**Receive Bit Control 3 E Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL
Address	800310280601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54:55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	**Receive Bit Control 3 E Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL
Address	800310290601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54:55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	**Receive Bit Control 3 E Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL
Address	8003102A0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54:55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	**Receive Bit Control 3 E Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL
Address	8003102B0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
53	NCX	Reserved field.
54:55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL
Address	8003102C0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54:55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Bit Control 3 E Per-Lane Register
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL
Address	8003102D0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54:55	NCX	Reserved field.
56	NCX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
57	NCX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	**Receive Bit Control 3 E Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL
Address	8003102E0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54:55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	**Receive Bit Control 3 E Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#4.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL
Address	8003102F0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54:55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	**Receive Bit Control 3 E Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#3.RXPACK.RD.SLICE#5.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL
Address	800310300601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54:55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	**Receive Bit Control 3 E Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL3_E_PL
Address	800310310601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54:55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#16.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	800380000601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#17.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	800380010601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#13.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	800380020601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Data Work Spare Mode Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#15.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	800380030601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Data Work Spare Mode Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#12.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	800380040601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#14.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	800380050601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#10.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	800380060601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#8.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	800380070601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#11.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	800380080601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#5.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	800380090601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#7.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	8003800A0601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#4.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	8003800B0601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#6.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	8003800C0601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#0.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	8003800D0601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#2.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	8003800E0601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#1.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	8003800F0601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#3.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	800380100601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#9.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	800380110601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Data Work Spare Mode Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#18.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	800380120601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Data Work Spare Mode Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#19.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	800380130601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Data Work Spare Mode Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#20.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	800380140601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Data Work Spare Mode Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#21.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	800380150601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Data Work Spare Mode Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#22.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	800380160601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#23.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	800380170601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#2.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	800380200601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#0.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	800380210601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#3.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	800380220601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#1.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	800380230601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#7.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	800380240601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#5.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	800380250601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Data Work Spare Mode Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#6.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	800380260601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Data Work Spare Mode Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#4.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	800380270601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#8.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	800380280601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#10.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	800380290601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#9.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	8003802A0601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#15.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	8003802B0601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Data Work Spare Mode Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#13.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	8003802C0601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Data Work Spare Mode Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#14.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	8003802D0601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Data Work Spare Mode Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#12.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	8003802E0601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#16.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	8003802F0601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#17.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	800380300601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#11.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	800380310601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#18.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	800380320601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#19.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	800380330601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#20.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	800380340601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#21.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	800380350601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#22.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	800380360601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#23.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	800380370601143F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#16.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	800388000601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.

Bits	SCOM	Field Mnemonic: Description
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#17.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	800388010601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#13.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	800388020601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#15.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	800388030601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.

Bits	SCOM	Field Mnemonic: Description
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#12.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	800388040601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#14.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	800388050601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	**Receive Work STAT1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#10.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	800388060601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#8.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	800388070601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	**Receive Work STAT1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#11.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	800388080601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#5.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	800388090601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#7.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	8003880A0601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#4.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	8003880B0601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	**Receive Work STAT1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#6.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	8003880C0601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#0.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	8003880D0601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	**Receive Work STAT1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#2.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	8003880E0601143F (SCOM)
Description	This register contains status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#1.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	8003880F0601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#3.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	800388100601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#9.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	800388110601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#18.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	800388120601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	**Receive Work STAT1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#19.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	800388130601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#20.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	800388140601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#21.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	800388150601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#22.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	800388160601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	**Receive Work STAT1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#23.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	800388170601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	**Receive Work STAT1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#2.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	800388200601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#0.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	800388210601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#3.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	800388220601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	**Receive Work STAT1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#1.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	800388230601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#7.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	800388240601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#5.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	800388250601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	**Receive Work STAT1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#6.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	800388260601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#4.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	800388270601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#8.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	800388280601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#10.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	800388290601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#9.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	8003882A0601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#15.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	8003882B0601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	**Receive Work STAT1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#13.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	8003882C0601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#14.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	8003882D0601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#12.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	8003882E0601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#16.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	8003882F0601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#17.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	800388300601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#11.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	800388310601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	**Receive Work STAT1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#18.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	800388320601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#19.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	800388330601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#20.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	800388340601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	**Receive Work STAT1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#21.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	800388350601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	**Receive Work STAT1 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#22.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	800388360601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#23.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	800388370601143F (SCOM)
Description	This register contains the first set of EO status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: The eye-optimization step failed the BER test. The lane is marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: The eye-optimization step failed the width test. The lane is marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: The eye-optimization step failed the height test. The lane is marked bad.
51	RO	constant = 0b0
52	RWX	RX_WT_LANE_DISABLED: The wire test disabled this lane.
53	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_WT_LANE_BAD_CODE: Wire test lane bad code. Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: \n0000 = GOOD LANE; not inverted (EDI and EI-4). \n0001 = BAD LANE; N leg stuck at 1; not inverted (EDI-only). \n0010 = BAD LANE; N leg stuck at 0; not inverted (EDI-only). \n0011 = BAD LANE; P leg stuck at 1; not inverted (EDI-only). \n0100 = BAD LANE; P leg stuck at 0; not inverted (EDI-only). \n0101 = BAD LANE; N/(P) leg floating if (NOT) inverted (EDI-only). \n0110 = BAD LANE; P/(N) leg floating if (NOT) inverted (EDI-only). \n0111 = BAD LANE; P and N legs stuck at same value, 0 or 1 (EDI only). \n1000 = GOOD LANE; inverted (EDI and EI-4). \n1001 = BAD LANE; N leg stuck at 1; inverted (EDI only). \n1010 = BAD LANE; N leg stuck at 0; inverted (EDI only). \n1011 = BAD LANE; P leg stuck at 1; inverted (EDI only). \n1100 = BAD LANE; P leg stuck at 0; inverted (EDI only). \n1101 = BAD LANE; P leg stuck at 0; N leg stuck at 1 (EDI and EI-4). \n1110 = BAD LANE; P leg stuck at 1; N leg stuck at 0 (EDI and EI-4). \n1111 = BAD LANE; Unknown reason; inversion undetermined (EDI and EI-4).
57	RWX	RX_BAD_BLOCK_LOCK: The deskew step block lock was not established. The lane is marked bad.
58	RWX	RX_BAD_SKEW: The deskew step skew value was not detected. The lane is marked bad.
59	RWX	RX_BAD_DESKEW: This bit contains the deskew step deskew value.
60:62	RO	constant = 0b000
63	RWX	RX_BIST_ERR: This bit indicates that RXBIST did not find two data eyes of sufficient width. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#16.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	800390000601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#17.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	800390010601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#13.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	800390020601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#15.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	800390030601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#12.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	800390040601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#14.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	800390050601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#10.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	800390060601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.

Bits	SCOM	Field Mnemonic: Description
49	RO	constant = 0b0
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#8.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	800390070601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#11.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	800390080601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#5.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	800390090601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#7.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	8003900A0601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#4.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	8003900B0601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	**Receive Work STAT2 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#6.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	8003900C0601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	**Receive Work STAT2 EO Per-Lane Register**
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#0.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	8003900D0601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#2.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	8003900E0601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#1.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	8003900F0601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#3.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	800390100601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#9.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	800390110601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#18.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	800390120601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#19.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	800390130601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#20.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	800390140601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#21.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	800390150601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#22.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	800390160601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#23.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	800390170601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#2.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	800390200601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#0.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	800390210601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#3.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	800390220601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#1.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	800390230601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#7.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	800390240601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#5.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	800390250601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#6.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	800390260601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#4.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	800390270601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#8.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	800390280601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#10.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	800390290601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#9.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	8003902A0601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#15.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	8003902B0601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#13.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	8003902C0601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#14.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	8003902D0601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#12.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	8003902E0601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#16.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	8003902F0601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#17.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	800390300601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#11.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	800390310601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#18.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	800390320601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#19.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	800390330601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#20.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	800390340601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#21.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	800390350601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#22.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	800390360601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#23.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	800390370601143F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RO	constant = 0b0
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RO	constant = 0b0
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#16.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	800398000601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#17.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	800398010601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#13.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	800398020601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#15.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	800398030601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#12.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	800398040601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#14.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	800398050601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#10.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	800398060601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#8.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	800398070601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#11.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	800398080601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#5.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	800398090601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#7.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	8003980A0601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#4.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	8003980B0601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#6.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	8003980C0601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#0.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	8003980D0601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#2.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	8003980E0601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#1.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	8003980F0601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#3.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	800398100601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#9.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	800398110601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#18.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	800398120601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#19.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	800398130601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#20.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	800398140601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#21.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	800398150601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#22.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	800398160601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX0.RX_WORK_REGS_MAC.SLICE#23.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	800398170601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#2.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	800398200601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#0.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	800398210601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#3.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	800398220601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#1.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	800398230601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#7.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	800398240601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#5.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	800398250601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#6.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	800398260601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#4.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	800398270601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#8.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	800398280601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#10.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	800398290601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#9.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	8003982A0601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#15.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	8003982B0601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#13.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	8003982C0601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#14.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	8003982D0601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#12.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	8003982E0601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#16.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	8003982F0601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#17.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	800398300601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#11.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	800398310601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#18.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	800398320601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#19.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	800398330601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#20.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	800398340601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#21.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	800398350601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#22.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	800398360601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOF2.RX.RX1.RX_WORK_REGS_MAC.SLICE#23.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	800398370601143F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_MODE1_PL
Address	800404000601143F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the transmit scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57	RWX	TX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
58:59	RO	constant = 0b00
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_MODE1_PL
Address	800404010601143F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the transmit scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57	RWX	TX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
58:59	RO	constant = 0b00
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_MODE1_PL
Address	800404020601143F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the transmit scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57	RWX	TX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
58:59	RO	constant = 0b00
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	**Transmit Mode 1 Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_MODE1_PL
Address	800404030601143F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.

Bits	SCOM	Field Mnemonic: Description
50:51	RWX	TX_LANE_QUIESCE: This field is This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the transmit scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57	RWX	TX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
58:59	RO	constant = 0b00
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#1.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_MODE1_PL
Address	800404040601143F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the transmit scrambler on a specific lane or all lanes by using a per-lane/per-group global write.

Bits	SCOM	Field Mnemonic: Description
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57	RWX	TX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
58:59	RO	constant = 0b00
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#1.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_MODE1_PL
Address	800404050601143F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the transmit scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57	RWX	TX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
58:59	RO	constant = 0b00
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#1.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_MODE1_PL
Address	800404060601143F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the transmit scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57	RWX	TX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
58:59	RO	constant = 0b00
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#1.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_MODE1_PL
Address	800404070601143F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the transmit scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57	RWX	TX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
58:59	RO	constant = 0b00
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	**Transmit Mode 1 Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#2.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_MODE1_PL
Address	800404080601143F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.

Bits	SCOM	Field Mnemonic: Description
50:51	RWX	TX_LANE_QUIESCE: This field is This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the transmit scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57	RWX	TX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
58:59	RO	constant = 0b00
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#2.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_MODE1_PL
Address	800404090601143F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the transmit scrambler on a specific lane or all lanes by using a per-lane/per-group global write.

Bits	SCOM	Field Mnemonic: Description
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57	RWX	TX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
58:59	RO	constant = 0b00
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	**Transmit Mode 1 Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#2.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_MODE1_PL
Address	8004040A0601143F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the transmit scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57	RWX	TX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
58:59	RO	constant = 0b00
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#2.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_MODE1_PL
Address	8004040B0601143F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the transmit scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57	RWX	TX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
58:59	RO	constant = 0b00
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_MODE1_PL
Address	8004040C0601143F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the transmit scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57	RWX	TX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
58:59	RO	constant = 0b00
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	**Transmit Mode 1 Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_MODE1_PL
Address	8004040D0601143F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.

Bits	SCOM	Field Mnemonic: Description
50:51	RWX	TX_LANE_QUIESCE: This field is This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the transmit scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57	RWX	TX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
58:59	RO	constant = 0b00
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_MODE1_PL
Address	8004040E0601143F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the transmit scrambler on a specific lane or all lanes by using a per-lane/per-group global write.

Bits	SCOM	Field Mnemonic: Description
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57	RWX	TX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
58:59	RO	constant = 0b00
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_MODE1_PL
Address	8004040F0601143F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the transmit scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57	RWX	TX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
58:59	RO	constant = 0b00
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#4.DD.TX_BIT_REGS.TX_MODE1_PL
Address	800404100601143F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the transmit scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57	RWX	TX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
58:59	RO	constant = 0b00
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#0.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_MODE1_PL
Address	800404200601143F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the transmit scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57	RWX	TX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
58:59	RO	constant = 0b00
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#0.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_MODE1_PL
Address	800404210601143F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.

Bits	SCOM	Field Mnemonic: Description
50:51	RWX	TX_LANE_QUIESCE: This field is This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the transmit scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57	RWX	TX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
58:59	RO	constant = 0b00
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#0.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_MODE1_PL
Address	800404220601143F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the transmit scrambler on a specific lane or all lanes by using a per-lane/per-group global write.

Bits	SCOM	Field Mnemonic: Description
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57	RWX	TX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
58:59	RO	constant = 0b00
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	**Transmit Mode 1 Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#0.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_MODE1_PL
Address	800404230601143F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the transmit scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57	RWX	TX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
58:59	RO	constant = 0b00
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#1.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_MODE1_PL
Address	800404240601143F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the transmit scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57	RWX	TX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
58:59	RO	constant = 0b00
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#1.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_MODE1_PL
Address	800404250601143F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the transmit scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57	RWX	TX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
58:59	RO	constant = 0b00
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	**Transmit Mode 1 Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#1.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_MODE1_PL
Address	800404260601143F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.

Bits	SCOM	Field Mnemonic: Description
50:51	RWX	TX_LANE_QUIESCE: This field is This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the transmit scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57	RWX	TX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
58:59	RO	constant = 0b00
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#1.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_MODE1_PL
Address	800404270601143F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the transmit scrambler on a specific lane or all lanes by using a per-lane/per-group global write.

Bits	SCOM	Field Mnemonic: Description
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57	RWX	TX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
58:59	RO	constant = 0b00
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_MODE1_PL
Address	800404280601143F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the transmit scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57	RWX	TX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
58:59	RO	constant = 0b00
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_MODE1_PL
Address	800404290601143F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the transmit scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57	RWX	TX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
58:59	RO	constant = 0b00
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_MODE1_PL
Address	8004042A0601143F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the transmit scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57	RWX	TX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
58:59	RO	constant = 0b00
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_MODE1_PL
Address	8004042B0601143F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.

Bits	SCOM	Field Mnemonic: Description
50:51	RWX	TX_LANE_QUIESCE: This field is This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the transmit scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57	RWX	TX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
58:59	RO	constant = 0b00
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_MODE1_PL
Address	8004042C0601143F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the transmit scrambler on a specific lane or all lanes by using a per-lane/per-group global write.

Bits	SCOM	Field Mnemonic: Description
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57	RWX	TX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
58:59	RO	constant = 0b00
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_MODE1_PL
Address	8004042D0601143F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the transmit scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57	RWX	TX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
58:59	RO	constant = 0b00
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_MODE1_PL
Address	8004042E0601143F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the transmit scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57	RWX	TX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
58:59	RO	constant = 0b00
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_MODE1_PL
Address	8004042F0601143F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the transmit scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57	RWX	TX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
58:59	RO	constant = 0b00
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#4.DD.TX_BIT_REGS.TX_MODE1_PL
Address	800404300601143F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.

Bits	SCOM	Field Mnemonic: Description
50:51	RWX	TX_LANE_QUIESCE: This field is This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_LANE_SCRAMBLE_DISABLE: This bit is used to disable the transmit scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57	RWX	TX_PSAVE_MODE_DISABLE: This bit disables psave mode for this physical lane.
58:59	RO	constant = 0b00
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C000601143F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:52	RO	constant = 0b00
53	RWX	TX_NEXT_CAL_LANE_SEL: When set, this bit negates the action of tx_pdwn_lite in a similar way to tx_cal_lane_sel. This enables the driver ahead of SLS shadowing.
54:55	RW	TX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by TX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.

Bits	SCOM	Field Mnemonic: Description
57	RO	constant = 0b0
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61	RWX	TX_PDWN_LITE: When set, this bit gates the TX data path (post FIFO) to zeros on unused spare lanes when not being recalibrated.
62	RWX	TX_CAL_LANE_SEL: SLS commands and recalibration.
63	RWX	TX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the transmit FIFO for slower frequency connections.

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C010601143F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:52	RO	constant = 0b00
53	RWX	TX_NEXT_CAL_LANE_SEL: When set, this bit negates the action of tx_pdwn_lite in a similar way to tx_cal_lane_sel. This enables the driver ahead of SLS shadowing.
54:55	RW	TX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by TX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RO	constant = 0b0
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61	RWX	TX_PDWN_LITE: When set, this bit gates the TX data path (post FIFO) to zeros on unused spare lanes when not being recalibrated.
62	RWX	TX_CAL_LANE_SEL: SLS commands and recalibration.
63	RWX	TX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the transmit FIFO for slower frequency connections.

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C020601143F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:52	RO	constant = 0b00
53	RWX	TX_NEXT_CAL_LANE_SEL: When set, this bit negates the action of tx_pdwn_lite in a similar way to tx_cal_lane_sel. This enables the driver ahead of SLS shadowing.
54:55	RW	TX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by TX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RO	constant = 0b0
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61	RWX	TX_PDWN_LITE: When set, this bit gates the TX data path (post FIFO) to zeros on unused spare lanes when not being recalibrated.
62	RWX	TX_CAL_LANE_SEL: SLS commands and recalibration.
63	RWX	TX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the transmit FIFO for slower frequency connections.

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C030601143F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:52	RO	constant = 0b00
53	RWX	TX_NEXT_CAL_LANE_SEL: When set, this bit negates the action of tx_pdwn_lite in a similar way to tx_cal_lane_sel. This enables the driver ahead of SLS shadowing.
54:55	RW	TX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by TX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RO	constant = 0b0
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61	RWX	TX_PDWN_LITE: When set, this bit gates the TX data path (post FIFO) to zeros on unused spare lanes when not being recalibrated.
62	RWX	TX_CAL_LANE_SEL: SLS commands and recalibration.
63	RWX	TX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the transmit FIFO for slower frequency connections.

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#1.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C040601143F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:52	RO	constant = 0b00
53	RWX	TX_NEXT_CAL_LANE_SEL: When set, this bit negates the action of tx_pdwn_lite in a similar way to tx_cal_lane_sel. This enables the driver ahead of SLS shadowing.

Bits	SCOM	Field Mnemonic: Description
54:55	RW	TX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by TX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RO	constant = 0b0
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61	RWX	TX_PDWN_LITE: When set, this bit gates the TX data path (post FIFO) to zeros on unused spare lanes when not being recalibrated.
62	RWX	TX_CAL_LANE_SEL: SLS commands and recalibration.
63	RWX	TX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the transmit FIFO for slower frequency connections.

Register Name	**Transmit Mode 2 Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#1.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C050601143F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:52	RO	constant = 0b00
53	RWX	TX_NEXT_CAL_LANE_SEL: When set, this bit negates the action of tx_pdwn_lite in a similar way to tx_cal_lane_sel. This enables the driver ahead of SLS shadowing.
54:55	RW	TX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by TX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RO	constant = 0b0
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61	RWX	TX_PDWN_LITE: When set, this bit gates the TX data path (post FIFO) to zeros on unused spare lanes when not being recalibrated.
62	RWX	TX_CAL_LANE_SEL: SLS commands and recalibration.

Bits	SCOM	Field Mnemonic: Description
63	RWX	TX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the transmit FIFO for slower frequency connections.

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#1.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C060601143F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:52	RO	constant = 0b00
53	RWX	TX_NEXT_CAL_LANE_SEL: When set, this bit negates the action of tx_pdwn_lite in a similar way to tx_cal_lane_sel. This enables the driver ahead of SLS shadowing.
54:55	RW	TX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by TX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RO	constant = 0b0
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61	RWX	TX_PDWN_LITE: When set, this bit gates the TX data path (post FIFO) to zeros on unused spare lanes when not being recalibrated.
62	RWX	TX_CAL_LANE_SEL: SLS commands and recalibration.
63	RWX	TX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the transmit FIFO for slower frequency connections.

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#1.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C070601143F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:52	RO	constant = 0b00
53	RWX	TX_NEXT_CAL_LANE_SEL: When set, this bit negates the action of tx_pdwn_lite in a similar way to tx_cal_lane_sel. This enables the driver ahead of SLS shadowing.
54:55	RW	TX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by TX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RO	constant = 0b0
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61	RWX	TX_PDWN_LITE: When set, this bit gates the TX data path (post FIFO) to zeros on unused spare lanes when not being recalibrated.
62	RWX	TX_CAL_LANE_SEL: SLS commands and recalibration.
63	RWX	TX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the transmit FIFO for slower frequency connections.

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#2.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C080601143F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:52	RO	constant = 0b00
53	RWX	TX_NEXT_CAL_LANE_SEL: When set, this bit negates the action of tx_pdwn_lite in a similar way to tx_cal_lane_sel. This enables the driver ahead of SLS shadowing.

Bits	SCOM	Field Mnemonic: Description
54:55	RW	TX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by TX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RO	constant = 0b0
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61	RWX	TX_PDWN_LITE: When set, this bit gates the TX data path (post FIFO) to zeros on unused spare lanes when not being recalibrated.
62	RWX	TX_CAL_LANE_SEL: SLS commands and recalibration.
63	RWX	TX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the transmit FIFO for slower frequency connections.

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#2.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C090601143F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:52	RO	constant = 0b00
53	RWX	TX_NEXT_CAL_LANE_SEL: When set, this bit negates the action of tx_pdwn_lite in a similar way to tx_cal_lane_sel. This enables the driver ahead of SLS shadowing.
54:55	RW	TX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by TX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RO	constant = 0b0
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61	RWX	TX_PDWN_LITE: When set, this bit gates the TX data path (post FIFO) to zeros on unused spare lanes when not being recalibrated.
62	RWX	TX_CAL_LANE_SEL: SLS commands and recalibration.

Bits	SCOM	Field Mnemonic: Description
63	RWX	TX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the transmit FIFO for slower frequency connections.

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#2.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C0A0601143F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:52	RO	constant = 0b00
53	RWX	TX_NEXT_CAL_LANE_SEL: When set, this bit negates the action of tx_pdwn_lite in a similar way to tx_cal_lane_sel. This enables the driver ahead of SLS shadowing.
54:55	RW	TX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by TX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RO	constant = 0b0
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61	RWX	TX_PDWN_LITE: When set, this bit gates the TX data path (post FIFO) to zeros on unused spare lanes when not being recalibrated.
62	RWX	TX_CAL_LANE_SEL: SLS commands and recalibration.
63	RWX	TX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the transmit FIFO for slower frequency connections.

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#2.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C0B0601143F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:52	RO	constant = 0b00
53	RWX	TX_NEXT_CAL_LANE_SEL: When set, this bit negates the action of tx_pdwn_lite in a similar way to tx_cal_lane_sel. This enables the driver ahead of SLS shadowing.
54:55	RW	TX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by TX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RO	constant = 0b0
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61	RWX	TX_PDWN_LITE: When set, this bit gates the TX data path (post FIFO) to zeros on unused spare lanes when not being recalibrated.
62	RWX	TX_CAL_LANE_SEL: SLS commands and recalibration.
63	RWX	TX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the transmit FIFO for slower frequency connections.

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C0C0601143F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:52	RO	constant = 0b00
53	RWX	TX_NEXT_CAL_LANE_SEL: When set, this bit negates the action of tx_pdwn_lite in a similar way to tx_cal_lane_sel. This enables the driver ahead of SLS shadowing.

Bits	SCOM	Field Mnemonic: Description
54:55	RW	TX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by TX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RO	constant = 0b0
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61	RWX	TX_PDWN_LITE: When set, this bit gates the TX data path (post FIFO) to zeros on unused spare lanes when not being recalibrated.
62	RWX	TX_CAL_LANE_SEL: SLS commands and recalibration.
63	RWX	TX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the transmit FIFO for slower frequency connections.

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C0D0601143F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:52	RO	constant = 0b00
53	RWX	TX_NEXT_CAL_LANE_SEL: When set, this bit negates the action of tx_pdwn_lite in a similar way to tx_cal_lane_sel. This enables the driver ahead of SLS shadowing.
54:55	RW	TX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by TX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RO	constant = 0b0
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61	RWX	TX_PDWN_LITE: When set, this bit gates the TX data path (post FIFO) to zeros on unused spare lanes when not being recalibrated.
62	RWX	TX_CAL_LANE_SEL: SLS commands and recalibration.

Bits	SCOM	Field Mnemonic: Description
63	RWX	TX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the transmit FIFO for slower frequency connections.

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C0E0601143F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:52	RO	constant = 0b00
53	RWX	TX_NEXT_CAL_LANE_SEL: When set, this bit negates the action of tx_pdwn_lite in a similar way to tx_cal_lane_sel. This enables the driver ahead of SLS shadowing.
54:55	RW	TX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by TX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RO	constant = 0b0
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61	RWX	TX_PDWN_LITE: When set, this bit gates the TX data path (post FIFO) to zeros on unused spare lanes when not being recalibrated.
62	RWX	TX_CAL_LANE_SEL: SLS commands and recalibration.
63	RWX	TX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the transmit FIFO for slower frequency connections.

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C0F0601143F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:52	RO	constant = 0b00
53	RWX	TX_NEXT_CAL_LANE_SEL: When set, this bit negates the action of tx_pdwn_lite in a similar way to tx_cal_lane_sel. This enables the driver ahead of SLS shadowing.
54:55	RW	TX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by TX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RO	constant = 0b0
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61	RWX	TX_PDWN_LITE: When set, this bit gates the TX data path (post FIFO) to zeros on unused spare lanes when not being recalibrated.
62	RWX	TX_CAL_LANE_SEL: SLS commands and recalibration.
63	RWX	TX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the transmit FIFO for slower frequency connections.

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#4.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C100601143F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:52	RO	constant = 0b00
53	RWX	TX_NEXT_CAL_LANE_SEL: When set, this bit negates the action of tx_pdwn_lite in a similar way to tx_cal_lane_sel. This enables the driver ahead of SLS shadowing.

Bits	SCOM	Field Mnemonic: Description
54:55	RW	TX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by TX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RO	constant = 0b0
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61	RWX	TX_PDWN_LITE: When set, this bit gates the TX data path (post FIFO) to zeros on unused spare lanes when not being recalibrated.
62	RWX	TX_CAL_LANE_SEL: SLS commands and recalibration.
63	RWX	TX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the transmit FIFO for slower frequency connections.

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#0.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C200601143F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:52	RO	constant = 0b00
53	RWX	TX_NEXT_CAL_LANE_SEL: When set, this bit negates the action of tx_pdwn_lite in a similar way to tx_cal_lane_sel. This enables the driver ahead of SLS shadowing.
54:55	RW	TX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by TX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RO	constant = 0b0
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61	RWX	TX_PDWN_LITE: When set, this bit gates the TX data path (post FIFO) to zeros on unused spare lanes when not being recalibrated.
62	RWX	TX_CAL_LANE_SEL: SLS commands and recalibration.

Bits	SCOM	Field Mnemonic: Description
63	RWX	TX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the transmit FIFO for slower frequency connections.

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#0.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C210601143F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:52	RO	constant = 0b00
53	RWX	TX_NEXT_CAL_LANE_SEL: When set, this bit negates the action of tx_pdwn_lite in a similar way to tx_cal_lane_sel. This enables the driver ahead of SLS shadowing.
54:55	RW	TX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by TX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RO	constant = 0b0
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61	RWX	TX_PDWN_LITE: When set, this bit gates the TX data path (post FIFO) to zeros on unused spare lanes when not being recalibrated.
62	RWX	TX_CAL_LANE_SEL: SLS commands and recalibration.
63	RWX	TX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the transmit FIFO for slower frequency connections.

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#0.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C220601143F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:52	RO	constant = 0b00
53	RWX	TX_NEXT_CAL_LANE_SEL: When set, this bit negates the action of tx_pdwn_lite in a similar way to tx_cal_lane_sel. This enables the driver ahead of SLS shadowing.
54:55	RW	TX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by TX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RO	constant = 0b0
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61	RWX	TX_PDWN_LITE: When set, this bit gates the TX data path (post FIFO) to zeros on unused spare lanes when not being recalibrated.
62	RWX	TX_CAL_LANE_SEL: SLS commands and recalibration.
63	RWX	TX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the transmit FIFO for slower frequency connections.

Register Name	**Transmit Mode 2 Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#0.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C230601143F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:52	RO	constant = 0b00
53	RWX	TX_NEXT_CAL_LANE_SEL: When set, this bit negates the action of tx_pdwn_lite in a similar way to tx_cal_lane_sel. This enables the driver ahead of SLS shadowing.

Bits	SCOM	Field Mnemonic: Description
54:55	RW	TX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by TX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RO	constant = 0b0
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61	RWX	TX_PDWN_LITE: When set, this bit gates the TX data path (post FIFO) to zeros on unused spare lanes when not being recalibrated.
62	RWX	TX_CAL_LANE_SEL: SLS commands and recalibration.
63	RWX	TX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the transmit FIFO for slower frequency connections.

Register Name	**Transmit Mode 2 Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#1.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C240601143F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:52	RO	constant = 0b00
53	RWX	TX_NEXT_CAL_LANE_SEL: When set, this bit negates the action of tx_pdwn_lite in a similar way to tx_cal_lane_sel. This enables the driver ahead of SLS shadowing.
54:55	RW	TX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by TX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RO	constant = 0b0
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61	RWX	TX_PDWN_LITE: When set, this bit gates the TX data path (post FIFO) to zeros on unused spare lanes when not being recalibrated.
62	RWX	TX_CAL_LANE_SEL: SLS commands and recalibration.

Bits	SCOM	Field Mnemonic: Description
63	RWX	TX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the transmit FIFO for slower frequency connections.

Register Name	**Transmit Mode 2 Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#1.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C250601143F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:52	RO	constant = 0b00
53	RWX	TX_NEXT_CAL_LANE_SEL: When set, this bit negates the action of tx_pdwn_lite in a similar way to tx_cal_lane_sel. This enables the driver ahead of SLS shadowing.
54:55	RW	TX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by TX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RO	constant = 0b0
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61	RWX	TX_PDWN_LITE: When set, this bit gates the TX data path (post FIFO) to zeros on unused spare lanes when not being recalibrated.
62	RWX	TX_CAL_LANE_SEL: SLS commands and recalibration.
63	RWX	TX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the transmit FIFO for slower frequency connections.

Register Name	**Transmit Mode 2 Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#1.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C260601143F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:52	RO	constant = 0b00
53	RWX	TX_NEXT_CAL_LANE_SEL: When set, this bit negates the action of tx_pdwn_lite in a similar way to tx_cal_lane_sel. This enables the driver ahead of SLS shadowing.
54:55	RW	TX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by TX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RO	constant = 0b0
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61	RWX	TX_PDWN_LITE: When set, this bit gates the TX data path (post FIFO) to zeros on unused spare lanes when not being recalibrated.
62	RWX	TX_CAL_LANE_SEL: SLS commands and recalibration.
63	RWX	TX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the transmit FIFO for slower frequency connections.

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#1.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C270601143F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:52	RO	constant = 0b00
53	RWX	TX_NEXT_CAL_LANE_SEL: When set, this bit negates the action of tx_pdwn_lite in a similar way to tx_cal_lane_sel. This enables the driver ahead of SLS shadowing.

Bits	SCOM	Field Mnemonic: Description
54:55	RW	TX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by TX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RO	constant = 0b0
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61	RWX	TX_PDWN_LITE: When set, this bit gates the TX data path (post FIFO) to zeros on unused spare lanes when not being recalibrated.
62	RWX	TX_CAL_LANE_SEL: SLS commands and recalibration.
63	RWX	TX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the transmit FIFO for slower frequency connections.

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C280601143F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:52	RO	constant = 0b00
53	RWX	TX_NEXT_CAL_LANE_SEL: When set, this bit negates the action of tx_pdwn_lite in a similar way to tx_cal_lane_sel. This enables the driver ahead of SLS shadowing.
54:55	RW	TX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by TX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RO	constant = 0b0
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61	RWX	TX_PDWN_LITE: When set, this bit gates the TX data path (post FIFO) to zeros on unused spare lanes when not being recalibrated.
62	RWX	TX_CAL_LANE_SEL: SLS commands and recalibration.

Bits	SCOM	Field Mnemonic: Description
63	RWX	TX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the transmit FIFO for slower frequency connections.

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C290601143F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:52	RO	constant = 0b00
53	RWX	TX_NEXT_CAL_LANE_SEL: When set, this bit negates the action of tx_pdwn_lite in a similar way to tx_cal_lane_sel. This enables the driver ahead of SLS shadowing.
54:55	RW	TX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by TX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RO	constant = 0b0
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61	RWX	TX_PDWN_LITE: When set, this bit gates the TX data path (post FIFO) to zeros on unused spare lanes when not being recalibrated.
62	RWX	TX_CAL_LANE_SEL: SLS commands and recalibration.
63	RWX	TX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the transmit FIFO for slower frequency connections.

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C2A0601143F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:52	RO	constant = 0b00
53	RWX	TX_NEXT_CAL_LANE_SEL: When set, this bit negates the action of tx_pdwn_lite in a similar way to tx_cal_lane_sel. This enables the driver ahead of SLS shadowing.
54:55	RW	TX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by TX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RO	constant = 0b0
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61	RWX	TX_PDWN_LITE: When set, this bit gates the TX data path (post FIFO) to zeros on unused spare lanes when not being recalibrated.
62	RWX	TX_CAL_LANE_SEL: SLS commands and recalibration.
63	RWX	TX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the transmit FIFO for slower frequency connections.

Register Name	**Transmit Mode 2 Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C2B0601143F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:52	RO	constant = 0b00
53	RWX	TX_NEXT_CAL_LANE_SEL: When set, this bit negates the action of tx_pdwn_lite in a similar way to tx_cal_lane_sel. This enables the driver ahead of SLS shadowing.

Bits	SCOM	Field Mnemonic: Description
54:55	RW	TX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by TX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RO	constant = 0b0
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61	RWX	TX_PDWN_LITE: When set, this bit gates the TX data path (post FIFO) to zeros on unused spare lanes when not being recalibrated.
62	RWX	TX_CAL_LANE_SEL: SLS commands and recalibration.
63	RWX	TX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the transmit FIFO for slower frequency connections.

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C2C0601143F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:52	RO	constant = 0b00
53	RWX	TX_NEXT_CAL_LANE_SEL: When set, this bit negates the action of tx_pdwn_lite in a similar way to tx_cal_lane_sel. This enables the driver ahead of SLS shadowing.
54:55	RW	TX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by TX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RO	constant = 0b0
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61	RWX	TX_PDWN_LITE: When set, this bit gates the TX data path (post FIFO) to zeros on unused spare lanes when not being recalibrated.
62	RWX	TX_CAL_LANE_SEL: SLS commands and recalibration.

Bits	SCOM	Field Mnemonic: Description
63	RWX	TX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the transmit FIFO for slower frequency connections.

Register Name	**Transmit Mode 2 Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C2D0601143F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:52	RO	constant = 0b00
53	RWX	TX_NEXT_CAL_LANE_SEL: When set, this bit negates the action of tx_pdwn_lite in a similar way to tx_cal_lane_sel. This enables the driver ahead of SLS shadowing.
54:55	RW	TX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by TX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RO	constant = 0b0
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61	RWX	TX_PDWN_LITE: When set, this bit gates the TX data path (post FIFO) to zeros on unused spare lanes when not being recalibrated.
62	RWX	TX_CAL_LANE_SEL: SLS commands and recalibration.
63	RWX	TX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the transmit FIFO for slower frequency connections.

Register Name	**Transmit Mode 2 Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C2E0601143F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:52	RO	constant = 0b00
53	RWX	TX_NEXT_CAL_LANE_SEL: When set, this bit negates the action of tx_pdwn_lite in a similar way to tx_cal_lane_sel. This enables the driver ahead of SLS shadowing.
54:55	RW	TX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by TX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RO	constant = 0b0
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61	RWX	TX_PDWN_LITE: When set, this bit gates the TX data path (post FIFO) to zeros on unused spare lanes when not being recalibrated.
62	RWX	TX_CAL_LANE_SEL: SLS commands and recalibration.
63	RWX	TX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the transmit FIFO for slower frequency connections.

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C2F0601143F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:52	RO	constant = 0b00
53	RWX	TX_NEXT_CAL_LANE_SEL: When set, this bit negates the action of tx_pdwn_lite in a similar way to tx_cal_lane_sel. This enables the driver ahead of SLS shadowing.

Bits	SCOM	Field Mnemonic: Description
54:55	RW	TX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by TX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RO	constant = 0b0
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61	RWX	TX_PDWN_LITE: When set, this bit gates the TX data path (post FIFO) to zeros on unused spare lanes when not being recalibrated.
62	RWX	TX_CAL_LANE_SEL: SLS commands and recalibration.
63	RWX	TX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the transmit FIFO for slower frequency connections.

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#4.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C300601143F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:52	RO	constant = 0b00
53	RWX	TX_NEXT_CAL_LANE_SEL: When set, this bit negates the action of tx_pdwn_lite in a similar way to tx_cal_lane_sel. This enables the driver ahead of SLS shadowing.
54:55	RW	TX_PRBS_SCRAMBLE_MODE: This field selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by TX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RO	constant = 0b0
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61	RWX	TX_PDWN_LITE: When set, this bit gates the TX data path (post FIFO) to zeros on unused spare lanes when not being recalibrated.
62	RWX	TX_CAL_LANE_SEL: SLS commands and recalibration.

Bits	SCOM	Field Mnemonic: Description
63	RWX	TX_FIFO_HALF_WIDTH_MODE: This bit selects half-width mode for the transmit FIFO for slower frequency connections.

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	800414000601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	800414010601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	800414020601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	800414030601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#1.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	800414040601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	**Transmit CNTL1G Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#1.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	800414050601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	**Transmit CNTL1G Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#1.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	800414060601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#1.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	800414070601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#2.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	800414080601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#2.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	800414090601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#2.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	8004140A0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#2.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	8004140B0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	8004140C0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	8004140D0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	8004140E0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	8004140F0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#4.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	800414100601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#0.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	800414200601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#0.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	800414210601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	**Transmit CNTL1G Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#0.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	800414220601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	**Transmit CNTL1G Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#0.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	800414230601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#1.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	800414240601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#1.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	800414250601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#1.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	800414260601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#1.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	800414270601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	800414280601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	800414290601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	8004142A0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	8004142B0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	8004142C0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	8004142D0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	8004142E0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	8004142F0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#4.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	800414300601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56	NCX	Reserved field.
57	NCX	Reserved field.
58	NCX	Reserved field.
59	NCX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C000601143F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.

Bits	SCOM	Field Mnemonic: Description
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C010601143F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C020601143F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C030601143F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#1.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C040601143F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#1.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C050601143F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#1.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C060601143F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#1.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C070601143F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.

Bits	SCOM	Field Mnemonic: Description
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#2.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C080601143F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#2.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C090601143F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	**Transmit STAT1 Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#2.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C0A0601143F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	**Transmit STAT1 Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#2.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C0B0601143F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	**Transmit STAT1 Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C0C0601143F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C0D0601143F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C0E0601143F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.

Bits	SCOM	Field Mnemonic: Description
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C0F0601143F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#4.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C100601143F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#0.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C200601143F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#0.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C210601143F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#0.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C220601143F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#0.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C230601143F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#1.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C240601143F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.

Bits	SCOM	Field Mnemonic: Description
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#1.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C250601143F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#1.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C260601143F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#1.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C270601143F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C280601143F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C290601143F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	**Transmit STAT1 Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C2A0601143F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	**Transmit STAT1 Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C2B0601143F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.

Bits	SCOM	Field Mnemonic: Description
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C2C0601143F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C2D0601143F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C2E0601143F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C2F0601143F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#4.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C300601143F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	**Transmit FIR Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_PL
Address	800424000601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	**Transmit FIR Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_PL
Address	800424010601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	**Transmit FIR Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_PL
Address	800424020601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_PL
Address	800424030601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#1.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_PL
Address	800424040601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#1.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_PL
Address	800424050601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#1.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_PL
Address	800424060601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	**Transmit FIR Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#1.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_PL
Address	800424070601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	**Transmit FIR Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#2.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_PL
Address	800424080601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	**Transmit FIR Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#2.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_PL
Address	800424090601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	**Transmit FIR Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#2.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_PL
Address	8004240A0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#2.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_PL
Address	8004240B0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_PL
Address	8004240C0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_PL
Address	8004240D0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_PL
Address	8004240E0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_PL
Address	8004240F0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#4.DD.TX_BIT_REGS.TX_FIR_PL
Address	800424100601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#0.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_PL
Address	800424200601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#0.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_PL
Address	800424210601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#0.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_PL
Address	800424220601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#0.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_PL
Address	800424230601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#1.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_PL
Address	800424240601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#1.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_PL
Address	800424250601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#1.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_PL
Address	800424260601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#1.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_PL
Address	800424270601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_PL
Address	800424280601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_PL
Address	800424290601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_PL
Address	8004242A0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_PL
Address	8004242B0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_PL
Address	8004242C0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_PL
Address	8004242D0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_PL
Address	8004242E0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_PL
Address	8004242F0601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#4.DD.TX_BIT_REGS.TX_FIR_PL
Address	800424300601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Mask Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C000601143F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Mask Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C010601143F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Mask Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C020601143F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Mask Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C030601143F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Mask Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#1.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C040601143F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.

Bits	SCOM	Field Mnemonic: Description
49:63	RO	constant = 0b000000000000000

Register Name	**Transmit FIR Mask Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#1.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C050601143F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	**Transmit FIR Mask Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#1.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C060601143F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	**Transmit FIR Mask Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#1.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C070601143F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	**Transmit FIR Mask Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#2.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C080601143F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Mask Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#2.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C090601143F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Mask Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#2.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C0A0601143F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Mask Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#2.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C0B0601143F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	**Transmit FIR Mask Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C0C0601143F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	**Transmit FIR Mask Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C0D0601143F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	**Transmit FIR Mask Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C0E0601143F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	**Transmit FIR Mask Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C0F0601143F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.

Bits	SCOM	Field Mnemonic: Description
49:63	RO	constant = 0b000000000000000

Register Name	**Transmit FIR Mask Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#4.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C100601143F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	**Transmit FIR Mask Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#0.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C200601143F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	**Transmit FIR Mask Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#0.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C210601143F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	**Transmit FIR Mask Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#0.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C220601143F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Mask Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#0.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C230601143F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Mask Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#1.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C240601143F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Mask Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#1.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C250601143F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	**Transmit FIR Mask Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#1.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C260601143F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	**Transmit FIR Mask Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#1.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C270601143F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	**Transmit FIR Mask Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C280601143F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	**Transmit FIR Mask Per-Lane Register**
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C290601143F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.

Bits	SCOM	Field Mnemonic: Description
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Mask Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C2A0601143F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Mask Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C2B0601143F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Mask Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C2C0601143F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Mask Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C2D0601143F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Mask Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C2E0601143F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Mask Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C2F0601143F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Mask Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#4.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C300601143F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	800434000601143F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	800434010601143F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	800434020601143F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	800434030601143F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.

Bits	SCOM	Field Mnemonic: Description
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#1.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	800434040601143F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#1.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	800434050601143F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#1.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	800434060601143F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#1.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	800434070601143F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#2.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	800434080601143F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#2.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	800434090601143F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#2.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	8004340A0601143F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#2.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	8004340B0601143F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	8004340C0601143F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	8004340D0601143F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	8004340E0601143F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.

Bits	SCOM	Field Mnemonic: Description
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	8004340F0601143F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#4.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	800434100601143F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#0.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	800434200601143F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#0.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	800434210601143F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#0.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	800434220601143F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#0.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	800434230601143F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#1.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	800434240601143F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#1.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	800434250601143F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#1.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	800434260601143F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#1.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	800434270601143F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	800434280601143F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.

Bits	SCOM	Field Mnemonic: Description
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	800434290601143F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	8004342A0601143F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	8004342B0601143F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	8004342C0601143F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	8004342D0601143F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	8004342E0601143F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	8004342F0601143F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#4.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	800434300601143F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL
Address	80043C000601143F (SCOM)
Description	This register contains the first set of transmit E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	TX_PRBS_SEED_VALUE_0_15: Transmit per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This must be set consistent with rx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in full- or half-width mode. 0b0000000000000000 = TX PRBS tap points A and B, and TX half-width tap point A. 0b0000000000011110 = TX PRBS tap point C. 0b0000000000011111 = TX PRBS tap point D. 0b0000000000001111 = TX PRBS tap point E, and TX half-width tap point B. 0b0000000001111100 = TX PRBS tap point F. 0b0000110001100011 = TX PRBS tap point G. 0b0000111001110011 = TX PRBS tap point H. 0b0000000111101111 = TX half-width PRBS tap point C. 0b0000000111110001 = TX half-width PRBS tap point D. 0b0000000011111011 = TX half-width PRBS tap point E. 0b0000011111000010 = TX half-width PRBS tap point F. 0b1100011000110001 = TX half-width PRBS tap point G. 0b1110011100111001 = TX half-width PRBS tap point H.

Register Name	Transmit Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL
Address	80043C010601143F (SCOM)
Description	This register contains the first set of transmit E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	TX_PRBS_SEED_VALUE_0_15: Transmit per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This must be set consistent with rx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in full- or half-width mode. 0b0000000000000000 = TX PRBS tap points A and B, and TX half-width tap point A. 0b0000000000011110 = TX PRBS tap point C. 0b0000000000011111 = TX PRBS tap point D. 0b0000000000001111 = TX PRBS tap point E, and TX half-width tap point B. 0b0000000001111100 = TX PRBS tap point F. 0b0000110001100011 = TX PRBS tap point G. 0b0000111001110011 = TX PRBS tap point H. 0b0000000111101111 = TX half-width PRBS tap point C. 0b0000000111110001 = TX half-width PRBS tap point D. 0b0000000011111011 = TX half-width PRBS tap point E. 0b0000011111000010 = TX half-width PRBS tap point F. 0b1100011000110001 = TX half-width PRBS tap point G. 0b1110011100111001 = TX half-width PRBS tap point H.

Register Name	Transmit Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL
Address	80043C020601143F (SCOM)
Description	This register contains the first set of transmit E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	TX_PRBS_SEED_VALUE_0_15: Transmit per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This must be set consistent with rx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in full- or half-width mode. 0b0000000000000000 = TX PRBS tap points A and B, and TX half-width tap point A. 0b0000000000011110 = TX PRBS tap point C. 0b0000000000011111 = TX PRBS tap point D. 0b0000000000001111 = TX PRBS tap point E, and TX half-width tap point B. 0b0000000001111100 = TX PRBS tap point F. 0b0000110001100011 = TX PRBS tap point G. 0b0000111001110011 = TX PRBS tap point H. 0b0000000111101111 = TX half-width PRBS tap point C. 0b0000000111110001 = TX half-width PRBS tap point D. 0b0000000011111011 = TX half-width PRBS tap point E. 0b0000011111000010 = TX half-width PRBS tap point F. 0b1100011000110001 = TX half-width PRBS tap point G. 0b1110011100111001 = TX half-width PRBS tap point H.

Register Name	Transmit Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL
Address	80043C030601143F (SCOM)
Description	This register contains the first set of transmit E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	TX_PRBS_SEED_VALUE_0_15: Transmit per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This must be set consistent with rx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in full- or half-width mode. 0b0000000000000000 = TX PRBS tap points A and B, and TX half-width tap point A. 0b0000000000011110 = TX PRBS tap point C. 0b0000000000011111 = TX PRBS tap point D. 0b0000000000001111 = TX PRBS tap point E, and TX half-width tap point B. 0b0000000001111100 = TX PRBS tap point F. 0b0000110001100011 = TX PRBS tap point G. 0b0000111001110011 = TX PRBS tap point H. 0b0000000111101111 = TX half-width PRBS tap point C. 0b0000000111110001 = TX half-width PRBS tap point D. 0b0000000011111011 = TX half-width PRBS tap point E. 0b0000011111000010 = TX half-width PRBS tap point F. 0b1100011000110001 = TX half-width PRBS tap point G. 0b1110011100111001 = TX half-width PRBS tap point H.

Register Name	Transmit Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#1.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL
Address	80043C040601143F (SCOM)
Description	This register contains the first set of transmit E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	TX_PRBS_SEED_VALUE_0_15: Transmit per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This must be set consistent with rx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in full- or half-width mode. 0b0000000000000000 = TX PRBS tap points A and B, and TX half-width tap point A. 0b0000000000011110 = TX PRBS tap point C. 0b0000000000011111 = TX PRBS tap point D. 0b0000000000001111 = TX PRBS tap point E, and TX half-width tap point B. 0b0000000001111100 = TX PRBS tap point F. 0b0000110001100011 = TX PRBS tap point G. 0b0000111001110011 = TX PRBS tap point H. 0b0000000111101111 = TX half-width PRBS tap point C. 0b0000000111110001 = TX half-width PRBS tap point D. 0b0000000011111011 = TX half-width PRBS tap point E. 0b0000011111000010 = TX half-width PRBS tap point F. 0b1100011000110001 = TX half-width PRBS tap point G. 0b1110011100111001 = TX half-width PRBS tap point H.

Register Name	Transmit Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#1.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL
Address	80043C050601143F (SCOM)
Description	This register contains the first set of transmit E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	TX_PRBS_SEED_VALUE_0_15: Transmit per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This must be set consistent with rx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in full- or half-width mode. 0b0000000000000000 = TX PRBS tap points A and B, and TX half-width tap point A. 0b0000000000011110 = TX PRBS tap point C. 0b0000000000011111 = TX PRBS tap point D. 0b0000000000001111 = TX PRBS tap point E, and TX half-width tap point B. 0b0000000001111100 = TX PRBS tap point F. 0b0000110001100011 = TX PRBS tap point G. 0b0000111001110011 = TX PRBS tap point H. 0b0000000111101111 = TX half-width PRBS tap point C. 0b0000000111110001 = TX half-width PRBS tap point D. 0b0000000011111011 = TX half-width PRBS tap point E. 0b0000011111000010 = TX half-width PRBS tap point F. 0b1100011000110001 = TX half-width PRBS tap point G. 0b1110011100111001 = TX half-width PRBS tap point H.

Register Name	Transmit Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#1.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL
Address	80043C060601143F (SCOM)
Description	This register contains the first set of transmit E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	TX_PRBS_SEED_VALUE_0_15: Transmit per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This must be set consistent with rx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in full- or half-width mode. 0b0000000000000000 = TX PRBS tap points A and B, and TX half-width tap point A. 0b0000000000011110 = TX PRBS tap point C. 0b0000000000011111 = TX PRBS tap point D. 0b0000000000001111 = TX PRBS tap point E, and TX half-width tap point B. 0b0000000001111100 = TX PRBS tap point F. 0b0000110001100011 = TX PRBS tap point G. 0b0000111001110011 = TX PRBS tap point H. 0b0000000111101111 = TX half-width PRBS tap point C. 0b0000000111110001 = TX half-width PRBS tap point D. 0b0000000011111011 = TX half-width PRBS tap point E. 0b0000011111000010 = TX half-width PRBS tap point F. 0b1100011000110001 = TX half-width PRBS tap point G. 0b1110011100111001 = TX half-width PRBS tap point H.

Register Name	Transmit Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#1.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL
Address	80043C070601143F (SCOM)
Description	This register contains the first set of transmit E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	TX_PRBS_SEED_VALUE_0_15: Transmit per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This must be set consistent with rx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in full- or half-width mode. 0b0000000000000000 = TX PRBS tap points A and B, and TX half-width tap point A. 0b0000000000011110 = TX PRBS tap point C. 0b0000000000011111 = TX PRBS tap point D. 0b0000000000001111 = TX PRBS tap point E, and TX half-width tap point B. 0b0000000001111100 = TX PRBS tap point F. 0b0000110001100011 = TX PRBS tap point G. 0b0000111001110011 = TX PRBS tap point H. 0b0000000111101111 = TX half-width PRBS tap point C. 0b0000000111110001 = TX half-width PRBS tap point D. 0b0000000011111011 = TX half-width PRBS tap point E. 0b0000011111000010 = TX half-width PRBS tap point F. 0b1100011000110001 = TX half-width PRBS tap point G. 0b1110011100111001 = TX half-width PRBS tap point H.

Register Name	Transmit Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#2.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL
Address	80043C080601143F (SCOM)
Description	This register contains the first set of transmit E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	TX_PRBS_SEED_VALUE_0_15: Transmit per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This must be set consistent with rx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in full- or half-width mode. 0b0000000000000000 = TX PRBS tap points A and B, and TX half-width tap point A. 0b0000000000011110 = TX PRBS tap point C. 0b0000000000011111 = TX PRBS tap point D. 0b0000000000001111 = TX PRBS tap point E, and TX half-width tap point B. 0b0000000001111100 = TX PRBS tap point F. 0b0000110001100011 = TX PRBS tap point G. 0b0000111001110011 = TX PRBS tap point H. 0b0000000111101111 = TX half-width PRBS tap point C. 0b0000000111110001 = TX half-width PRBS tap point D. 0b0000000011111011 = TX half-width PRBS tap point E. 0b0000011111000010 = TX half-width PRBS tap point F. 0b1100011000110001 = TX half-width PRBS tap point G. 0b1110011100111001 = TX half-width PRBS tap point H.

Register Name	Transmit Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#2.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL
Address	80043C090601143F (SCOM)
Description	This register contains the first set of transmit E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	TX_PRBS_SEED_VALUE_0_15: Transmit per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This must be set consistent with rx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in full- or half-width mode. 0b0000000000000000 = TX PRBS tap points A and B, and TX half-width tap point A. 0b0000000000011110 = TX PRBS tap point C. 0b0000000000011111 = TX PRBS tap point D. 0b0000000000001111 = TX PRBS tap point E, and TX half-width tap point B. 0b0000000001111100 = TX PRBS tap point F. 0b0000110001100011 = TX PRBS tap point G. 0b0000111001110011 = TX PRBS tap point H. 0b0000000111101111 = TX half-width PRBS tap point C. 0b0000000111110001 = TX half-width PRBS tap point D. 0b0000000011111011 = TX half-width PRBS tap point E. 0b0000011111000010 = TX half-width PRBS tap point F. 0b1100011000110001 = TX half-width PRBS tap point G. 0b1110011100111001 = TX half-width PRBS tap point H.

Register Name	Transmit Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#2.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL
Address	80043C0A0601143F (SCOM)
Description	This register contains the first set of transmit E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	TX_PRBS_SEED_VALUE_0_15: Transmit per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This must be set consistent with rx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in full- or half-width mode. 0b0000000000000000 = TX PRBS tap points A and B, and TX half-width tap point A. 0b0000000000011110 = TX PRBS tap point C. 0b0000000000011111 = TX PRBS tap point D. 0b0000000000001111 = TX PRBS tap point E, and TX half-width tap point B. 0b0000000001111100 = TX PRBS tap point F. 0b0000110001100011 = TX PRBS tap point G. 0b0000111001110011 = TX PRBS tap point H. 0b0000000111101111 = TX half-width PRBS tap point C. 0b0000000111110001 = TX half-width PRBS tap point D. 0b0000000011111011 = TX half-width PRBS tap point E. 0b0000011111000010 = TX half-width PRBS tap point F. 0b1100011000110001 = TX half-width PRBS tap point G. 0b1110011100111001 = TX half-width PRBS tap point H.

Register Name	Transmit Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#2.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL
Address	80043C0B0601143F (SCOM)
Description	This register contains the first set of transmit E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	TX_PRBS_SEED_VALUE_0_15: Transmit per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This must be set consistent with rx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in full- or half-width mode. 0b0000000000000000 = TX PRBS tap points A and B, and TX half-width tap point A. 0b0000000000011110 = TX PRBS tap point C. 0b0000000000011111 = TX PRBS tap point D. 0b0000000000001111 = TX PRBS tap point E, and TX half-width tap point B. 0b0000000001111100 = TX PRBS tap point F. 0b0000110001100011 = TX PRBS tap point G. 0b0000111001110011 = TX PRBS tap point H. 0b0000000111101111 = TX half-width PRBS tap point C. 0b0000000111110001 = TX half-width PRBS tap point D. 0b0000000011111011 = TX half-width PRBS tap point E. 0b0000011111000010 = TX half-width PRBS tap point F. 0b1100011000110001 = TX half-width PRBS tap point G. 0b1110011100111001 = TX half-width PRBS tap point H.

Register Name	Transmit Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL
Address	80043C0C0601143F (SCOM)
Description	This register contains the first set of transmit E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	TX_PRBS_SEED_VALUE_0_15: Transmit per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This must be set consistent with rx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in full- or half-width mode. 0b0000000000000000 = TX PRBS tap points A and B, and TX half-width tap point A. 0b0000000000011110 = TX PRBS tap point C. 0b0000000000011111 = TX PRBS tap point D. 0b0000000000001111 = TX PRBS tap point E, and TX half-width tap point B. 0b0000000001111100 = TX PRBS tap point F. 0b0000110001100011 = TX PRBS tap point G. 0b0000111001110011 = TX PRBS tap point H. 0b0000000111101111 = TX half-width PRBS tap point C. 0b0000000111110001 = TX half-width PRBS tap point D. 0b0000000011111011 = TX half-width PRBS tap point E. 0b0000011111000010 = TX half-width PRBS tap point F. 0b1100011000110001 = TX half-width PRBS tap point G. 0b1110011100111001 = TX half-width PRBS tap point H.

Register Name	Transmit Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL
Address	80043C0D0601143F (SCOM)
Description	This register contains the first set of transmit E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	TX_PRBS_SEED_VALUE_0_15: Transmit per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This must be set consistent with rx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in full- or half-width mode. 0b0000000000000000 = TX PRBS tap points A and B, and TX half-width tap point A. 0b0000000000011110 = TX PRBS tap point C. 0b0000000000011111 = TX PRBS tap point D. 0b0000000000001111 = TX PRBS tap point E, and TX half-width tap point B. 0b0000000001111100 = TX PRBS tap point F. 0b0000110001100011 = TX PRBS tap point G. 0b0000111001110011 = TX PRBS tap point H. 0b0000000111101111 = TX half-width PRBS tap point C. 0b0000000111110001 = TX half-width PRBS tap point D. 0b0000000011111011 = TX half-width PRBS tap point E. 0b0000011111000010 = TX half-width PRBS tap point F. 0b1100011000110001 = TX half-width PRBS tap point G. 0b1110011100111001 = TX half-width PRBS tap point H.

Register Name	Transmit Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL
Address	80043C0E0601143F (SCOM)
Description	This register contains the first set of transmit E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	TX_PRBS_SEED_VALUE_0_15: Transmit per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This must be set consistent with rx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in full- or half-width mode. 0b0000000000000000 = TX PRBS tap points A and B, and TX half-width tap point A. 0b0000000000011110 = TX PRBS tap point C. 0b0000000000011111 = TX PRBS tap point D. 0b0000000000001111 = TX PRBS tap point E, and TX half-width tap point B. 0b0000000001111100 = TX PRBS tap point F. 0b0000110001100011 = TX PRBS tap point G. 0b0000111001110011 = TX PRBS tap point H. 0b0000000111101111 = TX half-width PRBS tap point C. 0b0000000111110001 = TX half-width PRBS tap point D. 0b0000000011111011 = TX half-width PRBS tap point E. 0b0000011111000010 = TX half-width PRBS tap point F. 0b1100011000110001 = TX half-width PRBS tap point G. 0b1110011100111001 = TX half-width PRBS tap point H.

Register Name	Transmit Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL
Address	80043C0F0601143F (SCOM)
Description	This register contains the first set of transmit E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	TX_PRBS_SEED_VALUE_0_15: Transmit per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This must be set consistent with rx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in full- or half-width mode. 0b0000000000000000 = TX PRBS tap points A and B, and TX half-width tap point A. 0b0000000000011110 = TX PRBS tap point C. 0b0000000000011111 = TX PRBS tap point D. 0b0000000000001111 = TX PRBS tap point E, and TX half-width tap point B. 0b0000000001111100 = TX PRBS tap point F. 0b0000110001100011 = TX PRBS tap point G. 0b0000111001110011 = TX PRBS tap point H. 0b0000000111101111 = TX half-width PRBS tap point C. 0b0000000111110001 = TX half-width PRBS tap point D. 0b0000000011111011 = TX half-width PRBS tap point E. 0b0000011111000010 = TX half-width PRBS tap point F. 0b1100011000110001 = TX half-width PRBS tap point G. 0b1110011100111001 = TX half-width PRBS tap point H.

Register Name	Transmit Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#4.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL
Address	80043C100601143F (SCOM)
Description	This register contains the first set of transmit E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	TX_PRBS_SEED_VALUE_0_15: Transmit per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This must be set consistent with rx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in full- or half-width mode. 0b0000000000000000 = TX PRBS tap points A and B, and TX half-width tap point A. 0b0000000000011110 = TX PRBS tap point C. 0b0000000000011111 = TX PRBS tap point D. 0b0000000000001111 = TX PRBS tap point E, and TX half-width tap point B. 0b0000000001111100 = TX PRBS tap point F. 0b0000110001100011 = TX PRBS tap point G. 0b0000111001110011 = TX PRBS tap point H. 0b0000000111101111 = TX half-width PRBS tap point C. 0b0000000111110001 = TX half-width PRBS tap point D. 0b0000000011111011 = TX half-width PRBS tap point E. 0b0000011111000010 = TX half-width PRBS tap point F. 0b1100011000110001 = TX half-width PRBS tap point G. 0b1110011100111001 = TX half-width PRBS tap point H.

Register Name	Transmit Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#0.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL
Address	80043C200601143F (SCOM)
Description	This register contains the first set of transmit E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	TX_PRBS_SEED_VALUE_0_15: Transmit per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This must be set consistent with rx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in full- or half-width mode. 0b0000000000000000 = TX PRBS tap points A and B, and TX half-width tap point A. 0b0000000000011110 = TX PRBS tap point C. 0b0000000000011111 = TX PRBS tap point D. 0b0000000000001111 = TX PRBS tap point E, and TX half-width tap point B. 0b0000000001111100 = TX PRBS tap point F. 0b0000110001100011 = TX PRBS tap point G. 0b0000111001110011 = TX PRBS tap point H. 0b0000000111101111 = TX half-width PRBS tap point C. 0b0000000111110001 = TX half-width PRBS tap point D. 0b0000000011111011 = TX half-width PRBS tap point E. 0b0000011111000010 = TX half-width PRBS tap point F. 0b1100011000110001 = TX half-width PRBS tap point G. 0b1110011100111001 = TX half-width PRBS tap point H.

Register Name	Transmit Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#0.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL
Address	80043C210601143F (SCOM)
Description	This register contains the first set of transmit E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	TX_PRBS_SEED_VALUE_0_15: Transmit per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This must be set consistent with rx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in full- or half-width mode. 0b0000000000000000 = TX PRBS tap points A and B, and TX half-width tap point A. 0b0000000000011110 = TX PRBS tap point C. 0b0000000000011111 = TX PRBS tap point D. 0b0000000000001111 = TX PRBS tap point E, and TX half-width tap point B. 0b0000000001111100 = TX PRBS tap point F. 0b0000110001100011 = TX PRBS tap point G. 0b0000111001110011 = TX PRBS tap point H. 0b0000000111101111 = TX half-width PRBS tap point C. 0b0000000111110001 = TX half-width PRBS tap point D. 0b0000000011111011 = TX half-width PRBS tap point E. 0b0000011111000010 = TX half-width PRBS tap point F. 0b1100011000110001 = TX half-width PRBS tap point G. 0b1110011100111001 = TX half-width PRBS tap point H.

Register Name	Transmit Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#0.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL
Address	80043C220601143F (SCOM)
Description	This register contains the first set of transmit E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	TX_PRBS_SEED_VALUE_0_15: Transmit per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This must be set consistent with rx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in full- or half-width mode. 0b0000000000000000 = TX PRBS tap points A and B, and TX half-width tap point A. 0b0000000000011110 = TX PRBS tap point C. 0b0000000000011111 = TX PRBS tap point D. 0b0000000000001111 = TX PRBS tap point E, and TX half-width tap point B. 0b0000000001111100 = TX PRBS tap point F. 0b0000110001100011 = TX PRBS tap point G. 0b0000111001110011 = TX PRBS tap point H. 0b0000000111101111 = TX half-width PRBS tap point C. 0b0000000111110001 = TX half-width PRBS tap point D. 0b0000000011111011 = TX half-width PRBS tap point E. 0b0000011111000010 = TX half-width PRBS tap point F. 0b1100011000110001 = TX half-width PRBS tap point G. 0b1110011100111001 = TX half-width PRBS tap point H.

Register Name	Transmit Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#0.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL
Address	80043C230601143F (SCOM)
Description	This register contains the first set of transmit E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	TX_PRBS_SEED_VALUE_0_15: Transmit per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This must be set consistent with rx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in full- or half-width mode. 0b0000000000000000 = TX PRBS tap points A and B, and TX half-width tap point A. 0b0000000000011110 = TX PRBS tap point C. 0b0000000000011111 = TX PRBS tap point D. 0b0000000000001111 = TX PRBS tap point E, and TX half-width tap point B. 0b0000000001111100 = TX PRBS tap point F. 0b0000110001100011 = TX PRBS tap point G. 0b0000111001110011 = TX PRBS tap point H. 0b0000000111101111 = TX half-width PRBS tap point C. 0b0000000111110001 = TX half-width PRBS tap point D. 0b0000000011111011 = TX half-width PRBS tap point E. 0b0000011111000010 = TX half-width PRBS tap point F. 0b1100011000110001 = TX half-width PRBS tap point G. 0b1110011100111001 = TX half-width PRBS tap point H.

Register Name	Transmit Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#1.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL
Address	80043C240601143F (SCOM)
Description	This register contains the first set of transmit E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	TX_PRBS_SEED_VALUE_0_15: Transmit per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This must be set consistent with rx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in full- or half-width mode. 0b0000000000000000 = TX PRBS tap points A and B, and TX half-width tap point A. 0b0000000000011110 = TX PRBS tap point C. 0b0000000000011111 = TX PRBS tap point D. 0b0000000000001111 = TX PRBS tap point E, and TX half-width tap point B. 0b0000000001111100 = TX PRBS tap point F. 0b0000110001100011 = TX PRBS tap point G. 0b0000111001110011 = TX PRBS tap point H. 0b0000000111101111 = TX half-width PRBS tap point C. 0b0000000111110001 = TX half-width PRBS tap point D. 0b0000000011111011 = TX half-width PRBS tap point E. 0b0000011111000010 = TX half-width PRBS tap point F. 0b1100011000110001 = TX half-width PRBS tap point G. 0b1110011100111001 = TX half-width PRBS tap point H.

Register Name	Transmit Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#1.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL
Address	80043C250601143F (SCOM)
Description	This register contains the first set of transmit E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	TX_PRBS_SEED_VALUE_0_15: Transmit per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This must be set consistent with rx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in full- or half-width mode. 0b0000000000000000 = TX PRBS tap points A and B, and TX half-width tap point A. 0b0000000000011110 = TX PRBS tap point C. 0b0000000000011111 = TX PRBS tap point D. 0b0000000000001111 = TX PRBS tap point E, and TX half-width tap point B. 0b0000000001111100 = TX PRBS tap point F. 0b0000110001100011 = TX PRBS tap point G. 0b0000111001110011 = TX PRBS tap point H. 0b0000000111101111 = TX half-width PRBS tap point C. 0b0000000111110001 = TX half-width PRBS tap point D. 0b0000000011111011 = TX half-width PRBS tap point E. 0b0000011111000010 = TX half-width PRBS tap point F. 0b1100011000110001 = TX half-width PRBS tap point G. 0b1110011100111001 = TX half-width PRBS tap point H.

Register Name	Transmit Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#1.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL
Address	80043C260601143F (SCOM)
Description	This register contains the first set of transmit E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	TX_PRBS_SEED_VALUE_0_15: Transmit per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This must be set consistent with rx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in full- or half-width mode. 0b0000000000000000 = TX PRBS tap points A and B, and TX half-width tap point A. 0b0000000000011110 = TX PRBS tap point C. 0b0000000000011111 = TX PRBS tap point D. 0b0000000000001111 = TX PRBS tap point E, and TX half-width tap point B. 0b0000000001111100 = TX PRBS tap point F. 0b0000110001100011 = TX PRBS tap point G. 0b0000111001110011 = TX PRBS tap point H. 0b0000000111101111 = TX half-width PRBS tap point C. 0b0000000111110001 = TX half-width PRBS tap point D. 0b0000000011111011 = TX half-width PRBS tap point E. 0b0000011111000010 = TX half-width PRBS tap point F. 0b1100011000110001 = TX half-width PRBS tap point G. 0b1110011100111001 = TX half-width PRBS tap point H.

Register Name	Transmit Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#1.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL
Address	80043C270601143F (SCOM)
Description	This register contains the first set of transmit E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	TX_PRBS_SEED_VALUE_0_15: Transmit per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This must be set consistent with rx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in full- or half-width mode. 0b0000000000000000 = TX PRBS tap points A and B, and TX half-width tap point A. 0b0000000000011110 = TX PRBS tap point C. 0b0000000000011111 = TX PRBS tap point D. 0b0000000000001111 = TX PRBS tap point E, and TX half-width tap point B. 0b0000000001111100 = TX PRBS tap point F. 0b0000110001100011 = TX PRBS tap point G. 0b0000111001110011 = TX PRBS tap point H. 0b0000000111101111 = TX half-width PRBS tap point C. 0b0000000111110001 = TX half-width PRBS tap point D. 0b0000000011111011 = TX half-width PRBS tap point E. 0b0000011111000010 = TX half-width PRBS tap point F. 0b1100011000110001 = TX half-width PRBS tap point G. 0b1110011100111001 = TX half-width PRBS tap point H.

Register Name	Transmit Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL
Address	80043C280601143F (SCOM)
Description	This register contains the first set of transmit E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	TX_PRBS_SEED_VALUE_0_15: Transmit per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This must be set consistent with rx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in full- or half-width mode. 0b0000000000000000 = TX PRBS tap points A and B, and TX half-width tap point A. 0b0000000000011110 = TX PRBS tap point C. 0b0000000000011111 = TX PRBS tap point D. 0b0000000000001111 = TX PRBS tap point E, and TX half-width tap point B. 0b0000000001111100 = TX PRBS tap point F. 0b0000110001100011 = TX PRBS tap point G. 0b0000111001110011 = TX PRBS tap point H. 0b0000000111101111 = TX half-width PRBS tap point C. 0b0000000111110001 = TX half-width PRBS tap point D. 0b0000000011111011 = TX half-width PRBS tap point E. 0b0000011111000010 = TX half-width PRBS tap point F. 0b1100011000110001 = TX half-width PRBS tap point G. 0b1110011100111001 = TX half-width PRBS tap point H.

Register Name	Transmit Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL
Address	80043C290601143F (SCOM)
Description	This register contains the first set of transmit E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	TX_PRBS_SEED_VALUE_0_15: Transmit per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This must be set consistent with rx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in full- or half-width mode. 0b0000000000000000 = TX PRBS tap points A and B, and TX half-width tap point A. 0b0000000000011110 = TX PRBS tap point C. 0b0000000000011111 = TX PRBS tap point D. 0b0000000000001111 = TX PRBS tap point E, and TX half-width tap point B. 0b0000000001111100 = TX PRBS tap point F. 0b0000110001100011 = TX PRBS tap point G. 0b0000111001110011 = TX PRBS tap point H. 0b0000000111101111 = TX half-width PRBS tap point C. 0b0000000111110001 = TX half-width PRBS tap point D. 0b0000000011111011 = TX half-width PRBS tap point E. 0b0000011111000010 = TX half-width PRBS tap point F. 0b1100011000110001 = TX half-width PRBS tap point G. 0b1110011100111001 = TX half-width PRBS tap point H.

Register Name	Transmit Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL
Address	80043C2A0601143F (SCOM)
Description	This register contains the first set of transmit E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	TX_PRBS_SEED_VALUE_0_15: Transmit per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This must be set consistent with rx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in full- or half-width mode. 0b0000000000000000 = TX PRBS tap points A and B, and TX half-width tap point A. 0b0000000000011110 = TX PRBS tap point C. 0b0000000000011111 = TX PRBS tap point D. 0b0000000000001111 = TX PRBS tap point E, and TX half-width tap point B. 0b0000000001111100 = TX PRBS tap point F. 0b0000110001100011 = TX PRBS tap point G. 0b0000111001110011 = TX PRBS tap point H. 0b0000000111101111 = TX half-width PRBS tap point C. 0b0000000111110001 = TX half-width PRBS tap point D. 0b0000000011111011 = TX half-width PRBS tap point E. 0b0000011111000010 = TX half-width PRBS tap point F. 0b1100011000110001 = TX half-width PRBS tap point G. 0b1110011100111001 = TX half-width PRBS tap point H.

Register Name	Transmit Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL
Address	80043C2B0601143F (SCOM)
Description	This register contains the first set of transmit E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	TX_PRBS_SEED_VALUE_0_15: Transmit per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This must be set consistent with rx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in full- or half-width mode. 0b0000000000000000 = TX PRBS tap points A and B, and TX half-width tap point A. 0b0000000000011110 = TX PRBS tap point C. 0b0000000000011111 = TX PRBS tap point D. 0b0000000000001111 = TX PRBS tap point E, and TX half-width tap point B. 0b0000000001111100 = TX PRBS tap point F. 0b0000110001100011 = TX PRBS tap point G. 0b0000111001110011 = TX PRBS tap point H. 0b0000000111101111 = TX half-width PRBS tap point C. 0b0000000111110001 = TX half-width PRBS tap point D. 0b0000000011111011 = TX half-width PRBS tap point E. 0b0000011111000010 = TX half-width PRBS tap point F. 0b1100011000110001 = TX half-width PRBS tap point G. 0b1110011100111001 = TX half-width PRBS tap point H.

Register Name	Transmit Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL
Address	80043C2C0601143F (SCOM)
Description	This register contains the first set of transmit E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	TX_PRBS_SEED_VALUE_0_15: Transmit per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This must be set consistent with rx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in full- or half-width mode. 0b0000000000000000 = TX PRBS tap points A and B, and TX half-width tap point A. 0b0000000000011110 = TX PRBS tap point C. 0b0000000000011111 = TX PRBS tap point D. 0b0000000000001111 = TX PRBS tap point E, and TX half-width tap point B. 0b0000000001111100 = TX PRBS tap point F. 0b0000110001100011 = TX PRBS tap point G. 0b0000111001110011 = TX PRBS tap point H. 0b0000000111101111 = TX half-width PRBS tap point C. 0b0000000111110001 = TX half-width PRBS tap point D. 0b0000000011111011 = TX half-width PRBS tap point E. 0b0000011111000010 = TX half-width PRBS tap point F. 0b1100011000110001 = TX half-width PRBS tap point G. 0b1110011100111001 = TX half-width PRBS tap point H.

Register Name	Transmit Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL
Address	80043C2D0601143F (SCOM)
Description	This register contains the first set of transmit E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	TX_PRBS_SEED_VALUE_0_15: Transmit per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This must be set consistent with rx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in full- or half-width mode. 0b0000000000000000 = TX PRBS tap points A and B, and TX half-width tap point A. 0b0000000000011110 = TX PRBS tap point C. 0b0000000000011111 = TX PRBS tap point D. 0b0000000000001111 = TX PRBS tap point E, and TX half-width tap point B. 0b0000000001111100 = TX PRBS tap point F. 0b0000110001100011 = TX PRBS tap point G. 0b0000111001110011 = TX PRBS tap point H. 0b0000000111101111 = TX half-width PRBS tap point C. 0b0000000111110001 = TX half-width PRBS tap point D. 0b0000000011111011 = TX half-width PRBS tap point E. 0b0000011111000010 = TX half-width PRBS tap point F. 0b1100011000110001 = TX half-width PRBS tap point G. 0b1110011100111001 = TX half-width PRBS tap point H.

Register Name	Transmit Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL
Address	80043C2E0601143F (SCOM)
Description	This register contains the first set of transmit E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	TX_PRBS_SEED_VALUE_0_15: Transmit per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This must be set consistent with rx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in full- or half-width mode. 0b0000000000000000 = TX PRBS tap points A and B, and TX half-width tap point A. 0b0000000000011110 = TX PRBS tap point C. 0b0000000000011111 = TX PRBS tap point D. 0b0000000000001111 = TX PRBS tap point E, and TX half-width tap point B. 0b0000000001111100 = TX PRBS tap point F. 0b0000110001100011 = TX PRBS tap point G. 0b0000111001110011 = TX PRBS tap point H. 0b0000000111101111 = TX half-width PRBS tap point C. 0b0000000111110001 = TX half-width PRBS tap point D. 0b0000000011111011 = TX half-width PRBS tap point E. 0b0000011111000010 = TX half-width PRBS tap point F. 0b1100011000110001 = TX half-width PRBS tap point G. 0b1110011100111001 = TX half-width PRBS tap point H.

Register Name	Transmit Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL
Address	80043C2F0601143F (SCOM)
Description	This register contains the first set of transmit E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	TX_PRBS_SEED_VALUE_0_15: Transmit per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This must be set consistent with rx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in full- or half-width mode. 0b0000000000000000 = TX PRBS tap points A and B, and TX half-width tap point A. 0b0000000000011110 = TX PRBS tap point C. 0b0000000000011111 = TX PRBS tap point D. 0b0000000000001111 = TX PRBS tap point E, and TX half-width tap point B. 0b0000000001111100 = TX PRBS tap point F. 0b0000110001100011 = TX PRBS tap point G. 0b0000111001110011 = TX PRBS tap point H. 0b0000000111101111 = TX half-width PRBS tap point C. 0b0000000111110001 = TX half-width PRBS tap point D. 0b0000000011111011 = TX half-width PRBS tap point E. 0b0000011111000010 = TX half-width PRBS tap point F. 0b1100011000110001 = TX half-width PRBS tap point G. 0b1110011100111001 = TX half-width PRBS tap point H.

Register Name	Transmit Bit Mode 1 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#4.DD.TX_BIT_REGS.TX_BIT_MODE1_E_PL
Address	80043C300601143F (SCOM)
Description	This register contains the first set of transmit E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	TX_PRBS_SEED_VALUE_0_15: Transmit per-lane PRBS seed value. This field is used to specify the loading value of the PRBS scramble pattern when the synchronous pattern is detected. This must be set consistent with rx_prbs_seed_value. When connected to legacy POWER8 memory buffer parts, the seed must load such that it matches the sequence of those legacy parts. The patterns listed here match that, including variants required to seed in full- or half-width mode. 0b0000000000000000 = TX PRBS tap points A and B, and TX half-width tap point A. 0b0000000000011110 = TX PRBS tap point C. 0b0000000000011111 = TX PRBS tap point D. 0b0000000000001111 = TX PRBS tap point E, and TX half-width tap point B. 0b0000000001111100 = TX PRBS tap point F. 0b0000110001100011 = TX PRBS tap point G. 0b0000111001110011 = TX PRBS tap point H. 0b0000000111101111 = TX half-width PRBS tap point C. 0b0000000111110001 = TX half-width PRBS tap point D. 0b0000000011111011 = TX half-width PRBS tap point E. 0b0000011111000010 = TX half-width PRBS tap point F. 0b1100011000110001 = TX half-width PRBS tap point G. 0b1110011100111001 = TX half-width PRBS tap point H.

Register Name	Transmit Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_BIT_MODE2_E_PL
Address	800444000601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	TX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the transmit per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b0000001 = TX PRBS tap point A. 0b1111100 = TX PRBS tap point B. 0b1111011 = TX PRBS tap point C. 0b0001100 = TX PRBS tap points D and G. 0b1011110 = TX PRBS tap point E. 0b0010000 = TX PRBS tap point F, and TX half-width tap point A. 0b1001110 = TX PRBS tap point H, and TX half-width tap point B. 0b0111101 = TX half-width PRBS tap point C. 0b1000110 = TX half-width PRBS tap points D and G. 0b1101111 = TX half-width PRBS tap point E. 0b0001000 = TX half-width PRBS tap point F. 0b1100111 = TX half-width PRBS tap point H.
55:63	RO	constant = 0b000000000

Register Name	Transmit Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_BIT_MODE2_E_PL
Address	800444010601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	TX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the transmit per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b0000001 = TX PRBS tap point A. 0b1111100 = TX PRBS tap point B. 0b1111011 = TX PRBS tap point C. 0b0001100 = TX PRBS tap points D and G. 0b1011110 = TX PRBS tap point E. 0b0010000 = TX PRBS tap point F, and TX half-width tap point A. 0b1001110 = TX PRBS tap point H, and TX half-width tap point B. 0b0111101 = TX half-width PRBS tap point C. 0b1000110 = TX half-width PRBS tap points D and G. 0b1101111 = TX half-width PRBS tap point E. 0b0001000 = TX half-width PRBS tap point F. 0b1100111 = TX half-width PRBS tap point H.
55:63	RO	constant = 0b000000000

Register Name	Transmit Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_BIT_MODE2_E_PL
Address	800444020601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	TX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the transmit per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b0000001 = TX PRBS tap point A. 0b1111100 = TX PRBS tap point B. 0b1111011 = TX PRBS tap point C. 0b0001100 = TX PRBS tap points D and G. 0b1011110 = TX PRBS tap point E. 0b0010000 = TX PRBS tap point F, and TX half-width tap point A. 0b1001110 = TX PRBS tap point H, and TX half-width tap point B. 0b0111101 = TX half-width PRBS tap point C. 0b1000110 = TX half-width PRBS tap points D and G. 0b1101111 = TX half-width PRBS tap point E. 0b0001000 = TX half-width PRBS tap point F. 0b1100111 = TX half-width PRBS tap point H.
55:63	RO	constant = 0b000000000

Register Name	Transmit Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_BIT_MODE2_E_PL
Address	800444030601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	TX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the transmit per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b0000001 = TX PRBS tap point A. 0b1111100 = TX PRBS tap point B. 0b1111011 = TX PRBS tap point C. 0b0001100 = TX PRBS tap points D and G. 0b1011110 = TX PRBS tap point E. 0b0010000 = TX PRBS tap point F, and TX half-width tap point A. 0b1001110 = TX PRBS tap point H, and TX half-width tap point B. 0b0111101 = TX half-width PRBS tap point C. 0b1000110 = TX half-width PRBS tap points D and G. 0b1101111 = TX half-width PRBS tap point E. 0b0001000 = TX half-width PRBS tap point F. 0b1100111 = TX half-width PRBS tap point H.
55:63	RO	constant = 0b000000000

Register Name	Transmit Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#1.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_BIT_MODE2_E_PL
Address	800444040601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	TX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the transmit per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b0000001 = TX PRBS tap point A. 0b1111100 = TX PRBS tap point B. 0b1111011 = TX PRBS tap point C. 0b0001100 = TX PRBS tap points D and G. 0b1011110 = TX PRBS tap point E. 0b0010000 = TX PRBS tap point F, and TX half-width tap point A. 0b1001110 = TX PRBS tap point H, and TX half-width tap point B. 0b0111101 = TX half-width PRBS tap point C. 0b1000110 = TX half-width PRBS tap points D and G. 0b1101111 = TX half-width PRBS tap point E. 0b0001000 = TX half-width PRBS tap point F. 0b1100111 = TX half-width PRBS tap point H.
55:63	RO	constant = 0b000000000

Register Name	Transmit Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#1.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_BIT_MODE2_E_PL
Address	800444050601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	TX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the transmit per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b0000001 = TX PRBS tap point A. 0b1111100 = TX PRBS tap point B. 0b1111011 = TX PRBS tap point C. 0b0001100 = TX PRBS tap points D and G. 0b1011110 = TX PRBS tap point E. 0b0010000 = TX PRBS tap point F, and TX half-width tap point A. 0b1001110 = TX PRBS tap point H, and TX half-width tap point B. 0b0111101 = TX half-width PRBS tap point C. 0b1000110 = TX half-width PRBS tap points D and G. 0b1101111 = TX half-width PRBS tap point E. 0b0001000 = TX half-width PRBS tap point F. 0b1100111 = TX half-width PRBS tap point H.
55:63	RO	constant = 0b000000000

Register Name	Transmit Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#1.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_BIT_MODE2_E_PL
Address	800444060601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	TX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the transmit per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b0000001 = TX PRBS tap point A. 0b1111100 = TX PRBS tap point B. 0b1111011 = TX PRBS tap point C. 0b0001100 = TX PRBS tap points D and G. 0b1011110 = TX PRBS tap point E. 0b0010000 = TX PRBS tap point F, and TX half-width tap point A. 0b1001110 = TX PRBS tap point H, and TX half-width tap point B. 0b0111101 = TX half-width PRBS tap point C. 0b1000110 = TX half-width PRBS tap points D and G. 0b1101111 = TX half-width PRBS tap point E. 0b0001000 = TX half-width PRBS tap point F. 0b1100111 = TX half-width PRBS tap point H.
55:63	RO	constant = 0b000000000

Register Name	Transmit Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#1.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_BIT_MODE2_E_PL
Address	800444070601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	TX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the transmit per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b0000001 = TX PRBS tap point A. 0b1111100 = TX PRBS tap point B. 0b1111011 = TX PRBS tap point C. 0b0001100 = TX PRBS tap points D and G. 0b1011110 = TX PRBS tap point E. 0b0010000 = TX PRBS tap point F, and TX half-width tap point A. 0b1001110 = TX PRBS tap point H, and TX half-width tap point B. 0b0111101 = TX half-width PRBS tap point C. 0b1000110 = TX half-width PRBS tap points D and G. 0b1101111 = TX half-width PRBS tap point E. 0b0001000 = TX half-width PRBS tap point F. 0b1100111 = TX half-width PRBS tap point H.
55:63	RO	constant = 0b000000000

Register Name	Transmit Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#2.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_BIT_MODE2_E_PL
Address	800444080601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	TX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the transmit per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b0000001 = TX PRBS tap point A. 0b1111100 = TX PRBS tap point B. 0b1111011 = TX PRBS tap point C. 0b0001100 = TX PRBS tap points D and G. 0b1011110 = TX PRBS tap point E. 0b0010000 = TX PRBS tap point F, and TX half-width tap point A. 0b1001110 = TX PRBS tap point H, and TX half-width tap point B. 0b0111101 = TX half-width PRBS tap point C. 0b1000110 = TX half-width PRBS tap points D and G. 0b1101111 = TX half-width PRBS tap point E. 0b0001000 = TX half-width PRBS tap point F. 0b1100111 = TX half-width PRBS tap point H.
55:63	RO	constant = 0b000000000

Register Name	Transmit Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#2.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_BIT_MODE2_E_PL
Address	800444090601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	TX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the transmit per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b0000001 = TX PRBS tap point A. 0b1111100 = TX PRBS tap point B. 0b1111011 = TX PRBS tap point C. 0b0001100 = TX PRBS tap points D and G. 0b1011110 = TX PRBS tap point E. 0b0010000 = TX PRBS tap point F, and TX half-width tap point A. 0b1001110 = TX PRBS tap point H, and TX half-width tap point B. 0b0111101 = TX half-width PRBS tap point C. 0b1000110 = TX half-width PRBS tap points D and G. 0b1101111 = TX half-width PRBS tap point E. 0b0001000 = TX half-width PRBS tap point F. 0b1100111 = TX half-width PRBS tap point H.
55:63	RO	constant = 0b000000000

Register Name	Transmit Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#2.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_BIT_MODE2_E_PL
Address	8004440A0601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	TX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the transmit per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b0000001 = TX PRBS tap point A. 0b1111100 = TX PRBS tap point B. 0b1111011 = TX PRBS tap point C. 0b0001100 = TX PRBS tap points D and G. 0b1011110 = TX PRBS tap point E. 0b0010000 = TX PRBS tap point F, and TX half-width tap point A. 0b1001110 = TX PRBS tap point H, and TX half-width tap point B. 0b0111101 = TX half-width PRBS tap point C. 0b1000110 = TX half-width PRBS tap points D and G. 0b1101111 = TX half-width PRBS tap point E. 0b0001000 = TX half-width PRBS tap point F. 0b1100111 = TX half-width PRBS tap point H.
55:63	RO	constant = 0b000000000

Register Name	Transmit Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#2.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_BIT_MODE2_E_PL
Address	8004440B0601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	TX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the transmit per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b0000001 = TX PRBS tap point A. 0b1111100 = TX PRBS tap point B. 0b1111011 = TX PRBS tap point C. 0b0001100 = TX PRBS tap points D and G. 0b1011110 = TX PRBS tap point E. 0b0010000 = TX PRBS tap point F, and TX half-width tap point A. 0b1001110 = TX PRBS tap point H, and TX half-width tap point B. 0b0111101 = TX half-width PRBS tap point C. 0b1000110 = TX half-width PRBS tap points D and G. 0b1101111 = TX half-width PRBS tap point E. 0b0001000 = TX half-width PRBS tap point F. 0b1100111 = TX half-width PRBS tap point H.
55:63	RO	constant = 0b000000000

Register Name	Transmit Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_BIT_MODE2_E_PL
Address	8004440C0601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	TX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the transmit per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b0000001 = TX PRBS tap point A. 0b1111100 = TX PRBS tap point B. 0b1111011 = TX PRBS tap point C. 0b0001100 = TX PRBS tap points D and G. 0b1011110 = TX PRBS tap point E. 0b0010000 = TX PRBS tap point F, and TX half-width tap point A. 0b1001110 = TX PRBS tap point H, and TX half-width tap point B. 0b0111101 = TX half-width PRBS tap point C. 0b1000110 = TX half-width PRBS tap points D and G. 0b1101111 = TX half-width PRBS tap point E. 0b0001000 = TX half-width PRBS tap point F. 0b1100111 = TX half-width PRBS tap point H.
55:63	RO	constant = 0b000000000

Register Name	Transmit Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_BIT_MODE2_E_PL
Address	8004440D0601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	TX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the transmit per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b0000001 = TX PRBS tap point A. 0b1111100 = TX PRBS tap point B. 0b1111011 = TX PRBS tap point C. 0b0001100 = TX PRBS tap points D and G. 0b1011110 = TX PRBS tap point E. 0b0010000 = TX PRBS tap point F, and TX half-width tap point A. 0b1001110 = TX PRBS tap point H, and TX half-width tap point B. 0b0111101 = TX half-width PRBS tap point C. 0b1000110 = TX half-width PRBS tap points D and G. 0b1101111 = TX half-width PRBS tap point E. 0b0001000 = TX half-width PRBS tap point F. 0b1100111 = TX half-width PRBS tap point H.
55:63	RO	constant = 0b000000000

Register Name	Transmit Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_BIT_MODE2_E_PL
Address	8004440E0601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	TX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the transmit per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b0000001 = TX PRBS tap point A. 0b1111100 = TX PRBS tap point B. 0b1111011 = TX PRBS tap point C. 0b0001100 = TX PRBS tap points D and G. 0b1011110 = TX PRBS tap point E. 0b0010000 = TX PRBS tap point F, and TX half-width tap point A. 0b1001110 = TX PRBS tap point H, and TX half-width tap point B. 0b0111101 = TX half-width PRBS tap point C. 0b1000110 = TX half-width PRBS tap points D and G. 0b1101111 = TX half-width PRBS tap point E. 0b0001000 = TX half-width PRBS tap point F. 0b1100111 = TX half-width PRBS tap point H.
55:63	RO	constant = 0b000000000

Register Name	Transmit Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_BIT_MODE2_E_PL
Address	8004440F0601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	TX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the transmit per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b0000001 = TX PRBS tap point A. 0b1111100 = TX PRBS tap point B. 0b1111011 = TX PRBS tap point C. 0b0001100 = TX PRBS tap points D and G. 0b1011110 = TX PRBS tap point E. 0b0010000 = TX PRBS tap point F, and TX half-width tap point A. 0b1001110 = TX PRBS tap point H, and TX half-width tap point B. 0b0111101 = TX half-width PRBS tap point C. 0b1000110 = TX half-width PRBS tap points D and G. 0b1101111 = TX half-width PRBS tap point E. 0b0001000 = TX half-width PRBS tap point F. 0b1100111 = TX half-width PRBS tap point H.
55:63	RO	constant = 0b000000000

Register Name	Transmit Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#4.DD.TX_BIT_REGS.TX_BIT_MODE2_E_PL
Address	800444100601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	TX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the transmit per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b0000001 = TX PRBS tap point A. 0b1111100 = TX PRBS tap point B. 0b1111011 = TX PRBS tap point C. 0b0001100 = TX PRBS tap points D and G. 0b1011110 = TX PRBS tap point E. 0b0010000 = TX PRBS tap point F, and TX half-width tap point A. 0b1001110 = TX PRBS tap point H, and TX half-width tap point B. 0b0111101 = TX half-width PRBS tap point C. 0b1000110 = TX half-width PRBS tap points D and G. 0b1101111 = TX half-width PRBS tap point E. 0b0001000 = TX half-width PRBS tap point F. 0b1100111 = TX half-width PRBS tap point H.
55:63	RO	constant = 0b000000000

Register Name	Transmit Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#0.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_BIT_MODE2_E_PL
Address	800444200601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	TX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the transmit per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b0000001 = TX PRBS tap point A. 0b1111100 = TX PRBS tap point B. 0b1111011 = TX PRBS tap point C. 0b0001100 = TX PRBS tap points D and G. 0b1011110 = TX PRBS tap point E. 0b0010000 = TX PRBS tap point F, and TX half-width tap point A. 0b1001110 = TX PRBS tap point H, and TX half-width tap point B. 0b0111101 = TX half-width PRBS tap point C. 0b1000110 = TX half-width PRBS tap points D and G. 0b1101111 = TX half-width PRBS tap point E. 0b0001000 = TX half-width PRBS tap point F. 0b1100111 = TX half-width PRBS tap point H.
55:63	RO	constant = 0b000000000

Register Name	Transmit Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#0.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_BIT_MODE2_E_PL
Address	800444210601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	TX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the transmit per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b0000001 = TX PRBS tap point A. 0b1111100 = TX PRBS tap point B. 0b1111011 = TX PRBS tap point C. 0b0001100 = TX PRBS tap points D and G. 0b1011110 = TX PRBS tap point E. 0b0010000 = TX PRBS tap point F, and TX half-width tap point A. 0b1001110 = TX PRBS tap point H, and TX half-width tap point B. 0b0111101 = TX half-width PRBS tap point C. 0b1000110 = TX half-width PRBS tap points D and G. 0b1101111 = TX half-width PRBS tap point E. 0b0001000 = TX half-width PRBS tap point F. 0b1100111 = TX half-width PRBS tap point H.
55:63	RO	constant = 0b000000000

Register Name	Transmit Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#0.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_BIT_MODE2_E_PL
Address	800444220601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	TX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the transmit per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b0000001 = TX PRBS tap point A. 0b1111100 = TX PRBS tap point B. 0b1111011 = TX PRBS tap point C. 0b0001100 = TX PRBS tap points D and G. 0b1011110 = TX PRBS tap point E. 0b0010000 = TX PRBS tap point F, and TX half-width tap point A. 0b1001110 = TX PRBS tap point H, and TX half-width tap point B. 0b0111101 = TX half-width PRBS tap point C. 0b1000110 = TX half-width PRBS tap points D and G. 0b1101111 = TX half-width PRBS tap point E. 0b0001000 = TX half-width PRBS tap point F. 0b1100111 = TX half-width PRBS tap point H.
55:63	RO	constant = 0b000000000

Register Name	Transmit Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#0.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_BIT_MODE2_E_PL
Address	800444230601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	TX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the transmit per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b0000001 = TX PRBS tap point A. 0b1111100 = TX PRBS tap point B. 0b1111011 = TX PRBS tap point C. 0b0001100 = TX PRBS tap points D and G. 0b1011110 = TX PRBS tap point E. 0b0010000 = TX PRBS tap point F, and TX half-width tap point A. 0b1001110 = TX PRBS tap point H, and TX half-width tap point B. 0b0111101 = TX half-width PRBS tap point C. 0b1000110 = TX half-width PRBS tap points D and G. 0b1101111 = TX half-width PRBS tap point E. 0b0001000 = TX half-width PRBS tap point F. 0b1100111 = TX half-width PRBS tap point H.
55:63	RO	constant = 0b000000000

Register Name	Transmit Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#1.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_BIT_MODE2_E_PL
Address	800444240601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	TX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the transmit per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b0000001 = TX PRBS tap point A. 0b1111100 = TX PRBS tap point B. 0b1111011 = TX PRBS tap point C. 0b0001100 = TX PRBS tap points D and G. 0b1011110 = TX PRBS tap point E. 0b0010000 = TX PRBS tap point F, and TX half-width tap point A. 0b1001110 = TX PRBS tap point H, and TX half-width tap point B. 0b0111101 = TX half-width PRBS tap point C. 0b1000110 = TX half-width PRBS tap points D and G. 0b1101111 = TX half-width PRBS tap point E. 0b0001000 = TX half-width PRBS tap point F. 0b1100111 = TX half-width PRBS tap point H.
55:63	RO	constant = 0b000000000

Register Name	Transmit Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#1.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_BIT_MODE2_E_PL
Address	800444250601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	TX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the transmit per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b0000001 = TX PRBS tap point A. 0b1111100 = TX PRBS tap point B. 0b1111011 = TX PRBS tap point C. 0b0001100 = TX PRBS tap points D and G. 0b1011110 = TX PRBS tap point E. 0b0010000 = TX PRBS tap point F, and TX half-width tap point A. 0b1001110 = TX PRBS tap point H, and TX half-width tap point B. 0b0111101 = TX half-width PRBS tap point C. 0b1000110 = TX half-width PRBS tap points D and G. 0b1101111 = TX half-width PRBS tap point E. 0b0001000 = TX half-width PRBS tap point F. 0b1100111 = TX half-width PRBS tap point H.
55:63	RO	constant = 0b000000000

Register Name	Transmit Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#1.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_BIT_MODE2_E_PL
Address	800444260601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	TX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the transmit per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b0000001 = TX PRBS tap point A. 0b1111100 = TX PRBS tap point B. 0b1111011 = TX PRBS tap point C. 0b0001100 = TX PRBS tap points D and G. 0b1011110 = TX PRBS tap point E. 0b0010000 = TX PRBS tap point F, and TX half-width tap point A. 0b1001110 = TX PRBS tap point H, and TX half-width tap point B. 0b0111101 = TX half-width PRBS tap point C. 0b1000110 = TX half-width PRBS tap points D and G. 0b1101111 = TX half-width PRBS tap point E. 0b0001000 = TX half-width PRBS tap point F. 0b1100111 = TX half-width PRBS tap point H.
55:63	RO	constant = 0b000000000

Register Name	Transmit Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#1.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_BIT_MODE2_E_PL
Address	800444270601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	TX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the transmit per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b0000001 = TX PRBS tap point A. 0b1111100 = TX PRBS tap point B. 0b1111011 = TX PRBS tap point C. 0b0001100 = TX PRBS tap points D and G. 0b1011110 = TX PRBS tap point E. 0b0010000 = TX PRBS tap point F, and TX half-width tap point A. 0b1001110 = TX PRBS tap point H, and TX half-width tap point B. 0b0111101 = TX half-width PRBS tap point C. 0b1000110 = TX half-width PRBS tap points D and G. 0b1101111 = TX half-width PRBS tap point E. 0b0001000 = TX half-width PRBS tap point F. 0b1100111 = TX half-width PRBS tap point H.
55:63	RO	constant = 0b000000000

Register Name	Transmit Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_BIT_MODE2_E_PL
Address	800444280601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	TX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the transmit per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b0000001 = TX PRBS tap point A. 0b1111100 = TX PRBS tap point B. 0b1111011 = TX PRBS tap point C. 0b0001100 = TX PRBS tap points D and G. 0b1011110 = TX PRBS tap point E. 0b0010000 = TX PRBS tap point F, and TX half-width tap point A. 0b1001110 = TX PRBS tap point H, and TX half-width tap point B. 0b0111101 = TX half-width PRBS tap point C. 0b1000110 = TX half-width PRBS tap points D and G. 0b1101111 = TX half-width PRBS tap point E. 0b0001000 = TX half-width PRBS tap point F. 0b1100111 = TX half-width PRBS tap point H.
55:63	RO	constant = 0b000000000

Register Name	Transmit Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_BIT_MODE2_E_PL
Address	800444290601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	TX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the transmit per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b0000001 = TX PRBS tap point A. 0b1111100 = TX PRBS tap point B. 0b1111011 = TX PRBS tap point C. 0b0001100 = TX PRBS tap points D and G. 0b1011110 = TX PRBS tap point E. 0b0010000 = TX PRBS tap point F, and TX half-width tap point A. 0b1001110 = TX PRBS tap point H, and TX half-width tap point B. 0b0111101 = TX half-width PRBS tap point C. 0b1000110 = TX half-width PRBS tap points D and G. 0b1101111 = TX half-width PRBS tap point E. 0b0001000 = TX half-width PRBS tap point F. 0b1100111 = TX half-width PRBS tap point H.
55:63	RO	constant = 0b000000000

Register Name	Transmit Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_BIT_MODE2_E_PL
Address	8004442A0601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	TX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the transmit per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b0000001 = TX PRBS tap point A. 0b1111100 = TX PRBS tap point B. 0b1111011 = TX PRBS tap point C. 0b0001100 = TX PRBS tap points D and G. 0b1011110 = TX PRBS tap point E. 0b0010000 = TX PRBS tap point F, and TX half-width tap point A. 0b1001110 = TX PRBS tap point H, and TX half-width tap point B. 0b0111101 = TX half-width PRBS tap point C. 0b1000110 = TX half-width PRBS tap points D and G. 0b1101111 = TX half-width PRBS tap point E. 0b0001000 = TX half-width PRBS tap point F. 0b1100111 = TX half-width PRBS tap point H.
55:63	RO	constant = 0b000000000

Register Name	Transmit Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_BIT_MODE2_E_PL
Address	8004442B0601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	TX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the transmit per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b0000001 = TX PRBS tap point A. 0b1111100 = TX PRBS tap point B. 0b1111011 = TX PRBS tap point C. 0b0001100 = TX PRBS tap points D and G. 0b1011110 = TX PRBS tap point E. 0b0010000 = TX PRBS tap point F, and TX half-width tap point A. 0b1001110 = TX PRBS tap point H, and TX half-width tap point B. 0b0111101 = TX half-width PRBS tap point C. 0b1000110 = TX half-width PRBS tap points D and G. 0b1101111 = TX half-width PRBS tap point E. 0b0001000 = TX half-width PRBS tap point F. 0b1100111 = TX half-width PRBS tap point H.
55:63	RO	constant = 0b000000000

Register Name	Transmit Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_BIT_MODE2_E_PL
Address	8004442C0601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	TX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the transmit per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b0000001 = TX PRBS tap point A. 0b1111100 = TX PRBS tap point B. 0b1111011 = TX PRBS tap point C. 0b0001100 = TX PRBS tap points D and G. 0b1011110 = TX PRBS tap point E. 0b0010000 = TX PRBS tap point F, and TX half-width tap point A. 0b1001110 = TX PRBS tap point H, and TX half-width tap point B. 0b0111101 = TX half-width PRBS tap point C. 0b1000110 = TX half-width PRBS tap points D and G. 0b1101111 = TX half-width PRBS tap point E. 0b0001000 = TX half-width PRBS tap point F. 0b1100111 = TX half-width PRBS tap point H.
55:63	RO	constant = 0b000000000

Register Name	Transmit Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_BIT_MODE2_E_PL
Address	8004442D0601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	TX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the transmit per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b0000001 = TX PRBS tap point A. 0b1111100 = TX PRBS tap point B. 0b1111011 = TX PRBS tap point C. 0b0001100 = TX PRBS tap points D and G. 0b1011110 = TX PRBS tap point E. 0b0010000 = TX PRBS tap point F, and TX half-width tap point A. 0b1001110 = TX PRBS tap point H, and TX half-width tap point B. 0b0111101 = TX half-width PRBS tap point C. 0b1000110 = TX half-width PRBS tap points D and G. 0b1101111 = TX half-width PRBS tap point E. 0b0001000 = TX half-width PRBS tap point F. 0b1100111 = TX half-width PRBS tap point H.
55:63	RO	constant = 0b000000000

Register Name	Transmit Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_BIT_MODE2_E_PL
Address	8004442E0601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	TX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the transmit per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b0000001 = TX PRBS tap point A. 0b1111100 = TX PRBS tap point B. 0b1111011 = TX PRBS tap point C. 0b0001100 = TX PRBS tap points D and G. 0b1011110 = TX PRBS tap point E. 0b0010000 = TX PRBS tap point F, and TX half-width tap point A. 0b1001110 = TX PRBS tap point H, and TX half-width tap point B. 0b0111101 = TX half-width PRBS tap point C. 0b1000110 = TX half-width PRBS tap points D and G. 0b1101111 = TX half-width PRBS tap point E. 0b0001000 = TX half-width PRBS tap point F. 0b1100111 = TX half-width PRBS tap point H.
55:63	RO	constant = 0b000000000

Register Name	Transmit Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_BIT_MODE2_E_PL
Address	8004442F0601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	TX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the transmit per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b0000001 = TX PRBS tap point A. 0b1111100 = TX PRBS tap point B. 0b1111011 = TX PRBS tap point C. 0b0001100 = TX PRBS tap points D and G. 0b1011110 = TX PRBS tap point E. 0b0010000 = TX PRBS tap point F, and TX half-width tap point A. 0b1001110 = TX PRBS tap point H, and TX half-width tap point B. 0b0111101 = TX half-width PRBS tap point C. 0b1000110 = TX half-width PRBS tap points D and G. 0b1101111 = TX half-width PRBS tap point E. 0b0001000 = TX half-width PRBS tap point F. 0b1100111 = TX half-width PRBS tap point H.
55:63	RO	constant = 0b000000000

Register Name	Transmit Bit Mode 2 E Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#4.DD.TX_BIT_REGS.TX_BIT_MODE2_E_PL
Address	800444300601143F (SCOM)
Description	This register contains the second set of E mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	TX_PRBS_SEED_VALUE_16_22: This field contains the least-significant bits of the transmit per-lane PRBS seed value. For more information, see the rx_prbs_seed_value_0_15 register. 0b0000001 = TX PRBS tap point A. 0b1111100 = TX PRBS tap point B. 0b1111011 = TX PRBS tap point C. 0b0001100 = TX PRBS tap points D and G. 0b1011110 = TX PRBS tap point E. 0b0010000 = TX PRBS tap point F, and TX half-width tap point A. 0b1001110 = TX PRBS tap point H, and TX half-width tap point B. 0b0111101 = TX half-width PRBS tap point C. 0b1000110 = TX half-width PRBS tap points D and G. 0b1101111 = TX half-width PRBS tap point E. 0b0001000 = TX half-width PRBS tap point F. 0b1100111 = TX half-width PRBS tap point H.
55:63	RO	constant = 0b000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	800454000601143F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	800454010601143F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	800454020601143F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.

Bits	SCOM	Field Mnemonic: Description
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#0.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	800454030601143F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#1.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	800454040601143F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#1.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	800454050601143F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#1.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	800454060601143F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#1.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	800454070601143F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#2.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	800454080601143F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#2.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	800454090601143F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#2.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	8004540A0601143F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#2.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	8004540B0601143F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	8004540C0601143F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	8004540D0601143F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	8004540E0601143F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	8004540F0601143F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX0.TXPACKS#3.TXPACK.DD.SLICE#4.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	800454100601143F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#0.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	800454200601143F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#0.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	800454210601143F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#0.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	800454220601143F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#0.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	800454230601143F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#1.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	800454240601143F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#1.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	800454250601143F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#1.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	800454260601143F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#1.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	800454270601143F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	800454280601143F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	800454290601143F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	8004542A0601143F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#2.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	8004542B0601143F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	8004542C0601143F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	8004542D0601143F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	8004542E0601143F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	8004542F0601143F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOF2.TX_WRAP.TX1.TXPACKS#3.TXPACK.DD.SLICE#4.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	800454300601143F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Receive Spare Mode Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_SPARE_MODE_PG
Address	800800000601143F (SCOM)
Description	This register contains per-group spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PG_SPARE_MODE_0: Per-group spare mode latch.
49	RWX	RX_PG_SPARE_MODE_1: Per-group spare mode latch.
50	RWX	RX_PG_SPARE_MODE_2: Per-group spare mode latch.
51	RWX	RX_PG_SPARE_MODE_3: Per-group spare mode latch.
52	RWX	RX_PG_SPARE_MODE_4: This debug switch prevents the rx_sls_hndshk_state state machine and the rx_dyn_recal_hndshk_state state machine from ever being allowed to run at the same time. Setting this bit turns this feature off.
53:63	RO	constant = 0b00000000000

Register Name	Receive Spare Mode Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_SPARE_MODE_PG
Address	800800200601143F (SCOM)
Description	This register contains per-group spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PG_SPARE_MODE_0: Per-group spare mode latch.
49	RWX	RX_PG_SPARE_MODE_1: Per-group spare mode latch.
50	RWX	RX_PG_SPARE_MODE_2: Per-group spare mode latch.
51	RWX	RX_PG_SPARE_MODE_3: Per-group spare mode latch.
52	RWX	RX_PG_SPARE_MODE_4: This debug switch prevents the rx_sls_hndshk_state state machine and the rx_dyn_recal_hndshk_state state machine from ever being allowed to run at the same time. Setting this bit turns this feature off.
53:63	RO	constant = 0b00000000000

Register Name	Receive ID1 Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_ID1_PG
Address	800808000601143F (SCOM)
Description	This register is used to set the bus number of a clock group.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_BUS_ID: This field is used to programmatically set the bus number that a clock group belongs to.
54:63	RO	constant = 0b0000000000

Register Name	Receive ID1 Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_ID1_PG
Address	800808200601143F (SCOM)
Description	This register is used to set the bus number of a clock group.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_BUS_ID: This field is used to programmatically set the bus number that a clock group belongs to.
54:63	RO	constant = 0b0000000000

Register Name	Receive CTL Mode 1 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE1_EO_PG
Address	800810000601143F (SCOM)
Description	This register contains the first set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CLKDIST_PDWN: This field is used to disable the receive group clocks and put them into a low-power state.
49:50	RO	constant = 0b00
51:56	RWX	RX_BIST_MIN_EYE_WIDTH: Receive BIST minimum eye width. This field sets the minimum eye width value, in phase-rotator steps, that is considered acceptable in order to pass.
57	RWX	RX_A_BIST_EN: BIST enable pin.
58:63	RO	constant = 0b000000

Register Name	Receive CTL Mode 1 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE1_EO_PG
Address	800810200601143F (SCOM)
Description	This register contains the first set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CLKDIST_PDWN: This field is used to disable the receive group clocks and put them into a low-power state.
49:50	RO	constant = 0b00
51:56	RWX	RX_BIST_MIN_EYE_WIDTH: Receive BIST minimum eye width. This field sets the minimum eye width value, in phase-rotator steps, that is considered acceptable in order to pass.
57	RWX	RX_A_BIST_EN: BIST enable pin.
58:63	RO	constant = 0b000000

Register Name	Receive CTL Mode 2 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE2_EO_PG
Address	800818000601143F (SCOM)
Description	This register contains the second set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RWX	RX_DFE_CA_CFG: Receive DFE clock adjustment settings. This 2-bit field contains an encoded value for K as follows: \n00 = 8 \n01 = 10 \n10 = 12 \n11 = 14 Lab testing is required to determine the proper value of K.
50:53	RWX	RX_SCOPE_CONTROL: This 4-bit value indicates which scope bit is being captured. Valid values are 0 - 9.
54:59	RO	constant = 0b000000
60	RWX	RX_DATA_PIPE_CLR_ON_READ_MODE: This bit sets the data pipe capture on read mode. When set, reading rx_data_pipe_16_31 automatically captures new data. Otherwise, rx_data_pipe_capture must be written.
61:63	RO	constant = 0b000

Register Name	**Receive CTL Mode 2 EO Per-Group Register**
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE2_EO_PG
Address	800818200601143F (SCOM)
Description	This register contains the second set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_DFE_CA_CFG: Receive DFE clock adjustment settings. This 2-bit field contains an encoded value for K as follows: \n00 = 8 \n01 = 10 \n10 = 12 \n11 = 14 Lab testing is required to determine the proper value of K.
50:53	RWX	RX_SCOPE_CONTROL: This 4-bit value indicates which scope bit is being captured. Valid values are 0 - 9.
54:59	RO	constant = 0b000000
60	RWX	RX_DATA_PIPE_CLR_ON_READ_MODE: This bit sets the data pipe capture on read mode. When set, reading rx_data_pipe_16_31 automatically captures new data. Otherwise, rx_data_pipe_capture must be written.
61:63	RO	constant = 0b000

Register Name	**Receive CTL Mode 3 EO Per-Group Register**
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE3_EO_PG
Address	800820000601143F (SCOM)
Description	This register contains the third set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_SERVO_THRESH3: This field contains the threshold used to end DFE servo operations early.
52:53	RWX	RX_DFE_HTAP_CFG: This field contains the multiplier used when running H2 - H12 operations.
54:57	RWX	RX_DFE_INIT_TIMEOUT: This field contains the timeout for DFE 2 - 12 operations during initialization.

Bits	SCOM	Field Mnemonic: Description
58:61	RWX	RX_DFE_RECAL_TIMEOUT: This field contains the timeout for DFE 2 - 12 operations during recalibration.
62:63	RO	constant = 0b00

Register Name	Receive CTL Mode 3 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE3_EO_PG
Address	800820200601143F (SCOM)
Description	This register contains the third set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_SERVO_THRESH3: This field contains the threshold used to end DFE servo operations early.
52:53	RWX	RX_DFE_HTAP_CFG: This field contains the multiplier used when running H2 - H12 operations.
54:57	RWX	RX_DFE_INIT_TIMEOUT: This field contains the timeout for DFE 2 - 12 operations during initialization.
58:61	RWX	RX_DFE_RECAL_TIMEOUT: This field contains the timeout for DFE 2 - 12 operations during recalibration.
62:63	RO	constant = 0b00

Register Name	Receive CTL Mode 4 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE4_EO_PG
Address	800828000601143F (SCOM)
Description	This register contains the fourth set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_DISABLE_2TO12_CLEAR: This bit connects a configuration bit to disable the clear function when running the h1a_ratio cal.
49	RWX	RX_PEAK_ENABLE_DAC_CFG: This bit connects to a configuration bit so that the DAC can be disabled during peaking.
50	RWX	RX_AMIN_ENABLE_HDAC: This bit enables hDACs during amin measurements.
51	RWX	RX_USE_PREV_COARSE_VAL: This bit selects reading the previous integ coarse value as a starting point.
52:63	RO	constant = 0b000000000000

Register Name	Receive CTL Mode 4 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE4_EO_PG
Address	800828200601143F (SCOM)
Description	This register contains the fourth set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_DISABLE_2TO12_CLEAR: This bit connects a configuration bit to disable the clear function when running the h1a_ratio cal.

Bits	SCOM	Field Mnemonic: Description
49	RWX	RX_PEAK_ENABLE_DAC_CFG: This bit connects to a configuration bit so that the DAC can be disabled during peaking.
50	RWX	RX_AMIN_ENABLE_HDAC: This bit enables hDACs during amin measurements.
51	RWX	RX_USE_PREV_COARSE_VAL: This bit selects reading the previous integ coarse value as a starting point.
52:63	RO	constant = 0b000000000000

Register Name	Receive CTL Mode 5 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE5_EO_PG
Address	800830000601143F (SCOM)
Description	This register contains the fifth set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:50	RO	constant = 0b000000000000000000000000000000000000000000000000000
51:53	RWX	RX_DYN_RECAL_INTERVAL_TIMEOUT_SEL: Receive dynamic recalibration interval timeout selects. This timeout determines the time between status reporting timeouts. The actual time of sending a message is selected with rx_dyn_recal_status_rpt_timeout_sel. 0b000 = 1024 UI or 106.5 ns. 0b001 = 16k UI or 1.7 µs. 0b010 = 32k UI or 3.4 µs. 0b011 = 64k UI or 6.8 µs. 0b100 = 128k UI or 13.6 µs. 0b101 = 256k UI or 27.3 µs. 0b110 = 8192k UI or 872.4 µs. 0b111 = infinite.
54:55	RWX	RX_DYN_RECAL_STATUS_RPT_TIMEOUT_SEL: Receive dynamic recalibration status reporting timeout selects. This timeout determines the time that a status reporting timeout lasts. The first 1/4 is a blank period, the middle 1/2 is the command message, and the last 1/4 is another blank period. The time between messages is selected with rx_dyn_recal_interval_timeout_sel. 0B00 = 512 UI or 53.2 ns. 0B01 = 1024 UI or 106.5 ns. 0B10 = 2048 UI or 212.9 ns. 0B11 = 4096 UI or 426.0 ns.
56:59	RWX	RX_TRACKING_TIMEOUT_SEL: This field sets the time to wait for phase tracking to lock on the edge before proceeding in the state machine.
60:63	RWX	RX_PUP_LITE_WAIT_SEL: This field sets the time to wait for analog logic to power up an unused spare lane for recalibration and repair.

Register Name	Receive CTL Mode 5 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE5_EO_PG
Address	800830200601143F (SCOM)
Description	This register contains the fifth set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:50	RO	constant = 0b000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
51:53	RWX	RX_DYN_RECAL_INTERVAL_TIMEOUT_SEL: Receive dynamic recalibration interval timeout selects. This timeout determines the time between status reporting timeouts. The actual time of sending a message is selected with rx_dyn_recal_status_rpt_timeout_sel. 0b000 = 1024 UI or 106.5 ns. 0b001 = 16k UI or 1.7 μs. 0b010 = 32k UI or 3.4 μs. 0b011 = 64k UI or 6.8 μs. 0b100 = 128k UI or 13.6 μs. 0b101 = 256k UI or 27.3 μs. 0b110 = 8192k UI or 872.4 μs. 0b111 = infinite.
54:55	RWX	RX_DYN_RECAL_STATUS_RPT_TIMEOUT_SEL: Receive dynamic recalibration status reporting timeout selects. This timeout determines the time that a status reporting timeout lasts. The first 1/4 is a blank period, the middle 1/2 is the command message, and the last 1/4 is another blank period. The time between messages is selected with rx_dyn_recal_interval_timeout_sel. 0B00 = 512 UI or 53.2 ns. 0B01 = 1024 UI or 106.5 ns. 0B10 = 2048 UI or 212.9 ns. 0B11 = 4096 UI or 426.0 ns
56:59	RWX	RX_TRACKING_TIMEOUT_SEL: This field sets the time to wait for phase tracking to lock on the edge before proceeding in the state machine.
60:63	RWX	RX_PUP_LITE_WAIT_SEL: This field sets the time to wait for analog logic to power up an unused spare lane for recalibration and repair.

Register Name	Receive CTL Mode 6 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE6_EO_PG
Address	800838000601143F (SCOM)
Description	This register contains the sixth set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_EO_CONVERGED_END_COUNT: This field contains the end value of the receive eye-optimization convergence counter. This value represents the number of times through the vga + CTLE peaking substeps before giving up.
52:53	RWX	RX_HIST_MIN_EYE_WIDTH_MODE: This field indicates the receive historic eye width and height minimum measurement mode.
54:55	RWX	RX_HIST_MIN_EYE_HEIGHT_MODE: Receive historic eye-height minimum measurement mode. This field is inoperative on POWER8 processor with NVLink technology hardware. Use the rx_hist_min_eye_width_mode control instead. Set both the width and height_mode controls to the same value in test routines to maintain compatibility.
56:59	RWX	RX_AMP_GAIN_CNT_MAX: This field indicates the maximum number of attempts to adjust VGA gain before doing a peaking operation.
60:63	RO	constant = 0b0000

Register Name	Receive CTL Mode 6 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE6_EO_PG
Address	800838200601143F (SCOM)
Description	This register contains the sixth set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_EO_CONVERGED_END_COUNT: This field contains the end value of the receive eye-optimization convergence counter. This value represents the number of times through the vga + CTLE peaking substeps before giving up.
52:53	RWX	RX_HIST_MIN_EYE_WIDTH_MODE: This field indicates the receive historic eye width and height minimum measurement mode.
54:55	RWX	RX_HIST_MIN_EYE_HEIGHT_MODE: Receive historic eye-height minimum measurement mode. This field is inoperative on POWER8 processor with NVLink technology hardware. Use the rx_hist_min_eye_width_mode control instead. Set both the width and height_mode controls to the same value in test routines to maintain compatibility.
56:59	RWX	RX_AMP_GAIN_CNT_MAX: This field indicates the maximum number of attempts to adjust VGA gain before doing a peaking operation.
60:63	RO	constant = 0b0000

Register Name	Receive CTL Mode 7 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE7_EO_PG
Address	800840000601143F (SCOM)
Description	This register contains the seventh set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_ABORT_CHECK_TIMEOUT_SEL: This field selects the abort check timeout value.
52:55	RWX	RX_POLLING_TIMEOUT_SEL: This field selects the polling read timeout value.
56:59	RWX	RX_PSAVE_MODE_TIMEOUT_SEL: This field indicates how long to wait for analog logic to power up an unused spare lane for recalibration and repair.
60:63	RWX	RX_DYN_RECAL_OVERALL_TIMEOUT_SEL: This field contains the dynamic recalibration overall timeout selects.

Register Name	Receive CTL Mode 7 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE7_EO_PG
Address	800840200601143F (SCOM)
Description	This register contains the seventh set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_ABORT_CHECK_TIMEOUT_SEL: This field selects the abort check timeout value.
52:55	RWX	RX_POLLING_TIMEOUT_SEL: This field selects the polling read timeout value.
56:59	RWX	RX_PSAVE_MODE_TIMEOUT_SEL: This field indicates how long to wait for analog logic to power up an unused spare lane for recalibration and repair.
60:63	RWX	RX_DYN_RECAL_OVERALL_TIMEOUT_SEL: This field contains the dynamic recalibration overall timeout selects.

Register Name	Receive CTL Mode 8 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE8_EO_PG
Address	800848000601143F (SCOM)
Description	This register contains the eighth set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56:63	RWX	RX_MAX_BER_CHECK_COUNT: This field indicates the maximum acceptable number of bit errors allowable after recalibration.

Register Name	Receive CTL Mode 8 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE8_EO_PG
Address	800848200601143F (SCOM)
Description	This register contains the eighth set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56:63	RWX	RX_MAX_BER_CHECK_COUNT: This field indicates the maximum acceptable number of bit errors allowable after recalibration.

Register Name	Receive CTL Mode 9 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE9_EO_PG
Address	800850000601143F (SCOM)
Description	This register contains the ninth set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RX_MIN_EYE_WIDTH: This field indicates the minimum acceptable eye width used during initial or recalibration results checking. (EDI or EI4).
56:63	RWX	RX_MIN_EYE_HEIGHT: This field indicates the minimum acceptable eye height used during initial or recalibration results checking. (EDI only).

Register Name	Receive CTL Mode 9 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE9_EO_PG
Address	800850200601143F (SCOM)
Description	This register contains the ninth set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RX_MIN_EYE_WIDTH: This field indicates the minimum acceptable eye width used during initial or recalibration results checking. (EDI or EI4).
56:63	RWX	RX_MIN_EYE_HEIGHT: This field indicates the minimum acceptable eye height used during initial or recalibration results checking. (EDI only).

Register Name	Receive CTL Mode 10 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE10_EO_PG
Address	800858000601143F (SCOM)
Description	This register contains the tenth set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_AMP_INIT_CFG: This register controls the servo filter for amplitude measurements during initialization.
51:53	RWX	RX_AMP_RECAL_CFG: This register controls the servo filter for amplitude measurements during recalibration.
54:56	RWX	RX_PEAK_INIT_CFG: This register controls the servo filter for peaking during initialization.
57:59	RWX	RX_PEAK_RECAL_CFG: This register controls the servo filter for peaking during recalibration.
60:63	RWX	RX_AMP_CFG: This register controls the servo filter for rx_amp_0 and rx_amp_1 servo ops.

Register Name	Receive CTL Mode 10 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE10_EO_PG
Address	800858200601143F (SCOM)
Description	This register contains the tenth set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_AMP_INIT_CFG: This register controls the servo filter for amplitude measurements during initialization.
51:53	RWX	RX_AMP_RECAL_CFG: This register controls the servo filter for amplitude measurements during recalibration.
54:56	RWX	RX_PEAK_INIT_CFG: This register controls the servo filter for peaking during initialization.
57:59	RWX	RX_PEAK_RECAL_CFG: This register controls the servo filter for peaking during recalibration.
60:63	RWX	RX_AMP_CFG: This register controls the servo filter for rx_amp_0 and rx_amp_1 servo ops.

Register Name	Receive CTL Mode 11 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE11_EO_PG
Address	800860000601143F (SCOM)
Description	This register contains the 11th set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_OFF_INIT_CFG: This register controls the servo filter for offset measurements during initialization.
51:53	RWX	RX_OFF_RECAL_CFG: This register controls the servo filter for offset measurements during recalibration.
54:56	RWX	RX_CM_CFG: This register controls the servo during common-mode measurement.
57:59	RWX	RX_AMIN_CFG: This register controls the servo filtering used for amin measurements.

Bits	SCOM	Field Mnemonic: Description
60:63	RWX	RX_USERDEF_CFG: This register controls the servo filtering when running the user-defined servo operations.

Register Name	Receive CTL Mode 11 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE11_EO_PG
Address	800860200601143F (SCOM)
Description	This register contains the 11th set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_OFF_INIT_CFG: This register controls the servo filter for offset measurements during initialization.
51:53	RWX	RX_OFF_RECAL_CFG: This register controls the servo filter for offset measurements during recalibration.
54:56	RWX	RX_CM_CFG: This register controls the servo during common-mode measurement.
57:59	RWX	RX_AMIN_CFG: This register controls the servo filtering used for amin measurements.
60:63	RWX	RX_USERDEF_CFG: This register controls the servo filtering when running the user-defined servo operations.

Register Name	Receive CTL Mode 12 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE12_EO_PG
Address	800868000601143F (SCOM)
Description	This register contains the 12th set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_SERVO_CHG_CFG: This register controls the minimum acceptable changes of the accumulator for a valid servo operation. It is used to assure that we have reached a stable point.
52:54	RWX	RX_DAC_BO_CFG: This register controls the time of the DAC black out time.
55:56	RWX	RX_FILTER_MODE: Servo filter mode. 00 = Normal filter during the entire operation. 01 = Use the 1/4 - 1/2 mode. 10 = 1/8 - 1/4 mode. 11 = Automatic convergence detect mode.
57:58	RWX	RX_MISC_CFG: These are per-group receive miscellaneous configuration bits. Bit 0 is used to re-enable the progressive filter mode for peaking. Bit 1, when 1, enables the clearing of H1 during the amp0, amp1, and user-defined servo operations.
59	RWX	RX_DISABLE_H1_CLEAR: Per group. When set, this bit disables the clearing when running servo operations that typically clear and restore the H1 registers.
60:62	RWX	RX_VOFF_CFG: This is a per-group configuration register that is used for setting the filter value when running the VREF version of offset on edge latches.
63	RWX	RX_LOFF_AMP_EN: When set to 1, the amp DAC is enabled during the loff versions of local latch offset cancellation.

Register Name	Receive CTL Mode 12 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE12_EO_PG
Address	800868200601143F (SCOM)
Description	This register contains the 12th set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_SERVO_CHG_CFG: This register controls the minimum acceptable changes of the accumulator for a valid servo operation. It is used to assure that we have reached a stable point.
52:54	RWX	RX_DAC_BO_CFG: This register controls the time of the DAC black out time.
55:56	RWX	RX_FILTER_MODE: Servo filter mode. 00 = Normal filter during the entire operation. 01 = Use the 1/4 - 1/2 mode. 10 = 1/8 - 1/4 mode. 11 = Automatic convergence detect mode.
57:58	RWX	RX_MISC_CFG: These are per-group receive miscellaneous configuration bits. Bit 0 is used to re-enable the progressive filter mode for peaking. Bit 1, when 1, enables the clearing of H1 during the amp0, amp1, and user-defined servo operations.
59	RWX	RX_DISABLE_H1_CLEAR: Per group. When set, this bit disables the clearing when running servo operations that typically clear and restore the H1 registers.
60:62	RWX	RX_VOFF_CFG: This is a per-group configuration register that is used for setting the filter value when running the VREF version of offset on edge latches.
63	RWX	RX_LOFF_AMP_EN: When set to 1, the amp DAC is enabled during the loff versions of local latch offset cancellation.

Register Name	Receive CTL Mode 13 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE13_EO_PG
Address	800870000601143F (SCOM)
Description	This register contains the 13th set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant = 0b0000000000000000000000000000000000000000000000000
49:55	RWX	RX_CM_OFFSET_VAL: This field contains the value used to offset the amp DAC when running common mode.
56:59	RWX	RX_SERVO_THRESH1: This field contains the value used as a threshold of when to switch to normal filtering mode.
60:63	RWX	RX_SERVO_THRESH2: This field contains the value used as a threshold of when we think the servo has converged.

Register Name	Receive CTL Mode 13 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE13_EO_PG
Address	800870200601143F (SCOM)
Description	This register contains the 13th set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant = 0b0000000000000000000000000000000000000000000000000
49:55	RWX	RX_CM_OFFSET_VAL: This field contains the value used to offset the amp DAC when running common mode.
56:59	RWX	RX_SERVO_THRESH1: This field contains the value used as a threshold of when to switch to normal filtering mode.
60:63	RWX	RX_SERVO_THRESH2: This field contains the value used as a threshold of when we think the servo has converged.

Register Name	Receive CTL Mode 14 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE14_EO_PG
Address	800878000601143F (SCOM)
Description	This register contains the 14th set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_AMP_INIT_TIMEOUT: This field is used for amplitude measurements during initialization.
52:55	RWX	RX_AMP_RECAL_TIMEOUT: This field is used for amplitude measurements during recalibration.
56:59	RWX	RX_PEAK_INIT_TIMEOUT: This field is used for peaking measurements during initialization.
60:63	RWX	RX_PEAK_RECAL_TIMEOUT: This field is used for peaking measurements during recalibration

Register Name	Receive CTL Mode 14 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE14_EO_PG
Address	800878200601143F (SCOM)
Description	This register contains the 14th set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_AMP_INIT_TIMEOUT: This field is used for amplitude measurements during initialization.
52:55	RWX	RX_AMP_RECAL_TIMEOUT: This field is used for amplitude measurements during recalibration.
56:59	RWX	RX_PEAK_INIT_TIMEOUT: This field is used for peaking measurements during initialization.
60:63	RWX	RX_PEAK_RECAL_TIMEOUT: This field is used for peaking measurements during recalibration

Register Name	Receive CTL Mode 15 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE15_EO_PG
Address	800880000601143F (SCOM)
Description	This register contains the 15th set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_OFF_INIT_TIMEOUT: This field is used for offset measurements during initialization.

Bits	SCOM	Field Mnemonic: Description
52:55	RWX	RX_OFF_RECAL_TIMEOUT: This field is used for offset measurements during recalibration.
56:59	RWX	RX_CM_TIMEOUT: This field is used for common-mode measurements.
60:63	RWX	RX_AMIN_TIMEOUT: This field is used for Amin measurements.

Register Name	Receive CTL Mode 15 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE15_EO_PG
Address	800880200601143F (SCOM)
Description	This register contains the 15th set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_OFF_INIT_TIMEOUT: This field is used for offset measurements during initialization.
52:55	RWX	RX_OFF_RECAL_TIMEOUT: This field is used for offset measurements during recalibration.
56:59	RWX	RX_CM_TIMEOUT: This field is used for common-mode measurements.
60:63	RWX	RX_AMIN_TIMEOUT: This field is used for Amin measurements.

Register Name	Receive CTL Mode 16 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE16_EO_PG
Address	800888000601143F (SCOM)
Description	This register contains the 16th set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_AMP_TIMEOUT: This timeout is used when running the generic amplitude servo operations.
52:55	RWX	RX_USERDEF_TIMEOUT: This timeout is used when using the user-defined servo operations.
56:59	RWX	RX_BER_TIMEOUT: This timeout is used when making bit error measurements with a servo operation.
60:63	RWX	RX_SPARE4_TIMEOUT: This timeout is currently a spare.

Register Name	Receive CTL Mode 16 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE16_EO_PG
Address	800888200601143F (SCOM)
Description	This register contains the 16th set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_AMP_TIMEOUT: This timeout is used when running the generic amplitude servo operations.
52:55	RWX	RX_USERDEF_TIMEOUT: This timeout is used when using the user-defined servo operations.
56:59	RWX	RX_BER_TIMEOUT: This timeout is used when making bit error measurements with a servo operation.
60:63	RWX	RX_SPARE4_TIMEOUT: This timeout is currently a spare.

Register Name	Receive CTL Mode 17 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE17_EO_PG
Address	800890000601143F (SCOM)
Description	This register contains the 17th set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMAX_HIGH: This field contains the receive Amax high target in amplitude DAC steps (as measured by the 2Ap-Amin method). The default is d120.
56:63	RWX	RX_AMAX_LOW: This field contains the receive Amax low target in amplitude DAC steps (as measured by the 2Ap-Amin method). The default is d80.

Register Name	Receive CTL Mode 17 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE17_EO_PG
Address	800890200601143F (SCOM)
Description	This register contains the 17th set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMAX_HIGH: This field contains the receive Amax high target in amplitude DAC steps (as measured by the 2Ap-Amin method). The default is d120.
56:63	RWX	RX_AMAX_LOW: This field contains the receive Amax low target in amplitude DAC steps (as measured by the 2Ap-Amin method). The default is d80.

Register Name	Receive CTL Mode 18 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE18_EO_PG
Address	800898000601143F (SCOM)
Description	This register contains the 18th set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP0_FILTER_MASK: This register controls the filter and mask for the Amp_0 servo operations.
56:63	RWX	RX_AMP1_FILTER_MASK: This register controls the filter and mask for the Amp_1 servo operations.

Register Name	Receive CTL Mode 18 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE18_EO_PG
Address	800898200601143F (SCOM)
Description	This register contains the 18th set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RWX	RX_AMP0_FILTER_MASK: This register controls the filter and mask for the Amp_0 servo operations.
56:63	RWX	RX_AMP1_FILTER_MASK: This register controls the filter and mask for the Amp_1 servo operations.

Register Name	Receive CTL Mode 19 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE19_EO_PG
Address	8008A0000601143F (SCOM)
Description	This register contains the 19th set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_CTLE_GAIN_MAX: This field contains the receive CTLE (VGA) gain maximum allowable gain value.
52:55	RO	constant = 0b0000
56:63	RWX	RX_AMP_START_VAL: This field contains the receive amp start value, used when making amplitude measurements as the starting point.

Register Name	Receive CTL Mode 19 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE19_EO_PG
Address	8008A0200601143F (SCOM)
Description	This register contains the 19th set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_CTLE_GAIN_MAX: This field contains the receive CTLE (VGA) gain maximum allowable gain value.
52:55	RO	constant = 0b0000
56:63	RWX	RX_AMP_START_VAL: This field contains the receive amp start value, used when making amplitude measurements as the starting point.

Register Name	Receive CTL Mode 20 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE20_EO_PG
Address	8008A8000601143F (SCOM)
Description	This register contains the 20th set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_DFE_CONVERGED_CNT_MAX: This field contains the number of iterations through DFE H1 and kH1Ap adjustment before ending DFE, unless it is ended by the rx_ap110ap010_delta criteria being met.
52:55	RWX	RX_AP110_AP010_DELTA_MAX: This field contains the maximum delta between Apx110 and Apx010 measurements to end DFE H1 and kH1Ap adjustment, unless ended by dfe_converged_cnt_max.
56:63	RO	constant = 0b00000000

Register Name	Receive CTL Mode 20 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE20_EO_PG
Address	8008A8200601143F (SCOM)
Description	This register contains the 20th set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_DFE_CONVERGED_CNT_MAX: This field contains the number of iterations through DFE H1 and kH1Ap adjustment before ending DFE, unless it is ended by the rx_ap110ap010_delta criteria being met.
52:55	RWX	RX_AP110_AP010_DELTA_MAX: This field contains the maximum delta between Apx110 and Apx010 measurements to end DFE H1 and kH1Ap adjustment, unless ended by dfe_converged_cnt_max.
56:63	RO	constant = 0b00000000

Register Name	Receive CTL Mode 21 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE21_EO_PG
Address	8008B0000601143F (SCOM)
Description	This register contains the 21st set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_EO_ENABLE_INTEG_LATCH_OFFSET_CAL: This bit is the receive eye-optimization latch offset adjustment enable with an integrator-based disable.
49	RWX	RX_EO_ENABLE_CTLE_COARSE_CAL: This bit is the receive eye-optimization coarse CTLE/Peakin enable.
50	RWX	RX_EO_ENABLE_DAC_H1_CAL: This bit is the receive eye-optimization H! DAC calibration to reference.
51	RWX	RX_EO_ENABLE_VGA_CAL: This bit is the receive eye-optimization VGA gain and offset adjustment enable.
52	RWX	RX_EO_ENABLE_DFE_H1_CAL: This bit is the receive eye-optimization DFE H1 adjustment enable.
53	RWX	RX_EO_ENABLE_H1AP_TWEAK: This bit is the receive eye-optimization H1/AN PR adjust enable.
54	RWX	RX_EO_ENABLE_DDC: This bit is the receive eye-optimization dynamic data centering enable.
55	RWX	RX_EO_ENABLE_CM_COARSE_CAL: This bit is the receive eye-optimization common-mode coarse calibration enable.
56	RWX	RX_EO_ENABLE_CM_FINE_CAL: This bit is the receive eye-optimization common-mode fine calibration enable.
57	RWX	RX_EO_ENABLE_BER_TEST: This bit is the receive eye-optimization bit-error-rate test enable.
58	RWX	RX_EO_ENABLE_RESULT_CHECK: This bit is the receive eye-optimization final results check enable.
59	RWX	RX_EO_ENABLE_CTLE_EDGE_TRACK_ONLY: This bit is the receive eye-optimization CTLE/Peakin enable with edge tracking only.
60	RWX	RX_EO_ENABLE_DFE_H2_H12_CAL: This bit is the receive eye-optimization DFE H2-to-H12 calibration enable.
61	RWX	RX_EO_ENABLE_DAC_H1_TO_A_CAL: This bit is used for receive eye-optimization H! DAC-to-amplitude DAC cross-calibration.
62	RWX	RX_EO_ENABLE_FINAL_L2U_ADJ: This bit is the receive eye-optimization final receive FIFO load-to-unload delay adjustment enable.

Bits	SCOM	Field Mnemonic: Description
63	RWX	RX_EO_ENABLE_DONE_SIGNALING: This bit is the receive eye-optimization “eye-optimization done” signaling enable.

Register Name	Receive CTL Mode 21 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE21_EO_PG
Address	8008B0200601143F (SCOM)
Description	This register contains the 21st set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_EO_ENABLE_INTEG_LATCH_OFFSET_CAL: This bit is the receive eye-optimization latch offset adjustment enable with an integrator-based disable.
49	RWX	RX_EO_ENABLE_CTLE_COARSE_CAL: This bit is the receive eye-optimization coarse CTLE/Peakin enable.
50	RWX	RX_EO_ENABLE_DAC_H1_CAL: This bit is the receive eye-optimization H! DAC calibration to reference.
51	RWX	RX_EO_ENABLE_VGA_CAL: This bit is the receive eye-optimization VGA gain and offset adjustment enable.
52	RWX	RX_EO_ENABLE_DFE_H1_CAL: This bit is the receive eye-optimization DFE H1 adjustment enable.
53	RWX	RX_EO_ENABLE_H1AP_TWEAK: This bit is the receive eye-optimization H1/AN PR adjust enable.
54	RWX	RX_EO_ENABLE_DDC: This bit is the receive eye-optimization dynamic data centering enable.
55	RWX	RX_EO_ENABLE_CM_COARSE_CAL: This bit is the receive eye-optimization common-mode coarse calibration enable.
56	RWX	RX_EO_ENABLE_CM_FINE_CAL: This bit is the receive eye-optimization common-mode fine calibration enable.
57	RWX	RX_EO_ENABLE_BER_TEST: This bit is the receive eye-optimization bit-error-rate test enable.
58	RWX	RX_EO_ENABLE_RESULT_CHECK: This bit is the receive eye-optimization final results check enable.
59	RWX	RX_EO_ENABLE_CTLE_EDGE_TRACK_ONLY: This bit is the receive eye-optimization CTLE/Peakin enable with edge tracking only.
60	RWX	RX_EO_ENABLE_DFE_H2_H12_CAL: This bit is the receive eye-optimization DFE H2-to-H12 calibration enable.
61	RWX	RX_EO_ENABLE_DAC_H1_TO_A_CAL: This bit is used for receive eye-optimization H! DAC-to-amplitude DAC cross-calibration.
62	RWX	RX_EO_ENABLE_FINAL_L2U_ADJ: This bit is the receive eye-optimization final receive FIFO load-to-unload delay adjustment enable.
63	RWX	RX_EO_ENABLE_DONE_SIGNALING: This bit is the receive eye-optimization “eye-optimization done” signaling enable.

Register Name	Receive CTL Mode 22 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE22_EO_PG
Address	8008B8000601143F (SCOM)
Description	This register contains the 22nd set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_RC_ENABLE_INTEG_LATCH_OFFSET_CAL: This bit is the receive recalibration latch offset adjustment enable with integrator-based disable.
49	RWX	RX_RC_ENABLE_CTLE_COARSE_CAL: This bit is the receive recalibration coarse CTLE/Peakin enable.
50	RWX	RX_RC_ENABLE_DAC_H1_CAL: This bit is the receive recalibration H! DAC calibration to reference enable.
51	RWX	RX_RC_ENABLE_VGA_CAL: This bit is the receive recalibration VGA gain and offset adjustment enable.
52	RWX	RX_RC_ENABLE_DFE_H1_CAL: This bit is the receive recalibration DFE H1 adjustment enable.
53	RWX	RX_RC_ENABLE_H1AP_TWEAK: This bit is the receive recalibration H1/AN PR adjustment enable.
54	RWX	RX_RC_ENABLE_DDC: This bit is the receive recalibration dynamic data-centering enable.
55	RWX	RX_RC_ENABLE_CM_COARSE_CAL: This bit is the receive recalibration common-mode coarse calibration enable.
56	RWX	RX_RC_ENABLE_CM_FINE_CAL: This bit is the receive recalibration common-mode fine calibration enable.
57	RWX	RX_RC_ENABLE_BER_TEST: This bit is the receive recalibration bit-error-rate test enable. It is unsupported. Leave it at 0.
58	RWX	RX_RC_ENABLE_RESULT_CHECK: This bit is the receive recalibration final results check enable. It is unsupported. Leave it at 0.
59	RWX	RX_RC_ENABLE_CTLE_EDGE_TRACK_ONLY: This bit is the receive recalibration CTLE/peaking enable with edge tracking only.
60	RWX	RX_RC_ENABLE_DFE_H2_H12_CAL: This bit is the receive recalibration DFE H2-to-H12 calibration enable.
61	RWX	RX_RC_ENABLE_DAC_H1_TO_A_CAL: This bit is the receive recalibration H! DAC-to-amplitude DAC cross-calibration enable.
62:63	RO	constant = 0b00

Register Name	Receive CTL Mode 22 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE22_EO_PG
Address	8008B8200601143F (SCOM)
Description	This register contains the 22nd set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_RC_ENABLE_INTEG_LATCH_OFFSET_CAL: This bit is the receive recalibration latch offset adjustment enable with integrator-based disable.
49	RWX	RX_RC_ENABLE_CTLE_COARSE_CAL: This bit is the receive recalibration coarse CTLE/Peakin enable.
50	RWX	RX_RC_ENABLE_DAC_H1_CAL: This bit is the receive recalibration H! DAC calibration to reference enable.
51	RWX	RX_RC_ENABLE_VGA_CAL: This bit is the receive recalibration VGA gain and offset adjustment enable.
52	RWX	RX_RC_ENABLE_DFE_H1_CAL: This bit is the receive recalibration DFE H1 adjustment enable.
53	RWX	RX_RC_ENABLE_H1AP_TWEAK: This bit is the receive recalibration H1/AN PR adjustment enable.
54	RWX	RX_RC_ENABLE_DDC: This bit is the receive recalibration dynamic data-centering enable.

Bits	SCOM	Field Mnemonic: Description
55	RWX	RX_RC_ENABLE_CM_COARSE_CAL: This bit is the receive recalibration common-mode coarse calibration enable.
56	RWX	RX_RC_ENABLE_CM_FINE_CAL: This bit is the receive recalibration common-mode fine calibration enable.
57	RWX	RX_RC_ENABLE_BER_TEST: This bit is the receive recalibration bit-error-rate test enable. It is unsupported. Leave it at 0.
58	RWX	RX_RC_ENABLE_RESULT_CHECK: This bit is the receive recalibration final results check enable. It is unsupported. Leave it at 0.
59	RWX	RX_RC_ENABLE_CTLE_EDGE_TRACK_ONLY: This bit is the receive recalibration CTLE/peaking enable with edge tracking only.
60	RWX	RX_RC_ENABLE_DFE_H2_H12_CAL: This bit is the receive recalibration DFE H2-to-H12 calibration enable.
61	RWX	RX_RC_ENABLE_DAC_H1_TO_A_CAL: This bit is the receive recalibration H! DAC-to-amplitude DAC cross-calibration enable.
62:63	RO	constant = 0b00

Register Name	Receive CTL Mode 23 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE23_EO_PG
Address	8008C0000601143F (SCOM)
Description	This register contains the 23rd set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_QUAD_SEL: This field selects one of four possible phases for the deserialized receive I/O clock to send along with the data for integration flexibility and tuning for slack into the receive digital logic.
50:54	RO	constant = 0b00000
55	RWX	RX_PEAK_TUNE: Peak tune bit to analog.
56	RWX	RX_LTE_EN: This bit enables LTE.
57:58	RWX	RX_IQSPD_CFG: 00 = 7.8 Gbps to less than 9.6 Gbps. 01 = 9.6 Gbps to 12 Gbps. 10 = Unused. 11 = Greater than12 Gbps to 16 Gbps.
59	RWX	RX_DFEHISPD_EN: When 1, this bit puts the DFE into high-speed mode according to the per-system settings.
60	RWX	RX_DFE12_EN: When 1, the bit enables the logic for DFE H2 - H12.
61:63	RO	constant = 0b000

Register Name	Receive CTL Mode 23 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE23_EO_PG
Address	8008C0200601143F (SCOM)
Description	This register contains the 23rd set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_QUAD_SEL: This field selects one of four possible phases for the deserialized receive I/O clock to send along with the data for integration flexibility and tuning for slack into the receive digital logic.
50:54	RO	constant = 0b00000
55	RWX	RX_PEAK_TUNE: Peak tune bit to analog.
56	RWX	RX_LTE_EN: This bit enables LTE.
57:58	RWX	RX_IQSPD_CFG: 00 = 7.8 Gbps to less than 9.6 Gbps. 01 = 9.6 Gbps to 12 Gbps. 10 = Unused. 11 = Greater than12 Gbps to 16 Gbps.
59	RWX	RX_DFEHISPD_EN: When 1, this bit puts the DFE into high-speed mode according to the per-system settings.
60	RWX	RX_DFE12_EN: When 1, the bit enables the logic for DFE H2 - H12.
61:63	RO	constant = 0b000

Register Name	Receive CTL Mode 24 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE24_EO_PG
Address	8008C8000601143F (SCOM)
Description	This register contains the 24th set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_H1AP_CFG: This register controls the maximum allowed ration of H1 and Ap. This is not a servo setting, but rather the setting of a ration between H1 and the value of Ap.
50	RWX	RX_CTLE_UPDATE_MODE: This bit controls updating of the CTLE_COARSE (peaking) values.
51:55	RO	constant = 0b00000
56:63	RWX	RX_USER_FILTER_MASK: This register controls the filter and mask for user-defined servo operations.

Register Name	Receive CTL Mode 24 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE24_EO_PG
Address	8008C8200601143F (SCOM)
Description	This register contains the 24th set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_H1AP_CFG: This register controls the maximum allowed ration of H1 and Ap. This is not a servo setting, but rather the setting of a ration between H1 and the value of Ap.
50	RWX	RX_CTLE_UPDATE_MODE: This bit controls updating of the CTLE_COARSE (peaking) values.
51:55	RO	constant = 0b00000
56:63	RWX	RX_USER_FILTER_MASK: This register controls the filter and mask for user-defined servo operations.

Register Name	Receive CTL Mode 29 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE29_EO_PG
Address	8008D0000601143F (SCOM)
Description	This register contains the 29th set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_APX111_HIGH: This field contains the receive Amax high target, in amplitude DAC steps (as measured by ap_x111 and an_x000). The default is d102.
56:63	RWX	RX_APX111_LOW: This field contains the receive Amax low target, in amplitude DAC steps (as measured by ap_x111 and an_x000). The default is d68.

Register Name	Receive CTL Mode 29 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE29_EO_PG
Address	8008D0200601143F (SCOM)
Description	This register contains the 29th set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_APX111_HIGH: This field contains the receive Amax high target, in amplitude DAC steps (as measured by ap_x111 and an_x000). The default is d102.
56:63	RWX	RX_APX111_LOW: This field contains the receive Amax low target, in amplitude DAC steps (as measured by ap_x111 and an_x000). The default is d68.

Register Name	Receive CTL CNTL1 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL1_EO_PG
Address	8008D8000601143F (SCOM)
Description	This register contains the first set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BER_EN: Diagnostic bit error rate (BER) error checking enable control. When 1, this bit enables error checking. When 0, the error checking is disabled. This control enables the BER timer. It also enables the error checker and BER counters. The assumption is that the drivers are currently driving PRBS23, and the link was trained before enabling BER checking.
49	RWX	RX_BER_TIMER_FREEZE_EN: Diagnostic bit-error-rate (BER) timer freeze enable. When set to 1, the timer is frozen when any lane error count saturates in that pack.
50	RWX	RX_BER_COUNT_FREEZE_EN: Diagnostic BER lane error counter freeze enable. When set to 1, the per-lane error counters are frozen when the timer saturates in that pack.

Bits	SCOM	Field Mnemonic: Description
51:54	RWX	RX_BER_COUNT_SEL: Diagnostic BER lane error counter saturation select. This field selects the number of errors that saturates the counter and causes a freeze event. The default value is used during initialization and must only be changed post initialization. 0b0000 = 1. 0b0001 = 2. 0b0010 = 4. 0b0011 = 8. 0b0100 = 16. 0b0101 = 32. 0b0110 = 64. 0b0111 = 128. 0b1000 = 256. 0b1001 = 512. 0b1010 = 1024. 0b1011 = unused1. 0b1100 = unused2. 0b1101 = unused3. 0b1110 = unused4. 0b1111 = unused5.
55	RO	constant = 0b0
56:58	RWX	RX_BER_TIMER_SEL: Diagnostic BER timer saturation select. This field selects the timer value that saturates the timer and causes a freeze event. The default value is used during initialization and must only be changed post initialization. 0b000 = 2^{31}. 0b001 = 2^{27}. 0b010 = 2^{23}. 0b011 = 2^{19}. 0b100 = 2^{17}. 0b101 = 2^{13}. 0b110 = 2^{9}. 0b111 = 2^{5}.
59	RWX	RX_BER_CLR_COUNT_ON_READ_EN: Diagnostic BER lane error counter clear on read. When set to 1, this bit enables clearing a lane's error counter when it is read.
60	RWX	RX_BER_CLR_TIMER_ON_READ_EN: Diagnostic BER timer clear on read. When set to 1, this bit enables clearing a lane's timer when it is read from any lane in the pack.
61:63	RO	constant = 0b000

Register Name	Receive CTL CNTL1 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL1_EO_PG
Address	8008D8200601143F (SCOM)
Description	This register contains the first set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BER_EN: Diagnostic bit error rate (BER) error checking enable control. When 1, this bit enables error checking. When 0, the error checking is disabled. This control enables the BER timer. It also enables the error checker and BER counters. The assumption is that the drivers are currently driving PRBS23, and the link was trained before enabling BER checking.
49	RWX	RX_BER_TIMER_FREEZE_EN: Diagnostic bit-error-rate (BER) timer freeze enable. When set to 1, the timer is frozen when any lane error count saturates in that pack.

Bits	SCOM	Field Mnemonic: Description
50	RWX	RX_BER_COUNT_FREEZE_EN: Diagnostic BER lane error counter freeze enable. When set to 1, the per-lane error counters are frozen when the timer saturates in that pack.
51:54	RWX	RX_BER_COUNT_SEL: Diagnostic BER lane error counter saturation select. This field selects the number of errors that saturates the counter and causes a freeze event. The default value is used during initialization and must only be changed post initialization. 0b0000 = 1. 0b0001 = 2. 0b0010 = 4. 0b0011 = 8. 0b0100 = 16. 0b0101 = 32. 0b0110 = 64. 0b0111 = 128. 0b1000 = 256. 0b1001 = 512. 0b1010 = 1024. 0b1011 = unused1. 0b1100 = unused2. 0b1101 = unused3. 0b1110 = unused4. 0b1111 = unused5.
55	RO	constant = 0b0
56:58	RWX	RX_BER_TIMER_SEL: Diagnostic BER timer saturation select. This field selects the timer value that saturates the timer and causes a freeze event. The default value is used during initialization and must only be changed post initialization. 0b000 = 2^{31}. 0b001 = 2^{27}. 0b010 = 2^{23}. 0b011 = 2^{19}. 0b100 = 2^{17}. 0b101 = 2^{13}. 0b110 = 2^{9}. 0b111 = 2^{5}.
59	RWX	RX_BER_CLR_COUNT_ON_READ_EN: Diagnostic BER lane error counter clear on read. When set to 1, this bit enables clearing a lane's error counter when it is read.
60	RWX	RX_BER_CLR_TIMER_ON_READ_EN: Diagnostic BER timer clear on read. When set to 1, this bit enables clearing a lane's timer when it is read from any lane in the pack.
61:63	RO	constant = 0b000

Register Name	Receive CTL CNTL2 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL2_EO_PG
Address	8008E0000601143F (SCOM)
Description	This register contains the second set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RWX	RX_TRC_MODE: Receive trace mode. 0b0000 = Training state machines. 0b0001 = Dynamic repair state machines. 0b0010 = SLS handshake state machines with recovery. 0b0011 = Dynamic recalibration state machines. 0b0100 = Recalibration handshake state machine with recovery. 0b0101 = CRC or ECC tallying logic. 0b0110 = Receive SLS commands. 0b0111 = Receive bad lanes. 0b1000 = Receive SLS lanes. 0b1001 = GCR. 0b1010 = Per lane/per pack trace (see rx_pp_trc_mode for details). 0b1011 = TBD. 0b1100 = TBD. 0b1101 = TBD. 0b1110 = TBD. 0b1111 = TBD.
52:63	RO	constant = 0b000000000000

Register Name	Receive CTL CNTL2 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL2_EO_PG
Address	8008E0200601143F (SCOM)
Description	This register contains the second set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_TRC_MODE: Receive trace mode. 0b0000 = Training state machines. 0b0001 = Dynamic repair state machines. 0b0010 = SLS handshake state machines with recovery. 0b0011 = Dynamic recalibration state machines. 0b0100 = Recalibration handshake state machine with recovery. 0b0101 = CRC or ECC tallying logic. 0b0110 = Receive SLS commands. 0b0111 = Receive bad lanes. 0b1000 = Receive SLS lanes. 0b1001 = GCR. 0b1010 = Per lane/per pack trace (see rx_pp_trc_mode for details). 0b1011 = TBD. 0b1100 = TBD. 0b1101 = TBD. 0b1110 = TBD. 0b1111 = TBD.
52:63	RO	constant = 0b000000000000

Register Name	Receive CTL CNTL3 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL3_EO_PG
Address	8008E8000601143F (SCOM)
Description	This register contains the third set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_INT_MODE: This field contains the receive interrupt mode setting.
52:63	RWX	RX_INT_CURRENT_STATE: This field contains the receive interrupt current state to stop on.

Register Name	Receive CTL CNTL3 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL3_EO_PG
Address	8008E8200601143F (SCOM)
Description	This register contains the third set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_INT_MODE: This field contains the receive interrupt mode setting.
52:63	RWX	RX_INT_CURRENT_STATE: This field contains the receive interrupt current state to stop on.

Register Name	Receive CTL CNTL4 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL4_EO_PG
Address	8008F0000601143F (SCOM)
Description	This register contains the fourth set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_INT_ENABLE_ENC: This field contains the receive interrupt encoded enable.
52:63	RWX	RX_INT_NEXT_STATE: This field contains the receive interrupt next state to stop on.

Register Name	Receive CTL CNTL4 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL4_EO_PG
Address	8008F0200601143F (SCOM)
Description	This register contains the fourth set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_INT_ENABLE_ENC: This field contains the receive interrupt encoded enable.
52:63	RWX	RX_INT_NEXT_STATE: This field contains the receive interrupt next state to stop on.

Register Name	Receive CTL CNTL5 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL5_EO_PG
Address	8008F8000601143F (SCOM)
Description	This register contains the fifth set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:51	RO	constant = 0b0000000000000000000000000000000000000000000000000000
52:63	RWX	RX_INT_GOTO_STATE: This field contains the receive interrupt state to go to upon an interrupt trigger.

Register Name	Receive CTL CNTL5 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL5_EO_PG
Address	8008F8200601143F (SCOM)
Description	This register contains the fifth set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:51	RO	constant = 0b0000000000000000000000000000000000000000000000000000
52:63	RWX	RX_INT_GOTO_STATE: This field contains the receive interrupt state to go to upon an interrupt trigger.

Register Name	Receive CTL CNTL6 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL6_EO_PG
Address	800900000601143F (SCOM)
Description	This register contains the sixth set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:51	RO	constant = 0b0000000000000000000000000000000000000000000000000000
52:63	RWX	RX_INT_RETURN_STATE: This field contains the receive interrupt state to go to upon return from an interrupt code.

Register Name	Receive CTL CNTL6 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL6_EO_PG
Address	800900200601143F (SCOM)
Description	This register contains the sixth set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:51	RO	constant = 0b0000000000000000000000000000000000000000000000000000
52:63	RWX	RX_INT_RETURN_STATE: This field contains the receive interrupt state to go to upon return from an interrupt code.

Register Name	Receive CTL CNTL7 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTLX7_EO_PG
Address	800908000601143F (SCOM)
Description	This register contains the seventh set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_CAL_LANE_GCRMSG: This field contains the encoded calibration lane in relation to the entire receive bus (including multi-groups or partial groups).
55	RWX	RX_CAL_LANE_VAL_GCRMSG: This bit indicates that the receive calibration lane is valid.
56:60	RWX	RX_CAL_LANE_PG_PHY_GCRMSG: This field contains the encoded calibration lane in relation to the local, physical group.
61:63	RO	constant = 0b000

Register Name	Receive CTL CNTL7 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTLX7_EO_PG
Address	800908200601143F (SCOM)
Description	This register contains the seventh set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_CAL_LANE_GCRMSG: This field contains the encoded calibration lane in relation to the entire receive bus (including multi-groups or partial groups).
55	RWX	RX_CAL_LANE_VAL_GCRMSG: This bit indicates that the receive calibration lane is valid.
56:60	RWX	RX_CAL_LANE_PG_PHY_GCRMSG: This field contains the encoded calibration lane in relation to the local, physical group.
61:63	RO	constant = 0b000

Register Name	Receive CTL CNTL8 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL8_EO_PG
Address	800910000601143F (SCOM)
Description	This register contains the eighth set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:62	RWX	RX_SERVO_OP: This field contains the servo operation code. It is written by the global training state machine.
63	RWX	RX_SERVO_DONE: This bit indicates that the servo operation completed. It is read by the global training state machine.

Register Name	Receive CTL CNTL8 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL8_EO_PG
Address	800910200601143F (SCOM)
Description	This register contains the eighth set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:62	RWX	RX_SERVO_OP: This field contains the servo operation code. It is written by the global training state machine.
63	RWX	RX_SERVO_DONE: This bit indicates that the servo operation completed. It is read by the global training state machine.

Register Name	Receive CTL CNTL9 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL9_EO_PG
Address	800918000601143F (SCOM)
Description	This register contains the ninth set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BIST_EN: This bit enables the receive BIST state machine to begin testing. It is set by the BIST helper sequencer through a GCR message. To properly initialize and run the receive BIST, set the rx_start_bist register bit.
49	RWX	RX_BIST_EXT_START_MODE: This bit enables the receive BIST state machine to begin testing. It is set by the BIST helper sequencer through a GCR message. To properly initialize and run the receive BIST, set the rx_start_bist register bit.
50:52	RWX	RX_BIST_INIT_DISABLE: Each bit disables an individual step of the receive BIST initialization state machine when raised. Bit 0 disables the CU PLL lock. Bit 1 disables the receive FIFO initialization. Bit 2 disables eye optimization/training.
53	RWX	RX_BIST_CUPLL_LOCK_CHECK_EN: This bit enables the CU PLL lock check mode of the receive BIST initialization state machine. When set high, the test checks for the PLL lock signal and sets an error if it is not present.
54:59	RWX	RX_BIST_STORE_EYES_LANE_SEL: This register selects which lane to store receive BIST eye-width data from. The data is stored in the rx_bist_eye_a_width and rx_bist_eye_b_width registers.
60:61	RWX	RX_BIST_STORE_EYES_BANK_SEL: This register selects which bank to store receive BIST eye-width data from. 0b00 = Store bank A widths. 0b01 = Store bank B widths. 0b10 = Store bank E widths. 0b11 = EDI+ bank A.
62	RWX	RX_PERVASIVE_CAPT: This bit latches glb_ctl and jtag_bndy pervasive signals in iocrc_pervasive_capt when set high. RO register bit rx_prvcpt_change_det goes high when latched values differ from pervasive inputs.
63	RO	constant = 0b0

Register Name	Receive CTL CNTL9 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL9_EO_PG
Address	800918200601143F (SCOM)
Description	This register contains the ninth set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BIST_EN: This bit enables the receive BIST state machine to begin testing. It is set by the BIST helper sequencer through a GCR message. To properly initialize and run the receive BIST, set the rx_start_bist register bit.
49	RWX	RX_BIST_EXT_START_MODE: This bit enables the receive BIST state machine to begin testing. It is set by the BIST helper sequencer through a GCR message. To properly initialize and run the receive BIST, set the rx_start_bist register bit.

Bits	SCOM	Field Mnemonic: Description
50:52	RWX	RX_BIST_INIT_DISABLE: Each bit disables an individual step of the receive BIST initialization state machine when raised. Bit 0 disables the CU PLL lock. Bit 1 disables the receive FIFO initialization. Bit 2 disables eye optimization/training.
53	RWX	RX_BIST_CUPLL_LOCK_CHECK_EN: This bit enables the CU PLL lock check mode of the receive BIST initialization state machine. When set high, the test checks for the PLL lock signal and sets an error if it is not present.
54:59	RWX	RX_BIST_STORE_EYES_LANE_SEL: This register selects which lane to store receive BIST eye-width data from. The data is stored in the rx_bist_eye_a_width and rx_bist_eye_b_width registers.
60:61	RWX	RX_BIST_STORE_EYES_BANK_SEL: This register selects which bank to store receive BIST eye-width data from. 0b00 = Store bank A widths. 0b01 = Store bank B widths. 0b10 = Store bank E widths. 0b11 = EDI+ bank A.
62	RWX	RX_PERVASIVE_CAPT: This bit latches glb_ctl and jtag_bndy pervasive signals in iocrc_pervasive_capt when set high. RO register bit rx_prvcpt_change_det goes high when latched values differ from pervasive inputs.
63	RO	constant = 0b0

Register Name	Receive CTL CNTL10 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL10_EO_PG
Address	800920000601143F (SCOM)
Description	This register contains the tenth set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_BIST_PRBS_TEST_TIME: This field controls how long the receive BIST tests the PRBS7 data for errors.
52	RWX	RX_BIST_BUS_DATA_MODE: This bit enables a mode where the receive BIST tests data from the bus.
53:56	RWX	RX_BIST_PRBS_PROP_TIME: This field controls how long the receive BIST waits between incrementing a phase rotator and beginning to test the PRBS data.
57:60	RWX	RX_BIST_PLL_LOCK_TIMEOUT: This field controls how long the receive BIST initialization waits for the PLL lock signal before timing out.
61:63	RO	constant = 0b000

Register Name	Receive CTL CNTL10 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL10_EO_PG
Address	800920200601143F (SCOM)
Description	This register contains the tenth set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_BIST_PRBS_TEST_TIME: This field controls how long the receive BIST tests the PRBS7 data for errors.

Bits	SCOM	Field Mnemonic: Description
52	RWX	RX_BIST_BUS_DATA_MODE: This bit enables a mode where the receive BIST tests data from the bus.
53:56	RWX	RX_BIST_PRBS_PROP_TIME: This field controls how long the receive BIST waits between incrementing a phase rotator and beginning to test the PRBS data.
57:60	RWX	RX_BIST_PLL_LOCK_TIMEOUT: This field controls how long the receive BIST initialization waits for the PLL lock signal before timing out.
61:63	RO	constant = 0b000

Register Name	Receive CTL CNTL11 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL11_EO_PG
Address	800928000601143F (SCOM)
Description	This register contains the 11th set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:56	RWX	RX_DACTEST_LLMT: This control register is used to lower the threshold limit.
57	RWX	RX_DACTEST_RESET: This control register is used to reset the DACTEST.
58	RWX	RX_DACTEST_START: This control register is used to start the DACTEST.
59:63	RO	constant = 0b00000

Register Name	Receive CTL CNTL11 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL11_EO_PG
Address	800928200601143F (SCOM)
Description	This register contains the 11th set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:56	RWX	RX_DACTEST_LLMT: This control register is used to lower the threshold limit.
57	RWX	RX_DACTEST_RESET: This control register is used to reset the DACTEST.
58	RWX	RX_DACTEST_START: This control register is used to start the DACTEST.
59:63	RO	constant = 0b00000

Register Name	Receive CTL CNTL12 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL12_EO_PG
Address	800930000601143F (SCOM)
Description	This register contains the 12th set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:56	RWX	RX_DACTEST_HLMT: This control register is used to set a higher threshold limit.
57:63	RO	constant = 0b0000000

Register Name	Receive CTL CNTL12 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL12_EO_PG
Address	800930200601143F (SCOM)
Description	This register contains the 12th set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:56	RWX	RX_DACTEST_HLMT: This control register is used to set a higher threshold limit.
57:63	RO	constant = 0b0000000

Register Name	Receive CTL CNTL13 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL13_EO_PG
Address	800938000601143F (SCOM)
Description	This register contains the 13th set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_HIST_MIN_EYE_WIDTH_VALID: This bit indicates that the receive historic eye width minimum value and lane are valid.
49:53	RWX	RX_HIST_MIN_EYE_WIDTH_LANE: This field contains the receive historic eye width lane number.
54:61	RWX	RX_HIST_MIN_EYE_WIDTH: This field contains the receive historic eye width and height minimum measurement mode.
62:63	RO	constant = 0b00

Register Name	Receive CTL CNTL13 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL13_EO_PG
Address	800938200601143F (SCOM)
Description	This register contains the 13th set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_HIST_MIN_EYE_WIDTH_VALID: This bit indicates that the receive historic eye width minimum value and lane are valid.
49:53	RWX	RX_HIST_MIN_EYE_WIDTH_LANE: This field contains the receive historic eye width lane number.
54:61	RWX	RX_HIST_MIN_EYE_WIDTH: This field contains the receive historic eye width and height minimum measurement mode.
62:63	RO	constant = 0b00

Register Name	Receive CTL CNTL14 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL14_EO_PG
Address	800940000601143F (SCOM)
Description	This register contains the 14th set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_HIST_MIN_EYE_HEIGHT_VALID: This bit indicates that the receive historic eye height minimum value and lane are valid.
49:53	RWX	RX_HIST_MIN_EYE_HEIGHT_LANE: This field contains the receive historic eye height lane number.
54:61	RWX	RX_HIST_MIN_EYE_HEIGHT: This field contains the receive historic eye height minimum measurement mode. It is inoperative on POWER8 processor with NVLink technology hardware. Use the rx_hist_min_eye_width_mode control instead. Set both the width and height_mode controls to the same value in test routines to maintain compatibility.
62:63	RO	constant = 0b00

Register Name	Receive CTL CNTL14 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL14_EO_PG
Address	800940200601143F (SCOM)
Description	This register contains the 14th set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_HIST_MIN_EYE_HEIGHT_VALID: This bit indicates that the receive historic eye height minimum value and lane are valid.
49:53	RWX	RX_HIST_MIN_EYE_HEIGHT_LANE: This field contains the receive historic eye height lane number.
54:61	RWX	RX_HIST_MIN_EYE_HEIGHT: This field contains the receive historic eye height minimum measurement mode. It is inoperative on POWER8 processor with NVLink technology hardware. Use the rx_hist_min_eye_width_mode control instead. Set both the width and height_mode controls to the same value in test routines to maintain compatibility.
62:63	RO	constant = 0b00

Register Name	Receive CTL CNTL15 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL15_EO_PG
Address	800948000601143F (SCOM)
Description	This register contains the 15th set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_WTL_TEST_CLOCK: This bit is a signal from the main WT machine to start testing the clock lane.
49	RWX	RX_WTL_TEST_DATA: This bit is a signal from the main WT machine to start testing the data lane.
50	RWX	RX_WT_BS_CLOCK_EN_BYP: When asserted, this bit forces the BS enable for the clock. It can be used to override the WT state machine controls.

Bits	SCOM	Field Mnemonic: Description
51	RWX	RX_WT_BS_DATA_EN_BYP: When asserted, this bit forces the BS enable for the data. It can be used to override the WT state machine controls.
52:63	RO	constant = 0b000000000000

Register Name	Receive CTL CNTL15 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL15_EO_PG
Address	800948200601143F (SCOM)
Description	This register contains the 15th set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_WTL_TEST_CLOCK: This bit is a signal from the main WT machine to start testing the clock lane.
49	RWX	RX_WTL_TEST_DATA: This bit is a signal from the main WT machine to start testing the data lane.
50	RWX	RX_WT_BS_CLOCK_EN_BYP: When asserted, this bit forces the BS enable for the clock. It can be used to override the WT state machine controls.
51	RWX	RX_WT_BS_DATA_EN_BYP: When asserted, this bit forces the BS enable for the data. It can be used to override the WT state machine controls.
52:63	RO	constant = 0b000000000000

Register Name	Receive CTL STAT1 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_STAT1_EO_PG
Address	800950000601143F (SCOM)
Description	This register contains the servo operation result.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_SERVO_RESULT: This field contains the servo operation result. It is read by the global training state machine.
56:63	RO	constant = 0b00000000

Register Name	Receive CTL STAT1 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_STAT1_EO_PG
Address	800950200601143F (SCOM)
Description	This register contains the servo operation result.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_SERVO_RESULT: This field contains the servo operation result. It is read by the global training state machine.
56:63	RO	constant = 0b00000000

Register Name	Receive CTL STAT2 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_STAT2_EO_PG
Address	800958000601143F (SCOM)
Description	This register contains the status of the receive BIST.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BIST_INIT_DONE: This bit signals completion of the receive BIST initialization state machine.
49	RWX	RX_BIST_DONE: This bit signals completion of the entire receive BIST procedure.
50	RWX	RX_BIST_CU_PLL_ERR: This bit indicates that an error was detected during an rx_cu_pll lock error. \n0 = No error. \n1 = Error.
51	RWX	RX_BIST_NO_EDGE_DET: This bit indicates that one eye was counted to be significantly large (over 60 phase rotator steps).
52:57	RWX	RX_BIST_EYE_A_WIDTH: This register holds the counted eye A width of one particular lane.
58:63	RWX	RX_BIST_EYE_B_WIDTH: This register holds the counted eye B width of one particular lane.

Register Name	Receive CTL STAT2 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_STAT2_EO_PG
Address	800958200601143F (SCOM)
Description	This register contains the status of the receive BIST.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BIST_INIT_DONE: This bit signals completion of the receive BIST initialization state machine.
49	RWX	RX_BIST_DONE: This bit signals completion of the entire receive BIST procedure.
50	RWX	RX_BIST_CU_PLL_ERR: This bit indicates that an error was detected during an rx_cu_pll lock error. \n0 = No error. \n1 = Error.
51	RWX	RX_BIST_NO_EDGE_DET: This bit indicates that one eye was counted to be significantly large (over 60 phase rotator steps).
52:57	RWX	RX_BIST_EYE_A_WIDTH: This register holds the counted eye A width of one particular lane.
58:63	RWX	RX_BIST_EYE_B_WIDTH: This register holds the counted eye B width of one particular lane.

Register Name	Receive CTL STAT3 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_STAT3_EO_PG
Address	800960000601143F (SCOM)
Description	This register contains the status of the wire-test lane machine.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_WTL_SM_STATUS: This field indicates the wire-test lane machine status.
53:63	RO	constant = 0b00000000000

Register Name	Receive CTL STAT3 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_STAT3_EO_PG
Address	800960200601143F (SCOM)
Description	This register contains the status of the wire-test lane machine.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_WTL_SM_STATUS: This field indicates the wire-test lane machine status.
53:63	RO	constant = 0b00000000000

Register Name	Receive CTL Mode 26 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE26_EO_PG
Address	800968000601143F (SCOM)
Description	This register contains the 26th set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_EO_ENABLE_CTLE_1ST_LATCH_OFFSET_CAL: Receive eye-optimization; first latch offset adjustment enable with CTLE-based disable.
49	RWX	RX_EO_ENABLE_CTLE_2ND_LATCH_OFFSET_CAL: Receive eye-optimization; second latch offset adjustment enable with CTLE-based disable.
50	RWX	RX_EO_ENABLE_VGA_AMAX_MODE: Receive eye-optimization; VGA Ap measurement mode.
51:61	RWX	RX_EO_ENABLE_DFE_H2_H12_SUBSTEP: Receive eye optimization; this field contains individual controls for DFE H2-to-H12 tap optimization.
62	RWX	RX_EO_ENABLE_DFE_VOLTAGE_MODE: Receive eye optimization; this bit enables DFE H2-to-H12 voltage-mode adjustment.
63	RWX	RX_EO_ENABLE_DFE_H6_H12_FAST_MODE: Receive eye optimization; this bit enables DFE H2-to-H12 fast mode.

Register Name	Receive CTL Mode 26 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE26_EO_PG
Address	800968200601143F (SCOM)
Description	This register contains the 26th set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_EO_ENABLE_CTLE_1ST_LATCH_OFFSET_CAL: Receive eye-optimization; first latch offset adjustment enable with CTLE-based disable.
49	RWX	RX_EO_ENABLE_CTLE_2ND_LATCH_OFFSET_CAL: Receive eye-optimization; second latch offset adjustment enable with CTLE-based disable.
50	RWX	RX_EO_ENABLE_VGA_AMAX_MODE: Receive eye-optimization; VGA Ap measurement mode.

Bits	SCOM	Field Mnemonic: Description
51:61	RWX	RX_EO_ENABLE_DFE_H2_H12_SUBSTEP: Receive eye optimization; this field contains individual controls for DFE H2-to-H12 tap optimization.
62	RWX	RX_EO_ENABLE_DFE_VOLTAGE_MODE: Receive eye optimization; this bit enables DFE H2-to-H12 voltage-mode adjustment.
63	RWX	RX_EO_ENABLE_DFE_H6_H12_FAST_MODE: Receive eye optimization; this bit enables DFE H2-to-H12 fast mode.

Register Name	Receive CTL Mode 27 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE27_EO_PG
Address	800970000601143F (SCOM)
Description	This register contains the 27th set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_RC_ENABLE_CTLE_1ST_LATCH_OFFSET_CAL: Receive recalibration; first latch offset adjustment enable with CTLE-based disable.
49	RWX	RX_RC_ENABLE_CTLE_2ND_LATCH_OFFSET_CAL: Receive recalibration; second latch offset adjustment enable with CTLE-based disable.
50	RWX	RX_RC_ENABLE_VGA_AMAX_MODE: Receive recalibration; VGA Ap measurement mode.
51:61	RWX	RX_RC_ENABLE_DFE_H2_H12_SUBSTEP: Receive recalibration; This field contains individual controls for DFE H2-to-H12 tap optimization.
62	RWX	RX_RC_ENABLE_DFE_VOLTAGE_MODE: Receive recalibration; this bit enables DFE H2-to-H12 voltage-mode adjustment.
63	RWX	RX_RC_ENABLE_DFE_H6_H12_FAST_MODE: Receive recalibration; this bit enables DFE H6-to-H12 fast mode.

Register Name	Receive CTL Mode 27 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE27_EO_PG
Address	800970200601143F (SCOM)
Description	This register contains the 27th set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_RC_ENABLE_CTLE_1ST_LATCH_OFFSET_CAL: Receive recalibration; first latch offset adjustment enable with CTLE-based disable.
49	RWX	RX_RC_ENABLE_CTLE_2ND_LATCH_OFFSET_CAL: Receive recalibration; second latch offset adjustment enable with CTLE-based disable.
50	RWX	RX_RC_ENABLE_VGA_AMAX_MODE: Receive recalibration; VGA Ap measurement mode.
51:61	RWX	RX_RC_ENABLE_DFE_H2_H12_SUBSTEP: Receive recalibration; This field contains individual controls for DFE H2-to-H12 tap optimization.
62	RWX	RX_RC_ENABLE_DFE_VOLTAGE_MODE: Receive recalibration; this bit enables DFE H2-to-H12 voltage-mode adjustment.
63	RWX	RX_RC_ENABLE_DFE_H6_H12_FAST_MODE: Receive recalibration; this bit enables DFE H6-to-H12 fast mode.

Register Name	Receive CTL Mode 28 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE28_EO_PG
Address	800978000601143F (SCOM)
Description	This register contains the 28th set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_DC_ENABLE_CM_COARSE_CAL: This bit enables receive DC calibration eye-optimization common-mode coarse calibration.
49	RWX	RX_DC_ENABLE_CM_FINE_CAL: This bit enables receive DC calibration eye-optimization common-mode fine calibration.
50	RWX	RX_DC_ENABLE_CTLE_1ST_LATCH_OFFSET_CAL: Receive DC calibration eye-optimization latch offset adjustment enable done prior to CTLE.
51	RWX	RX_DC_ENABLE_CTLE_2ND_LATCH_OFFSET_CAL: Receive DC calibration eye-optimization latch offset adjustment enable done after CTLE.
52	RWX	RX_DC_ENABLE_INTEG_LATCH_OFFSET_CAL: Receive DC calibration eye-optimization latch offset adjustment enable done prior to integrator.
53	RWX	RX_DC_ENABLE_DAC_H1_CAL: Receive DC cal eye optimization H1 DAC calibration.
54	RWX	RX_DC_ENABLE_DAC_H1_TO_A_CAL: Receive DC cal eye optimization H1 DAC to amplitude DAC calibration.
55:63	RO	constant = 0b000000000

Register Name	Receive CTL Mode 28 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE28_EO_PG
Address	800978200601143F (SCOM)
Description	This register contains the 28th set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_DC_ENABLE_CM_COARSE_CAL: This bit enables receive DC calibration eye-optimization common-mode coarse calibration.
49	RWX	RX_DC_ENABLE_CM_FINE_CAL: This bit enables receive DC calibration eye-optimization common-mode fine calibration.
50	RWX	RX_DC_ENABLE_CTLE_1ST_LATCH_OFFSET_CAL: Receive DC calibration eye-optimization latch offset adjustment enable done prior to CTLE.
51	RWX	RX_DC_ENABLE_CTLE_2ND_LATCH_OFFSET_CAL: Receive DC calibration eye-optimization latch offset adjustment enable done after CTLE.
52	RWX	RX_DC_ENABLE_INTEG_LATCH_OFFSET_CAL: Receive DC calibration eye-optimization latch offset adjustment enable done prior to integrator.
53	RWX	RX_DC_ENABLE_DAC_H1_CAL: Receive DC cal eye optimization H1 DAC calibration.
54	RWX	RX_DC_ENABLE_DAC_H1_TO_A_CAL: Receive DC cal eye optimization H1 DAC to amplitude DAC calibration.
55:63	RO	constant = 0b000000000

Register Name	Receive ID2 Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_ID2_PG
Address	800980000601143F (SCOM)
Description	This register is used to set lane positions.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant = 0b0000000000000000000000000000000000000000000000000
49:55	RWX	RX_START_LANE_ID: This field is used to programmatically set the first lane position in the group, but relative to the bus.
56	RO	constant = 0b0
57:63	RWX	RX_END_LANE_ID: This field is used to programmatically set the last lane position in the group, but relative to the bus.

Register Name	Receive ID2 Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_ID2_PG
Address	800980200601143F (SCOM)
Description	This register is used to set lane positions.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant = 0b0000000000000000000000000000000000000000000000000
49:55	RWX	RX_START_LANE_ID: This field is used to programmatically set the first lane position in the group, but relative to the bus.
56	RO	constant = 0b0
57:63	RWX	RX_END_LANE_ID: This field is used to programmatically set the last lane position in the group, but relative to the bus.

Register Name	Receive CTL Mode 1 E Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE1_E_PG
Address	800990000601143F (SCOM)
Description	This register contains the first set of receive CTL E mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_MASTER_MODE: Master mode. This bit is used to set a chip bus as the master side of the interface. The master side of the interface is where training is kicked off and coordinated in the logic. 0b0 = Slave. 0b1 = Master.
49	RWX	RX_DISABLE_FENCE_RESET: This bit is set to disable clearing of the receive and transmit fence controls at the end of training. 0b0 = Clear the fence bit (default). 0b1 = Leave the fence in its current state.
50:56	RO	constant = 0b0000000

Bits	SCOM	Field Mnemonic: Description
57	RWX	RX_FENCE: Receive and transmit fence bit. 0b0 = Functional data is driven to and from the nest logic. 0b1 = Functional data is gated to zeros to and from nest logic. This setting also indicates that link training not yet complete.
58	RWX	RX_PDWN_LITE_DISABLE: This bit disables the power-down lite feature of unused spare lanes (generally, it should match tx_pdwn_lite_disable).
59	RWX	RX_USE_SLS_AS_SPR: This bit determines whether the receive SLS lane can be used as a spare lane on the bus to repair bad lanes. **Note:** If yes, recalibration is disabled after the SLS lane is used as a spare lane. This also applies to the transmit side.
60	RWX	RX_DYN_RECAL_SUSPEND: This bit suspends dynamic recalibration. Otherwise, it starts automatically after link training.
61	RO	constant = 0b0
62:63	RWX	RX_WT_PATTERN_LENGTH: Receive wire-test pattern length. This field specifies the length of N in the 3N-up/1N-down wire-test pattern. 0b00 = 128 (default). 0b01 = 256. 0b10 = 512. 0b11 = 1024.

Register Name	Receive CTL Mode 1 E Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE1_E_PG
Address	800990200601143F (SCOM)
Description	This register contains the first set of receive CTL E mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_MASTER_MODE: Master mode. This bit is used to set a chip bus as the master side of the interface. The master side of the interface is where training is kicked off and coordinated in the logic. 0b0 = Slave. 0b1 = Master.
49	RWX	RX_DISABLE_FENCE_RESET: This bit is set to disable clearing of the receive and transmit fence controls at the end of training. 0b0 = Clear the fence bit (default). 0b1 = Leave the fence in its current state.
50:56	RO	constant = 0b0000000
57	RWX	RX_FENCE: Receive and transmit fence bit. 0b0 = Functional data is driven to and from the nest logic. 0b1 = Functional data is gated to zeros to and from nest logic. This setting also indicates that link training not yet complete.
58	RWX	RX_PDWN_LITE_DISABLE: This bit disables the power-down lite feature of unused spare lanes (generally, it should match tx_pdwn_lite_disable).
59	RWX	RX_USE_SLS_AS_SPR: This bit determines whether the receive SLS lane can be used as a spare lane on the bus to repair bad lanes. **Note:** If yes, recalibration is disabled after the SLS lane is used as a spare lane. This also applies to the transmit side.
60	RWX	RX_DYN_RECAL_SUSPEND: This bit suspends dynamic recalibration. Otherwise, it starts automatically after link training.
61	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
62:63	RWX	RX_WT_PATTERN_LENGTH: Receive wire-test pattern length. This field specifies the length of N in the 3N-up/1N-down wire-test pattern. 0b00 = 128 (default). 0b01 = 256. 0b10 = 512. 0b11 = 1024.

Register Name	Receive CTL Mode 2 E Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE2_E_PG
Address	800998000601143F (SCOM)
Description	This register contains the second set of receive CTL E mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_WTR_MAX_BAD_LANES: This field contains the wire-test maximum number of bad lanes allowed per clock group. It is also the static repair, dynamic repair, and recalibration maximum number of bad lanes per RX bus. **Note:** This field must match the transmit side.
53:56	RWX	RX_SLS_EXTEND_SEL: This field indicates how long to extend sending of the transmit SLS command (that is, how long to delay sending gcr_wrt_done to the state machine.
57:63	RWX	RX_DYN_RPR_ENC_BAD_DATA_LANE_SHFT_AMT: CRC/ECC dynamic repair. This programmable register value is subtracted from the enc_bad_data_lane value provided from the CRC/ECC check logic (except for the all 1s clear pattern). For example, it must be set to 0x07 for the zMCI logic to compensate for disabled lanes. Otherwise, it is generally 0x00. **Note:** Always check the figtree for current settings.

Register Name	Receive CTL Mode 2 E Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE2_E_PG
Address	800998200601143F (SCOM)
Description	This register contains the second set of receive CTL E mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_WTR_MAX_BAD_LANES: This field contains the wire-test maximum number of bad lanes allowed per clock group. It is also the static repair, dynamic repair, and recalibration maximum number of bad lanes per RX bus. **Note:** This field must match the transmit side.
53:56	RWX	RX_SLS_EXTEND_SEL: This field indicates how long to extend sending of the transmit SLS command (that is, how long to delay sending gcr_wrt_done to the state machine.
57:63	RWX	RX_DYN_RPR_ENC_BAD_DATA_LANE_SHFT_AMT: CRC/ECC dynamic repair. This programmable register value is subtracted from the enc_bad_data_lane value provided from the CRC/ECC check logic (except for the all 1s clear pattern). For example, it must be set to 0x07 for the zMCI logic to compensate for disabled lanes. Otherwise, it is generally 0x00. **Note:** Always check the figtree for current settings.

Register Name	Receive CTL Mode 3 E Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE3_E_PG
Address	8009A0000601143F (SCOM)
Description	This register contains the third set of receive CTL E mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_SLS_TIMEOUT_SEL: This field selects the spare-lane signaling timeout value, which indicates how long to wait for a SLS handshake command. The value must be four times larger than tx_dyn_recal_interval_timeout_sel when performing recalibration aborts and four times rx_dyn_recal_overall_timeout_sel.
52:55	RWX	RX_CL_TIMEOUT_SEL: This field selects the clock lock timeout value.
56:59	RWX	RX_DS_SKEW_TIMEOUT_SEL: This field selects the deskew timeout value.
60:63	RWX	RX_DS_TIMEOUT_SEL: This field selects the deskew timeout value.

Register Name	Receive CTL Mode 3 E Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE3_E_PG
Address	8009A0200601143F (SCOM)
Description	This register contains the third set of receive CTL E mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_SLS_TIMEOUT_SEL: This field selects the spare-lane signaling timeout value, which indicates how long to wait for a SLS handshake command. The value must be four times larger than tx_dyn_recal_interval_timeout_sel when performing recalibration aborts and four times rx_dyn_recal_overall_timeout_sel.
52:55	RWX	RX_CL_TIMEOUT_SEL: This field selects the clock lock timeout value.
56:59	RWX	RX_DS_SKEW_TIMEOUT_SEL: This field selects the deskew timeout value.
60:63	RWX	RX_DS_TIMEOUT_SEL: This field selects the deskew timeout value.

Register Name	Receive CTL Mode 4 E Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE4_E_PG
Address	8009A8000601143F (SCOM)
Description	This register contains the fourth set of receive CTL E mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_WT_CHECK_COUNT: This field selects the number of extra times the wire--test pattern is checked for a good lane.
53:56	RWX	RX_PGOOD_TIMEOUT_SEL: This field selects the PLL partial-good reset timeout value.
57:60	RWX	RX_PLL_LOCK_TIMEOUT_SEL: This field selects the PLL lock timeout value.
61	RWX	RX_PSAVE_TIMER_WAKEUP_MODE: This bit enables a wakeup timer on a psave mode wakeup.

Bits	SCOM	Field Mnemonic: Description
62	RWX	RX_PSAVE_WAKEUP_LANE0_ENABLE: This bit enables lane 0 at all times as the wakeup lane from psave mode.
63	RO	constant = 0b0

Register Name	Receive CTL Mode 4 E Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE4_E_PG
Address	8009A8200601143F (SCOM)
Description	This register contains the fourth set of receive CTL E mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_WT_CHECK_COUNT: This field selects the number of extra times the wire--test pattern is checked for a good lane.
53:56	RWX	RX_PGOOD_TIMEOUT_SEL: This field selects the PLL partial-good reset timeout value.
57:60	RWX	RX_PLL_LOCK_TIMEOUT_SEL: This field selects the PLL lock timeout value.
61	RWX	RX_PSAVE_TIMER_WAKEUP_MODE: This bit enables a wakeup timer on a psave mode wakeup.
62	RWX	RX_PSAVE_WAKEUP_LANE0_ENABLE: This bit enables lane 0 at all times as the wakeup lane from psave mode.
63	RO	constant = 0b0

Register Name	Receive CTL Mode 5 E Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE5_E_PG
Address	8009B0000601143F (SCOM)
Description	This register contains the fifth set of receive CTL E mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_INITIAL_L2U_DLY: This field indicates the receive FIFO initial load to unload delay. For the setting X, the latency is 4 x X to 4 x X + 4 UI. The default is 16 - 20 UI.
52:55	RWX	RX_FIFO_FINAL_L2U_DLY: This field indicates the receive FIFO final load to unload delay. For the setting X, the latency is 4 x X to 4 x X + 4 UI. The default is 8 - 12 UI.
56:59	RWX	RX_WT_TIMEOUT_SEL: This field selects the wire-test timeout value.
60:63	RO	constant = 0b0000

Register Name	Receive CTL Mode 5 E Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE5_E_PG
Address	8009B0200601143F (SCOM)
Description	This register contains the fifth set of receive CTL E mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RWX	RX_FIFO_INITIAL_L2U_DLY: This field indicates the receive FIFO initial load to unload delay. For the setting X, the latency is 4 x X to 4 x X + 4 UI. The default is 16 - 20 UI.
52:55	RWX	RX_FIFO_FINAL_L2U_DLY: This field indicates the receive FIFO final load to unload delay. For the setting X, the latency is 4 x X to 4 x X + 4 UI. The default is 8 - 12 UI.
56:59	RWX	RX_WT_TIMEOUT_SEL: This field selects the wire-test timeout value.
60:63	RO	constant = 0b0000

Register Name	Receive CTL Mode 6 E Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE6_E_PG
Address	8009B8000601143F (SCOM)
Description	This register contains the sixth set of receive CTL E mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_TX_BUS_WIDTH: This field contains the transmit bus width.
55:61	RWX	RX_RX_BUS_WIDTH: This field contains the receive bus width.
62:63	RO	constant = 0b00

Register Name	Receive CTL Mode 6 E Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE6_E_PG
Address	8009B8200601143F (SCOM)
Description	This register contains the sixth set of receive CTL E mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_TX_BUS_WIDTH: This field contains the transmit bus width.
55:61	RWX	RX_RX_BUS_WIDTH: This field contains the receive bus width.
62:63	RO	constant = 0b00

Register Name	Receive CTL Mode 7 E Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE7_E_PG
Address	8009C0000601143F (SCOM)
Description	This register contains the seventh set of receive CTL E mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_SLS_DISABLE: This bit disables receiving and decoding SLS commands.

Bits	SCOM	Field Mnemonic: Description
49	RWX	TX_SLS_DISABLE: If set, the SLS command being sent is always just be a NOP. To actually disable the full SLS logic path, also perform some combination of the following: • Set the rx_sls_disable. • Manually override the tx_snd_sls_cmd_gcrmsg per pack registers. (However, if you do not also disable the various sending SMs, this will eventually get overwritten.) • Set tx_sls_lane_val_gcrmsg to 0. (If there is no valid transmit SLS lane, no SLS command gets sent on it). • Disable the recalibration, repair, and recovery SMs (rx_dyn_recal_suspend, rx_dyn_rpr_disable, rx_sls_rcvy_disable) that initiate the sending of SLS commands.
50:51	RWX	RX_SLS_CNTR_TAP_PTS: This field indicates how long the SLS receive command must be stable. Ensure that this scales with tx_dyn_recal_interval_timeout and status_rpt_timeout. 0b00 = 8 c16 clocks. 0b01 = 16 c16 clocks. 0b10 = 32 c16 clocks. 0b11 = 64 c16 clocks.
52:53	RWX	RX_NONSLS_CNTR_TAP_PTS: This field indicates how long a non-SLS receive command must be stable (to know that we have switched from an SLS command to data). Ensure that this scales with tx_dyn_recal_interval_timeout and status_rpt_timeout. 0b00 = 16 c16 clocks. 0b01 = 32 c16 clocks. 0b10 = 64 c16 clocks. 0b11 = 128 c16 clocks.
54:58	RO	constant = 0b00000
59	RWX	RX_SLS_EXCEPTION2_CS: This is a debug switch for the SLS exception2 command. Set this bit when mixing allv3 and later logic with logic previous to allv3. If set to 1, set rx_sls_timeout_sel to more than four times recal_overall_timeout_sel to avoid sending an exception on an SR interval and seeing a false exception RESMR.
60:61	RWX	RX_DYN_RPR_ERR_CNTR1_FILTER_MODE: To counteract possible DFE error ringing, select a filter that ignores syndrome tally errors for a number of fast clock cycles after a counted error. 0b00 = No filter, counts all errors. 0b01 = Skips one cycle after any error cycle. 0b10 = Skips three cycles after any error cycle. 0b11 = Skips seven cycles after any error cycle.
62:63	RO	constant = 0b00

Register Name	**Receive CTL Mode 7 E Per-Group Register**
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE7_E_PG
Address	8009C0200601143F (SCOM)
Description	This register contains the seventh set of receive CTL E mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_SLS_DISABLE: This bit disables receiving and decoding SLS commands.
49	RWX	TX_SLS_DISABLE: If set, the SLS command being sent is always just be a NOP. To actually disable the full SLS logic path, also perform some combination of the following: • Set the rx_sls_disable. • Manually override the tx_snd_sls_cmd_gcrmsg per pack registers. (However, if you do not also disable the various sending SMs, this will eventually get overwritten.) • Set tx_sls_lane_val_gcrmsg to 0. (If there is no valid transmit SLS lane, no SLS command gets sent on it). • Disable the recalibration, repair, and recovery SMs (rx_dyn_recal_suspend, rx_dyn_rpr_disable, rx_sls_rcvy_disable) that initiate the sending of SLS commands.

Bits	SCOM	Field Mnemonic: Description
50:51	RWX	RX_SLS_CNTR_TAP_PTS: This field indicates how long the SLS receive command must be stable. Ensure that this scales with tx_dyn_recal_interval_timeout and status_rpt_timeout. 0b00 = 8 c16 clocks. 0b01 = 16 c16 clocks. 0b10 = 32 c16 clocks. 0b11 = 64 c16 clocks.
52:53	RWX	RX_NONSLS_CNTR_TAP_PTS: This field indicates how long a non-SLS receive command must be stable (to know that we have switched from an SLS command to data). Ensure that this scales with tx_dyn_recal_interval_timeout and status_rpt_timeout. 0b00 = 16 c16 clocks. 0b01 = 32 c16 clocks. 0b10 = 64 c16 clocks. 0b11 = 128 c16 clocks.
54:58	RO	constant = 0b00000
59	RWX	RX_SLS_EXCEPTION2_CS: This is a debug switch for the SLS exception2 command. Set this bit when mixing allv3 and later logic with logic previous to allv3. If set to 1, set rx_sls_timeout_sel to more than four times recal_overall_timeout_sel to avoid sending an exception on an SR interval and seeing a false exception RESMR.
60:61	RWX	RX_DYN_RPR_ERR_CNTR1_FILTER_MODE: To counteract possible DFE error ringing, select a filter that ignores syndrome tally errors for a number of fast clock cycles after a counted error. 0b00 = No filter, counts all errors. 0b01 = Skips one cycle after any error cycle. 0b10 = Skips three cycles after any error cycle. 0b11 = Skips seven cycles after any error cycle.
62:63	RO	constant = 0b00

Register Name	**Receive CTL Mode 8 E Per-Group Register**
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE8_E_PG
Address	8009C8000601143F (SCOM)
Description	This register contains CRC/ECC dynamic repair information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_DYN_RPR_BAD_LANE_MAX: CRC/ECC dynamic repair. This field indicates the maximum number of times a lane can be found bad before it is repaired.

Bits	SCOM	Field Mnemonic: Description
55:58	RWX	RX_DYN_RPR_ERR_CNTR1_DURATION: CRC/ECC dynamic repair. This field indicates how long lane error counter 1 can run before it is cleared. This determines what error frequency is allowed. In slow clock cycles: 0b0000 = 32. 0b0001 = 1024. 0b0010 = 32 K. 0b0011 = 1 M. 0b0100 = 2 M. 0b0101 = 4 M. 0b0110 = 8 M. 0b0111 = 16 M. 0b1000 = 32 M. 0b1001 = 64 M. 0b1010 = 128 M. 0b1011 = 256 M. 0b1100 = 512 M. 0b1101 = 1 G. 0b1110 = 2 G. 0b1111 = Infinite.
59	RWX	RX_DYN_RPR_CLR_ERR_CNTR1: CRC/ECC dynamic repair. This bit enables firmware-based clearing of the Lane Error Counter1 Register.
60	RWX	RX_DYN_RPR_DISABLE: CRC/ECC dynamic repair. When set, this bit disables dynamic repair error tallying for both per-lane and per-bus error counters (cntr1 and cntr2).
61:63	RWX	RX_DYN_RPR_ENC_BAD_DATA_LANE_WIDTH: CRC/ECC dynamic repair. This field contains the width of the enc_bad_data_lane vector used to determine the number of ones in the clear code.

Register Name	Receive CTL Mode 8 E Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE8_E_PG
Address	8009C8200601143F (SCOM)
Description	This register contains CRC/ECC dynamic repair information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_DYN_RPR_BAD_LANE_MAX: CRC/ECC dynamic repair. This field indicates the maximum number of times a lane can be found bad before it is repaired.

Bits	SCOM	Field Mnemonic: Description
55:58	RWX	RX_DYN_RPR_ERR_CNTR1_DURATION: CRC/ECC dynamic repair. This field indicates how long lane error counter 1 can run before it is cleared. This determines what error frequency is allowed. In slow clock cycles: 0b0000 = 32. 0b0001 = 1024. 0b0010 = 32 K. 0b0011 = 1 M. 0b0100 = 2 M. 0b0101 = 4 M. 0b0110 = 8 M. 0b0111 = 16 M. 0b1000 = 32 M. 0b1001 = 64 M. 0b1010 = 128 M. 0b1011 = 256 M. 0b1100 = 512 M. 0b1101 = 1 G. 0b1110 = 2 G. 0b1111 = Infinite.
59	RWX	RX_DYN_RPR_CLR_ERR_CNTR1: CRC/ECC dynamic repair. This bit enables firmware-based clearing of the Lane Error Counter1 Register.
60	RWX	RX_DYN_RPR_DISABLE: CRC/ECC dynamic repair. When set, this bit disables dynamic repair error tallying for both per-lane and per-bus error counters (cntr1 and cntr2).
61:63	RWX	RX_DYN_RPR_ENC_BAD_DATA_LANE_WIDTH: CRC/ECC dynamic repair. This field contains the width of the enc_bad_data_lane vector used to determine the number of ones in the clear code.

Register Name	**Receive CTL Mode 9 E Per-Group Register**
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE9_E_PG
Address	8009D0000601143F (SCOM)
Description	This register contains CRC/ECC dynamic repair information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_DYN_RPR_BAD_BUS_MAX: CRC/ECC dynamic repair. This field indicates the maximum number of times CRC or ECC errors can be found on the bus (not included in the bad lane cntr1 tally) before setting a FIR error.

Bits	SCOM	Field Mnemonic: Description
55:58	RWX	RX_DYN_RPR_ERR_CNTR2_DURATION: CRC/ECC dynamic repair. This field indicates how long the bad bus cntr2 error counter can run before it is divided by 2. This determines what error frequency is allowed. On a 833 ps and 1250 ps slow clock: 0b0000 = 26.7 ns and 40.0 nS. 0b0001 = 853.0 ns and 1.3 μS. 0b0010 = 27.3 μS and 41.0 μS. 0b0011 = 873.5 μS and 1.3 mS. 0b0100 = 1.7 mS and 2.6 mS. 0b0101 = 3.5 mS and 5.1 mS. 0b0110 = 7.0 mS and 10.5 mS. 0b0111 = 14.0 mS and 21.0 mS. 0b1000 = 28.0 mS and 41.9 mS. 0b1001 = 55.9 mS and 83.9 mS. 0b1010 = 111.8 mS and 167.8 mS. 0b1011 = 223.6 mS and 335.5 mS. 0b1100 = 447.2 mS and 671.1 mS. 0b1101 = 894.4 mS and 1.3 S. 0b1110 = 1.8 S and 2.7 S. 0b1111 = Infinite.
59	RWX	RX_DYN_RPR_CLR_ERR_CNTR2: CRC/ECC dynamic repair. This bit enables firmware-based clearing of the Bus Error Counter2 Register.
60	RWX	RX_DYN_RPR_DISABLE2: CRC/ECC dynamic repair. When set, this bit disables the repair from the dynamic repair error tallying for both per-lane and per-bus error counters (cntr1 and cntr2). However, it leaves the counters running.
61:63	RO	constant = 0b000

Register Name	**Receive CTL Mode 9 E Per-Group Register**
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE9_E_PG
Address	8009D0200601143F (SCOM)
Description	This register contains CRC/ECC dynamic repair information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_DYN_RPR_BAD_BUS_MAX: CRC/ECC dynamic repair. This field indicates the maximum number of times CRC or ECC errors can be found on the bus (not included in the bad lane cntr1 tally) before setting a FIR error.

Bits	SCOM	Field Mnemonic: Description
55:58	RWX	RX_DYN_RPR_ERR_CNTR2_DURATION: CRC/ECC dynamic repair. This field indicates how long the bad bus cntr2 error counter can run before it is divided by 2. This determines what error frequency is allowed. On a 833 ps and 1250 ps slow clock: 0b0000 = 26.7 ns and 40.0 nS. 0b0001 = 853.0 ns and 1.3 µS . 0b0010 = 27.3 µS and 41.0 µS . 0b0011 = 873.5 µS and 1.3 mS. 0b0100 = 1.7 mS and 2.6 mS. 0b0101 = 3.5 mS and 5.1 mS. 0b0110 = 7.0 mS and 10.5 mS. 0b0111 = 14.0 mS and 21.0 mS. 0b1000 = 28.0 mS and 41.9 mS. 0b1001 = 55.9 mS and 83.9 mS. 0b1010 = 111.8 mS and 167.8 mS. 0b1011 = 223.6 mS and 335.5 mS. 0b1100 = 447.2 mS and 671.1 mS. 0b1101 = 894.4 mS and 1.3 S. 0b1110 = 1.8 S and 2.7 S. 0b1111 = Infinite.
59	RWX	RX_DYN_RPR_CLR_ERR_CNTR2: CRC/ECC dynamic repair. This bit enables firmware-based clearing of the Bus Error Counter2 Register.
60	RWX	RX_DYN_RPR_DISABLE2: CRC/ECC dynamic repair. When set, this bit disables the repair from the dynamic repair error tallying for both per-lane and per-bus error counters (cntr1 and cntr2). However, it leaves the counters running.
61:63	RO	constant = 0b000

Register Name	Receive CTL Mode 10 E Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE10_E_PG
Address	8009D8000601143F (SCOM)
Description	This register contains the maximum deskew limit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_DESKEW_MAX_LIMIT: This field contains the maximum deskewable skew fail threshold.
52:63	RO	constant = 0b000000000000

Register Name	Receive CTL Mode 10 E Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE10_E_PG
Address	8009D8200601143F (SCOM)
Description	This register contains the maximum deskew limit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_DESKEW_MAX_LIMIT: This field contains the maximum deskewable skew fail threshold.
52:63	RO	constant = 0b000000000000

Register Name	Receive CTL Mode 11 E Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE11_E_PG
Address	8009E0000601143F (SCOM)
Description	This register sets which lanes are ignored by the training logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RWX	RX_LANE_DISABLED_VEC_0_15: This field is used to set which lanes, of group lanes 0 - 15, are ignored by the training logic. This does not affect power down. **Note:** Disabled lanes must be contiguous.

Register Name	Receive CTL Mode 11 E Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE11_E_PG
Address	8009E0200601143F (SCOM)
Description	This register sets which lanes are ignored by the training logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RWX	RX_LANE_DISABLED_VEC_0_15: This field is used to set which lanes, of group lanes 0 - 15, are ignored by the training logic. This does not affect power down. **Note:** Disabled lanes must be contiguous.

Register Name	Receive CTL Mode 12 E Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE12_E_PG
Address	8009E8000601143F (SCOM)
Description	This register sets which lanes are ignored by the training logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_LANE_DISABLED_VEC_16_23: This field is used to set which lanes, of group lanes 16 - 23, are ignored by the training logic. This does not affect power down. **Note:** Disabled lanes must be contiguous.
56:63	RO	constant = 0b00000000

Register Name	Receive CTL Mode 12 E Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE12_E_PG
Address	8009E8200601143F (SCOM)
Description	This register sets which lanes are ignored by the training logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RWX	RX_LANE_DISABLED_VEC_16_23: This field is used to set which lanes, of group lanes 16 - 23, are ignored by the training logic. This does not affect power down. **Note:** Disabled lanes must be contiguous.
56:63	RO	constant = 0b00000000

Register Name	**Receive CTL CNTL1 E Per-Group Register**
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL1_E_PG
Address	8009F0000601143F (SCOM)
Description	This register controls the training state machine.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_START_WIRETEST: When this register is written to a 1, the training state machine runs the wire-test portion of the training states.
49	RWX	RX_START_DESKEW: When this register is written to a 1, the training state machine runs the deskew portion of the training states.
50	RWX	RX_START_EYE_OPT: When this register is written to a 1, the training state machine runs the data eye-optimization portion of the training states.
51	RWX	RX_START_REPAIR: When this register is written to a 1, the training state machine runs the static lane-repair portion of the training states.
52	RWX	RX_START_FUNC_MODE: When this register is written to a 1, the training state machine runs the transition-to-functional-data portion of the training states.
53	RWX	RX_START_DC_CALIBRATE: When this register is written to a 1, the training state machine runs the DC calibrate substeps defined in eye optimizations.
54:63	RO	constant = 0b0000000000

Register Name	**Receive CTL CNTL1 E Per-Group Register**
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL1_E_PG
Address	8009F0200601143F (SCOM)
Description	This register controls the training state machine.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_START_WIRETEST: When this register is written to a 1, the training state machine runs the wire-test portion of the training states.
49	RWX	RX_START_DESKEW: When this register is written to a 1, the training state machine runs the deskew portion of the training states.
50	RWX	RX_START_EYE_OPT: When this register is written to a 1, the training state machine runs the data eye-optimization portion of the training states.
51	RWX	RX_START_REPAIR: When this register is written to a 1, the training state machine runs the static lane-repair portion of the training states.
52	RWX	RX_START_FUNC_MODE: When this register is written to a 1, the training state machine runs the transition-to-functional-data portion of the training states.

Bits	SCOM	Field Mnemonic: Description
53	RWX	RX_START_DC_CALIBRATE: When this register is written to a 1, the training state machine runs the DC calibrate substeps defined in eye optimizations.
54:63	RO	constant = 0b0000000000

Register Name	**Receive CTL CNTL4 E Per-Group Register**
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL4_E_PG
Address	8009F8000601143F (SCOM)
Description	This register contains the fourth set of CTL CNTL E fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_WT_CU_PLL_PGOOD: This bit enables the PLL/DLL. 0b1 = Sets PGOOD on the receive PLL for locking. 0b0 = Places the receive PLL in reset.
49	RWX	RX_WT_CU_BYP_PLL_LOCK: This bit overrides the receive PLL/DLL lock. It must be ORed into places where PLL locked is checked (that is, the WT state machine). It is used to bypass waiting for a PLL lock.
50	RWX	RX_WT_PLL_REFCLKSEL: This bit selects between the I/O clock and the BIST reference clock. 0b0 = Selects the I/O clock. 0b1 = Selects the BIST reference clock.
51	RWX	RX_PLL_REFCLKSEL_SCOM_EN: This bit selects between the PLL controls and the GCR register to select the reference clock. 0b0 = Uses the PLL control to select the reference clock. 0b1 = Uses the GCR register, rx_wt_pll_refclksel, to select the reference clock.
52	RWX	RX_IORESET: This bit resets the given receive clock group, including the GCR slave.
53:63	RO	constant = 0b00000000000

Register Name	**Receive CTL CNTL4 E Per-Group Register**
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL4_E_PG
Address	8009F8200601143F (SCOM)
Description	This register contains the fourth set of CTL CNTL E fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_WT_CU_PLL_PGOOD: This bit enables the PLL/DLL. 0b1 = Sets PGOOD on the receive PLL for locking. 0b0 = Places the receive PLL in reset.
49	RWX	RX_WT_CU_BYP_PLL_LOCK: This bit overrides the receive PLL/DLL lock. It must be ORed into places where PLL locked is checked (that is, the WT state machine). It is used to bypass waiting for a PLL lock.
50	RWX	RX_WT_PLL_REFCLKSEL: This bit selects between the I/O clock and the BIST reference clock. 0b0 = Selects the I/O clock. 0b1 = Selects the BIST reference clock.
51	RWX	RX_PLL_REFCLKSEL_SCOM_EN: This bit selects between the PLL controls and the GCR register to select the reference clock. 0b0 = Uses the PLL control to select the reference clock. 0b1 = Uses the GCR register, rx_wt_pll_refclksel, to select the reference clock.

Bits	SCOM	Field Mnemonic: Description
52	RWX	RX_IORESET: This bit resets the given receive clock group, including the GCR slave.
53:63	RO	constant = 0b00000000000

Register Name	**Receive CTL CNTL4 E Per-Group Register**
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTLX11_E_PG
Address	800A30000601143F (SCOM)
Description	This register contains the 11th set of CTL CNTL E fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_DESKEW_SEQ_GCRMSG: Receive deskew sequencer GCR messages. 0b000 = Indicate that the prior group deskewed. 0b001 = Indicate that all groups deskewed. 0b010 = Indicate that the prior group completed deskew. 0b011 = Indicate that all groups completed deskew. 0b100 = Transmit skew values from the prior group. 0b101 = Transmit the maximum skew values to all groups. 0b110 = Unused. 0b111 = No message.
51	RO	constant = 0b0
52:55	RWX	RX_DESKEW_SKMIN_GCRMSG: This field contains the minimum skew value for the deskew sequence.
56:59	RWX	RX_DESKEW_SKMAX_GCRMSG: This field contains the maximum skew value for the deskew sequence.
60:63	RO	constant = 0b0000

Register Name	**Receive CTL CNTLX11 E Per_Group Register**
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTLX11_E_PG
Address	800A30200601143F (SCOM)
Description	This register contains the 11th set of CTL CNTLX E fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_DESKEW_SEQ_GCRMSG: Receive deskew sequencer GCR messages. 0b000 = Indicate that the prior group deskewed. 0b001 = Indicate that all groups deskewed. 0b010 = Indicate that the prior group completed deskew. 0b011 = Indicate that all groups completed deskew. 0b100 = Transmit skew values from the prior group. 0b101 = Transmit the maximum skew values to all groups. 0b110 = Unused. 0b111 = No message.
51	RO	constant = 0b0
52:55	RWX	RX_DESKEW_SKMIN_GCRMSG: This field contains the minimum skew value for the deskew sequence.
56:59	RWX	RX_DESKEW_SKMAX_GCRMSG: This field contains the maximum skew value for the deskew sequence.
60:63	RO	constant = 0b0000

Register Name	Receive CTL STAT1 E Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_STAT1_E_PG
Address	800A38000601143F (SCOM)
Description	This register contains the first set of CTL status E fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_WIRETEST_DONE: When this bit is read as a 1, the wire-test training state has completed. Check the corresponding rx_ts_*_failed register field for the pass/fail status of this training state.
49	RWX	RX_DESKEW_DONE: When this bit is read as a 1, the deskew training state has completed. Check the corresponding rx_ts_*_failed register field for the pass/fail status of this training state.
50	RWX	RX_EYE_OPT_DONE: When this bit is read as a 1, the eye-optimization training state has completed. Check the corresponding rx_ts_*_failed register field for the pass/fail status of this training state.
51	RWX	RX_REPAIR_DONE: When this bit is read as a 1, the static-lane-repair training state has completed. Check the corresponding rx_ts_*_failed register field for the pass/fail status of this training state.
52	RWX	RX_FUNC_MODE_DONE: When this bit is read as a 1, the transition-to-functional-data training state has completed. Check the corresponding rx_ts_*_failed register field for the pass/fail status of this training state.
53	RWX	RX_DC_CALIBRATE_DONE: When this bit is read as a 1, the DC calibration steps have been completed. Check the corresponding rx_dc_calibration_failed register field for the pass/fail status of the operation state.
54:55	RO	constant = 0b00
56	RWX	RX_WIRETEST_FAILED: When this bit is read as a 1, the wire-test training state encountered an error.
57	RWX	RX_DESKEW_FAILED: When this bit is read as a 1, the deskew training state encountered an error.
58	RWX	RX_EYE_OPT_FAILED: When this bit is read as a 1, the eye-optimization training state encountered an error.
59	RWX	RX_REPAIR_FAILED: When this bit is read as a 1, the static-lane-repair training state encountered an error.
60:63	RO	constant = 0b0000

Register Name	Receive CTL STAT1 E Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_STAT1_E_PG
Address	800A38200601143F (SCOM)
Description	This register contains the first set of CTL status E fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_WIRETEST_DONE: When this bit is read as a 1, the wire-test training state has completed. Check the corresponding rx_ts_*_failed register field for the pass/fail status of this training state.
49	RWX	RX_DESKEW_DONE: When this bit is read as a 1, the deskew training state has completed. Check the corresponding rx_ts_*_failed register field for the pass/fail status of this training state.
50	RWX	RX_EYE_OPT_DONE: When this bit is read as a 1, the eye-optimization training state has completed. Check the corresponding rx_ts_*_failed register field for the pass/fail status of this training state.
51	RWX	RX_REPAIR_DONE: When this bit is read as a 1, the static-lane-repair training state has completed. Check the corresponding rx_ts_*_failed register field for the pass/fail status of this training state.
52	RWX	RX_FUNC_MODE_DONE: When this bit is read as a 1, the transition-to-functional-data training state has completed. Check the corresponding rx_ts_*_failed register field for the pass/fail status of this training state.

Bits	SCOM	Field Mnemonic: Description
53	RWX	RX_DC_CALIBRATE_DONE: When this bit is read as a 1, the DC calibration steps have been completed. Check the corresponding rx_dc_calibration_failed register field for the pass/fail status of the operation state.
54:55	RO	constant = 0b00
56	RWX	RX_WIRETEST_FAILED: When this bit is read as a 1, the wire-test training state encountered an error.
57	RWX	RX_DESKEW_FAILED: When this bit is read as a 1, the deskew training state encountered an error.
58	RWX	RX_EYE_OPT_FAILED: When this bit is read as a 1, the eye-optimization training state encountered an error.
59	RWX	RX_REPAIR_FAILED: When this bit is read as a 1, the static-lane-repair training state encountered an error.
60:63	RO	constant = 0b0000

Register Name	**Receive CTL STAT 2 E Per-Group Register**
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_STAT2_E_PG
Address	800A40000601143F (SCOM)
Description	This register contains the second set of CTL status E fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RWX	RX_LANE_BAD_VEC_0_15: This field is used to report lanes found bad by hardware (status) or as a method to force a lane bad from software (control). The bad_lane vector is only updated during initial training.

Register Name	**Receive CTL STAT 2 E Per-Group Register**
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_STAT2_E_PG
Address	800A40200601143F (SCOM)
Description	This register contains the second set of CTL status E fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RWX	RX_LANE_BAD_VEC_0_15: This field is used to report lanes found bad by hardware (status) or as a method to force a lane bad from software (control). The bad_lane vector is only updated during initial training.

Register Name	**Receive CTL STAT 4 E Per-Group Register**
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_STAT4_E_PG
Address	800A50000601143F (SCOM)
Description	This register contains the fourth set of CTL status E fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_LANE_BAD_VEC_16_23: This field is used to report lanes found bad by hardware (status) or as a method to force a lane bad from software (control).
56:63	RO	constant = 0b00000000

Register Name	**Receive CTL STAT 4 E Per-Group Register**
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_STAT4_E_PG
Address	800A50200601143F (SCOM)
Description	This register contains the fourth set of CTL status E fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_LANE_BAD_VEC_16_23: This field is used to report lanes found bad by hardware (status) or as a method to force a lane bad from software (control).
56:63	RO	constant = 0b00000000

Register Name	**Receive CTL STAT 5 E Per-Group Register**
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_STAT5_E_PG
Address	800A58000601143F (SCOM)
Description	This register contains the fifth set of CTL status E fields.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant = 0b0000000000000000000000000000000000000000000000000
49	RWX	RX_WT_CLK_LANE_INVERTED: Clock wire-test lane inverted/swapped status. 0b0 = Not swapped or inverted. 0b1 = P-N swapped or inverted.
50:52	RWX	RX_WT_CLK_LANE_BAD_CODE: Clock wire-test lane bad code. 0b000 = Lane tested good. 0b001 = N leg stuck at 1. 0b010 = N leg stuck at 0. 0b011 = P leg stuck at 1. 0b100 = P leg stuck at 0. 0b101 = N or P leg floating or swapping undetermined. 0b110 = Unused. 0b111 = Unused.
53:63	RO	constant = 0b00000000000

Register Name	**Receive CTL STAT 5 E Per-Group Register**
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_STAT5_E_PG
Address	800A58200601143F (SCOM)
Description	This register contains the fifth set of CTL status E fields.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant = 0b0000000000000000000000000000000000000000000000000
49	RWX	RX_WT_CLK_LANE_INVERTED: Clock wire-test lane inverted/swapped status. 0b0 = Not swapped or inverted. 0b1 = P-N swapped or inverted.

Bits	SCOM	Field Mnemonic: Description
50:52	RWX	RX_WT_CLK_LANE_BAD_CODE: Clock wire-test lane bad code. 0b000 = Lane tested good. 0b001 = N leg stuck at 1. 0b010 = N leg stuck at 0. 0b011 = P leg stuck at 1. 0b100 = P leg stuck at 0. 0b101 = N or P leg floating or swapping undetermined. 0b110 = Unused. 0b111 = Unused.
53:63	RO	constant = 0b00000000000

Register Name	**Receive CTL STAT 6 E Per-Group Register**
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_STAT6_E_PG
Address	800A60000601143F (SCOM)
Description	This register contains the sixth set of CTL status E fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_DESKEW_MINSKEW_GRP: This field contains the deskew per-group raw skew minimum.
52:55	RWX	RX_DESKEW_MAXSKEW_GRP: This field contains the deskew per-group raw skew maximum.
56:63	RO	constant = 0b00000000

Register Name	**Receive CTL STAT 6 E Per-Group Register**
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_STAT6_E_PG
Address	800A60200601143F (SCOM)
Description	This register contains the sixth set of CTL status E fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_DESKEW_MINSKEW_GRP: This field contains the deskew per-group raw skew minimum.
52:55	RWX	RX_DESKEW_MAXSKEW_GRP: This field contains the deskew per-group raw skew maximum.
56:63	RO	constant = 0b00000000

Register Name	**Receive CTL STATX 8 E Per-Group Register**
Mnemonic	IOF2.RX.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_STATX8_E_PG
Address	800A68000601143F (SCOM)
Description	This register contains the eighth set of CTL status E fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_WT_PREV_DONE_GCRMSG: This bit indicates the the previous clock group completed the wire test.
49	RWX	RX_WT_ALL_DONE_GCRMSG: This bit indicates that all clock groups completed the wire test.

Bits	SCOM	Field Mnemonic: Description
50:51	RO	constant = 0b00
52	RWX	RX_CNTLS_PREV_LDED_GCRMSG: This bit indicates that the previous clock group finished updating the receive SLS/bad lane and repair controls.
53:63	RO	constant = 0b00000000000

Register Name	Receive CTL STATX 8 E Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_STATX8_E_PG
Address	800A68200601143F (SCOM)
Description	This register contains the eighth set of CTL status E fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_WT_PREV_DONE_GCRMSG: This bit indicates the the previous clock group completed the wire test.
49	RWX	RX_WT_ALL_DONE_GCRMSG: This bit indicates that all clock groups completed the wire test.
50:51	RO	constant = 0b00
52	RWX	RX_CNTLS_PREV_LDED_GCRMSG: This bit indicates that the previous clock group finished updating the receive SLS/bad lane and repair controls.
53:63	RO	constant = 0b00000000000

Register Name	Receive GLBSM Spare Mode Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_SPARE_MODE_PG
Address	800A80000601143F (SCOM)
Description	This register contains per-group controls and spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PG_GLBSM_SPARE_MODE_0: Per-group spare mode latch.
49	RWX	RX_PG_GLBSM_SPARE_MODE_1: Per-group spare mode latch.
50	RWX	RX_PG_GLBSM_SPARE_MODE_2: Per-group spare mode latch.
51	RWX	RX_PG_GLBSM_SPARE_MODE_3: Per-group spare mode latch.
52	RWX	RX_PG_GLBSM_SPARE_MODE_4: Per-group spare mode latch.
53	RWX	RX_PG_GLBSM_SPARE_MODE_5: Per-group spare mode latch.
54	RWX	RX_PG_GLBSM_SPARE_MODE_6: Per-group spare mode latch.
55	RWX	RX_PG_GLBSM_SPARE_MODE_7: Per-group spare mode latch.
56	RWX	RX_DESKEW_BUMP_AFTER: During deskew, choose to bump the clock to the center of the data after the lane deskewing operations have completed or before PRBS synchronization. 0b0 = Bump to center before deskew starts. 0b1 = Bump to center before PRBS synchronization starts.
57	RWX	RX_SLS_RCVY_DISABLE: This bit disables the SLS recovery state machine.
58:63	RO	constant = 0b000000

Register Name	Receive GLBSM Spare Mode Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_GLBSM_SPARE_MODE_PG
Address	800A80200601143F (SCOM)
Description	This register contains per-group controls and spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PG_GLBSM_SPARE_MODE_0: Per-group spare mode latch.
49	RWX	RX_PG_GLBSM_SPARE_MODE_1: Per-group spare mode latch.
50	RWX	RX_PG_GLBSM_SPARE_MODE_2: Per-group spare mode latch.
51	RWX	RX_PG_GLBSM_SPARE_MODE_3: Per-group spare mode latch.
52	RWX	RX_PG_GLBSM_SPARE_MODE_4: Per-group spare mode latch.
53	RWX	RX_PG_GLBSM_SPARE_MODE_5: Per-group spare mode latch.
54	RWX	RX_PG_GLBSM_SPARE_MODE_6: Per-group spare mode latch.
55	RWX	RX_PG_GLBSM_SPARE_MODE_7: Per-group spare mode latch.
56	RWX	RX_DESKEW_BUMP_AFTER: During deskew, choose to bump the clock to the center of the data after the lane deskewing operations have completed or before PRBS synchronization. 0b0 = Bump to center before deskew starts. 0b1 = Bump to center before PRBS synchronization starts.
57	RWX	RX_SLS_RCVY_DISABLE: This bit disables the SLS recovery state machine.
58:63	RO	constant = 0b000000

Register Name	Receive FIR1 Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_FIR1_PG
Address	800A88000601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	ROX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
60	ROX	Reserved field.
61	ROX	Reserved field.
62	ROX	Reserved field.
63	RO	constant = 0b0

Register Name	Receive FIR1 Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_FIR1_PG
Address	800A88200601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	ROX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60	ROX	Reserved field.
61	ROX	Reserved field.
62	ROX	Reserved field.
63	RO	constant = 0b0

Register Name	Receive FIR1 Mask Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_FIR1_MASK_PG
Address	800A90000601143F (SCOM)
Description	This register masks receive FIR per-group errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:62	RWX	RX_Per Group_FIR1_ERRS_MASK: This field provides a FIR mask for register or state-machine parity checkers in the per-group receive logic. A value of 1 masks the error from generating a FIR error. Bit 0 = (mask_pg_regs) RXCTL Register parity error mask. Bit 1 = Reserved. Bit 2 = Reserved. Bit 3 = (mask_gcrs_ld_sm) RXCTL GCR load state machine parity error mask. Bit 4 = (mask_gcrs_unld_sm) RXCTL GCR unload state machine parity error mask. Bit 5 = (mask_snd_msg_sm) RXCTL Send message parity error mask. Bit 6 = (mask_main_init_sm) RXCTL main init state machine parity error mask. Bit 7 = (mask_wtm_sm) RXCTL wire-test main state machine parity error mask.
63	RO	constant = 0b0

Register Name	Receive FIR1 Mask Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_FIR1_MASK_PG
Address	800A90200601143F (SCOM)
Description	This register masks receive FIR per-group errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:62	RWX	RX_Per Group_FIR1_ERRS_MASK: This field provides a FIR mask for register or state-machine parity checkers in the per-group receive logic. A value of 1 masks the error from generating a FIR error. Bit 0 = (mask_pg_regs) RXCTL Register parity error mask. Bit 1 = Reserved. Bit 2 = Reserved. Bit 3 = (mask_gcrs_ld_sm) RXCTL GCR load state machine parity error mask. Bit 4 = (mask_gcrs_unld_sm) RXCTL GCR unload state machine parity error mask. Bit 5 = (mask_snd_msg_sm) RXCTL Send message parity error mask. Bit 6 = (mask_main_init_sm) RXCTL main init state machine parity error mask. Bit 7 = (mask_wtm_sm) RXCTL wire-test main state machine parity error mask.
63	RO	constant = 0b0

Register Name	Receive FIR1 Error Inject Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_FIR1_ERROR_INJECT_PG
Address	800A98000601143F (SCOM)
Description	This register is used to inject parity errors into the per-group receive registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:62	RWX	RX_PG_FIR1_ERR_INJ: IOTK ALIAS: Receive per-group parity error injection. This field enables the injection of non-destructive parity errors in either register or state-machine latch banks. The register or state value is not affected.
63	RO	constant = 0b0

Register Name	Receive FIR1 Error Inject Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_FIR1_ERROR_INJECT_PG
Address	800A98200601143F (SCOM)
Description	This register is used to inject parity errors into the per-group receive registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:62	RWX	RX_PG_FIR1_ERR_INJ: IOTK ALIAS: Receive per-group parity error injection. This field enables the injection of non-destructive parity errors in either register or state-machine latch banks. The register or state value is not affected.
63	RO	constant = 0b0

Register Name	Receive FIR Training Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_FIR_TRAINING_PG
Address	800AA0000601143F (SCOM)
Description	This register is used for FIR training.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PG_FIR_TRAINING_ERROR: This field is now defunct. It is permanently masked in the rx_fir_training_mask_pg FIR isolation register.
49	RWX	RX_PG_FIR_STATIC_SPARE_DEPLOYED: A spare lane was deployed during training to heal a lane that was detected as bad. The RX_Static_Spare_Deployed (SSD) bit is set after the repair training step if, during training, either wire-test, deskew, eye-optimization, or repair operations were detected or one or more bad lanes were detected. The rx_bad_lane_enc_gcrmsg_pg register can be read to isolate which lanes were healed and the rx_bad_lane.
50	RWX	RX_PG_FIR_STATIC_MAX_SPARES_EXCEEDED: A lane was detected as bad during training, but there are no spare lanes available to heal it. This FIR is not set until the repair training step has run. **Note:** This is a catastrophic failure for the bus when in mission mode, but all training steps are still run on whatever good lanes there are. The rx_static_max_spares_exceeded bit is set if wire-test, deskew, eye-optimization or repair operations find an excessive number of bad lanes.
51	RWX	RX_PG_FIR_DYNAMIC_REPAIR_ERROR: A dynamic repair error occurred. The Recal Error FFDC registers can be read to help isolate to a particular piece of logic.
52	RWX	RX_PG_FIR_DYNAMIC_SPARE_DEPLOYED: A spare lane was deployed by the ECC/CRC logic to heal a lane that was detected as bad. The rx_bad_lane_enc_gcrmsg_pg register can be read to isolate which lanes were healed.
53	RWX	RX_PG_FIR_DYNAMIC_MAX_SPARES_EXCEEDED: A lane was detected as bad by the ECC/CRC logic, but there are no spare lanes to heal it. **Note:** This is a catastrophic failure for the bus.
54	RWX	RX_PG_FIR_RECAL_ERROR: A recalibration error occurred. The Recal Error FFDC registers can be read to help isolate the error to a particular piece of logic.
55	RWX	RX_PG_FIR_RECAL_SPARE_DEPLOYED: A spare lane was deployed during recalibration to heal a lane that was detected as bad. The rx_bad_lane_enc_gcrmsg_pg register can be read to isolate which lanes were healed.
56	RWX	RX_PG_FIR_RECAL_MAX_SPARES_EXCEEDED: A lane was detected as bad during recalibration, but there are no spare lanes to heal it. **Note:** This is a catastrophic failure for the bus.

Bits	SCOM	Field Mnemonic: Description
57	RWX	RX_PG_FIR_TOO_MANY_BUS_ERRORS: More than one lane was detected as having too many errors during functional operation. **Note:** This is a catastrophic failure for the bus.
58:63	RO	constant = 0b000000

Register Name	Receive FIR Training Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_FIR_TRAINING_PG
Address	800AA0200601143F (SCOM)
Description	This register is used for FIR training.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PG_FIR_TRAINING_ERROR: This field is now defunct. It is permanently masked in the rx_fir_training_mask_pg FIR isolation register.
49	RWX	RX_PG_FIR_STATIC_SPARE_DEPLOYED: A spare lane was deployed during training to heal a lane that was detected as bad. The RX_Static_Spare_Deployed (SSD) bit is set after the repair training step if, during training, either wire-test, deskew, eye-optimization, or repair operations were detected or one or more bad lanes were detected. The rx_bad_lane_enc_gcrmsg_pg register can be read to isolate which lanes were healed and the rx_bad_lane.
50	RWX	RX_PG_FIR_STATIC_MAX_SPARES_EXCEEDED: A lane was detected as bad during training, but there are no spare lanes available to heal it. This FIR is not set until the repair training step has run. **Note:** This is a catastrophic failure for the bus when in mission mode, but all training steps are still run on whatever good lanes there are. The rx_static_max_spares_exceeded bit is set if wire-test, deskew, eye-optimization or repair operations find an excessive number of bad lanes.
51	RWX	RX_PG_FIR_DYNAMIC_REPAIR_ERROR: A dynamic repair error occurred. The Recal Error FFDC registers can be read to help isolate this error to a particular piece of logic.
52	RWX	RX_PG_FIR_DYNAMIC_SPARE_DEPLOYED: A spare lane was deployed by the ECC/CRC logic to heal a lane that was detected as bad. The rx_bad_lane_enc_gcrmsg_pg register can be read to isolate which lanes were healed.
53	RWX	RX_PG_FIR_DYNAMIC_MAX_SPARES_EXCEEDED: A lane was detected as bad by the ECC/CRC logic, but there are no spare lanes to heal it. **Note:** This is a catastrophic failure for the bus.
54	RWX	RX_PG_FIR_RECAL_ERROR: A recalibration error occurred. The Recal Error FFDC registers can be read to help isolate the error to a particular piece of logic.
55	RWX	RX_PG_FIR_RECAL_SPARE_DEPLOYED: A spare lane was deployed during recalibration to heal a lane that was detected as bad. The rx_bad_lane_enc_gcrmsg_pg register can be read to isolate which lanes were healed.
56	RWX	RX_PG_FIR_RECAL_MAX_SPARES_EXCEEDED: A lane was detected as bad during recalibration, but there are no spare lanes to heal it. **Note:** This is a catastrophic failure for the bus.
57	RWX	RX_PG_FIR_TOO_MANY_BUS_ERRORS: More than one lane was detected as having too many errors during functional operation. **Note:** This is a catastrophic failure for the bus.
58:63	RO	constant = 0b000000

Register Name	Receive FIR Training Mask Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_FIR_TRAINING_MASK_PG
Address	800AA8000601143F (SCOM)
Description	This register masks receive FIR training errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PG_FIR_TRAINING_ERROR_MASK: This bit is the FIR mask for rx_pg_fir_training_error.
49	RWX	RX_PG_FIR_STATIC_SPARE_DEPLOYED_MASK: This bit is the FIR mask for rx_pg_fir_static_spare_deployed.
50	RWX	RX_PG_FIR_STATIC_MAX_SPARES_EXCEEDED_MASK: This bit is the FIR mask for rx_pg_fir_static_max_spares_exceeded.
51	RWX	RX_PG_FIR_DYNAMIC_REPAIR_ERROR_MASK: This bit is the FIR mask for rx_pg_fir_dynamic_repair_error.
52	RWX	RX_PG_FIR_DYNAMIC_SPARE_DEPLOYED_MASK: This bit is the FIR mask for rx_pg_fir_dynamic_spare_deployed.
53	RWX	RX_PG_FIR_DYNAMIC_MAX_SPARES_EXCEEDED_MASK: This bit is the FIR mask for rx_pg_fir_dynamic_max_spares_exceeded.
54	RWX	RX_PG_FIR_RECAL_ERROR_MASK: This bit is the FIR mask for rx_pg_fir_recal_error.
55	RWX	RX_PG_FIR_RECAL_SPARE_DEPLOYED_MASK: This bit is the FIR mask for rx_pg_fir_recal_spare_deployed.
56	RWX	RX_PG_FIR_RECAL_MAX_SPARES_EXCEEDED_MASK: This bit is the FIR mask for rx_pg_fir_recal_max_spares_exceeded.
57	RWX	RX_PG_FIR_TOO_MANY_BUS_ERRORS_MASK: This bit is the FIR mask for rx_pg_fir_too_many_bus_errors.
58:63	RO	constant = 0b000000

Register Name	Receive FIR Training Mask Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_FIR_TRAINING_MASK_PG
Address	800AA8200601143F (SCOM)
Description	This register masks receive FIR training errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PG_FIR_TRAINING_ERROR_MASK: This bit is the FIR mask for rx_pg_fir_training_error.
49	RWX	RX_PG_FIR_STATIC_SPARE_DEPLOYED_MASK: This bit is the FIR mask for rx_pg_fir_static_spare_deployed.
50	RWX	RX_PG_FIR_STATIC_MAX_SPARES_EXCEEDED_MASK: This bit is the FIR mask for rx_pg_fir_static_max_spares_exceeded.
51	RWX	RX_PG_FIR_DYNAMIC_REPAIR_ERROR_MASK: This bit is the FIR mask for rx_pg_fir_dynamic_repair_error.
52	RWX	RX_PG_FIR_DYNAMIC_SPARE_DEPLOYED_MASK: This bit is the FIR mask for rx_pg_fir_dynamic_spare_deployed.
53	RWX	RX_PG_FIR_DYNAMIC_MAX_SPARES_EXCEEDED_MASK: This bit is the FIR mask for rx_pg_fir_dynamic_max_spares_exceeded.

Bits	SCOM	Field Mnemonic: Description
54	RWX	RX_PG_FIR_RECAL_ERROR_MASK: This bit is the FIR mask for rx_pg_fir_recal_error.
55	RWX	RX_PG_FIR_RECAL_SPARE_DEPLOYED_MASK: This bit is the FIR mask for rx_pg_fir_recal_spare_deployed.
56	RWX	RX_PG_FIR_RECAL_MAX_SPARES_EXCEEDED_MASK: This bit is the FIR mask for rx_pg_fir_recal_max_spares_exceeded.
57	RWX	RX_PG_FIR_TOO_MANY_BUS_ERRORS_MASK: This bit is the FIR mask for rx_pg_fir_too_many_bus_errors.
58:63	RO	constant = 0b000000

Register Name	**Receive GLBSM CNTLX1 EO Per-Group Register**
Mnemonic	IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_CNTLX1_EO_PG
Address	800AB0000601143F (SCOM)
Description	This register controls per-group latches.

Bits	SCOM	Field Mnemonic: Description
0:61	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000
62	RWX	RX_CLR_PAR_ERRS: Clear all receive parity error latches. Toggle this field 0→1-→0 to clear all receive parity error latches.
63	RWX	RX_FIR_RESET: FIR reset. Toggle this field 0→1→0 to reset all the receive FIR-related latches including the isolation and parity error latches.

Register Name	**Receive GLBSM CNTLX1 EO Per-Group Register**
Mnemonic	IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_GLBSM_CNTLX1_EO_PG
Address	800AB0200601143F (SCOM)
Description	This register controls per-group latches.

Bits	SCOM	Field Mnemonic: Description
0:61	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000
62	RWX	RX_CLR_PAR_ERRS: Clear all receive parity error latches. Toggle this field 0→1-→0 to clear all receive parity error latches.
63	RWX	RX_FIR_RESET: FIR reset. Toggle this field 0→1→0 to reset all the receive FIR-related latches including the isolation and parity error latches.

Register Name	**Receive GLBSM STAT1 EO Per-Group Register**
Mnemonic	IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_STAT1_EO_PG
Address	800AB8000601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:59	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
60:63	RO	constant = 0b0000

Register Name	Receive GLBSM STAT1 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_GLBSM_STAT1_EO_PG
Address	800AB8200601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Receive GLBSM STAT2 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_STAT2_EO_PG
Address	800AC0000601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	ROX	Reserved field.

Register Name	Receive GLBSM STAT2 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_GLBSM_STAT2_EO_PG
Address	800AC0200601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	ROX	Reserved field.

Register Name	Receive GLBSM STAT3 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_STAT3_EO_PG
Address	800AC8000601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
50	ROX	Reserved field.
51:59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Receive GLBSM STAT3 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_GLBSM_STAT3_EO_PG
Address	800AC8200601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51:59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Receive GLBSM STAT4 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_STAT4_EO_PG
Address	800AD0000601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	ROX	Reserved field.

Register Name	Receive GLBSM STAT4 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_GLBSM_STAT4_EO_PG
Address	800AD0200601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	ROX	Reserved field.

Register Name	Receive GLBSM STAT5 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_STAT5_EO_PG
Address	800AD8000601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50:54	ROX	Reserved field.
55	ROX	Reserved field.
56:63	RO	constant = 0b00000000

Register Name	Receive GLBSM STAT5 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_GLBSM_STAT5_EO_PG
Address	800AD8200601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50:54	ROX	Reserved field.
55	ROX	Reserved field.
56:63	RO	constant = 0b00000000

Register Name	Receive GLBSM CNTL2 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_CNTL2_EO_PG
Address	800AE0000601143F (SCOM)
Description	This register controls single-lane recalibration and dynamic repair.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_DYN_RPR_REQ_MANUAL: When rx_dyn_rpr_sm_manual is set, this bit requests a dynamic repair of the encoded lane set in rx_enc_bus_lane2rpr_manual.
49	RWX	RX_CNT_SINGLE_LANE_RECAL: This bit selects single-lane recalibration monitor mode.
50:54	RWX	RX_RECAL_LANE_TO_MONITOR: This field designates the lane to monitor when rx_cnt_single_lane_recal is 1.
55	RWX	RX_DYN_RPR_SM_MANUAL: When set, this bit only allows the dynamic repair state machine to respond to a repair request from the rx_dyn_rpr_req_manual register bit. To run syndrome tallying without triggering the dynamic repair state machine, set this bit and clear rx_dyn_rpr_disable.

Bits	SCOM	Field Mnemonic: Description
56	RWX	RX_DIS_SYND_TALLYING: When set, this bit prevents syndrome tallying logic from counting any incoming errors reported.
57:63	RWX	RX_ENC_BUS_LANE2RPR_MANUAL: If a manual dynamic repair is requested (rx_dyn_rpr_req_manual), this is the lane to repair. This value must be set to the physical lane to repair, not to the functional data lane.

Register Name	Receive GLBSM CNTL2 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_GLBSM_CNTL2_EO_PG
Address	800AE0200601143F (SCOM)
Description	This register controls single-lane recalibration and dynamic repair.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_DYN_RPR_REQ_MANUAL: When rx_dyn_rpr_sm_manual is set, this bit requests a dynamic repair of the encoded lane set in rx_enc_bus_lane2rpr_manual.
49	RWX	RX_CNT_SINGLE_LANE_RECAL: This bit selects single-lane recalibration monitor mode.
50:54	RWX	RX_RECAL_LANE_TO_MONITOR: This field designates the lane to monitor when rx_cnt_single_lane_recal is 1.
55	RWX	RX_DYN_RPR_SM_MANUAL: When set, this bit only allows the dynamic repair state machine to respond to a repair request from the rx_dyn_rpr_req_manual register bit. To run syndrome tallying without triggering the dynamic repair state machine, set this bit and clear rx_dyn_rpr_disable.
56	RWX	RX_DIS_SYND_TALLYING: When set, this bit prevents syndrome tallying logic from counting any incoming errors reported.
57:63	RWX	RX_ENC_BUS_LANE2RPR_MANUAL: If a manual dynamic repair is requested (rx_dyn_rpr_req_manual), this is the lane to repair. This value must be set to the physical lane to repair, not to the functional data lane.

Register Name	Receive GLBSM CNTL3 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_CNTL3_EO_PG
Address	800AE8000601143F (SCOM)
Description	This register controls manual recalibration and timers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_MANUAL_RECAL_REQUEST: This bit indicates a recalibration request from the microcontroller.
49:50	RO	constant = 0b00
51:55	RWX	RX_MANUAL_RECAL_LANE: This field specifies the recalibration lane from the microcontroller.
56:57	RWX	RX_SLS_TIMEOUT_EXT_SEL: This field selects an extension multiplier for the rx_sls_timeout_sel register.
58	RWX	RX_HALF_RATE_MODE_GLBSM: When set to 1, this bit enables timers on the slow clock domain to consistently count UI when in 4-bit legacy mode. Otherwise, the slow clock domain counts only half of the UI when in 4-bit legacy mode.
59:63	RO	constant = 0b00000

Register Name	**Receive GLBSM CNTL3 EO Per-Group Register**
Mnemonic	IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_GLBSM_CNTL3_EO_PG
Address	800AE8200601143F (SCOM)
Description	This register controls manual recalibration and timers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_MANUAL_RECAL_REQUEST: This bit indicates a recalibration request from the microcontroller.
49:50	RO	constant = 0b00
51:55	RWX	RX_MANUAL_RECAL_LANE: This field specifies the recalibration lane from the microcontroller.
56:57	RWX	RX_SLS_TIMEOUT_EXT_SEL: This field selects an extension multiplier for the rx_sls_timeout_sel register.
58	RWX	RX_HALF_RATE_MODE_GLBSM: When set to 1, this bit enables timers on the slow clock domain to consistently count UI when in 4-bit legacy mode. Otherwise, the slow clock domain counts only half of the UI when in 4-bit legacy mode.
59:63	RO	constant = 0b00000

Register Name	**Receive GLBSM CNTL4 EO Per-Group Register**
Mnemonic	IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_CNTL4_EO_PG
Address	800AF0000601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	**Receive GLBSM CNTL4 EO Per-Group Register**
Mnemonic	IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_GLBSM_CNTL4_EO_PG
Address	800AF0200601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Mode 1 E Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_MODE1_E_PG
Address	800AF8000601143F (SCOM)
Description	This register selects timeout values.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_RPR_TX_LD_CNTLS_TIMEOUT_SEL: This field selects the timeout value for waiting for transmit to load repair controls.
52:55	RWX	RX_TX_SLS_LN_MV_TIMEOUT_SEL: This field selects the timeout value for waiting for transmit to move the SLS lane.
56:63	RO	constant = 0b00000000

Register Name	Receive GLBSM Mode 1 E Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_GLBSM_MODE1_E_PG
Address	800AF8200601143F (SCOM)
Description	This register selects timeout values.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_RPR_TX_LD_CNTLS_TIMEOUT_SEL: This field selects the timeout value for waiting for transmit to load repair controls.
52:55	RWX	RX_TX_SLS_LN_MV_TIMEOUT_SEL: This field selects the timeout value for waiting for transmit to move the SLS lane.
56:63	RO	constant = 0b00000000

Register Name	Receive FIR2 Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_FIR2_PG
Address	800B00000601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	ROX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60	ROX	Reserved field.
61	ROX	Reserved field.
62	ROX	Reserved field.
63	ROX	Reserved field.

Register Name	Receive FIR2 Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_FIR2_PG
Address	800B00200601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	ROX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60	ROX	Reserved field.
61	ROX	Reserved field.
62	ROX	Reserved field.
63	ROX	Reserved field.

Register Name	Receive FIR2 Mask Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_FIR2_MASK_PG
Address	800B08000601143F (SCOM)
Description	This register masks receive FIR2 errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RWX	RX_PG_FIR2_ERRS_MASK: IOTK ALIAS: This field provides a mask for rx_fir2_pg errors.

Register Name	Receive FIR2 Mask Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_FIR2_MASK_PG
Address	800B08200601143F (SCOM)
Description	This register masks receive FIR2 errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RWX	RX_PG_FIR2_ERRS_MASK: IOTK ALIAS: This field provides a mask for rx_fir2_pg errors.

Register Name	Receive FIR2 Error Inject Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_FIR2_ERROR_INJECT_PG
Address	800B10000601143F (SCOM)
Description	This register is used to inject parity errors into the per-group receive registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RWX	RX_PG_FIR2_ERR_INJ: IOTK ALIAS: Receive per-group parity error injection. This field enables the injection of non-destructive parity errors in either register or state-machine latch banks. The register or state value is not affected.

Register Name	Receive FIR2 Error Inject Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_FIR2_ERROR_INJECT_PG
Address	800B10200601143F (SCOM)
Description	This register is used to inject parity errors into the per-group receive registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RWX	RX_PG_FIR2_ERR_INJ: IOTK ALIAS: Receive per-group parity error injection. This field enables the injection of non-destructive parity errors in either register or state-machine latch banks. The register or state value is not affected.

Register Name	Receive GLBSM STAT1 E Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_STAT1_E_PG
Address	800B18000601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	ROX	Reserved field.
52:57	ROX	Reserved field.
58:62	ROX	Reserved field.
63	ROX	Reserved field.

Register Name	Receive GLBSM STAT1 E Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_GLBSM_STAT1_E_PG
Address	800B18200601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	ROX	Reserved field.
52:57	ROX	Reserved field.
58:62	ROX	Reserved field.
63	ROX	Reserved field.

Register Name	Receive GLBSM STAT2 E Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_STAT2_E_PG
Address	800B20000601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	ROX	Reserved field.
53:58	RO	constant = 0b000000
59:63	ROX	Reserved field.

Register Name	Receive GLBSM STAT2 E Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_GLBSM_STAT2_E_PG
Address	800B20200601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	ROX	Reserved field.
53:58	RO	constant = 0b000000
59:63	ROX	Reserved field.

Register Name	Receive GLBSM STAT3 E Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_STAT3_E_PG
Address	800B28000601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50:55	ROX	Reserved field.
56	RO	constant = 0b0
57:63	ROX	Reserved field.

Register Name	Receive GLBSM STAT3 E Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_GLBSM_STAT3_E_PG
Address	800B28200601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50:55	ROX	Reserved field.
56	RO	constant = 0b0
57:63	ROX	Reserved field.

Register Name	Receive GLBSM STAT4 E Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_STAT4_E_PG
Address	800B30000601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	ROX	Reserved field.
55	RO	constant = 0b0
56:60	ROX	Reserved field.
61:63	RO	constant = 0b000

Register Name	Receive GLBSM STAT4 E Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_GLBSM_STAT4_E_PG
Address	800B30200601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	ROX	Reserved field.
55	RO	constant = 0b0
56:60	ROX	Reserved field.
61:63	RO	constant = 0b000

Register Name	Receive GLBSM STAT7 E Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_STAT7_E_PG
Address	800B48000601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50:55	ROX	Reserved field.
56:62	ROX	Reserved field.
63	ROX	Reserved field.

Register Name	Receive GLBSM STAT7 E Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_GLBSM_STAT7_E_PG
Address	800B48200601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50:55	ROX	Reserved field.
56:62	ROX	Reserved field.
63	ROX	Reserved field.

Register Name	Receive GLBSM STAT8 E Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_STAT8_E_PG
Address	800B50000601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	ROX	Reserved field.
49	RO	constant = 0b0
50:55	ROX	Reserved field.
56:63	ROX	Reserved field.

Register Name	Receive GLBSM STAT8 E Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_GLBSM_STAT8_E_PG
Address	800B50200601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	RO	constant = 0b0
50:55	ROX	Reserved field.
56:63	ROX	Reserved field.

Register Name	Receive GLBSM STAT9 E Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_STAT9_E_PG
Address	800B58000601143F (SCOM)
Description	This register contains information about bad lanes.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_BAD_LANE1: Encoded bad lane one in relation to the entire receive bus.
55:61	RWX	RX_BAD_LANE2: Encoded bad lane two in relation to the entire receive bus.
62:63	RWX	RX_BAD_LANE_CODE: Receive bad-lane code. 0b00 = Zero bad lanes. 0b01 = Bad lane 1 valid. 0b10 = Bad lanes 1 and 2 valid. 0b11 = Three or more bad lanes.

Register Name	Receive GLBSM STAT9 E Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_GLBSM_STAT9_E_PG
Address	800B58200601143F (SCOM)
Description	This register contains information about bad lanes.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_BAD_LANE1: Encoded bad lane one in relation to the entire receive bus.
55:61	RWX	RX_BAD_LANE2: Encoded bad lane two in relation to the entire receive bus.

Bits	SCOM	Field Mnemonic: Description
62:63	RWX	RX_BAD_LANE_CODE: Receive bad-lane code. 0b00 = Zero bad lanes. 0b01 = Bad lane 1 valid. 0b10 = Bad lanes 1 and 2 valid. 0b11 = Three or more bad lanes.

Register Name	Receive GLBSM STAT10 E Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_STAT10_E_PG
Address	800B60000601143F (SCOM)
Description	This register indicates the state of servo lane calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_SERVO_RECAL_IP: This bit indicates that receive servo lane calibration is in progress.
49	RO	constant = 0b0
50:55	ROX	Reserved field.
56	RO	constant = 0b0
57:63	ROX	Reserved field.

Register Name	Receive GLBSM STAT10 E Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.GLBSM.REGS.RX_GLBSM_STAT10_E_PG
Address	800B60200601143F (SCOM)
Description	This register indicates the state of servo lane calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_SERVO_RECAL_IP: This bit indicates that receive servo lane calibration is in progress.
49	RO	constant = 0b0
50:55	ROX	Reserved field.
56	RO	constant = 0b0
57:63	ROX	Reserved field.

Register Name	Receive DATASM Spare Mode Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_SPARE_MODE_PG
Address	800B80000601143F (SCOM)
Description	This register contains per-group spare mode latches and is used to put logic into clock off mode.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PG_DATASM_SPARE_MODE_0: Per-group spare mode latch.
49	RWX	RX_PG_DATASM_SPARE_MODE_1: Per-group spare mode latch.

Bits	SCOM	Field Mnemonic: Description
50	RWX	RX_PG_DATASM_SPARE_MODE_2: Per-group spare mode latch.
51	RWX	RX_PG_DATASM_SPARE_MODE_3: Per-group spare mode latch.
52	RWX	RX_PG_DATASM_SPARE_MODE_4: Per-group spare mode latch.
53	RWX	RX_PG_DATASM_SPARE_MODE_5: Per-group spare mode latch.
54	RWX	RX_PG_DATASM_SPARE_MODE_6: Per-group spare mode latch.
55	RWX	RX_PG_DATASM_SPARE_MODE_7: Per-group spare mode latch.
56:59	RWX	RX_SERVO_CONFIG: Per-group servo configuration bits.
60	RWX	RX_CTL_DATASM_CLKDIST_PDWN: This bit is used to put additional rx_ctl_datasm_mac logic into clock off mode.
61:63	RO	constant = 0b000

Register Name	Receive DATASM Spare Mode Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.DATASM.DATASM_REGS.RX_DATASM_SPARE_MODE_PG
Address	800B80200601143F (SCOM)
Description	This register contains per-group spare mode latches and is used to put logic into clock off mode.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PG_DATASM_SPARE_MODE_0: Per-group spare mode latch.
49	RWX	RX_PG_DATASM_SPARE_MODE_1: Per-group spare mode latch.
50	RWX	RX_PG_DATASM_SPARE_MODE_2: Per-group spare mode latch.
51	RWX	RX_PG_DATASM_SPARE_MODE_3: Per-group spare mode latch.
52	RWX	RX_PG_DATASM_SPARE_MODE_4: Per-group spare mode latch.
53	RWX	RX_PG_DATASM_SPARE_MODE_5: Per-group spare mode latch.
54	RWX	RX_PG_DATASM_SPARE_MODE_6: Per-group spare mode latch.
55	RWX	RX_PG_DATASM_SPARE_MODE_7: Per-group spare mode latch.
56:59	RWX	RX_SERVO_CONFIG: Per-group servo configuration bits.
60	RWX	RX_CTL_DATASM_CLKDIST_PDWN: This bit is used to put additional rx_ctl_datasm_mac logic into clock off mode.
61:63	RO	constant = 0b000

Register Name	Receive DATASM CNTLX1 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_CNTLX1_EO_PG
Address	800B88000601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant = 0b0000000000000000000000000000000000000000000000000
49	NCX	Reserved field.
50	NCX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56:63	RO	constant = 0b00000000

Register Name	Receive DATASM CNTLX1 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.DATASM.DATASM_REGS.RX_DATASM_CNTLX1_EO_PG
Address	800B88200601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant = 0b0000000000000000000000000000000000000000000000000
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55	NCX	Reserved field.
56:63	RO	constant = 0b00000000

Register Name	Receive DATASM STAT1 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT1_EO_PG
Address	800B90000601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:58	ROX	Reserved field.
59	ROX	Reserved field.
60	ROX	Reserved field.
61	ROX	Reserved field.
62	ROX	Reserved field.
63	RO	constant = 0b0

Register Name	Receive DATASM STAT1 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT1_EO_PG
Address	800B90200601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:58	ROX	Reserved field.
59	ROX	Reserved field.
60	ROX	Reserved field.
61	ROX	Reserved field.
62	ROX	Reserved field.
63	RO	constant = 0b0

Register Name	Receive DATASM STAT2 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT2_EO_PG
Address	800B98000601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	ROX	Reserved field.

Register Name	Receive DATASM STAT2 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT2_EO_PG
Address	800B98200601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	ROX	Reserved field.

Register Name	Receive DATASM STAT3 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT3_EO_PG
Address	800BA0000601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	ROX	Reserved field.

Register Name	Receive DATASM STAT3 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT3_EO_PG
Address	800BA0200601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	ROX	Reserved field.

Register Name	Receive DATASM STAT4 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT4_EO_PG
Address	800BA8000601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	ROX	Reserved field.

Register Name	Receive DATASM STAT4 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT4_EO_PG
Address	800BA8200601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	ROX	Reserved field.

Register Name	Receive DATASM STAT5 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT5_EO_PG
Address	800BB0000601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	ROX	Reserved field.

Register Name	Receive DATASM STAT5 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT5_EO_PG
Address	800BB0200601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	ROX	Reserved field.

Register Name	Receive DATASM STAT6 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT6_EO_PG
Address	800BB8000601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	ROX	Reserved field.

Register Name	Receive DATASM STAT6 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT6_EO_PG
Address	800BB8200601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	ROX	Reserved field.

Register Name	Receive DATASM STAT7 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT7_EO_PG
Address	800BC0000601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	ROX	Reserved field.
52	ROX	Reserved field.
53	ROX	Reserved field.
54	ROX	Reserved field.
55:62	RO	constant = 0b00000000
63	ROX	Reserved field.

Register Name	Receive DATASM STAT7 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT7_EO_PG
Address	800BC0200601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	ROX	Reserved field.
52	ROX	Reserved field.
53	ROX	Reserved field.
54	ROX	Reserved field.
55:62	RO	constant = 0b00000000
63	ROX	Reserved field.

Register Name	Receive DATASM STAT8 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT8_EO_PG
Address	800BC8000601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	ROX	Reserved field.

Register Name	Receive DATASM STAT8 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT8_EO_PG
Address	800BC8200601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	ROX	Reserved field.

Register Name	Receive DATASM STAT9 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT9_EO_PG
Address	800BD0000601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:56	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
57:63	RO	constant = 0b0000000

Register Name	Receive DATASM STAT9 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT9_EO_PG
Address	800BD0200601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	Receive DATASM STAT10 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT10_EO_PG
Address	800BD8000601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56:63	ROX	Reserved field.

Register Name	Receive DATASM STAT10 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT10_EO_PG
Address	800BD8200601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56:63	ROX	Reserved field.

Register Name	Receive DATASM STAT11 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT11_EO_PG
Address	800BE0000601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	ROX	Reserved field.

Register Name	Receive DATASM STAT11 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT11_EO_PG
Address	800BE0200601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	ROX	Reserved field.

Register Name	Receive DATASM CNTL1 E Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_CNTL1_E_PG
Address	800BE8000601143F (SCOM)
Description	Register

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PG_PRBS_SCRAMBLE_MODE: This bit selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by RX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
50	RWX	RX_PG_PRBS_SEED_MODE: Set this bit to enable seeding of the descramble PRBS block from the incoming data stream.
51	RWX	RX_DESKEW_RATE: Transmit deskew rate. This bit selects between a div1 (1100) and div2 (11110000) deskew pattern rate for both pattern A and B. 0b0 = Divided deskew pattern for POWER9. 0b1 = Regular deskew pattern for POWER8 memory buffer.
52	RWX	RX_RUN_DYN_RECAL_TIMER: This bit enables checking for the 12/24 UI scramble synchronization pulse that enables the SLS status reporting timer. This bit must remain set to 1 to run the dynamic recalibration interval timer until a new full initialization is attempted. 0b0 = Disable checking (forces run_dyn_recal_timer to 0). 0b1 = Enable checking (run_dyn_recal_timer might go to 1 and stay that way after identifying the synchronization pulse).
53:54	RWX	RX_DESKEW_PATTCHK_TIMEOUT_SEL: This generic timer control is used to set the duration of the deskew pattern checking search. It allows multiple pattern periods (pattern length of 128 UI) to be included to increase confidence in an error-free deskew alignment.
55:62	RWX	RX_PG_PRBS_SLS_EXPECT: When an SLS message is expected on the incoming data stream, but it must be masked to complete PRBS seeding, write the expected value here. It is reverted, and the pure PRBS pattern enters the PRBS block.
63	RWX	RX_HALF_RATE_MODE_DATASM: When set to 1, this bit enables timers on the slow clock domain to consistently count UI when in 4-bit legacy mode. Otherwise, the slow clock domain counts only half of the UI when in 4-bit legacy mode.

Register Name	Receive DATASM CNTL1 E Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.DATASM.DATASM_REGS.RX_DATASM_CNTL1_E_PG
Address	800BE8200601143F (SCOM)
Description	Register

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PG_PRBS_SCRAMBLE_MODE: This bit selects the PRBS scramble sequence length. 0b00 = PRBS 23 (default). 0b01 = PRBS 7 (used by RX BIST). 0b10 = PRBS 11. 0b11 = PRBS 15.
50	RWX	RX_PG_PRBS_SEED_MODE: Set this bit to enable seeding of the descramble PRBS block from the incoming data stream.
51	RWX	RX_DESKEW_RATE: Transmit deskew rate. This bit selects between a div1 (1100) and div2 (11110000) deskew pattern rate for both pattern A and B. 0b0 = Divided deskew pattern for POWER9. 0b1 = Regular deskew pattern for POWER8 memory buffer.
52	RWX	RX_RUN_DYN_RECAL_TIMER: This bit enables checking for the 12/24 UI scramble synchronization pulse that enables the SLS status reporting timer. This bit must remain set to 1 to run the dynamic recalibration interval timer until a new full initialization is attempted. 0b0 = Disable checking (forces run_dyn_recal_timer to 0). 0b1 = Enable checking (run_dyn_recal_timer might go to 1 and stay that way after identifying the synchronization pulse)..
53:54	RWX	RX_DESKEW_PATTCHK_TIMEOUT_SEL: This generic timer control is used to set the duration of the deskew pattern checking search. It allows multiple pattern periods (pattern length of 128 UI) to be included to increase confidence in an error-free deskew alignment.
55:62	RWX	RX_PG_PRBS_SLS_EXPECT: When an SLS message is expected on the incoming data stream, but it must be masked to complete PRBS seeding, write the expected value here. It is reverted, and the pure PRBS pattern enters the PRBS block.
63	RWX	RX_HALF_RATE_MODE_DATASM: When set to 1, this bit enables timers on the slow clock domain to consistently count UI when in 4-bit legacy mode. Otherwise, the slow clock domain counts only half of the UI when in 4-bit legacy mode.

Register Name	Receive DATASM STAT12 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT12_EO_PG
Address	800BF0000601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	ROX	Reserved field.

Register Name	Receive DATASM STAT12 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT12_EO_PG
Address	800BF0200601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	ROX	Reserved field.

Register Name	Receive DATASM STAT13 EO Per-Group Register
Mnemonic	IOF2.RX.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT13_E_PG
Address	800BF8000601143F (SCOM)
Description	This register disables clearing the bad bus lane error counter.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_BUS_LANE_ERR_CNTR_DIS_CLR: This bit disables clearing of the bad bus lane error counter (also known as counter1) when the next CRC/ECC error comes in on a new lane.
49:55	ROX	Reserved field.
56	RO	constant = 0b0
57:63	ROX	Reserved field.

Register Name	Receive DATASM STAT13 EO Per-Group Register
Mnemonic	IOF2.RX.RX1.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT13_E_PG
Address	800BF8200601143F (SCOM)
Description	This register disables clearing the bad bus lane error counter.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_BUS_LANE_ERR_CNTR_DIS_CLR: This bit disables clearing of the bad bus lane error counter (also known as counter1) when the next CRC/ECC error comes in on a new lane.
49:55	ROX	Reserved field.
56	RO	constant = 0b0
57:63	ROX	Reserved field.

Register Name	Transmit Spare Mode Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX0.TXCTL.CTL_REGS.TX_CTL_REGS.TX_SPARE_MODE_PG
Address	800C04000601143F (SCOM)
Description	This register contains per-group spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PG_SPARE_MODE_0: Per-group spare mode latch.
49	RWX	TX_PG_SPARE_MODE_1: Per-group spare mode latch.
50	RWX	TX_PG_SPARE_MODE_2: Per-group spare mode latch.
51	RWX	TX_PG_SPARE_MODE_3: Per-group spare mode latch.
52	RWX	TX_PG_SPARE_MODE_4: Per-group spare mode latch.
53	RWX	TX_PG_SPARE_MODE_5: Per-group spare mode latch.
54	RWX	TX_PG_SPARE_MODE_6: Per-group spare mode latch.
55	RWX	TX_PG_SPARE_MODE_7: Per-group spare mode latch.

Bits	SCOM	Field Mnemonic: Description
56:57	RWX	TX_PG_SPARE_MODE_8_9: Per-group spare mode latch.
58:63	RO	constant = 0b000000

Register Name	Transmit Spare Mode Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX1.TXCTL.CTL_REGS.TX_CTL_REGS.TX_SPARE_MODE_PG
Address	800C04200601143F (SCOM)
Description	This register contains per-group spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PG_SPARE_MODE_0: Per-group spare mode latch.
49	RWX	TX_PG_SPARE_MODE_1: Per-group spare mode latch.
50	RWX	TX_PG_SPARE_MODE_2: Per-group spare mode latch.
51	RWX	TX_PG_SPARE_MODE_3: Per-group spare mode latch.
52	RWX	TX_PG_SPARE_MODE_4: Per-group spare mode latch.
53	RWX	TX_PG_SPARE_MODE_5: Per-group spare mode latch.
54	RWX	TX_PG_SPARE_MODE_6: Per-group spare mode latch.
55	RWX	TX_PG_SPARE_MODE_7: Per-group spare mode latch.
56:57	RWX	TX_PG_SPARE_MODE_8_9: Per-group spare mode latch.
58:63	RO	constant = 0b000000

Register Name	Transmit ID1 Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX0.TXCTL.CTL_REGS.TX_CTL_REGS.TX_ID1_PG
Address	800C0C000601143F (SCOM)
Description	This register is used to programmatically set the bus number that a group belongs to.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	TX_BUS_ID: This field is used to programmatically set the bus number that a group belongs to.
54:63	RO	constant = 0b0000000000

Register Name	Transmit ID1 Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX1.TXCTL.CTL_REGS.TX_CTL_REGS.TX_ID1_PG
Address	800C0C200601143F (SCOM)
Description	This register is used to programmatically set the bus number that a group belongs to.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	TX_BUS_ID: This field is used to programmatically set the bus number that a group belongs to.

Bits	SCOM	Field Mnemonic: Description
54:63	RO	constant = 0b0000000000

Register Name	Transmit CTL Mode 1 EO Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX0.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_MODE1_EO_PG
Address	800C14000601143F (SCOM)
Description	This register contains transmit control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_CLKDIST_PDWN: This field is used to disable the transmit group clocks and put them into a low-power state. It does not control per-lane circuits or logic
49:50	RO	constant = 0b00
51	RW	TX_BIST_EN: This bit enables the transmit BIST state machine to begin testing.
52	RW	TX_EXBIST_MODE: This bit is used to disable the BIST enable through external I/O.
53:57	RWX	TX_MAX_BAD_LANES: Static repair, dynamic repair, and recalibration maximum number of bad lanes per transmit bus. **Note:** This field must match the receive side.
58	RWX	TX_MSBSWAP: This bit is used to enable an end-for-end or MSb swap of transmit lanes. For example, lanes 0 and N-1 swap, lanes 1 and N-2 swap, and so on. 0b0 = No swap (default). 0b1 = End-for-end swap mode.
59	RWX	TX_PDWN_LITE_DISABLE: This bit disables the power-down lite feature of unused spare lanes. (In general, it must match rx_pdwn_lite_disable.)
60:61	RWX	TX_WT_PATTERN_LENGTH: Transmit wire-test pattern length. This field specifies the length of N in the 3N-up/1N-down wire-test pattern. 0b00 = 128 (default). 0b01 = 256. 0b10 = 512. 0b11 = 1024.
62	RWX	TX_DESKEW_RATE: Transmit deskew rate. This bit selects between a div1 (1100) and div2 (11110000) deskew pattern rate for both pattern A and B. 0b0 = Divided deskew pattern for POWER9. 0b1 = Regular deskew pattern for POWER8 memory buffer.
63	RO	constant = 0b0

Register Name	Transmit CTL Mode 1 EO Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX1.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_MODE1_EO_PG
Address	800C14200601143F (SCOM)
Description	This register contains transmit control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_CLKDIST_PDWN: This field is used to disable the transmit group clocks and put them into a low-power state. It does not control per-lane circuits or logic
49:50	RO	constant = 0b00

Bits	SCOM	Field Mnemonic: Description
51	RW	TX_BIST_EN: This bit enables the transmit BIST state machine to begin testing.
52	RW	TX_EXBIST_MODE: This bit is used to disable the BIST enable through external I/O.
53:57	RWX	TX_MAX_BAD_LANES: Static repair, dynamic repair, and recalibration maximum number of bad lanes per transmit bus. **Note:** This field must match the receive side.
58	RWX	TX_MSBSWAP: This bit is used to enable an end-for-end or MSb swap of transmit lanes. For example, lanes 0 and N-1 swap, lanes 1 and N-2 swap, and so on. 0b0 = No swap (default). 0b1 = End-for-end swap mode.
59	RWX	TX_PDWN_LITE_DISABLE: This bit disables the power-down lite feature of unused spare lanes. (In general, it must match rx_pdwn_lite_disable.)
60:61	RWX	TX_WT_PATTERN_LENGTH: Transmit wire-test pattern length. This field specifies the length of N in the 3N-up/1N-down wire-test pattern. 0b00 = 128 (default). 0b01 = 256. 0b10 = 512. 0b11 = 1024.
62	RWX	TX_DESKEW_RATE: Transmit deskew rate. This bit selects between a div1 (1100) and div2 (11110000) deskew pattern rate for both pattern A and B. 0b0 = Divided deskew pattern for POWER9. 0b1 = Regular deskew pattern for POWER8 memory buffer.
63	RO	constant = 0b0

Register Name	**Transmit CTL Mode 2 EO Per-Group Register**
Mnemonic	IOF2.TX_WRAP.TX0.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_MODE2_EO_PG
Address	800C1C000601143F (SCOM)
Description	This register contains transmit control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	TX_SLS_SCRAMBLE_MODE: This field selects SLS PRBS scramble mode for the ninth pattern. 0b00 = Use PRBS23. 0b01 = Use PRBS7. 0b10 = Use PRBS11. 0b11 = Use PRBS15.
50	RWX	TX_CLK_UNLOAD_CLK_DISABLE: This bit is set to 0 to clock off the synchronization logic on the clock slice and save power. It should not be necessary to use the synchronization logic on the clock slice because it has no FIFO, but control is available just in case.
51	RWX	TX_CLK_RUN_COUNT: Set this bit to 1 to enable the transmit clock slice serializer. This bit should be enabled at all times, but control is available as a precaution.
52:54	RWX	TX_CLK_UNLOAD_SEL: This field controls the preset value of the transmit clock slice unload counter. It should not be necessary to use this on the clock slice, but it is available as a precaution.
55	RWX	TX_CLK_HALF_WIDTH_MODE: This bit controls the 4-to-1 pin on the transmit clock slice. This bit should remain 0, but the control is provided as a precaution.
56:62	RWX	TX_BUS_WIDTH: This field provides the transmit bus width.
63	RO	constant = 0b0

Register Name	Transmit CTL Mode 2 EO Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX1.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_MODE2_EO_PG
Address	800C1C200601143F (SCOM)
Description	This register contains transmit control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	TX_SLS_SCRAMBLE_MODE: This field selects SLS PRBS scramble mode for the ninth pattern. 0b00 = Use PRBS23. 0b01 = Use PRBS7. 0b10 = Use PRBS11. 0b11 = Use PRBS15.
50	RWX	TX_CLK_UNLOAD_CLK_DISABLE: This bit is set to 0 to clock off the synchronization logic on the clock slice and save power. It should not be necessary to use the synchronization logic on the clock slice because it has no FIFO, but control is available just in case.
51	RWX	TX_CLK_RUN_COUNT: Set this bit to 1 to enable the transmit clock slice serializer. This bit should be enabled at all times, but control is available as a precaution.
52:54	RWX	TX_CLK_UNLOAD_SEL: This field controls the preset value of the transmit clock slice unload counter. It should not be necessary to use this on the clock slice, but it is available as a precaution.
55	RWX	TX_CLK_HALF_WIDTH_MODE: This bit controls the 4-to-1 pin on the transmit clock slice. This bit should remain 0, but the control is provided as a precaution.
56:62	RWX	TX_BUS_WIDTH: This field provides the transmit bus width.
63	RO	constant = 0b0

Register Name	Transmit CTL CNTLG1 EO Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX0.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_CNTLG1_EO_PG
Address	800C24000601143F (SCOM)
Description	This register contains the transmit drive patterns.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	TX_DRV_CLK_PATTERN_GCRMSG: Transmit clock drive patterns. 0b00 = Drive all 0s pattern. 0b01 = Drive wire-test pattern. 0b10 = Drive clock pattern. 0b11 = Unused.

Bits	SCOM	Field Mnemonic: Description
50:53	RWX	TX_DRV_DATA_PATTERN_GCRMSG: Transmit drive patterns. 0b0000 = Drive all 0s pattern. 0b0001 = Drive wire-test pattern. 0b0010 = Drive all 1s pattern. 0b0011 = Drive deskew pattern A. 0b0100 = Drive deskew pattern B. 0b0101 = PRBS full-speed scramble pattern (see tx_prbs_tap_id). 0b0110 = Alternate PRBS7 pattern for RX BIST. 0b0111 = PRBS calibration or 9th pattern. 0b1000 = PRBS7 pattern. 0b1001 = PRBS11 pattern. 0b1010 = Drives TDR pulse-square waves. 0b1011 = PRBS15 pattern. 0b1100 = Alternate PRBS23 for NVBUS. 0b1101 = PRBS31 pattern. 0b1110 = 1-to-1 clock pattern. 0b1111 = Unused.
54:63	RO	constant = 0b0000000000

Register Name	Transmit CTL CNTLG1 EO Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX1.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_CNTLG1_EO_PG
Address	800C24200601143F (SCOM)
Description	This register contains the transmit drive patterns.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	TX_DRV_CLK_PATTERN_GCRMSG: Transmit clock drive patterns. 0b00 = Drive all 0s pattern. 0b01 = Drive wire-test pattern. 0b10 = Drive clock pattern. 0b11 = Unused.
50:53	RWX	TX_DRV_DATA_PATTERN_GCRMSG: Transmit drive patterns. 0b0000 = Drive all 0s pattern. 0b0001 = Drive wire-test pattern. 0b0010 = Drive all 1s pattern. 0b0011 = Drive deskew pattern A. 0b0100 = Drive deskew pattern B. 0b0101 = PRBS full-speed scramble pattern (see tx_prbs_tap_id). 0b0110 = Alternate PRBS7 pattern for RX BIST. 0b0111 = PRBS calibration or 9th pattern. 0b1000 = PRBS7 pattern. 0b1001 = PRBS11 pattern. 0b1010 = Drives TDR pulse-square waves. 0b1011 = PRBS15 pattern. 0b1100 = Alternate PRBS23 for NVBUS. 0b1101 = PRBS31 pattern. 0b1110 = 1-to-1 clock pattern. 0b1111 = Unused.
54:63	RO	constant = 0b0000000000

Register Name	Transmit CTL CNTL2 EO Per-Group Register	
Mnemonic	IOF2.TX_WRAP.TX0.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_CNTL2_EO_PG	
Address	800C2C000601143F (SCOM)	
Description	This register contains per-group transmit control fields.	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	TX_ERR_INJ_A_FINE_SEL: This field contains the random LSB/fine-grained cycle offset variation control for pattern A, where cycles are deserialized domain cycles. 0b000 = Random offset in the range of 1 - 32 cycles(default). 0b001 = Random offset in the range of 1 - 16 cycles. 0b010 = Random offset in the range of 1 - 8 cycles. 0b011 = Random offset in the range of 1 - 4 cycles. 0b100 = Random offset in the range of 1 - 2 cycles. 0b101 = Fixed offset of 1 cycle. 0b110 = Fixed offset of 3 cycles. 0b111 = Fixed offset of 7 cycles.
51:54	RWX	TX_ERR_INJ_A_COARSE_SEL: This field contains the random MSB/coarse-grained multiplier for the base error rate counter, which controls bit-error-rate variation for pattern A. There are also a number of nonrandom settings that are specifically chosen to avoid powers of two.
55:60	RWX	TX_ERR_INJ_A_BER_SEL: This field is used to set the random bit-error injection rate for pattern A. When set to a binary value of N, the average bit error rate is 1/(2^N x beats x mean(MSB)).
61	RWX	TX_ERR_INJ_ENABLE: This bit is the overall error injection enable. When set to 0, all other injection is gated.
62	RWX	TX_ERR_INJ_CLOCK_ENABLE: This bit enables clocks to larger counter and PRBS logic. Use this to stagger start times and effectively seed the injection mechanism randomly.
63	RO	constant = 0b0

Register Name	Transmit CTL CNTL2 EO Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX1.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_CNTL2_EO_PG
Address	800C2C200601143F (SCOM)
Description	This register contains per-group transmit control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	TX_ERR_INJ_A_FINE_SEL: This field contains the random LSB/fine-grained cycle offset variation control for pattern A, where cycles are deserialized domain cycles. 0b000 = Random offset in the range of 1 - 32 cycles(default). 0b001 = Random offset in the range of 1 - 16 cycles. 0b010 = Random offset in the range of 1 - 8 cycles. 0b011 = Random offset in the range of 1 - 4 cycles. 0b100 = Random offset in the range of 1 - 2 cycles. 0b101 = Fixed offset of 1 cycle. 0b110 = Fixed offset of 3 cycles. 0b111 = Fixed offset of 7 cycles.
51:54	RWX	TX_ERR_INJ_A_COARSE_SEL: This field contains the random MSB/coarse-grained multiplier for the base error rate counter, which controls bit-error-rate variation for pattern A. There are also a number of nonrandom settings that are specifically chosen to avoid powers of two.
55:60	RWX	TX_ERR_INJ_A_BER_SEL: This field is used to set the random bit-error injection rate for pattern A. When set to a binary value of N, the average bit error rate is 1/(2^N x beats x mean(MSB)).

Bits	SCOM	Field Mnemonic: Description
61	RWX	TX_ERR_INJ_ENABLE: This bit is the overall error injection enable. When set to 0, all other injection is gated.
62	RWX	TX_ERR_INJ_CLOCK_ENABLE: This bit enables clocks to larger counter and PRBS logic. Use this to stagger start times and effectively seed the injection mechanism randomly.
63	RO	constant = 0b0

Register Name	Transmit CTL CNTL3 EO Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX0.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_CNTL3_EO_PG
Address	800C34000601143F (SCOM)
Description	This register contains per-group transmit control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	TX_ERR_INJ_B_FINE_SEL: This field contains the random LSB/fine-grained cycle offset variation control for pattern B, where cycles are deserialized domain cycles. 0b000 = Random offset in range of 1 - 32 cycles(default). 0b001 = Random offset in range of 1 - 16 cycles. 0b010 = Random offset in range of 1 - 8 cycles. 0b011 = Random offset in range of 1 - 4 cycles. 0b100 = Random offset in range of 1 - 2 cycles. 0b101 = Fixed offset of 1 cycle. 0b110 = Fixed offset of 3 cycles. 0b111 = Fixed offset of 7 cycles.
51:54	RWX	TX_ERR_INJ_B_COARSE_SEL: This field contains the random MSB/coarse-grained multiplier for the base error-rate counter, which controls the bit-error-rate variation for pattern B. There are also a number of nonrandom settings that are specifically chosen to avoid powers of two.
55:60	RWX	TX_ERR_INJ_B_BER_SEL: This field is used to set the random bit-error injection rate for pattern B. When set to a binary value of N, the average bit error rate is 1/(2^N x beats x mean(MSB)).
61:63	RO	constant = 0b000

Register Name	Transmit CTL CNTL3 EO Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX1.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_CNTL3_EO_PG
Address	800C34200601143F (SCOM)
Description	This register contains per-group transmit control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	TX_ERR_INJ_B_FINE_SEL: This field contains the random LSB/fine-grained cycle offset variation control for pattern B, where cycles are deserialized domain cycles. 0b000 = Random offset in range of 1 - 32 cycles(default). 0b001 = Random offset in range of 1 - 16 cycles. 0b010 = Random offset in range of 1 - 8 cycles. 0b011 = Random offset in range of 1 - 4 cycles. 0b100 = Random offset in range of 1 - 2 cycles. 0b101 = Fixed offset of 1 cycle. 0b110 = Fixed offset of 3 cycles. 0b111 = Fixed offset of 7 cycles.

Bits	SCOM	Field Mnemonic: Description
51:54	RWX	TX_ERR_INJ_B_COARSE_SEL: This field contains the random MSB/coarse-grained multiplier for the base error-rate counter, which controls the bit-error-rate variation for pattern B. There are also a number of nonrandom settings that are specifically chosen to avoid powers of two.
55:60	RWX	TX_ERR_INJ_B_BER_SEL: This field is used to set the random bit-error injection rate for pattern B. When set to a binary value of N, the average bit error rate is 1/(2^N x beats x mean(MSB)).
61:63	RO	constant = 0b000

Register Name	Transmit ID2 Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX0.TXCTL.CTL_REGS.TX_CTL_REGS.TX_ID2_PG
Address	800C84000601143F (SCOM)
Description	This register is used to set the first and last lane positions in the group relative to the bus.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant = 0b0000000000000000000000000000000000000000000000000
49:55	RWX	TX_START_LANE_ID: This field is used to programmatically set the first lane position in the group relative to the bus.
56	RO	constant = 0b0
57:63	RWX	TX_END_LANE_ID: This field is used to programmatically set the last lane position in the group relative to the bus.

Register Name	Transmit ID2 Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX1.TXCTL.CTL_REGS.TX_CTL_REGS.TX_ID2_PG
Address	800C84200601143F (SCOM)
Description	This register is used to set the first and last lane positions in the group relative to the bus.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant = 0b0000000000000000000000000000000000000000000000000
49:55	RWX	TX_START_LANE_ID: This field is used to programmatically set the first lane position in the group relative to the bus.
56	RO	constant = 0b0
57:63	RWX	TX_END_LANE_ID: This field is used to programmatically set the last lane position in the group relative to the bus.

Register Name	Transmit CTL Mode 1 E Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX0.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_MODE1_E_PG
Address	800C8C000601143F (SCOM)
Description	This register contains the first set of transmit mode E controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	TX_CLK_INVERT: This bit is used to invert the polarity of the clock. 0b0 = Normal clock polarity (default). 0b1 = Invert the clock.
49:50	RWX	TX_CLK_QUIESCE: This bit is used to force the output of the clock lane to a particular value. 0b00 = Functional data (default). 0b01 = Quiesce the clock lane to a static 0 value. 0b10 = Quiesce the clock lane to a static 1 value. 0b11 = Tri-state the clock lane output.
51:52	RO	constant = 0b00
53:54	RWX	TX_CLK_RATE: This bit is used to select the transmit bus clock rate. 0b00 = ODR/C8 mode. 0b01 = QDR/C4 mode. 0b10 = DDR/C2 mode. 0b11 = Unused.
55:57	RWX	TX_DYN_RECAL_INTERVAL_TIMEOUT_SEL: TX Dynamic recalibration interval timeout selects. This timeout determines the time between status reporting timeouts. The actual time of sending a message is selected with rx_dyn_recal_status_rpt_timeout_sel. 0B000 = 1024 UI or 106.5 ns. This very small value is for simulation only. 0b001 = 64k UI or 3.4 µs. 0b010 = 32k UI or 3.4 µs. 0b011 = 64k UI or 6.8 µs. 0b100 = 128k UI or 13.6 µs. 0b101 = 256k UI or 27.3 µs. 0b110 = 8192k UI or 872.4 µs. 0b111 = Infinite.
58:59	RWX	TX_DYN_RECAL_STATUS_RPT_TIMEOUT_SEL: Transmit dynamic recalibration status reporting timeout selects. This timeout determines the time that a status reporting timeout lasts. The first 1/4 is a blank period, the middle 1/2 is the command message, and the last 1/4 is another blank period. The time between messages is selected with rx_dyn_recal_interval_timeout_sel. **Note:** The first 1/4 and last 1/4 of this time are actually sending the PRBS pattern, so the actual time that the SLS command is on the lane is 1/2 of this value. 0B00 = 512 UI or 53.2 ns. 0B01 = 1024 UI or 106.5 ns. 0B10 = 2048 UI or 212.9 ns. 0B11 = 4096 UI or 426.0 ns.
60:63	RO	constant = 0b0000

Register Name	**Transmit CTL Mode 1 E Per-Group Register**
Mnemonic	IOF2.TX_WRAP.TX1.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_MODE1_E_PG
Address	800C8C200601143F (SCOM)
Description	This register contains the first set of transmit mode E controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_CLK_INVERT: This bit is used to invert the polarity of the clock. 0b0 = Normal clock polarity (default). 0b1 = Invert the clock.
49:50	RWX	TX_CLK_QUIESCE: This bit is used to force the output of the clock lane to a particular value. 0b00 = Functional data (default). 0b01 = Quiesce the clock lane to a static 0 value. 0b10 = Quiesce the clock lane to a static 1 value. 0b11 = Tri-state the clock lane output.

Bits	SCOM	Field Mnemonic: Description
51:52	RO	constant = 0b00
53:54	RWX	TX_CLK_RATE: This bit is used to select the transmit bus clock rate. 0b00 = ODR/C8 mode. 0b01 = QDR/C4 mode. 0b10 = DDR/C2 mode. 0b11 = Unused.
55:57	RWX	TX_DYN_RECAL_INTERVAL_TIMEOUT_SEL: TX Dynamic recalibration interval timeout selects. This timeout determines the time between status reporting timeouts. The actual time of sending a message is selected with rx_dyn_recal_status_rpt_timeout_sel. 0B000 = 1024 UI or 106.5 ns. This very small value is for simulation only. 0b001 = 64k UI or 3.4 µs. 0b010 = 32k UI or 3.4 µs. 0b011 = 64k UI or 6.8 µs. 0b100 = 128k UI or 13.6 µs. 0b101 = 256k UI or 27.3 µs. 0b110 = 8192k UI or 872.4 µs. 0b111 = Infinite.
58:59	RWX	TX_DYN_RECAL_STATUS_RPT_TIMEOUT_SEL: Transmit dynamic recalibration status reporting timeout selects. This timeout determines the time that a status reporting timeout lasts. The first 1/4 is a blank period, the middle 1/2 is the command message, and the last 1/4 is another blank period. The time between messages is selected with rx_dyn_recal_interval_timeout_sel. **Note:** The first 1/4 and last 1/4 of this time are actually sending the PRBS pattern, so the actual time that the SLS command is on the lane is 1/2 of this value. 0B00 = 512 UI or 53.2 ns. 0B01 = 1024 UI or 106.5 ns. 0B10 = 2048 UI or 212.9 ns. 0B11 = 4096 UI or 426.0 ns.
60:63	RO	constant = 0b0000

Register Name	Transmit CTL Mode 2 E Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX0.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_CNTL2_E_PG
Address	800C9C000601143F (SCOM)
Description	This register contains the second set of transmit mode E controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_IORESET: This bit resets the given transmit clock group and GCR slave.
49:50	RO	constant = 0b00
51	RWX	TX_ERR_INJ_SLS_MODE: This bit is used to set the random bit error injection for pattern A to work during SLS transmission only.
52	RWX	TX_ERR_INJ_SLS_ALL_CMD: This bit is used to qualify the SLS mode error injection for pattern A, to inject on all SLS command transmissions.
53	RWX	TX_ERR_INJ_SLS_RECAL: This bit is used to qualify the SLS mode error injection for pattern A, to inject on the calibration lane only when not sending an SLS command.
54:59	RWX	TX_ERR_INJ_SLS_CMD: This field is used to qualify the SLS mode error injection for pattern A, to inject on only this SLS command transmission.
60:63	RO	constant = 0b0000

Register Name	Transmit CTL Mode 2 E Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX1.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_CNTL2_E_PG
Address	800C9C200601143F (SCOM)
Description	This register contains the second set of transmit mode E controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_IORESET: This bit resets the given transmit clock group and GCR slave.
49:50	RO	constant = 0b00
51	RWX	TX_ERR_INJ_SLS_MODE: This bit is used to set the random bit error injection for pattern A to work during SLS transmission only.
52	RWX	TX_ERR_INJ_SLS_ALL_CMD: This bit is used to qualify the SLS mode error injection for pattern A, to inject on all SLS command transmissions.
53	RWX	TX_ERR_INJ_SLS_RECAL: This bit is used to qualify the SLS mode error injection for pattern A, to inject on the calibration lane only when not sending an SLS command. See workbook for details.
54:59	RWX	TX_ERR_INJ_SLS_CMD: This field is used to qualify the SLS mode error injection for pattern A, to inject on only this SLS command transmission.
60:63	RO	constant = 0b0000

Register Name	Transmit CTL CNTLG3 E Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX0.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_CNTLG3_E_PG
Address	800CA4000601143F (SCOM)
Description	This register is used for SLS commands.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_SND_SLS_CMD_GCRMSG: When set, this bit enables sending SLS commands or recalibration data.
49	RWX	TX_DYN_RECAL_TSR_IGNORE_GCRMSG: When set, this bit enables sending dynamic recalibration SLS commands all the time, not just during the status reporting interval.
50:55	RWX	TX_SLS_CMD_GCRMSG: This field contains the transmit SLS command.
56	RWX	TX_SND_SLS_CMD_PREV_GCRMSG: When set, this bit indicates to revert to sending the previous SLS command or recalibration data after the recovery repair is made.
57	RWX	TX_SND_SLS_USING_REG_SCRAMBLE: When set, this bit indicates to send the SLS command using the normal scramble pattern instead of calibration or the ninth pattern.
58:63	RO	constant = 0b000000

Register Name	Transmit CTL CNTLG3 E Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX1.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_CNTLG3_E_PG
Address	800CA4200601143F (SCOM)
Description	This register is used for SLS commands.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	TX_SND_SLS_CMD_GCRMSG: When set, this bit enables sending SLS commands or recalibration data.
49	RWX	TX_DYN_RECAL_TSR_IGNORE_GCRMSG: When set, this bit enables sending dynamic recalibration SLS commands all the time, not just during the status reporting interval.
50:55	RWX	TX_SLS_CMD_GCRMSG: This field contains the transmit SLS command.
56	RWX	TX_SND_SLS_CMD_PREV_GCRMSG: When set, this bit indicates to revert to sending the previous SLS command or recalibration data after the recovery repair is made.
57	RWX	TX_SND_SLS_USING_REG_SCRAMBLE: When set, this bit indicates to send the SLS command using the normal scramble pattern instead of calibration or the ninth pattern.
58:63	RO	constant = 0b000000

Register Name	**Transmit CTL CNTLG4 E Per-Group Register**
Mnemonic	IOF2.TX_WRAP.TX0.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_CNTLG4_E_PG
Address	800CAC000601143F (SCOM)
Description	This register is used for SLS lanes.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	TX_SLS_LANE_GCRMSG: This field contains the encoded SLS lane in relation to the entire transmit bus.
55	RWX	TX_SLS_LANE_VAL_GCRMSG: This bit indicates that the transmit SLS lane is valid.
56	RWX	TX_SLS_LANE_ENC_SPR1_GCRMSG: This bit is used for the transmit SLS lane control spare signal.
57:63	RO	constant = 0b0000000

Register Name	**Transmit CTL CNTLG4 E Per-Group Register**
Mnemonic	IOF2.TX_WRAP.TX1.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_CNTLG4_E_PG
Address	800CAC200601143F (SCOM)
Description	This register is used for SLS lanes.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	TX_SLS_LANE_GCRMSG: This field contains the encoded SLS lane in relation to the entire transmit bus.
55	RWX	TX_SLS_LANE_VAL_GCRMSG: This bit indicates that the transmit SLS lane is valid.
56	RWX	TX_SLS_LANE_ENC_SPR1_GCRMSG: This bit is used for the transmit SLS lane control spare signal.
57:63	RO	constant = 0b0000000

Register Name	**Transmit CTL CNTLG5 E Per-Group Register**
Mnemonic	IOF2.TX_WRAP.TX0.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_CNTLG5_E_PG
Address	800CB4000601143F (SCOM)
Description	This register is used for SLS lane shadowing.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_SLS_LANE_SHDW_GCRMSG: This bit enables SLS lane shadowing or unshadowing functional data. This is used to set up transmit multiplex controls and to enable powering up of the next SLS lane).
49	RWX	TX_SLS_LANE_SHDW_RPR_GCRMSG: This bit enables SLS lane shadowing or unshadowing functional data during a repair action. This is used to set up transmit multiplex controls and to enable powering up of the last good SLS lane.
50	RWX	TX_SLS_LANE_MUX_SPR1_GCRMSG: This bit enables SLS lane shadowing, unshadowing, or multiplexing spare control signal 1, to which the tx_set_sls_ln controller is sensitive.
51	RWX	TX_SLS_LANE_MUX_SPR2_GCRMSG: This bit enables SLS lane shadowing, unshadowing, or multiplexing spare control signal 2, to which the tx_set_sls_ln controller is sensitive.
52:63	RO	constant = 0b000000000000

Register Name	**Transmit CTL CNTLG5 E Per-Group Register**
Mnemonic	IOF2.TX_WRAP.TX1.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_CNTLG5_E_PG
Address	800CB4200601143F (SCOM)
Description	This register is used for SLS lane shadowing.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_SLS_LANE_SHDW_GCRMSG: This bit enables SLS lane shadowing or unshadowing functional data. This is used to set up transmit multiplex controls and to enable powering up of the next SLS lane).
49	RWX	TX_SLS_LANE_SHDW_RPR_GCRMSG: This bit enables SLS lane shadowing or unshadowing functional data during a repair action. This is used to set up transmit multiplex controls and to enable powering up of the last good SLS lane.
50	RWX	TX_SLS_LANE_MUX_SPR1_GCRMSG: This bit enables SLS lane shadowing, unshadowing, or multiplexing spare control signal 1, to which the tx_set_sls_ln controller is sensitive.
51	RWX	TX_SLS_LANE_MUX_SPR2_GCRMSG: This bit enables SLS lane shadowing, unshadowing, or multiplexing spare control signal 2, to which the tx_set_sls_ln controller is sensitive.
52:63	RO	constant = 0b000000000000

Register Name	**Transmit CTL CNTLG6 E Per-Group Register**
Mnemonic	IOF2.TX_WRAP.TX0.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_CNTLG6_E_PG
Address	800CBC000601143F (SCOM)
Description	This register is used for SLS lanes.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_SLV_MV_SLS_SHDW_REQ_GCRMSG: This bit is a request to the transmit slave to move the SLS lane.
49	RWX	TX_SLV_MV_SLS_SHDW_RPR_REQ_GCRMSG: This bit is a request to the transmit slave to move the SLS lane and set the bad lane register.
50	RWX	TX_SLV_MV_SLS_UNSHDW_REQ_GCRMSG: This bit is a request to the transmit slave to move the SLS lane.

Bits	SCOM	Field Mnemonic: Description
51	RWX	TX_SLV_MV_SLS_UNSHDW_RPR_REQ_GCRMSG: This bit is a request to the transmit slave to move the SLS lane and set the bad lane register.
52	RWX	TX_SLV_MV_SLS_SPR1_GCRMSG: This bit is spare request 1 to the transmit slave, to which SLS lane movement is sensitive.
53	RWX	TX_SLV_MV_SLS_SPR2_GCRMSG: This bit is spare request 2 to the transmit slave, to which SLS lane movement is sensitive.
54:58	RO	constant = 0b00000
59	RWX	TX_SLV_MV_SLS_RPR_REQ_GCRMSG: This bit is a request to the transmit slave to move the SLS lane and set the bad lane register.
60	RWX	TX_SLS_LANE_SEL_LG_GCRMSG: This bit sets the tx_sls_lane_sel_gcrmsg for the last good lane per bus during recalibration bad lane scenarios.
61	RWX	TX_SLS_LANE_UNSEL_LG_GCRMSG: This bit clears the tx_sls_lane_sel_gcrmsg for the last good lane per bus during recalibration bad lane scenarios.
62	RWX	TX_SPR_LNS_PDWN_LITE_GCRMSG: This bit signals the transmit side to power down lite (data gate) unused spare lanes at the end of static repair.
63	RWX	TX_SLV_LGL_RPR_REQ_GCRMSG: This bit is a request to the transmit slave to set the bad lane register to the last good lane of the bus (during recalibration bad lane scenarios).

Register Name	Transmit CTL CNTLG6 E Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX1.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_CNTLG6_E_PG
Address	800CBC200601143F (SCOM)
Description	This register is used for SLS lanes.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_SLV_MV_SLS_SHDW_REQ_GCRMSG: This bit is a request to the transmit slave to move the SLS lane.
49	RWX	TX_SLV_MV_SLS_SHDW_RPR_REQ_GCRMSG: This bit is a request to the transmit slave to move the SLS lane and set the bad lane register.
50	RWX	TX_SLV_MV_SLS_UNSHDW_REQ_GCRMSG: This bit is a request to the transmit slave to move the SLS lane.
51	RWX	TX_SLV_MV_SLS_UNSHDW_RPR_REQ_GCRMSG: This bit is a request to the transmit slave to move the SLS lane and set the bad lane register.
52	RWX	TX_SLV_MV_SLS_SPR1_GCRMSG: This bit is spare request 1 to the transmit slave, to which SLS lane movement is sensitive.
53	RWX	TX_SLV_MV_SLS_SPR2_GCRMSG: This bit is spare request 2 to the transmit slave, to which SLS lane movement is sensitive.
54:58	RO	constant = 0b00000
59	RWX	TX_SLV_MV_SLS_RPR_REQ_GCRMSG: This bit is a request to the transmit slave to move the SLS lane and set the bad lane register.
60	RWX	TX_SLS_LANE_SEL_LG_GCRMSG: This bit sets the tx_sls_lane_sel_gcrmsg for the last good lane per bus during recalibration bad lane scenarios.
61	RWX	TX_SLS_LANE_UNSEL_LG_GCRMSG: This bit clears the tx_sls_lane_sel_gcrmsg for the last good lane per bus during recalibration bad lane scenarios.
62	RWX	TX_SPR_LNS_PDWN_LITE_GCRMSG: This bit signals the transmit side to power down lite (data gate) unused spare lanes at the end of static repair.

Bits	SCOM	Field Mnemonic: Description
63	RWX	TX_SLV_LGL_RPR_REQ_GCRMSG: This bit is a request to the transmit slave to set the bad lane register to the last good lane of the bus (during recalibration bad lane scenarios).

Register Name	Transmit CTL CNTLG7 E Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX0.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_CNTLG7_E_PG
Address	800CC4000601143F (SCOM)
Description	This register enables wire-test driver segments.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_WT_EN_ALL_CLK_SEGS_GCRMSG: Transmit clock wire-test driver segments enable.
49	RWX	TX_WT_EN_ALL_DATA_SEGS_GCRMSG: Transmit data wire-test driver segments enable.
50:63	RO	constant = 0b00000000000000

Register Name	Transmit CTL CNTLG7 E Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX1.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_CNTLG7_E_PG
Address	800CC4200601143F (SCOM)
Description	This register enables wire-test driver segments.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_WT_EN_ALL_CLK_SEGS_GCRMSG: Transmit clock wire-test driver segments enable.
49	RWX	TX_WT_EN_ALL_DATA_SEGS_GCRMSG: Transmit data wire-test driver segments enable.
50:63	RO	constant = 0b00000000000000

Register Name	Transmit CTL CNTL8 EO Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX0.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_CNTL8_EO_PG
Address	800CCC000601143F (SCOM)
Description	This register is used to control the TDR function.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	TX_TDR_DAC_CNTL: This field controls the variable threshold receiver for the TDR function.
56	RO	constant = 0b0
57	RWX	TX_TDR_PHASE_SEL: This field controls phase select for the TDR function. 0 = _n leg. 1 = _p leg.
58:63	RO	constant = 0b000000

Register Name	**Transmit CTL CNTL8 EO Per-Group Register**
Mnemonic	IOF2.TX_WRAP.TX1.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_CNTL8_EO_PG
Address	800CCC200601143F (SCOM)
Description	This register is used to control the TDR function.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	TX_TDR_DAC_CNTL: This field controls the variable threshold receiver for the TDR function.
56	RO	constant = 0b0
57	RWX	TX_TDR_PHASE_SEL: This field controls phase select for the TDR function. 0 = _n leg. 1 = _p leg.
58:63	RO	constant = 0b000000

Register Name	**Transmit CTL CNTL9 EO Per-Group Register**
Mnemonic	IOF2.TX_WRAP.TX0.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_CNTL9_EO_PG
Address	800CD4000601143F (SCOM)
Description	This register is used to control the TDR function.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:61	RWX	TX_TDR_PULSE_OFFSET: This field contains the offset value for the TDR pulse.
62:63	RO	constant = 0b00

Register Name	**Transmit CTL CNTL9 EO Per-Group Register**
Mnemonic	IOF2.TX_WRAP.TX1.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_CNTL9_EO_PG
Address	800CD4200601143F (SCOM)
Description	This register is used to control the TDR function.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:61	RWX	TX_TDR_PULSE_OFFSET: This field contains the offset value for the TDR pulse.
62:63	RO	constant = 0b00

Register Name	**Transmit CTL CNTL10 EO Per-Group Register**
Mnemonic	IOF2.TX_WRAP.TX0.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_CNTL10_EO_PG
Address	800CDC000601143F (SCOM)
Description	This register is used to control the TDR function.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:56	RWX	TX_TDR_PULSE_WIDTH: The field controls the width of the TDR pulse.
57:63	RO	constant = 0b0000000

Register Name	Transmit CTL CNTL10 EO Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX1.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_CNTL10_EO_PG
Address	800CDC200601143F (SCOM)
Description	This register is used to control the TDR function.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:56	RWX	TX_TDR_PULSE_WIDTH: The field controls the width of the TDR pulse.
57:63	RO	constant = 0b0000000

Register Name	Transmit CTL STATG1 E Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX0.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_STATG1_E_PG
Address	800CE4000601143F (SCOM)
Description	This register encodes bad lanes.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	TX_BAD_LANE1_GCRMSG: This field contains encoded bad lane one in relation to the entire transmit bus.
55:61	RWX	TX_BAD_LANE2_GCRMSG: This field contains encoded bad lane two in relation to the entire transmit bus.
62:63	RWX	TX_BAD_LANE_CODE_GCRMSG: Transmit bad lane code. 0b00 = Zero bad lanes. 0b01 = Bad lane 1 is valid. 0b10 = Bad lanes 1 and 2 are valid. 0b11 = 3+ bad lanes.

Register Name	Transmit CTL STATG1 E Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX1.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_STATG1_E_PG
Address	800CE4200601143F (SCOM)
Description	This register encodes bad lanes.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	TX_BAD_LANE1_GCRMSG: This field contains encoded bad lane one in relation to the entire transmit bus.
55:61	RWX	TX_BAD_LANE2_GCRMSG: This field contains encoded bad lane two in relation to the entire transmit bus.
62:63	RWX	TX_BAD_LANE_CODE_GCRMSG: Transmit bad lane code. 0b00 = Zero bad lanes. 0b01 = Bad lane 1 is valid. 0b10 = Bad lanes 1 and 2 are valid. 0b11 = 3+ bad lanes.

Register Name	Transmit CRL Mode 2 E Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX0.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_MODE2_E_PG
Address	800CEC000601143F (SCOM)
Description	This register controls which group lanes are ignored by the training logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RWX	TX_LANE_DISABLED_VEC_0_15: This field is used to set which of group lanes 0 - 15 are ignored by the training logic. These settings do not affect power down. **Note:** Disabled lanes must be contiguous.

Register Name	Transmit CRL Mode 2 E Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX1.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_MODE2_E_PG
Address	800CEC200601143F (SCOM)
Description	This register controls which group lanes are ignored by the training logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RWX	TX_LANE_DISABLED_VEC_0_15: This field is used to set which of group lanes 0 - 15 are ignored by the training logic. These settings do not affect power down. **Note:** Disabled lanes must be contiguous.

Register Name	Transmit CRL Mode 3 E Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX0.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_MODE3_E_PG
Address	800CF4000601143F (SCOM)
Description	This register controls which group lanes are ignored by the training logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	TX_LANE_DISABLED_VEC_16_23: This field is used to set which of group lanes 16 - 23 are ignored by the training logic. These do not affect power down. **Note:** Disabled lanes must be contiguous.
56:63	RO	constant = 0b00000000

Register Name	Transmit CRL Mode 3 E Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX1.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_MODE3_E_PG
Address	800CF4200601143F (SCOM)
Description	This register controls which group lanes are ignored by the training logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RWX	TX_LANE_DISABLED_VEC_16_23: This field is used to set which of group lanes 16 - 23 are ignored by the training logic. These do not affect power down. **Note:** Disabled lanes must be contiguous.
56:63	RO	constant = 0b00000000

Register Name	Transmit Group FIR Error Source
Mnemonic	IOF2.TX_WRAP.TX0.TXCTL.TX_CTL_SM.REGS.TX_FIR_PG
Address	800D04000601143F (SCOM)
Description	This is an isolation register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53:62	RO	constant = 0b0000000000
63	ROX	Reserved field.

Register Name	Transmit Group FIR Error Source
Mnemonic	IOF2.TX_WRAP.TX1.TXCTL.TX_CTL_SM.REGS.TX_FIR_PG
Address	800D04200601143F (SCOM)
Description	This is an isolation register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53:62	RO	constant = 0b0000000000
63	ROX	Reserved field.

Register Name	Transmit Group FIR Error Mask Register
Mnemonic	IOF2.TX_WRAP.TX0.TXCTL.TX_CTL_SM.REGS.TX_FIR_MASK_PG
Address	800D0C000601143F (SCOM)
Description	This register masks transmit FIR per-group errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	TX_Per Group_FIR_ERRS_MASK: This field contains the FIR mask for register or state-machine parity checkers in the per-group TXCTL logic. A value of 1 masks the error from generating a FIR error. Bit 0 = par_err_mask_txctl_regs. Bit 1 = par_err_mask_gcr_buff. Bit 2 = Reserved. Bit 3 = par_err_mask_tx_stt_rpr_snd_msg_state. Bit 4 = par_err_mask_gcrs_ld_state. Bit 5 = par_err_mask_gcrs_unld_state. Bit 6 = Reserved. Bit 7 = Reserved.
53:62	RO	constant = 0b0000000000
63	RWX	TX_PL_FIR_ERR_MASK: IOTK ALIAS: This bit is a FIR mask for the per-lane transmit register checker.

Register Name	Transmit Group FIR Error Mask Register
Mnemonic	IOF2.TX_WRAP.TX1.TXCTL.TX_CTL_SM.REGS.TX_FIR_MASK_PG
Address	800D0C200601143F (SCOM)
Description	This register masks transmit FIR per-group errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	TX_Per Group_FIR_ERRS_MASK: This field contains the FIR mask for register or state-machine parity checkers in the per-group TXCTL logic. A value of 1 masks the error from generating a FIR error. Bit 0 = par_err_mask_txctl_regs. Bit 1 = par_err_mask_gcr_buff. Bit 2 = Reserved. Bit 3 = par_err_mask_tx_stt_rpr_snd_msg_state. Bit 4 = par_err_mask_gcrs_ld_state. Bit 5 = par_err_mask_gcrs_unld_state. Bit 6 = Reserved. Bit 7 = Reserved.
53:62	RO	constant = 0b0000000000
63	RWX	TX_PL_FIR_ERR_MASK: IOTK ALIAS: This bit is a FIR mask for the per-lane transmit register checker.

Register Name	Transmit Reset Control Action Register
Mnemonic	IOF2.TX_WRAP.TX0.TXCTL.TX_CTL_SM.REGS.TX_FIR_RESET_PG
Address	800D14000601143F (SCOM)
Description	This register controls per-group transmit latches.

Bits	SCOM	Field Mnemonic: Description
0:61	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000
62	RWX	TX_CLR_PAR_ERRS: Clear all transmit parity error latches. Toggle this field 0→1→0 to clear all transmit parity error latches.
63	RWX	TX_FIR_RESET: FIR reset. Toggle this field 0→1→0 to reset all transmit FIR-related latches including parity error latches.

Register Name	Transmit Reset Control Action Register
Mnemonic	IOF2.TX_WRAP.TX1.TXCTL.TX_CTL_SM.REGS.TX_FIR_RESET_PG
Address	800D14200601143F (SCOM)
Description	This register controls per-group transmit latches.

Bits	SCOM	Field Mnemonic: Description
0:61	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000
62	RWX	TX_CLR_PAR_ERRS: Clear all transmit parity error latches. Toggle this field 0→1→0 to clear all transmit parity error latches.
63	RWX	TX_FIR_RESET: FIR reset. Toggle this field 0→1→0 to reset all transmit FIR-related latches including parity error latches.

Register Name	Transmit Per-Group FIR Error Injection Register
Mnemonic	IOF2.TX_WRAP.TX0.TXCTL.TX_CTL_SM.REGS.TX_FIR_ERROR_INJECT_PG
Address	800D1C000601143F (SCOM)
Description	This register is used to inject errors into per-group transmit registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	TX_PG_FIR_ERR_INJ: IOTK ALIAS: While 1, inverts the parity check bit to force an error on the per-group TXCTL register or the state-machine parity checkers.
53:63	RO	constant = 0b00000000000

Register Name	Transmit Per-Group FIR Error Injection Register
Mnemonic	IOF2.TX_WRAP.TX1.TXCTL.TX_CTL_SM.REGS.TX_FIR_ERROR_INJECT_PG
Address	800D1C200601143F (SCOM)
Description	This register is used to inject errors into per-group transmit registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	TX_PG_FIR_ERR_INJ: IOTK ALIAS: While 1, inverts the parity check bit to force an error on the per-group TXCTL register or the state-machine parity checkers.
53:63	RO	constant = 0b00000000000

Register Name	Transmit CTLSM Spare Mode Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX0.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_SPARE_MODE_PG
Address	800D24000601143F (SCOM)
Description	This register contains per-group spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PG_CTL_SM_SPARE_MODE_0: Per-group spare mode latch.

Bits	SCOM	Field Mnemonic: Description
49	RWX	TX_PG_CTL_SM_SPARE_MODE_1: Per-group spare mode latch.
50	RWX	TX_PG_CTL_SM_SPARE_MODE_2: Per-group spare mode latch.
51	RWX	TX_PG_CTL_SM_SPARE_MODE_3: Per-group spare mode latch.
52	RWX	TX_PG_CTL_SM_SPARE_MODE_4: Per-group spare mode latch.
53	RWX	TX_PG_CTL_SM_SPARE_MODE_5: Per-group spare mode latch.
54	RWX	TX_PG_CTL_SM_SPARE_MODE_6: Per-group spare mode latch.
55	RWX	TX_PG_CTL_SM_SPARE_MODE_7: Per-group spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Transmit CTLSM Spare Mode Per-Group Register**
Mnemonic	IOF2.TX_WRAP.TX1.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_SPARE_MODE_PG
Address	800D24200601143F (SCOM)
Description	This register contains per-group spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PG_CTL_SM_SPARE_MODE_0: Per-group spare mode latch.
49	RWX	TX_PG_CTL_SM_SPARE_MODE_1: Per-group spare mode latch.
50	RWX	TX_PG_CTL_SM_SPARE_MODE_2: Per-group spare mode latch.
51	RWX	TX_PG_CTL_SM_SPARE_MODE_3: Per-group spare mode latch.
52	RWX	TX_PG_CTL_SM_SPARE_MODE_4: Per-group spare mode latch.
53	RWX	TX_PG_CTL_SM_SPARE_MODE_5: Per-group spare mode latch.
54	RWX	TX_PG_CTL_SM_SPARE_MODE_6: Per-group spare mode latch.
55	RWX	TX_PG_CTL_SM_SPARE_MODE_7: Per-group spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Transmit CTLSM Mode 1 EO Per-Group Register**
Mnemonic	IOF2.TX_WRAP.TX0.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_MODE1_EO_PG
Address	800D2C000601143F (SCOM)
Description	This register controls the driver segment test and other settings.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PSAVE_WAKEUP_LANE0_ENABLE: This bit enables lane 0 at all times as the wakeup lane from psave mode.
49	RWX	TX_PSAVE_FENCE_ENABLE: This bit enables fencing of the transmitter when the psave_mode_ip output of the receiver is high.
50:57	RWX	TX_SEG_TEST_MODE: Driver segment test mode. When this field is all 0s, it means normal function mode. When this field is not all 0s, the segment test begins.
58	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
59	RWX	TX_FFE_BOOST_EN: Driver segment test. This bit enables the boost function of the NVLink transmit.
60	RO	constant = 0b0
61	RWX	TX_SEG_TEST_LEAKAGE_CTRL: This bit controls txr_txc_sst_ctl_dc in every transmit slice. 1 = Run the segment test in low-leakage mode.
62	RWX	TX_HALF_RATE_MODE: When set to 1, this bit enables timers on the slow clock domain to consistently count UI when in 4-bit legacy mode. Otherwise, the slow clock domain counts only half of the UI when in 4-bit legacy mode.
63	RO	constant = 0b0

Register Name	Transmit CTLSM Mode 1 EO Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX1.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_MODE1_EO_PG
Address	800D2C200601143F (SCOM)
Description	This register controls the driver segment test and other settings.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PSAVE_WAKEUP_LANE0_ENABLE: This bit enables lane 0 at all times as the wakeup lane from psave mode.
49	RWX	TX_PSAVE_FENCE_ENABLE: This bit enables fencing of the transmitter when the psave_mode_ip output of the receiver is high.
50:57	RWX	TX_SEG_TEST_MODE: Driver segment test mode. When this field is all 0s, it means normal function mode. When this field is not all 0s, the segment test begins.
58	RO	constant = 0b0
59	RWX	TX_FFE_BOOST_EN: Driver segment test. This bit enables the boost function of the NVLink transmit.
60	RO	constant = 0b0
61	RWX	TX_SEG_TEST_LEAKAGE_CTRL: This bit controls txr_txc_sst_ctl_dc in every transmit slice. 1 = Run the segment test in low-leakage mode.
62	RWX	TX_HALF_RATE_MODE: When set to 1, this bit enables timers on the slow clock domain to consistently count UI when in 4-bit legacy mode. Otherwise, the slow clock domain counts only half of the UI when in 4-bit legacy mode.
63	RO	constant = 0b0

Register Name	Transmit CTLSM CNTL1 EO Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX0.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_CNTL1_EO_PG
Address	800D34000601143F (SCOM)
Description	This register contains transmit pseg controls.

Bits	SCOM	Field Mnemonic: Description
0:50	RO	constant = 0b000000000000000000000000000000000000000000000000000
51:55	RWX	TX_PSEG_PRE_EN: This field is used for pre-bank pseg enable.
56:60	RWX	TX_PSEG_PRE_SEL: This field is used for pre-bank pseg mode selection.
61:63	RO	constant = 0b000

Register Name	Transmit CTLSM CNTL1 EO Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX1.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_CNTL1_EO_PG
Address	800D34200601143F (SCOM)
Description	This register contains transmit pseg controls.

Bits	SCOM	Field Mnemonic: Description
0:50	RO	constant = 0b000000000000000000000000000000000000000000000000000
51:55	RWX	TX_PSEG_PRE_EN: This field is used for pre-bank pseg enable.
56:60	RWX	TX_PSEG_PRE_SEL: This field is used for pre-bank pseg mode selection.
61:63	RO	constant = 0b000

Register Name	Transmit CTLSM CNTL2 EO Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX0.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_CNTL2_EO_PG
Address	800D3C000601143F (SCOM)
Description	This register contains transmit per-group controls.

Bits	SCOM	Field Mnemonic: Description
0:50	RO	constant = 0b000000000000000000000000000000000000000000000000000
51:55	RWX	TX_NSEG_PRE_EN: This field is used for pre-bank nseg enable.
56:60	RWX	TX_NSEG_PRE_SEL: This field is used for pre-bank nseg mode selection.
61:63	RO	constant = 0b000

Register Name	Transmit CTLSM CNTL2 EO Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX1.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_CNTL2_EO_PG
Address	800D3C200601143F (SCOM)
Description	This register contains transmit per-group controls.

Bits	SCOM	Field Mnemonic: Description
0:50	RO	constant = 0b000000000000000000000000000000000000000000000000000
51:55	RWX	TX_NSEG_PRE_EN: This field is used for pre-bank nseg enable.
56:60	RWX	TX_NSEG_PRE_SEL: This field is used for pre-bank nseg mode selection.
61:63	RO	constant = 0b000

Register Name	Transmit CTLSM CNTL3 EO Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX0.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_CNTL3_EO_PG
Address	800D44000601143F (SCOM)
Description	This register contains transmit per-group controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RWX	TX_PSEG_MARGINPU_EN: This field is used for margin pull-up bank pseg enable.
56:63	RWX	TX_PSEG_MARGINPD_EN: This field is used for margin pull-down bank pseg enable.

Register Name	Transmit CTLSM CNTL3 EO Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX1.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_CNTL3_EO_PG
Address	800D44200601143F (SCOM)
Description	This register contains transmit per-group controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	TX_PSEG_MARGINPU_EN: This field is used for margin pull-up bank pseg enable.
56:63	RWX	TX_PSEG_MARGINPD_EN: This field is used for margin pull-down bank pseg enable.

Register Name	Transmit CTLSM CNTL4 EO Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX0.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_CNTL4_EO_PG
Address	800D4C000601143F (SCOM)
Description	This register contains transmit per-group controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	TX_NSEG_MARGINPU_EN: This field is used for margin pull-up bank nseg enable.
56:63	RWX	TX_NSEG_MARGINPD_EN: This field is used for margin pull-down bank nseg enable.

Register Name	Transmit CTLSM CNTL4 EO Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX1.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_CNTL4_EO_PG
Address	800D4C200601143F (SCOM)
Description	This register contains transmit per-group controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	TX_NSEG_MARGINPU_EN: This field is used for margin pull-up bank nseg enable.
56:63	RWX	TX_NSEG_MARGINPD_EN: This field is used for margin pull-down bank nseg enable.

Register Name	Transmit CTLSM CNTL5 EO Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX0.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_CNTL5_EO_PG
Address	800D54000601143F (SCOM)
Description	This register contains transmit per-group controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	TX_MARGINPU_SEL: This field is used for margin pull-up bank mode selection.
56:63	RWX	TX_MARGINPD_SEL: This field is used for margin pull-down bank mode selection.

Register Name	Transmit CTLSM CNTL5 EO Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX1.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_CNTL5_EO_PG
Address	800D54200601143F (SCOM)
Description	This register contains transmit per-group controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	TX_MARGINPU_SEL: This field is used for margin pull-up bank mode selection.
56:63	RWX	TX_MARGINPD_SEL: This field is used for margin pull-down bank mode selection.

Register Name	Transmit CTLSM CNTL6 EO Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX0.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_CNTL6_EO_PG
Address	800D5C000601143F (SCOM)
Description	This register contains transmit per-group controls.

Bits	SCOM	Field Mnemonic: Description
0:50	RO	constant = 0b000000000000000000000000000000000000000000000000000
51:63	RWX	TX_PSEG_MAIN_EN: This field is used for main bank pseg enable.

Register Name	Transmit CTLSM CNTL6 EO Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX1.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_CNTL6_EO_PG
Address	800D5C200601143F (SCOM)
Description	This register contains transmit per-group controls.

Bits	SCOM	Field Mnemonic: Description
0:50	RO	constant = 0b000000000000000000000000000000000000000000000000000
51:63	RWX	TX_PSEG_MAIN_EN: This field is used for main bank pseg enable.

Register Name	Transmit CTLSM CNTL7 EO Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX0.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_CNTL7_EO_PG
Address	800D64000601143F (SCOM)
Description	This register contains transmit per-group controls.

Bits	SCOM	Field Mnemonic: Description
0:50	RO	constant = 0b000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
51:63	RWX	TX_NSEG_MAIN_EN: This field is used for main bank nseg enable.

Register Name	Transmit CTLSM CNTL7 EO Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX1.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_CNTL7_EO_PG
Address	800D64200601143F (SCOM)
Description	This register contains transmit per-group controls.

Bits	SCOM	Field Mnemonic: Description
0:50	RO	constant = 0b000000000000000000000000000000000000000000000000000
51:63	RWX	TX_NSEG_MAIN_EN: This field is used for main bank nseg enable.

Register Name	Transmit CTLSM STAT1 EO Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX0.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_STAT1_EO_PG
Address	800D6C000601143F (SCOM)
Description	This register contains TXBIST information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_CLK_BIST_ERR: This bit indicates that a TXBIST clock side error occurred. 0b0 = No error. 0b1 = A clock side error was found.
49	RWX	TX_CLK_BIST_ACTIVITY_DET: This bit indicates that activity was detected in the PRBS checker for the clock pattern. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50	ROX	Reserved field.
51:55	ROX	Reserved field.
56:63	RO	constant = 0b00000000

Register Name	Transmit CTLSM STAT1 EO Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX1.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_STAT1_EO_PG
Address	800D6C200601143F (SCOM)
Description	This register contains TXBIST information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_CLK_BIST_ERR: This bit indicates that a TXBIST clock side error occurred. 0b0 = No error. 0b1 = A clock side error was found.
49	RWX	TX_CLK_BIST_ACTIVITY_DET: This bit indicates that activity was detected in the PRBS checker for the clock pattern. 0b0 = No activity. 0b1 = Activity was found during TXBIST.

Bits	SCOM	Field Mnemonic: Description
50	ROX	Reserved field.
51:55	ROX	Reserved field.
56:63	RO	constant = 0b00000000

Register Name	Transmit CTLSM CNTLG1 E Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX0.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_CNTLG1_E_PG
Address	800D84000601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CTLSM CNTLG1 E Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX1.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_CNTLG1_E_PG
Address	800D84200601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CTLSM STAT1 E Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX0.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_STAT1_E_PG
Address	800D8C000601143F (SCOM)
Description	This register contains the driver segment test results.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50:51	RWX	TX_SEG_TEST_CLK_STATUS: This field contains the driver segment test result for the clock lane. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:63	RO	constant = 0b000000000000

Register Name	Transmit CTLSM STAT1 E Per-Group Register
Mnemonic	IOF2.TX_WRAP.TX1.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_STAT1_E_PG
Address	800D8C200601143F (SCOM)
Description	This register contains the driver segment test results.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50:51	RWX	TX_SEG_TEST_CLK_STATUS: This field contains the driver segment test result for the clock lane. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:63	RO	constant = 0b000000000000

Register Name	Transmit Impedance Calibration Per-Bus Register
Mnemonic	IOF2.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.TX_IMPCAL_PB
Address	800F04000601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant = 0b0000000000000000000000000000000000000000000000000
49	NCX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	NCX	Reserved field.
54	ROX	Reserved field.
55:63	ROX	Reserved field.

Register Name	Transmit Impedance Calibration NVAL Per-Bus Register
Mnemonic	IOF2.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.TX_IMPCAL_NVAL_PB
Address	800F0C000601143F (SCOM)
Description	This register is used for impedance calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:56	RWX	TX_ZCAL_N: Calibration circuit NSeg enable value. This field holds the current value of the enabled segments. It is a 4x multiple of the actual segment count. It can be read for the current calibration result set during the calibration sequence. It can be written to immediately update circuit enables on each write. It is used with tx_zcal_swo_* for manual calibration. Do not write to this field when tx_zcal_req = 1. (binary code - 0x00 is zero slices, and 0xA1 is maximum slices).
57:63	RO	constant = 0b0000000

Register Name	Transmit Impedance Calibration PVAL Per-Bus Register
Mnemonic	IOF2.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.TX_IMPCAL_PVAL_PB
Address	800F14000601143F (SCOM)
Description	This register is used for impedance calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:56	RWX	TX_ZCAL_P: Calibration circuit PSeg enable value. This field holds the current value of the enabled segments. It is a 4x multiple of the actual segment count. It can be read for the current calibration result set during the calibration sequence. It can be written to immediately update circuit enables on each write. It is used with tx_zcal_swo_* for manual calibration. Do not write this field when tx_zcal_req = 1. (binary code - 0x00 is zero slices, and 0xA1 is maximum slices).
57:63	RO	constant = 0b0000000

Register Name	Transmit Impedance Calibration P 4X Per-Bus Register
Mnemonic	IOF2.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.TX_IMPCAL_P_4X_PB
Address	800F1C000601143F (SCOM)
Description	This register is used for impedance calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	TX_ZCAL_P_4X: Calibration circuit PSeg-4X enable value. This field holds the current value of the enabled segments. It is a 2x multiple of the actual segment count. It can be read for the current calibration result set during the calibration sequence. It can be written to immediately update circuit enables on each write. It is used with tx_zcal_swo_* for manual calibration. Do not write this field when tx_zcal_req = 1. (binary code - 0x00 is zero slices and 0x15 is maximum slices).
53:63	RO	constant = 0b00000000000

Register Name	Transmit Impedance Calibration SWO1 Per-Bus Register
Mnemonic	IOF2.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.TX_IMPCAL_SWO1_PB
Address	800F24000601143F (SCOM)
Description	This register is used for impedance calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_ZCAL_SWO_EN: Impedance calibration software override. This bit steers all calibration controls directly from these register fields. It effectively disables the state-machine logic (default). 0b0 = Inactive. 0b1 = Enable.
49	RWX	TX_ZCAL_SWO_CAL_SEGS: Impedance calibration software bank select. This bit enables PSeg calibration (default). 0b0 = Select NSeg bank comparison. 0b1 = Select PSeg bank comparison.
50	RWX	TX_ZCAL_SWO_CMP_INV: Impedance calibration software compare invert. This bit swaps calibration circuit comparator inputs (default). 0b0 = Select NSeg bank comparison. 0b1 = Select PSeg bank comparison.
51	RWX	TX_ZCAL_SWO_CMP_OFFSET: Impedance calibration software offset flush. This bit equalizes the comparator offset in the calibration circuit (default). 0b0 = Disable offset. 0b1 = Enable offset.

Bits	SCOM	Field Mnemonic: Description
52	RWX	TX_ZCAL_SWO_CMP_RESET: Impedance calibration software comparator reset. This bit resets the comparator in the calibration circuit (default). 0b0 = Disable reset. 0b1 = Enable reset.
53	RWX	TX_ZCAL_SWO_POWERDOWN: Impedance calibration software circuit power down. This bit enables the power-down calibration circuit (default). 0b0 = Disable power down. 0b1 = Enable power down.
54	RWX	TX_ZCAL_SWO_TCOIL: Impedance calibration software circuit TCoil.
55	RWX	TX_ZCAL_RANGE_CHECK: This bit controls the usage of tx_zcal_sm_min/max_val. 0 = These two registers are used to define the range of zcal. 1 = The calibration range is 1 - 80, and the minimum/maximum registers are only used to check whether the result is in range.
56	RWX	TX_ZCAL_CYA_DATA_INV: Impedance calibration CYA sample inversion. This bit selects inverted comparator values in case of a hardware error (default). 0b0 = No sample inversion. 0b1 = Invert samples.
57	RWX	TX_ZCAL_TEST_OVR_2R: Impedance calibration test-only 2R segment override.
58	RWX	TX_ZCAL_TEST_OVR_1R: Impedance calibration test-only 1R segment override.
59	RWX	TX_ZCAL_TEST_OVR_4X_SEG: Impedance calibration test-only 4x segment override.
60	RWX	TX_ZCAL_TEST_CLK_DIV: This register controls the clock for impedance BIST. 1 = The clock is divided by 32. 0 = PLL bypass mode is needed.
61:63	RO	constant = 0b000

Register Name	Transmit Impedance Calibration SWO2 Per-Bus Register
Mnemonic	IOF2.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.TX_IMPCAL_SWO2_PB
Address	800F2C000601143F (SCOM)
Description	This register is used for impedance calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	TX_ZCAL_SM_MIN_VAL: Impedance calibration minimum search threshold. This low-side segment count limit is used in the calibration process. (binary code - 0x00 is zero slices, and 0x50 is maximum slices).
55:61	RWX	TX_ZCAL_SM_MAX_VAL: Impedance calibration maximum search threshold. This high-side segment count limit is used in the calibration process. (binary code - 0x00 is zero slices and 0x50 is maximum slices).
62:63	RO	constant = 0b00

Register Name	Spare Mode Per-Bus Register
Mnemonic	IOF2.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.SPARE_MODE_PB
Address	800F34000601143F (SCOM)
Description	This register contains per-bus spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	PB_SPARE_MODE_0: Per-bus spare mode latch.
49	RWX	PB_SPARE_MODE_1: Per-bus spare mode latch.
50	RWX	PB_SPARE_MODE_2: Per-bus spare mode latch.
51	RWX	PB_SPARE_MODE_3: Per-bus spare mode latch.
52	RWX	PB_SPARE_MODE_4: Per-bus spare mode latch.
53	RWX	PB_SPARE_MODE_5: Per-bus spare mode latch.
54	RWX	PB_SPARE_MODE_6: Per-bus spare mode latch.
55	RWX	PB_SPARE_MODE_7: Per-bus spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Transmit IMPCAL2 Per-Bus Register**
Mnemonic	IOF2.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.TX_IMPCAL2_PB
Address	800F3C000601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant = 0b0000000000000000000000000000000000000000000000000
49	ROX	Reserved field.
50	ROX	Reserved field.
51:52	RO	constant = 0b00
53	NCX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.
56:63	RO	constant = 0b00000000

Register Name	**Receive FIR Reset Per-Bus Register**
Mnemonic	IOF2.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.RX_FIR_RESET_PB
Address	800F80000601143F (SCOM)
Description	This register controls per-bus transmit latches.

Bits	SCOM	Field Mnemonic: Description
0:61	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000
62	RWX	RX_PB_CLR_PAR_ERRS: Clear all receive parity error latches. Toggle this field 0→1→0 to clear parity-error latches in the BUSCTL logic.
63	RWX	RX_PB_FIR_RESET: FIR reset. Toggle this field 0→1→0 to reset the BUSCTL logic FIR-related latches, including the isolation and parity-error latches.

Register Name	Receive FIR Per-Bus Register
Mnemonic	IOF2.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.RX_FIR_PB
Address	800F88000601143F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:57	ROX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive FIR Mask Per-Bus Register
Mnemonic	IOF2.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.RX_FIR_MASK_PB
Address	800F90000601143F (SCOM)
Description	This register masks receive FIR per-bus errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:57	RWX	RX_PB_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pb errors.
58:63	RO	constant = 0b000000

Register Name	Receive FIR Error Inject Per-Bus Register
Mnemonic	IOF2.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.RX_FIR_ERROR_INJECT_PB
Address	800F98000601143F (SCOM)
Description	This register is used to inject errors into the per-bus receive registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:57	RWX	RX_PB_FIR_ERRS_INJ: IOTK ALIAS: Receive per-bus parity error injection. This field allows injection of non-destructive parity errors in either register or state-machine latch banks. The register or state value is not affected.
58:63	RO	constant = 0b000000

5. OB 0 Chiplet

The POWER9 processor registers are listed alphabetically by mnemonic in the following address table.

Mnemonic	Address	Page
IOO0.IOO_CPLT.BUSCTL.SCOM.SCOM_MODE_PB	0x0000000009010C20	1230
IOO0.IOO_PPE.SCOM_PPE_CNTL	0x0000000009011060	1230
IOO0.IOO_PPE.SCOM_PPE_FLAGS	0x0000000009011063	1231
IOO0.IOO_PPE.SCOM_PPE_WORK_REG1	0x0000000009011061	1231
IOO0.IOO_PPE.SCOM_PPE_WORK_REG2	0x0000000009011062	1231
PB.IOO.LL0.IOOL_CONFIG	0x000000000901080A	1215
PB.IOO.LL0.IOOL_CONTROL	0x000000000901080B	1215
PB.IOO.LL0.IOOL_DLL_STATUS	0x0000000009010828	1229
PB.IOO.LL0.IOOL_ERR_INJ_LFSR	0x000000000901081B	1224
PB.IOO.LL0.IOOL_LAT_MEASURE	0x000000000901080E	1217
PB.IOO.LL0.IOOL_LINK0_EDPL_STATUS	0x0000000009010824	1227
PB.IOO.LL0.IOOL_LINK0_ERROR_STATUS	0x0000000009010816	1221
PB.IOO.LL0.IOOL_LINK0_INFO	0x0000000009010814	1220
PB.IOO.LL0.IOOL_LINK0_QUALITY	0x0000000009010826	1228
PB.IOO.LL0.IOOL_LINK0_RX_LANE_CONTROL	0x0000000009010812	1220
PB.IOO.LL0.IOOL_LINK0_SYN_CAPTURE	0x0000000009010822	1226
PB.IOO.LL0.IOOL_LINK0_TX_LANE_CONTROL	0x0000000009010810	1219
PB.IOO.LL0.IOOL_LINK1_EDPL_STATUS	0x0000000009010825	1228
PB.IOO.LL0.IOOL_LINK1_ERROR_STATUS	0x0000000009010817	1222
PB.IOO.LL0.IOOL_LINK1_INFO	0x0000000009010815	1221
PB.IOO.LL0.IOOL_LINK1_QUALITY	0x0000000009010827	1228
PB.IOO.LL0.IOOL_LINK1_RX_LANE_CONTROL	0x0000000009010813	1220
PB.IOO.LL0.IOOL_LINK1_SYN_CAPTURE	0x0000000009010823	1227
PB.IOO.LL0.IOOL_LINK1_TX_LANE_CONTROL	0x0000000009010811	1219
PB.IOO.LL0.IOOL_LINKX_ERROR_STATUS	0x0000000009010829	1229
PB.IOO.LL0.IOOL_OPTICAL_CONFIG	0x000000000901080F	1218
PB.IOO.LL0.IOOL_PERF_COUNTERS_0	0x000000000901081E	1225
PB.IOO.LL0.IOOL_PERF_COUNTERS_1	0x000000000901081F	1226
PB.IOO.LL0.IOOL_PERF_COUNT_LSB_0	0x0000000009010820	1226
PB.IOO.LL0.IOOL_PERF_COUNT_LSB_1	0x0000000009010821	1226
PB.IOO.LL0.IOOL_PERF_SEL_CONFIG	0x000000000901081D	1225
PB.IOO.LL0.IOOL_PERF_TRACE_CONFIG	0x000000000901081C	1224
PB.IOO.LL0.IOOL_PHY_CONFIG	0x000000000901080C	1216
PB.IOO.LL0.IOOL_REPLAY_THRESHOLD	0x0000000009010818	1222
PB.IOO.LL0.IOOL_RETRAIN_THRESHOLD	0x000000000901081A	1223
PB.IOO.LL0.IOOL_SEC_CONFIG	0x000000000901080D	1217
PB.IOO.LL0.IOOL_SL_ECC_THRESHOLD	0x0000000009010819	1223
PB.IOO.LL0.PB_IOOL_FIR_ACTION0_REG	0x0000000009010806	1214
PB.IOO.LL0.PB_IOOL_FIR_ACTION1_REG	0x0000000009010807	1214
PB.IOO.LL0.PB_IOOL_FIR_MASK_REG	0x0000000009010803	1212
PB.IOO.LL0.PB_IOOL_FIR_REG	0x0000000009010800	1210
TP.TCOB0.OB.BIST	0x000000000903000B	1240

Mnemonic	Address	Page
TP.TCOB0.OB.CC_ATOMIC_LOCK_REG	0x00000000090303FF	1248
TP.TCOB0.OB.CC_PROTECT_MODE_REG	0x00000000090303FE	1248
TP.TCOB0.OB.CLK_REGION	0x0000000009030006	1237
TP.TCOB0.OB.CLOCK_STAT_ARY	0x000000000903000A	1239
TP.TCOB0.OB.CLOCK_STAT_NSL	0x0000000009030009	1238
TP.TCOB0.OB.CLOCK_STAT_SL	0x0000000009030008	1237
TP.TCOB0.OB.CPLT_CONF0	0x0000000009000008	1187
TP.TCOB0.OB.CPLT_CONF1	0x0000000009000009	1188
TP.TCOB0.OB.CPLT_CTRL0	0x0000000009000000	1184
TP.TCOB0.OB.CPLT_CTRL1	0x0000000009000001	1186
TP.TCOB0.OB.CPLT_MASK0	0x0000000009000101	1190
TP.TCOB0.OB.CPLT_STAT0	0x0000000009000100	1189
TP.TCOB0.OB.CTRL_ATOMIC_LOCK_REG	0x00000000090003FF	1190
TP.TCOB0.OB.CTRL_PROTECT_MODE_REG	0x00000000090003FE	1190
TP.TCOB0.OB.DBG_CBS_CC	0x0000000009030013	1247
TP.TCOB0.OB.EPS.DBG.DBG_INST1_COND_REG_1	0x00000000090107C1	1198
TP.TCOB0.OB.EPS.DBG.DBG_INST1_COND_REG_2	0x00000000090107C2	1201
TP.TCOB0.OB.EPS.DBG.DBG_INST1_COND_REG_3	0x00000000090107C3	1202
TP.TCOB0.OB.EPS.DBG.DBG_INST2_COND_REG_1	0x00000000090107C4	1202
TP.TCOB0.OB.EPS.DBG.DBG_INST2_COND_REG_2	0x00000000090107C5	1205
TP.TCOB0.OB.EPS.DBG.DBG_INST2_COND_REG_3	0x00000000090107C6	1206
TP.TCOB0.OB.EPS.DBG.DBG_MODE_REG	0x00000000090107C0	1198
TP.TCOB0.OB.EPS.DBG.DBG_TRACE_MODE_REG_2	0x00000000090107CF	1209
TP.TCOB0.OB.EPS.DBG.DBG_TRACE_REG_0	0x00000000090107CD	1206
TP.TCOB0.OB.EPS.DBG.DBG_TRACE_REG_1	0x00000000090107CE	1208
TP.TCOB0.OB.EPS.DBG.DEBUG_TRACE_CONTROL	0x00000000090107D0	1209
TP.TCOB0.OB.EPS.DBG.XTRA_TRACE_MODE	0x00000000090107D1	1210
TP.TCOB0.OB.EPS.FIR.GXSTOP0_MASK_REG	0x0000000009040014	1254
TP.TCOB0.OB.EPS.FIR.GXSTOP1_MASK_REG	0x0000000009040015	1255
TP.TCOB0.OB.EPS.FIR.GXSTOP2_MASK_REG	0x0000000009040016	1255
TP.TCOB0.OB.EPS.FIR.GXSTOP_TRIG_REG	0x0000000009040013	1254
TP.TCOB0.OB.EPS.FIR.LOCAL_FIR_ACTION0	0x0000000009040010	1253
TP.TCOB0.OB.EPS.FIR.LOCAL_FIR_ACTION1	0x0000000009040011	1254
TP.TCOB0.OB.EPS.FIR.LOCAL_FIR_MASK	0x000000000904000D	1253
TP.TCOB0.OB.EPS.FIR.MODE_REG	0x0000000009040008	1251
TP.TCOB0.OB.EPS.FIR.SUM_MASK_REG	0x0000000009040017	1256
TP.TCOB0.OB.EPS.PSC.PSC.ADDR_TRAP_REG	0x0000000009010003	1193
TP.TCOB0.OB.EPS.PSC.PSC.ATOMIC_LOCK_MASK_LATCH_REG	0x0000000009010007	1194
TP.TCOB0.OB.EPS.PSC.PSC.PSCOM_ERROR_MASK	0x0000000009010002	1192
TP.TCOB0.OB.EPS.PSC.PSC.PSCOM_MODE_REG	0x0000000009010000	1190
TP.TCOB0.OB.EPS.PSC.PSC.PSCOM_STATUS_ERROR_REG	0x0000000009010001	1191
TP.TCOB0.OB.EPS.PSC.PSC.RING_FENCE_MASK_LATCH_REG	0x0000000009010008	1194
TP.TCOB0.OB.EPS.PSC.PSC.WRITE_PROTECT_ENABLE_REG	0x0000000009010005	1193
TP.TCOB0.OB.EPS.PSC.PSC.WRITE_PROTECT_RINGS_REG	0x0000000009010006	1193
TP.TCOB0.OB.EPS.THERM.CONTROL_REG	0x0000000009050012	1260
TP.TCOB0.OB.EPS.THERM.DTS_RESULT0	0x0000000009050000	1257
TP.TCOB0.OB.EPS.THERM.DTS_TRC_RESULT	0x0000000009050003	1257
TP.TCOB0.OB.EPS.THERM.ERR_STATUS_REG	0x0000000009050013	1260

Mnemonic	Address	Page
TP.TCOB0.OB.EPS.THERM.INJECT_REG	0x0000000009050011	1260
TP.TCOB0.OB.EPS.THERM.SKITTER_CLKSRC_REG	0x0000000009050016	1263
TP.TCOB0.OB.EPS.THERM.SKITTER_DATA0	0x0000000009050019	1263
TP.TCOB0.OB.EPS.THERM.SKITTER_DATA1	0x000000000905001A	1263
TP.TCOB0.OB.EPS.THERM.SKITTER_DATA2	0x000000000905001B	1264
TP.TCOB0.OB.EPS.THERM.SKITTER_FORCE_REG	0x0000000009050014	1263
TP.TCOB0.OB.EPS.THERM.SKITTER_MODE_REG	0x0000000009050010	1259
TP.TCOB0.OB.EPS.THERM.THERM_MODE_REG	0x000000000905000F	1258
TP.TCOB0.OB.EPS.THERM.TIMESTAMP_COUNTER_READ	0x000000000905001C	1264
TP.TCOB0.OB.ERROR_STATUS	0x000000000903000F	1244
TP.TCOB0.OB.FIR_MASK	0x0000000009040002	1249
TP.TCOB0.OB.HOSTATTN	0x0000000009040009	1251
TP.TCOB0.OB.HOSTATTN_MASK	0x000000000904001A	1257
TP.TCOB0.OB.LOCAL_FIR	0x000000000904000A	1252
TP.TCOB0.OB.LOCAL_XSTOP_ERR	0x0000000009040018	1256
TP.TCOB0.OB.LOCAL_XSTOP_MASK	0x0000000009040019	1257
TP.TCOB0.OB.OPCG_ALIGN	0x0000000009030001	1232
TP.TCOB0.OB.OPCG_CAPT1	0x0000000009030010	1245
TP.TCOB0.OB.OPCG_CAPT2	0x0000000009030011	1246
TP.TCOB0.OB.OPCG_CAPT3	0x0000000009030012	1247
TP.TCOB0.OB.OPCG_REG0	0x0000000009030002	1234
TP.TCOB0.OB.OPCG_REG1	0x0000000009030003	1235
TP.TCOB0.OB.OPCG_REG2	0x0000000009030004	1235
TP.TCOB0.OB.RFIR	0x0000000009040001	1249
TP.TCOB0.OB.SCAN_REGION_TYPE	0x0000000009030005	1236
TP.TCOB0.OB.SPATTN	0x0000000009040004	1250
TP.TCOB0.OB.SPA_MASK	0x0000000009040007	1250
TP.TCOB0.OB.SYNC_CONFIG	0x0000000009030000	1231
TP.TCOB0.OB.TRA0.TR0.TRACE_HI_DATA_REG	0x0000000009010400	1194
TP.TCOB0.OB.TRA0.TR0.TRACE_LO_DATA_REG	0x0000000009010401	1194
TP.TCOB0.OB.TRA0.TR0.TRACE_TRCTRL_CONFIG	0x0000000009010402	1195
TP.TCOB0.OB.TRA0.TR0.TRACE_TRDATA_CONFIG_0	0x0000000009010403	1195
TP.TCOB0.OB.TRA0.TR0.TRACE_TRDATA_CONFIG_1	0x0000000009010404	1195
TP.TCOB0.OB.TRA0.TR0.TRACE_TRDATA_CONFIG_2	0x0000000009010405	1195
TP.TCOB0.OB.TRA0.TR0.TRACE_TRDATA_CONFIG_3	0x0000000009010406	1196
TP.TCOB0.OB.TRA0.TR0.TRACE_TRDATA_CONFIG_4	0x0000000009010407	1196
TP.TCOB0.OB.TRA0.TR0.TRACE_TRDATA_CONFIG_5	0x0000000009010408	1196
TP.TCOB0.OB.TRA0.TR0.TRACE_TRDATA_CONFIG_9	0x0000000009010409	1196
TP.TCOB0.OB.XFIR	0x0000000009040000	1249
TP.TCOB0.OB.XSTOP1	0x000000000903000C	1241
TP.TCOB0.OB.XSTOP2	0x000000000903000D	1242
TP.TCOB0.OB.XSTOP3	0x000000000903000E	1243

The POWER9 processor registers are listed in the following tables.

Register Name	Chiplet Control Register 0
Mnemonic	TP.TCOB0.OB.CPLT_CTRL0
Address	0000000009000000 (SCOM) 0000000009000010 (SCOM1) 0000000009000020 (SCOM2)
Description	This register contains the first set of vital chiplet controls.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_OR	WO_CLEAR	CTRL_CC_ABSTCLK_MUXSEL_DC: Select the ABIST clock source for arrays on a chiplet boundary. When set to 1, clocks are used from a chiplet with ABIST.
1	RW	WO_OR	WO_CLEAR	TC_UNIT_SYNCCLK_MUXSEL_DC: Select the synchronous clock for asynchronous latches. (The initial value is 1.)
2	RW	WO_OR	WO_CLEAR	CTRL_CC_FLUSHMODE_INH_DC: Prevent pipeline latches from going into flush mode. (The initial value is 1.)
3	RW	WO_OR	WO_CLEAR	CTRL_CC_FORCE_ALIGN_DC: Force an alignment signal to be sent. (The initial value is 1. Drop before dropping flushmode_inh.)
4	RW	WO_OR	WO_CLEAR	TC_UNIT_ARY_WRT_THRU_DC: Set the array into write-through mode. Used for LBIST.
5	RW	WO_OR	WO_CLEAR	TC_UNIT_AVP_MODE: Switches from refresh pulse to phase counter.
6	RW	WO_OR	WO_CLEAR	FREE_USAGE_6A: Free usage.
7	RW	WO_OR	WO_CLEAR	FREE_USAGE_7A: Free usage.
8	RW	WO_OR	WO_CLEAR	CTRL_CC_ABIST_RECOV_DISABLE_DC: New signal to disable recovery.
9	RW	WO_OR	WO_CLEAR	FREE_USAGE_9A: Free usage.
10	RW	WO_OR	WO_CLEAR	TC_UNIT_IOBIST_TX_WRAP_ENABLE_DC:
11	RW	WO_OR	WO_CLEAR	RESERVED_11A: Reserved.
12	RW	WO_OR	WO_CLEAR	TC_SKIT_MODE_BIST_DC:
13	RW	WO_OR	WO_CLEAR	TC_UNIT_DETERMINISTIC_TEST_ENABLE_DC: Forces login into deterministic test mode. For example, for LBIST.
14	RW	WO_OR	WO_CLEAR	TC_UNIT_CONSTRAIN_SAFESCAN_DC: Safe scan of N1L latches. Prevent lock when switching SE.
15	RW	WO_OR	WO_CLEAR	TC_UNIT_RRFA_TEST_ENABLE_DC:
16	RW	WO_OR	WO_CLEAR	TC_NBTI_HDR_ENABLE_OVR_DC: NBTI.
17	RW	WO_OR	WO_CLEAR	TC_NBTI_PROBE_GATE_DC: NBTI.
18	RW	WO_OR	WO_CLEAR	RESERVED_18A: Reserved.
19	RW	WO_OR	WO_CLEAR	RESERVED_19A: Reserved.
20:27	RW	WO_OR	WO_CLEAR	TC_PSRO_SEL_DC: PSRO select.
28	RW	WO_OR	WO_CLEAR	TC_BSC_WRAPSEL_DC: Wrap select for BSC.
29	RW	WO_OR	WO_CLEAR	TC_BSC_INTMODE_DC: INT Mode for BSC.
30	RW	WO_OR	WO_CLEAR	TC_BSC_INV_DC: INV for BSC mode.
31	RW	WO_OR	WO_CLEAR	TC_BSC_EXTMODE_DC: EXT mode for BSC.
32	RW	WO_OR	WO_CLEAR	TC_REFCLK_DRVR_EN_DC: Reference clock driver enable.
33	RW	WO_OR	WO_CLEAR	RESERVED_33A: Reserved.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
34	RW	WO_OR	WO_CLEAR	RESERVED_34A: Reserved.
35	RW	WO_OR	WO_CLEAR	RESERVED_35A: Reserved.
36	RW	WO_OR	WO_CLEAR	TC_OELCC_EDGE_DELAYED_DC: Allows to delay the alignment by one fast cycle. Only used in dual mesh chiplets.
37	RW	WO_OR	WO_CLEAR	TC_OELCC_ALIGN_FLUSH_DC: Forces the alignment and odd/even toggling latch into a flush state. For DFT only.
38	RW	WO_OR	WO_CLEAR	RESERVED_38A: Reserved.
39	RW	WO_OR	WO_CLEAR	RESERVED_39A: Reserved.
40:41	RW	WO_OR	WO_CLEAR	CTRL_MISC_CLKDIV_SEL_DC: Clock divider select. 00 = 1024:1 01 = 64:1 10 = 16:1 11 = 4:1
42	RW	WO_OR	WO_CLEAR	RESERVED_42A: Reserved.
43	RW	WO_OR	WO_CLEAR	RESERVED_43A: Reserved.
44	RW	WO_OR	WO_CLEAR	CTRL_CC_DCTEST_DC: TE = 1 only. Enable DCTEST.
45	RW	WO_OR	WO_CLEAR	CTRL_CC_OTP_PRGMODE_DC: TE = 1 only. OTP ROM program mode.
46	RW	WO_OR	WO_CLEAR	CTRL_CC_SSS_CALIBRATE_DC: TE = 1 only. Sensors calibration.
47	RW	WO_OR	WO_CLEAR	CTRL_CC_PIN_LBIST_DC: TE = 1 only. PIN LBIST mode. The LBIST is controlled by the pin, not by the OPCG.
48	RW	WO_OR	WO_CLEAR	FREE_USAGE_48A: Free usage.
49	RW	WO_OR	WO_CLEAR	FREE_USAGE_49A: Free usage.
50	RW	WO_OR	WO_CLEAR	FREE_USAGE_50A: Free usage.
51	RW	WO_OR	WO_CLEAR	FREE_USAGE_51A: Free usage.
52	RW	WO_OR	WO_CLEAR	FREE_USAGE_52A: Free usage.
53	RW	WO_OR	WO_CLEAR	FREE_USAGE_53A: Free usage.
54	RW	WO_OR	WO_CLEAR	FREE_USAGE_54A: Free usage.
55	RW	WO_OR	WO_CLEAR	FREE_USAGE_55A: Free usage.
56	RW	WO_OR	WO_CLEAR	FREE_USAGE_56A: Free usage.
57	RW	WO_OR	WO_CLEAR	FREE_USAGE_57A: Free usage.
58	RW	WO_OR	WO_CLEAR	FREE_USAGE_58A: Free usage.
59	RW	WO_OR	WO_CLEAR	FREE_USAGE_59A: Free usage.
60	RW	WO_OR	WO_CLEAR	FREE_USAGE_60A: Free usage.
61	RW	WO_OR	WO_CLEAR	FREE_USAGE_61A: Free usage.
62	RW	WO_OR	WO_CLEAR	FREE_USAGE_62A: Free usage.
63	RW	WO_OR	WO_CLEAR	FREE_USAGE_63A: Free usage.

Register Name	Chiplet Control Register 1
Mnemonic	TP.TCOB0.OB.CPLT_CTRL1
Address	0000000009000001 (SCOM) 0000000009000011 (SCOM1) 0000000009000021 (SCOM2)
Description	This register contains the second set of vital chiplet controls.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_OR	WO_CLEAR	UNUSED_0B: Unused.
1	RW	WO_OR	WO_CLEAR	UNUSED_1B: Unused.
2	RW	WO_OR	WO_CLEAR	UNUSED_2B: Unused.
3	RW	WO_OR	WO_CLEAR	TC_VITL_REGION_FENCE: VITL fence. Protect the VITL region logic from pollution by other regions during LBIST, or when the chiplet is not initialized and running yet.
4	RW	WO_OR	WO_CLEAR	TC_PERV_REGION_FENCE: Fence for pervasive region.
5	RW	WO_OR	WO_CLEAR	TC_REGION1_FENCE: Fence for region pbiooa0 (PB).
6	RW	WO_OR	WO_CLEAR	TC_REGION2_FENCE: Fence for region ioo0 (IOO).
7	RW	WO_OR	WO_CLEAR	UNUSED_7B: Unused.
8	RW	WO_OR	WO_CLEAR	UNUSED_8B: Unused.
9	RW	WO_OR	WO_CLEAR	UNUSED_9B: Unused.
10	RW	WO_OR	WO_CLEAR	UNUSED_10B: Unused.
11	RW	WO_OR	WO_CLEAR	UNUSED_11B: Unused.
12	RW	WO_OR	WO_CLEAR	UNUSED_12B: Unused.
13	RW	WO_OR	WO_CLEAR	UNUSED_13B: Unused.
14	RW	WO_OR	WO_CLEAR	UNUSED_14B: Unused.
15	RW	WO_OR	WO_CLEAR	RESERVED: Reserved.
16	RW	WO_OR	WO_CLEAR	TC_UNIT_MULTICYCLE_TEST_FENCE:
17	RW	WO_OR	WO_CLEAR	UNUSED_17B: Unused.
18	RW	WO_OR	WO_CLEAR	UNUSED_18B: Unused.
19	RW	WO_OR	WO_CLEAR	UNUSED_19B: Unused.
20	RW	WO_OR	WO_CLEAR	UNUSED_20B: Unused.
21	RW	WO_OR	WO_CLEAR	TC_PERV_MESH_CTRL:
22	RW	WO_OR	WO_CLEAR	UNUSED_22B: Unused.
23	RW	WO_OR	WO_CLEAR	UNUSED_23B: Unused.
24	RW	WO_OR	WO_CLEAR	UNUSED_24B: Unused.
25	RW	WO_OR	WO_CLEAR	UNUSED_25B: Unused.
26	RW	WO_OR	WO_CLEAR	UNUSED_26B: Unused.
27	RW	WO_OR	WO_CLEAR	UNUSED_27B: Unused.
28	RW	WO_OR	WO_CLEAR	UNUSED_28B: Unused.
29	RW	WO_OR	WO_CLEAR	UNUSED_29B: Unused.
30	RW	WO_OR	WO_CLEAR	UNUSED_30B: Unused.
31	RW	WO_OR	WO_CLEAR	UNUSED_31B: Unused.

Register Name	Chiplet Configuration Register 0
Mnemonic	TP.TCOB0.OB.CPLT_CONF0
Address	0000000009000008 (SCOM) 0000000009000018 (SCOM1) 0000000009000028 (SCOM2)
Description	This register contains the first set of vital chiplet configuration functions.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:5	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE0_SEL_DC: Probe 0 select.
6	RW	WO_OR	WO_CLEAR	RESERVED_6C: Reserved.
7	RW	WO_OR	WO_CLEAR	RESERVED_7C: Reserved.
8:13	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE1_SEL_DC: Probe 1 select.
14	RW	WO_OR	WO_CLEAR	RESERVED_14C: Reserved.
15	RW	WO_OR	WO_CLEAR	RESERVED_15C: Reserved.
16:21	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE2_SEL_DC: Probe 2 select.
22	RW	WO_OR	WO_CLEAR	RESERVED_22C: Reserved.
23	RW	WO_OR	WO_CLEAR	RESERVED_23C: Reserved.
24:29	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE3_SEL_DC: Probe 3 select.
30	RW	WO_OR	WO_CLEAR	RESERVED_30C: Reserved.
31	RW	WO_OR	WO_CLEAR	RESERVED_31C: Reserved.
32	RW	WO_OR	WO_CLEAR	CTRL_CC_OFLOW_FEH_SEL_DC: Enables ABIST overflow or failure indication.
33	RW	WO_OR	WO_CLEAR	CTRL_CC_SCAN_PROTECT_DC: Enables scan protection and the scan collision error mechanism.
34	RW	WO_OR	WO_CLEAR	CTRL_CC_SDIS_DC_N: Disables the scan diagnostic scan path.
35	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_35C: Reserved for test control.
36	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_36C: Reserved for test control.
37	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_37C: Reserved for test control.
38	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_38C: Reserved for test control.
39	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_39C: Reserved for test control.
40	RW	WO_OR	WO_CLEAR	CTRL_EPS_MASK_VITL_PCB_ERR_DC: Mask VITL PCB errors from CC or CPLT_CTRL.
41	RW	WO_OR	WO_CLEAR	CTRL_CC_MASK_VITL_SCAN_OPCG_ERR_DC: Mask VITL errors in CC, which are not PCB related.
42	RW	WO_OR	WO_CLEAR	RESERVED_42C: Reserved.
43	RW	WO_OR	WO_CLEAR	RESERVED_43C: Reserved.
44	RW	WO_OR	WO_CLEAR	FREE_USAGE_44C: Free usage.
45	RW	WO_OR	WO_CLEAR	FREE_USAGE_45C: Free usage.
46	RW	WO_OR	WO_CLEAR	FREE_USAGE_46C: Free usage.
47	RW	WO_OR	WO_CLEAR	FREE_USAGE_47C: Free usage.
48:51	RW	WO_OR	WO_CLEAR	TC_UNIT_GROUP_ID_DC: Group ID.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
52:54	RW	WO_OR	WO_CLEAR	TC_UNIT_CHIP_ID_DC: Chip ID.
55	RW	WO_OR	WO_CLEAR	RESERVED_ID_55C: Reserved ID.
56:60	RW	WO_OR	WO_CLEAR	TC_UNIT_SYS_ID_DC: SYS ID.
61	RW	WO_OR	WO_CLEAR	RESERVED_ID_61C: Reserved ID.
62	RW	WO_OR	WO_CLEAR	RESERVED_ID_62C: Reserved ID.
63	RW	WO_OR	WO_CLEAR	RESERVED_ID_63C: Reserved ID.

Register Name	Chiplet Configuration Register 1
Mnemonic	TP.TCOB0.OB.CPLT_CONF1
Address	0000000009000009 (SCOM) 0000000009000019 (SCOM1) 0000000009000029 (SCOM2)
Description	This register contains the second set of vital chiplet configuration functions.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_OR	WO_CLEAR	UNUSED_0D: Unused.
1	RW	WO_OR	WO_CLEAR	UNUSED_1D: Unused.
2	RW	WO_OR	WO_CLEAR	UNUSED_2D: Unused.
3	RW	WO_OR	WO_CLEAR	UNUSED_3D: Unused.
4	RW	WO_OR	WO_CLEAR	TC_PBIOO0_IOVALID:
5	RW	WO_OR	WO_CLEAR	TC_PBIOO1_IOVALID:
6	RW	WO_OR	WO_CLEAR	IOVALID_6D:
7	RW	WO_OR	WO_CLEAR	IOVALID_7D:
8	RW	WO_OR	WO_CLEAR	IOVALID_8D:
9	RW	WO_OR	WO_CLEAR	IOVALID_9D:
10	RW	WO_OR	WO_CLEAR	IOVALID_10D:
11	RW	WO_OR	WO_CLEAR	IOVALID_11D:
12	RW	WO_OR	WO_CLEAR	FREE_USAGE_12D: Free usage.
13	RW	WO_OR	WO_CLEAR	FREE_USAGE_13D: Free usage.
14	RW	WO_OR	WO_CLEAR	FREE_USAGE_14D: Free usage.
15	RW	WO_OR	WO_CLEAR	FREE_USAGE_15D: Free usage.
16:17	RW	WO_OR	WO_CLEAR	TC_OB_RATIO_DC:
18	RW	WO_OR	WO_CLEAR	FREE_USAGE_18D: Free usage.
19	RW	WO_OR	WO_CLEAR	FREE_USAGE_19D: Free usage.
20	RW	WO_OR	WO_CLEAR	FREE_USAGE_20D: Free usage.
21	RW	WO_OR	WO_CLEAR	FREE_USAGE_21D: Free usage.
22	RW	WO_OR	WO_CLEAR	FREE_USAGE_22D: Free usage.
23	RW	WO_OR	WO_CLEAR	FREE_USAGE_23D: Free usage.
24	RW	WO_OR	WO_CLEAR	FREE_USAGE_24D: Free usage.
25	RW	WO_OR	WO_CLEAR	FREE_USAGE_25D: Free usage.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
26	RW	WO_OR	WO_CLEAR	FREE_USAGE_26D: Free usage.
27	RW	WO_OR	WO_CLEAR	FREE_USAGE_27D: Free usage.
28	RW	WO_OR	WO_CLEAR	FREE_USAGE_28D: Free usage.
29	RW	WO_OR	WO_CLEAR	FREE_USAGE_29D: Free usage.
30	RW	WO_OR	WO_CLEAR	FREE_USAGE_30D: Free usage.
31	RW	WO_OR	WO_CLEAR	FREE_USAGE_31D: Free usage.

Register Name	Chiplet Status Register
Mnemonic	TP.TCOB0.OB.CPLT_STAT0
Address	0000000009000100 (SCOM)
Description	An interrupt is sent out on a bit change if not masked by the Chiplet Mask Register. A mask only masks the interrupt, not the status register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	SRAM_ABIST_DONE_DC: SRAM, eDRAM, and ABIST done.
1	ROX	DRAM_ABIST_DONE_DC: Unused in POWER9 DD1.
2	ROX	RESERVED_2E: Reserved.
3	ROX	RESERVED_3E: Reserved.
4	ROX	TC_DIAG_PORT0_OUT: Diagnostic output port.
5	ROX	TC_DIAG_PORT1_OUT: Diagnostic output port.
6	ROX	RESERVED_6E: Reserved.
7	ROX	PLL_DESTOUT: Reserved.
8	ROX	CC_CTRL_OPCG_DONE_DC: OPCG done. For LBIST, ABIST, or other OPCG runs.
9	ROX	CC_CTRL_CHIPLET_IS_ALIGNED_DC: Indicates that a chiplet is aligned.
10	ROX	FREE_USAGE_10E: Free usage.
11	ROX	FREE_USAGE_11E: Free usage.
12	ROX	FREE_USAGE_12E: Free usage.
13	ROX	FREE_USAGE_13E: Free usage.
14	ROX	FREE_USAGE_14E: Free usage.
15	ROX	FREE_USAGE_15E: Free usage.
16	ROX	FREE_USAGE_16E: Free usage.
17	ROX	FREE_USAGE_17E: Free usage.
18	ROX	FREE_USAGE_18E: Free usage.
19	ROX	FREE_USAGE_19E: Free usage.
20	ROX	FREE_USAGE_20E: Free usage.
21	ROX	FREE_USAGE_21E: Free usage.
22	ROX	FREE_USAGE_22E: Free usage.
23	ROX	FREE_USAGE_23E: Free usage.

Register Name	Chiplet Mask Register
Mnemonic	TP.TCOB0.OB.CPLT_MASK0
Address	0000000009000101 (SCOM)
Description	This register masks an interrupt when a bit changes in the Chiplet Status Register. It does not mask the status itself.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CPLTMASK0: Bitwise masking of the Chiplet Status Register.

Register Name	Control Protect Mode Register
Mnemonic	TP.TCOB0.OB.CTRL_PROTECT_MODE_REG
Address	00000000090003FE (SCOM)
Description	This register enables read and write protection.

Bits	SCOM	Field Mnemonic: Description
0	RW	CTRL_READ_PROTECT_ENABLE: Enables read protection.
1	RW	CTRL_WRITE_PROTECT_ENABLE: Enables write protection.

Register Name	Atomic Lock Register
Mnemonic	TP.TCOB0.OB.CTRL_ATOMIC_LOCK_REG
Address	00000000090003FF (SCOM)
Description	This register enables an atomic lock and an atomic lock counter.

Bits	SCOM	Field Mnemonic: Description
0	RW	CTRL_ATOMIC_LOCK_ENABLE: Enables atomic lock.
1:4	ROX	CTRL_ATOMIC_ID: Atomic ID.
5:7	RO	constant = 0b000
8:15	ROX	CTRL_ATOMIC_ACTIVITY: Atomic lock counter.

Register Name	PSCOMLE Mode Register
Mnemonic	TP.TCOB0.OB.EPS.PSC.PSC.PSCOM_MODE_REG
Address	0000000009010000 (SCOM)
Description	This is the parallel-to-serial communication light edition (PSCOMLE) mode register.

Bits	SCOM	Field Mnemonic: Description
0	RW	ABORT_ON_PCB_ADDR_PARITY_ERROR: Abort on PCB address parity error.
1	RW	ABORT_ON_PCB_WDATA_PARITY_ERROR: Abort on PCB write data parity error.
2	RW	ABORT_ON_DL_RETURN_P0_ERROR: Unused.
3	RW	ABORT_ON_DL_RETURN_WDATA_PARITY_ERROR: Abort on DL return write data parity error.
4	RW	WATCHDOG_ENABLE: Enable watchdog.

Bits	SCOM	Field Mnemonic: Description
5:6	RW	SCOM_HANG_LIMIT: 0b11 = 256 0b10 = 512 0b01 = 768 0b00 = 1023
7	RW	FORCE_ALL_RINGS: Set to a logical 1 if all rings should be enabled independent of the ring address.
8	RW	FSM_SELFRESET_ON_STATEVEC_PARITYERROR_ENABLE: FSM self reset on STATEVEC parity error enable.
9:11	RW	RESERVED_PSCOM_MODE_LT: Reserved.

Register Name	PSCOMLE Error Register
Mnemonic	TP.TCOB0.OB.EPS.PSC.PSC.PSCOM_STATUS_ERROR_REG
Address	0000000009010001 (SCOM)
Description	This is the parallel-to-serial communication light edition (PSCOMLE) error register.

Bits	SCOM	Field Mnemonic: Description
0	RWX	ACCUMULATED_PCB_WDATA_PARITY_ERROR: Accumulated PCB write data parity error.
1	RWX	ACCUMULATED_PCB_ADDRESS_PARITY_ERROR: Accumulated PCB address parity error.
2	RWX	ACCUMULATED_DL_RETURN_WDATA_PARITY_ERROR: Accumulated DL return write data parity error.
3	RWX	ACCUMULATED_DL_RETURN_P0_ERROR: Accumulated DL return P0 error.
4	RWX	ACCUMULATED_UL_RDATA_PARITY_ERROR: Accumulated UL read data parity error.
5	RWX	ACCUMULATED_UL_P0_ERROR: Accumulated UL P0 error.
6	RWX	ACCUMULATED_PARITY_ERROR_ON_INTERFACE_MACHINE: Accumulated parity error on interface machine.
7	RWX	ACCUMULATED_PARITY_ERROR_ON_P2S_MACHINE: Accumulated parity error on p2s machine.
8	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_ULCCH: Accumulated timeout while waiting for ULCCH.
9	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: Accumulated timeout while waiting for DLDCH return.
10	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_ULDCH: Accumulated timeout while waiting for ULDCH.
11	RWX	ACCUMULATED_PSCOM_PARALLEL_WRITE_NVLD: Accumulated PSCOM parallel write NVLD.
12	RWX	ACCUMULATED_PSCOM_PARALLEL_READ_NVLD: Accumulated PSCOM parallel read NVLD.
13	RWX	ACCUMULATED_PSCOM_PARALLEL_ADDR_INVALID: Accumulated PSCOM parallel address invalid.
14	RWX	ACCUMULATED_PCB_COMMAND_PARITY_ERROR: Accumulated PCB command parity error.
15	RWX	ACCUMULATED_GENERAL_TIMEOUT: Accumulated general timeout.
16	RWX	ACCUMULATED_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: Accumulated satellite acknowledge access violation.
17	RWX	ACCUMULATED_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: Accumulated satellite acknowledge invalid register.
18	RWX	TRAPPED_PCB_WDATA_PARITY_ERROR: Trapped PCB write data parity error.
19	RWX	TRAPPED_PCB_ADDRESS_PARITY_ERROR: Trapped PCB address parity error.
20	RWX	TRAPPED_DL_RETURN_WDATA_PARITY_ERROR: Trapped DL return write data parity error.

Bits	SCOM	Field Mnemonic: Description
21	RWX	TRAPPED_DL_RETURN_P0_ERROR: Trapped DL return P0 error.
22	RWX	TRAPPED_UL_RDATA_PARITY_ERROR: Trapped UL read data parity error.
23	RWX	TRAPPED_UL_P0_ERROR: Trapped UL P0 error.
24	RWX	TRAPPED_PARITY_ERROR_ON_INTERFACE_MACHINE: Trapped parity error on interface machine.
25	RWX	TRAPPED_PARITY_ERROR_ON_P2S_MACHINE: Trapped parity error on p2s machine.
26	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_ULCCH: Trapped timeout while waiting for ULCCH.
27	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: Trapped timeout while waiting for DLDCH return.
28	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_ULDCH: Trapped timeout while waiting for ULDCH.
29	RWX	TRAPPED_PSCOM_PARALLEL_WRITE_NVLD: Trapped PSCOM parallel write NVLD.
30	RWX	TRAPPED_PSCOM_PARALLEL_READ_NVLD: Trapped PSCOM parallel read NVLD.
31	RWX	TRAPPED_PSCOM_PARALLEL_ADDR_INVALID: Trapped PSCOM parallel address invalid.
32	RWX	TRAPPED_PCB_COMMAND_PARITY_ERROR: Trapped PCB command parity error.
33	RWX	TRAPPED_GENERAL_TIMEOUT: Trapped general timeout.
34	RWX	TRAPPED_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: Trapped satellite acknowledge access violation.
35	RWX	TRAPPED_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: Trapped satellite acknowledge invalid register.

Register Name	PSCOMLE Error Mask Register
Mnemonic	TP.TCOB0.OB.EPS.PSC.PSC.PSCOM_ERROR_MASK
Address	0000000009010002 (SCOM)
Description	This is the parallel-to-serial communication light edition (PSCOMLE) error mask register.

Bits	SCOM	Field Mnemonic: Description
0	RW	MASK_PCB_WDATA_PARITY_ERROR: Mask PCB write data parity error.
1	RW	MASK_PCB_ADDRESS_PARITY_ERROR: Mask PCB address parity error.
2	RW	MASK_DL_RETURN_WDATA_PARITY_ERROR: Mask DL return write data parity error.
3	RW	MASK_DL_RETURN_P0_ERROR: Mask DL return P0 error.
4	RW	MASK_UL_RDATA_PARITY_ERROR: Mask UL read data parity error.
5	RW	MASK_UL_P0_ERROR: Mask UL P0 error.
6	RW	MASK_PARITY_ERROR_ON_INTERFACE_MACHINE: Mask parity error on interface machine.
7	RW	MASK_PARITY_ERROR_ON_P2S_MACHINE: Mask parity error on p2s machine.
8	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_ULCCH: Mask timeout while waiting for ULCCH.
9	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: Mask timeout while waiting for DLDCH return.
10	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_ULDCH: Mask timeout while waiting for ULDCH.
11	RW	MASK_PSCOM_PARALLEL_WRITE_NVLD: Mask PSCOM parallel write NVLD.
12	RW	MASK_PSCOM_PARALLEL_READ_NVLD: Mask PSCOM parallel read NVLD.
13	RW	MASK_PSCOM_PARALLEL_ADDR_INVALID: Mask PSCOM parallel address invalid.
14	RW	MASK_PCB_COMMAND_PARITY_ERROR: Mask PCB command parity error.

Bits	SCOM	Field Mnemonic: Description
15	RW	MASK_GENERAL_TIMEOUT: Mask general timeout.
16	RW	MASK_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: Mask satellite acknowledge access violation.
17	RW	MASK_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: Mask satellite acknowledge invalid register.

Register Name	PSCOMLE Address Trap Register
Mnemonic	TP.TCOB0.OB.EPS.PSC.PSC.ADDR_TRAP_REG
Address	0000000009010003 (SCOM)
Description	This is the parallel-to-serial communication light edition (PSCOMLE) address trap register.

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	PCB_ADDRESS_OF_LAST_TRANSACTION_WITH_ERROR: PCB address of the last transaction with an error.
16	ROX	PCB_READ_NOTWRITE_OF_LAST_TRANSACTION_WITH_ERROR: PCB read, not write, of the last transaction with an error.
17	ROX	RESERVED_ADDR_LAST_TRAP_LT: Reserved_0.
18:30	ROX	SERIAL2PARALLEL_STATE_MACHINE_AT_TIME_OF_ERROR: Serial2 parallel state machine at the time of the error.
31	ROX	SATELLITE_ACKNOWLEDGE_BIT_RETURN_PARITY: This bit is set to 1 if no parity error is detected in the satellite number or acknowledgment bits.
32	ROX	SATELLITE_ACKNOWLEDGE_BIT_WRITE_PARITY_ERROR: Set if a write parity error is detected by the satellite.
33	ROX	SATELLITE_ACKNOWLEDGE_BIT_ACCESS_VIOLATION: Set if an invalid read or write access is detected by the satellite.
34	ROX	SATELLITE_ACKNOWLEDGE_BIT_INVALID_REGISTER: Set if an invalid register address is detected by the satellite.

Register Name	Ring Lock Enable Register
Mnemonic	TP.TCOB0.OB.EPS.PSC.PSC.WRITE_PROTECT_ENABLE_REG
Address	0000000009010005 (SCOM)
Description	This register enables the ring lock.

Bits	SCOM	Field Mnemonic: Description
0	RW	ENABLE_RING_LOCKING: General enable of ring locking upon write to a specific ring.
1	RW	RESERVED_RING_LOCKING: Reserved.

Register Name	Write Protect Rings Register
Mnemonic	TP.TCOB0.OB.EPS.PSC.PSC.WRITE_PROTECT_RINGS_REG
Address	0000000009010006 (SCOM)
Description	This register writes ring protect bit maps.

Bits	SCOM	Field Mnemonic: Description
0:15	RW	WRITE_PROTECT_RINGS: Write a protect bit map for each ring.

Register Name	Atomic Lock Mask Register
Mnemonic	TP.TCOB0.OB.EPS.PSC.PSC.ATOMIC_LOCK_MASK_LATCH_REG
Address	0000000009010007 (SCOM)
Description	This register provides a bit mask for atomic locking.

Bits	SCOM	Field Mnemonic: Description
0:15	RW	ATOMIC_LOCK_MASK: A bit mask for atomic locking on a ring-by-ring basis.

Register Name	Ring Fence Enable Mask Register
Mnemonic	TP.TCOB0.OB.EPS.PSC.PSC.RING_FENCE_MASK_LATCH_REG
Address	0000000009010008 (SCOM)
Description	This register provides a bit mask for ring fencing.

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:15	RW	RING_FENCE_ENABLE_MASK: Enable bit mask for ring fencing on a ring-by-ring basis.

Register Name	Trace Array High Data Register
Mnemonic	TP.TCOB0.OB.TRA0.TR0.TRACE_HI_DATA_REG
Address	0000000009010400 (SCOM)
Description	This register provides the high trace array data.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace array data 0:63.

Register Name	Trace Array Low Data Register
Mnemonic	TP.TCOB0.OB.TRA0.TR0.TRACE_LO_DATA_REG
Address	0000000009010401 (SCOM)
Description	This register provides the low trace array data.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace array data 64:95.
32:41	ROX	TRACE_ADDRESS: Trace address.
42:50	ROX	TRACE_LAST_BANK: Trace last bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace last valid bank.
52	ROX	TRACE_WRITE_ON_RUN: Trace write-on-run indicator.
53	ROX	TRACE_RUNNING: Trace run indicator.
54:63	ROX	TRACE_HOLD_ADDRESS: Trace hold address (pointing to last entry).

Register Name	Trace Control Configuration Register
Mnemonic	TP.TCOB0.OB.TRA0.TR0.TRACE_TRCTRL_CONFIG
Address	0000000009010402 (SCOM)
Description	This register contains trace control configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	STORE_ON_TRIG_MODE: Enable store on trigger mode.
1	RW	WRITE_ON_RUN_MODE: Enable unconditional forced write when trace runs.
2:9	RW	EXTEND_TRIG_MODE: Counter value for extended trigger mode.
10	RW	BANK_MODE: Enable bank mode.
11	RW	ENH_TRACE_MODE: Enable enhanced trace mode.
12	RW	LOCAL_CLOCK_GATE_CONTROL: When this bit is set, internal clock gating is disabled. The trace control logic and the trace data pipeline are always clocked.
13	RW	UNUSED_13B: Unused.
14:17	RW	TRACE_SELCT_CONTROL: Selector for two sets of external trace bus multiplexers, tra_mux0_sel(0:1) and tra_mux1_sel(0:1).
18:21	RW	SPARE_CONTROL: Spare control bits.

Register Name	Trace Data Configuration Register 0
Mnemonic	TP.TCOB0.OB.TRA0.TR0.TRACE_TRDATA_CONFIG_0
Address	0000000009010403 (SCOM)
Description	This register contains a trace data compare mask for bits 0 – 63.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: Trace data compare mask for bits 0 to 63.

Register Name	Trace Data Configuration Register 1
Mnemonic	TP.TCOB0.OB.TRA0.TR0.TRACE_TRDATA_CONFIG_1
Address	0000000009010404 (SCOM)
Description	This register contains a trace data compare mask for bits 64 – 87.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: Trace data compare mask for bits 64 to 87.

Register Name	Trace Data Configuration Register 2
Mnemonic	TP.TCOB0.OB.TRA0.TR0.TRACE_TRDATA_CONFIG_2
Address	0000000009010405 (SCOM)
Description	This register contains patterns A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: pattern_match_pata_0_to_23.

Bits	SCOM	Field Mnemonic: Description
24:47	RW	PATTERNB: pattern_match_patb_0_to_23.

Register Name	Trace Data Configuration Register 3
Mnemonic	TP.TCOB0.OB.TRA0.TR0.TRACE_TRDATA_CONFIG_3
Address	0000000009010406 (SCOM)
Description	This register contains patterns C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNC: pattern_match_patc_0_to_23.
24:47	RW	PATTERND: pattern_match_patd_0_to_23.

Register Name	Trace Data Configuration Register 4
Mnemonic	TP.TCOB0.OB.TRA0.TR0.TRACE_TRDATA_CONFIG_4
Address	0000000009010407 (SCOM)
Description	This register contains masks A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: mska.
24:47	RW	MASKB: mskb.

Register Name	Trace Data Configuration Register 5
Mnemonic	TP.TCOB0.OB.TRA0.TR0.TRACE_TRDATA_CONFIG_5
Address	0000000009010408 (SCOM)
Description	This register contains masks C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: mskc.
24:47	RW	MASKD: mskd.

Register Name	Trace Data Configuration Register 9
Mnemonic	TP.TCOB0.OB.TRA0.TR0.TRACE_TRDATA_CONFIG_9
Address	0000000009010409 (SCOM)
Description	This register contains trace data configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disable trace data compression (store data every cycle).
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Take into account changes in the error bit for trace data compression (default = 0).

Bits	SCOM	Field Mnemonic: Description
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.
10:13	RW	TRIG0_OR_MASK: The OR of all selected MATCHes is ORed with result of TRIG0_AND. 0b1xxx selects MATCHA OR 0bx1xx selects MATCHB OR 0bxx1x selects MATCHC OR 0bxxx1 selects MATCHD OR 0b0000 selects to not OR any MATCHes.
14:17	RW	TRIG0_AND_MASK: The AND of following selected MATCHes is ORed with result of TRIG0_OR. 0b1xxx selects MATCHA AND 0bx1xx selects MATCHB AND 0bxx1x selects MATCHC AND 0bxxx1 selects MATCHD AND 0b0000 selects to not AND any MATCHes together to form TRIG0.
18:21	RW	TRIG1_OR_MASK: The OR of all selected MATCHes is ORed with result of TRIG1_AND. 0b1xxx selects MATCHA OR 0bx1xx selects MATCHB OR 0bxx1x selects MATCHC OR 0bxxx1 selects MATCHD OR 0b0000 selects to not OR any MATCHes to form TRIG1.
22:25	RW	TRIG1_AND_MASK: The AND of following selected MATCHes is ORed with result of TRIG1_OR. 0b1xxx selects MATCHA AND 0bx1xx selects MATCHB AND 0bxx1x selects MATCHC AND 0bxxx1 selects MATCHD AND 0b0000 selects to not AND any MATCHes together to form TRIG1.
26	RW	TRIG0_NOT_MODE: Invert TRIG0 before using it.
27	RW	TRIG1_NOT_MODE: Invert TRIG1 before using it.
28:31	RW	MATCH_NOT_MODE: Invert the match polarity before using it to form a trigger. 0b1000 inverts MATCHA. 0b0100 inverts MATCHB. 0b0010 inverts MATCHC. 0b0001 inverts MATCHD.
32:35	RW	Reserved field.
36	RW	DD1_STRETCH_TRIGGER_PULSES: (DD1 workaround.) Stretch trigger output pulses to two clocks. Must be enabled for MCFAST and L2FAST traces.

Bits	SCOM	Field Mnemonic: Description
37	RW	Reserved field.

Register Name	Debug Mode Register
Mnemonic	TP.TCOB0.OB.EPS.DBG.DBG_MODE_REG
Address	00000000090107C0 (SCOM)
Description	This is debug macro configuration register 0 for the configuration component.

Bits	SCOM	Field Mnemonic: Description
0:2	RW	GLB_BRCST_MODE: Global broadcast mode (0 to 2): 100 = dbg_trace_run and dbg_trace_freeze. 101 = pc_tcdbg_trace_run_fncd and dbg_trace_freeze. 110 = dbg_triggers_out(0 to 1). 111 = pc_tcdbg_triggers(0 to 1) (from core).
3:5	RW	TRACE_SEL_MODE: Select source for trace_run and bank. 001 = Core trace run and bank. 010 = TP broadcast run and 0. 011 = tc_dbg_inter_brcst latched. 100 = tc_dbg_dbg_sync_brcst_rcv. else = dbg_trace_run and dbg_trace_bank.
6:7	RW	TRIG_SEL_MODE: Select source for tcdbg_trigger(0). 10 = Global broadcast. 11 = pc_tcdbg_trigger (from core). else = dbg_triggers_out(0:1).
8	RW	STOP_ON_XSTOP_SELECTION: Enable trace stop on checkstop.
9	RW	STOP_ON_RECOV_ERR_SELECTION: Enable trace stop on recoverable error.
10	RW	STOP_ON_SPATTN_SELECTION: Enable trace stop on special attention.
11	RW	FREEZE_SEL_MODE: Select freeze source: 0 = Local debug freeze. 1 = Via broadcast: tp_tcdbg_glb_brcst(1).
12:13	RW	SYNC_BRCST_MODE: Originally used for synchronous broadcast mode, but now obsolete. See trace_sel_mode.
14	RO	constant = 0b0
15	RO	constant = 0b0
16:31	ROX	dbg_status. Debug status.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	Debug Instance 1 Condition 1 Register
Mnemonic	TP.TCOB0.OB.EPS.DBG.DBG_INST1_COND_REG_1
Address	00000000090107C1 (SCOM)
Description	This is debug macro configuration register 1 for front-end component 1.

Bits	SCOM	Field Mnemonic: Description
0:7	RW	INST1_COND1_SEL_A: Multiplexer for cond1_trig_in(0). 000 = Select constant 0 001 = Select constant 1 -- CONDITION FEEDBACK --

Bits	SCOM	Field Mnemonic: Description
		002 = Select inst1_dbg_cond1. 003 = Select inst1_dbg_cond2. 004 = Select inst1_dbg_cond3. 005 = Select inst1_dbg_cond2timeout. 006 = Select inst2_dbg_cond1. 007 = Select inst2_dbg_cond2. 008 = Select inst2_dbg_cond3. 009 = Select inst2_dbg_cond2timeout. 010 = Select inst3_dbg_cond1 - unused, tied down. 011 = Select inst3_dbg_cond2 - unused, tied down. 012 = Select inst3_dbg_cond3 - unused, tied down. 013 = Select inst3_dbg_cond2timeout - unused, tied down. 014 = Select inst4_dbg_cond1 - unused, tied down. 015 = Select inst4_dbg_cond2 - unused, tied down. 016 = Select inst4_dbg_cond3 - unused, tied down. 017 = Select inst4_dbg_cond2timeout - unused, tied down. 018 = Select inst1_dbg_trig_sp. 019 = Select inst2_dbg_trig_sp. 020 = Select inst3_dbg_trig_sp - unused, tied down. 021 = Select inst4_dbg_trig_sp - unused, tied down. 022 = Select tctrc_tcdbg_trigger_a(0). 023 = Select tctrc_tcdbg_trigger_b(0). 024 = Select tctrc_tcdbg_trigger_a(0) and tctrc_tcdbg_trigger_b(0). 025 = Select tctrc_tcdbg_trigger_a(1). 026 = Select tctrc_tcdbg_trigger_b(1). 027 = Select tctrc_tcdbg_trigger_a(1) and tctrc_tcdbg_trigger_b(1). 028 = Select tctrc_tcdbg_trigger_a(2). 029 = Select tctrc_tcdbg_trigger_b(2). 030 = Select tctrc_tcdbg_trigger_a(2) and tctrc_tcdbg_trigger_b(2). 031 = Select tctrc_tcdbg_trigger_a(3). 032 = Select tctrc_tcdbg_trigger_b(3). 033 = Select tctrc_tcdbg_trigger_a(3) and tctrc_tcdbg_trigger_b(3). 034 = Select tctrc_tcdbg_trigger_a(4). 035 = Select tctrc_tcdbg_trigger_b(4). 036 = Select tctrc_tcdbg_trigger_a(4) and tctrc_tcdbg_trigger_b(4). 037 = Select tctrc_tcdbg_trigger_a(5). 038 = Select tctrc_tcdbg_trigger_b(5). 039 = Select tctrc_tcdbg_trigger_a(5) and tctrc_tcdbg_trigger_b(5). 040 = Select tctrc_tcdbg_trigger_a(6). 041 = Select tctrc_tcdbg_trigger_b(6). 042 = Select tctrc_tcdbg_trigger_a(6) and tctrc_tcdbg_trigger_b(6). 043 = Select tctrc_tcdbg_trigger_a(7). 044 = Select tctrc_tcdbg_trigger_b(7). 045 = Select tctrc_tcdbg_trigger_a(7) and tctrc_tcdbg_trigger_b(7). 046 = Select tctrc_tcdbg_trigger_a(8). 047 = Select tctrc_tcdbg_trigger_b(8). 048 = Select tctrc_tcdbg_trigger_a(8) and tctrc_tcdbg_trigger_b(8). 049 = Select tctrc_tcdbg_trigger_a(9). 050 = Select tctrc_tcdbg_trigger_b(9). 051 = Select tctrc_tcdbg_trigger_a(9) and tctrc_tcdbg_trigger_b(9). 052 = Select tctrc_tcdbg_trigger_a(10). 053 = Select tctrc_tcdbg_trigger_b(10). 054 = Select tctrc_tcdbg_trigger_a(10) and tctrc_tcdbg_trigger_b(10). 055 = Select tctrc_tcdbg_trigger_a(11). 056 = Select tctrc_tcdbg_trigger_b(11). 057 = Select tctrc_tcdbg_trigger_a(11) and tctrc_tcdbg_trigger_b(11). 058 = Select tctrc_tcdbg_trigger_a(12). 059 = Select tctrc_tcdbg_trigger_b(12). 060 = Select tctrc_tcdbg_trigger_a(12) and tctrc_tcdbg_trigger_b(12). 061 = Select tctrc_tcdbg_trigger_a(13). 062 = Select tctrc_tcdbg_trigger_b(13).

Bits	SCOM	Field Mnemonic: Description
		063 = Select tctrc_tcdbg_trigger_a(13) and tctrc_tcdbg_trigger_b(13). 064 = Select tctrc_tcdbg_trigger_a(14). 065 = Select tctrc_tcdbg_trigger_b(14). 066 = Select tctrc_tcdbg_trigger_a(14) and tctrc_tcdbg_trigger_b(14). 067 = Select tctrc_tcdbg_trigger_a(15). 068 = Select tctrc_tcdbg_trigger_b(15). 069 = Select tctrc_tcdbg_trigger_a(15) and tctrc_tcdbg_trigger_b(15). 070 = Select tctrc_tcdbg_trigger_a(16). 071 = Select tctrc_tcdbg_trigger_b(16). 072 = Select tctrc_tcdbg_trigger_a(16) and tctrc_tcdbg_trigger_b(16). 073 = Select tctrc_tcdbg_trigger_a(17). 074 = Select tctrc_tcdbg_trigger_b(17). 075 = Select tctrc_tcdbg_trigger_a(17) and tctrc_tcdbg_trigger_b(17). -- LOGIC (UNIT) TRIGGERS -- EP: 0:3 L3C0, 4:7 L3C1, 8:9 GX, 10 TP (hang), 11 spare, 12:13 MCA, 14:15 spare. ES: 0:4 L4C, 5:6 L4F, 7:8 TPTOD, 9 TP (hang), 10:15 spare. 076 = Select logic_trigger_in(0). 077 = Select logic_trigger_in(1). 078 = Select logic_trigger_in(2). 079 = Select logic_trigger_in(3). 080 = Select logic_trigger_in(4). 081 = Select logic_trigger_in(5). 082 = Select logic_trigger_in(6). 083 = Select logic_trigger_in(7). 084 = Select logic_trigger_in(8). 085 = Select logic_trigger_in(9). 086 = Select logic_trigger_in(10). 087 = Select logic_trigger_in(11). 088 = Select logic_trigger_in(12). 089 = Select logic_trigger_in(13). 090 = Select logic_trigger_in(14). 091 = Select logic_trigger_in(15). 092 = Select pc_tcdbg_trigger(0). 093 = Select pc_tcdbg_trigger(1). 094 = Select tctrc_tcdbg_glb_brcst(0). 095 = Select tctrc_tcdbg_glb_brcst(1). 096 = Select xstop_err. 097 = Select recov_err. 098 = Select spattn. 099 = Select fir_dbg_local_xstop_err. 100 = Select tc_dbg_inter_brcst(0). 101 = Select tc_dbg_inter_brcst(1). -- CORE TRIGGERS (EP chip only) -- **Note:** Set core_slave_mode to honor ec[0:5]_tc_trace_run. 102 = Select core trigger 0: any rising edge of ec[0:5]_tc_trace_run(0). 103 = Select core trigger 1: any rising edge of ec[0:5]_tc_trace_run(1). 104 = Select core trigger 2: any falling edge of ec[0:5]_tc_trace_run(0). 105 = Select core trigger 3: any falling edge of ec[0:5]_tc_trace_run(1). 106 = Select glb_trig_or_trace_in(0). 107 = Select glb_trig_or_trace_in(1). 108 = Select core_local_brcst_trc(0). 109 = Select core_local_brcst_trc(1). 110 = Select glb_freeze_brcst_rec(0). 111 = Select trig_2_extern_in(0). 112 = Select trig_2_extern_in(1). 113 = Select dbg_triggers_out(2). 114 = Select dbg_triggers_out(3). 115 = Select dbg_triggers_out(4). 116 = Select dbg_triggers_out(5). 117 = Select dbg_triggers_out(6). 118 = Select tcdbg_trigger_in(0).

Bits	SCOM	Field Mnemonic: Description
		119 = Select tcdbg_trigger_in(1).
8:15	RW	INST1_COND1_SEL_B: Multiplexer for cond1_trig_in(1). Selection as cond1_trig_in(0).
16:23	RW	INST1_COND2_SEL_A: Multiplexer for cond2_trig_in(0). Selection as cond1_trig_in(0).
24:31	RW	INST1_COND2_SEL_B: Multiplexer for cond2_trig_in(1). Selection as cond1_trig_in(0).
32	RW	INST1_C1_INAROW_MODE: Front end instance 1 counter 1 in-a-row mode.
33	RW	INST1_AND_TRIGGER_MODE1: Front end instance 1 and trigger mode condition1.
34	RW	INST1_NOT_TRIGGER_MODE1: Front end instance 1 inverted trigger mode condition1.
35	RW	INST1_EDGE_TRIGGER_MODE1: Front end instance 1 edge trigger mode condition1.
36:38	RWX	INST1_UNUSED_1: Unused.
39	RW	INST1_C2_INAROW_MODE: Front end instance 1 counter 2 in-a-row mode.
40	RW	INST1_AND_TRIGGER_MODE2: Front end instance 1 and trigger mode2.
41	RW	INST1_NOT_TRIGGER_MODE2: Front end instance 1 inverted (not) trigger.
42	RW	INST1_EDGE_TRIGGER_MODE2: Front end instance 1edge trigger.
43:45	RWX	INST1_UNUSED_2: Unused.
46	RW	INST1_COND3_ENABLE_RESET: Front end instance 1 condition 3 enable.
47	RW	INST1_EXACT_TO_MODE: Front end instance 1 exact timeout mode.
48	RW	INST1_RESET_C2TIMER_ON_C1: Front end instance 1 reset condition 2 timer on condition1.
49	RW	INST1_RESET_C3_ON_C0: Front end instance 1 reset condition3 on condition0.
50	RW	INST1_SLOW_TO_MODE: Front end instance 1 slow timeout mode.
51	RW	INST1_EXACT_RESET_C3_ON_TO: Front end instance 1 exact reset condition3 on timeout.
52:55	RW	INST1_C1_COUNT_LT: inst1 condition1 counter compare value.
56:59	RW	INST1_C2_COUNT_LT: inst1 condition2 counter compare value.
60:62	RW	INST1_RESET_C3_SELECT: Front end instance 1 reset condition3 for reset_c3_on_c0. 0B100 = dbg_cross_couple_triggers(4). 0B101 = dbg_cross_couple_triggers(12). 0B110 = dbg_cross_couple_triggers(20). 0B111 = dbg_cross_couple_triggers(28).

Register Name	**Debug Instance 1 Condition 2 Register**
Mnemonic	TP.TCOB0.OB.EPS.DBG.DBG_INST1_COND_REG_2
Address	00000000090107C2 (SCOM)
Description	This is debug macro configuration register 2 for front-end component 1.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	INST1_CROSS_COUPLE_SELECT_1_A: Cross coupling is the same for all selectors: 00000 = Selects inst1_cond1_trig_a. 00001 = Selects inst1_cond1_trig_b. 00010 = Selects inst1_cond2_trig_a. 00011 = Selects inst1_cond2_trig_b. 00100 = Selects inst1_condition1. 00101 = Selects inst1_condition2. 00110 = Selects inst1_condition3. 00111 = Selects inst1_cond2_timeout. 01000 = Selects inst2_cond1_trig_a.

Bits	SCOM	Field Mnemonic: Description
		01001 = Selects inst2_cond1_trig_b. 01010 = Selects inst2_cond2_trig_a. 01011 = Selects inst2_cond2_trig_b. 01100 = Selects inst2_condition1. 01101 = Selects inst2_condition2. 01110 = Selects inst2_condition3. 01111 = Selects inst2_cond2_timeout. 10000 = Selects inst3_cond1_trig_a. 10001 = Selects inst3_cond1_trig_b. 10010 = Selects inst3_cond2_trig_a. 10011 = Selects inst3_cond2_trig_b. 10100 = Selects inst3_condition1. 10101 = Selects inst3_condition2. 10110 = Selects inst3_condition3. 10111 = Selects inst3_cond2_timeout. 11000 = Selects inst4_cond1_trig_a. 11001 = Selects inst4_cond1_trig_b. 11010 = Selects inst4_cond2_trig_a. 11011 = Selects inst4_cond2_trig_b. 11100 = Selects inst4_condition1. 11101 = Selects inst4_condition2. 11110 = Selects inst4_condition3. 11111 = Selects inst4_cond2_timeout.
5:9	RW	INST1_CROSS_COUPLE_SELECT_1_B: inst1 cross couple select 1b.
10:14	RW	INST1_CROSS_COUPLE_SELECT_2_A: inst1 cross couple select 2a.
15:19	RW	INST1_CROSS_COUPLE_SELECT_2_B: inst1 cross couple select 2b.
20:43	RW	INST1_TO_CMP_LT: Compare value for special counter sp_cnt_lt in debug component 1.
44	RW	INST1_FORCE_TEST_MODE: Force test mode to compare without an actual compare.

Register Name	Debug Instance 1 Condition 3 Register
Mnemonic	TP.TCOB0.OB.EPS.DBG.DBG_INST1_COND_REG_3
Address	00000000090107C3 (SCOM)
Description	This is debug macro configuration register 2 for the front-end 1 component.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	INST1_SP_COUNT_LT: Timeout counter to compare value for dbg_cond_comp_1.

Register Name	Debug Instance 2 Condition 1 Register
Mnemonic	TP.TCOB0.OB.EPS.DBG.DBG_INST2_COND_REG_1
Address	00000000090107C4 (SCOM)
Description	This is debug macro configuration register 1 for the front-end 1 component.

Bits	SCOM	Field Mnemonic: Description
0:7	RW	INST2_COND1_SEL_A: Multiplexer for cond1_trig_in(0). 000 = Selects constant 0 001 = Selects constant 1 -- CONDITION FEEDBACK -- 002 = Selects inst2_dbg_cond1. 003 = Selects inst2_dbg_cond2.

Bits	SCOM	Field Mnemonic: Description
		004 = Selects inst2_dbg_cond3. 005 = Selects inst2_dbg_cond2timeout. 006 = Selects inst2_dbg_cond1. 007 = Selects inst2_dbg_cond2. 008 = Selects inst2_dbg_cond3. 009 = Selects inst2_dbg_cond2timeout. 010 = Selects inst3_dbg_cond1 - unused, tied down. 011 = Selects inst3_dbg_cond2 - unused, tied down. 012 = Selects inst3_dbg_cond3 - unused, tied down. 013 = Selects inst3_dbg_cond2timeout - unused, tied down. 014 = Selects inst4_dbg_cond1 - unused, tied down. 015 = Selects inst4_dbg_cond2 - unused, tied down. 016 = Selects inst4_dbg_cond3 - unused, tied down. 017 = Selects inst4_dbg_cond2timeout - unused, tied down. 018 = Selects inst2_dbg_trig_sp. 019 = Selects inst2_dbg_trig_sp. 020 = Selects inst3_dbg_trig_sp - unused, tied down. 021 = Selects inst4_dbg_trig_sp - unused, tied down. 022 = Selects tctrc_tcdbg_trigger_a(0). 023 = Selects tctrc_tcdbg_trigger_b(0). 024 = Selects tctrc_tcdbg_trigger_a(0) and tctrc_tcdbg_trigger_b(0). 025 = Selects tctrc_tcdbg_trigger_a(1). 026 = Selects tctrc_tcdbg_trigger_b(1). 027 = Selects tctrc_tcdbg_trigger_a(1) and tctrc_tcdbg_trigger_b(1). 028 = Selects tctrc_tcdbg_trigger_a(2). 029 = Selects tctrc_tcdbg_trigger_b(2). 030 = Selects tctrc_tcdbg_trigger_a(2) and tctrc_tcdbg_trigger_b(2). 031 = Selects tctrc_tcdbg_trigger_a(3). 032 = Selects tctrc_tcdbg_trigger_b(3). 033 = Selects tctrc_tcdbg_trigger_a(3) and tctrc_tcdbg_trigger_b(3). 034 = Selects tctrc_tcdbg_trigger_a(4). 035 = Selects tctrc_tcdbg_trigger_b(4). 026 = Selects tctrc_tcdbg_trigger_a(4) and tctrc_tcdbg_trigger_b(4). 027 = Selects tctrc_tcdbg_trigger_a(5). 028 = Selects tctrc_tcdbg_trigger_b(5). 029 = Selects tctrc_tcdbg_trigger_a(5) and tctrc_tcdbg_trigger_b(5). 030 = Selects tctrc_tcdbg_trigger_a(6). 031 = Selects tctrc_tcdbg_trigger_b(6). 032 = Selects tctrc_tcdbg_trigger_a(6) and tctrc_tcdbg_trigger_b(6). 033 = Selects tctrc_tcdbg_trigger_a(7). 034 = Selects tctrc_tcdbg_trigger_b(7). 035 = Selects tctrc_tcdbg_trigger_a(7) and tctrc_tcdbg_trigger_b(7). 036 = Selects tctrc_tcdbg_trigger_a(8). 037 = Selects tctrc_tcdbg_trigger_b(8). 038 = Selects tctrc_tcdbg_trigger_a(8) and tctrc_tcdbg_trigger_b(8). 039 = Selects tctrc_tcdbg_trigger_a(9). 040 = Selects tctrc_tcdbg_trigger_b(9). 041 = Selects tctrc_tcdbg_trigger_a(9) and tctrc_tcdbg_trigger_b(9). 042 = Selects xstop_err. 043 = Selects recov_err. 044 = Selects spattn. 045 = Selects fir_dbg_local_xstop_err. 046 = Selects tc_dbg_inter_brcst(0). 047 = Selects tc_dbg_inter_brcst(1). -- LOGIC (UNIT) TRIGGERS -- EP: 0:3 L3C0, 4:7 L3C1, 8:9 GX, 10 TP (hang), 11 spare, 12:13 MCA, 14:15 spare. ES: 0:4 L4C, 5:6 L4F, 7:8 TPTOD, 9 TP (hang), 10:15 spare. 102 = Selects logic_trigger_in(0). 103 = Selects logic_trigger_in(1). 104 = Selects logic_trigger_in(2). 105 = Selects logic_trigger_in(3).

Bits	SCOM	Field Mnemonic: Description
		106 = Selects logic_trigger_in(4). 107 = Selects logic_trigger_in(5). 108 = Selects logic_trigger_in(6). 109 = Selects logic_trigger_in(7). 110 = Selects logic_trigger_in(8). 111 = Selects logic_trigger_in(9). 112 = Selects logic_trigger_in(10). 113 = Selects logic_trigger_in(11). 114 = Selects logic_trigger_in(12). 115 = Selects logic_trigger_in(13). 116 = Selects logic_trigger_in(14). 117 = Selects logic_trigger_in(15). -- CORE TRIGGERS (EP chip only) -- **Note:** Set core_slave_mode to honor ec[0:5]_tc_trace_run. 118 = Selects core trigger 0: any rising edge of ec[0:5]_tc_trace_run(0). 119 = Selects core trigger 1: any rising edge of ec[0:5]_tc_trace_run(1). 120 = Selects core trigger 2: any falling edge of ec[0:5]_tc_trace_run(0). 121 = Selects core trigger 3: any falling edge of ec[0:5]_tc_trace_run(1). -- BROADCAST / ERRORS. 122 = Selects glb_trc_bdcst_recv (received global broadcast). 123 = Selects edge detected fir_dbg_xstop_err. 124 = Selects edge detected fir_dbg_recov_err. 125 = Selects edge detected fir_dbg_spatn. 126 ... 127 = Selects constant 0 (unused)
8:15	RW	INST2_COND1_SEL_B: Multiplexer for cond1_trig_in(1). Selection as cond1_trig_in(0).
16:23	RW	INST2_COND2_SEL_A: Multiplexer for cond2_trig_in(0). Selection as cond1_trig_in(0).
24:31	RW	INST2_COND2_SEL_B: Multiplexer for cond2_trig_in(1). Selection as cond1_trig_in(0).
32	RW	INST2_C1_INAROW_MODE: front end instance 1 c1_inarow_mode.
33	RW	INST2_AND_TRIGGER_MODE1: front end instance 1 and trigger mode condition1.
34	RW	INST2_NOT_TRIGGER_MODE1: front end instance 1 inverted trigger mode condition1.
35	RW	INST2_EDGE_TRIGGER_MODE1: front end instance 1 edge trigger mode condition1.
36:38	RWX	INST2_UNUSED_1: Unused.
39	RW	INST2_C2_INAROW_MODE: front end instance 1 Counter 2 in-a-rwo mode.
40	RW	INST2_AND_TRIGGER_MODE2: front end instance 1 and trigger mode2.
41	RW	INST2_NOT_TRIGGER_MODE2: front end instance 1 inverted (not) trigger.
42	RW	INST2_EDGE_TRIGGER_MODE2: front end instance 1edge trigger.
43:45	RWX	INST2_UNUSED_2: Unused.
46	RW	INST2_COND3_ENABLE_RESET: front end instance 1 condition3 enable.
47	RW	INST2_EXACT_TO_MODE: front end instance 1 exact timeout mode.
48	RW	INST2_RESET_C2TIMER_ON_C1: front end instance 1 reset condition2 timer on condition1.
49	RW	INST2_RESET_C3_ON_C0: front end instance 1 reset condition3 on condition0.
50	RW	INST2_SLOW_TO_MODE: front end instance 1 slow timeout mode.
51	RW	INST2_EXACT_RESET_C3_ON_TO: front end instance 1 exact reset condition3 on timeout.
52:55	RW	INST2_C1_COUNT_LT: inst2 condition1 counter compare value.
56:59	RW	INST2_C2_COUNT_LT: inst2 condition2 counter compare value.

Bits	SCOM	Field Mnemonic: Description
60:62	RW	INST2_RESET_C3_SELECT: front end instance 1: Reset condition3 for reset_c3_on_c0. 0b100: dbg_cross_couple_triggers(4). 0b101: dbg_cross_couple_triggers(12). 0b110: dbg_cross_couple_triggers(20). 0b111: dbg_cross_couple_triggers(28).

Register Name	Debug Instance 2 Condition 2 Register
Mnemonic	TP.TCOB0.OB.EPS.DBG.DBG_INST2_COND_REG_2
Address	00000000090107C5 (SCOM)
Description	This is debug macro configuration register 2 for the front-end 1 component.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	INST2_CROSS_COUPLE_SELECT_1_A: Cross coupling is the same for all selectors: 00000 = Selects inst2_cond1_trig_a. 00001 = Selects inst2_cond1_trig_b. 00010 = Selects inst2_cond2_trig_a. 00011 = Selects inst2_cond2_trig_b. 00100 = Selects inst2_condition1. 00101 = Selects inst2_condition2. 00110 = Selects inst2_condition3. 00111 = Selects inst2_cond2_timeout. 01000 = Selects inst2_cond1_trig_a. 01001 = Selects inst2_cond1_trig_b. 01010 = Selects inst2_cond2_trig_a. 01011 = Selects inst2_cond2_trig_b. 01100 = Selects inst2_condition1. 01101 = Selects inst2_condition2. 01110 = Selects inst2_condition3. 01111 = Selects inst2_cond2_timeout. 10000 = Selects inst3_cond1_trig_a. 10001 = Selects inst3_cond1_trig_b. 10010 = Selects inst3_cond2_trig_a. 10011 = Selects inst3_cond2_trig_b. 10100 = Selects inst3_condition1. 10101 = Selects inst3_condition2. 10110 = Selects inst3_condition3. 10111 = Selects inst3_cond2_timeout. 11000 = Selects inst4_cond1_trig_a. 11001 = Selects inst4_cond1_trig_b. 11010 = Selects inst4_cond2_trig_a. 11011 = Selects inst4_cond2_trig_b. 11100 = Selects inst4_condition1. 11101 = Selects inst4_condition2. 11110 = Selects inst4_condition3. 11111 = Selects inst4_cond2_timeout.
5:9	RW	INST2_CROSS_COUPLE_SELECT_1_B: inst2 cross couple select 1b.
10:14	RW	INST2_CROSS_COUPLE_SELECT_2_A: inst2 cross couple select 2a.
15:19	RW	INST2_CROSS_COUPLE_SELECT_2_B: inst2 cross couple select 2b.
20:43	RW	INST2_TO_CMP_LT: Compare value for special counter LT in debug component 2.
44	RW	INST2_FORCE_TEST_MODE: Force test mode to compare without an actual compare.

Register Name	Debug Instance 2 Condition 3 Register
Mnemonic	TP.TCOB0.OB.EPS.DBG.DBG_INST2_COND_REG_3
Address	00000000090107C6 (SCOM)
Description	This is debug macro configuration register 2 for the front-end 1 component.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	INST2_SP_COUNT_LT: Timeout counter to compare value for dbg_cond_comp_1.

Register Name	Debug Trace 0 Register
Mnemonic	TP.TCOB0.OB.EPS.DBG.DBG_TRACE_REG_0
Address	00000000090107CD (SCOM)
Description	This is debug macro configuration register 0 for the debug back-end component.

Bits	SCOM	Field Mnemonic: Description
0	RW	INST1_COND3_ENABLE: Enable instance 1 condition 3.
1	RW	INST2_COND3_ENABLE: Enable instance 2 condition 3.
2	RW	INST3_COND3_ENABLE: Unused.
3	RW	INST4_COND3_ENABLE: Unused.
4	RW	INST1_SLOW_LFSR_MODE: Enable slow LFSR mode of front end instance 1.
5	RW	INST2_SLOW_LFSR_MODE: Enable slow LFSR mode of front end instance 2.
6	RW	INST3_SLOW_LFSR_MODE: Unused.
7	RW	INST4_SLOW_LFSR_MODE: Unused.
8:9	RW	INST1_CONDITION1_TRIG_SEL: Select inst1 condition1 for output (external) triggers. 00 = Do nothing. 01 = trigger_out(0). 10 = trigger_out(1). 11 = trigger_out(2).
10:11	RW	INST1_CONDITION2_TRIG_SEL: Select inst1 condition2 for output (external) triggers. 00 = Do nothing. 01 = trigger_out(0). 10 = trigger_out(1). 11 = trigger_out(2).
12:13	RW	INST1_C2_TIMEOUT_TRIG_SEL: Select inst1 c2 time-out counter for output (external) triggers. 00 = Do nothing. 01 = trigger_out(0). 10 = trigger_out(1). 11 = trigger_out(2).
14:15	RW	INST2_CONDITION1_TRIG_SEL: Select inst2 condition1 for output (external) triggers. 00 = Do nothing. 01 = trigger_out(0). 10 = trigger_out(1). 11 = trigger_out(2).
16:17	RW	INST2_CONDITION2_TRIG_SEL: Select inst2 condition2 trigger for output (external) triggers. 00 = Do nothing. 01 = trigger_out(0). 10 = trigger_out(1). 11 = trigger_out(2).

Bits	SCOM	Field Mnemonic: Description
18:19	RW	INST2_C2_TIMEOUT_TRIG_SEL: Select inst2 c2 time-out counter for output (external) triggers. 00 = Do nothing. 01 = trigger_out(0). 10 = trigger_out(1). 11 = trigger_out(2).
20:31	RO	constant = 0b000000000000
32	RW	EXT_TRIG_ON_STOP: Enable trigger on stop.
33	RW	EXT_TRIG_ON_FREEZE: Enable trigger on freeze.
34:38	RW	CORE_RAS0_TRIG_SEL:
39:43	RW	CORE_RAS1_TRIG_SEL:
44:45	RW	PC_TP_TRIG_SEL:
46:49	RW	DBG_ARM_SEL:
50:53	RW	TRIG0_LEVEL_SEL: Select additional conditions for output (external) trigger signal trigger_out(0). **Note:** Some are N/A (inst3/4 conditions are tied to zero). 0001 = inst1_cond3_state_int(1). 0010 = inst1_cond3_state_int(0). 0011 = inst2_cond3_state_int(1). 0100 = inst2_cond3_state_int(0). 0101 = inst3_cond3_state_int(1). 0110 = inst3_cond3_state_int(0). 0111 = inst4_cond3_state_int(1). 1000 = inst4_cond3_state_int(0). 1001 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1). 1010 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1). 1011 = inst3_cond3_state_int(1) or inst4_cond3_state_int(1). 1100 = inst3_cond3_state_int(1) and inst4_cond3_state_int(1). 1101 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1). 1110 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1) and inst3_cond3_state_int(1). 1111 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1) or inst4_cond3_state_int(1).
54:57	RW	TRIG1_LEVEL_SEL: Select additional conditions for output (external) trigger signal trigger_out(1). **Note:** Some are N/A (inst3/4 conditions are tied to zero). 0001 = inst1_cond3_state_int(1). 0010 = inst1_cond3_state_int(0). 0011 = inst2_cond3_state_int(1). 0100 = inst2_cond3_state_int(0). 0101 = inst3_cond3_state_int(1). 0110 = inst3_cond3_state_int(0). 0111 = inst4_cond3_state_int(1). 1000 = inst4_cond3_state_int(0). 1001 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1). 1010 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1). 1011 = inst3_cond3_state_int(1) or inst4_cond3_state_int(1). 1100 = inst3_cond3_state_int(1) and inst4_cond3_state_int(1). 1101 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1). 1110 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1) and inst3_cond3_state_int(1). 1111 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1) or inst4_cond3_state_int(1).
58:63	RO	constant = 0b000000

Register Name	Debug Trace 1 Register
Mnemonic	TP.TCOB0.OB.EPS.DBG.DBG_TRACE_REG_1
Address	00000000090107CE (SCOM)
Description	This is debug macro configuration register 1 for the back-end component.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	INST1_CONDITION1_ACTION_DO: Inst1 action selection , condition1: 00 = Nothing. 01 = Start. 10 = Stop. 11 = RUNN: start now, and stop after n cycles.
2:3	RW	INST1_CONDITION2_ACTION_DO: Inst1 action selection , condition2: 00 = Nothing. 01 = Start. 10 = Stop. 11 = RUNN: start now, and stop after n cycles.
4:5	RW	INST1_C2_TIMEOUT_ACTION_DO: Inst1 action selection , c2_timeout: 00 = Nothing. 01 = Start. 10 = Stop. 11 = RUNN: start now, and stop after n cycles.
6:7	RW	INST2_CONDITION1_ACTION_DO: inst2 action selection , condition1: 00 = Nothing. 01 = Start. 10 = Stop. 11 = RUNN: start now, and stop after n cycles.
8:9	RW	INST2_CONDITION2_ACTION_DO: Inst2 action selection , condition2: 00 = Nothing. 01 = Start. 10 = Stop. 11 = RUNN: start now, and stop after n cycles.
10:11	RW	INST2_C2_TIMEOUT_ACTION_DO: Inst2 action selection , c2_timeout: 00 = Nothing. 01 = Start. 10 = Stop. 11 = RUNN: start now, and stop after n cycles.
12:23	RO	constant = 0b000000000000
24	RW	INST1_CONDITION1_ACTION_WAITN: Selection for WAITN.
25	RW	INST1_CONDITION2_ACTION_WAITN: Selection for WAITN.
26	RW	INST1_C2_TIMEOUT_ACTION_WAITN: Selection for WAITN.
27	RW	INST2_CONDITION1_ACTION_WAITN: Selection for WAITN.
28	RW	INST2_CONDITION2_ACTION_WAITN: Selection for WAITN.
29	RW	INST2_C2_TIMEOUT_ACTION_WAITN: Selection for WAITN.
30:35	RO	constant = 0b000000
36	RW	INST1_CONDITION1_ACTION_BANK: Trace bank switch (inst1, condition1).
37	RW	INST1_CONDITION2_ACTION_BANK: Trace bank switch (inst1, condition2).
38	RW	INST1_C2_TIMEOUT_ACTION_BANK: Trace bank switch (inst1, c2_timeout).
39	RW	INST2_CONDITION1_ACTION_BANK: Trace bank switch (inst2, condition1).
40	RW	INST2_CONDITION2_ACTION_BANK: Trace bank switch (inst2, condition2).

Bits	SCOM	Field Mnemonic: Description
41	RW	INST2_C2_TIMEOUT_ACTION_BANK: Trace bank switch (inst2, c2_timeout).
42:47	RO	constant = 0b000000
48:50	RW	INST1_CHECKSTOP_MODE_LT: Select additional condition with fir_error_lt for dbg_fir_xstop_on_trig output: 000 = inst1_condition1_lt. 001 = inst1_condition2_lt. 010 = inst1_condition3_lt. 011 = inst1_cond2_timeout_lt. 1xx = Disable checkstop mode.
51	RW	INST1_CHECKSTOP_MODE_SELECTOR: enable_fir_trig_xstop: Enable checkstop on debug trigger: 0 = Disable checkstop on debug trigger. 1 = Enable checkstop on debug trigger.
52:54	RW	INST2_CHECKSTOP_MODE_LT: Select additional condition with fir_error_lt for dbg_fir_xstop_on_trig output: 000 = inst2_condition1_lt. 001 = inst2_condition2_lt. 010 = inst2_condition3_lt. 011 = inst2_cond2_timeout_lt. 1xx = Disable checkstop_mode.
55	RW	INST2_CHECKSTOP_MODE_SELECTOR: enable_fir_error_xstop: Enable checkstop on fir error: 0 = Disable checkstop on FIR error. 1 = Enable checkstop on FIR error.
56:63	RO	constant = 0b00000000

Register Name	Debug Trace Mode 2 Register
Mnemonic	TP.TCOB0.OB.EPS.DBG.DBG_TRACE_MODE_REG_2
Address	00000000090107CF (SCOM)
Description	This is debug macro configuration register 2 for the back-end component.

Bits	SCOM	Field Mnemonic: Description
0:15	RW	RUNN_COUNT_COMPARE_VALUE: Compare value for the RUNN counter used in trace modes RUNN and WAITN.
16	RW	IMM_FREEZE_MODE: Immediate freeze mode.
17	RW	STOP_ON_ERR: Stop and freeze on checkstop.
18	RW	BANK_ON_RUNN_MATCH: Bank switch on RUNN match.
19	RW	FORCE_TEST_MODE: Force RUNN condition to be true.
20	RW	ACCUM_HIST_MODE: Accumulate history mode; do not clear history mode when trace_run active.
21	RW	FRZ_COUNT_ON_FRZ: Freeze condition counters on trace freeze.

Register Name	Debug Trace Control Register
Mnemonic	TP.TCOB0.OB.EPS.DBG.DEBUG_TRACE_CONTROL
Address	00000000090107D0 (SCOM)
Description	This is the trace start/stop/rest using SCOM command register. Use write data(0/1/2) = 1. This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0	WOX	Reserved field.
1	WOX	Reserved field.
2	WOX	Reserved field.

Register Name	**Extra Trace Mode Register**
Mnemonic	TP.TCOB0.OB.EPS.DBG.XTRA_TRACE_MODE
Address	00000000090107D1 (SCOM)
Description	This register provides an extra or dedicated trace mode register for core triggers.

Bits	SCOM	Field Mnemonic: Description
0:37	RW	XTRA_TRACE_MODE_DATA: Extra/dedicated trace mode for core triggers.

Register Name	**Power Bus OLL FIR Register**
Mnemonic	PB.IOO.LL0.PB_IOOL_FIR_REG
Address	0000000009010800 (SCOM) 0000000009010801 (SCOM1) 0000000009010802 (SCOM2)
Description	Processor bus OLL FIR register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_LINK0_TRAINED: link0 trained.
1	RWX	WOX_AND	WOX_OR	FIR_LINK1_TRAINED: link1 trained.
2	RWX	WOX_AND	WOX_OR	FIR_LINK0_OP_IRQ: link0 OP IRQ.
3	RWX	WOX_AND	WOX_OR	FIR_LINK1_OP_IRQ: link1 OP IRQ.
4	RWX	WOX_AND	WOX_OR	FIR_LINK0_REPLAY_THRESHOLD: link0 replay threshold.
5	RWX	WOX_AND	WOX_OR	FIR_LINK1_REPLAY_THRESHOLD: link1 replay threshold.
6	RWX	WOX_AND	WOX_OR	FIR_LINK0_CRC_ERROR: link0 CRC error.
7	RWX	WOX_AND	WOX_OR	FIR_LINK1_CRC_ERROR: link1 CRC error.
8	RWX	WOX_AND	WOX_OR	FIR_LINK0_NAK_RECEIVED: link0 NAK received.
9	RWX	WOX_AND	WOX_OR	FIR_LINK1_NAK_RECEIVED: link1 NAK received.
10	RWX	WOX_AND	WOX_OR	FIR_LINK0_REPLAY_BUFFER_FULL: link0 replay buffer full.
11	RWX	WOX_AND	WOX_OR	FIR_LINK1_REPLAY_BUFFER_FULL: link1 replay buffer full.
12	RWX	WOX_AND	WOX_OR	FIR_LINK0_SL_ECC_THRESHOLD: link0 SL ECC threshold.
13	RWX	WOX_AND	WOX_OR	FIR_LINK1_SL_ECC_THRESHOLD: link1 SL ECC threshold.
14	RWX	WOX_AND	WOX_OR	FIR_LINK0_SL_ECC_CORRECTABLE: link0 SL ECC correctable.
15	RWX	WOX_AND	WOX_OR	FIR_LINK1_SL_ECC_CORRECTABLE: link1 SL ECC correctable.
16	RWX	WOX_AND	WOX_OR	FIR_LINK0_SL_ECC_UE: link0 SL ECC UE.
17	RWX	WOX_AND	WOX_OR	FIR_LINK1_SL_ECC_UE: link1 SL ECC UE.
18	RWX	WOX_AND	WOX_OR	FIR_LINK0_RETRAIN_THRESHOLD: link0 retrain threshold.
19	RWX	WOX_AND	WOX_OR	FIR_LINK1_RETRAIN_THRESHOLD: link1 retrain threshold.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
20	RWX	WOX_AND	WOX_OR	FIR_LINK0_LOSS_BLOCK_ALIGN: link0 loss block align.
21	RWX	WOX_AND	WOX_OR	FIR_LINK1_LOSS_BLOCK_ALIGN: link1 loss block align.
22	RWX	WOX_AND	WOX_OR	FIR_LINK0_INVALID_BLOCK: link0 invalid block.
23	RWX	WOX_AND	WOX_OR	FIR_LINK1_INVALID_BLOCK: link1 invalid block.
24	RWX	WOX_AND	WOX_OR	FIR_LINK0_DESKEW_ERROR: link0 deskew error.
25	RWX	WOX_AND	WOX_OR	FIR_LINK1_DESKEW_ERROR: link1 deskew error.
26	RWX	WOX_AND	WOX_OR	FIR_LINK0_DESKEW_OVERFLOW: link0 deskew overflow.
27	RWX	WOX_AND	WOX_OR	FIR_LINK1_DESKEW_OVERFLOW: link1 deskew overflow.
28	RWX	WOX_AND	WOX_OR	FIR_LINK0_SW_RETRAIN: link0 sw retrain.
29	RWX	WOX_AND	WOX_OR	FIR_LINK1_SW_RETRAIN: link1 sw retrain.
30	RWX	WOX_AND	WOX_OR	FIR_LINK0_ACK_QUEUE_OVERFLOW: link0 ACK queue overflow.
31	RWX	WOX_AND	WOX_OR	FIR_LINK1_ACK_QUEUE_OVERFLOW: link1 ACK queue overflow.
32	RWX	WOX_AND	WOX_OR	FIR_LINK0_ACK_QUEUE_UNDERFLOW: link0 ACK queue underflow.
33	RWX	WOX_AND	WOX_OR	FIR_LINK1_ACK_QUEUE_UNDERFLOW: link1 ACK queue underflow.
34	RWX	WOX_AND	WOX_OR	FIR_LINK0_NUM_REPLAY: link0 num replay.
35	RWX	WOX_AND	WOX_OR	FIR_LINK1_NUM_REPLAY: link1 num replay.
36	RWX	WOX_AND	WOX_OR	FIR_LINK0_TRAINING_SET_RECEIVED: link0 training set received.
37	RWX	WOX_AND	WOX_OR	FIR_LINK1_TRAINING_SET_RECEIVED: link1 training set received.
38	RWX	WOX_AND	WOX_OR	FIR_LINK0_PRBS_SELECT_ERROR: link0 PRBS select error.
39	RWX	WOX_AND	WOX_OR	FIR_LINK1_PRBS_SELECT_ERROR: link1 PRBS select error.
40	RWX	WOX_AND	WOX_OR	FIR_LINK0_TCOMPLETE_BAD: link0 TCOMPLETE bad.
41	RWX	WOX_AND	WOX_OR	FIR_LINK1_TCOMPLETE_BAD: link1 TCOMPLETE bad.
42:43	RWX	WOX_AND	WOX_OR	Reserved.
44	RWX	WOX_AND	WOX_OR	FIR_LINK0_SPARE_DONE: link0 spare done.
45	RWX	WOX_AND	WOX_OR	FIR_LINK1_SPARE_DONE: link1 spare done.
46	RWX	WOX_AND	WOX_OR	FIR_LINK0_TOO_MANY_CRC_ERRORS: link0 too many CRC errors.
47	RWX	WOX_AND	WOX_OR	FIR_LINK1_TOO_MANY_CRC_ERRORS: link1 too many CRC errors.
48	RWX	WOX_AND	WOX_OR	FIR_LINK0_NPU_ERROR: link0 NPU error.
49	RWX	WOX_AND	WOX_OR	FIR_LINK1_NPU_ERROR: link1 NPU error.
50	RWX	WOX_AND	WOX_OR	FIR_LINKX_NPU_ERROR: linkx NPU error.
51	RWX	WOX_AND	WOX_OR	FIR_OSC_SWITCH: OSC switch.
52	RWX	WOX_AND	WOX_OR	FIR_LINK0_CORRECTABLE_ARRAY_ERROR: link0 correctable array error.
53	RWX	WOX_AND	WOX_OR	FIR_LINK1_CORRECTABLE_ARRAY_ERROR: link1 correctable array error.
54	RWX	WOX_AND	WOX_OR	FIR_LINK0_UNCORRECTABLE_ARRAY_ERROR: link0 uncorrectable array error.
55	RWX	WOX_AND	WOX_OR	FIR_LINK1_UNCORRECTABLE_ARRAY_ERROR: link1 uncorrectable array error.
56	RWX	WOX_AND	WOX_OR	FIR_LINK0_TRAINING_FAILED: link0 training failed.
57	RWX	WOX_AND	WOX_OR	FIR_LINK1_TRAINING_FAILED: link1 training failed.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
58	RWX	WOX_AND	WOX_OR	FIR_LINK0_UNRECOVERABLE_ERROR: link0 unrecoverable error.
59	RWX	WOX_AND	WOX_OR	FIR_LINK1_UNRECOVERABLE_ERROR: link1 unrecoverable error.
60	RWX	WOX_AND	WOX_OR	FIR_LINK0_INTERNAL_ERROR: link0 internal error.
61	RWX	WOX_AND	WOX_OR	FIR_LINK1_INTERNAL_ERROR: link1 internal error.
62	RWX	WOX_AND	WOX_OR	FIR_SCOM_ERR_DUP: FIR SCOM error dup.
63	RWX	WOX_AND	WOX_OR	FIR_SCOM_ERR: FIR SCOM error.

Register Name	Power Bus OLL FIR Mask Register
Mnemonic	PB.IOO.LL0.PB_IOOL_FIR_MASK_REG
Address	0000000009010803 (SCOM) 0000000009010804 (SCOM1) 0000000009010805 (SCOM2)
Description	Processor bus OLL FIR mask register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_LINK0_TRAINED_MASK: link0 trained mask.
1	RWX	WOX_AND	WOX_OR	FIR_LINK1_TRAINED_MASK: link1 trained mask.
2	RWX	WOX_AND	WOX_OR	FIR_LINK0_OP_IRQ_MASK: link0 OP IRQ mask.
3	RWX	WOX_AND	WOX_OR	FIR_LINK1_OP_IRQ_MASK: link1 OP IRQ mask.
4	RWX	WOX_AND	WOX_OR	FIR_LINK0_REPLAY_THRESHOLD_MASK: link0 replay threshold mask.
5	RWX	WOX_AND	WOX_OR	FIR_LINK1_REPLAY_THRESHOLD_MASK: link1 replay threshold mask.
6	RWX	WOX_AND	WOX_OR	FIR_LINK0_CRC_ERROR_MASK: link0 CRC error mask.
7	RWX	WOX_AND	WOX_OR	FIR_LINK1_CRC_ERROR_MASK: link1 CRC error mask.
8	RWX	WOX_AND	WOX_OR	FIR_LINK0_NAK_RECEIVED_MASK: link0 NAK received mask.
9	RWX	WOX_AND	WOX_OR	FIR_LINK1_NAK_RECEIVED_MASK: link1 NAK received mask.
10	RWX	WOX_AND	WOX_OR	FIR_LINK0_REPLAY_BUFFER_FULL_MASK: link0 replay buffer full mask.
11	RWX	WOX_AND	WOX_OR	FIR_LINK1_REPLAY_BUFFER_FULL_MASK: link1 replay buffer full mask.
12	RWX	WOX_AND	WOX_OR	FIR_LINK0_SL_ECC_THRESHOLD_MASK: link0 SL ECC threshold mask.
13	RWX	WOX_AND	WOX_OR	FIR_LINK1_SL_ECC_THRESHOLD_MASK: link1 SL ECC threshold mask.
14	RWX	WOX_AND	WOX_OR	FIR_LINK0_SL_ECC_CORRECTABLE_MASK: link0 SL ECC correctable mask.
15	RWX	WOX_AND	WOX_OR	FIR_LINK1_SL_ECC_CORRECTABLE_MASK: link1 SL ECC correctable mask.
16	RWX	WOX_AND	WOX_OR	FIR_LINK0_SL_ECC_UE_MASK: link0 SL ECC UE mask.
17	RWX	WOX_AND	WOX_OR	FIR_LINK1_SL_ECC_UE_MASK: link1 SL ECC UE mask.
18	RWX	WOX_AND	WOX_OR	FIR_LINK0_RETRAIN_THRESHOLD_MASK: link0 retrain threshold mask.
19	RWX	WOX_AND	WOX_OR	FIR_LINK1_RETRAIN_THRESHOLD_MASK: link1 retrain threshold mask.
20	RWX	WOX_AND	WOX_OR	FIR_LINK0_LOSS_BLOCK_ALIGN_MASK: link0 loss block align mask.
21	RWX	WOX_AND	WOX_OR	FIR_LINK1_LOSS_BLOCK_ALIGN_MASK: link1 loss block align mask.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
22	RWX	WOX_AND	WOX_OR	FIR_LINK0_INVALID_BLOCK_MASK: link0 invalid block mask.
23	RWX	WOX_AND	WOX_OR	FIR_LINK1_INVALID_BLOCK_MASK: link1 invalid block mask.
24	RWX	WOX_AND	WOX_OR	FIR_LINK0_DESKEW_ERROR_MASK: link0 deskew error mask.
25	RWX	WOX_AND	WOX_OR	FIR_LINK1_DESKEW_ERROR_MASK: link1 deskew error mask.
26	RWX	WOX_AND	WOX_OR	FIR_LINK0_DESKEW_OVERFLOW_MASK: link0 deskew overflow mask.
27	RWX	WOX_AND	WOX_OR	FIR_LINK1_DESKEW_OVERFLOW_MASK: link1 deskew error mask.
28	RWX	WOX_AND	WOX_OR	FIR_LINK0_SW_RETRAIN_MASK: link0 sw retrain mask.
29	RWX	WOX_AND	WOX_OR	FIR_LINK1_SW_RETRAIN_MASK: link1 sw retrain mask.
30	RWX	WOX_AND	WOX_OR	FIR_LINK0_ACK_QUEUE_OVERFLOW_MASK: link0 ACK queue overflow mask.
31	RWX	WOX_AND	WOX_OR	FIR_LINK1_ACK_QUEUE_OVERFLOW_MASK: link1 ACK queue overflow mask.
32	RWX	WOX_AND	WOX_OR	FIR_LINK0_ACK_QUEUE_UNDERFLOW_MASK: link0 ACK queue underflow mask.
33	RWX	WOX_AND	WOX_OR	FIR_LINK1_ACK_QUEUE_UNDERFLOW_MASK: link1 ACK queue underflow mask.
34	RWX	WOX_AND	WOX_OR	FIR_LINK0_NUM_REPLAY_MASK: link0 num replay mask.
35	RWX	WOX_AND	WOX_OR	FIR_LINK1_NUM_REPLAY_MASK: link1 num replay mask.
36	RWX	WOX_AND	WOX_OR	FIR_LINK0_TRAINING_SET_RECEIVED_MASK: link0 training set received mask.
37	RWX	WOX_AND	WOX_OR	FIR_LINK1_TRAINING_SET_RECEIVED_MASK: link1 training set received mask.
38	RWX	WOX_AND	WOX_OR	FIR_LINK0_PRBS_SELECT_ERROR_MASK: link0 PRBS select error mask.
39	RWX	WOX_AND	WOX_OR	FIR_LINK1_PRBS_SELECT_ERROR_MASK: link1 PRBS select error mask.
40	RWX	WOX_AND	WOX_OR	FIR_LINK0_TCOMPLETE_BAD_MASK: link0 tcomplete bad mask.
41	RWX	WOX_AND	WOX_OR	FIR_LINK1_TCOMPLETE_BAD_MASK: link1 tcomplete bad mask.
42:43	RWX	WOX_AND	WOX_OR	Reserved.
44	RWX	WOX_AND	WOX_OR	FIR_LINK0_SPARE_DONE_MASK: link0 spare done mask.
45	RWX	WOX_AND	WOX_OR	FIR_LINK1_SPARE_DONE_MASK: link1 spare done mask.
46	RWX	WOX_AND	WOX_OR	FIR_LINK0_TOO_MANY_CRC_ERRORS_MASK: link0 too many CRC errors mask.
47	RWX	WOX_AND	WOX_OR	FIR_LINK1_TOO_MANY_CRC_ERRORS_MASK: link1 too many CRC errors mask.
48	RWX	WOX_AND	WOX_OR	FIR_LINK0_NPU_ERROR_MASK: link0 NPU error mask.
49	RWX	WOX_AND	WOX_OR	FIR_LINK1_NPU_ERROR_MASK: link1 NPU error mask.
50	RWX	WOX_AND	WOX_OR	FIR_LINKX_NPU_ERROR_MASK: linkx NPU error mask.
51	RWX	WOX_AND	WOX_OR	FIR_OSC_SWITCH_MASK: OSC switch mask.
52	RWX	WOX_AND	WOX_OR	FIR_LINK0_CORRECTABLE_ARRAY_ERROR_MASK: link0 correctable array error mask.
53	RWX	WOX_AND	WOX_OR	FIR_LINK1_CORRECTABLE_ARRAY_ERROR_MASK: link1 correctable array error mask.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
54	RWX	WOX_AND	WOX_OR	FIR_LINK0_UNCORRECTABLE_ARRAY_ERROR_MASK: link0 uncorrectable array error mask.
55	RWX	WOX_AND	WOX_OR	FIR_LINK1_UNCORRECTABLE_ARRAY_ERROR_MASK: link1 uncorrectable array error mask.
56	RWX	WOX_AND	WOX_OR	FIR_LINK0_TRAINING_FAILED_MASK: link0 training failed mask.
57	RWX	WOX_AND	WOX_OR	FIR_LINK1_TRAINING_FAILED_MASK: link1 training failed mask.
58	RWX	WOX_AND	WOX_OR	FIR_LINK0_UNRECOVERABLE_ERROR_MASK: link0 unrecoverable error mask.
59	RWX	WOX_AND	WOX_OR	FIR_LINK1_UNRECOVERABLE_ERROR_MASK: link1 unrecoverable error mask.
60	RWX	WOX_AND	WOX_OR	FIR_LINK0_INTERNAL_ERROR_MASK: link0 internal error mask.
61	RWX	WOX_AND	WOX_OR	FIR_LINK1_INTERNAL_ERROR_MASK: link1 internal error mask.
62	RWX	WOX_AND	WOX_OR	FIR_SCOM_ERR_DUP_MASK: FIR SCOM error dup mask.
63	RWX	WOX_AND	WOX_OR	FIR_SCOM_ERR_MASK: FIR SCOM error mask.

Register Name	Power Bus OLL FIR Action 0 Register
Mnemonic	PB.IOO.LL0.PB_IOOL_FIR_ACTION0_REG
Address	0000000009010806 (SCOM)
Description	Processor bus OLL FIR action 0 register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	PB_IOOL_FIR_ACTION0: Processor bus FIR MSB of action select for corresponding bit in FIR. (Action0,Action1) = Action select. (0,0) = Checkstop. (0,1) = Recoverable error to service processor. (1,0) = Special attention to service processor. (1,1) = Invalid.

Register Name	Power Bus OLL FIR Action 1 Register
Mnemonic	PB.IOO.LL0.PB_IOOL_FIR_ACTION1_REG
Address	0000000009010807 (SCOM)
Description	Processor bus OLL FIR action 1 register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	PB_IOOL_FIR_ACTION1: Processor bus FIR LSB of action select for corresponding bit in FIR. (Action0,Action1) = Action select. (0,0) = Checkstop. (0,1) = Recoverable error to service processor. (1,0) = Special attention to service processor. (1,1) = Invalid.

Register Name	Power Bus OLL Configuration Register
Mnemonic	PB.IOO.LL0.IOOL_CONFIG
Address	000000000901080A (SCOM)
Description	Processor bus OLL configuration register

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_LINK_PAIR: When 1, the two links operate as a pair. When 0, only one of the links used or they are independent.
1	RW	CONFIG_DISABLE_SL_ECC: When 1, disable spare lane ECC correction.
2	RW	CONFIG_CRC_LANE_ID: When 1, use lane IDs from CRC for lane sparing.
3	RW	CONFIG_EDPL_LANE_ID: When 1, use lane IDs from EDPL for lane sparing.
4	RW	CONFIG_SL_UE_CRC_ERR: When 1, UEs on SL ECC cause the packet to be treated as a CRC error.
5	RW	CONFIG_REPORT_SL_CHKBIT_ERR: When 1, SL ECC single bit errors on check bits are reported to FIR.
6	RW	CONFIG_BW_SAMPLE_SIZE: When 1, use 256 packets for sample (instead of 64).
7	RW	CONFIG_BW_WINDOW_SIZE: When 1, shorten the sample window.
8:11	RW	CONFIG_UNUSED1: Spare bits.
12:15	RW	CONFIG_PACKET_DELAY_LIMIT: Number of cycles of delay of frame data to be considered delayed/replayed (0 is 16 cycles).
16:19	RW	CONFIG_TDM_DELAY: Adjustment factor of delay for entering/exiting TDM mode.
20	RW	CONFIG_AUTO_TDM_TX: When 1, use TX bandwidth for automatically entering TDM mode.
21	RW	CONFIG_AUTO_TDM_RX: When 1, use RX bandwidth for automatically entering TDM mode.
22	RW	CONFIG_AUTO_TDM_AND_NOT_OR: When 1, both BW and error rate needed (otherwise, either).
23	RW	CONFIG_UNUSED2: Spare bits.
24:27	RW	CONFIG_AUTO_TDM_BW_DIFF: Bandwidth difference for auto entry TDM mode.
28:31	RW	CONFIG_AUTO_TDM_ERROR_RATE: Error rate for auto entry TDM mode.
32:47	RW	CONFIG_UNUSED3: Spare bits.
48:51	RWX	CONFIG_TIMEOUT: Program timeout values, from 1 μs to 65 ms.
52:63	RWX	CONFIG_TIMER_1US: Program number of cycles in 1μs.

Register Name	Power Bus OLL Control Register
Mnemonic	PB.IOO.LL0.IOOL_CONTROL
Address	000000000901080B (SCOM)
Description	Processor bus OLL control register

Bits	SCOM	Field Mnemonic: Description
0	RW	LINK0_PHY_TRAINING: When 1, run PHY training.
1	RW	LINK0_STARTUP: When 1, start initialization/training.
2	RW	LINK0_HOLD_PATT_A: When 1, hold PHY training at sending Pattern A.
3	RW	LINK0_HOLD_PATT_B: When 1, hold PHY training at sending Pattern B.
4	RW	LINK0_RUN_LANE_DISABLE: When 1, hardware control of run_lane is disabled.
5	RW	LINK0_RUN_LANE_OVERRIDE: When 1, the run_lane signal is forced to 1.

Bits	SCOM	Field Mnemonic: Description
6	RW	LINK0_IGNORE_PHY: When 1, all data from PHY is ignored (like fence is 1).
7	RW	LINK0_IGNORE_FENCE: When 1, PHY fence signal is ignored (treated like 0).
8:11	RWX	LINK0_ERR_INJ_COMMAND: Command to do link error injection.
12:23	RWX	LINK0_ERR_INJ_COMMAND_LANES: Lanes for error inject command.
24:27	RWX	CONTROL_UNUSED0: Spare bits.
28:31	RWX	LINK0_COMMAND: Command to do an operation.
32	RW	LINK1_PHY_TRAINING: When 1, run PHY training.
33	RW	LINK1_STARTUP: When 1, start initialization/training.
34	RW	LINK1_HOLD_PATT_A: When 1, hold PHY training at sending Pattern A.
35	RW	LINK1_HOLD_PATT_B: When 1, hold PHY training at sending Pattern B.
36	RW	LINK1_RUN_LANE_DISABLE: When 1, hardware control of run_lane is disabled.
37	RW	LINK1_RUN_LANE_OVERRIDE: When 1, the run_lane signal is forced to 1.
38	RW	LINK1_IGNORE_PHY: When 1, all data from PHY is ignored (like fence is 1).
39	RW	LINK1_IGNORE_FENCE: When 1, PHY fence signal is ignored (treated like 0).
40:43	RWX	LINK1_ERR_INJ_COMMAND: Command to do link error injection.
44:55	RWX	LINK1_ERR_INJ_COMMAND_LANES: Lanes for error inject command.
56:59	RWX	CONTROL_UNUSED1: Spare bits.
60:63	RWX	LINK1_COMMAND: Command to do an operation.

Register Name	**Power Bus OLL PHY Training Configuration Register**
Mnemonic	PB.IOO.LL0.IOOL_PHY_CONFIG
Address	000000000901080C (SCOM)
Description	Processor bus OLL PHY training configuration register

Bits	SCOM	Field Mnemonic: Description
0:1	RW	CONFIG_PHY_TRAIN_A_ADJ: Adjust the number of bits out of 8 for pattern A detection.
2:3	RW	CONFIG_PHY_TRAIN_B_ADJ: Adjust the number of bits out of 16 for pattern B detection.
4:7	RW	CONFIG_PHY_TRAIN_TIME: Time to see Pattern A/B before reporting it.
8:11	RW	CONFIG_PHY_TRAIN_A_HYST: Amount of hysteresis in detecting Pattern A.
12:15	RW	CONFIG_PHY_TRAIN_B_HYST: Amount of hysteresis in detecting Pattern B.
16:39	RW	CONFIG_PRBS_PHASE_SELECT: Select phases for the lanes for PRBS transmit option (exactly 12 bits must be set).
40:49	RW	CONFIG_PRBS_CONFIG: Select PRBS length and tap.
50	RW	CONFIG_PRBS_INVERT: When 1, send the inverted PRBS pattern.
51:63	RW	CONFIG_PHY_UNUSED: Spare bits.

Register Name	Power Bus OLL Secondary Configuration Register
Mnemonic	PB.IOO.LL0.IOOL_SEC_CONFIG
Address	000000000901080D (SCOM)
Description	Processor bus OLL secondary configuration register

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_ENABLE_ERR_INJ: When 1, enable error injection (LFSR runs).
1:15	RW	CONFIG_UNUSED4: Spare bits.
16:17	RW	CONFIG_SBE_ERROR_RATE: Error injection SBE rate.
18:23	RW	CONFIG_RAND_ERROR_RATE: Error injection rate N (from 1 to 38), probability is 2^{-N}.
24:25	RW	CONFIG_INV_SH_ERROR_RATE: Error injection invalid sync header (SBE) rate.
26:31	RW	CONFIG_SYNC_HEADER_ERROR_RATE: Error injection rate N (from 1 to 38), probability is 2^{-N}.
32:47	RW	CONFIG_UNUSED5: Spare bits.
48:63	RW	CONFIG_EDPL_RATE: When 0, disable EDPL. Otherwise, the number of blocks transmitted between EDPL blocks.

Register Name	Power Bus OLL Latency Measure Register
Mnemonic	PB.IOO.LL0.IOOL_LAT_MEASURE
Address	000000000901080E (SCOM)
Description	Processor bus OLL latency measure register

Bits	SCOM	Field Mnemonic: Description
0	ROX	LINK0_ROUND_TRIP_VALID: When 1, the round trip value is valid.
1	RO	constant = 0b0
2:11	ROX	LINK0_ROUND_TRIP: Round trip time in cycles.
12	ROX	LINK1_ROUND_TRIP_VALID: When 1, the round trip value is valid.
13	RO	constant = 0b0
14:23	ROX	LINK1_ROUND_TRIP: Round trip time in cycles.
24	ROX	LOCAL_LATENCY_DIFFERENCE_VALID: When 1, the local latency difference is valid.
25	ROX	LOCAL_LATENCY_LONGER_LINK: When 1, link1 had the longer latency.
26:28	RO	constant = 0b000
29:35	ROX	LOCAL_LATENCY_DIFFERENCE: Received difference in latency between links.
36	ROX	REMOTE_LATENCY_DIFFERENCE_VALID: When 1, the remote latency difference is valid.
37	ROX	REMOTE_LATENCY_LONGER_LINK: When 1, link1 had the longer latency.
38:40	RO	constant = 0b000
41:47	ROX	REMOTE_LATENCY_DIFFERENCE: TX difference in latency between links (as received by other side).
48	RO	constant = 0b0
49:55	RWX	LINK0_TOD_LATENCY: Latency of TOD pulses.
56	RO	constant = 0b0
57:63	RWX	LINK1_TOD_LATENCY: Latency of TOD pulses.

Register Name	Power Bus OLL Optical Configuration Register
Mnemonic	PB.IOO.LL0.IOOL_OPTICAL_CONFIG
Address	000000000901080F (SCOM)
Description	Processor bus OLL optical configuration register

Bits	SCOM	Field Mnemonic: Description
0	RW	CONFIG_DISABLE_BAD_LANE_COUNT: When 1, disable bad lane counter for lane sparing.
1	RW	CONFIG_DISABLE_CLEAR_BAD_LANE_COUNT: When 1, disable clearing bad lane counter when a different error occurs.
2:3	RW	CONFIG_OPT_UNUSED1: Spare bits.
4:7	RW	CONFIG_BAD_LANE_DURATION: Selects time to reset bad lane counter.
8	RW	CONFIG_OPT_UNUSED2: Spare bits.
9:15	RW	CONFIG_BAD_LANE_MAX: Number of errors before marking a lane as bad.
16	RW	CONFIG_DISABLE_LINK_FAIL_COUNT: When 1, disable link fail counter for lane sparing.
17:19	RW	CONFIG_OPT_UNUSED3: Spare bits.
20:23	RW	CONFIG_LINK_FAIL_DURATION: Selects time to cut link fail counter in half.
24	RW	CONFIG_OPT_UNUSED4: Spare bits.
25:31	RW	CONFIG_LINK_FAIL_MAX: Number of errors before making the link fail.
32	RWX	CLEAR_LINK_FAIL_COUNTER: When 1, clear the link fail counter.
33	RWX	CLEAR_BAD_LANE_COUNTER: When 1, clear the bad lane counter.
34:36	RW	CONFIG_OPT_UNUSED5: Spare bits.
37	RW	CONFIG_ELEVEN_LANE_MODE: When 1, link uses 11 lanes (instead of 12).
38	RW	LINK0_ELEVEN_LANE_SHIFT: When 1, in 11-lane mode, use lanes 1-11 (instead of 0-10).
39	RW	LINK1_ELEVEN_LANE_SHIFT: When 1, in 11-lane mode, use lanes 1-11 (instead of 0-10).
40	RW	LINK0_RX_LANE_SWAP: When 1, the lanes are swapped (0 with 10/11, and so on).
41	RW	LINK0_TX_LANE_SWAP: When 1, the lanes are swapped (0 with 10/11, and so on).
42	RW	LINK1_RX_LANE_SWAP: When 1, the lanes are swapped (0 with 10/11, and so on).
43	RW	LINK1_TX_LANE_SWAP: When 1, the lanes are swapped (0 with 10/11, and so on).
44:47	RW	CONFIG_ACK_QUEUE_LOW: Low limit for ACK queue.
48:51	RWX	CONFIG_ACK_QUEUE_START: Start value for ACK queue.
52:55	RWX	CONFIG_ACK_QUEUE_HIGH: High limit for ACK queue.
56:57	RW	CONFIG_REPLAY_BUFFER_SIZE: Size of the replay buffer to use. CAPP mode is largest but cannot be used for fabric traffic.
58	RW	CONFIG_LINK0_OLL_ENABLED: Enable OLL link 0 to use shared PHY and transport buses.
59	RW	CONFIG_LINK1_OLL_ENABLED: Enable OLL link 1 to use shared PHY and transport buses.
60	RW	CONFIG_NPU_TRANSPORT_SWAP:
61	RW	CONFIG_NV0_NPU_ENABLED: Enable NPU NV brick 0 to use shared PHY and transport buses.
62	RW	CONFIG_NV1_NPU_ENABLED: Enable NPU NV brick 1 to use shared PHY and transport buses.
63	RW	CONFIG_NV2_NPU_ENABLED: Enable NPU NV brick 2 to use shared PHY and transport buses.

Register Name	Power Bus OLL Link 0 Transmit Lane Control Register
Mnemonic	PB.IOO.LL0.IOOL_LINK0_TX_LANE_CONTROL
Address	0000000009010810 (SCOM)
Description	Processor bus OLL link0 transmit lane control register

Bits	SCOM	Field Mnemonic: Description
0:3	RW	TX_LINK0_LANE00_CONTROL: Transmit lane control.
4:7	RW	TX_LINK0_LANE01_CONTROL: Transmit lane control.
8:11	RW	TX_LINK0_LANE02_CONTROL: Transmit lane control.
12:15	RW	TX_LINK0_LANE03_CONTROL: Transmit lane control.
16:19	RW	TX_LINK0_LANE04_CONTROL: Transmit lane control.
20:23	RW	TX_LINK0_LANE05_CONTROL: Transmit lane control.
24:27	RW	TX_LINK0_LANE06_CONTROL: Transmit lane control.
28:31	RW	TX_LINK0_LANE07_CONTROL: Transmit lane control.
32:35	RW	TX_LINK0_LANE08_CONTROL: Transmit lane control.
36:39	RW	TX_LINK0_LANE09_CONTROL: Transmit lane control.
40:43	RW	TX_LINK0_LANE10_CONTROL: Transmit lane control.
44:47	RW	TX_LINK0_LANE11_CONTROL: Transmit lane control.
48:59	ROX	TX_LINK0_LANE_FAILED: Bit per lane. When 1, the lane is bad as indicated by the other side.
60:63	RO	constant = 0b0000

Register Name	Power Bus OLL Link 1 Transmit Lane Control Register
Mnemonic	PB.IOO.LL0.IOOL_LINK1_TX_LANE_CONTROL
Address	0000000009010811 (SCOM)
Description	Processor bus OLL link0 transmit lane control register

Bits	SCOM	Field Mnemonic: Description
0:3	RW	TX_LINK1_LANE00_CONTROL: Transmit lane control.
4:7	RW	TX_LINK1_LANE01_CONTROL: Transmit lane control.
8:11	RW	TX_LINK1_LANE02_CONTROL: Transmit lane control.
12:15	RW	TX_LINK1_LANE03_CONTROL: Transmit lane control.
16:19	RW	TX_LINK1_LANE04_CONTROL: Transmit lane control.
20:23	RW	TX_LINK1_LANE05_CONTROL: Transmit lane control.
24:27	RW	TX_LINK1_LANE06_CONTROL: Transmit lane control.
28:31	RW	TX_LINK1_LANE07_CONTROL: Transmit lane control.
32:35	RW	TX_LINK1_LANE08_CONTROL: Transmit lane control.
36:39	RW	TX_LINK1_LANE09_CONTROL: Transmit lane control.
40:43	RW	TX_LINK1_LANE10_CONTROL: Transmit lane control.
44:47	RW	TX_LINK1_LANE11_CONTROL: Transmit lane control.
48:59	ROX	TX_LINK1_LANE_FAILED: Bit per lane. When 1, the lane is bad as indicated by other side.

Bits	SCOM	Field Mnemonic: Description
60:63	RO	constant = 0b0000

Register Name	Power Bus OLL Link 0 Receive Lane Control Register
Mnemonic	PB.IOO.LL0.IOOL_LINK0_RX_LANE_CONTROL
Address	0000000009010812 (SCOM)
Description	Processor bus OLL link0 receive lane control register

Bits	SCOM	Field Mnemonic: Description
0:11	RW	RX_LINK0_LANE_DISABLED: Bit per lane. When 1, the lane is disabled (all data ignored).
12:23	RW	RX_LINK0_LANE_BRINGUP: Bit per lane. When 1, the lane is not used functionally (can lock only).
24:35	RW	RX_LINK0_LANE_SPARED: Bit per lane. When 1, the lane is marked bad.
36:47	ROX	RX_LINK0_LANE_LOCKED: Bit per lane. When 1, the lane is block and scrambling locked.
48:59	ROX	RX_LINK0_LANE_FAILED: Bit per lane. When 1, the lane failed training.
60:63	RO	constant = 0b0000

Register Name	Power Bus OLL Link 1 Receive Lane Control Register
Mnemonic	PB.IOO.LL0.IOOL_LINK1_RX_LANE_CONTROL
Address	0000000009010813 (SCOM)
Description	Processor bus OLL link0 receive lane control register

Bits	SCOM	Field Mnemonic: Description
0:11	RW	RX_LINK1_LANE_DISABLED: Bit per lane. When 1, the lane is disabled (all data ignored).
12:23	RW	RX_LINK1_LANE_BRINGUP: Bit per lane. When 1, the lane is not used functionally (can lock only).
24:35	RW	RX_LINK1_LANE_SPARED: Bit per lane. When 1, the lane is marked bad.
36:47	ROX	RX_LINK1_LANE_LOCKED: Bit per lane. When 1, the lane is block and scrambling locked.
48:59	ROX	RX_LINK1_LANE_FAILED: Bit per lane. When 1, the lane failed training.
60:63	RO	constant = 0b0000

Register Name	Power Bus OLL Link 0 Information Register
Mnemonic	PB.IOO.LL0.IOOL_LINK0_INFO
Address	0000000009010814 (SCOM)
Description	Processor bus OLL link0 information register

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	LINK0_MAX_TIMEOUT: Maximum value reached by timeout counter.
16	ROX	LINK0_FRAME_CAP_VALID: When 1, error capture is valid.
17	ROX	LINK0_FRAME_CAP_INST: Array instance.
18:23	ROX	LINK0_FRAME_CAP_ADDR: Array address of captured error.
24:31	ROX	LINK0_FRAME_CAP_SYN: Syndrome of captured error.

Bits	SCOM	Field Mnemonic: Description
32	ROX	LINK0_REPLAY_CAP_VALID: When 1, error capture is valid.
33:34	ROX	LINK0_REPLAY_CAP_INST: Array instance.
35:43	ROX	LINK0_REPLAY_CAP_ADDR: Array address of captured error.
44:51	ROX	LINK0_REPLAY_CAP_SYN: Syndrome of captured error.
52	ROX	LINK0_ACK_FIFO_CAP_VALID: When 1, error capture is valid.
53:54	RO	constant = 0b00
55:63	ROX	LINK0_ACK_FIFO_CAP_ADDR: Array address of captured error.

Register Name	**Power Bus OLL Link 1 Information Register**
Mnemonic	PB.IOO.LL0.IOOL_LINK1_INFO
Address	0000000009010815 (SCOM)
Description	Processor bus OLL link0 information register

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	LINK1_MAX_TIMEOUT: Maximum value reached by timeout counter.
16	ROX	LINK1_FRAME_CAP_VALID: When 1, error capture is valid.
17	ROX	LINK1_FRAME_CAP_INST: Array instance.
18:23	ROX	LINK1_FRAME_CAP_ADDR: Array address of captured error.
24:31	ROX	LINK1_FRAME_CAP_SYN: Syndrome of captured error.
32	ROX	LINK1_REPLAY_CAP_VALID: When 1, error capture is valid.
33:34	ROX	LINK1_REPLAY_CAP_INST: Array instance.
35:43	ROX	LINK1_REPLAY_CAP_ADDR: Array address of captured error.
44:51	ROX	LINK1_REPLAY_CAP_SYN: Syndrome of captured error.
52	ROX	LINK1_ACK_FIFO_CAP_VALID: When 1, error capture is valid.
53:54	RO	constant = 0b00
55:63	ROX	LINK1_ACK_FIFO_CAP_ADDR: Array address of captured error.

Register Name	**Power Bus OLL Link 0 Error Status Register**
Mnemonic	PB.IOO.LL0.IOOL_LINK0_ERROR_STATUS
Address	0000000009010816 (SCOM)
Description	Processor bus OLL link0 error status register

Bits	SCOM	Field Mnemonic: Description
0	WOX	LINK0_RESET_KEEPER: Reset_keeper for link0 error status register.
1:3	ROX	LINK0_ERROR_STATUS_CE: c_err_rpt for correctable array errors.
4:7	RO	constant = 0b0000
8:9	ROX	LINK0_ERROR_STATUS_UE: c_err_rpt for uncorrectable array errors.
10:11	RO	constant = 0b00
12:13	ROX	LINK0_ERROR_STATUS_OSC: c_err_rpt for oscillator errors.

Bits	SCOM	Field Mnemonic: Description
14:15	RO	constant = 0b00
16:17	ROX	LINK0_ERROR_STATUS_TRAIN: c_err_rpt for training errors.
18:23	RO	constant = 0b000000
24:34	ROX	LINK0_ERROR_STATUS_UNRECOV: c_err_rpt for unrecoverable errors.
35:39	RO	constant = 0b00000
40:55	ROX	LINK0_ERROR_STATUS_INTERNAL: c_err_rpt for internal errors.
56:57	RO	constant = 0b00
58:61	ROX	LINK0_ERROR_STATUS_INTERNAL: c_err_rpt for internal errors.
62:63	RO	constant = 0b00

Register Name	Power Bus OLL Link 1 Error Status Register
Mnemonic	PB.IOO.LL0.IOOL_LINK1_ERROR_STATUS
Address	0000000009010817 (SCOM)
Description	Processor bus OLL link1 error status register

Bits	SCOM	Field Mnemonic: Description
0	WOX	LINK1_RESET_KEEPER: Reset_keeper for link1 error status register.
1:3	ROX	LINK1_ERROR_STATUS_CE: c_err_rpt for correctable array errors.
4:7	RO	constant = 0b0000
8:9	ROX	LINK1_ERROR_STATUS_UE: c_err_rpt for uncorrectable array errors.
10:11	RO	constant = 0b00
12:13	ROX	LINK1_ERROR_STATUS_OSC: c_err_rpt for oscillator errors.
14:15	RO	constant = 0b00
16:17	ROX	LINK1_ERROR_STATUS_TRAIN: c_err_rpt for training errors.
18:23	RO	constant = 0b000000
24:34	ROX	LINK1_ERROR_STATUS_UNRECOV: c_err_rpt for unrecoverable errors.
35:39	RO	constant = 0b00000
40:55	ROX	LINK1_ERROR_STATUS_INTERNAL: c_err_rpt for internal errors.
56:57	RO	constant = 0b00
58:61	ROX	LINK1_ERROR_STATUS_INTERNAL: c_err_rpt for internal errors.
62:63	RO	constant = 0b00

Register Name	Power Bus OLL Replay Threshold Register
Mnemonic	PB.IOO.LL0.IOOL_REPLAY_THRESHOLD
Address	0000000009010818 (SCOM)
Description	Processor bus OLL replay threshold register

Bits	SCOM	Field Mnemonic: Description
0:3	RW	THRESH_REPLAY_TB_SEL: Replay threshold Timebase select.

Bits	SCOM	Field Mnemonic: Description
4:7	RW	THRESH_REPLAY_TAP_SEL: Replay threshold tap select.
8:10	RW	THRESH_REPLAY_ENABLE: Replay threshold error enable.
11:25	RW	THRESH_REPLAY_UNUSED1: Spare bits.
26	RWX	THRESH_REPLAY_LINK0_CLEAR: Replay threshold counter clear.
27	RWX	THRESH_REPLAY_LINK1_CLEAR: Replay threshold counter clear.
28	RW	THRESH_REPLAY_DIS_TB_CLEAR: Threshold disable Timebase clear.
29	RW	THRESH_REPLAY_DIS_TAP_CLEAR: Threshold disable tap clear.
30	RW	THRESH_REPLAY_DIS_TAP_STOP: Threshold disable tap stop.
31	RW	THRESH_REPLAY_UNUSED2: Spare bits.
32:47	ROX	THRESH_REPLAY_LINK0_COUNT: Replay threshold count.
48:63	ROX	THRESH_REPLAY_LINK1_COUNT: Replay threshold count.

Register Name	Power Bus OLL SL ECC Threshold Register
Mnemonic	PB.IOO.LL0.IOOL_SL_ECC_THRESHOLD
Address	0000000009010819 (SCOM)
Description	Processor bus OLL SL ECC Threshold register

Bits	SCOM	Field Mnemonic: Description
0:3	RW	THRESH_SL_ECC_TB_SEL: SL ECC threshold Timebase select.
4:7	RW	THRESH_SL_ECC_TAP_SEL: SL ECC threshold tap select.
8:9	RW	THRESH_SL_ECC_ENABLE: SL ECC threshold error enable.
10:25	RW	THRESH_SL_ECC_UNUSED1: Spare bits.
26	RWX	THRESH_SL_ECC_LINK0_CLEAR: SL ECC threshold counter clear.
27	RWX	THRESH_SL_ECC_LINK1_CLEAR: SL ECC threshold counter clear.
28	RW	THRESH_SL_ECC_DIS_TB_CLEAR: Threshold disable Timebase clear.
29	RW	THRESH_SL_ECC_DIS_TAP_CLEAR: Threshold disable tap clear.
30	RW	THRESH_SL_ECC_DIS_TAP_STOP: Threshold disable tap stop.
31	RW	THRESH_SL_ECC_UNUSED2: Spare bits.
32:47	ROX	THRESH_SL_ECC_LINK0_COUNT: SL ECC threshold count.
48:63	ROX	THRESH_SL_ECC_LINK1_COUNT: SL ECC threshold count.

Register Name	Power Bus OLL Retrain Threshold Register
Mnemonic	PB.IOO.LL0.IOOL_RETRAIN_THRESHOLD
Address	000000000901081A (SCOM)
Description	Processor bus OLL retrain threshold register

Bits	SCOM	Field Mnemonic: Description
0:3	RW	THRESH_RETRAIN_TB_SEL: Retrain threshold Timebase select.
4:7	RW	THRESH_RETRAIN_TAP_SEL: Retrain threshold tap select.

Bits	SCOM	Field Mnemonic: Description
8:16	RW	THRESH_RETRAIN_ENABLE: Retrain threshold error enable.
17:25	RW	THRESH_RETRAIN_UNUSED1: Spare bits.
26	RWX	THRESH_RETRAIN_LINK0_CLEAR: Retrain threshold counter clear.
27	RWX	THRESH_RETRAIN_LINK1_CLEAR: Retrain threshold counter clear.
28	RW	THRESH_RETRAIN_DIS_TB_CLEAR: Threshold disable Timebase clear.
29	RW	THRESH_RETRAIN_DIS_TAP_CLEAR: Threshold disable tap clear.
30	RW	THRESH_RETRAIN_DIS_TAP_STOP: Threshold disable tap stop.
31	RW	THRESH_RETRAIN_UNUSED2: Spare bits.
32:47	ROX	THRESH_RETRAIN_LINK0_COUNT: Retrain threshold count.
48:63	ROX	THRESH_RETRAIN_LINK1_COUNT: Retrain threshold count.

Register Name	**Power Bus OLL Error Injection LFSR Register**
Mnemonic	PB.IOO.LL0.IOOL_ERR_INJ_LFSR
Address	000000000901081B (SCOM)
Description	Processor bus OLL error injection LFSR register

Bits	SCOM	Field Mnemonic: Description
0:60	RWX	ERR_INJ_LFSR: Error injection LFSR.
61:63	RO	constant = 0b000

Register Name	**Power Bus OLL Performance Trace Configuration Register**
Mnemonic	PB.IOO.LL0.IOOL_PERF_TRACE_CONFIG
Address	000000000901081C (SCOM)
Description	Processor bus OLL performance monitor and trace configuration register

Bits	SCOM	Field Mnemonic: Description
0:1	RW	CONFIG_ENABLE_PERF_0: Performance counter enable.
2:3	RW	CONFIG_ENABLE_PERF_1: Performance counter enable.
4:5	RW	CONFIG_ENABLE_PERF_2: Performance counter enable.
6:7	RW	CONFIG_ENABLE_PERF_3: Performance counter enable.
8:9	RW	CONFIG_ENABLE_PERF_4: Performance counter enable.
10:11	RW	CONFIG_ENABLE_PERF_5: Performance counter enable.
12:13	RW	CONFIG_ENABLE_PERF_6: Performance counter enable.
14:15	RW	CONFIG_ENABLE_PERF_7: Performance counter enable.
16:17	RW	CONFIG_PERF_SIZE_0: Performance counter size.
18:19	RW	CONFIG_PERF_SIZE_1: Performance counter size.
20:21	RW	CONFIG_PERF_SIZE_2: Performance counter size.
22:23	RW	CONFIG_PERF_SIZE_3: Performance counter size.
24:25	RW	CONFIG_PERF_SIZE_4: Performance counter size.

Bits	SCOM	Field Mnemonic: Description
26:27	RW	CONFIG_PERF_SIZE_5: Performance counter size.
28:29	RW	CONFIG_PERF_SIZE_6: Performance counter size.
30:31	RW	CONFIG_PERF_SIZE_7: Performance counter size.
32	RW	CONFIG_PMULET_FREEZE_MODE: PMUlet freeze mode: 0 = Freeze-on-full 1 = Free run
33	RW	CONFIG_COMMON_FREEZE_MODE: Common freeze mode: 0 = Independent per PMUlet. 1 = Any counter full freezes all.
34	RW	CONFIG_PERF_RESET_MODE: PMUlet reset mode: 0 = Reset on read. 1 = Reset on write.
35	RW	CONFIG_PERFTRACE_ENABLE: Performance trace enable. Multiplexer performance trace data onto trace bus.
36	RW	CONFIG_PERFTRACE_FIXED_WINDOW: Performance trace fixed window mode. Take a sample every 255 or 255 $\times$ 128 cycles.
37	RW	CONFIG_PERFTRACE_PRESCALE: Performance trace prescale mode. Wide-angle view; performance counts are prescaled by 128.
38:39	RW	CONFIG_PERFTRACE_MODE: Performance trace input selection.
40:51	RW	CONFIG_TRACE_CONFIG_0: Selection for trace bus bits 0:43.
52:63	RW	CONFIG_TRACE_CONFIG_1: Selection for trace bus bits 44:87.

Register Name	**Power Bus OLL Performance Monitor Selection Register**
Mnemonic	PB.IOO.LL0.IOOL_PERF_SEL_CONFIG
Address	000000000901081D (SCOM)
Description	Processor bus OLL performance monitor selection register

Bits	SCOM	Field Mnemonic: Description
0:7	RW	CONFIG_PERF_SELECT_0: Selection performance counter.
8:15	RW	CONFIG_PERF_SELECT_1: Selection performance counter.
16:23	RW	CONFIG_PERF_SELECT_2: Selection performance counter.
24:31	RW	CONFIG_PERF_SELECT_3: Selection performance counter.
32:39	RW	CONFIG_PERF_SELECT_4: Selection performance counter.
40:47	RW	CONFIG_PERF_SELECT_5: Selection performance counter.
48:55	RW	CONFIG_PERF_SELECT_6: Selection performance counter.
56:63	RW	CONFIG_PERF_SELECT_7: Selection performance counter.

Register Name	**Power Bus OLL Performance Monitor Counter 0 Register**
Mnemonic	PB.IOO.LL0.IOOL_PERF_COUNTERS_0
Address	000000000901081E (SCOM)
Description	Processor bus OLL performance monitor counter register 0

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRREG	PERFMON_COUNTER_0: Performance counter 16 MSB.
16:31	RWX_WCLRREG	PERFMON_COUNTER_1: Performance counter 16 MSB.
32:47	RWX_WCLRREG	PERFMON_COUNTER_2: Performance counter 16 MSB.
48:63	RWX_WCLRREG	PERFMON_COUNTER_3: Performance counter 16 MSB.

Register Name	Power Bus OLL Performance Monitor Counter 1 Register
Mnemonic	PB.IOO.LL0.IOOL_PERF_COUNTERS_1
Address	000000000901081F (SCOM)
Description	Processor bus OLL performance monitor counter register 1

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRREG	PERFMON_COUNTER_4: Performance counter 16 MSB.
16:31	RWX_WCLRREG	PERFMON_COUNTER_5: Performance counter 16 MSB.
32:47	RWX_WCLRREG	PERFMON_COUNTER_6: Performance counter 16 MSB.
48:63	RWX_WCLRREG	PERFMON_COUNTER_7: Performance counter 16 MSB.

Register Name	Power Bus OLL Performance Monitor Counter LSB 0 Register
Mnemonic	PB.IOO.LL0.IOOL_PERF_COUNT_LSB_0
Address	0000000009010820 (SCOM)
Description	Processor bus OLL performance monitor counter LSB register 0

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved.

Register Name	Power Bus OLL Performance Monitor Counter LSB 1 Register
Mnemonic	PB.IOO.LL0.IOOL_PERF_COUNT_LSB_1
Address	0000000009010821 (SCOM)
Description	Processor bus OLL Performance Monitor Couter LSB register 1

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved.

Register Name	Power Bus OLL Link 0 Syndrome Capture Register
Mnemonic	PB.IOO.LL0.IOOL_LINK0_SYN_CAPTURE
Address	0000000009010822 (SCOM)
Description	Processor bus OLL link0 syndrome capture register

Bits	SCOM	Field Mnemonic: Description
0:35	RWX	LINK0_LINK_CAP_CRC_SYN: CRC syndrome for captured link error.

Bits	SCOM	Field Mnemonic: Description
36:43	RWX	LINK0_LINK_CAP_SLECC_SYN0: SL ECC syndrome for captured link error.
44:51	RWX	LINK0_LINK_CAP_SLECC_SYN1: SL ECC syndrome for captured link error.
52:59	RWX	LINK0_LINK_CAP_SLECC_SYN2: SL ECC syndrome for captured link error.
60:63	RWX	LINK0_LINK_CAP_CRC_LANE: CRC lane from syndrome decode.

Register Name	Power Bus OLL Link 1 Syndrome Capture Register
Mnemonic	PB.IOO.LL0.IOOL_LINK1_SYN_CAPTURE
Address	0000000009010823 (SCOM)
Description	Processor bus OLL link1 syndrome capture register

Bits	SCOM	Field Mnemonic: Description
0:35	RWX	LINK1_LINK_CAP_CRC_SYN: CRC syndrome for captured link error.
36:43	RWX	LINK1_LINK_CAP_SLECC_SYN0: SL ECC syndrome for captured link error.
44:51	RWX	LINK1_LINK_CAP_SLECC_SYN1: SL ECC syndrome for captured link error.
52:59	RWX	LINK1_LINK_CAP_SLECC_SYN2: SL ECC syndrome for captured link error.
60:63	RWX	LINK1_LINK_CAP_CRC_LANE: CRC lane from syndrome decode.

Register Name	Power Bus OLL Link 0 EDPL Status Register
Mnemonic	PB.IOO.LL0.IOOL_LINK0_EDPL_STATUS
Address	0000000009010824 (SCOM)
Description	Processor bus OLL link0 EDPL status register

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	LINK0_EDPL_ERROR_COUNT_0: Count of EDPL errors.
4:7	ROX	LINK0_EDPL_ERROR_COUNT_1: Count of EDPL errors.
8:11	ROX	LINK0_EDPL_ERROR_COUNT_2: Count of EDPL errors.
12:15	ROX	LINK0_EDPL_ERROR_COUNT_3: Count of EDPL errors.
16:19	ROX	LINK0_EDPL_ERROR_COUNT_4: Count of EDPL errors.
20:23	ROX	LINK0_EDPL_ERROR_COUNT_5: Count of EDPL errors.
24:27	ROX	LINK0_EDPL_ERROR_COUNT_6: Count of EDPL errors.
28:31	ROX	LINK0_EDPL_ERROR_COUNT_7: Count of EDPL errors.
32:35	ROX	LINK0_EDPL_ERROR_COUNT_8: Count of EDPL errors.
36:39	ROX	LINK0_EDPL_ERROR_COUNT_9: Count of EDPL errors.
40:43	ROX	LINK0_EDPL_ERROR_COUNT_10: Count of EDPL errors.
44:47	ROX	LINK0_EDPL_ERROR_COUNT_11: Count of EDPL errors.
48:63	RO	constant = 0b0000000000000000

Register Name	Power Bus OLL Link 1 EDPL Status Register
Mnemonic	PB.IOO.LL0.IOOL_LINK1_EDPL_STATUS
Address	0000000009010825 (SCOM)
Description	Processor bus OLL link1 EDPL status register

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	LINK1_EDPL_ERROR_COUNT_0: Count of EDPL errors.
4:7	ROX	LINK1_EDPL_ERROR_COUNT_1: Count of EDPL errors.
8:11	ROX	LINK1_EDPL_ERROR_COUNT_2: Count of EDPL errors.
12:15	ROX	LINK1_EDPL_ERROR_COUNT_3: Count of EDPL errors.
16:19	ROX	LINK1_EDPL_ERROR_COUNT_4: Count of EDPL errors.
20:23	ROX	LINK1_EDPL_ERROR_COUNT_5: Count of EDPL errors.
24:27	ROX	LINK1_EDPL_ERROR_COUNT_6: Count of EDPL errors.
28:31	ROX	LINK1_EDPL_ERROR_COUNT_7: Count of EDPL errors.
32:35	ROX	LINK1_EDPL_ERROR_COUNT_8: Count of EDPL errors.
36:39	ROX	LINK1_EDPL_ERROR_COUNT_9: Count of EDPL errors.
40:43	ROX	LINK1_EDPL_ERROR_COUNT_10: Count of EDPL errors.
44:47	ROX	LINK1_EDPL_ERROR_COUNT_11: Count of EDPL errors.
48:63	RO	constant = 0b0000000000000000

Register Name	Power Bus OLL Link 0 Link Quality Status Register
Mnemonic	PB.IOO.LL0.IOOL_LINK0_QUALITY
Address	0000000009010826 (SCOM)
Description	Processor bus OLL link0 link quality status register

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:11	ROX	LINK0_TX_BW: Measure of transmit bandwidth.
12	RO	constant = 0b0
13:23	ROX	LINK0_RX_BW: Measure of receive bandwidth.
24	RO	constant = 0b0
25:47	ROX	LINK0_ERROR_RATE: Measure of received error rate.
48:63	RO	constant = 0b0000000000000000

Register Name	Power Bus OLL Link 1 Link Quality Status Register
Mnemonic	PB.IOO.LL0.IOOL_LINK1_QUALITY
Address	0000000009010827 (SCOM)
Description	Processor bus OLL link1 link quality status register

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:11	ROX	LINK1_TX_BW: Measure of transmit bandwidth.
12	RO	constant = 0b0
13:23	ROX	LINK1_RX_BW: Measure of receive bandwidth.
24	RO	constant = 0b0
25:47	ROX	LINK1_ERROR_RATE: Measure of received error rate.
48:63	RO	constant = 0b0000000000000000

Register Name	Power Bus OLL Status Register
Mnemonic	PB.IOO.LL0.IOOL_DLL_STATUS
Address	0000000009010828 (SCOM)
Description	Processor bus OLL status register

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b0000
4:7	ROX	LINK0_CURRENT_STATE: Current state of initialization/training state machine.
8:11	RO	constant = 0b0000
12:15	ROX	LINK0_PRIOR_STATE: Prior state of initialization/training state machine.
16	ROX	LINK0_OPTICS_RST_B: Value of driven tp_io_optics_rst_b.
17	ROX	LINK0_OPTICS_IRQ: Value of received io_tp_op_irq.
18	ROX	LINK0_TRAINING: Link is currently training.
19:23	ROX	LINK0_MAX_PKT_TIMER: Maximum value reached by packet delay counter.
24:27	RO	constant = 0b0000
28:31	ROX	LINK1_CURRENT_STATE: Current state of initialization/training state machine.
32:35	RO	constant = 0b0000
36:39	ROX	LINK1_PRIOR_STATE: Prior state of initialization/training state machine.
40	ROX	LINK1_OPTICS_RST_B: Value of driven tp_io_optics_rst_b.
41	ROX	LINK1_OPTICS_IRQ: Value of received io_tp_op_irq.
42	ROX	LINK1_TRAINING: Link is currently training.
43:47	ROX	LINK1_MAX_PKT_TIMER: Maximum value reached by packet delay counter.
48:63	RO	constant = 0b0000000000000000

Register Name	Power Bus OLL Link x Error Status Register
Mnemonic	PB.IOO.LL0.IOOL_LINKX_ERROR_STATUS
Address	0000000009010829 (SCOM)
Description	Processor bus OLL linkx error status register

Bits	SCOM	Field Mnemonic: Description
0	WOX	LINKX_RESET_KEEPER: Reset_keeper for link0 error status register.

Bits	SCOM	Field Mnemonic: Description
1:5	ROX	LINKX_ERROR_STATUS: c_err_rpt for link x NPU errors.
6:63	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000

Register Name	Normal SCOM Mode Register
Mnemonic	IOO0.IOO_CPLT.BUSCTL.SCOM.SCOM_MODE_PB
Address	0000000009010C20 (SCOM)
Description	Normal SCOM mode register

Bits	SCOM	Field Mnemonic: Description
0	RWX	GCR_TEST_MODE: GCR test mode. Puts register logic into GCR test mode, which allows all RW registers to be read and written by diagnostic code to verify all register accesses. This mode gates off both logic inputs to the registers as well as the outputs from the logic. The outputs are gated to their scan flush value.
1	RWX	ENABLE_GCR_OFL_BUFF: Enables a second GCR overflow buffer. The default is one.
2	RWX	IORESET_HARD_BUS0: I/O hard reset per-bus and GCR reset.
3	RWX	MMIO_PG_REG_ACCESS: MMIO PG register access is blocked by default. Setting this bit high grants MMIO access to the PG registers.
4:7	RWX	SCOM_MODE_PB_SPARES1: SCOM mode register spares.
8:10	RWX	GCR_HANG_DET_SEL: GCR hang detect threshold select.
11	ROX	GCR_BUFFER_ENABLED_RO_SIGNAL: Flag indicating that the extra GCR buffer is active, if the SCOM GCR enable buffer is off it means the hang threshold was reached.
12	RWX	GCR_HANG_ERROR_MASK: Mask for GCR hang error when a second buffer is enabled.
13	RWX	GCR_HANG_ERROR_INJ: Inject for GCR hang error.
14	RWX	PPE_GCR_MODE: GCR test mode/put register logic into GCR test mode which allows all RW registers to be read and written by diagnostic code to verify all register accesses. This mode gates off both logic inputs to the registers as well as the outputs from the logic. The outputs are gated to their scan flush value.
15:22	RWX	CHAN_FAIL_MASK: Channel fail mask.
23:30	RWX	SCOM_MODE_PB_SPARES2: SCOM mode register spares.
31:63	RO	constant = 0b000000000000000000000000000000000

Register Name	PPE Control Register
Mnemonic	IOO0.IOO_PPE.SCOM_PPE_CNTL
Address	0000000009011060 (SCOM)
Description	PPE Misc Control Register

Bits	SCOM	Field Mnemonic: Description
0	RW	SCOM_PPE_IORESET: Reset I/O-specific logic in the PPE macro. (This does not actually reset the PPE or ARB logic.)
1	RW	SCOM_PPE_PDWN: Power down I/O-specific logic in the PPE macro. (This does not actually reset the PPE or ARB logic.)
2	RW	SCOM_PPE_INTERRUPT: Manually force an external interrupt in the PPE.
3	RW	SCOM_PPE_ARB_ECC_INJECT_ERR: Force an ECC error in the memory arbiter.
4:15	RW	SCOM_PPE_SPARES: PPE Miscellaneous control spares.

Bits	SCOM	Field Mnemonic: Description
16:31	RO	constant = 0b0000000000000000

Register Name	PPE Work 1 Register
Mnemonic	IOO0.IOO_PPE.SCOM_PPE_WORK_REG1
Address	0000000009011061 (SCOM)
Description	PPE Work Register 1

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	SCOM_PPE_WORK1: PPE work register field 1.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	PPE Work 2 Register
Mnemonic	IOO0.IOO_PPE.SCOM_PPE_WORK_REG2
Address	0000000009011062 (SCOM)
Description	PPE Work Register 2

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	SCOM_PPE_WORK2: PPE work register field 2.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	PPE Flag Register
Mnemonic	IOO0.IOO_PPE.SCOM_PPE_FLAGS
Address	0000000009011063 (SCOM) 0000000009011064 (SCOM1) 0000000009011065 (SCOM2)
Description	PPE Flag Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:15	RWX	WOX_OR	WOX_CLEAR	SCOM_PPE_FLAGS_FIELD: PPE flags register field.
16:31	RO	RO	RO	constant = 0b0000000000000000

Register Name	Synchronous Configuration Register
Mnemonic	TP.TCOB0.OB.SYNC_CONFIG
Address	0000000009030000 (SCOM)
Description	configuration of CC counters

Bits	SCOM	Field Mnemonic: Description
0:3	RW	SYNC_PULSE_DELAY: Delay incoming synchronous pulse. The default is 8 latches, including asynchronous. 0000 = Delay by 8 latches (default). 0001 = Delay by 2 latches. 0010 = Delay by 3 latches. 0011 = Delay by 4 latches. 0100 = Delay by 5 latches. 0101 = Delay by 6 latches. 0110 = Delay by 7 latches. 0111 = Delay by 8 latches. 1000 = Delay by 9 latches. 1001 = Delay by 10 latches. 1010 = Delay by 11 latches. 1011 = Delay by 12 latches. 1100 = Delay by 13 latches. 1101 = Delay by 14 latches. 1110 = Delay by 15 latches. 1111 = Delay by 16 latches.
4	RW	LISTEN_TO_SYNC_PULSE_DIS: Disable phase counter synchronization by sync_pulse signal (default is enabled). **Note:** When listen_to_sync is enabled, the chiplet becomes corrupted for 200 cycles.
5	RW	SYNC_PULSE_INPUT_SEL: The default is 0. When set to 1, the alternative input of the sync_pulse will be used. **Note:** When toggling the input select, the chiplet becomes corrupted for 200 cycles.
6	RW	USE_SYNC_FOR_SCAN: When set, use OPCG initial alignment for scan requests.
7	RW	CLEAR_CHIPLET_IS_ALIGNED: This bit clears the chiplet_is_aligned bit. See the Chiplet Status Register.
8	RW	UNIT_REGION_CLKCMD_ENABLE: Enable the unit interface to start or stop one dedicated region. Used for POWER9 cache/core.
9	RW	DISABLE_PCB_ITR: Disable interrupt generation within CC. Interrupt sent on each HLD event.
10	RW	ENABLE_VITL_ALIGN_CHECK: Enable the VITL align check to compare alignment of incoming synchronous pulse with 2:1 VITL LCB.
11	RW	SYNC_PULSE_OUT_DIS: Disables sync_pulse output when set to 1. The master chiplet will no longer send synchronous pulses to slave chiplets.
12:19	RW	UNUSED1219: Unused.

Register Name	**OPCG Alignment Register**
Mnemonic	TP.TCOB0.OB.OPCG_ALIGN
Address	0000000009030001 (SCOM)
Description	OPCG ALIGN

Bits	SCOM	Field Mnemonic: Description
0:3	RW	INOP_ALIGN: INOP phase alignment: 0 = None 1 = 2:1 2 = 3:1 3 = 4:1 4 = 6:1 5 = 8:1 6 = 12:1 7 = 16:1 8 = 24:1 9-15 = 48:1
4:7	RW	SNOP_ALIGN: SNOP phase alignment: 0 = None 1 = 2:1 2 = 3:1 3 = 4:1 4 = 6:1 5 = 8:1 6 = 12:1 7 = 16:1 8 = 24:1 9-15 = 48:1
8:11	RW	ENOP_ALIGN: ENOP phase alignment: 0 = None 1 = 2:1 2 = 3:1 3 = 4:1 4 = 6:1 5 = 8:1 6 = 12:1 7 = 16:1 8 = 24:1 9-15 = 48:1
12:19	RW	INOP_WAIT: INOP cycle delay (0-255).
20:31	RW	SNOP_WAIT: SNOP cycle delay (0-4095).
32:39	RW	ENOP_WAIT: ENOP cycle delay (0-255).
40	RW	INOP_FORCE_SG: INOP: Set SG high during INOP.
41	RW	SNOP_FORCE_SG: SNOP: Set SG high during SNOP.
42	RW	ENOP_FORCE_SG: ENOP: Set SG high during ENOP (including LOOP phase).
43	RW	NO_WAIT_ON_CLK_CMD: 0 = A clock change request will first wait the OPCG_WAIT cycles. 1 = A clock change request will not wait, when not in flush.
44:45	RW	ALIGN_SOURCE_SELECT: 0 = Use inopa setting from opcg_reg0. 1 = Use rising edge of synchronous pulse. 2 = Use unit0_sync_lvl to align (for AVP: refresh0). 3 = Use unit1_sync_lvl to align (for AVP: refresh1).
46	RW	UNUSED46: Unused.

Bits	SCOM	Field Mnemonic: Description
47:51	RW	SCAN_RATIO: Scan ratio. The default is 4:1 = 00011. 0 to 15 = (n+1):1 16 = 24:1 17 = 32:1 18 = 48:1 19 = 64:1 20 = 128:1
52:63	RW	OPCG_WAIT_CYCLES: Old PAD value; delay at the beginning and end of the OPCG run, to allow DC signals to be there at the right time (0-4095). The default is 0x020. **Note:** Must be higher than plat depth.

Register Name	OPCG Control 0 Register
Mnemonic	TP.TCOB0.OB.OPCG_REG0
Address	0000000009030002 (SCOM)
Description	OPCG Control Register 0

Bits	SCOM	Field Mnemonic: Description
0	RW	RUNN_MODE: 0 = BIST-mode; used for LBIST. 1 = RUNN-mode; used for ABIST/IOBIST.
1	RWX	OPCG_GO: Start OPCG. The bit is cleared when OPCG completes. Poll for opcg_done in the Chiplet Status Register.
2	RWX	RUN_SCAN0: Run scan0 (overrides all BIST mode settings but the scan_ratio). Starts a scan0 run, and the bit is cleared when OPCG is done. Poll for opcg_done in the Chiplet Status Register.
3	RW	SCAN0_MODE: Sets PRPGs in scan0_mode but does not run the automatic scan0 sequence.
4	RWX	OPCG_IN_SLAVE_MODE: When selected, OPCG waits for the master chiplet to get started. When Keep_MS_Mode is 0, SLAVE_MODE is cleared after the incoming trigger.
5	RWX	OPCG_IN_MASTER_MODE: When selected, OPCG sends out a trigger to all slave chiplets. When Keep_MS_Mode is 0, MASTER_MODE is cleared after sending out one master trigger.
6	RW	KEEP_MS_MODE: When set to 1, OPCG in master and slave mode bits are not cleared after one incoming OPCG trigger. The default is to clear master and slave mode bits.
7	RW	TRIGGER_OPCG_ON_UNIT0_SYNC_LVL: Unit pin used for AVP can trigger OPCG (unit0_sync_lvl).
8	RW	TRIGGER_OPCG_ON_UNIT1_SYNC_LVL: Unit pin used for AVP can trigger OPCG (unit1_sync_lvl).
9	RWX	RUN_CHIPLET_SCAN0: Run scan0 on all regions and types; clears the chiplet at all regions and types.
10	RWX	RUN_CHIPLET_SCAN0_NO_PLL: Run scan0 on all regions and types; clears the chiplet at all exclude-PLL regions. PLL can continue to run.
11	RW	RUN_OPCG_ON_UPDATE_DR: Start the OPCG engine when scan update (update_dr) is received (set pulse) Cronus requires this bit to be set at 1 for a set pulse WRITE.
12	RW	RUN_OPCG_ON_CAPTURE_DR: Start the OPCG engine when scan update (capture_dr) is received (set pulse). Cronus requires this bit to be set at 1 for a set pulse READ.
13	RW	STOP_RUNN_ON_XSTOP: RUNN mode. Stops RUNN on checkstop.
14	RW	OPCG_STARTS_BIST: RUNN mode. The OPCG engine controls start_bist for ABIST or IOBIST (see the BIST Register).
15:20	RW	UNUSED1520: Unused.
21:63	RWX	LOOP_COUNT: Loop counter for LBIST and RUNN. write = Target value. read = Current counter value. Counts from 0 to the target value.

Register Name	OPCG Control 1 Register
Mnemonic	TP.TCOB0.OB.OPCG_REG1
Address	0000000009030003 (SCOM)
Description	OPCG Control Register 1

Bits	SCOM	Field Mnemonic: Description
0:11	RW	SCAN_COUNT: BIST mode: Channel scan count (s = 0-4095) RUNN-mode: start_bist match value (0:11)
12:23	RW	MISR_A_VAL: BIST mode: a value for MISR aperture RUNN-mode: start_bist match value (12:23)
24:35	RW	MISR_B_VAL: BIST mode: b value for MISR aperture RUNN-mode: start_bist match value (24:35)
36:47	RW	MISR_INIT_WAIT: BIST mode: delay MISR aperture; MISRs become active after this number of loops.
48	RW	OPCG_SUPPRESS_EVEN_CLK: OPCG creates only even, and not odd, clocks. Used for RUNN to create only one clock in fast domain. The default is 0.
49	RW	SCAN_CLK_USE_EVEN: Generate scan clock in even cycle instead of odd cycle. The default is 0 (odd cycle).
50:51	RW	UNUSED2: Unused.
52	RW	RTIM_THOLD_FORCE: Force rtim_thold low when not in test_dc mode (must be 0 at all times).
53	RW	DISABLE_ARY_CLK_DURING_FILL: LBIST and SCAN0. Prevent the firing of the ARY HLD bit during NSL fill.
54	RW	SG_HIGH_DURING_FILL: LBIST and SCAN0: Hold SG high during NSL fill.
55:56	RW	LBIST_SKITTER_CTL: BIST mode: 00 = Enable skitter during lbist_ip 01 = Enable skitter when misr_active; see misr_init_wait 10 = Skitter OPCG_GO mode; falling edge = start, rising edge = stop 11 = Unused
57	RW	MISR_MODE: BIST mode. MISR aperture mode (0: a-1 to b-1, 1: start to a and b to end).
58	RW	INFINITE_MODE: Infinite mode. RUNN and LBIST will run indefinitely and ignore the loop count.
59:63	RW	NSL_FILL_COUNT: BIST mode. NSL-fill count (0-31).

Register Name	OPCG Control 2 Register
Mnemonic	TP.TCOB0.OB.OPCG_REG2
Address	0000000009030004 (SCOM)
Description	OPCG Control Register 2

Bits	SCOM	Field Mnemonic: Description
0	RWX	OPCG_GO2: Start OPCG for broadcast sequences (start sequence).
1:3	RW	PRPG_WEIGHTING: prpg_activate: 1/2, 1/4, 1/8, 1/16, 1/2, 3/4, 7/8, 15/16.
4:15	RWX	PRPG_VALUE: Set to 0 to keep PRPG always on, else seed.
16:27	RW	PRPG_A_VAL: a value for PRPG aperture.

Bits	SCOM	Field Mnemonic: Description
28:39	RW	PRPG_B_VAL: b value for PRPG aperture.
40	RW	PRPG_MODE: PRPG aperture mode (0: a-1 to b-1, 1: start to a and b to end).
41:63	RW	UNUSED41_63: Unused.

Register Name	Scan Region and Type Register
Mnemonic	TP.TCOB0.OB.SCAN_REGION_TYPE
Address	0000000009030005 (SCOM)
Description	Scan Region and Type

Bits	SCOM	Field Mnemonic: Description
0	RWX	SYSTEM_FAST_INIT: Default is 0. When set to 1, the MASK bits in the CMSK chain govern which part will be scanned or scan0. MASK = 1: scan0. MASK = 0: Partial or scan chain.
1:2	RO	constant = 0b00
3	NCX	SCAN_REGION_VITL: Scan clock region VITL (Vital = Clock).
4	RWX	SCAN_REGION_PERV: Scan clock region perv (pervasive).
5	RWX	SCAN_REGION_UNIT1: Scan clock region pbiooa0 (PB).
6	RWX	SCAN_REGION_UNIT2: Scan clock region ioo0 (IOO).
7	RWX	SCAN_REGION_UNIT3: Scan clock region unused.
8	RWX	SCAN_REGION_UNIT4: Scan clock region unused.
9	RWX	SCAN_REGION_UNIT5: Scan clock region unused.
10	RWX	SCAN_REGION_UNIT6: Scan clock region unused.
11	RWX	SCAN_REGION_UNIT7: Scan clock region unused.
12	RWX	SCAN_REGION_UNIT8: Scan clock region unused.
13	RWX	SCAN_REGION_UNIT9: Scan clock region unused.
14	RWX	SCAN_REGION_UNIT10: Scan clock region pllioo0 (IOO).
15:47	RO	constant = 0b000000000000000000000000000000000
48	RW	SCAN_TYPE_FUNC: Scan chain is functional.
49	RW	SCAN_TYPE_CFG: Scan chain mode (boot configuration and debug configuration).
50	RW	SCAN_TYPE_CCFG_GPTR: Scan chain ccfg / gptr (pervasive: CC configuration; others: GPTR).
51	RW	SCAN_TYPE_REGF: Scan chain regf (register files).
52	RW	SCAN_TYPE_LBIST: Scan chain lbst (LBIST).
53	RW	SCAN_TYPE_ABIST: Scan chain abst (ABIST).
54	RW	SCAN_TYPE_REPR: Scan chain repr (array repair).
55	RW	SCAN_TYPE_TIME: Scan chain time (array timing).
56	RW	SCAN_TYPE_BNDY: Scan chain bndy (boundary IOs).
57	RW	SCAN_TYPE_FARR: Scan chain farr (fast array unload).
58	RW	SCAN_TYPE_CMSK: Scan chain cmsk (LBIST channel mask).
59	RW	SCAN_TYPE_INEX: Scan chain idex (c14 ASIC).

Bits	SCOM	Field Mnemonic: Description
60:63	RO	constant = 0b0000

Register Name	Clock Region Register
Mnemonic	TP.TCOB0.OB.CLK_REGION
Address	0000000009030006 (SCOM)
Description	start/stop of Clocks

Bits	SCOM	Field Mnemonic: Description
0:1	RWX	CLOCK_CMD: Command for clock control: 00 = NOP 01 = Start 10 = Stop 11 = Pulse (one pulse)
2	RWX	SLAVE_MODE: When selected, the clock command waits for the master chiplet to start. The bit is cleared after the incoming slave trigger and Keep_MS_Mode_after_trigger is set to 0.
3	RWX	MASTER_MODE: When selected, the clock command sends out a trigger to all slave chiplets. The bit is cleared after sending out one master trigger and Keep_MS_Mode_after_trigger is set to 0.
4	RWX	CLOCK_REGION_PERV: For clock region perv (pervasive).
5	RWX	CLOCK_REGION_UNIT1: For clock region pbiooa0 (PB).
6	RWX	CLOCK_REGION_UNIT2: For clock region ioo0 (IOO).
7	RWX	CLOCK_REGION_UNIT3: For clock region unused.
8	RWX	CLOCK_REGION_UNIT4: For clock region unused.
9	RWX	CLOCK_REGION_UNIT5: For clock region unused.
10	RWX	CLOCK_REGION_UNIT6: For clock region unused.
11	RWX	CLOCK_REGION_UNIT7: For clock region unused.
12	RWX	CLOCK_REGION_UNIT8: For clock region unused.
13	RWX	CLOCK_REGION_UNIT9: For clock region unused.
14	RWX	CLOCK_REGION_UNIT10: For clock region pllioo0 (IOO).
15:47	RO	constant = 0b000000000000000000000000000000000
48	RWX	SEL_THOLD_SL: Select SL tholds.
49	RWX	SEL_THOLD_NSL: Select NSL tholds.
50	RWX	SEL_THOLD_ARY: Select array thold.
51	RO	constant = 0b0
52	RW	CLOCK_PULSE_USE_EVEN: For dual mesh support. The default for pulse is ODD phase. When this bit is set, pulse is applied on EVEN phase.
53:63	RO	constant = 0b00000000000

Register Name	Clock Status SL Register
Mnemonic	TP.TCOB0.OB.CLOCK_STAT_SL
Address	0000000009030008 (SCOM)
Description	Clocks running SL

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b1111
4	ROX	CLOCK_STATUS_PERV_SL: Status of pervasive SL HLD. 0 = Run. 1 = Stop.
5	ROX	CLOCK_STATUS_UNIT1_SL: Status of pbiooa0 (PB SL HLD). - pb sl hld 0 = Run. 1 = Stop.
6	ROX	CLOCK_STATUS_UNIT2_SL: Status of ioo0 (IOO SL HLD). 0 = Run. 1 = Stop.
7	ROX	CLOCK_STATUS_UNIT3_SL: Status of unused SL HLD. 0 = Run. 1 = Stop.
8	ROX	CLOCK_STATUS_UNIT4_SL: Status of unused SL HLD. 0 = Run. 1 = Stop.
9	ROX	CLOCK_STATUS_UNIT5_SL: Status of unused SL HLD. 0 = Run. 1 = Stop.
10	ROX	CLOCK_STATUS_UNIT6_SL: Status of unused SL HLD. 0 = Run. 1 = Stop.
11	ROX	CLOCK_STATUS_UNIT7_SL: Status of unused SL HLD. 0 = Run. 1 = Stop.
12	ROX	CLOCK_STATUS_UNIT8_SL: Status of unused SL HLD. 0 = Run. 1 = Stop.
13	ROX	CLOCK_STATUS_UNIT9_SL: Status of unused SL HLD. 0 = Run. 1 = Stop.
14	ROX	CLOCK_STATUS_UNIT10_SL: Status of pllioo0 (IOO SL HLD). 0 = Run. 1 = Stop.
15:63	RO	constant = 0b1111111111111111111111111111111111111111111111111

Register Name	Clock Status NSL Register
Mnemonic	TP.TCOB0.OB.CLOCK_STAT_NSL
Address	0000000009030009 (SCOM)
Description	Clocks running nsl

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b1111
4	ROX	CLOCK_STATUS_PERV_NSL: Status of pervasive NSL HLD. 0 = Run. 1 = Stop.

Bits	SCOM	Field Mnemonic: Description
5	ROX	CLOCK_STATUS_UNIT1_NSL: Status of pbiooa0 (PB NSL HLD). 0 = Run. 1 = Stop.
6	ROX	CLOCK_STATUS_UNIT2_NSL: status of ioo0 (IOO NSL HLD). 0 = Run. 1 = Stop.
7	ROX	CLOCK_STATUS_UNIT3_NSL: Status of unused NSL HLD. 0 = Run. 1 = Stop.
8	ROX	CLOCK_STATUS_UNIT4_NSL: Status of unused NSL HLD. 0 = Run. 1 = Stop.
9	ROX	CLOCK_STATUS_UNIT5_NSL: Status of unused NSL HLD. 0 = Run. 1 = Stop.
10	ROX	CLOCK_STATUS_UNIT6_NSL: Status of unused NSL HLD. 0 = Run. 1 = Stop.
11	ROX	CLOCK_STATUS_UNIT7_NSL: Status of unused NSL HLD. 0 = Run. 1 = Stop.
12	ROX	CLOCK_STATUS_UNIT8_NSL: Status of unused NSL HLD. 0 = Run. 1 = Stop.
13	ROX	CLOCK_STATUS_UNIT9_NSL: Status of unused NSL HLD. 0 = Run. 1 = Stop.
14	ROX	CLOCK_STATUS_UNIT10_NSL: status of pllioo0 (IOO NSL HLD). 0 = Run. 1 = Stop.
15:63	RO	constant = 0b1111111111111111111111111111111111111111111111111

Register Name	**Clock Status Array Register**
Mnemonic	TP.TCOB0.OB.CLOCK_STAT_ARY
Address	000000000903000A (SCOM)
Description	Clocks running ary

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b1111
4	ROX	CLOCK_STATUS_PERV_ARY: Status of pervasive ARY HLD. 0 = Run. 1 = Stop.
5	ROX	CLOCK_STATUS_UNIT1_ARY: Status of pbiooa0 (PB ARY HLD). 0 = Run. 1 = Stop.
6	ROX	CLOCK_STATUS_UNIT2_ARY: Status of ioo0 (IOO ARY HLD). 0 = Run. 1 = Stop.

Bits	SCOM	Field Mnemonic: Description
7	ROX	CLOCK_STATUS_UNIT3_ARY: Status of unused ARY HLD. 0 = Run. 1 = Stop.
8	ROX	CLOCK_STATUS_UNIT4_ARY: Status of unused ARY HLD. 0 = Run. 1 = Stop.
9	ROX	CLOCK_STATUS_UNIT5_ARY: Status of unused ARY HLD. 0 = Run. 1 = Stop.
10	ROX	CLOCK_STATUS_UNIT6_ARY: Status of unused ARY HLD. 0 = Run. 1 = Stop.
11	ROX	CLOCK_STATUS_UNIT7_ARY: Status of unused ARY HLD. 0 = Run. 1 = Stop.
12	ROX	CLOCK_STATUS_UNIT8_ARY: Status of unused ARY HLD. 0 = Run. 1 = Stop.
13	ROX	CLOCK_STATUS_UNIT9_ARY: Status of unused ARY HLD. 0 = Run. 1 = Stop.
14	ROX	CLOCK_STATUS_UNIT10_ARY: Status of pllioo0 (IOO ARY HLD). 0 = Run. 1 = Stop.
15:63	RO	constant = 0b1111111111111111111111111111111111111111111111111

Register Name	ABIST and IOBIST Register
Mnemonic	TP.TCOB0.OB.BIST
Address	000000000903000B (SCOM)
Description	ABIST and IOBIST per region

Bits	SCOM	Field Mnemonic: Description
0	RW	TC_BIST_START_TEST_DC: Keep this at 0 during ABIST/IOBIST. It can be used to bypass the RUNN start. When this bit is set, the BIST_START_TEST goes high immediately without waiting for RUNN. BIST starts with the first HLD clock cycle.
1	RW	TC_SRAM_ABIST_MODE_DC: Select the ABIST engines for SRAMs.
2	RW	TC_EDRAM_ABIST_MODE_DC: Select the ABIST engines for eDRAMs.
3	RW	TC_IOBIST_MODE_DC: Select the IOBIST engines.
4	RW	BIST_PERV: Region pervasive: 1 = BIST_START_TEST for this region is triggered. 0 = The region is not part of the ABIST/IOBIST run.
5	RW	BIST_UNIT1: Region pbiooa0 (PB): 1 = BIST_START_TEST for this region is triggered. 0 = The region is not part of the ABIST/IOBIST run.
6	RW	BIST_UNIT2: Region ioo0 (IOO): 1 = BIST_START_TEST for this region is triggered. 0 = The region is not part of the ABIST/IOBIST run.

Bits	SCOM	Field Mnemonic: Description
7	RW	BIST_UNIT3: Region unused: 1 = BIST_START_TEST for this region is triggered. 0 = The region is not part of the ABIST/IOBIST run.
8	RW	BIST_UNIT4: Region unused: 1 = BIST_START_TEST for this region is triggered. 0 = The region is not part of the ABIST/IOBIST run.
9	RW	BIST_UNIT5: Region unused: 1 = BIST_START_TEST for this region is triggered. 0 = The region is not part of the ABIST/IOBIST run.
10	RW	BIST_UNIT6: Region unused: 1 = BIST_START_TEST for this region is triggered. 0 = The region is not part of the ABIST/IOBIST run.
11	RW	BIST_UNIT7: Region unused: 1 = BIST_START_TEST for this region is triggered. 0 = The region is not part of the ABIST/IOBIST run.
12	RW	BIST_UNIT8: Region unused: 1 = BIST_START_TEST for this region is triggered. 0 = The region is not part of the ABIST/IOBIST run.
13	RW	BIST_UNIT9: Region unused: 1 = BIST_START_TEST for this region is triggered. 0 = The region is not part of the ABIST/IOBIST run.
14	RW	BIST_UNIT10: Region pllioo0 (IOO): 1 = BIST_START_TEST for this region is triggered. 0 = The region is not part of the ABIST/IOBIST run.
15:47	RO	constant = 0b000000000000000000000000000000000
48	RW	BIST_STROBE_WINDOW_EN: Enable strobe window only in TE = 1 mode. The OPCGGO tester pin enables the ABIST compare, once ABIST has been started. Special setup in the ABIST engine is required. The default is 0. System mode cannot enable this feature.
49:63	RO	constant = 0b000000000000000

Register Name	Checkstop 1 Register
Mnemonic	TP.TCOB0.OB.XSTOP1
Address	000000000903000C (SCOM)
Description	checkstop per region

Bits	SCOM	Field Mnemonic: Description
0	RW	XSTOP1_MASK_B: Mask for checkstop to clockstop of select regions. (See xstop_perv, xstop_unit0..n.) 0 = Ignore checkstop. 1 = Stop on checkstop.
1	RW	XSTOP1_UNUSED: Unused.
2	RW	TRIGGER_OPCG_ON_XSTOP1: Trigger OPCG on checkstop instead of performing clockstop.
3	RW	XSTOP1_WAIT_ALLWAYS: When set to 1, checkstop waits independently of flush. The default is to not wait when flush is not set.
4	RW	XSTOP1_PERV: Region perv: 1 = The region is stopped. 0 = The region continues to run on checkstop.

Bits	SCOM	Field Mnemonic: Description
5	RW	XSTOP1_UNIT1: Region pbiooa0 (PB): 1 = The region is stopped. 0 = The region continues to run on checkstop.
6	RW	XSTOP1_UNIT2: Region ioo0 (IOO): 1 = The region is stopped. 0 = The region continues to run on checkstop.
7	RW	XSTOP1_UNIT3: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
8	RW	XSTOP1_UNIT4: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
9	RW	XSTOP1_UNIT5: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
10	RW	XSTOP1_UNIT6: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
11	RW	XSTOP1_UNIT7: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
12	RW	XSTOP1_UNIT8: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
13	RW	XSTOP1_UNIT9: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
14	RW	XSTOP1_UNIT10: Region pllioo0 (IOO): 1 = The region is stopped. 0 = The region continues to run on checkstop.
15:47	RO	constant = 0b000000000000000000000000000000000
48:59	RW	XSTOP1_WAIT_CYCLES: Specifies how many cycles checkstop waits (0 - 4095) after dropping flush before tholds are dropped.
60:63	RO	constant = 0b0000

Register Name	Checkstop 2 Register
Mnemonic	TP.TCOB0.OB.XSTOP2
Address	000000000903000D (SCOM)
Description	XSTOP per region

Bits	SCOM	Field Mnemonic: Description
0	RW	XSTOP2_MASK_B: Mask for checkstop to clockstop of select regions (see xstop_perv, xstop_unit0..n). 0 = Ignore checkstop 1 = Stop on checkstop
1	RW	XSTOP2_UNUSED: Unused.
2	RW	TRIGGER_OPCG_ON_XSTOP2: Trigger OPCG on checkstop instead of performing clockstop.
3	RW	XSTOP2_WAIT_ALLWAYS: When set to 1, checkstop waits independently of flush. The default is to not wait when flush is not set.

Bits	SCOM	Field Mnemonic: Description
4	RW	XSTOP2_PERV: Region pervasive: 1 = The region is stopped. 0 = The region continues to run on checkstop.
5	RW	XSTOP2_UNIT1: Region pbiooa0 (PB): 1 = The region is stopped. 0 = The region continues to run on checkstop.
6	RW	XSTOP2_UNIT2: Region ioo0 (IOO): 1 = The region is stopped. 0 = The region continues to run on checkstop.
7	RW	XSTOP2_UNIT3: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
8	RW	XSTOP2_UNIT4: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
9	RW	XSTOP2_UNIT5: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
10	RW	XSTOP2_UNIT6: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
11	RW	XSTOP2_UNIT7: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
12	RW	XSTOP2_UNIT8: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
13	RW	XSTOP2_UNIT9: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
14	RW	XSTOP2_UNIT10: Region pllioo0 (IOO): 1 = The region is stopped. 0 = The region continues to run on checkstop.
15:47	RO	constant = 0b000000000000000000000000000000000
48:59	RW	XSTOP2_WAIT_CYCLES: Specifies how many cycles checkstop waits (0 - 4095) after dropping flush before tholds are dropped.
60:63	RO	constant = 0b0000

Register Name	Checkstop 3 Register
Mnemonic	TP.TCOB0.OB.XSTOP3
Address	000000000903000E (SCOM)
Description	XSTOP per region

Bits	SCOM	Field Mnemonic: Description
0	RW	XSTOP3_MASK_B: Mask for checkstop to clockstop of select regions. (See xstop_perv, xstop_unit0..n). 0 = Ignore checkstop. 1 = Stop on checkstop.
1	RW	XSTOP3_UNUSED: Unused.

Bits	SCOM	Field Mnemonic: Description
2	RW	TRIGGER_OPCG_ON_XSTOP3: Trigger OPCG on checkstop instead of performing clockstop.
3	RW	XSTOP3_WAIT_ALLWAYS: When set to 1, checkstop waits independently of flush. The default is to not wait when flush is not set.
4	RW	XSTOP3_PERV: Region pervasive: 1 = The region is stopped. 0 = The region continues to run on checkstop.
5	RW	XSTOP3_UNIT1: Region pbiooa0 (PB): 1 = The region is stopped. 0 = The region continues to run on checkstop.
6	RW	XSTOP3_UNIT2: Region ioo0 (IOO): 1 = The region is stopped. 0 = The region continues to run on checkstop.
7	RW	XSTOP3_UNIT3: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
8	RW	XSTOP3_UNIT4: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
9	RW	XSTOP3_UNIT5: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
10	RW	XSTOP3_UNIT6: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
11	RW	XSTOP3_UNIT7: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
12	RW	XSTOP3_UNIT8: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
13	RW	XSTOP3_UNIT9: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
14	RW	XSTOP3_UNIT10: Region pllioo0 (IOO): 1 = The region is stopped. 0 = The region continues to run on checkstop.
15:47	RO	constant = 0b000000000000000000000000000000000
48:59	RW	XSTOP3_WAIT_CYCLES: Specifies how many cycles checkstop waits (0 - 4095) after dropping flush before tholds are dropped.
60:63	RO	constant = 0b0000

Register Name	Error Status Register
Mnemonic	TP.TCOB0.OB.ERROR_STATUS
Address	000000000903000F (SCOM)
Description	Error Status of CC

Bits	SCOM	Field Mnemonic: Description
0	RWX	PCB_WRITE_NOT_ALLOWED_ERR: A write was attempted on a read only register.

Bits	SCOM	Field Mnemonic: Description
1	RWX	PCB_READ_NOT_ALLOWED_ERR: A read is not allowed; the register might be write only.
2	RWX	PCB_PARITY_ON_CMD_ERR: A parity error on the command.
3	RWX	PCB_ADDRESS_NOT_VALID_ERR: Invalid address.
4	RWX	PCB_PARITY_ON_ADDR_ERR: Parity error on the address.
5	RWX	PCB_PARITY_ON_DATA_ERR: Parity error on data.
6	RWX	PCB_PROTECTED_ACCESS_INVALID_ERR: Protection violation.
7	RWX	PCB_PARITY_ON_SPCIF_ERR: Parity error on SPCIF.
8	RWX	PCB_WRITE_AND_OPCG_IP_ERR: A PCB write was attempted while OPCG is running.
9	RWX	SCAN_READ_AND_OPCG_IP_ERR: A scan read was attempted while OPCG is running.
10	RWX	CLOCK_CMD_CONFLICT_ERR: A clock command is in progress.
11	RWX	SCAN_COLLISION_ERR: Scan region was selected on a running region.
12	RWX	PREVENTED_SCAN_COLLISION_ERR: PCB request to set a scan region that is running.
13	RWX	OPCG_TRIGGER_ERR: OPCG was triggered while OPCG is running.
14	RWX	PHASE_CNT_CORRUPTION_ERR: The phase counters inside the chiplet are out of sync.
15	RWX	CLOCK_CMD_PREVENTED_ERR: Security or scan collision prevented a clock start.
16	RWX	PARITY_ON_OPCG_SM_ERR: Parity error on the OPCG state machine.
17	RWX	PARITY_ON_CLOCK_MUX_REG_ERR: Parity error on scan/clock region/type or clock status register.
18	RWX	PARITY_ON_OPCG_REG_ERR: Parity error on OPCG registers.
19	RWX	PARITY_ON_SYNC_CONFIG_REG_ERR: Parity error on sync configuration register.
20	RWX	PARITY_ON_XSTOP_REG_ERR: Parity error on checkstop register.
21	RWX	PARITY_ON_GPIO_REG_ERR: Parity error on GP0,4,5,6 registers.
22	RWX	CLKCMD_REQUEST_ERR: Region clkcmd has one request pending but received a second one.
23	RWX	CBS_PROTOCOL_ERR: CBS protocol error. The REQ / ACK sequence is wrong.
24	RWX	VITL_ALIGN_ERR: VITL alignment is out of sync to the sync pulse.
25	RWX	UNIT_SYNC_LVL_ERR: Unit0 and Unit1 sync lvl pulse are not in sync. AVP is broken.
26	RWX	PARITY_ON_SELFBOOT_CMD_STATE_ERR: Parity error on SELFBOOT command state.
27	RWX	UNUSED_ERROR27: Unused.
28	RWX	UNUSED_ERROR28: Unused.
29	RWX	UNUSED_ERROR29: Unused.
30	RWX	UNUSED_ERROR30: Unused.
31	RWX	UNUSED_ERROR31: Unused.

Register Name	OPCG Control Capture 1 Register
Mnemonic	TP.TCOB0.OB.OPCG_CAPT1
Address	0000000009030010 (SCOM)
Description	OPCG Control Register Capture1

Bits	SCOM	Field Mnemonic: Description
0:3	RW	COUNT: 0000 = 12 cycles 0001 – 1100 = Cycles 1-12 1101-1111 = 24 cycles for normal, slow regions
4:8	RW	SEQ_01: Sequence cycle 1 for normal/slow region (SL, NSL, ARY, SE, FCE).
9:13	RW	SEQ_02: Sequence cycle 2 for normal/slow region (SL, NSL, ARY, SE, FCE).
14:18	RW	SEQ_03: Sequence cycle 3 for normal/slow region (SL, NSL, ARY, SE, FCE).
19:23	RW	SEQ_04: Sequence cycle 4 for normal/slow region (SL, NSL, ARY, SE, FCE).
24:28	RW	SEQ_05: Sequence cycle 5 for normal/slow region (SL, NSL, ARY, SE, FCE).
29:33	RW	SEQ_06: Sequence cycle 6 for normal/slow region (SL, NSL, ARY, SE, FCE).
34:38	RW	SEQ_07: Sequence cycle 7 for normal/slow region (SL, NSL, ARY, SE, FCE).
39:43	RW	SEQ_08: Sequence cycle 8 for normal/slow region (SL, NSL, ARY, SE, FCE).
44:48	RW	SEQ_09: Sequence cycle 9 for normal/slow region (SL, NSL, ARY, SE, FCE).
49:53	RW	SEQ_10: Sequence cycle 10 for normal/slow region (SL, NSL, ARY, SE, FCE).
54:58	RW	SEQ_11: Sequence cycle 11 for normal/slow region (SL, NSL, ARY, SE, FCE).
59:63	RW	SEQ_12: Sequence cycle 12 for normal/slow region (SL, NSL, ARY, SE, FCE).

Register Name	OPCG Control Capture 2 Register
Mnemonic	TP.TCOB0.OB.OPCG_CAPT2
Address	0000000009030011 (SCOM)
Description	OPCG Control Register Capture 2

Bits	SCOM	Field Mnemonic: Description
0:3	RW	UNUSED_CAPT2:
4:8	RW	SEQ_13_01EVEN: Sequence cycle 1 is even for fast region or cycle 13 for normal region (SL, NSL, ARY, SE, FCE).
9:13	RW	SEQ_14_01ODD: Sequence cycle 1 is odd for fast region or cycle 14 for normal region (SL, NSL, ARY, SE, FCE).
14:18	RW	SEQ_15_02EVEN: Sequence cycle 2 is even for fast region or cycle 15 for normal region (SL, NSL, ARY, SE, FCE).
19:23	RW	SEQ_16_02ODD: Sequence cycle 2 is odd for fast region or cycle 16 for normal region (SL, NSL, ARY, SE, FCE).
24:28	RW	SEQ_17_03EVEN: Sequence cycle 3 is even for fast region or cycle 17 for normal region (SL, NSL, ARY, SE, FCE).
29:33	RW	SEQ_18_03ODD: Sequence cycle 3 is odd for fast region or cycle 18 for normal region (SL, NSL, ARY, SE, FCE).
34:38	RW	SEQ_19_04EVEN: Sequence cycle 4 is even for fast region or cycle 19 for normal region (SL, NSL, ARY, SE, FCE).
39:43	RW	SEQ_20_04ODD: Sequence cycle 4 is odd for fast region or cycle 20 for normal region (SL, NSL, ARY, SE, FCE).
44:48	RW	SEQ_21_05EVEN: Sequence cycle 5 is even for fast region or cycle 21 for normal region (SL, NSL, ARY, SE, FCE).
49:53	RW	SEQ_22_05ODD: Sequence cycle 5 is odd for fast region or cycle 22 for normal region (SL, NSL, ARY, SE, FCE).

Bits	SCOM	Field Mnemonic: Description
54:58	RW	SEQ_23_06EVEN: Sequence cycle 6 is even for fast region or cycle 23 for normal region (SL, NSL, ARY, SE, FCE).
59:63	RW	SEQ_24_06ODD: Sequence cycle 6 is odd for fast region or cycle 24 for normal region (SL, NSL, ARY, SE, FCE).

Register Name	OPCG Capture 3 Register
Mnemonic	TP.TCOB0.OB.OPCG_CAPT3
Address	0000000009030012 (SCOM)
Description	OPCG Control Register Capture 3

Bits	SCOM	Field Mnemonic: Description
0:3	RW	UNUSED_CAPT3:
4:8	RW	SEQ_07EVEN: Sequence cycle 7 is even for fast region (SL, NSL, ARY, SE, FCE).
9:13	RW	SEQ_07ODD: Sequence cycle 7 is odd for fast region (SL, NSL, ARY, SE, FCE).
14:18	RW	SEQ_08EVEN: Sequence cycle 8 is even for fast region (SL, NSL, ARY, SE, FCE).
19:23	RW	SEQ_08ODD: Sequence cycle 8 is odd for fast region (SL, NSL, ARY, SE, FCE).
24:28	RW	SEQ_09EVEN: Sequence cycle 9 is even for fast region (SL, NSL, ARY, SE, FCE).
29:33	RW	SEQ_09ODD: Sequence cycle 9 is odd for fast region (SL, NSL, ARY, SE, FCE).
34:38	RW	SEQ_10EVEN: Sequence cycle 10 is even for fast region (SL, NSL, ARY, SE, FCE).
39:43	RW	SEQ_10ODD: Sequence cycle 10 is odd for fast region (SL, NSL, ARY, SE, FCE).
44:48	RW	SEQ_11EVEN: Sequence cycle 11 is even for fast region (SL, NSL, ARY, SE, FCE).
49:53	RW	SEQ_11ODD: Sequence cycle 11 is odd for fast region (SL, NSL, ARY, SE, FCE).
54:58	RW	SEQ_12EVEN: Sequence cycle 12 is even for fast region (SL, NSL, ARY, SE, FCE).
59:63	RW	SEQ_12ODD: Sequence cycle 12 is odd for fast region (SL, NSL, ARY, SE, FCE).

Register Name	Debug CBS CC Register
Mnemonic	TP.TCOB0.OB.DBG_CBS_CC
Address	0000000009030013 (SCOM)
Description	Debug CBS CC Register

Bits	SCOM	Field Mnemonic: Description
0	ROX	DBG_RESET_EP: Reset endpoint.
1	ROX	DBG_OPCG_IP: OPCG in progress, not in idle state.
2	ROX	DBG_VITL_CLKOFF: VITL HLD stopped. When enabled, plat-depth cycles are needed to switch this latch.
3	ROX	DBG_TEST_ENABLE: Test enable.
4	ROX	DBG_CBS_REQ: CBS Interface. Request (latched).
5:7	ROX	DBG_CBS_CMD: CBS Interface. Command (latched).
8:12	ROX	DBG_CBS_STATE: CBS Command State Machine; 00000 = Idle.
13	ROX	DBG_SECURITY_DEBUG_MODE: Status of the security mode bit.

Bits	SCOM	Field Mnemonic: Description
14	ROX	DBG_CBS_PROTOCOL_ERROR: CBS protocol error. Request raised, although state machine is not in idle state. Need reset_ep to clear this bit. No impact on IPL.
15	ROX	DBG_PCB_IDLE: PCB Interface in idle state.
16:19	ROX	DBG_CURRENT_OPCG_MODE: The current (latest) OPCG mode: 0 = NOP 1 = LBIST 2 = ABIST 3 = RUNN 4 = SCAN0 5 = SCAN 6 = SCAN rotate 7 = SCAN with UpdateDR 8 = SCAN with CaptureDR 9 = CLK Change Request 10-15 = Unused
20:23	ROX	DBG_LAST_OPCG_MODE: Previous OPCG mode.
24	ROX	DBG_PCB_ERROR: PCB interface error. Read the CC error register or set CBS_CMD = 001 to switch the FSI CBS debug information to the CC error register.
25	ROX	DBG_PARITY_ERROR: Any parity error, non-PCB parity. Read the CC error register or set CBS_CMD = 001 to switch the FSI CBS debug information to the CC error register.
26	ROX	DBG_CC_ERROR: Any other CC error. Read the CC error register or set CBS_CMD = 001 to switch the FSI CBS debug information to the CC error register.
27	ROX	DBG_CHIPLET_IS_ALIGNED: Set to 1 when a valid align pulse was sent out.
28	ROX	DBG_PCB_REQUEST_SINCE_RESET: Reset clears this bit, and the first PCB request sets it.
29	ROX	DBG_PARANOIA_TEST_ENABLE_CHANGE: Rising or falling edge on test enable, after reset. Need reset_ep to clear. No impact on IPL.
30	ROX	DBG_PARANOIA_VITL_CLKOFF_CHANGE: Rising or falling edge on vitl_clkoff, after reset. Need reset_ep to clear. No impact on IPL.
31	ROX	TP_TPFSI_CBS_ACK: This is the only representation of the CC acknowledge signal that is sent to FSI.

Register Name	CC Protect Mode Register
Mnemonic	TP.TCOB0.OB.CC_PROTECT_MODE_REG
Address	00000000090303FE (SCOM)
Description	Enables read and write protection.

Bits	SCOM	Field Mnemonic: Description
0	RW	CC_READ_PROTECT_ENABLE: Enables read protection.
1	RW	CC_WRITE_PROTECT_ENABLE: Enables write protection.

Register Name	Atomic Lock Register
Mnemonic	TP.TCOB0.OB.CC_ATOMIC_LOCK_REG
Address	00000000090303FF (SCOM)
Description	Enables an atomic lock and an atomic lock counter.

Bits	SCOM	Field Mnemonic: Description
0	RW	CC_ATOMIC_LOCK_ENABLE: Enables atomic lock.
1:4	ROX	CC_ATOMIC_ID: Atomic ID.
5:7	RO	constant = 0b000
8:15	ROX	CC_ATOMIC_ACTIVITY: Atomic lock counter.

Register Name	Global Checkstop FIR Register
Mnemonic	TP.TCOB0.OB.XFIR
Address	0000000009040000 (SCOM)
Description	Global checkstop FIR

Bits	SCOM	Field Mnemonic: Description
0	RWX	XFIR_IN0: Summary bit (any checkstop).
1	RWX	XFIR_IN1: Checkstop broadcast via OOB.
2	RWX	XFIR_IN2: Unused.
3	RWX	XFIR_IN3: Checkstop from pervasive unit.
4	RWX	XFIR_IN4: Checkstop from PBIOOA.
5	RWX	XFIR_IN5: Checkstop from IOO.
6	RWX	XFIR_IN6: Checkstop from IOOPPE.
7:25	RWX	XFIR_IN7: Unused.
26	RWX	XFIR_IN26: Checkstop on debug trigger.

Register Name	Global Recoverable FIR Register
Mnemonic	TP.TCOB0.OB.RFIR
Address	0000000009040001 (SCOM)
Description	Global recoverable FIR

Bits	SCOM	Field Mnemonic: Description
0	ROX	RFIR_IN0: Local checkstop from PBIOX0, PBIOX1, PBIOX2, and IOPPE.
1	ROX	LFIR_RECOV_ERR: Recoverable error from pervasive unit.
2	ROX	RFIR_IN4: Recovery from PBIOOA.
3	ROX	RFIR_IN5: Recovery from IOO.
4	ROX	RFIR_IN6: Recovery from IOOPPE.
5:23	ROX	RFIR_IN7: Unused.

Register Name	FIR Mask Register
Mnemonic	TP.TCOB0.OB.FIR_MASK
Address	0000000009040002 (SCOM)
Description	FIR Mask

Bits	SCOM	Field Mnemonic: Description
0	RW	FIR_MASK_IN0: Mask for XFIR summary bit (any checkstop).
1	RW	FIR_MASK_IN1: Mask for XFIR from other chiplets.
2	RW	FIR_MASK_IN2: Unused.
3	RW	FIR_MASK_IN3: Mask for XFIR from pervasive unit.
4	RW	FIR_MASK_IN4: Mask for PBIOOA, XFIR, and RFIR.
5	RW	FIR_MASK_IN5: Mask for IOO, XFIR, and RFIR.
6	RW	FIR_MASK_IN6: Mask for IOOPPE, XFIR, and RFIR.
7:25	RW	FIR_MASK_IN7: Unused.
26	RW	FIR_MASK_IN26: Mask for debug trigger and local checkstop to recoverable error.

Register Name	Special Attention Register
Mnemonic	TP.TCOB0.OB.SPATTN
Address	0000000009040004 (SCOM) 0000000009040005 (SCOM1) 0000000009040006 (SCOM2)
Description	Special Attention

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	ROX	NCX	NCX	SPATTN_IN0: Special attention from PBIOOA.
1	ROX	NCX	NCX	SPATTN_IN1: Special attention from IOO.
2	ROX	NCX	NCX	SPATTN_IN2: Special attention from IOOPPE.
3	ROX	NCX	NCX	SPATTN_IN3: Unused special attentions.
4	ROX	NCX	NCX	SPATTN_IN4: Unused special attentions.
5	ROX	NCX	NCX	SPATTN_IN5: Unused special attentions.
6	ROX	NCX	NCX	SPATTN_IN6: Unused special attentions.
7	ROX	NCX	NCX	SPATTN_IN7: Unused special attentions.
8	ROX	NCX	NCX	SPATTN_IN8: Unused special attentions.
9	ROX	NCX	NCX	SPATTN_IN9: Unused special attentions.

Register Name	Special Attention Mask Register
Mnemonic	TP.TCOB0.OB.SPA_MASK
Address	0000000009040007 (SCOM)
Description	Special Attention Mask

Bits	SCOM	Field Mnemonic: Description
0:9	RW	SPA_MASK_IN: Special attention mask.

Register Name	FIR Mode Register
Mnemonic	TP.TCOB0.OB.EPS.FIR.MODE_REG
Address	0000000009040008 (SCOM)
Description	Mode Register

Bits	SCOM	Field Mnemonic: Description
0	RW	MODE_IN0: Unused.
1	RW	MODE_IN1: Unused.
2	RW	MODE_IN2: Unused.
3	RW	MODE_IN3: Unused.
4	RW	MODE_IN4: Stop chip TOD on checkstop. (Unused in POWER9).
5	RW	MODE_IN5: Stop chip TOD on recoverable. (Unused in POWER9).
6	RW	MODE_IN6: Disable propagation of checkstop to other chips.
7	RW	MODE_IN7: Unused.
8	RW	MODE_IN8: Enable checkstop on special attention.
9	RW	MODE_IN9: mask_direct/local_error.
10	RW	MODE_IN10: Unused.
11	RW	MODE_IN11: Unused.
12:15	RW	MODE_IN: Unused.

Register Name	Host Attention Register
Mnemonic	TP.TCOB0.OB.HOSTATTN
Address	0000000009040009 (SCOM)
Description	Host Attention

Bits	SCOM	Field Mnemonic: Description
0	ROX	HOSTATTN_IN0: Host attention summary bit.
1	ROX	HOSTATTN_IN1: Unused.
2	ROX	HOSTATTN_IN2: Unused.
3	ROX	HOSTATTN_IN3: Unused.
4	ROX	HOSTATTN_IN4: Unused.
5	ROX	HOSTATTN_IN5: Unused.
6	ROX	HOSTATTN_IN6: Unused.
7	ROX	HOSTATTN_IN7: Unused.
8	ROX	HOSTATTN_IN8: Unused.
9	ROX	HOSTATTN_IN9: Unused.
10	ROX	HOSTATTN_IN10: Unused.
11	ROX	HOSTATTN_IN11: Unused.
12	ROX	HOSTATTN_IN12: Unused.
13	ROX	HOSTATTN_IN13: Unused.

Bits	SCOM	Field Mnemonic: Description
14	ROX	HOSTATTN_IN14: Unused.
15	ROX	HOSTATTN_IN15: Unused.
16	ROX	HOSTATTN_IN16: Unused.
17	ROX	HOSTATTN_IN17: Unused.
18	ROX	HOSTATTN_IN18: Unused.
19	ROX	HOSTATTN_IN19: Unused.
20	ROX	HOSTATTN_IN20: Unused.
21	ROX	HOSTATTN_IN21: Unused.
22	ROX	HOSTATTN_IN22: Unused.

Register Name	Local FIR Register
Mnemonic	TP.TCOB0.OB.LOCAL_FIR
Address	000000000904000A (SCOM) 000000000904000B (SCOM1) 000000000904000C (SCOM2)
Description	Local FIR

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_IN0: CFIR internal parity error.
1	RWX	WOX_AND	WOX_OR	FIR_IN1: Local errors from GPIO (PCB error).
2	RWX	WOX_AND	WOX_OR	FIR_IN2: Local errors from CC (PCB error).
3	RWX	WOX_AND	WOX_OR	FIR_IN3: Local errors from CC (OPCG, parity, scan collision, and so on).
4	RWX	WOX_AND	WOX_OR	FIR_IN4: Local errors from PSC (PCB error).
5	RWX	WOX_AND	WOX_OR	FIR_IN5: Local errors from PSC (parity error).
6	RWX	WOX_AND	WOX_OR	FIR_IN6: Local errors from Thermal (parity error).
7	RWX	WOX_AND	WOX_OR	FIR_IN7: Local errors from Thermal (PCB error).
8	RWX	WOX_AND	WOX_OR	FIR_IN8: Local errors from Thermal (trip error critical).
9	RWX	WOX_AND	WOX_OR	FIR_IN9: Local errors from Thermal (trip error fatal).
10	RWX	WOX_AND	WOX_OR	FIR_IN10: Therm volttrip error.
11	RWX	WOX_AND	WOX_OR	FIR_IN11: Local errors from Debug (error).
12	RWX	WOX_AND	WOX_OR	FIR_IN12: Local errors from Trace Array0 (SCOM error).
13	RWX	WOX_AND	WOX_OR	FIR_IN13: Local errors from Trace Array0.
14	RWX	WOX_AND	WOX_OR	FIR_IN14: Unused.
15	RWX	WOX_AND	WOX_OR	FIR_IN15: Unused.
16	RWX	WOX_AND	WOX_OR	FIR_IN16: Unused.
17	RWX	WOX_AND	WOX_OR	FIR_IN17: Unused.
18	RWX	WOX_AND	WOX_OR	FIR_IN18: Unused.
19	RWX	WOX_AND	WOX_OR	FIR_IN19: Unused.
20	RWX	WOX_AND	WOX_OR	FIR_IN20: Unused.
21	RWX	WOX_AND	WOX_OR	FIR_IN21: Unused.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
22	RWX	WOX_AND	WOX_OR	FIR_IN22: Unused.
23	RWX	WOX_AND	WOX_OR	FIR_IN23: Unused.
24	RWX	WOX_AND	WOX_OR	FIR_IN24: Unused.
25	RWX	WOX_AND	WOX_OR	FIR_IN25: Unused.
26	RWX	WOX_AND	WOX_OR	FIR_IN26: Unused.
27	RWX	WOX_AND	WOX_OR	FIR_IN27: Unused.
28	RWX	WOX_AND	WOX_OR	FIR_IN28: Unused.
29	RWX	WOX_AND	WOX_OR	FIR_IN29: Unused.
30	RWX	WOX_AND	WOX_OR	FIR_IN30: Unused.
31	RWX	WOX_AND	WOX_OR	FIR_IN31: Unused.
32	RWX	WOX_AND	WOX_OR	FIR_IN32: Unused.
33	RWX	WOX_AND	WOX_OR	FIR_IN33: Unused.
34	RWX	WOX_AND	WOX_OR	FIR_IN34: Unused.
35	RWX	WOX_AND	WOX_OR	FIR_IN35: Unused.
36	RWX	WOX_AND	WOX_OR	FIR_IN36: Unused.
37	RWX	WOX_AND	WOX_OR	FIR_IN37: Unused.
38	RWX	WOX_AND	WOX_OR	FIR_IN38: Unused.
39	RWX	WOX_AND	WOX_OR	FIR_IN39: Unused.
40	RWX	WOX_AND	WOX_OR	FIR_IN40: Unused.
41	RWX	WOX_AND	WOX_OR	FIR_IN41: Malfunction alert broadcast via OOB.

Register Name	Local FIR Mask Register
Mnemonic	TP.TCOB0.OB.EPS.FIR.LOCAL_FIR_MASK
Address	000000000904000D (SCOM) 000000000904000E (SCOM1) 000000000904000F (SCOM2)
Description	Local FIR Mask

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:41	RW	WO_AND	WO_OR	LFIR_MASK_IN: Mask for LEM error collection vector.

Register Name	Local FIR Action 0 Register
Mnemonic	TP.TCOB0.OB.EPS.FIR.LOCAL_FIR_ACTION0
Address	0000000009040010 (SCOM)
Description	Local FIR Action0

Bits	SCOM	Field Mnemonic: Description
0:41	RW	FIR_ACTION0_IN: action0 mask.

Register Name	Local FIR Action 1 Register
Mnemonic	TP.TCOB0.OB.EPS.FIR.LOCAL_FIR_ACTION1
Address	0000000009040011 (SCOM)
Description	Local FIR Action1

Bits	SCOM	Field Mnemonic: Description
0:41	RW	FIR_ACTION1_IN: action1 mask.

Register Name	Group Checkstop Mask Register
Mnemonic	TP.TCOB0.OB.EPS.FIR.GXSTOP_TRIG_REG
Address	0000000009040013 (SCOM)
Description	Group checkstop Mask Register

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP_TRIG_IN0: Mask bit for system checkstop.
1	RW	GXSTP_TRIG_IN1: Mask bit for recoverable error.
2	RW	GXSTP_TRIG_IN2: Mask bit for special attention.
3	RW	GXSTP_TRIG_IN3: Mask bit for local checkstop.
4	RW	GXSTP_TRIG_IN4: Mask bit for type 4 error (host attention).
5	RW	GXSTP_TRIG_IN5: Mask bit for OOB sys_checkstop input (0).
6	RW	GXSTP_TRIG_IN6: Mask bit for OOB sys_checkstop input (1).
7	RW	GXSTP_TRIG_IN7: Mask bit for group checkstop input (0).
8	RW	GXSTP_TRIG_IN8: Mask bit for group checkstop input (1).
9	RW	GXSTP_TRIG_IN9: Mask bit for debug checkstop on trigger.
10	RW	GXSTP_TRIG_IN10: Unused.
11	RW	GXSTP_TRIG_IN11: Unused.

Register Name	Group 0 Checkstop Mask Register
Mnemonic	TP.TCOB0.OB.EPS.FIR.GXSTOP0_MASK_REG
Address	0000000009040014 (SCOM)
Description	Group0 checkstop Mask Register

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP0_TRIG_IN0: Mask bit for system checkstop.
1	RW	GXSTP0_TRIG_IN1: Mask bit for recoverable error.
2	RW	GXSTP0_TRIG_IN2: Mask bit for special attention.
3	RW	GXSTP0_TRIG_IN3: Mask bit for local checkstop.
4	RW	GXSTP0_TRIG_IN4: Mask bit for type 4 error (host attention).
5	RW	GXSTP0_TRIG_IN5: Mask bit for OOB sys_checkstop Input (0).
6	RW	GXSTP0_TRIG_IN6: Mask bit for OOB sys_checkstop Input (1).

Bits	SCOM	Field Mnemonic: Description
7	RW	GXSTP0_TRIG_IN7: Mask bit for group checkstop input (0).
8	RW	GXSTP0_TRIG_IN8: Mask bit for group checkstop input (1).
9	RW	GXSTP0_TRIG_IN9: Mask bit for debug checkstop on trigger.
10	RW	GXSTP0_TRIG_IN10: Unused.
11	RW	GXSTP0_TRIG_IN11: Unused.

Register Name	Group1 Checkstop Mask Register
Mnemonic	TP.TCOB0.OB.EPS.FIR.GXSTOP1_MASK_REG
Address	0000000009040015 (SCOM)
Description	Group1 checkstop Mask Register

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP1_TRIG_IN0: Mask bit for system checkstop.
1	RW	GXSTP1_TRIG_IN1: Mask bit for recoverable error.
2	RW	GXSTP1_TRIG_IN2: Mask bit for special attention.
3	RW	GXSTP1_TRIG_IN3: Mask bit for local checkstop.
4	RW	GXSTP1_TRIG_IN4: Mask bit for type 4 error (host attention).
5	RW	GXSTP1_TRIG_IN5: Mask bit for OOB sys_checkstop Input (0).
6	RW	GXSTP1_TRIG_IN6: Mask bit for OOB sys_checkstop Input (1).
7	RW	GXSTP1_TRIG_IN7: Mask bit for group checkstop input (0).
8	RW	GXSTP1_TRIG_IN8: Mask bit for group checkstop input (1).
9	RW	GXSTP1_TRIG_IN9: Mask bit for debug checkstop on trigger.
10	RW	GXSTP1_TRIG_IN10: Unused.
11	RW	GXSTP1_TRIG_IN11: Unused.

Register Name	Group 2 Checkstop Mask Register
Mnemonic	TP.TCOB0.OB.EPS.FIR.GXSTOP2_MASK_REG
Address	0000000009040016 (SCOM)
Description	Group2 Xstop Mask Reg

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP2_TRIG_IN0: Mask bit for system checkstop.
1	RW	GXSTP2_TRIG_IN1: Mask bit for recoverable error.
2	RW	GXSTP2_TRIG_IN2: Mask bit for special attention.
3	RW	GXSTP2_TRIG_IN3: Mask bit for local checkstop.
4	RW	GXSTP2_TRIG_IN4: Mask bit for type 4 error (host attention).
5	RW	GXSTP2_TRIG_IN5: Mask bit for OOB sys_checkstop Input (0).
6	RW	GXSTP2_TRIG_IN6: Mask bit for OOB sys_checkstop Input (1).
7	RW	GXSTP2_TRIG_IN7: Mask bit for group checkstop input (0).

Bits	SCOM	Field Mnemonic: Description
8	RW	GXSTP2_TRIG_IN8: Mask bit for group checkstop input (1).
9	RW	GXSTP2_TRIG_IN9: Mask bit for debug checkstop on trigger.
10	RW	GXSTP2_TRIG_IN10: Unused.
11	RW	GXSTP2_TRIG_IN11: Unused.

Register Name	Summary Mask Register
Mnemonic	TP.TCOB0.OB.EPS.FIR.SUM_MASK_REG
Address	0000000009040017 (SCOM)
Description	Summary Mask Register

Bits	SCOM	Field Mnemonic: Description
0	RW	SMASK_IN0: System checkstop summary bit.
1	RW	SMASK_IN1: Recoverable summary bit.
2	RW	SMASK_IN2: Special attention summary bit.
3	RW	SMASK_IN3: Local checkstop summary bit.
4	RW	SMASK_IN4: Type4 (host attention) summary bit.

Register Name	Local Checkstop Error Register
Mnemonic	TP.TCOB0.OB.LOCAL_XSTOP_ERR
Address	0000000009040018 (SCOM)
Description	Local Checkstop

Bits	SCOM	Field Mnemonic: Description
0	ROX	LOCAL_XSTOP_IN0: Local checkstop summary bit.
1	ROX	LOCAL_XSTOP_IN1: Local checkstop from IOO, bit 0.
2	ROX	LOCAL_XSTOP_IN2: Local checkstop from IOO PPE, bit 1.
3	ROX	LOCAL_XSTOP_IN3: Unused.
4	ROX	LOCAL_XSTOP_IN4: Unused.
5	ROX	LOCAL_XSTOP_IN5: Unused.
6	ROX	LOCAL_XSTOP_IN6: Unused.
7	ROX	LOCAL_XSTOP_IN7: Unused.
8	ROX	LOCAL_XSTOP_IN8: Unused.
9	ROX	LOCAL_XSTOP_IN9: Unused.
10	ROX	LOCAL_XSTOP_IN10: Unused.
11	ROX	LOCAL_XSTOP_IN11: Unused.
12	ROX	LOCAL_XSTOP_IN12: Unused.
13	ROX	LOCAL_XSTOP_IN13: Unused.
14	ROX	LOCAL_XSTOP_IN14: Unused.
15	ROX	LOCAL_XSTOP_IN15: Unused.

Bits	SCOM	Field Mnemonic: Description
16	ROX	LOCAL_XSTOP_IN16: Unused.
17	ROX	LOCAL_XSTOP_IN17: Unused.
18	ROX	LOCAL_XSTOP_IN18: Unused.
19	ROX	LOCAL_XSTOP_IN19: Unused.
20	ROX	LOCAL_XSTOP_IN20: Unused.
21	ROX	LOCAL_XSTOP_IN21: Unused.
22	ROX	LOCAL_XSTOP_IN22: Unused.

Register Name	Local Checkstop Mask Register
Mnemonic	TP.TCOB0.OB.LOCAL_XSTOP_MASK
Address	0000000009040019 (SCOM)
Description	Local Checkstop Mask

Bits	SCOM	Field Mnemonic: Description
0:21	RW	LOCAL_XSTOP_MASK_IN: Local checkstop mask.

Register Name	Host Attention Mask Register
Mnemonic	TP.TCOB0.OB.HOSTATTN_MASK
Address	000000000904001A (SCOM)
Description	Host Attention Mask

Bits	SCOM	Field Mnemonic: Description
0:21	RW	HOSTATTN_MASK_IN: Host attention mask.

Register Name	DTS Thermal Sensor Result 0 Register
Mnemonic	TP.TCOB0.OB.EPS.THERM.DTS_RESULT0
Address	0000000009050000 (SCOM)
Description	DTS thermal sensor loop1 results

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	DTS_0_RESULT: Calibrated DTS result of sensor with ID 0.
16:31	ROX	DTS_1_RESULT: Calibrated DTS result of sensor with ID 1.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	DTS Trace Result Register
Mnemonic	TP.TCOB0.OB.EPS.THERM.DTS_TRC_RESULT
Address	0000000009050003 (SCOM)
Description	DTS Trace Results

Bits	SCOM	Field Mnemonic: Description
0:43	ROX	TIMESTAMP_COUNTER_VALUE: Time stamp counter value during DTS trace mode.
44	ROX	TIMESTAMP_COUNTER_OVERFLOW_ERR: Over flow error bit of the time stamp counter value during DTS trace mode.
45:47	RO	constant = 0b000
48:63	ROX	DTS_1_RESULT: Calibrated DTS result of sensor with ID 1.

Register Name	Thermal Sensor Mode Register
Mnemonic	TP.TCOB0.OB.EPS.THERM.THERM_MODE_REG
Address	000000000905000F (SCOM)
Description	Enables and controls CPM and DTS.

Bits	SCOM	Field Mnemonic: Description
0	RW	THERM_DIS_CPM_BUBBLE_CORR: Critical path result bubble correction active.
1	RW	THERM_FORCE_THRES_ACT: Forces tpc_therm_thres_mac clock gating off and activates clocks.
2:4	RW	THERM_THRES_TRIP_ENA: Enables therm_thres_trip compare. 1xx = trip0, warning. x1x = trip1, critical. xx1 = trip2, fatal.
5	RW	THERM_DTS_SAMPLE_ENA: 0 = No DTS sampling. 1 = DTS sampling is enabled and a below-counter compare match can occur.
6:9	RW	THERM_SAMPLE_PULSE_CNT: A 16 MHz sample pulse is fed into an 18-bit counter. therm_sample_pulse_cnt enables the selection of a high order bit of the counter to enable resolution of sampling DTSs between 2.5 µs and 80 ms. An edge detection circuit detects the rising edge of the selected counter bit and this triggers a DTS sample. 0000 = 16 ms. 0001 = 8 ms. 0010 = 4 ms. 0011 = 2 ms. 0100 = 1 ms. 0101 = 0.5 ms. 0110 = 250 µs. 0111 = 125 µs. 1000 = 62 .5 µs. 1001 = 31.3 µs. 1010 = 15.6 µs. 1011 = 7.8 µs. 1100 = 3.9 µs. 1101 = 2 µs. 1110 = 1 µs. 1111 = 0.5 µs.
10:11	RW	THERM_THRES_MODE_ENA: Forces maximum or minimum mode in the threshold unit: 00 = Off. 11 = Illegal. 10 = Maximum mode. 01 = Minimum mode.
12	RW	DTS_TRIGGER_MODE: Unused.
13	RW	DTS_TRIGGER_SEL: Unused.

Bits	SCOM	Field Mnemonic: Description
14	RW	THERM_THRES_OVERFLOW_MASK: 0 = therm_overflow_err is enabled. 1 = therm_overflow_err is disabled.
15	RW	THERM_MODE_UNUSED: Unused.
16:19	RW	THERM_DTS_READ_SEL: Selects which DTS result will be provided with PCB read addr_v(4): 0000 = DTS 0. 0001 = DTS 1. 0010 = DTS 2. 0100 = DTS 4. 1111 = Worst case sensor.
20:21	RW	THERM_DTS_ENABLE_L1: Loop1 DTS enables: 1x = DTS 0 available. x1 = DTS 1 available.
22:34	RO	constant = 0b0000000000000
35:36	RW	Reserved field.

Register Name	Skitter Control Register
Mnemonic	TP.TCOB0.OB.EPS.THERM.SKITTER_MODE_REG
Address	0000000009050010 (SCOM)
Description	Skitter Control Register

Bits	SCOM	Field Mnemonic: Description
0	RW	SKITTER_HOLD_SAMPLE: Forces skitter to hold the current sample.
1	RW	DISABLE_SKITTER_STICKINESS: A value of '0' specifies accumulation mode. A value of '1' samples a new value on each cycle and resets the sticky value.
2:3	RW	SKITTER_MODE_UNUSED1: Unused.
4:5	RW	SKITTER_HOLD_DBGTRIG_SEL: bit0 = hold_on_trigger0 bit1 = hold_on_trigger1
6:7	RW	SKITTER_RESET_TRIG_SEL: bit0 = reset_sticky_on_trigger0 bit1 = reset_sticky_on_trigger1
8:9	RW	SKITTER_SAMPLE_GUTS: Selects which guts to measure: 00 = guts1. 01 = guts2. 10 = guts3. 11 = guts4.
10:43	RO	constant = 0b0000000000000000000000000000000000
44	ROX	SKITTER_HOLD_SAMPLE_WITH_TRIGGER: Forces skitter to hold the current sample on debug trigger; this has highest priority.
45	ROX	SKITTER_DATA_V_LT: If set to '1', the data requested by a skitter force read register has finished and data is present in the skitter data register in the collector macro. The data be read by any combination of V25/V26/V27 PCB reads.

Register Name	Error Injection Control Register
Mnemonic	TP.TCOB0.OB.EPS.THERM.INJECT_REG
Address	0000000009050011 (SCOM)
Description	Error Injection Control Register

Bits	SCOM	Field Mnemonic: Description
0:1	RW	THERM_INJECT_TRIP: 00 = No injection. 01 = Warning trip level injection. 10 = Critical trip level injection. 11 = Fatal trip level injection.
2:3	RW	THERM_INJECT_MODE: 00 = No injection. 01 = Injection on the next DTS sample. 10 = Solid injection for the next DTS samples until bit setting changes. 11 = Not used.

Register Name	Thermal Control Register
Mnemonic	TP.TCOB0.OB.EPS.THERM.CONTROL_REG
Address	0000000009050012 (SCOM)
Description	Control / Force Reset Register

Bits	SCOM	Field Mnemonic: Description
0	WO_1P	Reserved field.
1	WO_1P	Reserved field.
2	WO_1P	Reserved field.
3	WO_1P	Reserved field.
4	WO_1P	Reserved field.
5	WO_1P	Reserved field.
6	WO_1P	Reserved field.
7	WO_1P	Reserved field.
8	WO_1P	Reserved field.
9	WO_1P	Reserved field.
10	WO_1P	Reserved field.
11	WO_1P	Reserved field.
12	WO_1P	Reserved field.

Register Name	Thermal Error Status Register
Mnemonic	TP.TCOB0.OB.EPS.THERM.ERR_STATUS_REG
Address	0000000009050013 (SCOM)
Description	Thermal Error Status Register

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	Reserved field.
2	ROX	Reserved field.
3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
7	ROX	Reserved field.
8	ROX	Reserved field.
9	ROX	Reserved field.
10	ROX	Reserved field.
11	ROX	Reserved field.
12	ROX	Reserved field.
13	ROX	Reserved field.
14	ROX	Reserved field.
15	ROX	Reserved field.
16	ROX	SERIAL_SHIFTCNT_MODEREG_PARITY_ERR_MASK: Serial shift count parity error mask.
17	ROX	THERM_MODEREG_PARITY_ERR_MASK: Thermal Mode Register parity error mask.
18	ROX	SKITTER_MODEREG_PARITY_ERR_MASK: Skitter Mode Register parity error mask.
19	ROX	SKITTER_FORCEREG_PARITY_ERR_MASK: Skitter Force Register parity error mask.
20	ROX	SCAN_INIT_VERSION_REG_PARITY_ERR_MASK: Scan Initial Version Register parity error mask.
21	ROX	VOLT_MODEREG_PARITY_ERR_MASK: Volt Mode Register parity error mask.
22	RO	constant = 0b0
23	ROX	COUNT_STATE_ERR_MASK: Count state machine error mask.
24	ROX	RUN_STATE_ERR_MASK: Run state machine error mask.
25	ROX	THRES_STATE_ERR_MASK: Threshold state machine error mask.
26	ROX	OVERFLOW_ERR_MASK: DTS calibration calculation overflow error mask.
27	ROX	SHIFTER_PARITY_ERR_MASK: Shifter parity error mask.
28	ROX	SHIFTER_VALID_ERR_MASK: Shifter valid error mask.
29	ROX	TIMEOUT_ERR_MASK: Timeout error mask.
30	ROX	F_SKITTER_READ_ERR_MASK: Force skitter read error mask.
31	ROX	PCB_ERR_MASK: Pervasive control bus error mask.
32:39	RO	constant = 0b00000000
40:43	ROX	Reserved field.
44:46	ROX	Reserved field.
47	ROX	Reserved field.
48	ROX	Reserved field.
49:50	ROX	Reserved field.
51:54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Skitter Force Read Register
Mnemonic	TP.TCOB0.OB.EPS.THERM.SKITTER_FORCE_REG
Address	0000000009050014 (SCOM)
Description	Skitter Force Read Register

Bits	SCOM	Field Mnemonic: Description
0	RW	F_SKITTER_READ: Forces the read of that particular skitter.

Register Name	Skitter Clock Source Control Register
Mnemonic	TP.TCOB0.OB.EPS.THERM.SKITTER_CLKSRC_REG
Address	0000000009050016 (SCOM)
Description	Skitter clock source control register

Bits	SCOM	Field Mnemonic: Description
0:2	RW	SKITTER0_CLKSRC: Selects the clock to measure: 000: Local mesh clock. 001: External pin skitter_c1_1_in. 010: Local d1clk only if d_mode = 1. 011: External pin skitter_c1_2_in. 100: Local lclk only if d_mode = 1. 101: External pin skitter_c1_3_in. 110: Unused. 111: External pin skitter_c1_4_in.
3:35	RO	constant = 0b000000000000000000000000000000000
36:37	RW	SKITTER0_DELAY_SELECT: Selects the delay to be added between the skitter0 clock source multiplexer and the inverter chain. The base line delay is 12.2 psec. 00 = No delay. 01 = 0.6 psec. 10 = 1.8 psec. 11 = 5 psec.

Register Name	Skitter Data 0 Register
Mnemonic	TP.TCOB0.OB.EPS.THERM.SKITTER_DATA0
Address	0000000009050019 (SCOM)
Description	Skitter Data Register Read Bit0:63

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved.

Register Name	Skitter Data 1 Register
Mnemonic	TP.TCOB0.OB.EPS.THERM.SKITTER_DATA1
Address	000000000905001A (SCOM)
Description	Skitter Data Register Read Bit32:95

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved.

Register Name	Skitter Data 2 Register
Mnemonic	TP.TCOB0.OB.EPS.THERM.SKITTER_DATA2
Address	000000000905001B (SCOM)
Description	Skitter Data Register Read Bit64:127

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved.

Register Name	Timestamp Counter Read Register
Mnemonic	TP.TCOB0.OB.EPS.THERM.TIMESTAMP_COUNTER_READ
Address	000000000905001C (SCOM)
Description	Timestamp Counter Read

Bits	SCOM	Field Mnemonic: Description
0:43	ROX	TIMESTAMP_COUNTER_VALUE: Time stamp counter value during DTS trace mode.
44	ROX	TIMESTAMP_COUNTER_OVERFLOW_ERR: Over flow error bit of the time stamp counter value during DTS trace mode.

6. OB 0 Chiplet PCB Slave

The POWER9 processor registers are listed alphabetically by mnemonic in the following address table.

Mnemonic	Address	Page
TP.TPCHIP.NET.PCBSLOB0.ASSIST_INTERRUPT_REG	0x00000000090F0011	1268
TP.TPCHIP.NET.PCBSLOB0.ATOMIC_LOCK_REG	0x00000000090F03FF	1275
TP.TPCHIP.NET.PCBSLOB0.ATTN_INTERRUPT_REG	0x00000000090F001A	1269
TP.TPCHIP.NET.PCBSLOB0.EDRAM_STATUS	0x00000000090F0029	1273
TP.TPCHIP.NET.PCBSLOB0.ERROR_REG	0x00000000090F001F	1270
TP.TPCHIP.NET.PCBSLOB0.HANG_PULSE_0_REG	0x00000000090F0020	1271
TP.TPCHIP.NET.PCBSLOB0.HANG_PULSE_1_REG	0x00000000090F0021	1271
TP.TPCHIP.NET.PCBSLOB0.HANG_PULSE_2_REG	0x00000000090F0022	1271
TP.TPCHIP.NET.PCBSLOB0.HANG_PULSE_3_REG	0x00000000090F0023	1272
TP.TPCHIP.NET.PCBSLOB0.HANG_PULSE_4_REG	0x00000000090F0024	1272
TP.TPCHIP.NET.PCBSLOB0.HANG_PULSE_5_REG	0x00000000090F0025	1272
TP.TPCHIP.NET.PCBSLOB0.HANG_PULSE_6_REG	0x00000000090F0026	1272
TP.TPCHIP.NET.PCBSLOB0.HEARTBEAT_REG	0x00000000090F0018	1269
TP.TPCHIP.NET.PCBSLOB0.MULTICAST_GROUP_1	0x00000000090F0001	1266
TP.TPCHIP.NET.PCBSLOB0.MULTICAST_GROUP_2	0x00000000090F0002	1266
TP.TPCHIP.NET.PCBSLOB0.MULTICAST_GROUP_3	0x00000000090F0003	1267
TP.TPCHIP.NET.PCBSLOB0.MULTICAST_GROUP_4	0x00000000090F0004	1267
TP.TPCHIP.NET.PCBSLOB0.NET_CTRL0	0x00000000090F0040	1273
TP.TPCHIP.NET.PCBSLOB0.NET_CTRL1	0x00000000090F0044	1274
TP.TPCHIP.NET.PCBSLOB0.PLL_LOCK_REG	0x00000000090F0019	1269
TP.TPCHIP.NET.PCBSLOB0.PRE_COUNTER_REG	0x00000000090F0028	1273
TP.TPCHIP.NET.PCBSLOB0.PRIMARY_ADDRESS_REG	0x00000000090F0000	1265
TP.TPCHIP.NET.PCBSLOB0.PROTECT_MODE_REG	0x00000000090F03FE	1275
TP.TPCHIP.NET.PCBSLOB0.RECOV_INTERRUPT_REG	0x00000000090F001B	1269
TP.TPCHIP.NET.PCBSLOB0.SLAVE_CONFIG_REG	0x00000000090F001E	1270
TP.TPCHIP.NET.PCBSLOB0.TIMEOUT_REG	0x00000000090F0010	1268
TP.TPCHIP.NET.PCBSLOB0.VITAL_SCAN_OUT	0x00000000090F0017	1268
TP.TPCHIP.NET.PCBSLOB0.XSTOP_INTERRUPT_REG	0x00000000090F001C	1269

The POWER9 processor registers are listed in the following tables.

Register Name	**Primary PCB Slave Address Register**
Mnemonic	TP.TPCHIP.NET.PCBSLOB0.PRIMARY_ADDRESS_REG
Address	00000000090F0000 (SCOM)
Description	This register contains the PCB slave's primary address.

Bits	SCOM	Field Mnemonic: Description
0:5	RO	Reserved field. This is the primary_address setting.

Register Name	Multicast Group 1 Register
Mnemonic	TP.TPCHIP.NET.PCBSLOB0.MULTICAST_GROUP_1
Address	00000000090F0001 (SCOM)
Description	Multicast Group Registers 1 – 4 are used to are used to assign chiplets to a specific multicast group within the pervasive connect bus (PCB). Multicast groups make it possible to address more than a single chiplet at a time. They are used to read or write the same resource in multiple chiplets at the same time. **Note:** Multicast groups are initially set up at IPL, but they can be modified at any time by firmware or power management code.

Bits	SCOM	Field Mnemonic: Description
0:2	RO	constant = 0b111
3:5	RW	MULTICAST1_GROUP: Multicast group1 setting. Set this field to a multicast group that this chiplet should be a member of. The chiplet can be assigned to up to four multicast groups by setting this field in the four multicast group registers to the corresponding multicast group numbers. If the chiplet is member of less than four multicast groups, set this field to 0b111 in the multicast group register that is not required. The 0b111 setting indicates multicast group 7; all chiplets are members of multicast group 7 regardless of any multicast register being set to 0b111. 000: Multicast group 0. 001: Multicast group 1. 010: Multicast group 2. 011: Multicast group 3. 100: Multicast group 4 – unused. 101: Multicast group 5 – unused. 110: Multicast group 6 – unused. 111: Multicast group 7.

Register Name	Multicast Group 2 Register
Mnemonic	TP.TPCHIP.NET.PCBSLOB0.MULTICAST_GROUP_2
Address	00000000090F0002 (SCOM)
Description	Multicast Group Registers 1 – 4 are used to are used to assign chiplets to a specific multicast group within the pervasive connect bus (PCB). Multicast groups make it possible to address more than a single chiplet at a time. They are used to read or write the same resource in multiple chiplets at the same time. **Note:** Multicast groups are initially set up at IPL, but they can be modified at any time by firmware or power management code.

Bits	SCOM	Field Mnemonic: Description
0:2	RO	constant = 0b111

Bits	SCOM	Field Mnemonic: Description
3:5	RW	MULTICAST2_GROUP: Multicast group2 setting. Set this field to a multicast group that this chiplet should be a member of. The chiplet can be assigned to up to four multicast groups by setting this field in the four multicast group registers to the corresponding multicast group numbers. If the chiplet is member of less than four multicast groups, set this field to 0b111 in the multicast group register that is not required. The 0b111 setting indicates multicast group 7; all chiplets are members of multicast group 7 regardless of any multicast register being set to 0b111. 000: Multicast group 0. 001: Multicast group 1. 010: Multicast group 2. 011: Multicast group 3. 100: Multicast group 4 – unused. 101: Multicast group 5 – unused. 110: Multicast group 6 – unused. 111: Multicast group 7.

Register Name	Multicast Group 3 Register
Mnemonic	TP.TPCHIP.NET.PCBSLOB0.MULTICAST_GROUP_3
Address	00000000090F0003 (SCOM)
Description	Multicast Group Registers 1 – 4 are used to are used to assign chiplets to a specific multicast group within the pervasive connect bus (PCB). Multicast groups make it possible to address more than a single chiplet at a time. They are used to read or write the same resource in multiple chiplets at the same time. **Note:** Multicast groups are initially set up at IPL, but they can be modified at any time by firmware or power management code.

Bits	SCOM	Field Mnemonic: Description
0:2	RO	constant = 0b111
3:5	RW	MULTICAST3_GROUP: Multicast group3 setting. Set this field to a multicast group that this chiplet should be a member of. The chiplet can be assigned to up to four multicast groups by setting this field in the four multicast group registers to the corresponding multicast group numbers. If the chiplet is member of less than four multicast groups, set this field to 0b111 in the multicast group register that is not required. The 0b111 setting indicates multicast group 7; all chiplets are members of multicast group 7 regardless of any multicast register being set to 0b111. 000: Multicast group 0. 001: Multicast group 1. 010: Multicast group 2. 011: Multicast group 3. 100: Multicast group 4 – unused. 101: Multicast group 5 – unused. 110: Multicast group 6 – unused. 111: Multicast group 7.

Register Name	Multicast Group 4 Register
Mnemonic	TP.TPCHIP.NET.PCBSLOB0.MULTICAST_GROUP_4
Address	00000000090F0004 (SCOM)
Description	Multicast Group Registers 1 – 4 are used to are used to assign chiplets to a specific multicast group within the pervasive connect bus (PCB). Multicast groups make it possible to address more than a single chiplet at a time. They are used to read or write the same resource in multiple chiplets at the same time. **Note:** Multicast groups are initially set up at IPL, but they can be modified at any time by firmware or power management code.

Bits	SCOM	Field Mnemonic: Description
0:2	RO	constant = 0b111
3:5	RW	MULTICAST4_GROUP: Multicast group4 setting. Set this field to a multicast group that this chiplet should be a member of. The chiplet can be assigned to up to four multicast groups by setting this field in the four multicast group registers to the corresponding multicast group numbers. If the chiplet is member of less than four multicast groups, set this field to 0b111 in the multicast group register that is not required. The 0b111 setting indicates multicast group 7; all chiplets are members of multicast group 7 regardless of any multicast register being set to 0b111. 000: Multicast group 0. 001: Multicast group 1. 010: Multicast group 2. 011: Multicast group 3. 100: Multicast group 4 – unused. 101: Multicast group 5 – unused. 110: Multicast group 6 – unused. 111: Multicast group 7.

Register Name	Timeout Select Register
Mnemonic	TP.TPCHIP.NET.PCBSLOB0.TIMEOUT_REG
Address	00000000090F0010 (SCOM)
Description	This register contains the int_timeout setting.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	Reserved field. This is the int_timeout setting.

Register Name	Assist Interrupt Register
Mnemonic	TP.TPCHIP.NET.PCBSLOB0.ASSIST_INTERRUPT_REG
Address	00000000090F0011 (SCOM)
Description	This register contains the attn, recov, and xstop (checkstop) settings.

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. This is the attn setting.
1	ROX	Reserved field. This is the recov setting.
2	ROX	Reserved field. This is the xstop setting.

Register Name	Vital Scan Out Register
Mnemonic	TP.TPCHIP.NET.PCBSLOB0.VITAL_SCAN_OUT
Address	00000000090F0017 (SCOM)
Description	This register contains the vital scan out settings.

Bits	SCOM	Field Mnemonic: Description
0	ROX	RESERVED.

Register Name	Chiplet Heartbeat Register
Mnemonic	TP.TPCHIP.NET.PCBSLOB0.HEARTBEAT_REG
Address	00000000090F0018 (SCOM)
Description	This register indicates whether a chiplet heartbeat is detected.

Bits	SCOM	Field Mnemonic: Description
0	ROX	HEARTBEAT_DEAD: A chiplet heartbeat is not detected.

Register Name	PLL Lock indications Register
Mnemonic	TP.TPCHIP.NET.PCBSLOB0.PLL_LOCK_REG
Address	00000000090F0019 (SCOM)
Description	This register contains lock indications from the PLLs,

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	Reserved field. This is the lock setting.

Register Name	Attention Interrupt Register
Mnemonic	TP.TPCHIP.NET.PCBSLOB0.ATTN_INTERRUPT_REG
Address	00000000090F001A (SCOM)
Description	This register contains the attn setting.

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. This is the attn setting.

Register Name	Recovery Interrupt Register
Mnemonic	TP.TPCHIP.NET.PCBSLOB0.RECOV_INTERRUPT_REG
Address	00000000090F001B (SCOM)
Description	This register contains the recoverable interrupt setting.

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. This is the recov setting.

Register Name	Checkstop Interrupt Register
Mnemonic	TP.TPCHIP.NET.PCBSLOB0.XSTOP_INTERRUPT_REG
Address	00000000090F001C (SCOM)
Description	This register contains the checkstop interrupt setting.

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. This is the xstop setting.

Register Name	Slave Configuration Register
Mnemonic	TP.TPCHIP.NET.PCBSLOB0.SLAVE_CONFIG_REG
Address	00000000090F001E (SCOM)
Description	This is the slave configuration register.

Bits	SCOM	Field Mnemonic: Description
0	RW	CFG_DISABLE_PERV_THOLD_CHECK: This bit disables the pervasive threshold check.
1	RW	CFG_DISABLE_MALF_PULSE_GEN: This bit disables pulse generation for a malfunction alert. Switch back to level.
2	RW	CFG_STOP_HANG_CNT_SYS_XSTP: This bit disables the hang counter stop for a system checkstop.
3	RW	CFG_DISABLE_CL_ATOMIC_LOCK: This bit disables the atomic lock for chiplet accesses.
4	RW	CFG_DISABLE_HEARTBEAT: This bit disables the check for voltage and gridclock in the chiplet.
5	RW	CFG_DISABLE_FORCE_TO_ZERO: This bit disables the force to zero for error cases.
6	RW	CFG_PM_DISABLE: This bit disables the power management set/reset interface for net_ctrl registers.
7	RW	CFG_PM_MUX_DISABLE: This bit disables the power-management multiplex request signal.
8:13	RW	ERROR_MASK: These are mask bits for slave error reporting.
14:15	RW	RESERVED.

Register Name	Error Capture Register
Mnemonic	TP.TPCHIP.NET.PCBSLOB0.ERROR_REG
Address	00000000090F001F (SCOM)
Description	This register is used to capture errors.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	CE_ERROR: Correctable error on the PCB bus.
1:3	RWX_WCLEAR	CHIPLET_ERRORS: Errors reported by the chiplet. 000 = No error. 001 = XSCOM command blocked due to pending errors. 010 = Chiplet offline. 011 = Partial good. 100 = Invalid address, address error, or bad access type. 101 = Clock error. 110 = Parity error, received unexpected packet, or wrong packet number. 111 = Timeout. This register is for debug purposes only. It only holds meaningful data if it is cleared after each error.
4	RWX_WCLEAR	PARITY_ERROR: Parity error on the PCB interface.
5	RWX_WCLEAR	DATA_BUFFER_ERROR: Parity error in the data buffer.
6	RWX_WCLEAR	ADDR_BUFFER_ERROR: Parity error in the address buffer.
7	RWX_WCLEAR	PCB_FSM_ERROR: Invalid state error in the PCB FSM.
8	RWX_WCLEAR	CL_FSM_ERROR: Invalid state error in the chiplet FSM.
9	RWX_WCLEAR	INT_RX_FSM_ERROR: Invalid state error in the interrupt RX FSM.
10	RWX_WCLEAR	INT_TX_FSM_ERROR: Invalid state error in the interrupt TX FSM.
11	RWX_WCLEAR	INT_TYPE_ERROR: Invalid interrupt type.
12	RWX_WCLEAR	CL_DATA_ERROR: Parity error on the chiplet interface.

Bits	SCOM	Field Mnemonic: Description
13	RWX_WCLEAR	INFO_ERROR: Parity error on the chiplet information lines.
14	RWX_WCLEAR	UNUSED_0:
15	RWX_WCLEAR	CHIPLET_ATOMIC_LOCK_ERROR: Chiplet atomic lock error.
16	RWX_WCLEAR	PCB_INTERFACE_ERROR: Error on the PCB interface component for the internal endpoint.
17	RWX_WCLEAR	CHIPLET_OFFLINE: A heartbeat check indicated that the chiplet is offline.
18	RWX_WCLEAR	EDRAM_SEQUENCE_ERR: Error in the eDRAM power-up sequence.
19	RWX_WCLEAR	CTRL_REG_PARITY_ERROR: The control register parity is bad.
20	RWX_WCLEAR	ADDRESS_REG_PARITY_ERROR: The address register parity is bad.
21	RWX_WCLEAR	TIMEOUT_REG_PARITY_ERROR: The timeout select register parity is bad.
22	RWX_WCLEAR	CONFIG_REG_PARITY_ERROR: The slave configuration register parity is bad.
23	RWX_WCLEAR	UNUSED_1:
24	RWX_WCLEAR	DIV_REG_PARITY_ERROR: The divider register parity is bad.
25:28	RWX_WCLEAR	PLL_UNLOCK_ERROR: Unlock from the chiplet PLL.

Register Name	Hang Pulse Generation Register 0
Mnemonic	TP.TPCHIP.NET.PCBSLOB0.HANG_PULSE_0_REG
Address	00000000090F0020 (SCOM)
Description	This register contains hang pulse 0 information.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_0: This field contains the value of hang pulse 0. The time period equals 2^{value} x (precounter_reg + 1) / pcb_freq. The range of valid values is 34 – 0.
6	RW	SUPPRESS_HANG_0: If set to '1', hang pulses are suppressed in case of a checkstop.

Register Name	Hang Pulse Generation Register 1
Mnemonic	TP.TPCHIP.NET.PCBSLOB0.HANG_PULSE_1_REG
Address	00000000090F0021 (SCOM)
Description	This register contains hang pulse 1 information.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_1: This field contains the value of hang pulse 1. The time period equals 2^{value} x (precounter_reg + 1) / pcb_freq. The range of valid values is 34 – 0.
6	RW	SUPPRESS_HANG_1: If set to '1', hang pulses are suppressed in case of a checkstop.

Register Name	Hang Pulse Generation Register 2
Mnemonic	TP.TPCHIP.NET.PCBSLOB0.HANG_PULSE_2_REG
Address	00000000090F0022 (SCOM)
Description	This register contains hang pulse 2 information.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_2: This field contains the value of hang pulse 2. The time period equals 2^{value} x (precounter_reg + 1) / pcb_freq. The range of valid values is 34 – 0.
6	RW	SUPPRESS_HANG_2: If set to '1', hang pulses are suppressed in case of a checkstop.

Register Name	Hang Pulse Generation Register 3
Mnemonic	TP.TPCHIP.NET.PCBSLOB0.HANG_PULSE_3_REG
Address	00000000090F0023 (SCOM)
Description	This register contains hang pulse 3 information.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_3: This field contains the value of hang pulse 3. The time period equals 2^{value} x (precounter_reg + 1) / pcb_freq. The range of valid values is 34 – 0.
6	RW	SUPPRESS_HANG_3: If set to '1', hang pulses are suppressed in case of a checkstop.

Register Name	Hang Pulse Generation Register 4
Mnemonic	TP.TPCHIP.NET.PCBSLOB0.HANG_PULSE_4_REG
Address	00000000090F0024 (SCOM)
Description	This register contains hang pulse 4 information.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_4: This field contains the value of hang pulse 4. The time period equals 2^{value} x (precounter_reg + 1) / pcb_freq. The range of valid values is 34 – 0.
6	RW	SUPPRESS_HANG_4: If set to '1', hang pulses are suppressed in case of a checkstop.

Register Name	Hang Pulse Generation Register 5
Mnemonic	TP.TPCHIP.NET.PCBSLOB0.HANG_PULSE_5_REG
Address	00000000090F0025 (SCOM)
Description	This register contains hang pulse 5 information. This hang counter is exclusively used to generate the malfunction alert pulse.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_5: This field contains the value of hang pulse 5. The time period equals 2^{value} x (precounter_reg + 1) / pcb_freq. The range of valid values is 34 – 0.
6	RW	SUPPRESS_HANG_5: If set to '1', hang pulses are suppressed in case of a checkstop.

Register Name	Hang Pulse Generation Register 6
Mnemonic	TP.TPCHIP.NET.PCBSLOB0.HANG_PULSE_6_REG
Address	00000000090F0026 (SCOM)
Description	This register contains hang pulse 6 information. This hang counter is exclusively used for heartbeat generation.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_6: This field contains the value of hang pulse 6. The time period equals 2^{value} x (precounter_reg + 1) / pcb_freq. The range of valid values is 34 – 0.
6	RW	SUPPRESS_HANG_6: If set to '1', hang pulses are suppressed in case of a checkstop.

Register Name	**Hang Counter Clock Divider Register**
Mnemonic	TP.TPCHIP.NET.PCBSLOB0.PRE_COUNTER_REG
Address	00000000090F0028 (SCOM)
Description	This register is the divider for the hang counter clock.

Bits	SCOM	Field Mnemonic: Description
0:7	RW	PRE_COUNTER: This field is the divider for the hang counter clock. It divides the clock by n + 1. (The default is n = 0).

Register Name	**eDRAM Control Status Register**
Mnemonic	TP.TPCHIP.NET.PCBSLOB0.EDRAM_STATUS
Address	00000000090F0029 (SCOM)
Description	This register contains the eDRAM control status.

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	EDRAM_STAT: This field contains the eDRAM control status.

Register Name	**NET CTRL0 Register**
Mnemonic	TP.TPCHIP.NET.PCBSLOB0.NET_CTRL0
Address	00000000090F0040 (SCOM) 00000000090F0041 (SCOM1) 00000000090F0042 (SCOM2)
Description	This register contains NET controls. It is not applicable to the pervasive chiplet.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	CHIPLET_ENABLE: This bit is set if the chiplet is good.
1	RWX	RWX_WAND	RWX_WOR	PCB_EP_RESET: The output is ORed to the global EP reset.
2	RWX	RWX_WAND	RWX_WOR	CLK_ASYNC_RESET: POWER9 cache chiplet: EQ skew adjust reset. POWER9 core chiplet: Core duty cycle adjust reset. POWER9 memory chiplet: Memory glitchless multiplexer asynchronous reset.
3	RWX	RWX_WAND	RWX_WOR	PLL_TEST_EN: Test enable for the chiplet PLL.
4	RWX	RWX_WAND	RWX_WOR	PLL_RESET: Reset for the chiplet PLL.
5	RWX	RWX_WAND	RWX_WOR	PLL_BYPASS: Enable bypass for the chiplet PLL.
6	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN: Scan control for the chiplet vital domain.
7	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN_IN: Scan in for the chiplet vital domain.
8	RWX	RWX_WAND	RWX_WOR	VITAL_PHASE: Phase for the vital domain.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
9	RWX	RWX_WAND	RWX_WOR	FLUSH_ALIGN_OVR: When set to 1, this mechanism overrides automatic control by the clock controller of the flush, flush_nto1, and align signals in the chiplet.
10	RWX	RWX_WAND	RWX_WOR	VITAL_AL: Align for the vital domain.
11	RWX	RWX_WAND	RWX_WOR	ACT_DIS: ACT disable control for LCBs in the vital logic.
12	RWX	RWX_WAND	RWX_WOR	MPW1: Modify pulse width 1 (MPW1) control for LCBs in the vital logic.
13	RWX	RWX_WAND	RWX_WOR	MPW2: Modify pulse width 2 (MPW2) control for LCBs in the vital logic.
14	RWX	RWX_WAND	RWX_WOR	MPW3: Modify pulse width 3 (MPW3) control for LCBs in the vital logic.
15	RWX	RWX_WAND	RWX_WOR	DELAY_LCLKR: LCB control signal for the vital logic.
16	RWX	RWX_WAND	RWX_WOR	VITAL_THOLD: Threshold for the chiplet vital domain.
17	RWX	RWX_WAND	RWX_WOR	FLUSH_SCAN_N: Flush scan control.
18	RWX	RWX_WAND	RWX_WOR	FENCE_EN: Fencing signal for the chiplet.
19	RWX	RWX_WAND	RWX_WOR	CPLT_RCTRL: Chiplet receiver enable.
20	RWX	RWX_WAND	RWX_WOR	CPLT_DCTRL: Chiplet driver enable.
21	RWX	RWX_WAND	RWX_WOR	Reserved field. This is the pm_access setting.
22	RWX	RWX_WAND	RWX_WOR	ADJ_FUNC_CLKSEL: POWER9 cache chiplet: Clock select for the skew adjust/duty cycle adjust logic. POWER9 core chiplet: Skew sense to skew adjust fencing.
23:24	RWX	RWX_WAND	RWX_WOR	Reserved field. This is the pm_access setting.
25	RWX	RWX_WAND	RWX_WOR	TP_FENCE_PCB: Fence the chiplet from the PCB bus. If set, the PCB slave reports “Chiplet Offline.”
26	RWX	RWX_WAND	RWX_WOR	LVLTRANS_FENCE: Fence control for the level translators.
27	RWX	RWX_WAND	RWX_WOR	ARRAY_WRITE_ASSIST_EN: Array write assist.
28	RWX	RWX_WAND	RWX_WOR	HTB_INTEST: HTB intest mode.
29	RWX	RWX_WAND	RWX_WOR	HTB_EXTEST: HTB intest mode.
30	RWX	RWX_WAND	RWX_WOR	Reserved field. This is the pm_access setting.
31	RWX	RWX_WAND	RWX_WOR	PLLFORCE_OUT_EN: PLL force out enable.

Register Name	NET CTRL1 Register
Mnemonic	TP.TPCHIP.NET.PCBSLOB0.NET_CTRL1
Address	00000000090F0044 (SCOM) 00000000090F0045 (SCOM1) 00000000090F0046 (SCOM2)
Description	This register contains NET controls. It is not applicable to the pervasive chiplet.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	PLL_CLKIN_SEL: PLL clkin select.
1	RWX	RWX_WAND	RWX_WOR	CLK_DCC_BYPASS_EN: POWER9 cache chiplet: L2-0, L2-1, L3 duty cycle control bypass. POWER9 core chiplet: Core duty cycle control bypass. POWER9 memory chiplet: Memory duty cycle control bypass.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
2	RWX	RWX_WAND	RWX_WOR	CLK_PDLY_BYPASS_EN: POWER9 cache chiplet: L2-0, L2-1, L3 programmable delay bypass. POWER9 core chiplet: Core programmable delay bypass. POWER9 memory chiplet: Memory programmable delay bypass.
3	RWX	RWX_WAND	RWX_WOR	CLK_DIV_BYPASS_EN: Enable clock divider bypass.
4	RWX	RWX_WAND	RWX_WOR	REFCLK_CLKMUX0_SEL: Select for reference clock mux0.
5	RWX	RWX_WAND	RWX_WOR	REFCLK_CLKMUX1_SEL: Select for reference clock mux1.
6	RWX	RWX_WAND	RWX_WOR	PLL_BNDY_BYPASS_EN: Bypass for IOP PLL.
7	RWX	RWX_WAND	RWX_WOR	Reserved field. This is the pcb_access setting.
8:15	RWX	RWX_WAND	RWX_WOR	DPLL_TEST_SEL: DPLL testout multiplexing.
16:19	RWX	RWX_WAND	RWX_WOR	SB_STRENGTH: Sector buffer driver strength.
20	RWX	RWX_WAND	RWX_WOR	ASYNC_TYPE: This is a control signal for testing latches with asynchronous set and reset capabilities.
21	RWX	RWX_WAND	RWX_WOR	ASYNC_OBS: This is a control signal for testing latches with asynchronous set and reset capabilities.
22	RWX	RWX_WAND	RWX_WOR	CPM_CAL_SET: CPM calibrate.
23	RWX	RWX_WAND	RWX_WOR	SENSEADJ_RESET0: POWER9 cache chiplet: L2-0 duty cycle adjust reset.
24	RWX	RWX_WAND	RWX_WOR	SENSEADJ_RESET1: POWER9 cache chiplet: L2-1 duty cycle adjust reset.
25	RWX	RWX_WAND	RWX_WOR	CLK_PULSE_EN: Clock pulse mode enable.
26:27	RWX	RWX_WAND	RWX_WOR	CLK_PULSE_MODE: Clock pulse mode setting.
28:31	RWX	RWX_WAND	RWX_WOR	Reserved field. This is the pcb_access setting.

Register Name	Protect Mode Register
Mnemonic	TP.TPCHIP.NET.PCBSLOB0.PROTECT_MODE_REG
Address	00000000090F03FE (SCOM)
Description	This register is used to enable read and write protection.

Bits	SCOM	Field Mnemonic: Description
0	RW	READ_PROTECT_ENABLE: Enable read protection.
1	RW	WRITE_PROTECT_ENABLE: Enable write protection.

Register Name	Atomic Lock Register
Mnemonic	TP.TPCHIP.NET.PCBSLOB0.ATOMIC_LOCK_REG
Address	00000000090F03FF (SCOM)
Description	This register contains atomic lock information.

Bits	SCOM	Field Mnemonic: Description
0	RW	ATOMIC_LOCK_ENABLE: This bit enables the atomic lock.
1:4	ROX	ATOMIC_ID: This field contains the atomic ID.
5:7	RO	constant = 0b000

Bits	SCOM	Field Mnemonic: Description
8:15	ROX	ATOMIC_ACTIVITY: This is the atomic lock counter.

7. OB 0 Chiplet Indirect

The POWER9 processor registers are listed alphabetically by mnemonic in the following address table.

Mnemonic	Address	Page
IOO0.IOO_CPLT.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.RX_FIR_ERROR_INJECT_PB	0x800F980009010C3F	1848
IOO0.IOO_CPLT.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.RX_FIR_MASK_PB	0x800F900009010C3F	1848
IOO0.IOO_CPLT.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.RX_FIR_PB	0x800F880009010C3F	1848
IOO0.IOO_CPLT.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.RX_FIR_RESET_PB	0x800F800009010C3F	1847
IOO0.IOO_CPLT.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.SPARE_MODE_PB	0x800F340009010C3F	1847
IOO0.IOO_CPLT.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.TX_IMPCAL2_PB	0x800F3C0009010C3F	1847
IOO0.IOO_CPLT.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.TX_IMPCAL_NVAL_PB	0x800F0C0009010C3F	1844
IOO0.IOO_CPLT.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.TX_IMPCAL_PB	0x800F040009010C3F	1844
IOO0.IOO_CPLT.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.TX_IMPCAL_PVAL_PB	0x800F140009010C3F	1845
IOO0.IOO_CPLT.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.TX_IMPCAL_P_4X_PB	0x800F1C0009010C3F	1845
IOO0.IOO_CPLT.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.TX_IMPCAL_SWO1_PB	0x800F240009010C3F	1845
IOO0.IOO_CPLT.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.TX_IMPCAL_SWO2_PB	0x800F2C0009010C3F	1846
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL10_EO_PG	0x8009200009010C3F	1823
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL11_EO_PG	0x8009280009010C3F	1823
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL12_EO_PG	0x8009300009010C3F	1824
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL13_EO_PG	0x8009380009010C3F	1824
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL14_EO_PG	0x8009400009010C3F	1824
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL1_EO_PG	0x8008D80009010C3F	1819
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL2_EO_PG	0x8008E00009010C3F	1820
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL3_EO_PG	0x8008E80009010C3F	1821
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL4_EO_PG	0x8008F00009010C3F	1821
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL5_EO_PG	0x8008F80009010C3F	1821
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL6_EO_PG	0x8009000009010C3F	1822
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL8_EO_PG	0x8009100009010C3F	1822
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL9_EO_PG	0x8009180009010C3F	1822
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTLX7_EO_PG	0x8009080009010C3F	1822
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE10_EO_PG	0x8008580009010C3F	1813
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE11_EO_PG	0x8008600009010C3F	1814
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE12_EO_PG	0x8008680009010C3F	1814
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE13_EO_PG	0x8008700009010C3F	1815
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE14_EO_PG	0x8008780009010C3F	1815
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE15_EO_PG	0x8008800009010C3F	1815
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE16_EO_PG	0x8008880009010C3F	1816
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE17_EO_PG	0x8008900009010C3F	1816
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE18_EO_PG	0x8008980009010C3F	1816
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE19_EO_PG	0x8008A00009010C3F	1817
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE1_EO_PG	0x8008100009010C3F	1811
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE1_O_PG	0x8009B00009010C3F	1827
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE20_EO_PG	0x8008A80009010C3F	1817
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE21_EO_PG	0x8008B00009010C3F	1817
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE22_EO_PG	0x8008B80009010C3F	1818
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE23_EO_PG	0x8008C00009010C3F	1818

Mnemonic	Address	Page
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE24_EO_PG	0x8008C80009010C3F	1819
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE26_EO_PG	0x8009680009010C3F	1825
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE27_EO_PG	0x8009700009010C3F	1826
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE28_EO_PG	0x8009780009010C3F	1826
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE29_EO_PG	0x8008D00009010C3F	1819
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE2_EO_PG	0x8008180009010C3F	1812
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE2_O_PG	0x8009880009010C3F	1827
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE5_EO_PG	0x8008300009010C3F	1812
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE6_EO_PG	0x8008380009010C3F	1812
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE7_EO_PG	0x8008400009010C3F	1813
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE9_EO_PG	0x8008500009010C3F	1813
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_STAT1_EO_PG	0x8009500009010C3F	1825
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_STAT2_EO_PG	0x8009580009010C3F	1825
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_ID1_PG	0x8008080009010C3F	1811
IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_SPARE_MODE_PG	0x8008000009010C3F	1810
IOO0.IOO_CPLT.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_CNTLX1_EO_PG	0x800B880009010C3F	1832
IOO0.IOO_CPLT.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_SPARE_MODE_PG	0x800B800009010C3F	1832
IOO0.IOO_CPLT.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT10_EO_PG	0x800BD80009010C3F	1835
IOO0.IOO_CPLT.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT11_EO_PG	0x800BE00009010C3F	1835
IOO0.IOO_CPLT.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT1_EO_PG	0x800B900009010C3F	1833
IOO0.IOO_CPLT.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT2_EO_PG	0x800B980009010C3F	1833
IOO0.IOO_CPLT.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT3_EO_PG	0x800BA00009010C3F	1833
IOO0.IOO_CPLT.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT4_EO_PG	0x800BA80009010C3F	1833
IOO0.IOO_CPLT.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT5_EO_PG	0x800BB00009010C3F	1834
IOO0.IOO_CPLT.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT6_EO_PG	0x800BB80009010C3F	1834
IOO0.IOO_CPLT.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT7_EO_PG	0x800BC00009010C3F	1834
IOO0.IOO_CPLT.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT8_EO_PG	0x800BC80009010C3F	1834
IOO0.IOO_CPLT.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT9_EO_PG	0x800BD00009010C3F	1835
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.REGS.RX_FIR1_ERROR_INJECT_PG	0x800A980009010C3F	1829
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.REGS.RX_FIR1_MASK_PG	0x800A900009010C3F	1828
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.REGS.RX_FIR1_PG	0x800A880009010C3F	1828
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_CNTL2_EO_PG	0x800AE00009010C3F	1831
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_CNTL3_EO_PG	0x800AE80009010C3F	1831
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_CNTL4_EO_PG	0x800AF00009010C3F	1831
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_CNTLX1_EO_PG	0x800AB00009010C3F	1829
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_SPARE_MODE_PG	0x800A800009010C3F	1827
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_STAT1_EO_PG	0x800AB80009010C3F	1829
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_STAT2_EO_PG	0x800AC00009010C3F	1830
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_STAT3_EO_PG	0x800AC80009010C3F	1830
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_STAT4_EO_PG	0x800AD00009010C3F	1830
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_STAT5_EO_PG	0x800AD80009010C3F	1830
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#0.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL	0x8003300009010C3F	1672
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#0.PLREGS.RX_GLBSM_PL_CNTL1_O_PL	0x8003200009010C3F	1655
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#0.PLREGS.RX_GLBSM_PL_STAT1_O_PL	0x8003280009010C3F	1664
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#1.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL	0x8003300109010C3F	1673
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#1.PLREGS.RX_GLBSM_PL_CNTL1_O_PL	0x8003200109010C3F	1656
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#1.PLREGS.RX_GLBSM_PL_STAT1_O_PL	0x8003280109010C3F	1665
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#10.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL	0x8003300A09010C3F	1676

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IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#10.PLREGS.RX_GLBSM_PL_CNTL1_O_PL	0x8003200A09010C3F	1659
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#10.PLREGS.RX_GLBSM_PL_STAT1_O_PL	0x8003280A09010C3F	1668
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#11.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL	0x8003300B09010C3F	1676
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#11.PLREGS.RX_GLBSM_PL_CNTL1_O_PL	0x8003200B09010C3F	1660
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#11.PLREGS.RX_GLBSM_PL_STAT1_O_PL	0x8003280B09010C3F	1668
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#12.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL	0x8003300C09010C3F	1676
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#12.PLREGS.RX_GLBSM_PL_CNTL1_O_PL	0x8003200C09010C3F	1660
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#12.PLREGS.RX_GLBSM_PL_STAT1_O_PL	0x8003280C09010C3F	1668
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#13.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL	0x8003300D09010C3F	1677
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#13.PLREGS.RX_GLBSM_PL_CNTL1_O_PL	0x8003200D09010C3F	1660
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#13.PLREGS.RX_GLBSM_PL_STAT1_O_PL	0x8003280D09010C3F	1669
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#14.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL	0x8003300E09010C3F	1677
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#14.PLREGS.RX_GLBSM_PL_CNTL1_O_PL	0x8003200E09010C3F	1661
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#14.PLREGS.RX_GLBSM_PL_STAT1_O_PL	0x8003280E09010C3F	1669
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#15.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL	0x8003300F09010C3F	1677
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#15.PLREGS.RX_GLBSM_PL_CNTL1_O_PL	0x8003200F09010C3F	1661
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#15.PLREGS.RX_GLBSM_PL_STAT1_O_PL	0x8003280F09010C3F	1669
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#16.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL	0x8003301009010C3F	1678
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#16.PLREGS.RX_GLBSM_PL_CNTL1_O_PL	0x8003201009010C3F	1661
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#16.PLREGS.RX_GLBSM_PL_STAT1_O_PL	0x8003281009010C3F	1670
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#17.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL	0x8003301109010C3F	1678
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#17.PLREGS.RX_GLBSM_PL_CNTL1_O_PL	0x8003201109010C3F	1662
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#17.PLREGS.RX_GLBSM_PL_STAT1_O_PL	0x8003281109010C3F	1670
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#18.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL	0x8003301209010C3F	1678
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#18.PLREGS.RX_GLBSM_PL_CNTL1_O_PL	0x8003201209010C3F	1662
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#18.PLREGS.RX_GLBSM_PL_STAT1_O_PL	0x8003281209010C3F	1670
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#19.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL	0x8003301309010C3F	1679
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IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#19.PLREGS.RX_GLBSM_PL_STAT1_O_PL	0x8003281309010C3F	1671
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#2.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL	0x8003300209010C3F	1673
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#2.PLREGS.RX_GLBSM_PL_CNTL1_O_PL	0x8003200209010C3F	1656
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#2.PLREGS.RX_GLBSM_PL_STAT1_O_PL	0x8003280209010C3F	1665
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#20.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL	0x8003301409010C3F	1679
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#20.PLREGS.RX_GLBSM_PL_CNTL1_O_PL	0x8003201409010C3F	1663
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#20.PLREGS.RX_GLBSM_PL_STAT1_O_PL	0x8003281409010C3F	1671
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#21.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL	0x8003301509010C3F	1679
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#21.PLREGS.RX_GLBSM_PL_CNTL1_O_PL	0x8003201509010C3F	1663
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#21.PLREGS.RX_GLBSM_PL_STAT1_O_PL	0x8003281509010C3F	1671
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#22.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL	0x8003301609010C3F	1680
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#22.PLREGS.RX_GLBSM_PL_CNTL1_O_PL	0x8003201609010C3F	1664
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#22.PLREGS.RX_GLBSM_PL_STAT1_O_PL	0x8003281609010C3F	1672
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#23.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL	0x8003301709010C3F	1680
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#23.PLREGS.RX_GLBSM_PL_CNTL1_O_PL	0x8003201709010C3F	1664
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#23.PLREGS.RX_GLBSM_PL_STAT1_O_PL	0x8003281709010C3F	1672
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#3.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL	0x8003300309010C3F	1673
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#3.PLREGS.RX_GLBSM_PL_CNTL1_O_PL	0x8003200309010C3F	1657
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#3.PLREGS.RX_GLBSM_PL_STAT1_O_PL	0x8003280309010C3F	1665
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#4.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL	0x8003300409010C3F	1674

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IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#4.PLREGS.RX_GLBSM_PL_CNTL1_O_PL	0x8003200409010C3F	1657
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#4.PLREGS.RX_GLBSM_PL_STAT1_O_PL	0x8003280409010C3F	1666
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#5.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL	0x8003300509010C3F	1674
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#5.PLREGS.RX_GLBSM_PL_CNTL1_O_PL	0x8003200509010C3F	1657
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#5.PLREGS.RX_GLBSM_PL_STAT1_O_PL	0x8003280509010C3F	1666
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#6.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL	0x8003300609010C3F	1674
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#6.PLREGS.RX_GLBSM_PL_CNTL1_O_PL	0x8003200609010C3F	1658
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#6.PLREGS.RX_GLBSM_PL_STAT1_O_PL	0x8003280609010C3F	1666
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#7.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL	0x8003300709010C3F	1675
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#7.PLREGS.RX_GLBSM_PL_CNTL1_O_PL	0x8003200709010C3F	1658
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#7.PLREGS.RX_GLBSM_PL_STAT1_O_PL	0x8003280709010C3F	1667
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#8.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL	0x8003300809010C3F	1675
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#8.PLREGS.RX_GLBSM_PL_CNTL1_O_PL	0x8003200809010C3F	1658
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#8.PLREGS.RX_GLBSM_PL_STAT1_O_PL	0x8003280809010C3F	1667
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#9.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL	0x8003300909010C3F	1675
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#9.PLREGS.RX_GLBSM_PL_CNTL1_O_PL	0x8003200909010C3F	1659
IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#9.PLREGS.RX_GLBSM_PL_STAT1_O_PL	0x8003280909010C3F	1667
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x8002480009010C3F	1572
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x8002500009010C3F	1592
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x8002580009010C3F	1601
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x8002600009010C3F	1610
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x8002400009010C3F	1560
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x8002200009010C3F	1520
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x8002280009010C3F	1531
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IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x8002680009010C3F	1618
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL	0x8003180009010C3F	1649
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x8002700009010C3F	1624
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x8002780009010C3F	1634
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL	0x8002800009010C3F	1641
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x8002180009010C3F	1513
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x8002100009010C3F	1507
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_PL	0x8002080009010C3F	1501

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IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x8002000009010C3F	1491
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL	0x8000C80009010C3F	1484
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x8000080009010C3F	1336
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL	0x8000800009010C3F	1408
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x8000100009010C3F	1348
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IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x8000180009010C3F	1360
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL	0x8000900009010C3F	1426
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x8000200009010C3F	1368
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL	0x8000980009010C3F	1434
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x8000280009010C3F	1376
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL	0x8000A00009010C3F	1443
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x8000300009010C3F	1385
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL	0x8000A80009010C3F	1450
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x8000380009010C3F	1393
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL	0x8000B00009010C3F	1458
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x8000400009010C3F	1401
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL	0x8000B80009010C3F	1466
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL	0x8000C00009010C3F	1475
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x8000000009010C3F	1325
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x8002480109010C3F	1573
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x8002500109010C3F	1592
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x8002580109010C3F	1601
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IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x8002400109010C3F	1561
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x8002200109010C3F	1520
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x8002280109010C3F	1531

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IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x8002300109010C3F	1540
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL	0x8002380109010C3F	1549
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x8002680109010C3F	1618
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL	0x8003180109010C3F	1649
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x8002700109010C3F	1624
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x8002780109010C3F	1635
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IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x8002180109010C3F	1513
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x8002100109010C3F	1507
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_PL	0x8002080109010C3F	1501
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x8002000109010C3F	1491
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL	0x8000C80109010C3F	1484
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x8000080109010C3F	1337
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL	0x8000800109010C3F	1408
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x8000100109010C3F	1349
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL	0x8000880109010C3F	1418
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x8000180109010C3F	1361
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL	0x8000900109010C3F	1426
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x8000200109010C3F	1369
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL	0x8000980109010C3F	1435
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x8000280109010C3F	1377
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL	0x8000A00109010C3F	1444
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x8000300109010C3F	1386
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL	0x8000A80109010C3F	1451
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x8000380109010C3F	1394
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL	0x8000B00109010C3F	1459
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x8000400109010C3F	1402

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IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL	0x8000B80109010C3F	1467
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL	0x8000C00109010C3F	1475
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x8000000109010C3F	1326
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x8002480209010C3F	1574
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x8002500209010C3F	1593
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x8002580209010C3F	1602
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x8002600209010C3F	1611
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x8002400209010C3F	1561
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x8002200209010C3F	1521
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x8002280209010C3F	1531
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x8002300209010C3F	1541
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL	0x8002380209010C3F	1549
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x8002680209010C3F	1618
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL	0x8003180209010C3F	1649
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x8002700209010C3F	1624
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x8002780209010C3F	1635
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL	0x8002800209010C3F	1642
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x8002180209010C3F	1514
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x8002100209010C3F	1507
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_PL	0x8002080209010C3F	1501
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x8002000209010C3F	1491
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL	0x8000C80209010C3F	1484
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x8000080209010C3F	1337
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL	0x8000800209010C3F	1409
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x8000100209010C3F	1349
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL	0x8000880209010C3F	1418
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x8000180209010C3F	1361

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IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL	0x8000900209010C3F	1427
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x8000200209010C3F	1369
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL	0x8000980209010C3F	1435
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x8000280209010C3F	1377
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL	0x8000A00209010C3F	1444
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x8000300209010C3F	1386
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL	0x8000A80209010C3F	1451
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x8000380209010C3F	1394
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL	0x8000B00209010C3F	1459
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x8000400209010C3F	1402
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL	0x8000B80209010C3F	1467
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL	0x8000C00209010C3F	1475
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x8000000209010C3F	1326
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x8002480309010C3F	1575
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x8002500309010C3F	1593
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x8002580309010C3F	1602
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x8002600309010C3F	1611
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IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x8002200309010C3F	1521
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x8002280309010C3F	1532
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x8002300309010C3F	1541
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IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x8002680309010C3F	1618
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IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x8002700309010C3F	1625
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x8002780309010C3F	1635
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL	0x8002800309010C3F	1642

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IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x8002180309010C3F	1514
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x8002100309010C3F	1508
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_PL	0x8002080309010C3F	1502
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x8002000309010C3F	1492
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL	0x8000C80309010C3F	1485
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x8000080309010C3F	1338
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL	0x8000800309010C3F	1409
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x8000100309010C3F	1350
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL	0x8000880309010C3F	1418
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x8000180309010C3F	1361
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL	0x8000900309010C3F	1427
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x8000200309010C3F	1369
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL	0x8000980309010C3F	1436
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x8000280309010C3F	1377
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL	0x8000A00309010C3F	1444
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x8000300309010C3F	1386
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL	0x8000A80309010C3F	1451
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x8000380309010C3F	1394
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL	0x8000B00309010C3F	1459
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x8000400309010C3F	1402
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL	0x8000B80309010C3F	1467
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL	0x8000C00309010C3F	1476
IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x8000000309010C3F	1327
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x8002480409010C3F	1575
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x8002500409010C3F	1594
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x8002580409010C3F	1602
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x8002600409010C3F	1612

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IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x8002400409010C3F	1562
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x8002200409010C3F	1522
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x8002280409010C3F	1532
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x8002300409010C3F	1541
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL	0x8002380409010C3F	1550
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x8002680409010C3F	1619
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL	0x8003180409010C3F	1650
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x8002700409010C3F	1625
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x8002780409010C3F	1636
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL	0x8002800409010C3F	1643
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x8002180409010C3F	1514
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x8002100409010C3F	1508
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_PL	0x8002080409010C3F	1502
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x8002000409010C3F	1492
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL	0x8000C80409010C3F	1485
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x8000080409010C3F	1338
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL	0x8000800409010C3F	1409
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x8000100409010C3F	1350
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL	0x8000880409010C3F	1419
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x8000180409010C3F	1362
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL	0x8000900409010C3F	1427
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x8000200409010C3F	1370
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL	0x8000980409010C3F	1436
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x8000280409010C3F	1378
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL	0x8000A00409010C3F	1445
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x8000300409010C3F	1387
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL	0x8000A80409010C3F	1452

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IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x8000380409010C3F	1395
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL	0x8000B00409010C3F	1460
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x8000400409010C3F	1402
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL	0x8000B80409010C3F	1468
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL	0x8000C00409010C3F	1476
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x8000000409010C3F	1327
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x8002480509010C3F	1576
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x8002500509010C3F	1594
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x8002580509010C3F	1603
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IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x8002280509010C3F	1533
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x8002300509010C3F	1542
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL	0x8002380509010C3F	1551
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x8002680509010C3F	1619
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL	0x8003180509010C3F	1650
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IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x8002780509010C3F	1636
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IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x8002180509010C3F	1514
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x8002100509010C3F	1508
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IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x8000180509010C3F	1362
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL	0x8000900509010C3F	1428
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x8000200509010C3F	1370
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL	0x8000980509010C3F	1436
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x8000280509010C3F	1378
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IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL	0x8000A80509010C3F	1452
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IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x8002480609010C3F	1577
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IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x8002100609010C3F	1508
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_PL	0x8002080609010C3F	1502
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IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL	0x8000900609010C3F	1428
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IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x8000280609010C3F	1378
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL	0x8000A00609010C3F	1445
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x8000300609010C3F	1387
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL	0x8000A80609010C3F	1452
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x8000380609010C3F	1395
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IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL	0x8000C00609010C3F	1477
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IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x8002480709010C3F	1578

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IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x8002280709010C3F	1533
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IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL	0x8002800709010C3F	1643
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x8002180709010C3F	1515
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IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_PL	0x8002080709010C3F	1503
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x8002000709010C3F	1494
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IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL	0x8000880709010C3F	1420
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Mnemonic	Address	Page
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL	0x8000A00709010C3F	1445
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x8000300709010C3F	1388
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL	0x8000A80709010C3F	1453
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x8000380709010C3F	1396
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL	0x8000B00709010C3F	1461
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x8000400709010C3F	1403
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL	0x8000B80709010C3F	1469
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL	0x8000C00709010C3F	1477
IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x8000000709010C3F	1329
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x8002480809010C3F	1579
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x8002500809010C3F	1595
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x8002580809010C3F	1604
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x8002600809010C3F	1613
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x8002400809010C3F	1564
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x8002200809010C3F	1523
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x8002280809010C3F	1534
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x8002300809010C3F	1543
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL	0x8002380809010C3F	1552
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x8002680809010C3F	1620
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL	0x8003180809010C3F	1651
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x8002700809010C3F	1627
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x8002780809010C3F	1637
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL	0x8002800809010C3F	1644
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x8002180809010C3F	1515
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x8002100809010C3F	1509
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_PL	0x8002080809010C3F	1503
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x8002000809010C3F	1494

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IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL	0x8000C80809010C3F	1486
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x8000080809010C3F	1340
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL	0x8000800809010C3F	1411
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x8000100809010C3F	1352
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL	0x8000880809010C3F	1420
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x8000180809010C3F	1363
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL	0x8000900809010C3F	1429
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x8000200809010C3F	1371
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL	0x8000980809010C3F	1437
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x8000280809010C3F	1379
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL	0x8000A00809010C3F	1446
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x8000300809010C3F	1388
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL	0x8000A80809010C3F	1453
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x8000380809010C3F	1396
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL	0x8000B00809010C3F	1461
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x8000400809010C3F	1403
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL	0x8000B80809010C3F	1469
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL	0x8000C00809010C3F	1478
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x8000000809010C3F	1329
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x8002480909010C3F	1580
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x8002500909010C3F	1595
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x8002580909010C3F	1604
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x8002600909010C3F	1613
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x8002400909010C3F	1565
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x8002200909010C3F	1524
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x8002280909010C3F	1534
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x8002300909010C3F	1543

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IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL	0x8002380909010C3F	1553
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x8002680909010C3F	1620
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL	0x8003180909010C3F	1651
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x8002700909010C3F	1628
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x8002780909010C3F	1637
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL	0x8002800909010C3F	1644
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x8002180909010C3F	1516
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x8002100909010C3F	1509
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_PL	0x8002080909010C3F	1503
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x8002000909010C3F	1494
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL	0x8000C80909010C3F	1486
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x8000080909010C3F	1341
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL	0x8000800909010C3F	1411
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x8000100909010C3F	1353
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL	0x8000880909010C3F	1421
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x8000180909010C3F	1363
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL	0x8000900909010C3F	1429
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x8000200909010C3F	1371
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL	0x8000980909010C3F	1438
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x8000280909010C3F	1380
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL	0x8000A00909010C3F	1446
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x8000300909010C3F	1388
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL	0x8000A80909010C3F	1453
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x8000380909010C3F	1396
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL	0x8000B00909010C3F	1461
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x8000400909010C3F	1404
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL	0x8000B80909010C3F	1469

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IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL	0x8000C00909010C3F	1478
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x8000000909010C3F	1329
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x8002480A09010C3F	1580
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x8002500A09010C3F	1596
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x8002580A09010C3F	1605
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x8002600A09010C3F	1613
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x8002400A09010C3F	1565
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x8002200A09010C3F	1524
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x8002280A09010C3F	1535
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x8002300A09010C3F	1543
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL	0x8002380A09010C3F	1553
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x8002680A09010C3F	1620
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL	0x8003180A09010C3F	1651
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x8002700A09010C3F	1628
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x8002780A09010C3F	1637
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL	0x8002800A09010C3F	1644
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x8002180A09010C3F	1516
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x8002100A09010C3F	1509
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_PL	0x8002080A09010C3F	1503
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x8002000A09010C3F	1495
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL	0x8000C80A09010C3F	1487
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x8000080A09010C3F	1341
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL	0x8000800A09010C3F	1412
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x8000100A09010C3F	1353
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL	0x8000880A09010C3F	1421
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x8000180A09010C3F	1364
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL	0x8000900A09010C3F	1429

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IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x8000200A09010C3F	1372
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL	0x8000980A09010C3F	1438
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x8000280A09010C3F	1380
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL	0x8000A00A09010C3F	1446
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x8000300A09010C3F	1389
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL	0x8000A80A09010C3F	1454
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x8000380A09010C3F	1397
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL	0x8000B00A09010C3F	1462
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x8000400A09010C3F	1404
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL	0x8000B80A09010C3F	1470
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL	0x8000C00A09010C3F	1478
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x8000000A09010C3F	1330
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x8002480B09010C3F	1581
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x8002500B09010C3F	1596
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x8002580B09010C3F	1605
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x8002600B09010C3F	1614
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x8002400B09010C3F	1566
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x8002200B09010C3F	1525
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x8002280B09010C3F	1535
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x8002300B09010C3F	1544
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL	0x8002380B09010C3F	1554
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x8002680B09010C3F	1620
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL	0x8003180B09010C3F	1652
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x8002700B09010C3F	1629
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x8002780B09010C3F	1638
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL	0x8002800B09010C3F	1645
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x8002180B09010C3F	1516

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IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x8002100B09010C3F	1510
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_PL	0x8002080B09010C3F	1504
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x8002000B09010C3F	1495
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL	0x8000C80B09010C3F	1487
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x8000080B09010C3F	1342
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL	0x8000800B09010C3F	1412
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x8000100B09010C3F	1354
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL	0x8000880B09010C3F	1421
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x8000180B09010C3F	1364
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL	0x8000900B09010C3F	1430
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x8000200B09010C3F	1372
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL	0x8000980B09010C3F	1439
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x8000280B09010C3F	1380
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL	0x8000A00B09010C3F	1447
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x8000300B09010C3F	1389
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL	0x8000A80B09010C3F	1454
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x8000380B09010C3F	1397
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL	0x8000B00B09010C3F	1462
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x8000400B09010C3F	1404
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL	0x8000B80B09010C3F	1470
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL	0x8000C00B09010C3F	1479
IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x8000000B09010C3F	1330
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x8002480C09010C3F	1582
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x8002500C09010C3F	1596
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x8002580C09010C3F	1606
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x8002600C09010C3F	1614
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IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x8002200C09010C3F	1525
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x8002280C09010C3F	1535
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x8002300C09010C3F	1544
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL	0x8002380C09010C3F	1554
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x8002680C09010C3F	1621
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL	0x8003180C09010C3F	1652
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x8002700C09010C3F	1629
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x8002780C09010C3F	1638
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL	0x8002800C09010C3F	1645
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x8002180C09010C3F	1516
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x8002100C09010C3F	1510
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_PL	0x8002080C09010C3F	1504
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x8002000C09010C3F	1496
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IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x8000080C09010C3F	1342
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL	0x8000800C09010C3F	1413
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x8000100C09010C3F	1354
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL	0x8000880C09010C3F	1422
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x8000180C09010C3F	1364
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL	0x8000900C09010C3F	1430
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x8000200C09010C3F	1372
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL	0x8000980C09010C3F	1439
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x8000280C09010C3F	1381
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL	0x8000A00C09010C3F	1447
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x8000300C09010C3F	1389
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL	0x8000A80C09010C3F	1454
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x8000380C09010C3F	1397

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IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL	0x8000B00C09010C3F	1462
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x8000400C09010C3F	1405
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL	0x8000B80C09010C3F	1470
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL	0x8000C00C09010C3F	1479
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x8000000C09010C3F	1331
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x8002480D09010C3F	1583
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x8002500D09010C3F	1597
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x8002580D09010C3F	1606
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x8002600D09010C3F	1614
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x8002400D09010C3F	1567
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x8002200D09010C3F	1526
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x8002280D09010C3F	1536
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x8002300D09010C3F	1544
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL	0x8002380D09010C3F	1555
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x8002680D09010C3F	1621
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL	0x8003180D09010C3F	1652
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x8002700D09010C3F	1629
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x8002780D09010C3F	1638
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL	0x8002800D09010C3F	1645
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x8002180D09010C3F	1517
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x8002100D09010C3F	1510
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_PL	0x8002080D09010C3F	1504
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x8002000D09010C3F	1496
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL	0x8000C80D09010C3F	1487
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x8000080D09010C3F	1343
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL	0x8000800D09010C3F	1413
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x8000100D09010C3F	1355

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IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL	0x8000880D09010C3F	1422
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x8000180D09010C3F	1365
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL	0x8000900D09010C3F	1431
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x8000200D09010C3F	1373
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL	0x8000980D09010C3F	1439
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x8000280D09010C3F	1381
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL	0x8000A00D09010C3F	1447
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x8000300D09010C3F	1390
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IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x8000380D09010C3F	1398
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL	0x8000B00D09010C3F	1463
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x8000400D09010C3F	1405
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL	0x8000B80D09010C3F	1471
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL	0x8000C00D09010C3F	1480
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x8000000D09010C3F	1331
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x8002480E09010C3F	1584
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x8002500E09010C3F	1597
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x8002580E09010C3F	1606
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x8002600E09010C3F	1615
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x8002400E09010C3F	1567
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x8002200E09010C3F	1526
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x8002280E09010C3F	1536
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x8002300E09010C3F	1545
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL	0x8002380E09010C3F	1555
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x8002680E09010C3F	1621
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL	0x8003180E09010C3F	1653
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x8002700E09010C3F	1630

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IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x8002780E09010C3F	1638
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL	0x8002800E09010C3F	1646
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x8002180E09010C3F	1517
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x8002100E09010C3F	1510
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_PL	0x8002080E09010C3F	1504
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x8002000E09010C3F	1497
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL	0x8000C80E09010C3F	1488
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x8000080E09010C3F	1343
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL	0x8000800E09010C3F	1413
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x8000100E09010C3F	1355
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL	0x8000880E09010C3F	1422
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x8000180E09010C3F	1365
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL	0x8000900E09010C3F	1431
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x8000200E09010C3F	1373
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL	0x8000980E09010C3F	1440
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x8000280E09010C3F	1381
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL	0x8000A00E09010C3F	1447
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x8000300E09010C3F	1390
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL	0x8000A80E09010C3F	1455
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x8000380E09010C3F	1398
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL	0x8000B00E09010C3F	1463
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x8000400E09010C3F	1405
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL	0x8000B80E09010C3F	1471
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL	0x8000C00E09010C3F	1480
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x8000000E09010C3F	1332
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x8002480F09010C3F	1585
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x8002500F09010C3F	1598

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IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x8002580F09010C3F	1607
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x8002600F09010C3F	1615
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x8002400F09010C3F	1568
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x8002200F09010C3F	1527
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x8002280F09010C3F	1537
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x8002300F09010C3F	1545
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IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x8002680F09010C3F	1621
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL	0x8003180F09010C3F	1653
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x8002700F09010C3F	1630
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x8002780F09010C3F	1639
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL	0x8002800F09010C3F	1646
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x8002180F09010C3F	1517
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x8002100F09010C3F	1511
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_PL	0x8002080F09010C3F	1505
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x8002000F09010C3F	1497
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL	0x8000C80F09010C3F	1488
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IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x8000100F09010C3F	1356
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL	0x8000880F09010C3F	1423
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x8000180F09010C3F	1365
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IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x8000200F09010C3F	1373
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL	0x8000980F09010C3F	1440
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x8000280F09010C3F	1382
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IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x8000300F09010C3F	1390
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL	0x8000A80F09010C3F	1455
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x8000380F09010C3F	1398
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL	0x8000B00F09010C3F	1463
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x8000400F09010C3F	1405
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IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL	0x8000C00F09010C3F	1480
IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x8000000F09010C3F	1332
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x8002481009010C3F	1585
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x8002501009010C3F	1598
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x8002581009010C3F	1607
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x8002601009010C3F	1615
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x8002401009010C3F	1568
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x8002201009010C3F	1527
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x8002281009010C3F	1537
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x8002301009010C3F	1545
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL	0x8002381009010C3F	1556
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x8002681009010C3F	1622
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL	0x8003181009010C3F	1653
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x8002701009010C3F	1631
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x8002781009010C3F	1639
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL	0x8002801009010C3F	1646
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x8002181009010C3F	1518
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x8002101009010C3F	1511
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_PL	0x8002081009010C3F	1505
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x8002001009010C3F	1497
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL	0x8000C81009010C3F	1488

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IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL	0x8000801009010C3F	1414
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x8000101009010C3F	1356
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL	0x8000881009010C3F	1423
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x8000181009010C3F	1366
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL	0x8000901009010C3F	1432
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x8000201009010C3F	1374
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL	0x8000981009010C3F	1440
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x8000281009010C3F	1382
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL	0x8000A01009010C3F	1448
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x8000301009010C3F	1391
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL	0x8000A81009010C3F	1456
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x8000381009010C3F	1399
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IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x8000401009010C3F	1406
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL	0x8000B81009010C3F	1472
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL	0x8000C01009010C3F	1481
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x8000001009010C3F	1333
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x8002481109010C3F	1586
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x8002501109010C3F	1598
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x8002581109010C3F	1608
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x8002601109010C3F	1615
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x8002401109010C3F	1569
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x8002201109010C3F	1527
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x8002281109010C3F	1537
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x8002301109010C3F	1546
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL	0x8002381109010C3F	1557

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IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x8002681109010C3F	1622
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL	0x8003181109010C3F	1653
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x8002701109010C3F	1631
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x8002781109010C3F	1639
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL	0x8002801109010C3F	1646
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x8002181109010C3F	1518
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x8002101109010C3F	1511
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_PL	0x8002081109010C3F	1505
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x8002001109010C3F	1498
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL	0x8000C81109010C3F	1489
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x8000081109010C3F	1345
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL	0x8000801109010C3F	1415
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x8000101109010C3F	1357
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL	0x8000881109010C3F	1423
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x8000181109010C3F	1366
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL	0x8000901109010C3F	1432
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x8000201109010C3F	1374
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL	0x8000981109010C3F	1441
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x8000281109010C3F	1383
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL	0x8000A01109010C3F	1448
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x8000301109010C3F	1391
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL	0x8000A81109010C3F	1456
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x8000381109010C3F	1399
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL	0x8000B01109010C3F	1464
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x8000401109010C3F	1406
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL	0x8000B81109010C3F	1472
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL	0x8000C01109010C3F	1481

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IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x8000001109010C3F	1333
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x8002481209010C3F	1587
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x8002501209010C3F	1599
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x8002581209010C3F	1608
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x8002601209010C3F	1616
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x8002401209010C3F	1569
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x8002201209010C3F	1528
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x8002281209010C3F	1538
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x8002301209010C3F	1546
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL	0x8002381209010C3F	1557
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x8002681209010C3F	1622
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL	0x8003181209010C3F	1654
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x8002701209010C3F	1632
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x8002781209010C3F	1640
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL	0x8002801209010C3F	1647
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x8002181209010C3F	1518
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x8002101209010C3F	1511
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_PL	0x8002081209010C3F	1505
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x8002001209010C3F	1498
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL	0x8000C81209010C3F	1489
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x8000081209010C3F	1345
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL	0x8000801209010C3F	1415
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x8000101209010C3F	1357
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL	0x8000881209010C3F	1424
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x8000181209010C3F	1366
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL	0x8000901209010C3F	1432
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x8000201209010C3F	1374

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IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL	0x8000981209010C3F	1441
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x8000281209010C3F	1383
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL	0x8000A01209010C3F	1449
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x8000301209010C3F	1391
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL	0x8000A81209010C3F	1456
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x8000381209010C3F	1399
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL	0x8000B01209010C3F	1464
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x8000401209010C3F	1406
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL	0x8000B81209010C3F	1473
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL	0x8000C01209010C3F	1481
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x8000001209010C3F	1333
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x8002481309010C3F	1588
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x8002501309010C3F	1599
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x8002581309010C3F	1608
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x8002601309010C3F	1616
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x8002401309010C3F	1570
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x8002201309010C3F	1528
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x8002281309010C3F	1538
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x8002301309010C3F	1546
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL	0x8002381309010C3F	1558
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x8002681309010C3F	1622
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL	0x8003181309010C3F	1654
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x8002701309010C3F	1632
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x8002781309010C3F	1640
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL	0x8002801309010C3F	1647
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x8002181309010C3F	1518
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x8002101309010C3F	1512

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IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_PL	0x8002081309010C3F	1506
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x8002001309010C3F	1499
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL	0x8000C81309010C3F	1489
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x8000081309010C3F	1346
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL	0x8000801309010C3F	1415
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x8000101309010C3F	1358
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL	0x8000881309010C3F	1424
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x8000181309010C3F	1367
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL	0x8000901309010C3F	1433
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x8000201309010C3F	1375
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL	0x8000981309010C3F	1442
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x8000281309010C3F	1383
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL	0x8000A01309010C3F	1449
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x8000301309010C3F	1392
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL	0x8000A81309010C3F	1457
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x8000381309010C3F	1400
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL	0x8000B01309010C3F	1465
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x8000401309010C3F	1406
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL	0x8000B81309010C3F	1473
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL	0x8000C01309010C3F	1482
IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x8000001309010C3F	1334
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x8002481409010C3F	1589
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x8002501409010C3F	1599
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x8002581409010C3F	1609
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x8002601409010C3F	1616
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x8002401409010C3F	1570
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x8002201409010C3F	1529

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IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x8002301409010C3F	1547
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL	0x8002381409010C3F	1558
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x8002681409010C3F	1623
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL	0x8003181409010C3F	1654
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x8002701409010C3F	1633
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x8002781409010C3F	1640
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL	0x8002801409010C3F	1647
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x8002181409010C3F	1519
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x8002101409010C3F	1512
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_PL	0x8002081409010C3F	1506
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x8002001409010C3F	1499
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL	0x8000C81409010C3F	1489
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x8000081409010C3F	1346
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL	0x8000801409010C3F	1416
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x8000101409010C3F	1358
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL	0x8000881409010C3F	1424
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x8000181409010C3F	1367
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL	0x8000901409010C3F	1433
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x8000201409010C3F	1375
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL	0x8000981409010C3F	1442
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x8000281409010C3F	1384
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL	0x8000A01409010C3F	1449
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x8000301409010C3F	1392
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL	0x8000A81409010C3F	1457
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x8000381409010C3F	1400
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL	0x8000B01409010C3F	1465

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IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x8000401409010C3F	1407
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL	0x8000B81409010C3F	1473
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL	0x8000C01409010C3F	1482
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x8000001409010C3F	1334
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x8002481509010C3F	1590
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x8002501509010C3F	1600
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x8002581509010C3F	1609
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x8002601509010C3F	1617
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x8002401509010C3F	1571
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x8002201509010C3F	1529
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x8002281509010C3F	1539
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x8002301509010C3F	1547
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL	0x8002381509010C3F	1559
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x8002681509010C3F	1623
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL	0x8003181509010C3F	1655
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x8002701509010C3F	1633
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x8002781509010C3F	1640
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL	0x8002801509010C3F	1648
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x8002181509010C3F	1519
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x8002101509010C3F	1512
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_PL	0x8002081509010C3F	1506
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x8002001509010C3F	1500
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL	0x8000C81509010C3F	1490
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x8000081509010C3F	1347
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL	0x8000801509010C3F	1416
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IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x8000181509010C3F	1367
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL	0x8000901509010C3F	1433
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x8000201509010C3F	1375
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL	0x8000981509010C3F	1442
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x8000281509010C3F	1384
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL	0x8000A01509010C3F	1449
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x8000301509010C3F	1392
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL	0x8000A81509010C3F	1457
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x8000381509010C3F	1400
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL	0x8000B01509010C3F	1465
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x8000401509010C3F	1407
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL	0x8000B81509010C3F	1474
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL	0x8000C01509010C3F	1483
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x8000001509010C3F	1335
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x8002481609010C3F	1590
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x8002501609010C3F	1600
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL	0x8002581609010C3F	1610
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL	0x8002601609010C3F	1617
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x8002401609010C3F	1571
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x8002201609010C3F	1530
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x8002281609010C3F	1539
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x8002301609010C3F	1547
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL	0x8002381609010C3F	1559
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x8002681609010C3F	1623
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL	0x8003181609010C3F	1655
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IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x8002781609010C3F	1641

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IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x8002181609010C3F	1519
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_MASK_PL	0x8002101609010C3F	1512
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_PL	0x8002081609010C3F	1506
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x8002001609010C3F	1500
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IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x8000081609010C3F	1347
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL	0x8000801609010C3F	1417
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x8000101609010C3F	1359
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL	0x8000881609010C3F	1425
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x8000181609010C3F	1368
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL	0x8000901609010C3F	1434
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x8000201609010C3F	1376
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL	0x8000981609010C3F	1443
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x8000281609010C3F	1384
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL	0x8000A01609010C3F	1450
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x8000301609010C3F	1393
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL	0x8000A81609010C3F	1458
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x8000381609010C3F	1401
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL	0x8000B01609010C3F	1466
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x8000401609010C3F	1407
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IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x8000001609010C3F	1335
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL	0x8002481709010C3F	1591
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL	0x8002501709010C3F	1600
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IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL	0x8002401709010C3F	1572
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL	0x8002201709010C3F	1530
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL	0x8002281709010C3F	1540
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL	0x8002301709010C3F	1548
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL	0x8002381709010C3F	1560
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL	0x8002681709010C3F	1623
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL	0x8003181709010C3F	1655
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL	0x8002701709010C3F	1634
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL	0x8002781709010C3F	1641
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL	0x8002801709010C3F	1648
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL	0x8002181709010C3F	1520
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IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_PL	0x8002081709010C3F	1507
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x8002001709010C3F	1500
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL	0x8000C81709010C3F	1490
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL	0x8000081709010C3F	1348
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL	0x8000801709010C3F	1417
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL	0x8000101709010C3F	1360
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL	0x8000881709010C3F	1426
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL	0x8000181709010C3F	1368
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL	0x8000901709010C3F	1434
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL	0x8000201709010C3F	1376
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL	0x8000981709010C3F	1443
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL	0x8000281709010C3F	1385
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL	0x8000A01709010C3F	1450
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL	0x8000301709010C3F	1393

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IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL	0x8000A81709010C3F	1458
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL	0x8000381709010C3F	1401
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL	0x8000B01709010C3F	1466
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL	0x8000401709010C3F	1408
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL	0x8000B81709010C3F	1474
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL	0x8000C01709010C3F	1483
IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL	0x8000001709010C3F	1336
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IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#0.RX_WORK_REGS.RX_WORK_STAT1_EO_PL	0x8003880009010C3F	1691
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IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#1.RX_WORK_REGS.RX_WORK_STAT2_EO_PL	0x8003900109010C3F	1702
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IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#12.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL	0x8003800C09010C3F	1686
IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#12.RX_WORK_REGS.RX_WORK_CNTL1_O_PL	0x8003A80C09010C3F	1728
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IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#13.RX_WORK_REGS.RX_WORK_STAT2_EO_PL	0x8003900D09010C3F	1707
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IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#3.RX_WORK_REGS.RX_WORK_STAT2_EO_PL	0x8003900309010C3F	1703
IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#3.RX_WORK_REGS.RX_WORK_STAT3_EO_PL	0x8003980309010C3F	1713
IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#3.RX_WORK_REGS.RX_WORK_STAT4_O_PL	0x8003A00309010C3F	1719
IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#4.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL	0x8003800409010C3F	1682
IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#4.RX_WORK_REGS.RX_WORK_CNTL1_O_PL	0x8003A80409010C3F	1726
IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#4.RX_WORK_REGS.RX_WORK_STAT1_EO_PL	0x8003880409010C3F	1693
IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#4.RX_WORK_REGS.RX_WORK_STAT2_EO_PL	0x8003900409010C3F	1703
IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#4.RX_WORK_REGS.RX_WORK_STAT3_EO_PL	0x8003980409010C3F	1713
IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#4.RX_WORK_REGS.RX_WORK_STAT4_O_PL	0x8003A00409010C3F	1720
IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#5.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL	0x8003800509010C3F	1683
IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#5.RX_WORK_REGS.RX_WORK_CNTL1_O_PL	0x8003A80509010C3F	1727
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IOO0.IOO_CPLT.TX0.TXPACKS#1.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_MODE2_PL	0x80040C0709010C3F	1753
IOO0.IOO_CPLT.TX0.TXPACKS#1.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_STAT1_PL	0x80041C0709010C3F	1772
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IOO0.IOO_CPLT.TX0.TXPACKS#2.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL	0x8004340809010C3F	1794
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IOO0.IOO_CPLT.TX0.TXPACKS#2.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_PL	0x8004240809010C3F	1781
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IOO0.IOO_CPLT.TX0.TXPACKS#2.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_STAT1_PL	0x80041C0809010C3F	1772
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IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_CNTL2_O_PL	0x80044C1509010C3F	1804
IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_CNTL3_EO_PL	0x8004541509010C3F	1810
IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL	0x8004341509010C3F	1798
IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_MASK_PL	0x80042C1509010C3F	1791

Mnemonic	Address	Page
IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_PL	0x8004241509010C3F	1785
IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_MODE1_PL	0x8004041509010C3F	1747
IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_MODE2_PL	0x80040C1509010C3F	1761
IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_STAT1_PL	0x80041C1509010C3F	1778
IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_CNTL1G_PL	0x8004141609010C3F	1768
IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_CNTL2_O_PL	0x80044C1609010C3F	1804
IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_CNTL3_EO_PL	0x8004541609010C3F	1810
IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL	0x8004341609010C3F	1798
IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_MASK_PL	0x80042C1609010C3F	1791
IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_PL	0x8004241609010C3F	1785
IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_MODE1_PL	0x8004041609010C3F	1747
IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_MODE2_PL	0x80040C1609010C3F	1761
IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_STAT1_PL	0x80041C1609010C3F	1778
IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_CNTL1G_PL	0x8004141709010C3F	1769
IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_CNTL2_O_PL	0x80044C1709010C3F	1804
IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_CNTL3_EO_PL	0x8004541709010C3F	1810
IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL	0x8004341709010C3F	1798
IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_MASK_PL	0x80042C1709010C3F	1792
IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_PL	0x8004241709010C3F	1785
IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_MODE1_PL	0x8004041709010C3F	1748
IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_MODE2_PL	0x80040C1709010C3F	1762
IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_STAT1_PL	0x80041C1709010C3F	1779

The POWER9 processor registers are listed in the following tables.

Register Name	**Receive Data DAC Spare Mode Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	8000000009010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	8000000109010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	8000000209010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	8000000309010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	8000000409010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Data DAC Spare Mode Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	8000000509010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Data DAC Spare Mode Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	8000000609010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Data DAC Spare Mode Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	8000000709010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Data DAC Spare Mode Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	8000000809010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Data DAC Spare Mode Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	8000000909010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	8000000A09010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	8000000B09010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	8000000C09010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	8000000D09010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	8000000E09010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	8000000F09010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	8000001009010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	8000001109010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	8000001209010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	8000001309010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	8000001409010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	8000001509010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	8000001609010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data DAC Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DATA_DAC_SPARE_MODE_PL
Address	8000001709010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_DAC_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_DAC_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_DAC_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_DAC_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_DAC_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_DAC_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_DAC_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_DAC_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	8000080009010C3F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	RX_B_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.

Register Name	**Receive DAC Control 1 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	8000080109010C3F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RWX	RX_B_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.

Register Name	**Receive DAC Control 1 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	8000080209010C3F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.

Bits	SCOM	Field Mnemonic: Description
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RWX	RX_B_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.

Register Name	**Receive DAC Control 1 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	8000080309010C3F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RWX	RX_B_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.

Register Name	**Receive DAC Control 1 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	8000080409010C3F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.

Bits	SCOM	Field Mnemonic: Description
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RWX	RX_B_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	8000080509010C3F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RWX	RX_B_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	8000080609010C3F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_A_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RWX	RX_B_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	8000080709010C3F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RWX	RX_B_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	8000080809010C3F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RWX	RX_B_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	8000080909010C3F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RWX	RX_B_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	8000080A09010C3F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RWX	RX_B_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	8000080B09010C3F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RWX	RX_B_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	8000080C09010C3F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RWX	RX_B_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	8000080D09010C3F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RWX	RX_B_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	8000080E09010C3F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RWX	RX_B_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	8000080F09010C3F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RWX	RX_B_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	8000081009010C3F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RWX	RX_B_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	8000081109010C3F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RWX	RX_B_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	8000081209010C3F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RWX	RX_B_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	8000081309010C3F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RWX	RX_B_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	8000081409010C3F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RWX	RX_B_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	8000081509010C3F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RWX	RX_B_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	8000081609010C3F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RWX	RX_B_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.

Register Name	Receive DAC Control 1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_EO_PL
Address	8000081709010C3F (SCOM)
Description	This register contains the first set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.
54	RWX	RX_LANE_ANA_PDWN: This bit controls the lane power down of analog and custom circuits.
55:57	RWX	RX_PRBS_TEST_DATA: This field contains PRBS test data.
58:63	RWX	RX_B_BANK_CONTROLS: This field controls the power-down pins. Bit 0 = CML2CMOS. Bit 1 = CTLE. Bit 2 = DAC. Bit 3 = Deserializer. Bit 4 = Integrator. Bit 5 = Phase rotator.

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	8000100009010C3F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	**Receive DAC Control 2 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	8000100109010C3F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	**Receive DAC Control 2 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	8000100209010C3F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	8000100309010C3F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	8000100409010C3F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	8000100509010C3F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	8000100609010C3F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	8000100709010C3F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	8000100809010C3F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	8000100909010C3F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	8000100A09010C3F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	8000100B09010C3F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	8000100C09010C3F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	8000100D09010C3F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	8000100E09010C3F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	8000100F09010C3F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	8000101009010C3F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	8000101109010C3F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	8000101209010C3F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	8000101309010C3F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	8000101409010C3F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	**Receive DAC Control 2 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	8000101509010C3F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	**Receive DAC Control 2 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	8000101609010C3F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_EO_PL
Address	8000101709010C3F (SCOM)
Description	This register contains the second set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff. Bit 5 = When set, this bit disables all the H-DACs. CPG.
54:56	RWX	RX_CM_CNTL: Bit 0 = This bit enables integrator common mode cal, which is used in conjunction with integrator cal enable. Bit 1 = This is the polarity bit. Bit 2 = When 1, this bit enables common mode even. When 0, this bit enables common mode odd. CPG.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	8000180009010C3F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.

Bits	SCOM	Field Mnemonic: Description
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	8000180109010C3F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	8000180209010C3F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	8000180309010C3F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	8000180409010C3F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	8000180509010C3F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	8000180609010C3F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	8000180709010C3F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	8000180809010C3F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	8000180909010C3F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	8000180A09010C3F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	8000180B09010C3F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	8000180C09010C3F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	**Receive DAC Control 3 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	8000180D09010C3F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	**Receive DAC Control 3 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	8000180E09010C3F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	**Receive DAC Control 3 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	8000180F09010C3F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	8000181009010C3F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	8000181109010C3F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	8000181209010C3F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	8000181309010C3F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	8000181409010C3F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	8000181509010C3F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	8000181609010C3F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_EO_PL
Address	8000181709010C3F (SCOM)
Description	This register contains the third set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	8000200009010C3F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	8000200109010C3F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	8000200209010C3F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	8000200309010C3F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	8000200409010C3F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	8000200509010C3F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	8000200609010C3F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	8000200709010C3F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	8000200809010C3F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	8000200909010C3F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	8000200A09010C3F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	8000200B09010C3F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	8000200C09010C3F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	8000200D09010C3F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	8000200E09010C3F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	8000200F09010C3F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	8000201009010C3F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	8000201109010C3F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	8000201209010C3F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	8000201309010C3F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	8000201409010C3F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	8000201509010C3F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	8000201609010C3F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_EO_PL
Address	8000201709010C3F (SCOM)
Description	This register contains the fourth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch.
55	RO	constant = 0b0
56:62	RWX	RX_A_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch.
63	RO	constant = 0b0

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	8000280009010C3F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	8000280109010C3F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	8000280209010C3F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	8000280309010C3F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.

Bits	SCOM	Field Mnemonic: Description
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	8000280409010C3F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	8000280509010C3F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	8000280609010C3F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	**Receive DAC Control 5 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	8000280709010C3F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	**Receive DAC Control 5 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	8000280809010C3F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	8000280909010C3F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	8000280A09010C3F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	8000280B09010C3F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.

Bits	SCOM	Field Mnemonic: Description
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	8000280C09010C3F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	8000280D09010C3F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	8000280E09010C3F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	8000280F09010C3F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	8000281009010C3F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	8000281109010C3F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	8000281209010C3F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	8000281309010C3F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.

Bits	SCOM	Field Mnemonic: Description
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	8000281409010C3F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	8000281509010C3F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	8000281609010C3F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_EO_PL
Address	8000281709010C3F (SCOM)
Description	This register contains the fifth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_A_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_A_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	8000300009010C3F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_CTLE_COARSE: This is the CTLE coarse peak value. Only 4 bits are currently used.
52	RO	constant = 0b0
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	8000300109010C3F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_CTLE_COARSE: This is the CTLE coarse peak value. Only 4 bits are currently used.
52	RO	constant = 0b0
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	8000300209010C3F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_CTLE_COARSE: This is the CTLE coarse peak value. Only 4 bits are currently used.
52	RO	constant = 0b0
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	8000300309010C3F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_CTLE_COARSE: This is the CTLE coarse peak value. Only 4 bits are currently used.
52	RO	constant = 0b0
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	8000300409010C3F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_CTLE_COARSE: This is the CTLE coarse peak value. Only 4 bits are currently used.
52	RO	constant = 0b0
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	8000300509010C3F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_CTLE_COARSE: This is the CTLE coarse peak value. Only 4 bits are currently used.
52	RO	constant = 0b0
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	8000300609010C3F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_CTLE_COARSE: This is the CTLE coarse peak value. Only 4 bits are currently used.
52	RO	constant = 0b0
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	8000300709010C3F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_CTLE_COARSE: This is the CTLE coarse peak value. Only 4 bits are currently used.
52	RO	constant = 0b0
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	8000300809010C3F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_CTLE_COARSE: This is the CTLE coarse peak value. Only 4 bits are currently used.
52	RO	constant = 0b0
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	8000300909010C3F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_CTLE_COARSE: This is the CTLE coarse peak value. Only 4 bits are currently used.
52	RO	constant = 0b0
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	8000300A09010C3F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_CTLE_COARSE: This is the CTLE coarse peak value. Only 4 bits are currently used.
52	RO	constant = 0b0
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	8000300B09010C3F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_CTLE_COARSE: This is the CTLE coarse peak value. Only 4 bits are currently used.
52	RO	constant = 0b0
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	8000300C09010C3F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_CTLE_COARSE: This is the CTLE coarse peak value. Only 4 bits are currently used.
52	RO	constant = 0b0
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	8000300D09010C3F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_CTLE_COARSE: This is the CTLE coarse peak value. Only 4 bits are currently used.
52	RO	constant = 0b0
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	8000300E09010C3F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_CTLE_COARSE: This is the CTLE coarse peak value. Only 4 bits are currently used.
52	RO	constant = 0b0
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	8000300F09010C3F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_CTLE_COARSE: This is the CTLE coarse peak value. Only 4 bits are currently used.
52	RO	constant = 0b0
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	8000301009010C3F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_CTLE_COARSE: This is the CTLE coarse peak value. Only 4 bits are currently used.
52	RO	constant = 0b0
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	8000301109010C3F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_CTLE_COARSE: This is the CTLE coarse peak value. Only 4 bits are currently used.
52	RO	constant = 0b0
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	8000301209010C3F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_CTLE_COARSE: This is the CTLE coarse peak value. Only 4 bits are currently used.
52	RO	constant = 0b0
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	8000301309010C3F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_CTLE_COARSE: This is the CTLE coarse peak value. Only 4 bits are currently used.
52	RO	constant = 0b0
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	8000301409010C3F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_CTLE_COARSE: This is the CTLE coarse peak value. Only 4 bits are currently used.
52	RO	constant = 0b0
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	8000301509010C3F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_CTLE_COARSE: This is the CTLE coarse peak value. Only 4 bits are currently used.
52	RO	constant = 0b0
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	8000301609010C3F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_CTLE_COARSE: This is the CTLE coarse peak value. Only 4 bits are currently used.
52	RO	constant = 0b0
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 6 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_EO_PL
Address	8000301709010C3F (SCOM)
Description	This register contains the sixth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_A_CTLE_COARSE: This is the CTLE coarse peak value. Only 4 bits are currently used.
52	RO	constant = 0b0
53:56	RWX	RX_A_CTLE_GAIN: This is the CTLE gain setting.
57:63	RO	constant = 0b0000000

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	8000380009010C3F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	8000380109010C3F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	8000380209010C3F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	8000380309010C3F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	8000380409010C3F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	8000380509010C3F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	8000380609010C3F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	**Receive DAC Control 7 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	8000380709010C3F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	**Receive DAC Control 7 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	8000380809010C3F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	**Receive DAC Control 7 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	8000380909010C3F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	8000380A09010C3F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	8000380B09010C3F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	8000380C09010C3F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	8000380D09010C3F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	8000380E09010C3F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	8000380F09010C3F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	8000381009010C3F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	8000381109010C3F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	8000381209010C3F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	8000381309010C3F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	8000381409010C3F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	8000381509010C3F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	**Receive DAC Control 7 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	8000381609010C3F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	**Receive DAC Control 7 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_EO_PL
Address	8000381709010C3F (SCOM)
Description	This register contains the seventh set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_A_H1E_VAL: This field contains the DFE H1 value for even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_A_H1O_VAL: This field contains the DFE H1 value for odd samplers.
63	RO	constant = 0b0

Register Name	**Receive DAC Control 8 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	8000400009010C3F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	8000400109010C3F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	8000400209010C3F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	8000400309010C3F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	8000400409010C3F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.

Bits	SCOM	Field Mnemonic: Description
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	8000400509010C3F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	8000400609010C3F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	8000400709010C3F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	8000400809010C3F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	8000400909010C3F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	8000400A09010C3F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	8000400B09010C3F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	**Receive DAC Control 8 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	8000400C09010C3F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	**Receive DAC Control 8 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	8000400D09010C3F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	**Receive DAC Control 8 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	8000400E09010C3F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	**Receive DAC Control 8 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	8000400F09010C3F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.

Bits	SCOM	Field Mnemonic: Description
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	8000401009010C3F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	8000401109010C3F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	8000401209010C3F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	8000401309010C3F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	8000401409010C3F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	8000401509010C3F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	8000401609010C3F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 8 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_EO_PL
Address	8000401709010C3F (SCOM)
Description	This register contains the eighth set of EO DAC controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP_VAL: This field contains the receive AmpDAC value stored as sign magnitude.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL
Address	8000800009010C3F (SCOM)
Description	This register contains the first set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_B_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL
Address	8000800109010C3F (SCOM)
Description	This register contains the first set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_B_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL
Address	8000800209010C3F (SCOM)
Description	This register contains the first set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_B_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL
Address	8000800309010C3F (SCOM)
Description	This register contains the first set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_B_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL
Address	8000800409010C3F (SCOM)
Description	This register contains the first set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:52	RWX	RX_B_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff.
53:63	RO	constant = 0b00000000000

Register Name	**Receive DAC Control 1 O Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL
Address	8000800509010C3F (SCOM)
Description	This register contains the first set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_B_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff.
53:63	RO	constant = 0b00000000000

Register Name	**Receive DAC Control 1 O Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL
Address	8000800609010C3F (SCOM)
Description	This register contains the first set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_B_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL
Address	8000800709010C3F (SCOM)
Description	This register contains the first set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_B_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL
Address	8000800809010C3F (SCOM)
Description	This register contains the first set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_B_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL
Address	8000800909010C3F (SCOM)
Description	This register contains the first set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:52	RWX	RX_B_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL
Address	8000800A09010C3F (SCOM)
Description	This register contains the first set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_B_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL
Address	8000800B09010C3F (SCOM)
Description	This register contains the first set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_B_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL
Address	8000800C09010C3F (SCOM)
Description	This register contains the first set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_B_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL
Address	8000800D09010C3F (SCOM)
Description	This register contains the first set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_B_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL
Address	8000800E09010C3F (SCOM)
Description	This register contains the first set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:52	RWX	RX_B_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL
Address	8000800F09010C3F (SCOM)
Description	This register contains the first set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_B_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL
Address	8000801009010C3F (SCOM)
Description	This register contains the first set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_B_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL
Address	8000801109010C3F (SCOM)
Description	This register contains the first set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_B_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL
Address	8000801209010C3F (SCOM)
Description	This register contains the first set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_B_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL
Address	8000801309010C3F (SCOM)
Description	This register contains the first set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:52	RWX	RX_B_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL
Address	8000801409010C3F (SCOM)
Description	This register contains the first set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_B_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL
Address	8000801509010C3F (SCOM)
Description	This register contains the first set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_B_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL
Address	8000801609010C3F (SCOM)
Description	This register contains the first set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_B_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL1_O_PL
Address	8000801709010C3F (SCOM)
Description	This register contains the first set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	RX_B_CONTROLS: Bit 0 = DFE H1 speculation mux select override enables speculation. Bit 1 = DFE H1 speculation mux select override. Bit 2 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 3 = This bit enables the amp DAC for measurements in this bank. Bit 4 = This bit enables the fence for initloff.
53:63	RO	constant = 0b00000000000

Register Name	Receive DAC Control 2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL
Address	8000880009010C3F (SCOM)
Description	This register contains the second set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch. The step size is Vio/256.

Bits	SCOM	Field Mnemonic: Description
63	RO	constant = 0b0

Register Name	Receive DAC Control 2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL
Address	8000880109010C3F (SCOM)
Description	This register contains the second set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL
Address	8000880209010C3F (SCOM)
Description	This register contains the second set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL
Address	8000880309010C3F (SCOM)
Description	This register contains the second set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.

Bits	SCOM	Field Mnemonic: Description
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL
Address	8000880409010C3F (SCOM)
Description	This register contains the second set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL
Address	8000880509010C3F (SCOM)
Description	This register contains the second set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL
Address	8000880609010C3F (SCOM)
Description	This register contains the second set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL
Address	8000880709010C3F (SCOM)
Description	This register contains the second set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL
Address	8000880809010C3F (SCOM)
Description	This register contains the second set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL
Address	8000880909010C3F (SCOM)
Description	This register contains the second set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL
Address	8000880A09010C3F (SCOM)
Description	This register contains the second set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL
Address	8000880B09010C3F (SCOM)
Description	This register contains the second set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL
Address	8000880C09010C3F (SCOM)
Description	This register contains the second set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL
Address	8000880D09010C3F (SCOM)
Description	This register contains the second set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL
Address	8000880E09010C3F (SCOM)
Description	This register contains the second set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch. The step size is Vio/256.

Bits	SCOM	Field Mnemonic: Description
63	RO	constant = 0b0

Register Name	Receive DAC Control 2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL
Address	8000880F09010C3F (SCOM)
Description	This register contains the second set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL
Address	8000881009010C3F (SCOM)
Description	This register contains the second set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL
Address	8000881109010C3F (SCOM)
Description	This register contains the second set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.

Bits	SCOM	Field Mnemonic: Description
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL
Address	8000881209010C3F (SCOM)
Description	This register contains the second set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL
Address	8000881309010C3F (SCOM)
Description	This register contains the second set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL
Address	8000881409010C3F (SCOM)
Description	This register contains the second set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL
Address	8000881509010C3F (SCOM)
Description	This register contains the second set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL
Address	8000881609010C3F (SCOM)
Description	This register contains the second set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL2_O_PL
Address	8000881709010C3F (SCOM)
Description	This register contains the second set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_E0: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_E1: This is the vertical offset of the even high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL
Address	8000900009010C3F (SCOM)
Description	This register contains the third set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL
Address	8000900109010C3F (SCOM)
Description	This register contains the third set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL
Address	8000900209010C3F (SCOM)
Description	This register contains the third set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL
Address	8000900309010C3F (SCOM)
Description	This register contains the third set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL
Address	8000900409010C3F (SCOM)
Description	This register contains the third set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch. The step size is Vio/256.

Bits	SCOM	Field Mnemonic: Description
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL
Address	8000900509010C3F (SCOM)
Description	This register contains the third set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL
Address	8000900609010C3F (SCOM)
Description	This register contains the third set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL
Address	8000900709010C3F (SCOM)
Description	This register contains the third set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.

Bits	SCOM	Field Mnemonic: Description
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL
Address	8000900809010C3F (SCOM)
Description	This register contains the third set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL
Address	8000900909010C3F (SCOM)
Description	This register contains the third set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL
Address	8000900A09010C3F (SCOM)
Description	This register contains the third set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL
Address	8000900B09010C3F (SCOM)
Description	This register contains the third set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL
Address	8000900C09010C3F (SCOM)
Description	This register contains the third set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL
Address	8000900D09010C3F (SCOM)
Description	This register contains the third set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL
Address	8000900E09010C3F (SCOM)
Description	This register contains the third set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL
Address	8000900F09010C3F (SCOM)
Description	This register contains the third set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL
Address	8000901009010C3F (SCOM)
Description	This register contains the third set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL
Address	8000901109010C3F (SCOM)
Description	This register contains the third set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL
Address	8000901209010C3F (SCOM)
Description	This register contains the third set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch. The step size is Vio/256.

Bits	SCOM	Field Mnemonic: Description
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL
Address	8000901309010C3F (SCOM)
Description	This register contains the third set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL
Address	8000901409010C3F (SCOM)
Description	This register contains the third set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL
Address	8000901509010C3F (SCOM)
Description	This register contains the third set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.

Bits	SCOM	Field Mnemonic: Description
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL
Address	8000901609010C3F (SCOM)
Description	This register contains the third set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 3 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL3_O_PL
Address	8000901709010C3F (SCOM)
Description	This register contains the third set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_OFFSET_O0: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_B_OFFSET_O1: This is the vertical offset of the odd high-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 4 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL
Address	8000980009010C3F (SCOM)
Description	This register contains the fourth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_B_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_B_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	**Receive DAC Control 4 O Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL
Address	8000980109010C3F (SCOM)
Description	This register contains the fourth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_B_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_B_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	**Receive DAC Control 4 O Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL
Address	8000980209010C3F (SCOM)
Description	This register contains the fourth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_B_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_B_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 4 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL
Address	8000980309010C3F (SCOM)
Description	This register contains the fourth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_B_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_B_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 4 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL
Address	8000980409010C3F (SCOM)
Description	This register contains the fourth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_B_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_B_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 4 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL
Address	8000980509010C3F (SCOM)
Description	This register contains the fourth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_B_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.

Bits	SCOM	Field Mnemonic: Description
57:61	RWX	RX_B_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 4 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL
Address	8000980609010C3F (SCOM)
Description	This register contains the fourth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_B_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_B_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 4 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL
Address	8000980709010C3F (SCOM)
Description	This register contains the fourth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_B_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_B_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 4 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL
Address	8000980809010C3F (SCOM)
Description	This register contains the fourth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_B_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_B_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 4 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL
Address	8000980909010C3F (SCOM)
Description	This register contains the fourth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_B_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_B_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 4 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL
Address	8000980A09010C3F (SCOM)
Description	This register contains the fourth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_B_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_B_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 4 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL
Address	8000980B09010C3F (SCOM)
Description	This register contains the fourth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_B_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_B_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 4 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL
Address	8000980C09010C3F (SCOM)
Description	This register contains the fourth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_B_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_B_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 4 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL
Address	8000980D09010C3F (SCOM)
Description	This register contains the fourth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_B_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.

Bits	SCOM	Field Mnemonic: Description
57:61	RWX	RX_B_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 4 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL
Address	8000980E09010C3F (SCOM)
Description	This register contains the fourth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_B_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_B_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 4 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL
Address	8000980F09010C3F (SCOM)
Description	This register contains the fourth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_B_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_B_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 4 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL
Address	8000981009010C3F (SCOM)
Description	This register contains the fourth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_B_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_B_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 4 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL
Address	8000981109010C3F (SCOM)
Description	This register contains the fourth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_B_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_B_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 4 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL
Address	8000981209010C3F (SCOM)
Description	This register contains the fourth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_B_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_B_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 4 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL
Address	8000981309010C3F (SCOM)
Description	This register contains the fourth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_B_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_B_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 4 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL
Address	8000981409010C3F (SCOM)
Description	This register contains the fourth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_B_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_B_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 4 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL
Address	8000981509010C3F (SCOM)
Description	This register contains the fourth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_B_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.

Bits	SCOM	Field Mnemonic: Description
57:61	RWX	RX_B_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 4 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL
Address	8000981609010C3F (SCOM)
Description	This register contains the fourth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_B_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_B_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 4 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL4_O_PL
Address	8000981709010C3F (SCOM)
Description	This register contains the fourth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_B_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_B_ODD_INTEG_FINE_GAIN: This is the odd integrator fine-gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 5 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL
Address	8000A00009010C3F (SCOM)
Description	This register contains the fifth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_B_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	**Receive DAC Control 5 O Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL
Address	8000A00109010C3F (SCOM)
Description	This register contains the fifth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_B_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	**Receive DAC Control 5 O Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL
Address	8000A00209010C3F (SCOM)
Description	This register contains the fifth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_B_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	**Receive DAC Control 5 O Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL
Address	8000A00309010C3F (SCOM)
Description	This register contains the fifth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_B_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 5 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL
Address	8000A00409010C3F (SCOM)
Description	This register contains the fifth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_B_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 5 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL
Address	8000A00509010C3F (SCOM)
Description	This register contains the fifth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_B_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 5 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL
Address	8000A00609010C3F (SCOM)
Description	This register contains the fifth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_B_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 5 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL
Address	8000A00709010C3F (SCOM)
Description	This register contains the fifth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_B_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	**Receive DAC Control 5 O Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL
Address	8000A00809010C3F (SCOM)
Description	This register contains the fifth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_B_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	**Receive DAC Control 5 O Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL
Address	8000A00909010C3F (SCOM)
Description	This register contains the fifth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_B_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	**Receive DAC Control 5 O Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL
Address	8000A00A09010C3F (SCOM)
Description	This register contains the fifth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_B_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 5 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL
Address	8000A00B09010C3F (SCOM)
Description	This register contains the fifth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_B_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 5 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL
Address	8000A00C09010C3F (SCOM)
Description	This register contains the fifth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_B_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 5 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL
Address	8000A00D09010C3F (SCOM)
Description	This register contains the fifth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_B_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 5 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL
Address	8000A00E09010C3F (SCOM)
Description	This register contains the fifth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_B_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 5 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL
Address	8000A00F09010C3F (SCOM)
Description	This register contains the fifth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_B_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 5 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL
Address	8000A01009010C3F (SCOM)
Description	This register contains the fifth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_B_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 5 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL
Address	8000A01109010C3F (SCOM)
Description	This register contains the fifth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_B_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 5 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL
Address	8000A01209010C3F (SCOM)
Description	This register contains the fifth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_B_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 5 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL
Address	8000A01309010C3F (SCOM)
Description	This register contains the fifth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_B_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 5 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL
Address	8000A01409010C3F (SCOM)
Description	This register contains the fifth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_B_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 5 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL
Address	8000A01509010C3F (SCOM)
Description	This register contains the fifth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_B_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 5 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL
Address	8000A01609010C3F (SCOM)
Description	This register contains the fifth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_B_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 5 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL5_O_PL
Address	8000A01709010C3F (SCOM)
Description	This register contains the fifth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_B_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_B_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 6 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL
Address	8000A80009010C3F (SCOM)
Description	This register contains the sixth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_H1E_VAL: This field contains the DFE H1 value for the even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_B_H1O_VAL: This field contains the DFE H1 value for the odd samplers.

Bits	SCOM	Field Mnemonic: Description
63	RO	constant = 0b0

Register Name	Receive DAC Control 6 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL
Address	8000A80109010C3F (SCOM)
Description	This register contains the sixth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_H1E_VAL: This field contains the DFE H1 value for the even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_B_H1O_VAL: This field contains the DFE H1 value for the odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 6 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL
Address	8000A80209010C3F (SCOM)
Description	This register contains the sixth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_H1E_VAL: This field contains the DFE H1 value for the even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_B_H1O_VAL: This field contains the DFE H1 value for the odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 6 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL
Address	8000A80309010C3F (SCOM)
Description	This register contains the sixth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_H1E_VAL: This field contains the DFE H1 value for the even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_B_H1O_VAL: This field contains the DFE H1 value for the odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 6 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL
Address	8000A80409010C3F (SCOM)
Description	This register contains the sixth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_H1E_VAL: This field contains the DFE H1 value for the even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_B_H1O_VAL: This field contains the DFE H1 value for the odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 6 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL
Address	8000A80509010C3F (SCOM)
Description	This register contains the sixth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_H1E_VAL: This field contains the DFE H1 value for the even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_B_H1O_VAL: This field contains the DFE H1 value for the odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 6 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL
Address	8000A80609010C3F (SCOM)
Description	This register contains the sixth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_H1E_VAL: This field contains the DFE H1 value for the even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_B_H1O_VAL: This field contains the DFE H1 value for the odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 6 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL
Address	8000A80709010C3F (SCOM)
Description	This register contains the sixth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_H1E_VAL: This field contains the DFE H1 value for the even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_B_H1O_VAL: This field contains the DFE H1 value for the odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 6 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL
Address	8000A80809010C3F (SCOM)
Description	This register contains the sixth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_H1E_VAL: This field contains the DFE H1 value for the even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_B_H1O_VAL: This field contains the DFE H1 value for the odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 6 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL
Address	8000A80909010C3F (SCOM)
Description	This register contains the sixth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_H1E_VAL: This field contains the DFE H1 value for the even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_B_H1O_VAL: This field contains the DFE H1 value for the odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 6 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL
Address	8000A80A09010C3F (SCOM)
Description	This register contains the sixth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_H1E_VAL: This field contains the DFE H1 value for the even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_B_H1O_VAL: This field contains the DFE H1 value for the odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 6 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL
Address	8000A80B09010C3F (SCOM)
Description	This register contains the sixth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_H1E_VAL: This field contains the DFE H1 value for the even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_B_H1O_VAL: This field contains the DFE H1 value for the odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 6 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL
Address	8000A80C09010C3F (SCOM)
Description	This register contains the sixth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_H1E_VAL: This field contains the DFE H1 value for the even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_B_H1O_VAL: This field contains the DFE H1 value for the odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 6 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL
Address	8000A80D09010C3F (SCOM)
Description	This register contains the sixth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_H1E_VAL: This field contains the DFE H1 value for the even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_B_H1O_VAL: This field contains the DFE H1 value for the odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 6 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL
Address	8000A80E09010C3F (SCOM)
Description	This register contains the sixth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_H1E_VAL: This field contains the DFE H1 value for the even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_B_H1O_VAL: This field contains the DFE H1 value for the odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 6 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL
Address	8000A80F09010C3F (SCOM)
Description	This register contains the sixth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_H1E_VAL: This field contains the DFE H1 value for the even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_B_H1O_VAL: This field contains the DFE H1 value for the odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 6 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL
Address	8000A81009010C3F (SCOM)
Description	This register contains the sixth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_H1E_VAL: This field contains the DFE H1 value for the even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_B_H1O_VAL: This field contains the DFE H1 value for the odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 6 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL
Address	8000A81109010C3F (SCOM)
Description	This register contains the sixth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_H1E_VAL: This field contains the DFE H1 value for the even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_B_H1O_VAL: This field contains the DFE H1 value for the odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 6 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL
Address	8000A81209010C3F (SCOM)
Description	This register contains the sixth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_H1E_VAL: This field contains the DFE H1 value for the even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_B_H1O_VAL: This field contains the DFE H1 value for the odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 6 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL
Address	8000A81309010C3F (SCOM)
Description	This register contains the sixth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_H1E_VAL: This field contains the DFE H1 value for the even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_B_H1O_VAL: This field contains the DFE H1 value for the odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 6 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL
Address	8000A81409010C3F (SCOM)
Description	This register contains the sixth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_H1E_VAL: This field contains the DFE H1 value for the even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_B_H1O_VAL: This field contains the DFE H1 value for the odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 6 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL
Address	8000A81509010C3F (SCOM)
Description	This register contains the sixth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_H1E_VAL: This field contains the DFE H1 value for the even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_B_H1O_VAL: This field contains the DFE H1 value for the odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 6 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL
Address	8000A81609010C3F (SCOM)
Description	This register contains the sixth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_H1E_VAL: This field contains the DFE H1 value for the even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_B_H1O_VAL: This field contains the DFE H1 value for the odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 6 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL6_O_PL
Address	8000A81709010C3F (SCOM)
Description	This register contains the sixth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_B_H1E_VAL: This field contains the DFE H1 value for the even samplers.
55	RO	constant = 0b0
56:62	RWX	RX_B_H1O_VAL: This field contains the DFE H1 value for the odd samplers.
63	RO	constant = 0b0

Register Name	Receive DAC Control 7 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL
Address	8000B00009010C3F (SCOM)
Description	This register contains the seventh set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_E_CONTROLS: Bit 0 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 1 = This bit enables the amp DAC for measurements in this bank. Bit 2 = This bit enables the fence for initloff.
51:63	RO	constant = 0b0000000000000

Register Name	Receive DAC Control 7 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL
Address	8000B00109010C3F (SCOM)
Description	This register contains the seventh set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_E_CONTROLS: Bit 0 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 1 = This bit enables the amp DAC for measurements in this bank. Bit 2 = This bit enables the fence for initloff.
51:63	RO	constant = 0b0000000000000

Register Name	Receive DAC Control 7 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL
Address	8000B00209010C3F (SCOM)
Description	This register contains the seventh set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_E_CONTROLS: Bit 0 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 1 = This bit enables the amp DAC for measurements in this bank. Bit 2 = This bit enables the fence for initloff.
51:63	RO	constant = 0b0000000000000

Register Name	Receive DAC Control 7 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL
Address	8000B00309010C3F (SCOM)
Description	This register contains the seventh set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_E_CONTROLS: Bit 0 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 1 = This bit enables the amp DAC for measurements in this bank. Bit 2 = This bit enables the fence for initloff.
51:63	RO	constant = 0b0000000000000

Register Name	Receive DAC Control 7 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL
Address	8000B00409010C3F (SCOM)
Description	This register contains the seventh set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_E_CONTROLS: Bit 0 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 1 = This bit enables the amp DAC for measurements in this bank. Bit 2 = This bit enables the fence for initloff.
51:63	RO	constant = 0b0000000000000

Register Name	Receive DAC Control 7 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL
Address	8000B00509010C3F (SCOM)
Description	This register contains the seventh set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_E_CONTROLS: Bit 0 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 1 = This bit enables the amp DAC for measurements in this bank. Bit 2 = This bit enables the fence for initloff.
51:63	RO	constant = 0b0000000000000

Register Name	Receive DAC Control 7 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL
Address	8000B00609010C3F (SCOM)
Description	This register contains the seventh set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_E_CONTROLS: Bit 0 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 1 = This bit enables the amp DAC for measurements in this bank. Bit 2 = This bit enables the fence for initloff.
51:63	RO	constant = 0b0000000000000

Register Name	Receive DAC Control 7 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL
Address	8000B00709010C3F (SCOM)
Description	This register contains the seventh set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_E_CONTROLS: Bit 0 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 1 = This bit enables the amp DAC for measurements in this bank. Bit 2 = This bit enables the fence for initloff.
51:63	RO	constant = 0b0000000000000

Register Name	Receive DAC Control 7 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL
Address	8000B00809010C3F (SCOM)
Description	This register contains the seventh set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_E_CONTROLS: Bit 0 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 1 = This bit enables the amp DAC for measurements in this bank. Bit 2 = This bit enables the fence for initloff.
51:63	RO	constant = 0b0000000000000

Register Name	Receive DAC Control 7 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL
Address	8000B00909010C3F (SCOM)
Description	This register contains the seventh set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_E_CONTROLS: Bit 0 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 1 = This bit enables the amp DAC for measurements in this bank. Bit 2 = This bit enables the fence for initloff.
51:63	RO	constant = 0b0000000000000

Register Name	Receive DAC Control 7 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL
Address	8000B00A09010C3F (SCOM)
Description	This register contains the seventh set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_E_CONTROLS: Bit 0 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 1 = This bit enables the amp DAC for measurements in this bank. Bit 2 = This bit enables the fence for initloff.
51:63	RO	constant = 0b0000000000000

Register Name	Receive DAC Control 7 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL
Address	8000B00B09010C3F (SCOM)
Description	This register contains the seventh set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_E_CONTROLS: Bit 0 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 1 = This bit enables the amp DAC for measurements in this bank. Bit 2 = This bit enables the fence for initloff.
51:63	RO	constant = 0b0000000000000

Register Name	Receive DAC Control 7 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL
Address	8000B00C09010C3F (SCOM)
Description	This register contains the seventh set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_E_CONTROLS: Bit 0 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 1 = This bit enables the amp DAC for measurements in this bank. Bit 2 = This bit enables the fence for initloff.
51:63	RO	constant = 0b0000000000000

Register Name	Receive DAC Control 7 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL
Address	8000B00D09010C3F (SCOM)
Description	This register contains the seventh set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_E_CONTROLS: Bit 0 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 1 = This bit enables the amp DAC for measurements in this bank. Bit 2 = This bit enables the fence for initloff.
51:63	RO	constant = 0b0000000000000

Register Name	Receive DAC Control 7 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL
Address	8000B00E09010C3F (SCOM)
Description	This register contains the seventh set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_E_CONTROLS: Bit 0 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 1 = This bit enables the amp DAC for measurements in this bank. Bit 2 = This bit enables the fence for initloff.
51:63	RO	constant = 0b0000000000000

Register Name	Receive DAC Control 7 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL
Address	8000B00F09010C3F (SCOM)
Description	This register contains the seventh set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_E_CONTROLS: Bit 0 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 1 = This bit enables the amp DAC for measurements in this bank. Bit 2 = This bit enables the fence for initloff.
51:63	RO	constant = 0b0000000000000

Register Name	Receive DAC Control 7 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL
Address	8000B01009010C3F (SCOM)
Description	This register contains the seventh set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_E_CONTROLS: Bit 0 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 1 = This bit enables the amp DAC for measurements in this bank. Bit 2 = This bit enables the fence for initloff.
51:63	RO	constant = 0b0000000000000

Register Name	Receive DAC Control 7 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL
Address	8000B01109010C3F (SCOM)
Description	This register contains the seventh set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_E_CONTROLS: Bit 0 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 1 = This bit enables the amp DAC for measurements in this bank. Bit 2 = This bit enables the fence for initloff.
51:63	RO	constant = 0b0000000000000

Register Name	Receive DAC Control 7 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL
Address	8000B01209010C3F (SCOM)
Description	This register contains the seventh set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_E_CONTROLS: Bit 0 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 1 = This bit enables the amp DAC for measurements in this bank. Bit 2 = This bit enables the fence for initloff.
51:63	RO	constant = 0b0000000000000

Register Name	Receive DAC Control 7 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL
Address	8000B01309010C3F (SCOM)
Description	This register contains the seventh set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_E_CONTROLS: Bit 0 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 1 = This bit enables the amp DAC for measurements in this bank. Bit 2 = This bit enables the fence for initloff.
51:63	RO	constant = 0b0000000000000

Register Name	Receive DAC Control 7 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL
Address	8000B01409010C3F (SCOM)
Description	This register contains the seventh set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_E_CONTROLS: Bit 0 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 1 = This bit enables the amp DAC for measurements in this bank. Bit 2 = This bit enables the fence for initloff.
51:63	RO	constant = 0b0000000000000

Register Name	Receive DAC Control 7 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL
Address	8000B01509010C3F (SCOM)
Description	This register contains the seventh set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_E_CONTROLS: Bit 0 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 1 = This bit enables the amp DAC for measurements in this bank. Bit 2 = This bit enables the fence for initloff.
51:63	RO	constant = 0b0000000000000

Register Name	Receive DAC Control 7 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL
Address	8000B01609010C3F (SCOM)
Description	This register contains the seventh set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_E_CONTROLS: Bit 0 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 1 = This bit enables the amp DAC for measurements in this bank. Bit 2 = This bit enables the fence for initloff.
51:63	RO	constant = 0b0000000000000

Register Name	Receive DAC Control 7 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL7_O_PL
Address	8000B01709010C3F (SCOM)
Description	This register contains the seventh set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_E_CONTROLS: Bit 0 = When set, this bit puts this lane's front end into offset cancellation mode. It is also needed for common- mode calibration. Bit 1 = This bit enables the amp DAC for measurements in this bank. Bit 2 = This bit enables the fence for initloff.
51:63	RO	constant = 0b0000000000000

Register Name	Receive DAC Control 8 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL
Address	8000B80009010C3F (SCOM)
Description	This register contains the eighth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_E_OFFSET_E: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_E_OFFSET_O: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	**Receive DAC Control 8 O Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL
Address	8000B80109010C3F (SCOM)
Description	This register contains the eighth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_E_OFFSET_E: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_E_OFFSET_O: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	**Receive DAC Control 8 O Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL
Address	8000B80209010C3F (SCOM)
Description	This register contains the eighth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_E_OFFSET_E: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_E_OFFSET_O: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	**Receive DAC Control 8 O Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL
Address	8000B80309010C3F (SCOM)
Description	This register contains the eighth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_E_OFFSET_E: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_E_OFFSET_O: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 8 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL
Address	8000B80409010C3F (SCOM)
Description	This register contains the eighth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_E_OFFSET_E: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_E_OFFSET_O: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 8 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL
Address	8000B80509010C3F (SCOM)
Description	This register contains the eighth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_E_OFFSET_E: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_E_OFFSET_O: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 8 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL
Address	8000B80609010C3F (SCOM)
Description	This register contains the eighth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_E_OFFSET_E: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_E_OFFSET_O: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.

Bits	SCOM	Field Mnemonic: Description
63	RO	constant = 0b0

Register Name	Receive DAC Control 8 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL
Address	8000B80709010C3F (SCOM)
Description	This register contains the eighth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_E_OFFSET_E: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_E_OFFSET_O: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 8 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL
Address	8000B80809010C3F (SCOM)
Description	This register contains the eighth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_E_OFFSET_E: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_E_OFFSET_O: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 8 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL
Address	8000B80909010C3F (SCOM)
Description	This register contains the eighth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_E_OFFSET_E: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.

Bits	SCOM	Field Mnemonic: Description
55	RO	constant = 0b0
56:62	RWX	RX_E_OFFSET_O: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 8 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL
Address	8000B80A09010C3F (SCOM)
Description	This register contains the eighth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_E_OFFSET_E: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_E_OFFSET_O: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 8 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL
Address	8000B80B09010C3F (SCOM)
Description	This register contains the eighth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_E_OFFSET_E: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_E_OFFSET_O: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 8 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL
Address	8000B80C09010C3F (SCOM)
Description	This register contains the eighth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_E_OFFSET_E: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_E_OFFSET_O: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 8 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL
Address	8000B80D09010C3F (SCOM)
Description	This register contains the eighth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_E_OFFSET_E: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_E_OFFSET_O: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 8 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL
Address	8000B80E09010C3F (SCOM)
Description	This register contains the eighth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_E_OFFSET_E: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_E_OFFSET_O: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 8 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL
Address	8000B80F09010C3F (SCOM)
Description	This register contains the eighth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_E_OFFSET_E: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_E_OFFSET_O: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 8 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL
Address	8000B81009010C3F (SCOM)
Description	This register contains the eighth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_E_OFFSET_E: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_E_OFFSET_O: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 8 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL
Address	8000B81109010C3F (SCOM)
Description	This register contains the eighth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_E_OFFSET_E: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_E_OFFSET_O: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 8 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL
Address	8000B81209010C3F (SCOM)
Description	This register contains the eighth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_E_OFFSET_E: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_E_OFFSET_O: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 8 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL
Address	8000B81309010C3F (SCOM)
Description	This register contains the eighth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_E_OFFSET_E: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_E_OFFSET_O: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 8 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL
Address	8000B81409010C3F (SCOM)
Description	This register contains the eighth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_E_OFFSET_E: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_E_OFFSET_O: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.

Bits	SCOM	Field Mnemonic: Description
63	RO	constant = 0b0

Register Name	Receive DAC Control 8 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL
Address	8000B81509010C3F (SCOM)
Description	This register contains the eighth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_E_OFFSET_E: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_E_OFFSET_O: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 8 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL
Address	8000B81609010C3F (SCOM)
Description	This register contains the eighth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_E_OFFSET_E: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.
55	RO	constant = 0b0
56:62	RWX	RX_E_OFFSET_O: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	Receive DAC Control 8 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL8_O_PL
Address	8000B81709010C3F (SCOM)
Description	This register contains the eighth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_E_OFFSET_E: This is the vertical offset of the even low-threshold sampling latch. The step size is Vio/256.

Bits	SCOM	Field Mnemonic: Description
55	RO	constant = 0b0
56:62	RWX	RX_E_OFFSET_O: This is the vertical offset of the odd low-threshold sampling latch. The step size is Vio/256.
63	RO	constant = 0b0

Register Name	**Receive DAC Control 9 O Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL
Address	8000C00009010C3F (SCOM)
Description	This register contains the ninth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_E_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_E_ODD_INTEG_FINE_GAIN: This is the odd integrator fine gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	**Receive DAC Control 9 O Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL
Address	8000C00109010C3F (SCOM)
Description	This register contains the ninth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_E_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_E_ODD_INTEG_FINE_GAIN: This is the odd integrator fine gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	**Receive DAC Control 9 O Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL
Address	8000C00209010C3F (SCOM)
Description	This register contains the ninth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_E_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_E_ODD_INTEG_FINE_GAIN: This is the odd integrator fine gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL
Address	8000C00309010C3F (SCOM)
Description	This register contains the ninth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_E_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_E_ODD_INTEG_FINE_GAIN: This is the odd integrator fine gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL
Address	8000C00409010C3F (SCOM)
Description	This register contains the ninth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_E_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_E_ODD_INTEG_FINE_GAIN: This is the odd integrator fine gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL
Address	8000C00509010C3F (SCOM)
Description	This register contains the ninth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_E_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_E_ODD_INTEG_FINE_GAIN: This is the odd integrator fine gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL
Address	8000C00609010C3F (SCOM)
Description	This register contains the ninth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_E_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_E_ODD_INTEG_FINE_GAIN: This is the odd integrator fine gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL
Address	8000C00709010C3F (SCOM)
Description	This register contains the ninth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_E_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.

Bits	SCOM	Field Mnemonic: Description
57:61	RWX	RX_E_ODD_INTEG_FINE_GAIN: This is the odd integrator fine gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL
Address	8000C00809010C3F (SCOM)
Description	This register contains the ninth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_E_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_E_ODD_INTEG_FINE_GAIN: This is the odd integrator fine gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL
Address	8000C00909010C3F (SCOM)
Description	This register contains the ninth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_E_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_E_ODD_INTEG_FINE_GAIN: This is the odd integrator fine gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL
Address	8000C00A09010C3F (SCOM)
Description	This register contains the ninth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_E_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_E_ODD_INTEG_FINE_GAIN: This is the odd integrator fine gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL
Address	8000C00B09010C3F (SCOM)
Description	This register contains the ninth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_E_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_E_ODD_INTEG_FINE_GAIN: This is the odd integrator fine gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL
Address	8000C00C09010C3F (SCOM)
Description	This register contains the ninth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_E_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_E_ODD_INTEG_FINE_GAIN: This is the odd integrator fine gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL
Address	8000C00D09010C3F (SCOM)
Description	This register contains the ninth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_E_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_E_ODD_INTEG_FINE_GAIN: This is the odd integrator fine gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL
Address	8000C00E09010C3F (SCOM)
Description	This register contains the ninth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_E_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_E_ODD_INTEG_FINE_GAIN: This is the odd integrator fine gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL
Address	8000C00F09010C3F (SCOM)
Description	This register contains the ninth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_E_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.

Bits	SCOM	Field Mnemonic: Description
57:61	RWX	RX_E_ODD_INTEG_FINE_GAIN: This is the odd integrator fine gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL
Address	8000C01009010C3F (SCOM)
Description	This register contains the ninth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_E_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_E_ODD_INTEG_FINE_GAIN: This is the odd integrator fine gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL
Address	8000C01109010C3F (SCOM)
Description	This register contains the ninth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_E_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_E_ODD_INTEG_FINE_GAIN: This is the odd integrator fine gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL
Address	8000C01209010C3F (SCOM)
Description	This register contains the ninth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_E_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_E_ODD_INTEG_FINE_GAIN: This is the odd integrator fine gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL
Address	8000C01309010C3F (SCOM)
Description	This register contains the ninth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_E_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_E_ODD_INTEG_FINE_GAIN: This is the odd integrator fine gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL
Address	8000C01409010C3F (SCOM)
Description	This register contains the ninth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_E_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_E_ODD_INTEG_FINE_GAIN: This is the odd integrator fine gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL
Address	8000C01509010C3F (SCOM)
Description	This register contains the ninth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_E_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_E_ODD_INTEG_FINE_GAIN: This is the odd integrator fine gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL
Address	8000C01609010C3F (SCOM)
Description	This register contains the ninth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_E_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.
57:61	RWX	RX_E_ODD_INTEG_FINE_GAIN: This is the odd integrator fine gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 9 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL9_O_PL
Address	8000C01709010C3F (SCOM)
Description	This register contains the ninth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_INTEG_COARSE_GAIN: This is the integrator coarse-gain control used in making common mode adjustments.
52:56	RWX	RX_E_EVEN_INTEG_FINE_GAIN: This is the even integrator fine-gain control used in making common mode adjustments.

Bits	SCOM	Field Mnemonic: Description
57:61	RWX	RX_E_ODD_INTEG_FINE_GAIN: This is the odd integrator fine gain control used in making common mode adjustments.
62:63	RO	constant = 0b00

Register Name	Receive DAC Control 10 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL
Address	8000C80009010C3F (SCOM)
Description	This register contains the tenth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_E_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 10 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL
Address	8000C80109010C3F (SCOM)
Description	This register contains the tenth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_E_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 10 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL
Address	8000C80209010C3F (SCOM)
Description	This register contains the tenth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_E_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 10 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL
Address	8000C80309010C3F (SCOM)
Description	This register contains the tenth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_E_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 10 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL
Address	8000C80409010C3F (SCOM)
Description	This register contains the tenth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_E_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 10 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL
Address	8000C80509010C3F (SCOM)
Description	This register contains the tenth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_E_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 10 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL
Address	8000C80609010C3F (SCOM)
Description	This register contains the tenth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_E_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 10 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL
Address	8000C80709010C3F (SCOM)
Description	This register contains the tenth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_E_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 10 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL
Address	8000C80809010C3F (SCOM)
Description	This register contains the tenth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_E_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 10 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL
Address	8000C80909010C3F (SCOM)
Description	This register contains the tenth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_E_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 10 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL
Address	8000C80A09010C3F (SCOM)
Description	This register contains the tenth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_E_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 10 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL
Address	8000C80B09010C3F (SCOM)
Description	This register contains the tenth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_E_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 10 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL
Address	8000C80C09010C3F (SCOM)
Description	This register contains the tenth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_E_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 10 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL
Address	8000C80D09010C3F (SCOM)
Description	This register contains the tenth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_E_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 10 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL
Address	8000C80E09010C3F (SCOM)
Description	This register contains the tenth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_E_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 10 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL
Address	8000C80F09010C3F (SCOM)
Description	This register contains the tenth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_E_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 10 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL
Address	8000C81009010C3F (SCOM)
Description	This register contains the tenth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_E_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	**Receive DAC Control 10 O Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL
Address	8000C81109010C3F (SCOM)
Description	This register contains the tenth set of O controls.

Bits	**SCOM**	**Field Mnemonic: Description**
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_E_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	**Receive DAC Control 10 O Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL
Address	8000C81209010C3F (SCOM)
Description	This register contains the tenth set of O controls.

Bits	**SCOM**	**Field Mnemonic: Description**
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_E_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	**Receive DAC Control 10 O Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL
Address	8000C81309010C3F (SCOM)
Description	This register contains the tenth set of O controls.

Bits	**SCOM**	**Field Mnemonic: Description**
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_E_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	**Receive DAC Control 10 O Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL
Address	8000C81409010C3F (SCOM)
Description	This register contains the tenth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_E_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 10 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL
Address	8000C81509010C3F (SCOM)
Description	This register contains the tenth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_E_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 10 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL
Address	8000C81609010C3F (SCOM)
Description	This register contains the tenth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_E_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	Receive DAC Control 10 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RX_DAC_REGS.RX_DAC_REGS.RX_DAC_CNTL10_O_PL
Address	8000C81709010C3F (SCOM)
Description	This register contains the tenth set of O controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_E_CTLE_COARSE: This is the CTLE coarse peak value.
52:55	RWX	RX_E_CTLE_GAIN: This is the CTLE gain setting.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	8002000009010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	8002000109010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	8002000209010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	8002000309010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	8002000409010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	8002000509010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	8002000609010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	8002000709010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	8002000809010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	8002000909010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Spare Mode Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	8002000A09010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Spare Mode Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	8002000B09010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	8002000C09010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	8002000D09010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Spare Mode Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	8002000E09010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Spare Mode Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	8002000F09010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Spare Mode Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	8002001009010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	8002001109010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	8002001209010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	8002001309010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	8002001409010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	8002001509010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	8002001609010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	8002001709010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_PL
Address	8002080009010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_PL
Address	8002080109010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_PL
Address	8002080209010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_PL
Address	8002080309010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_PL
Address	8002080409010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_PL
Address	8002080509010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_PL
Address	8002080609010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_PL
Address	8002080709010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_PL
Address	8002080809010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_PL
Address	8002080909010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_PL
Address	8002080A09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_PL
Address	8002080B09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_PL
Address	8002080C09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_PL
Address	8002080D09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_PL
Address	8002080E09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_PL
Address	8002080F09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_PL
Address	8002081009010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_PL
Address	8002081109010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_PL
Address	8002081209010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_PL
Address	8002081309010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_PL
Address	8002081409010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_PL
Address	8002081509010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_PL
Address	8002081609010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	**Receive FIR Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_PL
Address	8002081709010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	**Receive FIR Mask Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8002100009010C3F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	**Receive FIR Mask Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8002100109010C3F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	**Receive FIR Mask Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8002100209010C3F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8002100309010C3F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8002100409010C3F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8002100509010C3F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8002100609010C3F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8002100709010C3F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8002100809010C3F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8002100909010C3F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8002100A09010C3F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8002100B09010C3F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8002100C09010C3F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8002100D09010C3F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8002100E09010C3F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	**Receive FIR Mask Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8002100F09010C3F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	**Receive FIR Mask Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8002101009010C3F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	**Receive FIR Mask Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8002101109010C3F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	**Receive FIR Mask Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8002101209010C3F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8002101309010C3F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8002101409010C3F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8002101509010C3F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8002101609010C3F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Mask Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8002101709010C3F (SCOM)
Description	This register masks receive FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pl errors.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8002180009010C3F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8002180109010C3F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8002180209010C3F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8002180309010C3F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8002180409010C3F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8002180509010C3F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8002180609010C3F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8002180709010C3F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8002180809010C3F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	**Receive FIR Error Inject Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8002180909010C3F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	**Receive FIR Error Inject Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8002180A09010C3F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	**Receive FIR Error Inject Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8002180B09010C3F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	**Receive FIR Error Inject Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8002180C09010C3F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8002180D09010C3F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8002180E09010C3F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8002180F09010C3F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8002181009010C3F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8002181109010C3F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8002181209010C3F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8002181309010C3F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8002181409010C3F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8002181509010C3F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8002181609010C3F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive FIR Error Inject Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8002181709010C3F (SCOM)
Description	This register is used to inject errors into the per-lane Receive Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: When a bit in this field is set to 1, it inverts the parity check bit to force an error on the per-lane Receive Registers.
51:63	RO	constant = 0b0000000000000

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	8002200009010C3F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50	RWX	RX_DECOUPLE_EDGE_A: This bit enables a mode where phase rotator A is decoupled from the edge. Its position is directly equal to the rx_pr_data_a_offset value.
51	RWX	RX_DECOUPLE_EDGE_B: This bit enables a mode where phase rotator B is decoupled from the edge. Its position is directly equal to the rx_pr_data_b_offset value.
52	RWX	RX_PSAVE_DIG_REQ_DIS: This bit disables digital RX slice power gating from link-layer psav_req control.
53	RWX	RX_PSAVE_ANA_REQ_DIS: This bit disables analog RX slice power gating from link-layer psav_req control.
54:63	RO	constant = 0b0000000000

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	8002200109010C3F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50	RWX	RX_DECOUPLE_EDGE_A: This bit enables a mode where phase rotator A is decoupled from the edge. Its position is directly equal to the rx_pr_data_a_offset value.

Bits	SCOM	Field Mnemonic: Description
51	RWX	RX_DECOUPLE_EDGE_B: This bit enables a mode where phase rotator B is decoupled from the edge. Its position is directly equal to the rx_pr_data_b_offset value.
52	RWX	RX_PSAVE_DIG_REQ_DIS: This bit disables digital RX slice power gating from link-layer psav_req control.
53	RWX	RX_PSAVE_ANA_REQ_DIS: This bit disables analog RX slice power gating from link-layer psav_req control.
54:63	RO	constant = 0b0000000000

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	8002200209010C3F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50	RWX	RX_DECOUPLE_EDGE_A: This bit enables a mode where phase rotator A is decoupled from the edge. Its position is directly equal to the rx_pr_data_a_offset value.
51	RWX	RX_DECOUPLE_EDGE_B: This bit enables a mode where phase rotator B is decoupled from the edge. Its position is directly equal to the rx_pr_data_b_offset value.
52	RWX	RX_PSAVE_DIG_REQ_DIS: This bit disables digital RX slice power gating from link-layer psav_req control.
53	RWX	RX_PSAVE_ANA_REQ_DIS: This bit disables analog RX slice power gating from link-layer psav_req control.
54:63	RO	constant = 0b0000000000

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	8002200309010C3F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50	RWX	RX_DECOUPLE_EDGE_A: This bit enables a mode where phase rotator A is decoupled from the edge. Its position is directly equal to the rx_pr_data_a_offset value.
51	RWX	RX_DECOUPLE_EDGE_B: This bit enables a mode where phase rotator B is decoupled from the edge. Its position is directly equal to the rx_pr_data_b_offset value.
52	RWX	RX_PSAVE_DIG_REQ_DIS: This bit disables digital RX slice power gating from link-layer psav_req control.
53	RWX	RX_PSAVE_ANA_REQ_DIS: This bit disables analog RX slice power gating from link-layer psav_req control.

Bits	SCOM	Field Mnemonic: Description
54:63	RO	constant = 0b0000000000

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	8002200409010C3F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50	RWX	RX_DECOUPLE_EDGE_A: This bit enables a mode where phase rotator A is decoupled from the edge. Its position is directly equal to the rx_pr_data_a_offset value.
51	RWX	RX_DECOUPLE_EDGE_B: This bit enables a mode where phase rotator B is decoupled from the edge. Its position is directly equal to the rx_pr_data_b_offset value.
52	RWX	RX_PSAVE_DIG_REQ_DIS: This bit disables digital RX slice power gating from link-layer psav_req control.
53	RWX	RX_PSAVE_ANA_REQ_DIS: This bit disables analog RX slice power gating from link-layer psav_req control.
54:63	RO	constant = 0b0000000000

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	8002200509010C3F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50	RWX	RX_DECOUPLE_EDGE_A: This bit enables a mode where phase rotator A is decoupled from the edge. Its position is directly equal to the rx_pr_data_a_offset value.
51	RWX	RX_DECOUPLE_EDGE_B: This bit enables a mode where phase rotator B is decoupled from the edge. Its position is directly equal to the rx_pr_data_b_offset value.
52	RWX	RX_PSAVE_DIG_REQ_DIS: This bit disables digital RX slice power gating from link-layer psav_req control.
53	RWX	RX_PSAVE_ANA_REQ_DIS: This bit disables analog RX slice power gating from link-layer psav_req control.
54:63	RO	constant = 0b0000000000

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	8002200609010C3F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50	RWX	RX_DECOUPLE_EDGE_A: This bit enables a mode where phase rotator A is decoupled from the edge. Its position is directly equal to the rx_pr_data_a_offset value.
51	RWX	RX_DECOUPLE_EDGE_B: This bit enables a mode where phase rotator B is decoupled from the edge. Its position is directly equal to the rx_pr_data_b_offset value.
52	RWX	RX_PSAVE_DIG_REQ_DIS: This bit disables digital RX slice power gating from link-layer psav_req control.
53	RWX	RX_PSAVE_ANA_REQ_DIS: This bit disables analog RX slice power gating from link-layer psav_req control.
54:63	RO	constant = 0b0000000000

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	8002200709010C3F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50	RWX	RX_DECOUPLE_EDGE_A: This bit enables a mode where phase rotator A is decoupled from the edge. Its position is directly equal to the rx_pr_data_a_offset value.
51	RWX	RX_DECOUPLE_EDGE_B: This bit enables a mode where phase rotator B is decoupled from the edge. Its position is directly equal to the rx_pr_data_b_offset value.
52	RWX	RX_PSAVE_DIG_REQ_DIS: This bit disables digital RX slice power gating from link-layer psav_req control.
53	RWX	RX_PSAVE_ANA_REQ_DIS: This bit disables analog RX slice power gating from link-layer psav_req control.
54:63	RO	constant = 0b0000000000

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	8002200809010C3F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50	RWX	RX_DECOUPLE_EDGE_A: This bit enables a mode where phase rotator A is decoupled from the edge. Its position is directly equal to the rx_pr_data_a_offset value.
51	RWX	RX_DECOUPLE_EDGE_B: This bit enables a mode where phase rotator B is decoupled from the edge. Its position is directly equal to the rx_pr_data_b_offset value.
52	RWX	RX_PSAVE_DIG_REQ_DIS: This bit disables digital RX slice power gating from link-layer psav_req control.
53	RWX	RX_PSAVE_ANA_REQ_DIS: This bit disables analog RX slice power gating from link-layer psav_req control.
54:63	RO	constant = 0b0000000000

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	8002200909010C3F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50	RWX	RX_DECOUPLE_EDGE_A: This bit enables a mode where phase rotator A is decoupled from the edge. Its position is directly equal to the rx_pr_data_a_offset value.
51	RWX	RX_DECOUPLE_EDGE_B: This bit enables a mode where phase rotator B is decoupled from the edge. Its position is directly equal to the rx_pr_data_b_offset value.
52	RWX	RX_PSAVE_DIG_REQ_DIS: This bit disables digital RX slice power gating from link-layer psav_req control.
53	RWX	RX_PSAVE_ANA_REQ_DIS: This bit disables analog RX slice power gating from link-layer psav_req control.
54:63	RO	constant = 0b0000000000

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	8002200A09010C3F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.

Bits	SCOM	Field Mnemonic: Description
50	RWX	RX_DECOUPLE_EDGE_A: This bit enables a mode where phase rotator A is decoupled from the edge. Its position is directly equal to the rx_pr_data_a_offset value.
51	RWX	RX_DECOUPLE_EDGE_B: This bit enables a mode where phase rotator B is decoupled from the edge. Its position is directly equal to the rx_pr_data_b_offset value.
52	RWX	RX_PSAVE_DIG_REQ_DIS: This bit disables digital RX slice power gating from link-layer psav_req control.
53	RWX	RX_PSAVE_ANA_REQ_DIS: This bit disables analog RX slice power gating from link-layer psav_req control.
54:63	RO	constant = 0b0000000000

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	8002200B09010C3F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50	RWX	RX_DECOUPLE_EDGE_A: This bit enables a mode where phase rotator A is decoupled from the edge. Its position is directly equal to the rx_pr_data_a_offset value.
51	RWX	RX_DECOUPLE_EDGE_B: This bit enables a mode where phase rotator B is decoupled from the edge. Its position is directly equal to the rx_pr_data_b_offset value.
52	RWX	RX_PSAVE_DIG_REQ_DIS: This bit disables digital RX slice power gating from link-layer psav_req control.
53	RWX	RX_PSAVE_ANA_REQ_DIS: This bit disables analog RX slice power gating from link-layer psav_req control.
54:63	RO	constant = 0b0000000000

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	8002200C09010C3F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50	RWX	RX_DECOUPLE_EDGE_A: This bit enables a mode where phase rotator A is decoupled from the edge. Its position is directly equal to the rx_pr_data_a_offset value.
51	RWX	RX_DECOUPLE_EDGE_B: This bit enables a mode where phase rotator B is decoupled from the edge. Its position is directly equal to the rx_pr_data_b_offset value.
52	RWX	RX_PSAVE_DIG_REQ_DIS: This bit disables digital RX slice power gating from link-layer psav_req control.

Bits	SCOM	Field Mnemonic: Description
53	RWX	RX_PSAVE_ANA_REQ_DIS: This bit disables analog RX slice power gating from link-layer psav_req control.
54:63	RO	constant = 0b0000000000

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	8002200D09010C3F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50	RWX	RX_DECOUPLE_EDGE_A: This bit enables a mode where phase rotator A is decoupled from the edge. Its position is directly equal to the rx_pr_data_a_offset value.
51	RWX	RX_DECOUPLE_EDGE_B: This bit enables a mode where phase rotator B is decoupled from the edge. Its position is directly equal to the rx_pr_data_b_offset value.
52	RWX	RX_PSAVE_DIG_REQ_DIS: This bit disables digital RX slice power gating from link-layer psav_req control.
53	RWX	RX_PSAVE_ANA_REQ_DIS: This bit disables analog RX slice power gating from link-layer psav_req control.
54:63	RO	constant = 0b0000000000

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	8002200E09010C3F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50	RWX	RX_DECOUPLE_EDGE_A: This bit enables a mode where phase rotator A is decoupled from the edge. Its position is directly equal to the rx_pr_data_a_offset value.
51	RWX	RX_DECOUPLE_EDGE_B: This bit enables a mode where phase rotator B is decoupled from the edge. Its position is directly equal to the rx_pr_data_b_offset value.
52	RWX	RX_PSAVE_DIG_REQ_DIS: This bit disables digital RX slice power gating from link-layer psav_req control.
53	RWX	RX_PSAVE_ANA_REQ_DIS: This bit disables analog RX slice power gating from link-layer psav_req control.
54:63	RO	constant = 0b0000000000

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	8002200F09010C3F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50	RWX	RX_DECOUPLE_EDGE_A: This bit enables a mode where phase rotator A is decoupled from the edge. Its position is directly equal to the rx_pr_data_a_offset value.
51	RWX	RX_DECOUPLE_EDGE_B: This bit enables a mode where phase rotator B is decoupled from the edge. Its position is directly equal to the rx_pr_data_b_offset value.
52	RWX	RX_PSAVE_DIG_REQ_DIS: This bit disables digital RX slice power gating from link-layer psav_req control.
53	RWX	RX_PSAVE_ANA_REQ_DIS: This bit disables analog RX slice power gating from link-layer psav_req control.
54:63	RO	constant = 0b0000000000

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	8002201009010C3F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50	RWX	RX_DECOUPLE_EDGE_A: This bit enables a mode where phase rotator A is decoupled from the edge. Its position is directly equal to the rx_pr_data_a_offset value.
51	RWX	RX_DECOUPLE_EDGE_B: This bit enables a mode where phase rotator B is decoupled from the edge. Its position is directly equal to the rx_pr_data_b_offset value.
52	RWX	RX_PSAVE_DIG_REQ_DIS: This bit disables digital RX slice power gating from link-layer psav_req control.
53	RWX	RX_PSAVE_ANA_REQ_DIS: This bit disables analog RX slice power gating from link-layer psav_req control.
54:63	RO	constant = 0b0000000000

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	8002201109010C3F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50	RWX	RX_DECOUPLE_EDGE_A: This bit enables a mode where phase rotator A is decoupled from the edge. Its position is directly equal to the rx_pr_data_a_offset value.
51	RWX	RX_DECOUPLE_EDGE_B: This bit enables a mode where phase rotator B is decoupled from the edge. Its position is directly equal to the rx_pr_data_b_offset value.
52	RWX	RX_PSAVE_DIG_REQ_DIS: This bit disables digital RX slice power gating from link-layer psav_req control.
53	RWX	RX_PSAVE_ANA_REQ_DIS: This bit disables analog RX slice power gating from link-layer psav_req control.
54:63	RO	constant = 0b0000000000

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	8002201209010C3F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50	RWX	RX_DECOUPLE_EDGE_A: This bit enables a mode where phase rotator A is decoupled from the edge. Its position is directly equal to the rx_pr_data_a_offset value.
51	RWX	RX_DECOUPLE_EDGE_B: This bit enables a mode where phase rotator B is decoupled from the edge. Its position is directly equal to the rx_pr_data_b_offset value.
52	RWX	RX_PSAVE_DIG_REQ_DIS: This bit disables digital RX slice power gating from link-layer psav_req control.
53	RWX	RX_PSAVE_ANA_REQ_DIS: This bit disables analog RX slice power gating from link-layer psav_req control.
54:63	RO	constant = 0b0000000000

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	8002201309010C3F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.

Bits	SCOM	Field Mnemonic: Description
50	RWX	RX_DECOUPLE_EDGE_A: This bit enables a mode where phase rotator A is decoupled from the edge. Its position is directly equal to the rx_pr_data_a_offset value.
51	RWX	RX_DECOUPLE_EDGE_B: This bit enables a mode where phase rotator B is decoupled from the edge. Its position is directly equal to the rx_pr_data_b_offset value.
52	RWX	RX_PSAVE_DIG_REQ_DIS: This bit disables digital RX slice power gating from link-layer psav_req control.
53	RWX	RX_PSAVE_ANA_REQ_DIS: This bit disables analog RX slice power gating from link-layer psav_req control.
54:63	RO	constant = 0b0000000000

Register Name	**Receive Bit Mode 1 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	8002201409010C3F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50	RWX	RX_DECOUPLE_EDGE_A: This bit enables a mode where phase rotator A is decoupled from the edge. Its position is directly equal to the rx_pr_data_a_offset value.
51	RWX	RX_DECOUPLE_EDGE_B: This bit enables a mode where phase rotator B is decoupled from the edge. Its position is directly equal to the rx_pr_data_b_offset value.
52	RWX	RX_PSAVE_DIG_REQ_DIS: This bit disables digital RX slice power gating from link-layer psav_req control.
53	RWX	RX_PSAVE_ANA_REQ_DIS: This bit disables analog RX slice power gating from link-layer psav_req control.
54:63	RO	constant = 0b0000000000

Register Name	**Receive Bit Mode 1 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	8002201509010C3F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50	RWX	RX_DECOUPLE_EDGE_A: This bit enables a mode where phase rotator A is decoupled from the edge. Its position is directly equal to the rx_pr_data_a_offset value.
51	RWX	RX_DECOUPLE_EDGE_B: This bit enables a mode where phase rotator B is decoupled from the edge. Its position is directly equal to the rx_pr_data_b_offset value.
52	RWX	RX_PSAVE_DIG_REQ_DIS: This bit disables digital RX slice power gating from link-layer psav_req control.

Bits	SCOM	Field Mnemonic: Description
53	RWX	RX_PSAVE_ANA_REQ_DIS: This bit disables analog RX slice power gating from link-layer psav_req control.
54:63	RO	constant = 0b0000000000

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	8002201609010C3F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50	RWX	RX_DECOUPLE_EDGE_A: This bit enables a mode where phase rotator A is decoupled from the edge. Its position is directly equal to the rx_pr_data_a_offset value.
51	RWX	RX_DECOUPLE_EDGE_B: This bit enables a mode where phase rotator B is decoupled from the edge. Its position is directly equal to the rx_pr_data_b_offset value.
52	RWX	RX_PSAVE_DIG_REQ_DIS: This bit disables digital RX slice power gating from link-layer psav_req control.
53	RWX	RX_PSAVE_ANA_REQ_DIS: This bit disables analog RX slice power gating from link-layer psav_req control.
54:63	RO	constant = 0b0000000000

Register Name	Receive Bit Mode 1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE1_EO_PL
Address	8002201709010C3F (SCOM)
Description	This register contains the first set of EO mode bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_DIG_PDWN: This bit is used to power down the digital logic for a lane.
49	RWX	RX_BER_DPIPE_MUX_SEL: Diag BER data pipe mux select. When this bit is set to 1, the XOR of the main and alt data is multiplexed onto the main data path feeding the data pipe.
50	RWX	RX_DECOUPLE_EDGE_A: This bit enables a mode where phase rotator A is decoupled from the edge. Its position is directly equal to the rx_pr_data_a_offset value.
51	RWX	RX_DECOUPLE_EDGE_B: This bit enables a mode where phase rotator B is decoupled from the edge. Its position is directly equal to the rx_pr_data_b_offset value.
52	RWX	RX_PSAVE_DIG_REQ_DIS: This bit disables digital RX slice power gating from link-layer psav_req control.
53	RWX	RX_PSAVE_ANA_REQ_DIS: This bit disables analog RX slice power gating from link-layer psav_req control.
54:63	RO	constant = 0b0000000000

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	8002280009010C3F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	RWX	RX_PR_FW_OFF: Removes the flywheel from the phase-rotator (PR) accumulator. **Note:** This is not the same as setting the inertia amount to zero.
57:59	RWX	RX_PR_FW_INERTIA_AMT: This field contains the amount to be added or subtracted from the flywheel inertia. **Note:** Setting this field to zero might not turn off the flywheel if the flywheel accumulator already has a value (as if it were turned off after having run for some time).
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	8002280109010C3F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	RWX	RX_PR_FW_OFF: Removes the flywheel from the PR accumulator. **Note:** This is not the same as setting the inertia amount to zero.
57:59	RWX	RX_PR_FW_INERTIA_AMT: This field contains the amount to be added or subtracted from the flywheel inertia. **Note:** Setting this field to zero might not turn off the flywheel if the flywheel accumulator already has a value (as if it were turned off after having run for some time).
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	8002280209010C3F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	RWX	RX_PR_FW_OFF: Removes the flywheel from the PR accumulator. **Note:** This is not the same as setting the inertia amount to zero.

Bits	SCOM	Field Mnemonic: Description
57:59	RWX	RX_PR_FW_INERTIA_AMT: This field contains the amount to be added or subtracted from the flywheel inertia. **Note:** Setting this field to zero might not turn off the flywheel if the flywheel accumulator already has a value (as if it were turned off after having run for some time).
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	8002280309010C3F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	RWX	RX_PR_FW_OFF: Removes the flywheel from the PR accumulator. **Note:** This is not the same as setting the inertia amount to zero.
57:59	RWX	RX_PR_FW_INERTIA_AMT: This field contains the amount to be added or subtracted from the flywheel inertia. **Note:** Setting this field to zero might not turn off the flywheel if the flywheel accumulator already has a value (as if it were turned off after having run for some time).
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	8002280409010C3F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	RWX	RX_PR_FW_OFF: Removes the flywheel from the PR accumulator. **Note:** This is not the same as setting the inertia amount to zero.
57:59	RWX	RX_PR_FW_INERTIA_AMT: This field contains the amount to be added or subtracted from the flywheel inertia. **Note:** Setting this field to zero might not turn off the flywheel if the flywheel accumulator already has a value (as if it were turned off after having run for some time).
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	8002280509010C3F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	RWX	RX_PR_FW_OFF: Removes the flywheel from the PR accumulator. **Note:** This is not the same as setting the inertia amount to zero.
57:59	RWX	RX_PR_FW_INERTIA_AMT: This field contains the amount to be added or subtracted from the flywheel inertia. **Note:** Setting this field to zero might not turn off the flywheel if the flywheel accumulator already has a value (as if it were turned off after having run for some time).
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	8002280609010C3F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	RWX	RX_PR_FW_OFF: Removes the flywheel from the PR accumulator. **Note:** This is not the same as setting the inertia amount to zero.
57:59	RWX	RX_PR_FW_INERTIA_AMT: This field contains the amount to be added or subtracted from the flywheel inertia. **Note:** Setting this field to zero might not turn off the flywheel if the flywheel accumulator already has a value (as if it were turned off after having run for some time).
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	8002280709010C3F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	RWX	RX_PR_FW_OFF: Removes the flywheel from the PR accumulator. **Note:** This is not the same as setting the inertia amount to zero.

Bits	SCOM	Field Mnemonic: Description
57:59	RWX	RX_PR_FW_INERTIA_AMT: This field contains the amount to be added or subtracted from the flywheel inertia. **Note:** Setting this field to zero might not turn off the flywheel if the flywheel accumulator already has a value (as if it were turned off after having run for some time).
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	8002280809010C3F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	RWX	RX_PR_FW_OFF: Removes the flywheel from the PR accumulator. **Note:** This is not the same as setting the inertia amount to zero.
57:59	RWX	RX_PR_FW_INERTIA_AMT: This field contains the amount to be added or subtracted from the flywheel inertia. **Note:** Setting this field to zero might not turn off the flywheel if the flywheel accumulator already has a value (as if it were turned off after having run for some time).
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	8002280909010C3F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	RWX	RX_PR_FW_OFF: Removes the flywheel from the PR accumulator. **Note:** This is not the same as setting the inertia amount to zero.
57:59	RWX	RX_PR_FW_INERTIA_AMT: This field contains the amount to be added or subtracted from the flywheel inertia. **Note:** Setting this field to zero might not turn off the flywheel if the flywheel accumulator already has a value (as if it were turned off after having run for some time).
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	8002280A09010C3F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	RWX	RX_PR_FW_OFF: Removes the flywheel from the PR accumulator. **Note:** This is not the same as setting the inertia amount to zero.
57:59	RWX	RX_PR_FW_INERTIA_AMT: This field contains the amount to be added or subtracted from the flywheel inertia. **Note:** Setting this field to zero might not turn off the flywheel if the flywheel accumulator already has a value (as if it were turned off after having run for some time).
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	8002280B09010C3F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	RWX	RX_PR_FW_OFF: Removes the flywheel from the PR accumulator. **Note:** This is not the same as setting the inertia amount to zero.
57:59	RWX	RX_PR_FW_INERTIA_AMT: This field contains the amount to be added or subtracted from the flywheel inertia. **Note:** Setting this field to zero might not turn off the flywheel if the flywheel accumulator already has a value (as if it were turned off after having run for some time).
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	8002280C09010C3F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	RWX	RX_PR_FW_OFF: Removes the flywheel from the PR accumulator. **Note:** This is not the same as setting the inertia amount to zero.

Bits	SCOM	Field Mnemonic: Description
57:59	RWX	RX_PR_FW_INERTIA_AMT: This field contains the amount to be added or subtracted from the flywheel inertia. **Note:** Setting this field to zero might not turn off the flywheel if the flywheel accumulator already has a value (as if it were turned off after having run for some time).
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	8002280D09010C3F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	RWX	RX_PR_FW_OFF: Removes the flywheel from the PR accumulator. **Note:** This is not the same as setting the inertia amount to zero.
57:59	RWX	RX_PR_FW_INERTIA_AMT: This field contains the amount to be added or subtracted from the flywheel inertia. **Note:** Setting this field to zero might not turn off the flywheel if the flywheel accumulator already has a value (as if it were turned off after having run for some time).
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	8002280E09010C3F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	RWX	RX_PR_FW_OFF: Removes the flywheel from the PR accumulator. **Note:** This is not the same as setting the inertia amount to zero.
57:59	RWX	RX_PR_FW_INERTIA_AMT: This field contains the amount to be added or subtracted from the flywheel inertia. **Note:** Setting this field to zero might not turn off the flywheel if the flywheel accumulator already has a value (as if it were turned off after having run for some time).
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	8002280F09010C3F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	RWX	RX_PR_FW_OFF: Removes the flywheel from the PR accumulator. **Note:** This is not the same as setting the inertia amount to zero.
57:59	RWX	RX_PR_FW_INERTIA_AMT: This field contains the amount to be added or subtracted from the flywheel inertia. **Note:** Setting this field to zero might not turn off the flywheel if the flywheel accumulator already has a value (as if it were turned off after having run for some time).
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	8002281009010C3F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	RWX	RX_PR_FW_OFF: Removes the flywheel from the PR accumulator. **Note:** This is not the same as setting the inertia amount to zero.
57:59	RWX	RX_PR_FW_INERTIA_AMT: This field contains the amount to be added or subtracted from the flywheel inertia. **Note:** Setting this field to zero might not turn off the flywheel if the flywheel accumulator already has a value (as if it were turned off after having run for some time).
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	8002281109010C3F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	RWX	RX_PR_FW_OFF: Removes the flywheel from the PR accumulator. **Note:** This is not the same as setting the inertia amount to zero.

Bits	SCOM	Field Mnemonic: Description
57:59	RWX	RX_PR_FW_INERTIA_AMT: This field contains the amount to be added or subtracted from the flywheel inertia. **Note:** Setting this field to zero might not turn off the flywheel if the flywheel accumulator already has a value (as if it were turned off after having run for some time).
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	8002281209010C3F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	RWX	RX_PR_FW_OFF: Removes the flywheel from the PR accumulator. **Note:** This is not the same as setting the inertia amount to zero.
57:59	RWX	RX_PR_FW_INERTIA_AMT: This field contains the amount to be added or subtracted from the flywheel inertia. **Note:** Setting this field to zero might not turn off the flywheel if the flywheel accumulator already has a value (as if it were turned off after having run for some time).
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	8002281309010C3F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	RWX	RX_PR_FW_OFF: Removes the flywheel from the PR accumulator. **Note:** This is not the same as setting the inertia amount to zero.
57:59	RWX	RX_PR_FW_INERTIA_AMT: This field contains the amount to be added or subtracted from the flywheel inertia. **Note:** Setting this field to zero might not turn off the flywheel if the flywheel accumulator already has a value (as if it were turned off after having run for some time).
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	8002281409010C3F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	RWX	RX_PR_FW_OFF: Removes the flywheel from the PR accumulator. **Note:** This is not the same as setting the inertia amount to zero.
57:59	RWX	RX_PR_FW_INERTIA_AMT: This field contains the amount to be added or subtracted from the flywheel inertia. **Note:** Setting this field to zero might not turn off the flywheel if the flywheel accumulator already has a value (as if it were turned off after having run for some time).
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	8002281509010C3F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	RWX	RX_PR_FW_OFF: Removes the flywheel from the PR accumulator. **Note:** This is not the same as setting the inertia amount to zero.
57:59	RWX	RX_PR_FW_INERTIA_AMT: This field contains the amount to be added or subtracted from the flywheel inertia. **Note:** Setting this field to zero might not turn off the flywheel if the flywheel accumulator already has a value (as if it were turned off after having run for some time).
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	Receive Bit Mode 2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	8002281609010C3F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	RWX	RX_PR_FW_OFF: Removes the flywheel from the PR accumulator. **Note:** This is not the same as setting the inertia amount to zero.

Bits	SCOM	Field Mnemonic: Description
57:59	RWX	RX_PR_FW_INERTIA_AMT: This field contains the amount to be added or subtracted from the flywheel inertia. **Note:** Setting this field to zero might not turn off the flywheel if the flywheel accumulator already has a value (as if it were turned off after having run for some time).
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	**Receive Bit Mode 2 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE2_EO_PL
Address	8002281709010C3F (SCOM)
Description	This register contains the second set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	RWX	RX_PR_FW_OFF: Removes the flywheel from the PR accumulator. **Note:** This is not the same as setting the inertia amount to zero.
57:59	RWX	RX_PR_FW_INERTIA_AMT: This field contains the amount to be added or subtracted from the flywheel inertia. **Note:** Setting this field to zero might not turn off the flywheel if the flywheel accumulator already has a value (as if it were turned off after having run for some time).
60:63	RWX	RX_PR_PHASE_STEP: This field contains the amount to be added to or subtracted from the phase rotator accumulator on each shift left or right. The value 0000 is decoded as b10000 in logic. Therefore, the PR updates every four shifts. Other values update with every 4 x (16/phase_step) shifts.

Register Name	**Receive Bit Mode 3 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	8002300009010C3F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	**Receive Bit Mode 3 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	8002300109010C3F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	8002300209010C3F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	8002300309010C3F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	8002300409010C3F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	8002300509010C3F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	8002300609010C3F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	8002300709010C3F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	8002300809010C3F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	8002300909010C3F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	8002300A09010C3F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	8002300B09010C3F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	8002300C09010C3F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	8002300D09010C3F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	8002300E09010C3F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	8002300F09010C3F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	8002301009010C3F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	8002301109010C3F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	8002301209010C3F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	8002301309010C3F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	8002301409010C3F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	8002301509010C3F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	8002301609010C3F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE3_EO_PL
Address	8002301709010C3F (SCOM)
Description	This register contains the third set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_BER_CFG: This register controls the bit-error-rate threshold used for DDC.
51:52	RWX	RX_FIFO_DLY_CFG: This register controls how many parallel clock cycles we wait after every change to the phase rotator before we begin using the data again.
53:54	RWX	RX_DDC_CFG: This register controls how many parallel clock cycles we wait while looking for errors as we progress further into the edge.
55:63	RO	constant = 0b000000000

Register Name	Receive Bit Mode 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL
Address	8002380009010C3F (SCOM)
Description	This register contains the fourth set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_COARSE_MODE_EN: This bit enables the CDR to switch into coarse mode, as needed, on a CDR stop/start or on an invalid lock (if enabled).
49	RWX	RX_PR_INVALID_LOCK_COARSE_EN: This bit enables the CDR to switch into coarse mode, when enabled, on an invalid lock. It remains in coarse mode until there are no invalid locks, regardless of this bit.
50:52	RWX	RX_PR_FW_INERTIA_AMT_COARSE: This field contains the flywheel inertia in coarse mode. For more information, see the RX_PR_FW_INERTIA_AMT field in the Receive Bit Mode 2 EO Per-Lane Register.
53:56	RWX	RX_PR_PHASE_STEP_COARSE: This field contains the phase step in coarse mode. For more information, see the RX_PR_PHASE_STEP field in the Receive Bit Mode 2 EO Per-Lane Register.
57:58	RWX	RX_PR_COARSE_MODE_TIMER_SEL: This field selects how long to remain in coarse mode. The timer is always reset on an invalid lock. 00 = ~1.3 s. 01 = ~2.6 μs. 10 = ~5.2 μs. 11 = ~10.5 μs.
59:63	RO	constant = 0b00000

Register Name	Receive Bit Mode 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL
Address	8002380109010C3F (SCOM)
Description	This register contains the fourth set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_COARSE_MODE_EN: This bit enables the CDR to switch into coarse mode, as needed, on a CDR stop/start or on an invalid lock (if enabled).
49	RWX	RX_PR_INVALID_LOCK_COARSE_EN: This bit enables the CDR to switch into coarse mode, when enabled, on an invalid lock. It remains in coarse mode until there are no invalid locks, regardless of this bit.
50:52	RWX	RX_PR_FW_INERTIA_AMT_COARSE: This field contains the flywheel inertia in coarse mode. For more information, see the RX_PR_FW_INERTIA_AMT field in the Receive Bit Mode 2 EO Per-Lane Register.
53:56	RWX	RX_PR_PHASE_STEP_COARSE: This field contains the phase step in coarse mode. For more information, see the RX_PR_PHASE_STEP field in the Receive Bit Mode 2 EO Per-Lane Register.
57:58	RWX	RX_PR_COARSE_MODE_TIMER_SEL: This field selects how long to remain in coarse mode. The timer is always reset on an invalid lock. 00 = ~1.3 µs. 01 = ~2.6 µs. 10 = ~5.2 µs. 11 = ~10.5 µs.
59:63	RO	constant = 0b00000

Register Name	Receive Bit Mode 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL
Address	8002380209010C3F (SCOM)
Description	This register contains the fourth set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_COARSE_MODE_EN: This bit enables the CDR to switch into coarse mode, as needed, on a CDR stop/start or on an invalid lock (if enabled).
49	RWX	RX_PR_INVALID_LOCK_COARSE_EN: This bit enables the CDR to switch into coarse mode, when enabled, on an invalid lock. It remains in coarse mode until there are no invalid locks, regardless of this bit.
50:52	RWX	RX_PR_FW_INERTIA_AMT_COARSE: This field contains the flywheel inertia in coarse mode. For more information, see the RX_PR_FW_INERTIA_AMT field in the Receive Bit Mode 2 EO Per-Lane Register.
53:56	RWX	RX_PR_PHASE_STEP_COARSE: This field contains the phase step in coarse mode. For more information, see the RX_PR_PHASE_STEP field in the Receive Bit Mode 2 EO Per-Lane Register.
57:58	RWX	RX_PR_COARSE_MODE_TIMER_SEL: This field selects how long to remain in coarse mode. The timer is always reset on an invalid lock. 00 = ~1.3 µs. 01 = ~2.6 µs. 10 = ~5.2 µs. 11 = ~10.5 µs.
59:63	RO	constant = 0b00000

Register Name	Receive Bit Mode 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL
Address	8002380309010C3F (SCOM)
Description	This register contains the fourth set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_COARSE_MODE_EN: This bit enables the CDR to switch into coarse mode, as needed, on a CDR stop/start or on an invalid lock (if enabled).
49	RWX	RX_PR_INVALID_LOCK_COARSE_EN: This bit enables the CDR to switch into coarse mode, when enabled, on an invalid lock. It remains in coarse mode until there are no invalid locks, regardless of this bit.
50:52	RWX	RX_PR_FW_INERTIA_AMT_COARSE: This field contains the flywheel inertia in coarse mode. For more information, see the RX_PR_FW_INERTIA_AMT field in the Receive Bit Mode 2 EO Per-Lane Register.
53:56	RWX	RX_PR_PHASE_STEP_COARSE: This field contains the phase step in coarse mode. For more information, see the RX_PR_PHASE_STEP field in the Receive Bit Mode 2 EO Per-Lane Register.
57:58	RWX	RX_PR_COARSE_MODE_TIMER_SEL: This field selects how long to remain in coarse mode. The timer is always reset on an invalid lock. 00 = ~1.3 μs. 01 = ~2.6 μs. 10 = ~5.2 μs. 11 = ~10.5 μs.
59:63	RO	constant = 0b00000

Register Name	Receive Bit Mode 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL
Address	8002380409010C3F (SCOM)
Description	This register contains the fourth set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_COARSE_MODE_EN: This bit enables the CDR to switch into coarse mode, as needed, on a CDR stop/start or on an invalid lock (if enabled).
49	RWX	RX_PR_INVALID_LOCK_COARSE_EN: This bit enables the CDR to switch into coarse mode, when enabled, on an invalid lock. It remains in coarse mode until there are no invalid locks, regardless of this bit.
50:52	RWX	RX_PR_FW_INERTIA_AMT_COARSE: This field contains the flywheel inertia in coarse mode. For more information, see the RX_PR_FW_INERTIA_AMT field in the Receive Bit Mode 2 EO Per-Lane Register.
53:56	RWX	RX_PR_PHASE_STEP_COARSE: This field contains the phase step in coarse mode. For more information, see the RX_PR_PHASE_STEP field in the Receive Bit Mode 2 EO Per-Lane Register.
57:58	RWX	RX_PR_COARSE_MODE_TIMER_SEL: This field selects how long to remain in coarse mode. The timer is always reset on an invalid lock. 00 = ~1.3 μs. 01 = ~2.6 μs. 10 = ~5.2 μs. 11 = ~10.5 μs.
59:63	RO	constant = 0b00000

Register Name	Receive Bit Mode 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL
Address	8002380509010C3F (SCOM)
Description	This register contains the fourth set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_COARSE_MODE_EN: This bit enables the CDR to switch into coarse mode, as needed, on a CDR stop/start or on an invalid lock (if enabled).
49	RWX	RX_PR_INVALID_LOCK_COARSE_EN: This bit enables the CDR to switch into coarse mode, when enabled, on an invalid lock. It remains in coarse mode until there are no invalid locks, regardless of this bit.
50:52	RWX	RX_PR_FW_INERTIA_AMT_COARSE: This field contains the flywheel inertia in coarse mode. For more information, see the RX_PR_FW_INERTIA_AMT field in the Receive Bit Mode 2 EO Per-Lane Register.
53:56	RWX	RX_PR_PHASE_STEP_COARSE: This field contains the phase step in coarse mode. For more information, see the RX_PR_PHASE_STEP field in the Receive Bit Mode 2 EO Per-Lane Register.
57:58	RWX	RX_PR_COARSE_MODE_TIMER_SEL: This field selects how long to remain in coarse mode. The timer is always reset on an invalid lock. 00 = ~1.3 μs. 01 = ~2.6 μs. 10 = ~5.2 μs. 11 = ~10.5 μs.
59:63	RO	constant = 0b00000

Register Name	Receive Bit Mode 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL
Address	8002380609010C3F (SCOM)
Description	This register contains the fourth set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_COARSE_MODE_EN: This bit enables the CDR to switch into coarse mode, as needed, on a CDR stop/start or on an invalid lock (if enabled).
49	RWX	RX_PR_INVALID_LOCK_COARSE_EN: This bit enables the CDR to switch into coarse mode, when enabled, on an invalid lock. It remains in coarse mode until there are no invalid locks, regardless of this bit.
50:52	RWX	RX_PR_FW_INERTIA_AMT_COARSE: This field contains the flywheel inertia in coarse mode. For more information, see the RX_PR_FW_INERTIA_AMT field in the Receive Bit Mode 2 EO Per-Lane Register.
53:56	RWX	RX_PR_PHASE_STEP_COARSE: This field contains the phase step in coarse mode. For more information, see the RX_PR_PHASE_STEP field in the Receive Bit Mode 2 EO Per-Lane Register.
57:58	RWX	RX_PR_COARSE_MODE_TIMER_SEL: This field selects how long to remain in coarse mode. The timer is always reset on an invalid lock. 00 = ~1.3 μs. 01 = ~2.6 μs. 10 = ~5.2 μs. 11 = ~10.5 μs.
59:63	RO	constant = 0b00000

Register Name	Receive Bit Mode 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL
Address	8002380709010C3F (SCOM)
Description	This register contains the fourth set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_COARSE_MODE_EN: This bit enables the CDR to switch into coarse mode, as needed, on a CDR stop/start or on an invalid lock (if enabled).
49	RWX	RX_PR_INVALID_LOCK_COARSE_EN: This bit enables the CDR to switch into coarse mode, when enabled, on an invalid lock. It remains in coarse mode until there are no invalid locks, regardless of this bit.
50:52	RWX	RX_PR_FW_INERTIA_AMT_COARSE: This field contains the flywheel inertia in coarse mode. For more information, see the RX_PR_FW_INERTIA_AMT field in the Receive Bit Mode 2 EO Per-Lane Register.
53:56	RWX	RX_PR_PHASE_STEP_COARSE: This field contains the phase step in coarse mode. For more information, see the RX_PR_PHASE_STEP field in the Receive Bit Mode 2 EO Per-Lane Register.
57:58	RWX	RX_PR_COARSE_MODE_TIMER_SEL: This field selects how long to remain in coarse mode. The timer is always reset on an invalid lock. 00 = ~1.3 μs. 01 = ~2.6 μs. 10 = ~5.2 μs. 11 = ~10.5 μs.
59:63	RO	constant = 0b00000

Register Name	Receive Bit Mode 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL
Address	8002380809010C3F (SCOM)
Description	This register contains the fourth set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_COARSE_MODE_EN: This bit enables the CDR to switch into coarse mode, as needed, on a CDR stop/start or on an invalid lock (if enabled).
49	RWX	RX_PR_INVALID_LOCK_COARSE_EN: This bit enables the CDR to switch into coarse mode, when enabled, on an invalid lock. It remains in coarse mode until there are no invalid locks, regardless of this bit.
50:52	RWX	RX_PR_FW_INERTIA_AMT_COARSE: This field contains the flywheel inertia in coarse mode. For more information, see the RX_PR_FW_INERTIA_AMT field in the Receive Bit Mode 2 EO Per-Lane Register.
53:56	RWX	RX_PR_PHASE_STEP_COARSE: This field contains the phase step in coarse mode. For more information, see the RX_PR_PHASE_STEP field in the Receive Bit Mode 2 EO Per-Lane Register.
57:58	RWX	RX_PR_COARSE_MODE_TIMER_SEL: This field selects how long to remain in coarse mode. The timer is always reset on an invalid lock. 00 = ~1.3 μs. 01 = ~2.6 μs. 10 = ~5.2 μs. 11 = ~10.5 μs.
59:63	RO	constant = 0b00000

Register Name	Receive Bit Mode 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL
Address	8002380909010C3F (SCOM)
Description	This register contains the fourth set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_COARSE_MODE_EN: This bit enables the CDR to switch into coarse mode, as needed, on a CDR stop/start or on an invalid lock (if enabled).
49	RWX	RX_PR_INVALID_LOCK_COARSE_EN: This bit enables the CDR to switch into coarse mode, when enabled, on an invalid lock. It remains in coarse mode until there are no invalid locks, regardless of this bit.
50:52	RWX	RX_PR_FW_INERTIA_AMT_COARSE: This field contains the flywheel inertia in coarse mode. For more information, see the RX_PR_FW_INERTIA_AMT field in the Receive Bit Mode 2 EO Per-Lane Register.
53:56	RWX	RX_PR_PHASE_STEP_COARSE: This field contains the phase step in coarse mode. For more information, see the RX_PR_PHASE_STEP field in the Receive Bit Mode 2 EO Per-Lane Register.
57:58	RWX	RX_PR_COARSE_MODE_TIMER_SEL: This field selects how long to remain in coarse mode. The timer is always reset on an invalid lock. 00 = ~1.3 μs. 01 = ~2.6 μs. 10 = ~5.2 μs. 11 = ~10.5 μs.
59:63	RO	constant = 0b00000

Register Name	Receive Bit Mode 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL
Address	8002380A09010C3F (SCOM)
Description	This register contains the fourth set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_COARSE_MODE_EN: This bit enables the CDR to switch into coarse mode, as needed, on a CDR stop/start or on an invalid lock (if enabled).
49	RWX	RX_PR_INVALID_LOCK_COARSE_EN: This bit enables the CDR to switch into coarse mode, when enabled, on an invalid lock. It remains in coarse mode until there are no invalid locks, regardless of this bit.
50:52	RWX	RX_PR_FW_INERTIA_AMT_COARSE: This field contains the flywheel inertia in coarse mode. For more information, see the RX_PR_FW_INERTIA_AMT field in the Receive Bit Mode 2 EO Per-Lane Register.
53:56	RWX	RX_PR_PHASE_STEP_COARSE: This field contains the phase step in coarse mode. For more information, see the RX_PR_PHASE_STEP field in the Receive Bit Mode 2 EO Per-Lane Register.
57:58	RWX	RX_PR_COARSE_MODE_TIMER_SEL: This field selects how long to remain in coarse mode. The timer is always reset on an invalid lock. 00 = ~1.3 μs. 01 = ~2.6 μs. 10 = ~5.2 μs. 11 = ~10.5 μs.
59:63	RO	constant = 0b00000

Register Name	Receive Bit Mode 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL
Address	8002380B09010C3F (SCOM)
Description	This register contains the fourth set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_COARSE_MODE_EN: This bit enables the CDR to switch into coarse mode, as needed, on a CDR stop/start or on an invalid lock (if enabled).
49	RWX	RX_PR_INVALID_LOCK_COARSE_EN: This bit enables the CDR to switch into coarse mode, when enabled, on an invalid lock. It remains in coarse mode until there are no invalid locks, regardless of this bit.
50:52	RWX	RX_PR_FW_INERTIA_AMT_COARSE: This field contains the flywheel inertia in coarse mode. For more information, see the RX_PR_FW_INERTIA_AMT field in the Receive Bit Mode 2 EO Per-Lane Register.
53:56	RWX	RX_PR_PHASE_STEP_COARSE: This field contains the phase step in coarse mode. For more information, see the RX_PR_PHASE_STEP field in the Receive Bit Mode 2 EO Per-Lane Register.
57:58	RWX	RX_PR_COARSE_MODE_TIMER_SEL: This field selects how long to remain in coarse mode. The timer is always reset on an invalid lock. 00 = ~1.3 μs. 01 = ~2.6 μs. 10 = ~5.2 μs. 11 = ~10.5 μs.
59:63	RO	constant = 0b00000

Register Name	Receive Bit Mode 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL
Address	8002380C09010C3F (SCOM)
Description	This register contains the fourth set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_COARSE_MODE_EN: This bit enables the CDR to switch into coarse mode, as needed, on a CDR stop/start or on an invalid lock (if enabled).
49	RWX	RX_PR_INVALID_LOCK_COARSE_EN: This bit enables the CDR to switch into coarse mode, when enabled, on an invalid lock. It remains in coarse mode until there are no invalid locks, regardless of this bit.
50:52	RWX	RX_PR_FW_INERTIA_AMT_COARSE: This field contains the flywheel inertia in coarse mode. For more information, see the RX_PR_FW_INERTIA_AMT field in the Receive Bit Mode 2 EO Per-Lane Register.
53:56	RWX	RX_PR_PHASE_STEP_COARSE: This field contains the phase step in coarse mode. For more information, see the RX_PR_PHASE_STEP field in the Receive Bit Mode 2 EO Per-Lane Register.
57:58	RWX	RX_PR_COARSE_MODE_TIMER_SEL: This field selects how long to remain in coarse mode. The timer is always reset on an invalid lock. 00 = ~1.3 μs. 01 = ~2.6 μs. 10 = ~5.2 μs. 11 = ~10.5 μs.
59:63	RO	constant = 0b00000

Register Name	Receive Bit Mode 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL
Address	8002380D09010C3F (SCOM)
Description	This register contains the fourth set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_COARSE_MODE_EN: This bit enables the CDR to switch into coarse mode, as needed, on a CDR stop/start or on an invalid lock (if enabled).
49	RWX	RX_PR_INVALID_LOCK_COARSE_EN: This bit enables the CDR to switch into coarse mode, when enabled, on an invalid lock. It remains in coarse mode until there are no invalid locks, regardless of this bit.
50:52	RWX	RX_PR_FW_INERTIA_AMT_COARSE: This field contains the flywheel inertia in coarse mode. For more information, see the RX_PR_FW_INERTIA_AMT field in the Receive Bit Mode 2 EO Per-Lane Register.
53:56	RWX	RX_PR_PHASE_STEP_COARSE: This field contains the phase step in coarse mode. For more information, see the RX_PR_PHASE_STEP field in the Receive Bit Mode 2 EO Per-Lane Register.
57:58	RWX	RX_PR_COARSE_MODE_TIMER_SEL: This field selects how long to remain in coarse mode. The timer is always reset on an invalid lock. 00 = ~1.3 μs. 01 = ~2.6 μs. 10 = ~5.2 μs. 11 = ~10.5 μs.
59:63	RO	constant = 0b00000

Register Name	Receive Bit Mode 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL
Address	8002380E09010C3F (SCOM)
Description	This register contains the fourth set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_COARSE_MODE_EN: This bit enables the CDR to switch into coarse mode, as needed, on a CDR stop/start or on an invalid lock (if enabled).
49	RWX	RX_PR_INVALID_LOCK_COARSE_EN: This bit enables the CDR to switch into coarse mode, when enabled, on an invalid lock. It remains in coarse mode until there are no invalid locks, regardless of this bit.
50:52	RWX	RX_PR_FW_INERTIA_AMT_COARSE: This field contains the flywheel inertia in coarse mode. For more information, see the RX_PR_FW_INERTIA_AMT field in the Receive Bit Mode 2 EO Per-Lane Register.
53:56	RWX	RX_PR_PHASE_STEP_COARSE: This field contains the phase step in coarse mode. For more information, see the RX_PR_PHASE_STEP field in the Receive Bit Mode 2 EO Per-Lane Register.
57:58	RWX	RX_PR_COARSE_MODE_TIMER_SEL: This field selects how long to remain in coarse mode. The timer is always reset on an invalid lock. 00 = ~1.3 μs. 01 = ~2.6 μs. 10 = ~5.2 μs. 11 = ~10.5 μs.
59:63	RO	constant = 0b00000

Register Name	Receive Bit Mode 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL
Address	8002380F09010C3F (SCOM)
Description	This register contains the fourth set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_COARSE_MODE_EN: This bit enables the CDR to switch into coarse mode, as needed, on a CDR stop/start or on an invalid lock (if enabled).
49	RWX	RX_PR_INVALID_LOCK_COARSE_EN: This bit enables the CDR to switch into coarse mode, when enabled, on an invalid lock. It remains in coarse mode until there are no invalid locks, regardless of this bit.
50:52	RWX	RX_PR_FW_INERTIA_AMT_COARSE: This field contains the flywheel inertia in coarse mode. For more information, see the RX_PR_FW_INERTIA_AMT field in the Receive Bit Mode 2 EO Per-Lane Register.
53:56	RWX	RX_PR_PHASE_STEP_COARSE: This field contains the phase step in coarse mode. For more information, see the RX_PR_PHASE_STEP field in the Receive Bit Mode 2 EO Per-Lane Register.
57:58	RWX	RX_PR_COARSE_MODE_TIMER_SEL: This field selects how long to remain in coarse mode. The timer is always reset on an invalid lock. 00 = ~1.3 μs. 01 = ~2.6 μs. 10 = ~5.2 μs. 11 = ~10.5 μs.
59:63	RO	constant = 0b00000

Register Name	Receive Bit Mode 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL
Address	8002381009010C3F (SCOM)
Description	This register contains the fourth set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_COARSE_MODE_EN: This bit enables the CDR to switch into coarse mode, as needed, on a CDR stop/start or on an invalid lock (if enabled).
49	RWX	RX_PR_INVALID_LOCK_COARSE_EN: This bit enables the CDR to switch into coarse mode, when enabled, on an invalid lock. It remains in coarse mode until there are no invalid locks, regardless of this bit.
50:52	RWX	RX_PR_FW_INERTIA_AMT_COARSE: This field contains the flywheel inertia in coarse mode. For more information, see the RX_PR_FW_INERTIA_AMT field in the Receive Bit Mode 2 EO Per-Lane Register.
53:56	RWX	RX_PR_PHASE_STEP_COARSE: This field contains the phase step in coarse mode. For more information, see the RX_PR_PHASE_STEP field in the Receive Bit Mode 2 EO Per-Lane Register.
57:58	RWX	RX_PR_COARSE_MODE_TIMER_SEL: This field selects how long to remain in coarse mode. The timer is always reset on an invalid lock. 00 = ~1.3 μs. 01 = ~2.6 μs. 10 = ~5.2 μs. 11 = ~10.5 μs.
59:63	RO	constant = 0b00000

Register Name	Receive Bit Mode 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL
Address	8002381109010C3F (SCOM)
Description	This register contains the fourth set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_COARSE_MODE_EN: This bit enables the CDR to switch into coarse mode, as needed, on a CDR stop/start or on an invalid lock (if enabled).
49	RWX	RX_PR_INVALID_LOCK_COARSE_EN: This bit enables the CDR to switch into coarse mode, when enabled, on an invalid lock. It remains in coarse mode until there are no invalid locks, regardless of this bit.
50:52	RWX	RX_PR_FW_INERTIA_AMT_COARSE: This field contains the flywheel inertia in coarse mode. For more information, see the RX_PR_FW_INERTIA_AMT field in the Receive Bit Mode 2 EO Per-Lane Register.
53:56	RWX	RX_PR_PHASE_STEP_COARSE: This field contains the phase step in coarse mode. For more information, see the RX_PR_PHASE_STEP field in the Receive Bit Mode 2 EO Per-Lane Register.
57:58	RWX	RX_PR_COARSE_MODE_TIMER_SEL: This field selects how long to remain in coarse mode. The timer is always reset on an invalid lock. 00 = ~1.3 µs. 01 = ~2.6 µs. 10 = ~5.2 µs. 11 = ~10.5 µs.
59:63	RO	constant = 0b00000

Register Name	Receive Bit Mode 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL
Address	8002381209010C3F (SCOM)
Description	This register contains the fourth set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_COARSE_MODE_EN: This bit enables the CDR to switch into coarse mode, as needed, on a CDR stop/start or on an invalid lock (if enabled).
49	RWX	RX_PR_INVALID_LOCK_COARSE_EN: This bit enables the CDR to switch into coarse mode, when enabled, on an invalid lock. It remains in coarse mode until there are no invalid locks, regardless of this bit.
50:52	RWX	RX_PR_FW_INERTIA_AMT_COARSE: This field contains the flywheel inertia in coarse mode. For more information, see the RX_PR_FW_INERTIA_AMT field in the Receive Bit Mode 2 EO Per-Lane Register.
53:56	RWX	RX_PR_PHASE_STEP_COARSE: This field contains the phase step in coarse mode. For more information, see the RX_PR_PHASE_STEP field in the Receive Bit Mode 2 EO Per-Lane Register.
57:58	RWX	RX_PR_COARSE_MODE_TIMER_SEL: This field selects how long to remain in coarse mode. The timer is always reset on an invalid lock. 00 = ~1.3 µs. 01 = ~2.6 µs. 10 = ~5.2 µs. 11 = ~10.5 µs.
59:63	RO	constant = 0b00000

Register Name	Receive Bit Mode 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL
Address	8002381309010C3F (SCOM)
Description	This register contains the fourth set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_COARSE_MODE_EN: This bit enables the CDR to switch into coarse mode, as needed, on a CDR stop/start or on an invalid lock (if enabled).
49	RWX	RX_PR_INVALID_LOCK_COARSE_EN: This bit enables the CDR to switch into coarse mode, when enabled, on an invalid lock. It remains in coarse mode until there are no invalid locks, regardless of this bit.
50:52	RWX	RX_PR_FW_INERTIA_AMT_COARSE: This field contains the flywheel inertia in coarse mode. For more information, see the RX_PR_FW_INERTIA_AMT field in the Receive Bit Mode 2 EO Per-Lane Register.
53:56	RWX	RX_PR_PHASE_STEP_COARSE: This field contains the phase step in coarse mode. For more information, see the RX_PR_PHASE_STEP field in the Receive Bit Mode 2 EO Per-Lane Register.
57:58	RWX	RX_PR_COARSE_MODE_TIMER_SEL: This field selects how long to remain in coarse mode. The timer is always reset on an invalid lock. 00 = ~1.3 μs. 01 = ~2.6 μs. 10 = ~5.2 μs. 11 = ~10.5 μs.
59:63	RO	constant = 0b00000

Register Name	Receive Bit Mode 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL
Address	8002381409010C3F (SCOM)
Description	This register contains the fourth set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_COARSE_MODE_EN: This bit enables the CDR to switch into coarse mode, as needed, on a CDR stop/start or on an invalid lock (if enabled).
49	RWX	RX_PR_INVALID_LOCK_COARSE_EN: This bit enables the CDR to switch into coarse mode, when enabled, on an invalid lock. It remains in coarse mode until there are no invalid locks, regardless of this bit.
50:52	RWX	RX_PR_FW_INERTIA_AMT_COARSE: This field contains the flywheel inertia in coarse mode. For more information, see the RX_PR_FW_INERTIA_AMT field in the Receive Bit Mode 2 EO Per-Lane Register.
53:56	RWX	RX_PR_PHASE_STEP_COARSE: This field contains the phase step in coarse mode. For more information, see the RX_PR_PHASE_STEP field in the Receive Bit Mode 2 EO Per-Lane Register.
57:58	RWX	RX_PR_COARSE_MODE_TIMER_SEL: This field selects how long to remain in coarse mode. The timer is always reset on an invalid lock. 00 = ~1.3 μs. 01 = ~2.6 μs. 10 = ~5.2 μs. 11 = ~10.5 μs.
59:63	RO	constant = 0b00000

Register Name	Receive Bit Mode 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL
Address	8002381509010C3F (SCOM)
Description	This register contains the fourth set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_COARSE_MODE_EN: This bit enables the CDR to switch into coarse mode, as needed, on a CDR stop/start or on an invalid lock (if enabled).
49	RWX	RX_PR_INVALID_LOCK_COARSE_EN: This bit enables the CDR to switch into coarse mode, when enabled, on an invalid lock. It remains in coarse mode until there are no invalid locks, regardless of this bit.
50:52	RWX	RX_PR_FW_INERTIA_AMT_COARSE: This field contains the flywheel inertia in coarse mode. For more information, see the RX_PR_FW_INERTIA_AMT field in the Receive Bit Mode 2 EO Per-Lane Register.
53:56	RWX	RX_PR_PHASE_STEP_COARSE: This field contains the phase step in coarse mode. For more information, see the RX_PR_PHASE_STEP field in the Receive Bit Mode 2 EO Per-Lane Register.
57:58	RWX	RX_PR_COARSE_MODE_TIMER_SEL: This field selects how long to remain in coarse mode. The timer is always reset on an invalid lock. 00 = ~1.3 μs. 01 = ~2.6 μs. 10 = ~5.2 μs. 11 = ~10.5 μs.
59:63	RO	constant = 0b00000

Register Name	Receive Bit Mode 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL
Address	8002381609010C3F (SCOM)
Description	This register contains the fourth set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_COARSE_MODE_EN: This bit enables the CDR to switch into coarse mode, as needed, on a CDR stop/start or on an invalid lock (if enabled).
49	RWX	RX_PR_INVALID_LOCK_COARSE_EN: This bit enables the CDR to switch into coarse mode, when enabled, on an invalid lock. It remains in coarse mode until there are no invalid locks, regardless of this bit.
50:52	RWX	RX_PR_FW_INERTIA_AMT_COARSE: This field contains the flywheel inertia in coarse mode. For more information, see the RX_PR_FW_INERTIA_AMT field in the Receive Bit Mode 2 EO Per-Lane Register.
53:56	RWX	RX_PR_PHASE_STEP_COARSE: This field contains the phase step in coarse mode. For more information, see the RX_PR_PHASE_STEP field in the Receive Bit Mode 2 EO Per-Lane Register.
57:58	RWX	RX_PR_COARSE_MODE_TIMER_SEL: This field selects how long to remain in coarse mode. The timer is always reset on an invalid lock. 00 = ~1.3 μs. 01 = ~2.6 μs. 10 = ~5.2 μs. 11 = ~10.5 μs.
59:63	RO	constant = 0b00000

Register Name	Receive Bit Mode 4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_MODE4_EO_PL
Address	8002381709010C3F (SCOM)
Description	This register contains the fourth set of EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_COARSE_MODE_EN: This bit enables the CDR to switch into coarse mode, as needed, on a CDR stop/start or on an invalid lock (if enabled).
49	RWX	RX_PR_INVALID_LOCK_COARSE_EN: This bit enables the CDR to switch into coarse mode, when enabled, on an invalid lock. It remains in coarse mode until there are no invalid locks, regardless of this bit.
50:52	RWX	RX_PR_FW_INERTIA_AMT_COARSE: This field contains the flywheel inertia in coarse mode. For more information, see the RX_PR_FW_INERTIA_AMT field in the Receive Bit Mode 2 EO Per-Lane Register.
53:56	RWX	RX_PR_PHASE_STEP_COARSE: This field contains the phase step in coarse mode. For more information, see the RX_PR_PHASE_STEP field in the Receive Bit Mode 2 EO Per-Lane Register.
57:58	RWX	RX_PR_COARSE_MODE_TIMER_SEL: This field selects how long to remain in coarse mode. The timer is always reset on an invalid lock. 00 = ~1.3 μs. 01 = ~2.6 μs. 10 = ~5.2 μs. 11 = ~10.5 μs.
59:63	RO	constant = 0b00000

Register Name	Receive Bit CNTLX1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	8002400009010C3F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49:50	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic.
51	RWX	RX_BANK_SEL_A: This field selects which data bank to select for main data samples and alt data samples. 0b0 = Data bank B is selected for main data, and data bank A is selected for alt data. 0b1 = Data bank A is selected for main data, and data bank B is selected for alt data.
52	RWX	RX_PIPE_MARGIN: This field adds extra cycles of padding on the asynchronous data pipe handshake.
53:54	RWX	RX_SCOPE_MODE: This field adds extra cycles in the asynchronous crossing for scope mode.
55:56	RO	constant = 0b00
57	RWX	RX_BIST_PIPE_DATA_SHIFT: This field selects what to mux onto the data pipe bus going to the rx_bist engine to get the upper-order lanes on the edge and alt only.
58:63	RO	constant = 0b000000

Register Name	Receive Bit CNTLX1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	8002400109010C3F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49:50	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic.
51	RWX	RX_BANK_SEL_A: This field selects which data bank to select for main data samples and alt data samples. 0b0 = Data bank B is selected for main data, and data bank A is selected for alt data. 0b1 = Data bank A is selected for main data, and data bank B is selected for alt data.
52	RWX	RX_PIPE_MARGIN: This field adds extra cycles of padding on the asynchronous data pipe handshake.
53:54	RWX	RX_SCOPE_MODE: This field adds extra cycles in the asynchronous crossing for scope mode.
55:56	RO	constant = 0b00
57	RWX	RX_BIST_PIPE_DATA_SHIFT: This field selects what to mux onto the data pipe bus going to the rx_bist engine to get the upper-order lanes on the edge and alt only.
58:63	RO	constant = 0b000000

Register Name	Receive Bit CNTLX1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	8002400209010C3F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49:50	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic.
51	RWX	RX_BANK_SEL_A: This field selects which data bank to select for main data samples and alt data samples. 0b0 = Data bank B is selected for main data, and data bank A is selected for alt data. 0b1 = Data bank A is selected for main data, and data bank B is selected for alt data.
52	RWX	RX_PIPE_MARGIN: This field adds extra cycles of padding on the asynchronous data pipe handshake.
53:54	RWX	RX_SCOPE_MODE: This field adds extra cycles in the asynchronous crossing for scope mode.
55:56	RO	constant = 0b00
57	RWX	RX_BIST_PIPE_DATA_SHIFT: This field selects what to mux onto the data pipe bus going to the rx_bist engine to get the upper-order lanes on the edge and alt only.
58:63	RO	constant = 0b000000

Register Name	Receive Bit CNTLX1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	8002400309010C3F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49:50	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic.
51	RWX	RX_BANK_SEL_A: This field selects which data bank to select for main data samples and alt data samples. 0b0 = Data bank B is selected for main data, and data bank A is selected for alt data. 0b1 = Data bank A is selected for main data, and data bank B is selected for alt data.
52	RWX	RX_PIPE_MARGIN: This field adds extra cycles of padding on the asynchronous data pipe handshake.
53:54	RWX	RX_SCOPE_MODE: This field adds extra cycles in the asynchronous crossing for scope mode.
55:56	RO	constant = 0b00
57	RWX	RX_BIST_PIPE_DATA_SHIFT: This field selects what to mux onto the data pipe bus going to the rx_bist engine to get the upper-order lanes on the edge and alt only.
58:63	RO	constant = 0b000000

Register Name	Receive Bit CNTLX1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	8002400409010C3F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49:50	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic.
51	RWX	RX_BANK_SEL_A: This field selects which data bank to select for main data samples and alt data samples. 0b0 = Data bank B is selected for main data, and data bank A is selected for alt data. 0b1 = Data bank A is selected for main data, and data bank B is selected for alt data.
52	RWX	RX_PIPE_MARGIN: This field adds extra cycles of padding on the asynchronous data pipe handshake.
53:54	RWX	RX_SCOPE_MODE: This field adds extra cycles in the asynchronous crossing for scope mode.
55:56	RO	constant = 0b00
57	RWX	RX_BIST_PIPE_DATA_SHIFT: This field selects what to mux onto the data pipe bus going to the rx_bist engine to get the upper-order lanes on the edge and alt only.
58:63	RO	constant = 0b000000

Register Name	**Receive Bit CNTLX1 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	8002400509010C3F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49:50	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic.
51	RWX	RX_BANK_SEL_A: This field selects which data bank to select for main data samples and alt data samples. 0b0 = Data bank B is selected for main data, and data bank A is selected for alt data. 0b1 = Data bank A is selected for main data, and data bank B is selected for alt data.
52	RWX	RX_PIPE_MARGIN: This field adds extra cycles of padding on the asynchronous data pipe handshake.
53:54	RWX	RX_SCOPE_MODE: This field adds extra cycles in the asynchronous crossing for scope mode.
55:56	RO	constant = 0b00
57	RWX	RX_BIST_PIPE_DATA_SHIFT: This field selects what to mux onto the data pipe bus going to the rx_bist engine to get the upper-order lanes on the edge and alt only.
58:63	RO	constant = 0b000000

Register Name	**Receive Bit CNTLX1 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	8002400609010C3F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49:50	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic.
51	RWX	RX_BANK_SEL_A: This field selects which data bank to select for main data samples and alt data samples. 0b0 = Data bank B is selected for main data, and data bank A is selected for alt data. 0b1 = Data bank A is selected for main data, and data bank B is selected for alt data.
52	RWX	RX_PIPE_MARGIN: This field adds extra cycles of padding on the asynchronous data pipe handshake.
53:54	RWX	RX_SCOPE_MODE: This field adds extra cycles in the asynchronous crossing for scope mode.
55:56	RO	constant = 0b00
57	RWX	RX_BIST_PIPE_DATA_SHIFT: This field selects what to mux onto the data pipe bus going to the rx_bist engine to get the upper-order lanes on the edge and alt only.
58:63	RO	constant = 0b000000

Register Name	Receive Bit CNTLX1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	8002400709010C3F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49:50	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic.
51	RWX	RX_BANK_SEL_A: This field selects which data bank to select for main data samples and alt data samples. 0b0 = Data bank B is selected for main data, and data bank A is selected for alt data. 0b1 = Data bank A is selected for main data, and data bank B is selected for alt data.
52	RWX	RX_PIPE_MARGIN: This field adds extra cycles of padding on the asynchronous data pipe handshake.
53:54	RWX	RX_SCOPE_MODE: This field adds extra cycles in the asynchronous crossing for scope mode.
55:56	RO	constant = 0b00
57	RWX	RX_BIST_PIPE_DATA_SHIFT: This field selects what to mux onto the data pipe bus going to the rx_bist engine to get the upper-order lanes on the edge and alt only.
58:63	RO	constant = 0b000000

Register Name	Receive Bit CNTLX1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	8002400809010C3F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49:50	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic.
51	RWX	RX_BANK_SEL_A: This field selects which data bank to select for main data samples and alt data samples. 0b0 = Data bank B is selected for main data, and data bank A is selected for alt data. 0b1 = Data bank A is selected for main data, and data bank B is selected for alt data.
52	RWX	RX_PIPE_MARGIN: This field adds extra cycles of padding on the asynchronous data pipe handshake.
53:54	RWX	RX_SCOPE_MODE: This field adds extra cycles in the asynchronous crossing for scope mode.
55:56	RO	constant = 0b00
57	RWX	RX_BIST_PIPE_DATA_SHIFT: This field selects what to mux onto the data pipe bus going to the rx_bist engine to get the upper-order lanes on the edge and alt only.
58:63	RO	constant = 0b000000

Register Name	**Receive Bit CNTLX1 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	8002400909010C3F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49:50	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic.
51	RWX	RX_BANK_SEL_A: This field selects which data bank to select for main data samples and alt data samples. 0b0 = Data bank B is selected for main data, and data bank A is selected for alt data. 0b1 = Data bank A is selected for main data, and data bank B is selected for alt data.
52	RWX	RX_PIPE_MARGIN: This field adds extra cycles of padding on the asynchronous data pipe handshake.
53:54	RWX	RX_SCOPE_MODE: This field adds extra cycles in the asynchronous crossing for scope mode.
55:56	RO	constant = 0b00
57	RWX	RX_BIST_PIPE_DATA_SHIFT: This field selects what to mux onto the data pipe bus going to the rx_bist engine to get the upper-order lanes on the edge and alt only.
58:63	RO	constant = 0b000000

Register Name	**Receive Bit CNTLX1 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	8002400A09010C3F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49:50	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic.
51	RWX	RX_BANK_SEL_A: This field selects which data bank to select for main data samples and alt data samples. 0b0 = Data bank B is selected for main data, and data bank A is selected for alt data. 0b1 = Data bank A is selected for main data, and data bank B is selected for alt data.
52	RWX	RX_PIPE_MARGIN: This field adds extra cycles of padding on the asynchronous data pipe handshake.
53:54	RWX	RX_SCOPE_MODE: This field adds extra cycles in the asynchronous crossing for scope mode.
55:56	RO	constant = 0b00
57	RWX	RX_BIST_PIPE_DATA_SHIFT: This field selects what to mux onto the data pipe bus going to the rx_bist engine to get the upper-order lanes on the edge and alt only.
58:63	RO	constant = 0b000000

Register Name	Receive Bit CNTLX1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	8002400B09010C3F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49:50	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic.
51	RWX	RX_BANK_SEL_A: This field selects which data bank to select for main data samples and alt data samples. 0b0 = Data bank B is selected for main data, and data bank A is selected for alt data. 0b1 = Data bank A is selected for main data, and data bank B is selected for alt data.
52	RWX	RX_PIPE_MARGIN: This field adds extra cycles of padding on the asynchronous data pipe handshake.
53:54	RWX	RX_SCOPE_MODE: This field adds extra cycles in the asynchronous crossing for scope mode.
55:56	RO	constant = 0b00
57	RWX	RX_BIST_PIPE_DATA_SHIFT: This field selects what to mux onto the data pipe bus going to the rx_bist engine to get the upper-order lanes on the edge and alt only.
58:63	RO	constant = 0b000000

Register Name	Receive Bit CNTLX1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	8002400C09010C3F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49:50	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic.
51	RWX	RX_BANK_SEL_A: This field selects which data bank to select for main data samples and alt data samples. 0b0 = Data bank B is selected for main data, and data bank A is selected for alt data. 0b1 = Data bank A is selected for main data, and data bank B is selected for alt data.
52	RWX	RX_PIPE_MARGIN: This field adds extra cycles of padding on the asynchronous data pipe handshake.
53:54	RWX	RX_SCOPE_MODE: This field adds extra cycles in the asynchronous crossing for scope mode.
55:56	RO	constant = 0b00
57	RWX	RX_BIST_PIPE_DATA_SHIFT: This field selects what to mux onto the data pipe bus going to the rx_bist engine to get the upper-order lanes on the edge and alt only.
58:63	RO	constant = 0b000000

Register Name	Receive Bit CNTLX1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	8002400D09010C3F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49:50	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic.
51	RWX	RX_BANK_SEL_A: This field selects which data bank to select for main data samples and alt data samples. 0b0 = Data bank B is selected for main data, and data bank A is selected for alt data. 0b1 = Data bank A is selected for main data, and data bank B is selected for alt data.
52	RWX	RX_PIPE_MARGIN: This field adds extra cycles of padding on the asynchronous data pipe handshake.
53:54	RWX	RX_SCOPE_MODE: This field adds extra cycles in the asynchronous crossing for scope mode.
55:56	RO	constant = 0b00
57	RWX	RX_BIST_PIPE_DATA_SHIFT: This field selects what to mux onto the data pipe bus going to the rx_bist engine to get the upper-order lanes on the edge and alt only.
58:63	RO	constant = 0b000000

Register Name	Receive Bit CNTLX1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	8002400E09010C3F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49:50	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic.
51	RWX	RX_BANK_SEL_A: This field selects which data bank to select for main data samples and alt data samples. 0b0 = Data bank B is selected for main data, and data bank A is selected for alt data. 0b1 = Data bank A is selected for main data, and data bank B is selected for alt data.
52	RWX	RX_PIPE_MARGIN: This field adds extra cycles of padding on the asynchronous data pipe handshake.
53:54	RWX	RX_SCOPE_MODE: This field adds extra cycles in the asynchronous crossing for scope mode.
55:56	RO	constant = 0b00
57	RWX	RX_BIST_PIPE_DATA_SHIFT: This field selects what to mux onto the data pipe bus going to the rx_bist engine to get the upper-order lanes on the edge and alt only.
58:63	RO	constant = 0b000000

Register Name	Receive Bit CNTLX1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	8002400F09010C3F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49:50	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic.
51	RWX	RX_BANK_SEL_A: This field selects which data bank to select for main data samples and alt data samples. 0b0 = Data bank B is selected for main data, and data bank A is selected for alt data. 0b1 = Data bank A is selected for main data, and data bank B is selected for alt data.
52	RWX	RX_PIPE_MARGIN: This field adds extra cycles of padding on the asynchronous data pipe handshake.
53:54	RWX	RX_SCOPE_MODE: This field adds extra cycles in the asynchronous crossing for scope mode.
55:56	RO	constant = 0b00
57	RWX	RX_BIST_PIPE_DATA_SHIFT: This field selects what to mux onto the data pipe bus going to the rx_bist engine to get the upper-order lanes on the edge and alt only.
58:63	RO	constant = 0b000000

Register Name	Receive Bit CNTLX1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	8002401009010C3F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49:50	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic.
51	RWX	RX_BANK_SEL_A: This field selects which data bank to select for main data samples and alt data samples. 0b0 = Data bank B is selected for main data, and data bank A is selected for alt data. 0b1 = Data bank A is selected for main data, and data bank B is selected for alt data.
52	RWX	RX_PIPE_MARGIN: This field adds extra cycles of padding on the asynchronous data pipe handshake.
53:54	RWX	RX_SCOPE_MODE: This field adds extra cycles in the asynchronous crossing for scope mode.
55:56	RO	constant = 0b00
57	RWX	RX_BIST_PIPE_DATA_SHIFT: This field selects what to mux onto the data pipe bus going to the rx_bist engine to get the upper-order lanes on the edge and alt only.
58:63	RO	constant = 0b000000

Register Name	**Receive Bit CNTLX1 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	8002401109010C3F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49:50	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic.
51	RWX	RX_BANK_SEL_A: This field selects which data bank to select for main data samples and alt data samples. 0b0 = Data bank B is selected for main data, and data bank A is selected for alt data. 0b1 = Data bank A is selected for main data, and data bank B is selected for alt data.
52	RWX	RX_PIPE_MARGIN: This field adds extra cycles of padding on the asynchronous data pipe handshake.
53:54	RWX	RX_SCOPE_MODE: This field adds extra cycles in the asynchronous crossing for scope mode.
55:56	RO	constant = 0b00
57	RWX	RX_BIST_PIPE_DATA_SHIFT: This field selects what to mux onto the data pipe bus going to the rx_bist engine to get the upper-order lanes on the edge and alt only.
58:63	RO	constant = 0b000000

Register Name	**Receive Bit CNTLX1 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	8002401209010C3F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49:50	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic.
51	RWX	RX_BANK_SEL_A: This field selects which data bank to select for main data samples and alt data samples. 0b0 = Data bank B is selected for main data, and data bank A is selected for alt data. 0b1 = Data bank A is selected for main data, and data bank B is selected for alt data.
52	RWX	RX_PIPE_MARGIN: This field adds extra cycles of padding on the asynchronous data pipe handshake.
53:54	RWX	RX_SCOPE_MODE: This field adds extra cycles in the asynchronous crossing for scope mode.
55:56	RO	constant = 0b00
57	RWX	RX_BIST_PIPE_DATA_SHIFT: This field selects what to mux onto the data pipe bus going to the rx_bist engine to get the upper-order lanes on the edge and alt only.
58:63	RO	constant = 0b000000

Register Name	Receive Bit CNTLX1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	8002401309010C3F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49:50	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic.
51	RWX	RX_BANK_SEL_A: This field selects which data bank to select for main data samples and alt data samples. 0b0 = Data bank B is selected for main data, and data bank A is selected for alt data. 0b1 = Data bank A is selected for main data, and data bank B is selected for alt data.
52	RWX	RX_PIPE_MARGIN: This field adds extra cycles of padding on the asynchronous data pipe handshake.
53:54	RWX	RX_SCOPE_MODE: This field adds extra cycles in the asynchronous crossing for scope mode.
55:56	RO	constant = 0b00
57	RWX	RX_BIST_PIPE_DATA_SHIFT: This field selects what to mux onto the data pipe bus going to the rx_bist engine to get the upper-order lanes on the edge and alt only.
58:63	RO	constant = 0b000000

Register Name	Receive Bit CNTLX1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	8002401409010C3F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49:50	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic.
51	RWX	RX_BANK_SEL_A: This field selects which data bank to select for main data samples and alt data samples. 0b0 = Data bank B is selected for main data, and data bank A is selected for alt data. 0b1 = Data bank A is selected for main data, and data bank B is selected for alt data.
52	RWX	RX_PIPE_MARGIN: This field adds extra cycles of padding on the asynchronous data pipe handshake.
53:54	RWX	RX_SCOPE_MODE: This field adds extra cycles in the asynchronous crossing for scope mode.
55:56	RO	constant = 0b00
57	RWX	RX_BIST_PIPE_DATA_SHIFT: This field selects what to mux onto the data pipe bus going to the rx_bist engine to get the upper-order lanes on the edge and alt only.
58:63	RO	constant = 0b000000

Register Name	Receive Bit CNTLX1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	8002401509010C3F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49:50	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic.
51	RWX	RX_BANK_SEL_A: This field selects which data bank to select for main data samples and alt data samples. 0b0 = Data bank B is selected for main data, and data bank A is selected for alt data. 0b1 = Data bank A is selected for main data, and data bank B is selected for alt data.
52	RWX	RX_PIPE_MARGIN: This field adds extra cycles of padding on the asynchronous data pipe handshake.
53:54	RWX	RX_SCOPE_MODE: This field adds extra cycles in the asynchronous crossing for scope mode.
55:56	RO	constant = 0b00
57	RWX	RX_BIST_PIPE_DATA_SHIFT: This field selects what to mux onto the data pipe bus going to the rx_bist engine to get the upper-order lanes on the edge and alt only.
58:63	RO	constant = 0b000000

Register Name	Receive Bit CNTLX1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	8002401609010C3F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49:50	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic.
51	RWX	RX_BANK_SEL_A: This field selects which data bank to select for main data samples and alt data samples. 0b0 = Data bank B is selected for main data, and data bank A is selected for alt data. 0b1 = Data bank A is selected for main data, and data bank B is selected for alt data.
52	RWX	RX_PIPE_MARGIN: This field adds extra cycles of padding on the asynchronous data pipe handshake.
53:54	RWX	RX_SCOPE_MODE: This field adds extra cycles in the asynchronous crossing for scope mode.
55:56	RO	constant = 0b00
57	RWX	RX_BIST_PIPE_DATA_SHIFT: This field selects what to mux onto the data pipe bus going to the rx_bist engine to get the upper-order lanes on the edge and alt only.
58:63	RO	constant = 0b000000

Register Name	Receive Bit CNTLX1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTLX1_EO_PL
Address	8002401709010C3F (SCOM)
Description	This is the receive bit CNTLX1 EO per-lane register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_CAL_LANE_SEL: This bit selects which lane to recalibrate.
49:50	RWX	RX_PIPE_SEL: This bit selects what to multiplex onto the data pipe bus going to the calibration logic.
51	RWX	RX_BANK_SEL_A: This field selects which data bank to select for main data samples and alt data samples. 0b0 = Data bank B is selected for main data, and data bank A is selected for alt data. 0b1 = Data bank A is selected for main data, and data bank B is selected for alt data.
52	RWX	RX_PIPE_MARGIN: This field adds extra cycles of padding on the asynchronous data pipe handshake.
53:54	RWX	RX_SCOPE_MODE: This field adds extra cycles in the asynchronous crossing for scope mode.
55:56	RO	constant = 0b00
57	RWX	RX_BIST_PIPE_DATA_SHIFT: This field selects what to mux onto the data pipe bus going to the rx_bist engine to get the upper-order lanes on the edge and alt only.
58:63	RO	constant = 0b000000

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	8002480009010C3F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51	RWX	RX_PR_WOBBLE_B: This bit wobbles the PR position for PR B for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
52	RWX	RX_PR_WOBBLE_EDGE: This bit wobbles the PR position for the PR edge for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RWX	RX_PR_DDC_B: This bit enables the DDC state machine to go through its DDC routine on PR B. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.

Bits	SCOM	Field Mnemonic: Description
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_EDGE_B: This bit bumps PR B position to the edge. (Not supported).
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported).
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported).
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62	RWX	RX_PR_USE_DFE_CLOCK_B: RX Use the B-bank DFE (h1/Ap-adjusted clock). RJRDMB.
63	RO	constant = 0b0

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	8002480109010C3F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51	RWX	RX_PR_WOBBLE_B: This bit wobbles the PR position for PR B for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
52	RWX	RX_PR_WOBBLE_EDGE: This bit wobbles the PR position for the PR edge for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RWX	RX_PR_DDC_B: This bit enables the DDC state machine to go through its DDC routine on PR B. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_EDGE_B: This bit bumps PR B position to the edge. (Not supported.)
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported.)
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported.)
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.

Bits	SCOM	Field Mnemonic: Description
62	RWX	RX_PR_USE_DFE_CLOCK_B: RX Use the B-bank DFE (h1/Ap-adjusted clock). RJRDMB.
63	RO	constant = 0b0

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	8002480209010C3F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51	RWX	RX_PR_WOBBLE_B: This bit wobbles the PR position for PR B for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
52	RWX	RX_PR_WOBBLE_EDGE: This bit wobbles the PR position for the PR edge for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RWX	RX_PR_DDC_B: This bit enables the DDC state machine to go through its DDC routine on PR B. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_EDGE_B: This bit bumps PR B position to the edge. (Not supported.)
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported.)
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported.)
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62	RWX	RX_PR_USE_DFE_CLOCK_B: RX Use the B-bank DFE (h1/Ap-adjusted clock). RJRDMB.
63	RO	constant = 0b0

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	8002480309010C3F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51	RWX	RX_PR_WOBBLE_B: This bit wobbles the PR position for PR B for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
52	RWX	RX_PR_WOBBLE_EDGE: This bit wobbles the PR position for the PR edge for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RWX	RX_PR_DDC_B: This bit enables the DDC state machine to go through its DDC routine on PR B. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_EDGE_B: This bit bumps PR B position to the edge. (Not supported.)
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported.)
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported.)
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62	RWX	RX_PR_USE_DFE_CLOCK_B: RX Use the B-bank DFE (h1/Ap-adjusted clock). RJRDMB.
63	RO	constant = 0b0

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	8002480409010C3F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51	RWX	RX_PR_WOBBLE_B: This bit wobbles the PR position for PR B for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
52	RWX	RX_PR_WOBBLE_EDGE: This bit wobbles the PR position for the PR edge for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RWX	RX_PR_DDC_B: This bit enables the DDC state machine to go through its DDC routine on PR B. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_EDGE_B: This bit bumps PR B position to the edge. (Not supported.)
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported.)
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported.)
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62	RWX	RX_PR_USE_DFE_CLOCK_B: RX Use the B-bank DFE (h1/Ap-adjusted clock). RJRDMB.
63	RO	constant = 0b0

Register Name	**Receive Bit CNTL2 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	8002480509010C3F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.

Bits	SCOM	Field Mnemonic: Description
51	RWX	RX_PR_WOBBLE_B: This bit wobbles the PR position for PR B for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
52	RWX	RX_PR_WOBBLE_EDGE: This bit wobbles the PR position for the PR edge for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RWX	RX_PR_DDC_B: This bit enables the DDC state machine to go through its DDC routine on PR B. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_EDGE_B: This bit bumps PR B position to the edge. (Not supported.)
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported.)
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported.)
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62	RWX	RX_PR_USE_DFE_CLOCK_B: RX Use the B-bank DFE (h1/Ap-adjusted clock). RJRDMB.
63	RO	constant = 0b0

Register Name	**Receive Bit CNTL2 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	8002480609010C3F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51	RWX	RX_PR_WOBBLE_B: This bit wobbles the PR position for PR B for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
52	RWX	RX_PR_WOBBLE_EDGE: This bit wobbles the PR position for the PR edge for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.

Bits	SCOM	Field Mnemonic: Description
54	RWX	RX_PR_DDC_B: This bit enables the DDC state machine to go through its DDC routine on PR B. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_EDGE_B: This bit bumps PR B position to the edge. (Not supported.)
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported.)
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported.)
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62	RWX	RX_PR_USE_DFE_CLOCK_B: RX Use the B-bank DFE (h1/Ap-adjusted clock). RJRDMB.
63	RO	constant = 0b0

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	8002480709010C3F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51	RWX	RX_PR_WOBBLE_B: This bit wobbles the PR position for PR B for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
52	RWX	RX_PR_WOBBLE_EDGE: This bit wobbles the PR position for the PR edge for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RWX	RX_PR_DDC_B: This bit enables the DDC state machine to go through its DDC routine on PR B. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_EDGE_B: This bit bumps PR B position to the edge. (Not supported.)
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported.)

Bits	SCOM	Field Mnemonic: Description
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported.)
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62	RWX	RX_PR_USE_DFE_CLOCK_B: RX Use the B-bank DFE (h1/Ap-adjusted clock). RJRDMB.
63	RO	constant = 0b0

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	8002480809010C3F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51	RWX	RX_PR_WOBBLE_B: This bit wobbles the PR position for PR B for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
52	RWX	RX_PR_WOBBLE_EDGE: This bit wobbles the PR position for the PR edge for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RWX	RX_PR_DDC_B: This bit enables the DDC state machine to go through its DDC routine on PR B. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_EDGE_B: This bit bumps PR B position to the edge. (Not supported.)
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported.)
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported.)
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62	RWX	RX_PR_USE_DFE_CLOCK_B: RX Use the B-bank DFE (h1/Ap-adjusted clock). RJRDMB.
63	RO	constant = 0b0

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	8002480909010C3F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51	RWX	RX_PR_WOBBLE_B: This bit wobbles the PR position for PR B for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
52	RWX	RX_PR_WOBBLE_EDGE: This bit wobbles the PR position for the PR edge for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RWX	RX_PR_DDC_B: This bit enables the DDC state machine to go through its DDC routine on PR B. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_EDGE_B: This bit bumps PR B position to the edge. (Not supported.)
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported.)
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported.)
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62	RWX	RX_PR_USE_DFE_CLOCK_B: RX Use the B-bank DFE (h1/Ap-adjusted clock). RJRDMB.
63	RO	constant = 0b0

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	8002480A09010C3F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51	RWX	RX_PR_WOBBLE_B: This bit wobbles the PR position for PR B for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
52	RWX	RX_PR_WOBBLE_EDGE: This bit wobbles the PR position for the PR edge for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RWX	RX_PR_DDC_B: This bit enables the DDC state machine to go through its DDC routine on PR B. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_EDGE_B: This bit bumps PR B position to the edge. (Not supported.)
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported.)
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported.)
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62	RWX	RX_PR_USE_DFE_CLOCK_B: RX Use the B-bank DFE (h1/Ap-adjusted clock). RJRDMB.
63	RO	constant = 0b0

Register Name	**Receive Bit CNTL2 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	8002480B09010C3F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.

Bits	SCOM	Field Mnemonic: Description
51	RWX	RX_PR_WOBBLE_B: This bit wobbles the PR position for PR B for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
52	RWX	RX_PR_WOBBLE_EDGE: This bit wobbles the PR position for the PR edge for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RWX	RX_PR_DDC_B: This bit enables the DDC state machine to go through its DDC routine on PR B. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_EDGE_B: This bit bumps PR B position to the edge. (Not supported.)
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported.)
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported.)
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62	RWX	RX_PR_USE_DFE_CLOCK_B: RX Use the B-bank DFE (h1/Ap-adjusted clock). RJRDMB.
63	RO	constant = 0b0

Register Name	**Receive Bit CNTL2 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	8002480C09010C3F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51	RWX	RX_PR_WOBBLE_B: This bit wobbles the PR position for PR B for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
52	RWX	RX_PR_WOBBLE_EDGE: This bit wobbles the PR position for the PR edge for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.

Bits	SCOM	Field Mnemonic: Description
54	RWX	RX_PR_DDC_B: This bit enables the DDC state machine to go through its DDC routine on PR B. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_EDGE_B: This bit bumps PR B position to the edge. (Not supported.)
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported.)
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported.)
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62	RWX	RX_PR_USE_DFE_CLOCK_B: RX Use the B-bank DFE (h1/Ap-adjusted clock). RJRDMB.
63	RO	constant = 0b0

Register Name	**Receive Bit CNTL2 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	8002480D09010C3F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51	RWX	RX_PR_WOBBLE_B: This bit wobbles the PR position for PR B for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
52	RWX	RX_PR_WOBBLE_EDGE: This bit wobbles the PR position for the PR edge for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RWX	RX_PR_DDC_B: This bit enables the DDC state machine to go through its DDC routine on PR B. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_EDGE_B: This bit bumps PR B position to the edge. (Not supported.)
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported.)

Bits	SCOM	Field Mnemonic: Description
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported.)
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62	RWX	RX_PR_USE_DFE_CLOCK_B: RX Use the B-bank DFE (h1/Ap-adjusted clock). RJRDMB.
63	RO	constant = 0b0

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	8002480E09010C3F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51	RWX	RX_PR_WOBBLE_B: This bit wobbles the PR position for PR B for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
52	RWX	RX_PR_WOBBLE_EDGE: This bit wobbles the PR position for the PR edge for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RWX	RX_PR_DDC_B: This bit enables the DDC state machine to go through its DDC routine on PR B. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_EDGE_B: This bit bumps PR B position to the edge. (Not supported.)
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported.)
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported.)
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62	RWX	RX_PR_USE_DFE_CLOCK_B: RX Use the B-bank DFE (h1/Ap-adjusted clock). RJRDMB.
63	RO	constant = 0b0

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	8002480F09010C3F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51	RWX	RX_PR_WOBBLE_B: This bit wobbles the PR position for PR B for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
52	RWX	RX_PR_WOBBLE_EDGE: This bit wobbles the PR position for the PR edge for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RWX	RX_PR_DDC_B: This bit enables the DDC state machine to go through its DDC routine on PR B. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_EDGE_B: This bit bumps PR B position to the edge. (Not supported.)
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported.)
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported.)
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62	RWX	RX_PR_USE_DFE_CLOCK_B: RX Use the B-bank DFE (h1/Ap-adjusted clock). RJRDMB.
63	RO	constant = 0b0

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	8002481009010C3F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51	RWX	RX_PR_WOBBLE_B: This bit wobbles the PR position for PR B for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
52	RWX	RX_PR_WOBBLE_EDGE: This bit wobbles the PR position for the PR edge for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RWX	RX_PR_DDC_B: This bit enables the DDC state machine to go through its DDC routine on PR B. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_EDGE_B: This bit bumps PR B position to the edge. (Not supported.)
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported.)
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported.)
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62	RWX	RX_PR_USE_DFE_CLOCK_B: RX Use the B-bank DFE (h1/Ap-adjusted clock). RJRDMB.
63	RO	constant = 0b0

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	8002481109010C3F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.

Bits	SCOM	Field Mnemonic: Description
51	RWX	RX_PR_WOBBLE_B: This bit wobbles the PR position for PR B for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
52	RWX	RX_PR_WOBBLE_EDGE: This bit wobbles the PR position for the PR edge for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RWX	RX_PR_DDC_B: This bit enables the DDC state machine to go through its DDC routine on PR B. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_EDGE_B: This bit bumps PR B position to the edge. (Not supported.)
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported.)
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported.)
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62	RWX	RX_PR_USE_DFE_CLOCK_B: RX Use the B-bank DFE (h1/Ap-adjusted clock). RJRDMB.
63	RO	constant = 0b0

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	8002481209010C3F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51	RWX	RX_PR_WOBBLE_B: This bit wobbles the PR position for PR B for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
52	RWX	RX_PR_WOBBLE_EDGE: This bit wobbles the PR position for the PR edge for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.

Bits	SCOM	Field Mnemonic: Description
54	RWX	RX_PR_DDC_B: This bit enables the DDC state machine to go through its DDC routine on PR B. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_EDGE_B: This bit bumps PR B position to the edge. (Not supported.)
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported.)
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported.)
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62	RWX	RX_PR_USE_DFE_CLOCK_B: RX Use the B-bank DFE (h1/Ap-adjusted clock). RJRDMB.
63	RO	constant = 0b0

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	8002481309010C3F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51	RWX	RX_PR_WOBBLE_B: This bit wobbles the PR position for PR B for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
52	RWX	RX_PR_WOBBLE_EDGE: This bit wobbles the PR position for the PR edge for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RWX	RX_PR_DDC_B: This bit enables the DDC state machine to go through its DDC routine on PR B. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_EDGE_B: This bit bumps PR B position to the edge. (Not supported.)
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported.)

Bits	SCOM	Field Mnemonic: Description
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported.)
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62	RWX	RX_PR_USE_DFE_CLOCK_B: RX Use the B-bank DFE (h1/Ap-adjusted clock). RJRDMB.
63	RO	constant = 0b0

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	8002481409010C3F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51	RWX	RX_PR_WOBBLE_B: This bit wobbles the PR position for PR B for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
52	RWX	RX_PR_WOBBLE_EDGE: This bit wobbles the PR position for the PR edge for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RWX	RX_PR_DDC_B: This bit enables the DDC state machine to go through its DDC routine on PR B. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_EDGE_B: This bit bumps PR B position to the edge. (Not supported.)
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported.)
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported.)
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62	RWX	RX_PR_USE_DFE_CLOCK_B: RX Use the B-bank DFE (h1/Ap-adjusted clock). RJRDMB.
63	RO	constant = 0b0

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	8002481509010C3F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51	RWX	RX_PR_WOBBLE_B: This bit wobbles the PR position for PR B for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
52	RWX	RX_PR_WOBBLE_EDGE: This bit wobbles the PR position for the PR edge for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RWX	RX_PR_DDC_B: This bit enables the DDC state machine to go through its DDC routine on PR B. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_EDGE_B: This bit bumps PR B position to the edge. (Not supported.)
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported.)
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported.)
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62	RWX	RX_PR_USE_DFE_CLOCK_B: RX Use the B-bank DFE (h1/Ap-adjusted clock). RJRDMB.
63	RO	constant = 0b0

Register Name	Receive Bit CNTL2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	8002481609010C3F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
51	RWX	RX_PR_WOBBLE_B: This bit wobbles the PR position for PR B for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
52	RWX	RX_PR_WOBBLE_EDGE: This bit wobbles the PR position for the PR edge for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RWX	RX_PR_DDC_B: This bit enables the DDC state machine to go through its DDC routine on PR B. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_EDGE_B: This bit bumps PR B position to the edge. (Not supported.)
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported.)
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported.)
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62	RWX	RX_PR_USE_DFE_CLOCK_B: RX Use the B-bank DFE (h1/Ap-adjusted clock). RJRDMB.
63	RO	constant = 0b0

Register Name	**Receive Bit CNTL2 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL2_EO_PL
Address	8002481709010C3F (SCOM)
Description	This register contains the second set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PR_EDGE_TRACK_CNTL: This field runs edge tracking on the selected bank. 00 = No edge tracking. 01 = Tracks against A data. 10 = Tracks against B data. 11 = Unused.
50	RWX	RX_PR_WOBBLE_A: This bit wobbles the PR position for PR A for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.

Bits	SCOM	Field Mnemonic: Description
51	RWX	RX_PR_WOBBLE_B: This bit wobbles the PR position for PR B for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
52	RWX	RX_PR_WOBBLE_EDGE: This bit wobbles the PR position for the PR edge for the offset function. This is done by first shifting 1 UI away in one direction, and then back and forth 2 UIs to cover the entire range of PR values. When de-asserted, the PR returns to the original value.
53	RWX	RX_PR_DDC_A: This bit enables the DDC state machine to go through its DDC routine on PR A. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
54	RWX	RX_PR_DDC_B: This bit enables the DDC state machine to go through its DDC routine on PR B. It works by shifting to the left and right looking for errors to find the edges. Then, it adds an offset that centers the data between the two edges.
55	RWX	RX_PR_BUMP_TO_EDGE_A: This bit bumps PR A position to the edge => +(16 - clkadj).
56	RWX	RX_PR_BUMP_TO_EDGE_B: This bit bumps PR B position to the edge. (Not supported.)
57	RWX	RX_PR_BUMP_SL_1UI: This bit bumps the PR position of all PRs to the next eye by shifting 32 steps. (Not supported.)
58	RWX	RX_PR_BUMP_SR_1UI: This bit bumps the PR position to the previous eye by shifting 32 steps. (Not supported.)
59:60	RO	constant = 0b00
61	RWX	RX_PR_USE_DFE_CLOCK_A: RX Use the A-bank DFE (h1/Ap-adjusted clock). RJRDMB.
62	RWX	RX_PR_USE_DFE_CLOCK_B: RX Use the B-bank DFE (h1/Ap-adjusted clock). RJRDMB.
63	RO	constant = 0b0

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	8002500009010C3F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RWX	RX_PR_DATA_B_OFFSET: This field contains the offset value applied to PR B.
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	8002500109010C3F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RWX	RX_PR_DATA_B_OFFSET: This field contains the offset value applied to PR B.
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	**Receive Bit CNTL3 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	8002500209010C3F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RWX	RX_PR_DATA_B_OFFSET: This field contains the offset value applied to PR B.
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	**Receive Bit CNTL3 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	8002500309010C3F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RWX	RX_PR_DATA_B_OFFSET: This field contains the offset value applied to PR B.
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	8002500409010C3F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RWX	RX_PR_DATA_B_OFFSET: This field contains the offset value applied to PR B.
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	8002500509010C3F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RWX	RX_PR_DATA_B_OFFSET: This field contains the offset value applied to PR B.
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	8002500609010C3F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RWX	RX_PR_DATA_B_OFFSET: This field contains the offset value applied to PR B.
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.

Bits	SCOM	Field Mnemonic: Description
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	8002500709010C3F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RWX	RX_PR_DATA_B_OFFSET: This field contains the offset value applied to PR B.
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	8002500809010C3F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RWX	RX_PR_DATA_B_OFFSET: This field contains the offset value applied to PR B.
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	8002500909010C3F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RWX	RX_PR_DATA_B_OFFSET: This field contains the offset value applied to PR B.

Bits	SCOM	Field Mnemonic: Description
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	8002500A09010C3F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RWX	RX_PR_DATA_B_OFFSET: This field contains the offset value applied to PR B.
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	8002500B09010C3F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RWX	RX_PR_DATA_B_OFFSET: This field contains the offset value applied to PR B.
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	8002500C09010C3F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RWX	RX_PR_DATA_B_OFFSET: This field contains the offset value applied to PR B.
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	8002500D09010C3F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RWX	RX_PR_DATA_B_OFFSET: This field contains the offset value applied to PR B.
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	8002500E09010C3F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RWX	RX_PR_DATA_B_OFFSET: This field contains the offset value applied to PR B.
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	8002500F09010C3F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RWX	RX_PR_DATA_B_OFFSET: This field contains the offset value applied to PR B.
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	8002501009010C3F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RWX	RX_PR_DATA_B_OFFSET: This field contains the offset value applied to PR B.
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	8002501109010C3F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RWX	RX_PR_DATA_B_OFFSET: This field contains the offset value applied to PR B.
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.

Bits	SCOM	Field Mnemonic: Description
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	8002501209010C3F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RWX	RX_PR_DATA_B_OFFSET: This field contains the offset value applied to PR B.
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	8002501309010C3F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RWX	RX_PR_DATA_B_OFFSET: This field contains the offset value applied to PR B.
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	8002501409010C3F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RWX	RX_PR_DATA_B_OFFSET: This field contains the offset value applied to PR B.

Bits	SCOM	Field Mnemonic: Description
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	8002501509010C3F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RWX	RX_PR_DATA_B_OFFSET: This field contains the offset value applied to PR B.
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	8002501609010C3F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RWX	RX_PR_DATA_B_OFFSET: This field contains the offset value applied to PR B.
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	Receive Bit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL3_EO_PL
Address	8002501709010C3F (SCOM)
Description	This register contains the third set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_PR_DATA_A_OFFSET: This field contains the offset value applied to PR A.
54:59	RWX	RX_PR_DATA_B_OFFSET: This field contains the offset value applied to PR B.
60	RWX	RX_PR_BIT_LOCK_DONE: This bit indicates that the bit lock is done. It is used to gate the invalid lock in the CDR logic.
61	RWX	RX_PR_INVALID_LOCK_FILTER_EN: This bit enables the filtered invalid-lock, phase-rotator shift right. The default is ON.
62:63	RWX	RX_PR_INVALID_LOCK_BUMP_SIZE: This field sets the size of the invalid_lock_bump.

Register Name	**Receive Bit CNTL4 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	8002580009010C3F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58:61	RO	constant = 0b0000
62	RWX	RX_PR_RESET: Set this bit to reset the CDR logic. Power and clocks must be enabled in the slice.
63	RWX	RX_IORESET: This bit resets the given RX lane (except the CDR logic).

Register Name	**Receive Bit CNTL4 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	8002580109010C3F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58:61	RO	constant = 0b0000
62	RWX	RX_PR_RESET: Set this bit to reset the CDR logic. Power and clocks must be enabled in the slice.
63	RWX	RX_IORESET: This bit resets the given RX lane (except the CDR logic).

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	8002580209010C3F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58:61	RO	constant = 0b0000
62	RWX	RX_PR_RESET: Set this bit to reset the CDR logic. Power and clocks must be enabled in the slice.
63	RWX	RX_IORESET: This bit resets the given RX lane (except the CDR logic).

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	8002580309010C3F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58:61	RO	constant = 0b0000
62	RWX	RX_PR_RESET: Set this bit to reset the CDR logic. Power and clocks must be enabled in the slice.
63	RWX	RX_IORESET: This bit resets the given RX lane (except the CDR logic).

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	8002580409010C3F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.

Bits	SCOM	Field Mnemonic: Description
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58:61	RO	constant = 0b0000
62	RWX	RX_PR_RESET: Set this bit to reset the CDR logic. Power and clocks must be enabled in the slice.
63	RWX	RX_IORESET: This bit resets the given RX lane (except the CDR logic).

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	8002580509010C3F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58:61	RO	constant = 0b0000
62	RWX	RX_PR_RESET: Set this bit to reset the CDR logic. Power and clocks must be enabled in the slice.
63	RWX	RX_IORESET: This bit resets the given RX lane (except the CDR logic).

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	8002580609010C3F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58:61	RO	constant = 0b0000
62	RWX	RX_PR_RESET: Set this bit to reset the CDR logic. Power and clocks must be enabled in the slice.
63	RWX	RX_IORESET: This bit resets the given RX lane (except the CDR logic).

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	8002580709010C3F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58:61	RO	constant = 0b0000
62	RWX	RX_PR_RESET: Set this bit to reset the CDR logic. Power and clocks must be enabled in the slice.
63	RWX	RX_IORESET: This bit resets the given RX lane (except the CDR logic).

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	8002580809010C3F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58:61	RO	constant = 0b0000
62	RWX	RX_PR_RESET: Set this bit to reset the CDR logic. Power and clocks must be enabled in the slice.
63	RWX	RX_IORESET: This bit resets the given RX lane (except the CDR logic).

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	8002580909010C3F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.

Bits	SCOM	Field Mnemonic: Description
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58:61	RO	constant = 0b0000
62	RWX	RX_PR_RESET: Set this bit to reset the CDR logic. Power and clocks must be enabled in the slice.
63	RWX	RX_IORESET: This bit resets the given RX lane (except the CDR logic).

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	8002580A09010C3F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58:61	RO	constant = 0b0000
62	RWX	RX_PR_RESET: Set this bit to reset the CDR logic. Power and clocks must be enabled in the slice.
63	RWX	RX_IORESET: This bit resets the given RX lane (except the CDR logic).

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	8002580B09010C3F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58:61	RO	constant = 0b0000
62	RWX	RX_PR_RESET: Set this bit to reset the CDR logic. Power and clocks must be enabled in the slice.
63	RWX	RX_IORESET: This bit resets the given RX lane (except the CDR logic).

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	8002580C09010C3F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58:61	RO	constant = 0b0000
62	RWX	RX_PR_RESET: Set this bit to reset the CDR logic. Power and clocks must be enabled in the slice.
63	RWX	RX_IORESET: This bit resets the given RX lane (except the CDR logic).

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	8002580D09010C3F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58:61	RO	constant = 0b0000
62	RWX	RX_PR_RESET: Set this bit to reset the CDR logic. Power and clocks must be enabled in the slice.
63	RWX	RX_IORESET: This bit resets the given RX lane (except the CDR logic).

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	8002580E09010C3F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.

Bits	SCOM	Field Mnemonic: Description
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58:61	RO	constant = 0b0000
62	RWX	RX_PR_RESET: Set this bit to reset the CDR logic. Power and clocks must be enabled in the slice.
63	RWX	RX_IORESET: This bit resets the given RX lane (except the CDR logic).

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	8002580F09010C3F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58:61	RO	constant = 0b0000
62	RWX	RX_PR_RESET: Set this bit to reset the CDR logic. Power and clocks must be enabled in the slice.
63	RWX	RX_IORESET: This bit resets the given RX lane (except the CDR logic).

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	8002581009010C3F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58:61	RO	constant = 0b0000
62	RWX	RX_PR_RESET: Set this bit to reset the CDR logic. Power and clocks must be enabled in the slice.
63	RWX	RX_IORESET: This bit resets the given RX lane (except the CDR logic).

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	8002581109010C3F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58:61	RO	constant = 0b0000
62	RWX	RX_PR_RESET: Set this bit to reset the CDR logic. Power and clocks must be enabled in the slice.
63	RWX	RX_IORESET: This bit resets the given RX lane (except the CDR logic).

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	8002581209010C3F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58:61	RO	constant = 0b0000
62	RWX	RX_PR_RESET: Set this bit to reset the CDR logic. Power and clocks must be enabled in the slice.
63	RWX	RX_IORESET: This bit resets the given RX lane (except the CDR logic).

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	8002581309010C3F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.

Bits	SCOM	Field Mnemonic: Description
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58:61	RO	constant = 0b0000
62	RWX	RX_PR_RESET: Set this bit to reset the CDR logic. Power and clocks must be enabled in the slice.
63	RWX	RX_IORESET: This bit resets the given RX lane (except the CDR logic).

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	8002581409010C3F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58:61	RO	constant = 0b0000
62	RWX	RX_PR_RESET: Set this bit to reset the CDR logic. Power and clocks must be enabled in the slice.
63	RWX	RX_IORESET: This bit resets the given RX lane (except the CDR logic).

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	8002581509010C3F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58:61	RO	constant = 0b0000
62	RWX	RX_PR_RESET: Set this bit to reset the CDR logic. Power and clocks must be enabled in the slice.
63	RWX	RX_IORESET: This bit resets the given RX lane (except the CDR logic).

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	8002581609010C3F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58:61	RO	constant = 0b0000
62	RWX	RX_PR_RESET: Set this bit to reset the CDR logic. Power and clocks must be enabled in the slice.
63	RWX	RX_IORESET: This bit resets the given RX lane (except the CDR logic).

Register Name	Receive Bit CNTL4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL4_EO_PL
Address	8002581709010C3F (SCOM)
Description	This register contains the fourth set of EO control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PR_TRACE_DDC_STOP: This bit enables the trace debug DDC state to stop the state machines.
49:53	RWX	RX_PR_TRACE_DDC_SM: This bit determines when to stop the state machine for trace debug.
54	RWX	RX_PR_TRACE_WOBBLE_STOP: This bit enables the trace debug wobble state to stop the state machines.
55:57	RWX	RX_PR_TRACE_WOBBLE_SM: This field determines when to stop the state machine for trace debug.
58:61	RO	constant = 0b0000
62	RWX	RX_PR_RESET: Set this bit to reset the CDR logic. Power and clocks must be enabled in the slice.
63	RWX	RX_IORESET: This bit resets the given RX lane (except the CDR logic).

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	8002600009010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
50	NCX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	8002600109010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	8002600209010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	8002600309010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	8002600409010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	8002600509010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	8002600609010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	8002600709010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	8002600809010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	8002600909010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	8002600A09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
50	NCX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	8002600B09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	8002600C09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	8002600D09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	**Receive Bit CNTL5 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	8002600E09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	**Receive Bit CNTL5 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	8002600F09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	**Receive Bit CNTL5 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	8002601009010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	**Receive Bit CNTL5 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	8002601109010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	8002601209010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	8002601309010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	8002601409010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
50	NCX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	8002601509010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	8002601609010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Receive Bit CNTL5 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_CNTL5_EO_PL
Address	8002601709010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	**Receive Bit STAT1 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	8002680009010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	**Receive Bit STAT1 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	8002680109010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	**Receive Bit STAT1 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	8002680209010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	**Receive Bit STAT1 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	8002680309010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	8002680409010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	8002680509010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	8002680609010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	8002680709010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	8002680809010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	8002680909010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	8002680A09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	8002680B09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	8002680C09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	8002680D09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	8002680E09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	8002680F09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	**Receive Bit STAT1 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	8002681009010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	**Receive Bit STAT1 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	8002681109010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	**Receive Bit STAT1 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	8002681209010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	**Receive Bit STAT1 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	8002681309010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	8002681409010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	8002681509010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	8002681609010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	Receive Bit STAT1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT1_EO_PL
Address	8002681709010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	8002700009010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	ROX	Reserved field.
54	ROX	Reserved field.
55	RO	constant = 0b0
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59:63	RO	constant = 0b00000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	8002700109010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	ROX	Reserved field.
54	ROX	Reserved field.
55	RO	constant = 0b0
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59:63	RO	constant = 0b00000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	8002700209010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	ROX	Reserved field.
54	ROX	Reserved field.
55	RO	constant = 0b0
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59:63	RO	constant = 0b00000

Register Name	**Receive Bit STAT2 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	8002700309010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	ROX	Reserved field.
54	ROX	Reserved field.
55	RO	constant = 0b0
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59:63	RO	constant = 0b00000

Register Name	**Receive Bit STAT2 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	8002700409010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
52	ROX	Reserved field.
53	ROX	Reserved field.
54	ROX	Reserved field.
55	RO	constant = 0b0
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59:63	RO	constant = 0b00000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	8002700509010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	ROX	Reserved field.
54	ROX	Reserved field.
55	RO	constant = 0b0
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59:63	RO	constant = 0b00000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	8002700609010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	ROX	Reserved field.
54	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
55	RO	constant = 0b0
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59:63	RO	constant = 0b00000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	8002700709010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	ROX	Reserved field.
54	ROX	Reserved field.
55	RO	constant = 0b0
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59:63	RO	constant = 0b00000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	8002700809010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	ROX	Reserved field.
54	ROX	Reserved field.
55	RO	constant = 0b0
56	ROX	Reserved field.
57	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
58	ROX	Reserved field.
59:63	RO	constant = 0b00000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	8002700909010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	ROX	Reserved field.
54	ROX	Reserved field.
55	RO	constant = 0b0
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59:63	RO	constant = 0b00000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	8002700A09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	ROX	Reserved field.
54	ROX	Reserved field.
55	RO	constant = 0b0
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59:63	RO	constant = 0b00000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	8002700B09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	ROX	Reserved field.
54	ROX	Reserved field.
55	RO	constant = 0b0
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59:63	RO	constant = 0b00000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	8002700C09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	ROX	Reserved field.
54	ROX	Reserved field.
55	RO	constant = 0b0
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59:63	RO	constant = 0b00000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	8002700D09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	ROX	Reserved field.
54	ROX	Reserved field.
55	RO	constant = 0b0
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59:63	RO	constant = 0b00000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	8002700E09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	ROX	Reserved field.
54	ROX	Reserved field.
55	RO	constant = 0b0
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59:63	RO	constant = 0b00000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	8002700F09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
52	ROX	Reserved field.
53	ROX	Reserved field.
54	ROX	Reserved field.
55	RO	constant = 0b0
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59:63	RO	constant = 0b00000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	8002701009010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	ROX	Reserved field.
54	ROX	Reserved field.
55	RO	constant = 0b0
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59:63	RO	constant = 0b00000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	8002701109010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	ROX	Reserved field.
54	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
55	RO	constant = 0b0
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59:63	RO	constant = 0b00000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	8002701209010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	ROX	Reserved field.
54	ROX	Reserved field.
55	RO	constant = 0b0
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59:63	RO	constant = 0b00000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	8002701309010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	ROX	Reserved field.
54	ROX	Reserved field.
55	RO	constant = 0b0
56	ROX	Reserved field.
57	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
58	ROX	Reserved field.
59:63	RO	constant = 0b00000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	8002701409010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	ROX	Reserved field.
54	ROX	Reserved field.
55	RO	constant = 0b0
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59:63	RO	constant = 0b00000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	8002701509010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	ROX	Reserved field.
54	ROX	Reserved field.
55	RO	constant = 0b0
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59:63	RO	constant = 0b00000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	8002701609010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	ROX	Reserved field.
54	ROX	Reserved field.
55	RO	constant = 0b0
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59:63	RO	constant = 0b00000

Register Name	Receive Bit STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT2_EO_PL
Address	8002701709010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	ROX	Reserved field.
54	ROX	Reserved field.
55	RO	constant = 0b0
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59:63	RO	constant = 0b00000

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	8002780009010C3F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	8002780109010C3F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	8002780209010C3F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	8002780309010C3F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	**Receive Bit STAT3 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	8002780409010C3F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	**SCOM**	**Field Mnemonic: Description**
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	**Receive Bit STAT3 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	8002780509010C3F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	**SCOM**	**Field Mnemonic: Description**
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	**Receive Bit STAT3 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	8002780609010C3F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	**SCOM**	**Field Mnemonic: Description**
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	**Receive Bit STAT3 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	8002780709010C3F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	8002780809010C3F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	8002780909010C3F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	8002780A09010C3F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	**Receive Bit STAT3 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	8002780B09010C3F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	**Receive Bit STAT3 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	8002780C09010C3F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	**Receive Bit STAT3 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	8002780D09010C3F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	**Receive Bit STAT3 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	8002780E09010C3F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	8002780F09010C3F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	8002781009010C3F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	8002781109010C3F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	8002781209010C3F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	8002781309010C3F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	8002781409010C3F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	8002781509010C3F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	8002781609010C3F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT3_EO_PL
Address	8002781709010C3F (SCOM)
Description	This register contains the third set of EO status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_A_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank A clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL
Address	8002800009010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50:56	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
57:63	RO	constant = 0b0000000

Register Name	Receive Bit STAT4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL
Address	8002800109010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50:56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	Receive Bit STAT4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL
Address	8002800209010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50:56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	Receive Bit STAT4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL
Address	8002800309010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50:56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	Receive Bit STAT4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL
Address	8002800409010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50:56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	Receive Bit STAT4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL
Address	8002800509010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50:56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	Receive Bit STAT4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL
Address	8002800609010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50:56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	Receive Bit STAT4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL
Address	8002800709010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50:56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	Receive Bit STAT4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL
Address	8002800809010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50:56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	Receive Bit STAT4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL
Address	8002800909010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50:56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	Receive Bit STAT4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL
Address	8002800A09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
50:56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	Receive Bit STAT4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL
Address	8002800B09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50:56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	Receive Bit STAT4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL
Address	8002800C09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50:56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	Receive Bit STAT4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL
Address	8002800D09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50:56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	Receive Bit STAT4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL
Address	8002800E09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50:56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	Receive Bit STAT4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL
Address	8002800F09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50:56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	Receive Bit STAT4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL
Address	8002801009010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50:56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	Receive Bit STAT4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL
Address	8002801109010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50:56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	Receive Bit STAT4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL
Address	8002801209010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50:56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	Receive Bit STAT4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL
Address	8002801309010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50:56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	Receive Bit STAT4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL
Address	8002801409010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
50:56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	Receive Bit STAT4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL
Address	8002801509010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50:56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	Receive Bit STAT4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL
Address	8002801609010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50:56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	Receive Bit STAT4 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT4_EO_PL
Address	8002801709010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50:56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	Receive Bit STAT1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL
Address	8003180009010C3F (SCOM)
Description	This register contains the first set of O status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_B_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank B clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL
Address	8003180109010C3F (SCOM)
Description	This register contains the first set of O status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_B_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank B clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL
Address	8003180209010C3F (SCOM)
Description	This register contains the first set of O status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_B_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank B clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#0.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL
Address	8003180309010C3F (SCOM)
Description	This register contains the first set of O status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_B_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank B clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL
Address	8003180409010C3F (SCOM)
Description	This register contains the first set of O status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_B_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank B clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL
Address	8003180509010C3F (SCOM)
Description	This register contains the first set of O status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_B_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank B clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL
Address	8003180609010C3F (SCOM)
Description	This register contains the first set of O status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_B_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank B clock offset when performing a DFE calibration.

Register Name	**Receive Bit STAT1 O Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#1.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL
Address	8003180709010C3F (SCOM)
Description	This register contains the first set of O status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_B_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank B clock offset when performing a DFE calibration.

Register Name	**Receive Bit STAT1 O Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL
Address	8003180809010C3F (SCOM)
Description	This register contains the first set of O status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_B_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank B clock offset when performing a DFE calibration.

Register Name	**Receive Bit STAT1 O Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL
Address	8003180909010C3F (SCOM)
Description	This register contains the first set of O status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_B_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank B clock offset when performing a DFE calibration.

Register Name	**Receive Bit STAT1 O Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL
Address	8003180A09010C3F (SCOM)
Description	This register contains the first set of O status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_B_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank B clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#2.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL
Address	8003180B09010C3F (SCOM)
Description	This register contains the first set of O status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_B_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank B clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL
Address	8003180C09010C3F (SCOM)
Description	This register contains the first set of O status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_B_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank B clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL
Address	8003180D09010C3F (SCOM)
Description	This register contains the first set of O status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_B_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank B clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL
Address	8003180E09010C3F (SCOM)
Description	This register contains the first set of O status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_B_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank B clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#3.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL
Address	8003180F09010C3F (SCOM)
Description	This register contains the first set of O status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_B_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank B clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL
Address	8003181009010C3F (SCOM)
Description	This register contains the first set of O status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_B_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank B clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL
Address	8003181109010C3F (SCOM)
Description	This register contains the first set of O status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_B_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank B clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL
Address	8003181209010C3F (SCOM)
Description	This register contains the first set of O status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_B_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank B clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#4.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL
Address	8003181309010C3F (SCOM)
Description	This register contains the first set of O status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_B_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank B clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL
Address	8003181409010C3F (SCOM)
Description	This register contains the first set of O status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_B_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank B clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.
Address	8003181509010C3F (SCOM)
Description	This register contains the first set of O status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_B_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank B clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL
Address	8003181609010C3F (SCOM)
Description	This register contains the first set of O status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_B_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank B clock offset when performing a DFE calibration.

Register Name	Receive Bit STAT1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXPACKS#5.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIT_STAT1_O_PL
Address	8003181709010C3F (SCOM)
Description	This register contains the first set of O status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	ROX	Reserved field.
54:59	ROX	Reserved field.
60:63	RWX	RX_B_PR_DFE_CLKADJ: This field contains the tweak value, in phase rotator steps, for the bank B clock offset when performing a DFE calibration.

Register Name	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#0.PLREGS.RX_GLBSM_PL_CNTL1_O_PL
Address	8003200009010C3F (SCOM)
Description	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_RUN_LANE: This bit runs training and subsequent recalibration on the given lane.
49	RWX	RX_RUN_DCCAL: This bit runs on-die DC training on the given lane.
50	RWX	RX_RECAL_REQ: This bit requests recalibration on the given lane.
51	RWX	RX_RECAL_ABORT: This bit stops recalibration on the given lane.
52	RWX	RX_LANE_DISABLED: This bit is used to set the given lane to be ignored by the training logic. This bit does not affect power down.
53:63	RO	constant = 0b00000000000

Register Name	**Receive GLBSM Per-Lane CNTL1 O Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#1.PLREGS.RX_GLBSM_PL_CNTL1_O_PL
Address	8003200109010C3F (SCOM)
Description	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_RUN_LANE: This bit runs training and subsequent recalibration on the given lane.
49	RWX	RX_RUN_DCCAL: This bit runs on-die DC training on the given lane.
50	RWX	RX_RECAL_REQ: This bit requests recalibration on the given lane.
51	RWX	RX_RECAL_ABORT: This bit stops recalibration on the given lane.
52	RWX	RX_LANE_DISABLED: This bit is used to set the given lane to be ignored by the training logic. This bit does not affect power down.
53:63	RO	constant = 0b00000000000

Register Name	**Receive GLBSM Per-Lane CNTL1 O Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#2.PLREGS.RX_GLBSM_PL_CNTL1_O_PL
Address	8003200209010C3F (SCOM)
Description	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_RUN_LANE: This bit runs training and subsequent recalibration on the given lane.
49	RWX	RX_RUN_DCCAL: This bit runs on-die DC training on the given lane.
50	RWX	RX_RECAL_REQ: This bit requests recalibration on the given lane.
51	RWX	RX_RECAL_ABORT: This bit stops recalibration on the given lane.
52	RWX	RX_LANE_DISABLED: This bit is used to set the given lane to be ignored by the training logic. This bit does not affect power down.
53:63	RO	constant = 0b00000000000

Register Name	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#3.PLREGS.RX_GLBSM_PL_CNTL1_O_PL
Address	8003200309010C3F (SCOM)
Description	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_RUN_LANE: This bit runs training and subsequent recalibration on the given lane.
49	RWX	RX_RUN_DCCAL: This bit runs on-die DC training on the given lane.
50	RWX	RX_RECAL_REQ: This bit requests recalibration on the given lane.
51	RWX	RX_RECAL_ABORT: This bit stops recalibration on the given lane.
52	RWX	RX_LANE_DISABLED: This bit is used to set the given lane to be ignored by the training logic. This bit does not affect power down.
53:63	RO	constant = 0b00000000000

Register Name	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#4.PLREGS.RX_GLBSM_PL_CNTL1_O_PL
Address	8003200409010C3F (SCOM)
Description	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_RUN_LANE: This bit runs training and subsequent recalibration on the given lane.
49	RWX	RX_RUN_DCCAL: This bit runs on-die DC training on the given lane.
50	RWX	RX_RECAL_REQ: This bit requests recalibration on the given lane.
51	RWX	RX_RECAL_ABORT: This bit stops recalibration on the given lane.
52	RWX	RX_LANE_DISABLED: This bit is used to set the given lane to be ignored by the training logic. This bit does not affect power down.
53:63	RO	constant = 0b00000000000

Register Name	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#5.PLREGS.RX_GLBSM_PL_CNTL1_O_PL
Address	8003200509010C3F (SCOM)
Description	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_RUN_LANE: This bit runs training and subsequent recalibration on the given lane.
49	RWX	RX_RUN_DCCAL: This bit runs on-die DC training on the given lane.
50	RWX	RX_RECAL_REQ: This bit requests recalibration on the given lane.
51	RWX	RX_RECAL_ABORT: This bit stops recalibration on the given lane.

Bits	SCOM	Field Mnemonic: Description
52	RWX	RX_LANE_DISABLED: This bit is used to set the given lane to be ignored by the training logic. This bit does not affect power down.
53:63	RO	constant = 0b00000000000

Register Name	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#6.PLREGS.RX_GLBSM_PL_CNTL1_O_PL
Address	8003200609010C3F (SCOM)
Description	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_RUN_LANE: This bit runs training and subsequent recalibration on the given lane.
49	RWX	RX_RUN_DCCAL: This bit runs on-die DC training on the given lane.
50	RWX	RX_RECAL_REQ: This bit requests recalibration on the given lane.
51	RWX	RX_RECAL_ABORT: This bit stops recalibration on the given lane.
52	RWX	RX_LANE_DISABLED: This bit is used to set the given lane to be ignored by the training logic. This bit does not affect power down.
53:63	RO	constant = 0b00000000000

Register Name	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#7.PLREGS.RX_GLBSM_PL_CNTL1_O_PL
Address	8003200709010C3F (SCOM)
Description	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_RUN_LANE: This bit runs training and subsequent recalibration on the given lane.
49	RWX	RX_RUN_DCCAL: This bit runs on-die DC training on the given lane.
50	RWX	RX_RECAL_REQ: This bit requests recalibration on the given lane.
51	RWX	RX_RECAL_ABORT: This bit stops recalibration on the given lane.
52	RWX	RX_LANE_DISABLED: This bit is used to set the given lane to be ignored by the training logic. This bit does not affect power down.
53:63	RO	constant = 0b00000000000

Register Name	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#8.PLREGS.RX_GLBSM_PL_CNTL1_O_PL
Address	8003200809010C3F (SCOM)
Description	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_RUN_LANE: This bit runs training and subsequent recalibration on the given lane.
49	RWX	RX_RUN_DCCAL: This bit runs on-die DC training on the given lane.
50	RWX	RX_RECAL_REQ: This bit requests recalibration on the given lane.
51	RWX	RX_RECAL_ABORT: This bit stops recalibration on the given lane.
52	RWX	RX_LANE_DISABLED: This bit is used to set the given lane to be ignored by the training logic. This bit does not affect power down.
53:63	RO	constant = 0b00000000000

Register Name	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#9.PLREGS.RX_GLBSM_PL_CNTL1_O_PL
Address	8003200909010C3F (SCOM)
Description	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_RUN_LANE: This bit runs training and subsequent recalibration on the given lane.
49	RWX	RX_RUN_DCCAL: This bit runs on-die DC training on the given lane.
50	RWX	RX_RECAL_REQ: This bit requests recalibration on the given lane.
51	RWX	RX_RECAL_ABORT: This bit stops recalibration on the given lane.
52	RWX	RX_LANE_DISABLED: This bit is used to set the given lane to be ignored by the training logic. This bit does not affect power down.
53:63	RO	constant = 0b00000000000

Register Name	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#10.PLREGS.RX_GLBSM_PL_CNTL1_O_PL
Address	8003200A09010C3F (SCOM)
Description	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_RUN_LANE: This bit runs training and subsequent recalibration on the given lane.
49	RWX	RX_RUN_DCCAL: This bit runs on-die DC training on the given lane.
50	RWX	RX_RECAL_REQ: This bit requests recalibration on the given lane.
51	RWX	RX_RECAL_ABORT: This bit stops recalibration on the given lane.
52	RWX	RX_LANE_DISABLED: This bit is used to set the given lane to be ignored by the training logic. This bit does not affect power down.
53:63	RO	constant = 0b00000000000

Register Name	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#11.PLREGS.RX_GLBSM_PL_CNTL1_O_PL
Address	8003200B09010C3F (SCOM)
Description	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_RUN_LANE: This bit runs training and subsequent recalibration on the given lane.
49	RWX	RX_RUN_DCCAL: This bit runs on-die DC training on the given lane.
50	RWX	RX_RECAL_REQ: This bit requests recalibration on the given lane.
51	RWX	RX_RECAL_ABORT: This bit stops recalibration on the given lane.
52	RWX	RX_LANE_DISABLED: This bit is used to set the given lane to be ignored by the training logic. This bit does not affect power down.
53:63	RO	constant = 0b00000000000

Register Name	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#12.PLREGS.RX_GLBSM_PL_CNTL1_O_PL
Address	8003200C09010C3F (SCOM)
Description	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_RUN_LANE: This bit runs training and subsequent recalibration on the given lane.
49	RWX	RX_RUN_DCCAL: This bit runs on-die DC training on the given lane.
50	RWX	RX_RECAL_REQ: This bit requests recalibration on the given lane.
51	RWX	RX_RECAL_ABORT: This bit stops recalibration on the given lane.
52	RWX	RX_LANE_DISABLED: This bit is used to set the given lane to be ignored by the training logic. This bit does not affect power down.
53:63	RO	constant = 0b00000000000

Register Name	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#13.PLREGS.RX_GLBSM_PL_CNTL1_O_PL
Address	8003200D09010C3F (SCOM)
Description	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_RUN_LANE: This bit runs training and subsequent recalibration on the given lane.
49	RWX	RX_RUN_DCCAL: This bit runs on-die DC training on the given lane.
50	RWX	RX_RECAL_REQ: This bit requests recalibration on the given lane.
51	RWX	RX_RECAL_ABORT: This bit stops recalibration on the given lane.

Bits	SCOM	Field Mnemonic: Description
52	RWX	RX_LANE_DISABLED: This bit is used to set the given lane to be ignored by the training logic. This bit does not affect power down.
53:63	RO	constant = 0b00000000000

Register Name	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#14.PLREGS.RX_GLBSM_PL_CNTL1_O_PL
Address	8003200E09010C3F (SCOM)
Description	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_RUN_LANE: This bit runs training and subsequent recalibration on the given lane.
49	RWX	RX_RUN_DCCAL: This bit runs on-die DC training on the given lane.
50	RWX	RX_RECAL_REQ: This bit requests recalibration on the given lane.
51	RWX	RX_RECAL_ABORT: This bit stops recalibration on the given lane.
52	RWX	RX_LANE_DISABLED: This bit is used to set the given lane to be ignored by the training logic. This bit does not affect power down.
53:63	RO	constant = 0b00000000000

Register Name	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#15.PLREGS.RX_GLBSM_PL_CNTL1_O_PL
Address	8003200F09010C3F (SCOM)
Description	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_RUN_LANE: This bit runs training and subsequent recalibration on the given lane.
49	RWX	RX_RUN_DCCAL: This bit runs on-die DC training on the given lane.
50	RWX	RX_RECAL_REQ: This bit requests recalibration on the given lane.
51	RWX	RX_RECAL_ABORT: This bit stops recalibration on the given lane.
52	RWX	RX_LANE_DISABLED: This bit is used to set the given lane to be ignored by the training logic. This bit does not affect power down.
53:63	RO	constant = 0b00000000000

Register Name	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#16.PLREGS.RX_GLBSM_PL_CNTL1_O_PL
Address	8003201009010C3F (SCOM)
Description	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_RUN_LANE: This bit runs training and subsequent recalibration on the given lane.
49	RWX	RX_RUN_DCCAL: This bit runs on-die DC training on the given lane.
50	RWX	RX_RECAL_REQ: This bit requests recalibration on the given lane.
51	RWX	RX_RECAL_ABORT: This bit stops recalibration on the given lane.
52	RWX	RX_LANE_DISABLED: This bit is used to set the given lane to be ignored by the training logic. This bit does not affect power down.
53:63	RO	constant = 0b00000000000

Register Name	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#17.PLREGS.RX_GLBSM_PL_CNTL1_O_PL
Address	8003201109010C3F (SCOM)
Description	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_RUN_LANE: This bit runs training and subsequent recalibration on the given lane.
49	RWX	RX_RUN_DCCAL: This bit runs on-die DC training on the given lane.
50	RWX	RX_RECAL_REQ: This bit requests recalibration on the given lane.
51	RWX	RX_RECAL_ABORT: This bit stops recalibration on the given lane.
52	RWX	RX_LANE_DISABLED: This bit is used to set the given lane to be ignored by the training logic. This bit does not affect power down.
53:63	RO	constant = 0b00000000000

Register Name	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#18.PLREGS.RX_GLBSM_PL_CNTL1_O_PL
Address	8003201209010C3F (SCOM)
Description	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_RUN_LANE: This bit runs training and subsequent recalibration on the given lane.
49	RWX	RX_RUN_DCCAL: This bit runs on-die DC training on the given lane.
50	RWX	RX_RECAL_REQ: This bit requests recalibration on the given lane.
51	RWX	RX_RECAL_ABORT: This bit stops recalibration on the given lane.
52	RWX	RX_LANE_DISABLED: This bit is used to set the given lane to be ignored by the training logic. This bit does not affect power down.
53:63	RO	constant = 0b00000000000

Register Name	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#19.PLREGS.RX_GLBSM_PL_CNTL1_O_PL
Address	8003201309010C3F (SCOM)
Description	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_RUN_LANE: This bit runs training and subsequent recalibration on the given lane.
49	RWX	RX_RUN_DCCAL: This bit runs on-die DC training on the given lane.
50	RWX	RX_RECAL_REQ: This bit requests recalibration on the given lane.
51	RWX	RX_RECAL_ABORT: This bit stops recalibration on the given lane.
52	RWX	RX_LANE_DISABLED: This bit is used to set the given lane to be ignored by the training logic. This bit does not affect power down.
53:63	RO	constant = 0b00000000000

Register Name	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#20.PLREGS.RX_GLBSM_PL_CNTL1_O_PL
Address	8003201409010C3F (SCOM)
Description	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_RUN_LANE: This bit runs training and subsequent recalibration on the given lane.
49	RWX	RX_RUN_DCCAL: This bit runs on-die DC training on the given lane.
50	RWX	RX_RECAL_REQ: This bit requests recalibration on the given lane.
51	RWX	RX_RECAL_ABORT: This bit stops recalibration on the given lane.
52	RWX	RX_LANE_DISABLED: This bit is used to set the given lane to be ignored by the training logic. This bit does not affect power down.
53:63	RO	constant = 0b00000000000

Register Name	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#21.PLREGS.RX_GLBSM_PL_CNTL1_O_PL
Address	8003201509010C3F (SCOM)
Description	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_RUN_LANE: This bit runs training and subsequent recalibration on the given lane.
49	RWX	RX_RUN_DCCAL: This bit runs on-die DC training on the given lane.
50	RWX	RX_RECAL_REQ: This bit requests recalibration on the given lane.
51	RWX	RX_RECAL_ABORT: This bit stops recalibration on the given lane.

Bits	SCOM	Field Mnemonic: Description
52	RWX	RX_LANE_DISABLED: This bit is used to set the given lane to be ignored by the training logic. This bit does not affect power down.
53:63	RO	constant = 0b00000000000

Register Name	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#22.PLREGS.RX_GLBSM_PL_CNTL1_O_PL
Address	8003201609010C3F (SCOM)
Description	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_RUN_LANE: This bit runs training and subsequent recalibration on the given lane.
49	RWX	RX_RUN_DCCAL: This bit runs on-die DC training on the given lane.
50	RWX	RX_RECAL_REQ: This bit requests recalibration on the given lane.
51	RWX	RX_RECAL_ABORT: This bit stops recalibration on the given lane.
52	RWX	RX_LANE_DISABLED: This bit is used to set the given lane to be ignored by the training logic. This bit does not affect power down.
53:63	RO	constant = 0b00000000000

Register Name	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#23.PLREGS.RX_GLBSM_PL_CNTL1_O_PL
Address	8003201709010C3F (SCOM)
Description	Receive GLBSM Per-Lane CNTL1 O Per-Lane Register

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_RUN_LANE: This bit runs training and subsequent recalibration on the given lane.
49	RWX	RX_RUN_DCCAL: This bit runs on-die DC training on the given lane.
50	RWX	RX_RECAL_REQ: This bit requests recalibration on the given lane.
51	RWX	RX_RECAL_ABORT: This bit stops recalibration on the given lane.
52	RWX	RX_LANE_DISABLED: This bit is used to set the given lane to be ignored by the training logic. This bit does not affect power down.
53:63	RO	constant = 0b00000000000

Register Name	Receive GLBSM Per-Lane STAT1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#0.PLREGS.RX_GLBSM_PL_STAT1_O_PL
Address	8003280009010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Per-Lane STAT1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#1.PLREGS.RX_GLBSM_PL_STAT1_O_PL
Address	8003280109010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Per-Lane STAT1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#2.PLREGS.RX_GLBSM_PL_STAT1_O_PL
Address	8003280209010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Per-Lane STAT1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#3.PLREGS.RX_GLBSM_PL_STAT1_O_PL
Address	8003280309010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Per-Lane STAT1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#4.PLREGS.RX_GLBSM_PL_STAT1_O_PL
Address	8003280409010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Per-Lane STAT1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#5.PLREGS.RX_GLBSM_PL_STAT1_O_PL
Address	8003280509010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Per-Lane STAT1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#6.PLREGS.RX_GLBSM_PL_STAT1_O_PL
Address	8003280609010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	**Receive GLBSM Per-Lane STAT1 O Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#7.PLREGS.RX_GLBSM_PL_STAT1_O_PL
Address	8003280709010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	**Receive GLBSM Per-Lane STAT1 O Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#8.PLREGS.RX_GLBSM_PL_STAT1_O_PL
Address	8003280809010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	**Receive GLBSM Per-Lane STAT1 O Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#9.PLREGS.RX_GLBSM_PL_STAT1_O_PL
Address	8003280909010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Per-Lane STAT1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#10.PLREGS.RX_GLBSM_PL_STAT1_O_PL
Address	8003280A09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Per-Lane STAT1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#11.PLREGS.RX_GLBSM_PL_STAT1_O_PL
Address	8003280B09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Per-Lane STAT1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#12.PLREGS.RX_GLBSM_PL_STAT1_O_PL
Address	8003280C09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Per-Lane STAT1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#13.PLREGS.RX_GLBSM_PL_STAT1_O_PL
Address	8003280D09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Per-Lane STAT1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#14.PLREGS.RX_GLBSM_PL_STAT1_O_PL
Address	8003280E09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Per-Lane STAT1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#15.PLREGS.RX_GLBSM_PL_STAT1_O_PL
Address	8003280F09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Per-Lane STAT1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#16.PLREGS.RX_GLBSM_PL_STAT1_O_PL
Address	8003281009010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Per-Lane STAT1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#17.PLREGS.RX_GLBSM_PL_STAT1_O_PL
Address	8003281109010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Per-Lane STAT1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#18.PLREGS.RX_GLBSM_PL_STAT1_O_PL
Address	8003281209010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Per-Lane STAT1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#19.PLREGS.RX_GLBSM_PL_STAT1_O_PL
Address	8003281309010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Per-Lane STAT1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#20.PLREGS.RX_GLBSM_PL_STAT1_O_PL
Address	8003281409010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Per-Lane STAT1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#21.PLREGS.RX_GLBSM_PL_STAT1_O_PL
Address	8003281509010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Per-Lane STAT1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#22.PLREGS.RX_GLBSM_PL_STAT1_O_PL
Address	8003281609010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Per-Lane STAT1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#23.PLREGS.RX_GLBSM_PL_STAT1_O_PL
Address	8003281709010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Per-Lane CNTL1X O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#0.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL
Address	8003300009010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Per-Lane CNTL1X O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#1.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL
Address	8003300109010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Per-Lane CNTL1X O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#2.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL
Address	8003300209010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Per-Lane CNTL1X O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#3.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL
Address	8003300309010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Per-Lane CNTL1X O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#4.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL
Address	8003300409010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Per-Lane CNTL1X O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#5.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL
Address	8003300509010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Per-Lane CNTL1X O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#6.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL
Address	8003300609010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Per-Lane CNTL1X O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#7.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL
Address	8003300709010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Per-Lane CNTL1X O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#8.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL
Address	8003300809010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Per-Lane CNTL1X O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#9.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL
Address	8003300909010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Per-Lane CNTL1X O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#10.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL
Address	8003300A09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Per-Lane CNTL1X O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#11.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL
Address	8003300B09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Per-Lane CNTL1X O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#12.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL
Address	8003300C09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Per-Lane CNTL1X O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#13.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL
Address	8003300D09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Per-Lane CNTL1X O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#14.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL
Address	8003300E09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Per-Lane CNTL1X O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#15.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL
Address	8003300F09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Per-Lane CNTL1X O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#16.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL
Address	8003301009010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Per-Lane CNTL1X O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#17.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL
Address	8003301109010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Per-Lane CNTL1X O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#18.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL
Address	8003301209010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Per-Lane CNTL1X O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#19.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL
Address	8003301309010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Per-Lane CNTL1X O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#20.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL
Address	8003301409010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive GLBSM Per-Lane CNTL1X O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#21.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL
Address	8003301509010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	**Receive GLBSM Per-Lane CNTL1X O Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#22.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL
Address	8003301609010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	**Receive GLBSM Per-Lane CNTL1X O Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.SLICE#23.PLREGS.RX_GLBSM_PL_CNTL1X_O_PL
Address	8003301709010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	**Receive Data Work Spare Mode Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#0.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	8003800009010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#1.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	8003800109010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#2.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	8003800209010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#3.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	8003800309010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#4.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	8003800409010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#5.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	8003800509010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#6.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	8003800609010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Data Work Spare Mode Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#7.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	8003800709010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Data Work Spare Mode Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#8.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	8003800809010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Data Work Spare Mode Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#9.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	8003800909010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Data Work Spare Mode Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#10.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	8003800A09010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Data Work Spare Mode Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#11.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	8003800B09010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#12.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	8003800C09010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#13.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	8003800D09010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Data Work Spare Mode Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#14.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	8003800E09010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Receive Data Work Spare Mode Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#15.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	8003800F09010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#16.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	8003801009010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#17.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	8003801109010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#18.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	8003801209010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#19.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	8003801309010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#20.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	8003801409010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#21.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	8003801509010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#22.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	8003801609010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Data Work Spare Mode Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#23.RX_WORK_REGS.RX_DATA_WORK_SPARE_MODE_PL
Address	8003801709010C3F (SCOM)
Description	This register contains per-lane spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_DATA_WORK_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_DATA_WORK_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_DATA_WORK_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_DATA_WORK_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_DATA_WORK_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_DATA_WORK_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_DATA_WORK_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_DATA_WORK_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#0.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	8003880009010C3F (SCOM)
Description	This register contains the RX BIST error status.

Bits	SCOM	Field Mnemonic: Description
0:60	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000
61	RWX	RX_BIST_ERR_A: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank A. 0b0 = No error. 0b1 = An error occurred during RXBIST.
62	RWX	RX_BIST_ERR_B: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank B. 0b0 = No error. 0b1 = An error occurred during RXBIST.
63	RWX	RX_BIST_ERR_E: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank E. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#1.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	8003880109010C3F (SCOM)
Description	This register contains the RX BIST error status.

Bits	SCOM	Field Mnemonic: Description
0:60	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000
61	RWX	RX_BIST_ERR_A: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank A. 0b0 = No error. 0b1 = An error occurred during RXBIST.
62	RWX	RX_BIST_ERR_B: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank B. 0b0 = No error. 0b1 = An error occurred during RXBIST.
63	RWX	RX_BIST_ERR_E: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank E. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#2.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	8003880209010C3F (SCOM)
Description	This register contains the RX BIST error status.

Bits	SCOM	Field Mnemonic: Description
0:60	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000
61	RWX	RX_BIST_ERR_A:This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank A. 0b0 = No error. 0b1 = An error occurred during RXBIST.
62	RWX	RX_BIST_ERR_B: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank B. 0b0 = No error. 0b1 = An error occurred during RXBIST.
63	RWX	RX_BIST_ERR_E: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank E. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#3.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	8003880309010C3F (SCOM)
Description	This register contains the RX BIST error status.

Bits	SCOM	Field Mnemonic: Description
0:60	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
61	RWX	RX_BIST_ERR_A: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank A. 0b0 = No error. 0b1 = An error occurred during RXBIST.
62	RWX	RX_BIST_ERR_B: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank B. 0b0 = No error. 0b1 = An error occurred during RXBIST.
63	RWX	RX_BIST_ERR_E: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank E. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	**Receive Work STAT1 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#4.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	8003880409010C3F (SCOM)
Description	This register contains the RX BIST error status.

Bits	SCOM	Field Mnemonic: Description
0:60	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000
61	RWX	RX_BIST_ERR_A: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank A. 0b0 = No error. 0b1 = An error occurred during RXBIST.
62	RWX	RX_BIST_ERR_B: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank B. 0b0 = No error. 0b1 = An error occurred during RXBIST.
63	RWX	RX_BIST_ERR_E: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank E. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	**Receive Work STAT1 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#5.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	8003880509010C3F (SCOM)
Description	This register contains the RX BIST error status.

Bits	SCOM	Field Mnemonic: Description
0:60	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000
61	RWX	RX_BIST_ERR_A: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank A. 0b0 = No error. 0b1 = An error occurred during RXBIST.
62	RWX	RX_BIST_ERR_B: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank B. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Bits	SCOM	Field Mnemonic: Description
63	RWX	RX_BIST_ERR_E: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank E. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#6.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	8003880609010C3F (SCOM)
Description	This register contains the RX BIST error status.

Bits	SCOM	Field Mnemonic: Description
0:60	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000
61	RWX	RX_BIST_ERR_A: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank A. 0b0 = No error. 0b1 = An error occurred during RXBIST.
62	RWX	RX_BIST_ERR_B: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank B. 0b0 = No error. 0b1 = An error occurred during RXBIST.
63	RWX	RX_BIST_ERR_E: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank E. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#7.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	8003880709010C3F (SCOM)
Description	This register contains the RX BIST error status.

Bits	SCOM	Field Mnemonic: Description
0:60	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000
61	RWX	RX_BIST_ERR_A: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank A. 0b0 = No error. 0b1 = An error occurred during RXBIST.
62	RWX	RX_BIST_ERR_B: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank B. 0b0 = No error. 0b1 = An error occurred during RXBIST.
63	RWX	RX_BIST_ERR_E: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank E. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#8.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	8003880809010C3F (SCOM)
Description	This register contains the RX BIST error status.

Bits	SCOM	Field Mnemonic: Description
0:60	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000
61	RWX	RX_BIST_ERR_A: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank A. 0b0 = No error. 0b1 = An error occurred during RXBIST.
62	RWX	RX_BIST_ERR_B: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank B. 0b0 = No error. 0b1 = An error occurred during RXBIST.
63	RWX	RX_BIST_ERR_E: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank E. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#9.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	8003880909010C3F (SCOM)
Description	This register contains the RX BIST error status.

Bits	SCOM	Field Mnemonic: Description
0:60	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000
61	RWX	RX_BIST_ERR_A: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank A. 0b0 = No error. 0b1 = An error occurred during RXBIST.
62	RWX	RX_BIST_ERR_B: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank B. 0b0 = No error. 0b1 = An error occurred during RXBIST.
63	RWX	RX_BIST_ERR_E: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank E. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#10.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	8003880A09010C3F (SCOM)
Description	This register contains the RX BIST error status.

Bits	SCOM	Field Mnemonic: Description
0:60	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
61	RWX	RX_BIST_ERR_A: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank A. 0b0 = No error. 0b1 = An error occurred during RXBIST.
62	RWX	RX_BIST_ERR_B: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank B. 0b0 = No error. 0b1 = An error occurred during RXBIST.
63	RWX	RX_BIST_ERR_E: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank E. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	**Receive Work STAT1 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#11.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	8003880B09010C3F (SCOM)
Description	This register contains the RX BIST error status.

Bits	SCOM	Field Mnemonic: Description
0:60	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000
61	RWX	RX_BIST_ERR_A: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank A. 0b0 = No error. 0b1 = An error occurred during RXBIST.
62	RWX	RX_BIST_ERR_B: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank B. 0b0 = No error. 0b1 = An error occurred during RXBIST.
63	RWX	RX_BIST_ERR_E: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank E. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	**Receive Work STAT1 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#12.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	8003880C09010C3F (SCOM)
Description	This register contains the RX BIST error status.

Bits	SCOM	Field Mnemonic: Description
0:60	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000
61	RWX	RX_BIST_ERR_A: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank A. 0b0 = No error. 0b1 = An error occurred during RXBIST.
62	RWX	RX_BIST_ERR_B: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank B. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Bits	SCOM	Field Mnemonic: Description
63	RWX	RX_BIST_ERR_E: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank E. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#13.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	8003880D09010C3F (SCOM)
Description	This register contains the RX BIST error status.

Bits	SCOM	Field Mnemonic: Description
0:60	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000
61	RWX	RX_BIST_ERR_A: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank A. 0b0 = No error. 0b1 = An error occurred during RXBIST.
62	RWX	RX_BIST_ERR_B: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank B. 0b0 = No error. 0b1 = An error occurred during RXBIST.
63	RWX	RX_BIST_ERR_E: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank E. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#14.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	8003880E09010C3F (SCOM)
Description	This register contains the RX BIST error status.

Bits	SCOM	Field Mnemonic: Description
0:60	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000
61	RWX	RX_BIST_ERR_A: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank A. 0b0 = No error. 0b1 = An error occurred during RXBIST.
62	RWX	RX_BIST_ERR_B: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank B. 0b0 = No error. 0b1 = An error occurred during RXBIST.
63	RWX	RX_BIST_ERR_E: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank E. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#15.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	8003880F09010C3F (SCOM)
Description	This register contains the RX BIST error status.

Bits	SCOM	Field Mnemonic: Description
0:60	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000
61	RWX	RX_BIST_ERR_A: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank A. 0b0 = No error. 0b1 = An error occurred during RXBIST.
62	RWX	RX_BIST_ERR_B: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank B. 0b0 = No error. 0b1 = An error occurred during RXBIST.
63	RWX	RX_BIST_ERR_E: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank E. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#16.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	8003881009010C3F (SCOM)
Description	This register contains the RX BIST error status.

Bits	SCOM	Field Mnemonic: Description
0:60	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000
61	RWX	RX_BIST_ERR_A: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank A. 0b0 = No error. 0b1 = An error occurred during RXBIST.
62	RWX	RX_BIST_ERR_B: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank B. 0b0 = No error. 0b1 = An error occurred during RXBIST.
63	RWX	RX_BIST_ERR_E: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank E. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#17.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	8003881109010C3F (SCOM)
Description	This register contains the RX BIST error status.

Bits	SCOM	Field Mnemonic: Description
0:60	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
61	RWX	RX_BIST_ERR_A: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank A. 0b0 = No error. 0b1 = An error occurred during RXBIST.
62	RWX	RX_BIST_ERR_B: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank B. 0b0 = No error. 0b1 = An error occurred during RXBIST.
63	RWX	RX_BIST_ERR_E: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank E. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#18.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	8003881209010C3F (SCOM)
Description	This register contains the RX BIST error status.

Bits	SCOM	Field Mnemonic: Description
0:60	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000
61	RWX	RX_BIST_ERR_A: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank A. 0b0 = No error. 0b1 = An error occurred during RXBIST.
62	RWX	RX_BIST_ERR_B: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank B. 0b0 = No error. 0b1 = An error occurred during RXBIST.
63	RWX	RX_BIST_ERR_E: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank E. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#19.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	8003881309010C3F (SCOM)
Description	This register contains the RX BIST error status.

Bits	SCOM	Field Mnemonic: Description
0:60	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000
61	RWX	RX_BIST_ERR_A: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank A. 0b0 = No error. 0b1 = An error occurred during RXBIST.
62	RWX	RX_BIST_ERR_B: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank B. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Bits	SCOM	Field Mnemonic: Description
63	RWX	RX_BIST_ERR_E: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank E. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#20.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	8003881409010C3F (SCOM)
Description	This register contains the RX BIST error status.

Bits	SCOM	Field Mnemonic: Description
0:60	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000
61	RWX	RX_BIST_ERR_A: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank A. 0b0 = No error. 0b1 = An error occurred during RXBIST.
62	RWX	RX_BIST_ERR_B: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank B. 0b0 = No error. 0b1 = An error occurred during RXBIST.
63	RWX	RX_BIST_ERR_E: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank E. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#21.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	8003881509010C3F (SCOM)
Description	This register contains the RX BIST error status.

Bits	SCOM	Field Mnemonic: Description
0:60	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000
61	RWX	RX_BIST_ERR_A: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank A. 0b0 = No error. 0b1 = An error occurred during RXBIST.
62	RWX	RX_BIST_ERR_B: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank B. 0b0 = No error. 0b1 = An error occurred during RXBIST.
63	RWX	RX_BIST_ERR_E: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank E. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#22.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	8003881609010C3F (SCOM)
Description	This register contains the RX BIST error status.

Bits	SCOM	Field Mnemonic: Description
0:60	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000
61	RWX	RX_BIST_ERR_A: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank A. 0b0 = No error. 0b1 = An error occurred during RXBIST.
62	RWX	RX_BIST_ERR_B: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank B. 0b0 = No error. 0b1 = An error occurred during RXBIST.
63	RWX	RX_BIST_ERR_E: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank E. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT1 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#23.RX_WORK_REGS.RX_WORK_STAT1_EO_PL
Address	8003881709010C3F (SCOM)
Description	This register contains the RX BIST error status.

Bits	SCOM	Field Mnemonic: Description
0:60	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000
61	RWX	RX_BIST_ERR_A: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank A. 0b0 = No error. 0b1 = An error occurred during RXBIST.
62	RWX	RX_BIST_ERR_B: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank B. 0b0 = No error. 0b1 = An error occurred during RXBIST.
63	RWX	RX_BIST_ERR_E: This bit indicates that the RXBIST did not find two data eyes of sufficient width while testing bank E. 0b0 = No error. 0b1 = An error occurred during RXBIST.

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#0.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	8003900009010C3F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RWX	RX_B_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank B. Not less than rx_ap110_ap010_delta_max.
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RWX	RX_B_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank B. This limit is used instead of the kH1/Ap value.
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#1.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	8003900109010C3F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RWX	RX_B_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank B. Not less than rx_ap110_ap010_delta_max.
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RWX	RX_B_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank B. This limit is used instead of the kH1/Ap value.
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#2.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	8003900209010C3F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RWX	RX_B_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank B. Not less than rx_ap110_ap010_delta_max.
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.

Bits	SCOM	Field Mnemonic: Description
51	RWX	RX_B_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank B. This limit is used instead of the kH1/Ap value.
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#3.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	8003900309010C3F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RWX	RX_B_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank B. Not less than rx_ap110_ap010_delta_max.
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RWX	RX_B_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank B. This limit is used instead of the kH1/Ap value.
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#4.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	8003900409010C3F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RWX	RX_B_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank B. Not less than rx_ap110_ap010_delta_max.
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RWX	RX_B_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank B. This limit is used instead of the kH1/Ap value.
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#5.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	8003900509010C3F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RWX	RX_B_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank B. Not less than rx_ap110_ap010_delta_max.
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RWX	RX_B_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank B. This limit is used instead of the kH1/Ap value.
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#6.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	8003900609010C3F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RWX	RX_B_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank B. Not less than rx_ap110_ap010_delta_max.
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RWX	RX_B_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank B. This limit is used instead of the kH1/Ap value.
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#7.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	8003900709010C3F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RWX	RX_B_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank B. Not less than rx_ap110_ap010_delta_max.
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RWX	RX_B_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank B. This limit is used instead of the kH1/Ap value.
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	**Receive Work STAT2 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#8.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	8003900809010C3F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RWX	RX_B_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank B. Not less than rx_ap110_ap010_delta_max.
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RWX	RX_B_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank B. This limit is used instead of the kH1/Ap value.
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	**Receive Work STAT2 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#9.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	8003900909010C3F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RWX	RX_B_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank B. Not less than rx_ap110_ap010_delta_max.
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.

Bits	SCOM	Field Mnemonic: Description
51	RWX	RX_B_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank B. This limit is used instead of the kH1/Ap value.
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#10.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	8003900A09010C3F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RWX	RX_B_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank B. Not less than rx_ap110_ap010_delta_max.
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RWX	RX_B_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank B. This limit is used instead of the kH1/Ap value.
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#11.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	8003900B09010C3F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RWX	RX_B_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank B. Not less than rx_ap110_ap010_delta_max.
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RWX	RX_B_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank B. This limit is used instead of the kH1/Ap value.
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#12.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	8003900C09010C3F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RWX	RX_B_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank B. Not less than rx_ap110_ap010_delta_max.
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RWX	RX_B_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank B. This limit is used instead of the kH1/Ap value.
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#13.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	8003900D09010C3F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RWX	RX_B_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank B. Not less than rx_ap110_ap010_delta_max.
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RWX	RX_B_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank B. This limit is used instead of the kH1/Ap value.
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#14.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	8003900E09010C3F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RWX	RX_B_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank B. Not less than rx_ap110_ap010_delta_max.
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RWX	RX_B_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank B. This limit is used instead of the kH1/Ap value.
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#15.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	8003900F09010C3F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RWX	RX_B_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank B. Not less than rx_ap110_ap010_delta_max.
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RWX	RX_B_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank B. This limit is used instead of the kH1/Ap value.
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#16.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	8003901009010C3F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RWX	RX_B_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank B. Not less than rx_ap110_ap010_delta_max.
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.

Bits	SCOM	Field Mnemonic: Description
51	RWX	RX_B_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank B. This limit is used instead of the kH1/Ap value.
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#17.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	8003901109010C3F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RWX	RX_B_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank B. Not less than rx_ap110_ap010_delta_max.
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RWX	RX_B_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank B. This limit is used instead of the kH1/Ap value.
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#18.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	8003901209010C3F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RWX	RX_B_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank B. Not less than rx_ap110_ap010_delta_max.
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RWX	RX_B_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank B. This limit is used instead of the kH1/Ap value.
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#19.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	8003901309010C3F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RWX	RX_B_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank B. Not less than rx_ap110_ap010_delta_max.
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RWX	RX_B_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank B. This limit is used instead of the kH1/Ap value.
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#20.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	8003901409010C3F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RWX	RX_B_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank B. Not less than rx_ap110_ap010_delta_max.
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RWX	RX_B_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank B. This limit is used instead of the kH1/Ap value.
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#21.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	8003901509010C3F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RWX	RX_B_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank B. Not less than rx_ap110_ap010_delta_max.
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RWX	RX_B_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank B. This limit is used instead of the kH1/Ap value.
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#22.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	8003901609010C3F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RWX	RX_B_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank B. Not less than rx_ap110_ap010_delta_max.
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.
51	RWX	RX_B_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank B. This limit is used instead of the kH1/Ap value.
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT2 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#23.RX_WORK_REGS.RX_WORK_STAT2_EO_PL
Address	8003901709010C3F (SCOM)
Description	This register contains eye-optimization status information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_A_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank A. Not less than rx_ap110_ap010_delta_max.
49	RWX	RX_B_BAD_DFE_CONV: The eye-optimization step failed DFD convergence on bank B. Not less than rx_ap110_ap010_delta_max.
50	RWX	RX_A_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank A. This limit is used instead of the kH1/Ap value.

Bits	SCOM	Field Mnemonic: Description
51	RWX	RX_B_H1AP_AT_LIMIT: The eye-optimization H1/Ap ratio limit hit bank B. This limit is used instead of the kH1/Ap value.
52:59	RWX	RX_A_AP: This field contains the eye-optimization stored Ap value.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#0.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	8003980009010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#1.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	8003980109010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#2.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	8003980209010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#3.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	8003980309010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#4.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	8003980409010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#5.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	8003980509010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#6.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	8003980609010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#7.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	8003980709010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#8.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	8003980809010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#9.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	8003980909010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#10.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	8003980A09010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#11.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	8003980B09010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#12.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	8003980C09010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#13.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	8003980D09010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#14.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	8003980E09010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#15.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	8003980F09010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#16.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	8003981009010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#17.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	8003981109010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#18.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	8003981209010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#19.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	8003981309010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#20.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	8003981409010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#21.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	8003981509010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#22.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	8003981609010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#23.RX_WORK_REGS.RX_WORK_STAT3_EO_PL
Address	8003981709010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_A_PATH_OFF_EVEN: This field contains the eye-optimization A bank even path offset.
54:59	RWX	RX_A_PATH_OFF_ODD: This field contains the eye-optimization A bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT4 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#0.RX_WORK_REGS.RX_WORK_STAT4_O_PL
Address	8003A00009010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_B_PATH_OFF_EVEN: This field contains the eye-optimization B bank even path offset.
54:59	RWX	RX_B_PATH_OFF_ODD: This field contains the eye-optimization B bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT4 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#1.RX_WORK_REGS.RX_WORK_STAT4_O_PL
Address	8003A00109010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_B_PATH_OFF_EVEN: This field contains the eye-optimization B bank even path offset.
54:59	RWX	RX_B_PATH_OFF_ODD: This field contains the eye-optimization B bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT4 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#2.RX_WORK_REGS.RX_WORK_STAT4_O_PL
Address	8003A00209010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_B_PATH_OFF_EVEN: This field contains the eye-optimization B bank even path offset.
54:59	RWX	RX_B_PATH_OFF_ODD: This field contains the eye-optimization B bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT4 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#3.RX_WORK_REGS.RX_WORK_STAT4_O_PL
Address	8003A00309010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_B_PATH_OFF_EVEN: This field contains the eye-optimization B bank even path offset.
54:59	RWX	RX_B_PATH_OFF_ODD: This field contains the eye-optimization B bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT4 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#4.RX_WORK_REGS.RX_WORK_STAT4_O_PL
Address	8003A00409010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_B_PATH_OFF_EVEN: This field contains the eye-optimization B bank even path offset.
54:59	RWX	RX_B_PATH_OFF_ODD: This field contains the eye-optimization B bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT4 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#5.RX_WORK_REGS.RX_WORK_STAT4_O_PL
Address	8003A00509010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_B_PATH_OFF_EVEN: This field contains the eye-optimization B bank even path offset.
54:59	RWX	RX_B_PATH_OFF_ODD: This field contains the eye-optimization B bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT4 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#6.RX_WORK_REGS.RX_WORK_STAT4_O_PL
Address	8003A00609010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_B_PATH_OFF_EVEN: This field contains the eye-optimization B bank even path offset.
54:59	RWX	RX_B_PATH_OFF_ODD: This field contains the eye-optimization B bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT4 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#7.RX_WORK_REGS.RX_WORK_STAT4_O_PL
Address	8003A00709010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_B_PATH_OFF_EVEN: This field contains the eye-optimization B bank even path offset.
54:59	RWX	RX_B_PATH_OFF_ODD: This field contains the eye-optimization B bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT4 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#8.RX_WORK_REGS.RX_WORK_STAT4_O_PL
Address	8003A00809010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_B_PATH_OFF_EVEN: This field contains the eye-optimization B bank even path offset.
54:59	RWX	RX_B_PATH_OFF_ODD: This field contains the eye-optimization B bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT4 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#9.RX_WORK_REGS.RX_WORK_STAT4_O_PL
Address	8003A00909010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_B_PATH_OFF_EVEN: This field contains the eye-optimization B bank even path offset.
54:59	RWX	RX_B_PATH_OFF_ODD: This field contains the eye-optimization B bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT4 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#10.RX_WORK_REGS.RX_WORK_STAT4_O_PL
Address	8003A00A09010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_B_PATH_OFF_EVEN: This field contains the eye-optimization B bank even path offset.
54:59	RWX	RX_B_PATH_OFF_ODD: This field contains the eye-optimization B bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT4 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#11.RX_WORK_REGS.RX_WORK_STAT4_O_PL
Address	8003A00B09010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_B_PATH_OFF_EVEN: This field contains the eye-optimization B bank even path offset.
54:59	RWX	RX_B_PATH_OFF_ODD: This field contains the eye-optimization B bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT4 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#12.RX_WORK_REGS.RX_WORK_STAT4_O_PL
Address	8003A00C09010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_B_PATH_OFF_EVEN: This field contains the eye-optimization B bank even path offset.
54:59	RWX	RX_B_PATH_OFF_ODD: This field contains the eye-optimization B bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT4 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#13.RX_WORK_REGS.RX_WORK_STAT4_O_PL
Address	8003A00D09010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_B_PATH_OFF_EVEN: This field contains the eye-optimization B bank even path offset.
54:59	RWX	RX_B_PATH_OFF_ODD: This field contains the eye-optimization B bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	**Receive Work STAT4 O Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#14.RX_WORK_REGS.RX_WORK_STAT4_O_PL
Address	8003A00E09010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	**SCOM**	**Field Mnemonic: Description**
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_B_PATH_OFF_EVEN: This field contains the eye-optimization B bank even path offset.
54:59	RWX	RX_B_PATH_OFF_ODD: This field contains the eye-optimization B bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	**Receive Work STAT4 O Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#15.RX_WORK_REGS.RX_WORK_STAT4_O_PL
Address	8003A00F09010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	**SCOM**	**Field Mnemonic: Description**
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_B_PATH_OFF_EVEN: This field contains the eye-optimization B bank even path offset.
54:59	RWX	RX_B_PATH_OFF_ODD: This field contains the eye-optimization B bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	**Receive Work STAT4 O Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#16.RX_WORK_REGS.RX_WORK_STAT4_O_PL
Address	8003A01009010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	**SCOM**	**Field Mnemonic: Description**
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_B_PATH_OFF_EVEN: This field contains the eye-optimization B bank even path offset.
54:59	RWX	RX_B_PATH_OFF_ODD: This field contains the eye-optimization B bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	**Receive Work STAT4 O Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#17.RX_WORK_REGS.RX_WORK_STAT4_O_PL
Address	8003A01109010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	**SCOM**	**Field Mnemonic: Description**
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RWX	RX_B_PATH_OFF_EVEN: This field contains the eye-optimization B bank even path offset.
54:59	RWX	RX_B_PATH_OFF_ODD: This field contains the eye-optimization B bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT4 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#18.RX_WORK_REGS.RX_WORK_STAT4_O_PL
Address	8003A01209010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_B_PATH_OFF_EVEN: This field contains the eye-optimization B bank even path offset.
54:59	RWX	RX_B_PATH_OFF_ODD: This field contains the eye-optimization B bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT4 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#19.RX_WORK_REGS.RX_WORK_STAT4_O_PL
Address	8003A01309010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_B_PATH_OFF_EVEN: This field contains the eye-optimization B bank even path offset.
54:59	RWX	RX_B_PATH_OFF_ODD: This field contains the eye-optimization B bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT4 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#20.RX_WORK_REGS.RX_WORK_STAT4_O_PL
Address	8003A01409010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_B_PATH_OFF_EVEN: This field contains the eye-optimization B bank even path offset.
54:59	RWX	RX_B_PATH_OFF_ODD: This field contains the eye-optimization B bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT4 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#21.RX_WORK_REGS.RX_WORK_STAT4_O_PL
Address	8003A01509010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_B_PATH_OFF_EVEN: This field contains the eye-optimization B bank even path offset.
54:59	RWX	RX_B_PATH_OFF_ODD: This field contains the eye-optimization B bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT4 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#22.RX_WORK_REGS.RX_WORK_STAT4_O_PL
Address	8003A01609010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_B_PATH_OFF_EVEN: This field contains the eye-optimization B bank even path offset.
54:59	RWX	RX_B_PATH_OFF_ODD: This field contains the eye-optimization B bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work STAT4 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#23.RX_WORK_REGS.RX_WORK_STAT4_O_PL
Address	8003A01709010C3F (SCOM)
Description	This register contains eye-optimization information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_B_PATH_OFF_EVEN: This field contains the eye-optimization B bank even path offset.
54:59	RWX	RX_B_PATH_OFF_ODD: This field contains the eye-optimization B bank odd path offset.
60:63	RO	constant = 0b0000

Register Name	Receive Work Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#0.RX_WORK_REGS.RX_WORK_CNTL1_O_PL
Address	8003A80009010C3F (SCOM)
Description	This register is used to reset the work registers of a single slice.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	RX_WORK_REGS_IORESET: Set this bit to reset the work registers of a single slice.
49:63	RO	constant = 0b000000000000000

Register Name	Receive Work Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#1.RX_WORK_REGS.RX_WORK_CNTL1_O_PL
Address	8003A80109010C3F (SCOM)
Description	This register is used to reset the work registers of a single slice.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_WORK_REGS_IORESET: Set this bit to reset the work registers of a single slice.
49:63	RO	constant = 0b000000000000000

Register Name	Receive Work Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#2.RX_WORK_REGS.RX_WORK_CNTL1_O_PL
Address	8003A80209010C3F (SCOM)
Description	This register is used to reset the work registers of a single slice.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_WORK_REGS_IORESET: Set this bit to reset the work registers of a single slice.
49:63	RO	constant = 0b000000000000000

Register Name	Receive Work Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#3.RX_WORK_REGS.RX_WORK_CNTL1_O_PL
Address	8003A80309010C3F (SCOM)
Description	This register is used to reset the work registers of a single slice.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_WORK_REGS_IORESET: Set this bit to reset the work registers of a single slice.
49:63	RO	constant = 0b000000000000000

Register Name	Receive Work Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#4.RX_WORK_REGS.RX_WORK_CNTL1_O_PL
Address	8003A80409010C3F (SCOM)
Description	This register is used to reset the work registers of a single slice.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_WORK_REGS_IORESET: Set this bit to reset the work registers of a single slice.
49:63	RO	constant = 0b000000000000000

Register Name	Receive Work Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#5.RX_WORK_REGS.RX_WORK_CNTL1_O_PL
Address	8003A80509010C3F (SCOM)
Description	This register is used to reset the work registers of a single slice.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_WORK_REGS_IORESET: Set this bit to reset the work registers of a single slice.
49:63	RO	constant = 0b000000000000000

Register Name	Receive Work Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#6.RX_WORK_REGS.RX_WORK_CNTL1_O_PL
Address	8003A80609010C3F (SCOM)
Description	This register is used to reset the work registers of a single slice.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_WORK_REGS_IORESET: Set this bit to reset the work registers of a single slice.
49:63	RO	constant = 0b000000000000000

Register Name	Receive Work Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#7.RX_WORK_REGS.RX_WORK_CNTL1_O_PL
Address	8003A80709010C3F (SCOM)
Description	This register is used to reset the work registers of a single slice.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_WORK_REGS_IORESET: Set this bit to reset the work registers of a single slice.
49:63	RO	constant = 0b000000000000000

Register Name	Receive Work Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#8.RX_WORK_REGS.RX_WORK_CNTL1_O_PL
Address	8003A80809010C3F (SCOM)
Description	This register is used to reset the work registers of a single slice.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_WORK_REGS_IORESET: Set this bit to reset the work registers of a single slice.
49:63	RO	constant = 0b000000000000000

Register Name	Receive Work Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#9.RX_WORK_REGS.RX_WORK_CNTL1_O_PL
Address	8003A80909010C3F (SCOM)
Description	This register is used to reset the work registers of a single slice.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_WORK_REGS_IORESET: Set this bit to reset the work registers of a single slice.
49:63	RO	constant = 0b000000000000000

Register Name	Receive Work Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#10.RX_WORK_REGS.RX_WORK_CNTL1_O_PL
Address	8003A80A09010C3F (SCOM)
Description	This register is used to reset the work registers of a single slice.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_WORK_REGS_IORESET: Set this bit to reset the work registers of a single slice.
49:63	RO	constant = 0b000000000000000

Register Name	Receive Work Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#11.RX_WORK_REGS.RX_WORK_CNTL1_O_PL
Address	8003A80B09010C3F (SCOM)
Description	This register is used to reset the work registers of a single slice.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_WORK_REGS_IORESET: Set this bit to reset the work registers of a single slice.
49:63	RO	constant = 0b000000000000000

Register Name	Receive Work Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#12.RX_WORK_REGS.RX_WORK_CNTL1_O_PL
Address	8003A80C09010C3F (SCOM)
Description	This register is used to reset the work registers of a single slice.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_WORK_REGS_IORESET: Set this bit to reset the work registers of a single slice.
49:63	RO	constant = 0b000000000000000

Register Name	Receive Work Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#13.RX_WORK_REGS.RX_WORK_CNTL1_O_PL
Address	8003A80D09010C3F (SCOM)
Description	This register is used to reset the work registers of a single slice.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_WORK_REGS_IORESET: Set this bit to reset the work registers of a single slice.
49:63	RO	constant = 0b000000000000000

Register Name	Receive Work Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#14.RX_WORK_REGS.RX_WORK_CNTL1_O_PL
Address	8003A80E09010C3F (SCOM)
Description	This register is used to reset the work registers of a single slice.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_WORK_REGS_IORESET: Set this bit to reset the work registers of a single slice.
49:63	RO	constant = 0b000000000000000

Register Name	Receive Work Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#15.RX_WORK_REGS.RX_WORK_CNTL1_O_PL
Address	8003A80F09010C3F (SCOM)
Description	This register is used to reset the work registers of a single slice.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_WORK_REGS_IORESET: Set this bit to reset the work registers of a single slice.
49:63	RO	constant = 0b000000000000000

Register Name	Receive Work Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#16.RX_WORK_REGS.RX_WORK_CNTL1_O_PL
Address	8003A81009010C3F (SCOM)
Description	This register is used to reset the work registers of a single slice.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_WORK_REGS_IORESET: Set this bit to reset the work registers of a single slice.
49:63	RO	constant = 0b000000000000000

Register Name	Receive Work Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#17.RX_WORK_REGS.RX_WORK_CNTL1_O_PL
Address	8003A81109010C3F (SCOM)
Description	This register is used to reset the work registers of a single slice.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_WORK_REGS_IORESET: Set this bit to reset the work registers of a single slice.
49:63	RO	constant = 0b000000000000000

Register Name	Receive Work Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#18.RX_WORK_REGS.RX_WORK_CNTL1_O_PL
Address	8003A81209010C3F (SCOM)
Description	This register is used to reset the work registers of a single slice.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_WORK_REGS_IORESET: Set this bit to reset the work registers of a single slice.
49:63	RO	constant = 0b000000000000000

Register Name	Receive Work Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#19.RX_WORK_REGS.RX_WORK_CNTL1_O_PL
Address	8003A81309010C3F (SCOM)
Description	This register is used to reset the work registers of a single slice.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_WORK_REGS_IORESET: Set this bit to reset the work registers of a single slice.
49:63	RO	constant = 0b000000000000000

Register Name	Receive Work Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#20.RX_WORK_REGS.RX_WORK_CNTL1_O_PL
Address	8003A81409010C3F (SCOM)
Description	This register is used to reset the work registers of a single slice.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_WORK_REGS_IORESET: Set this bit to reset the work registers of a single slice.
49:63	RO	constant = 0b000000000000000

Register Name	Receive Work Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#21.RX_WORK_REGS.RX_WORK_CNTL1_O_PL
Address	8003A81509010C3F (SCOM)
Description	This register is used to reset the work registers of a single slice.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_WORK_REGS_IORESET: Set this bit to reset the work registers of a single slice.
49:63	RO	constant = 0b000000000000000

Register Name	Receive Work Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#22.RX_WORK_REGS.RX_WORK_CNTL1_O_PL
Address	8003A81609010C3F (SCOM)
Description	This register is used to reset the work registers of a single slice.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_WORK_REGS_IORESET: Set this bit to reset the work registers of a single slice.
49:63	RO	constant = 0b000000000000000

Register Name	Receive Work Control 1 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.RX0.RX_WORK_REGS_MAC.SLICE#23.RX_WORK_REGS.RX_WORK_CNTL1_O_PL
Address	8003A81709010C3F (SCOM)
Description	This register is used to reset the work registers of a single slice.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_WORK_REGS_IORESET: Set this bit to reset the work registers of a single slice.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#0.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_MODE1_PL
Address	8004040009010C3F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_PSAVE_REQ_DIS: This bit disables TX slice power gating from link-layer psav_req control.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57:59	RO	constant = 0b000
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	**Transmit Mode 1 Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#0.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_MODE1_PL
Address	8004040109010C3F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.

Bits	SCOM	Field Mnemonic: Description
52:53	RO	constant = 0b00
54	RWX	TX_PSAVE_REQ_DIS: This bit disables TX slice power gating from link-layer psav_req control.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57:59	RO	constant = 0b000
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#0.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_MODE1_PL
Address	8004040209010C3F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_PSAVE_REQ_DIS: This bit disables TX slice power gating from link-layer psav_req control.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57:59	RO	constant = 0b000
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#0.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_MODE1_PL
Address	8004040309010C3F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_PSAVE_REQ_DIS: This bit disables TX slice power gating from link-layer psav_req control.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57:59	RO	constant = 0b000
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#1.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_MODE1_PL
Address	8004040409010C3F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_PSAVE_REQ_DIS: This bit disables TX slice power gating from link-layer psav_req control.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57:59	RO	constant = 0b000
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	**Transmit Mode 1 Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#1.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_MODE1_PL
Address	8004040509010C3F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_PSAVE_REQ_DIS: This bit disables TX slice power gating from link-layer psav_req control.

Bits	SCOM	Field Mnemonic: Description
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57:59	RO	constant = 0b000
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#1.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_MODE1_PL
Address	8004040609010C3F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_PSAVE_REQ_DIS: This bit disables TX slice power gating from link-layer psav_req control.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57:59	RO	constant = 0b000
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#1.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_MODE1_PL
Address	8004040709010C3F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_PSAVE_REQ_DIS: This bit disables TX slice power gating from link-layer psav_req control.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57:59	RO	constant = 0b000
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#2.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_MODE1_PL
Address	8004040809010C3F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.

Bits	SCOM	Field Mnemonic: Description
50:51	RWX	TX_LANE_QUIESCE: This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_PSAVE_REQ_DIS: This bit disables TX slice power gating from link-layer psav_req control.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57:59	RO	constant = 0b000
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#2.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_MODE1_PL
Address	8004040909010C3F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_PSAVE_REQ_DIS: This bit disables TX slice power gating from link-layer psav_req control.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57:59	RO	constant = 0b000

Bits	SCOM	Field Mnemonic: Description
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#2.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_MODE1_PL
Address	8004040A09010C3F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_PSAVE_REQ_DIS: This bit disables TX slice power gating from link-layer psav_req control.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57:59	RO	constant = 0b000
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#2.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_MODE1_PL
Address	8004040B09010C3F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_PSAVE_REQ_DIS: This bit disables TX slice power gating from link-layer psav_req control.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57:59	RO	constant = 0b000
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#3.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_MODE1_PL
Address	8004040C09010C3F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00

Bits	SCOM	Field Mnemonic: Description
54	RWX	TX_PSAVE_REQ_DIS: This bit disables TX slice power gating from link-layer psav_req control.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57:59	RO	constant = 0b000
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#3.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_MODE1_PL
Address	8004040D09010C3F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_PSAVE_REQ_DIS: This bit disables TX slice power gating from link-layer psav_req control.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57:59	RO	constant = 0b000
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#3.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_MODE1_PL
Address	8004040E09010C3F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_PSAVE_REQ_DIS: This bit disables TX slice power gating from link-layer psav_req control.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57:59	RO	constant = 0b000
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#3.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_MODE1_PL
Address	8004040F09010C3F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).

Bits	SCOM	Field Mnemonic: Description
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_PSAVE_REQ_DIS: This bit disables TX slice power gating from link-layer psav_req control.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57:59	RO	constant = 0b000
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#4.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_MODE1_PL
Address	8004041009010C3F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_PSAVE_REQ_DIS: This bit disables TX slice power gating from link-layer psav_req control.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.

Bits	SCOM	Field Mnemonic: Description
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57:59	RO	constant = 0b000
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#4.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_MODE1_PL
Address	8004041109010C3F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_PSAVE_REQ_DIS: This bit disables TX slice power gating from link-layer psav_req control.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57:59	RO	constant = 0b000
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#4.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_MODE1_PL
Address	8004041209010C3F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_PSAVE_REQ_DIS: This bit disables TX slice power gating from link-layer psav_req control.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57:59	RO	constant = 0b000
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#4.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_MODE1_PL
Address	8004041309010C3F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.

Bits	SCOM	Field Mnemonic: Description
50:51	RWX	TX_LANE_QUIESCE: This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_PSAVE_REQ_DIS: This bit disables TX slice power gating from link-layer psav_req control.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57:59	RO	constant = 0b000
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_MODE1_PL
Address	8004041409010C3F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_PSAVE_REQ_DIS: This bit disables TX slice power gating from link-layer psav_req control.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57:59	RO	constant = 0b000

Bits	SCOM	Field Mnemonic: Description
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_MODE1_PL
Address	8004041509010C3F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_PSAVE_REQ_DIS: This bit disables TX slice power gating from link-layer psav_req control.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57:59	RO	constant = 0b000
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_MODE1_PL
Address	8004041609010C3F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00
54	RWX	TX_PSAVE_REQ_DIS: This bit disables TX slice power gating from link-layer psav_req control.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57:59	RO	constant = 0b000
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_MODE1_PL
Address	8004041709010C3F (SCOM)
Description	This register contains the first set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: This bit is used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. 0b0 = Lane powered up. 0b1 = Lane drive inhibited (tristated) and powered down (default).
49	RWX	TX_LANE_INVERT: This bit is used to invert the polarity of a lane. 0b0 = Normal lane polarity (default). 0b1 = Lane inverted.
50:51	RWX	TX_LANE_QUIESCE: This field is used to force the output of a lane to a particular logical value. 0b00 = Functional data (default). 0b01 = Quiesce lane to a static 0 value. 0b10 = Quiesce lane to a static 1 value. 0b11 = Tri-state lane output.
52:53	RO	constant = 0b00

Bits	SCOM	Field Mnemonic: Description
54	RWX	TX_PSAVE_REQ_DIS: This bit disables TX slice power gating from link-layer psav_req control.
55	RWX	TX_ERR_INJ_A_ENABLE: This bit enables the random bit error-injection pattern A for this lane (default). 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane.
56	RWX	TX_ERR_INJ_B_ENABLE: This bit enables the random bit error-injection pattern B for this lane (default). 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane.
57:59	RO	constant = 0b000
60	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
61	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
62	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
63	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#0.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C0009010C3F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:55	RO	constant = 0b00000
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RWX	TX_RXCAL: This bit sets the transmitter to drive vio/2 common mode on both legs. Use this control during far-end RX offset calibration.
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61:63	RO	constant = 0b000

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#0.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C0109010C3F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:55	RO	constant = 0b00000
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RWX	TX_RXCAL: This bit sets the transmitter to drive vio/2 common mode on both legs. Use this control during far-end RX offset calibration.
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61:63	RO	constant = 0b000

Register Name	**Transmit Mode 2 Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#0.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C0209010C3F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:55	RO	constant = 0b00000
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RWX	TX_RXCAL: This bit sets the transmitter to drive vio/2 common mode on both legs. Use this control during far-end RX offset calibration.
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61:63	RO	constant = 0b000

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#0.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C0309010C3F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:55	RO	constant = 0b00000
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RWX	TX_RXCAL: This bit sets the transmitter to drive vio/2 common mode on both legs. Use this control during far-end RX offset calibration.
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61:63	RO	constant = 0b000

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#1.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C0409010C3F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:55	RO	constant = 0b00000
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RWX	TX_RXCAL: This bit sets the transmitter to drive vio/2 common mode on both legs. Use this control during far-end RX offset calibration.
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.

Bits	SCOM	Field Mnemonic: Description
61:63	RO	constant = 0b000

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#1.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C0509010C3F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:55	RO	constant = 0b00000
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RWX	TX_RXCAL: This bit sets the transmitter to drive vio/2 common mode on both legs. Use this control during far-end RX offset calibration.
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61:63	RO	constant = 0b000

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#1.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C0609010C3F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:55	RO	constant = 0b00000
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.

Bits	SCOM	Field Mnemonic: Description
57	RWX	TX_RXCAL: This bit sets the transmitter to drive vio/2 common mode on both legs. Use this control during far-end RX offset calibration.
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61:63	RO	constant = 0b000

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#1.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C0709010C3F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:55	RO	constant = 0b00000
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RWX	TX_RXCAL: This bit sets the transmitter to drive vio/2 common mode on both legs. Use this control during far-end RX offset calibration.
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61:63	RO	constant = 0b000

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#2.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C0809010C3F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.

Bits	SCOM	Field Mnemonic: Description
51:55	RO	constant = 0b00000
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RWX	TX_RXCAL: This bit sets the transmitter to drive vio/2 common mode on both legs. Use this control during far-end RX offset calibration.
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61:63	RO	constant = 0b000

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#2.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C0909010C3F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:55	RO	constant = 0b00000
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RWX	TX_RXCAL: This bit sets the transmitter to drive vio/2 common mode on both legs. Use this control during far-end RX offset calibration.
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61:63	RO	constant = 0b000

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#2.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C0A09010C3F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:55	RO	constant = 0b00000
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RWX	TX_RXCAL: This bit sets the transmitter to drive vio/2 common mode on both legs. Use this control during far-end RX offset calibration.
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61:63	RO	constant = 0b000

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#2.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C0B09010C3F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:55	RO	constant = 0b00000
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RWX	TX_RXCAL: This bit sets the transmitter to drive vio/2 common mode on both legs. Use this control during far-end RX offset calibration.
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61:63	RO	constant = 0b000

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#3.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C0C09010C3F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:55	RO	constant = 0b00000
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RWX	TX_RXCAL: This bit sets the transmitter to drive vio/2 common mode on both legs. Use this control during far-end RX offset calibration.
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61:63	RO	constant = 0b000

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#3.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C0D09010C3F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:55	RO	constant = 0b00000
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RWX	TX_RXCAL: This bit sets the transmitter to drive vio/2 common mode on both legs. Use this control during far-end RX offset calibration.
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.

Bits	SCOM	Field Mnemonic: Description
61:63	RO	constant = 0b000

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#3.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C0E09010C3F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:55	RO	constant = 0b00000
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RWX	TX_RXCAL: This bit sets the transmitter to drive vio/2 common mode on both legs. Use this control during far-end RX offset calibration.
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61:63	RO	constant = 0b000

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#3.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C0F09010C3F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:55	RO	constant = 0b00000
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.

Bits	SCOM	Field Mnemonic: Description
57	RWX	TX_RXCAL: This bit sets the transmitter to drive vio/2 common mode on both legs. Use this control during far-end RX offset calibration.
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61:63	RO	constant = 0b000

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#4.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C1009010C3F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:55	RO	constant = 0b00000
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RWX	TX_RXCAL: This bit sets the transmitter to drive vio/2 common mode on both legs. Use this control during far-end RX offset calibration.
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61:63	RO	constant = 0b000

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#4.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C1109010C3F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.

Bits	SCOM	Field Mnemonic: Description
51:55	RO	constant = 0b00000
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RWX	TX_RXCAL: This bit sets the transmitter to drive vio/2 common mode on both legs. Use this control during far-end RX offset calibration.
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61:63	RO	constant = 0b000

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#4.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C1209010C3F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:55	RO	constant = 0b00000
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RWX	TX_RXCAL: This bit sets the transmitter to drive vio/2 common mode on both legs. Use this control during far-end RX offset calibration.
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61:63	RO	constant = 0b000

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#4.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C1309010C3F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:55	RO	constant = 0b00000
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RWX	TX_RXCAL: This bit sets the transmitter to drive vio/2 common mode on both legs. Use this control during far-end RX offset calibration.
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61:63	RO	constant = 0b000

Register Name	**Transmit Mode 2 Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C1409010C3F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:55	RO	constant = 0b00000
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RWX	TX_RXCAL: This bit sets the transmitter to drive vio/2 common mode on both legs. Use this control during far-end RX offset calibration.
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61:63	RO	constant = 0b000

Register Name	**Transmit Mode 2 Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C1509010C3F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:55	RO	constant = 0b00000
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RWX	TX_RXCAL: This bit sets the transmitter to drive vio/2 common mode on both legs. Use this control during far-end RX offset calibration.
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61:63	RO	constant = 0b000

Register Name	**Transmit Mode 2 Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C1609010C3F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:55	RO	constant = 0b00000
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RWX	TX_RXCAL: This bit sets the transmitter to drive vio/2 common mode on both legs. Use this control during far-end RX offset calibration.
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.

Bits	SCOM	Field Mnemonic: Description
61:63	RO	constant = 0b000

Register Name	Transmit Mode 2 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_MODE2_PL
Address	80040C1709010C3F (SCOM)
Description	This register contains the second set of transmit mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay as follows: 0b000 = 0 to 2 UI. 0b001 = 4 to 6 UI (default). 0b010 = 8 to 10 UI. 0b011 = 12 to 14 UI. 0b100 = 16 to 18 UI. 0b101 = 20 to 22 UI. 0b110 = 24 to 26 UI. 0b111 = 28 to 30 UI.
51:55	RO	constant = 0b00000
56	RWX	TX_UNLOAD_CLK_DISABLE: This bit is set to 0 to enable synchronization of the TX custom serializer via the tx_fifo_init register. It is set to 1 to clock off the synchronization logic and save power.
57	RWX	TX_RXCAL: This bit sets the transmitter to drive vio/2 common mode on both legs. Use this control during far-end RX offset calibration.
58:60	RWX	TX_UNLOAD_SEL: This field controls the preset value of the TX slice unload counter, which effectively gives it subcycle control of the offset of the TX unload clock from the grid clock.
61:63	RO	constant = 0b000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#0.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	8004140009010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54:63	RO	constant = 0b0000000000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#0.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	8004140109010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54:63	RO	constant = 0b0000000000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#0.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	8004140209010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54:63	RO	constant = 0b0000000000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#0.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	8004140309010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54:63	RO	constant = 0b0000000000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#1.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	8004140409010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54:63	RO	constant = 0b0000000000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#1.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	8004140509010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54:63	RO	constant = 0b0000000000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#1.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	8004140609010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54:63	RO	constant = 0b0000000000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#1.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	8004140709010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54:63	RO	constant = 0b0000000000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#2.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	8004140809010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54:63	RO	constant = 0b0000000000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#2.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	8004140909010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54:63	RO	constant = 0b0000000000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#2.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	8004140A09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54:63	RO	constant = 0b0000000000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#2.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	8004140B09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54:63	RO	constant = 0b0000000000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#3.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	8004140C09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54:63	RO	constant = 0b0000000000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#3.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	8004140D09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54:63	RO	constant = 0b0000000000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#3.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	8004140E09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54:63	RO	constant = 0b0000000000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#3.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	8004140F09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54:63	RO	constant = 0b0000000000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#4.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	8004141009010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54:63	RO	constant = 0b0000000000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#4.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	8004141109010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54:63	RO	constant = 0b0000000000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#4.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	8004141209010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54:63	RO	constant = 0b0000000000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#4.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	8004141309010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54:63	RO	constant = 0b0000000000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	8004141409010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54:63	RO	constant = 0b0000000000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	8004141509010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54:63	RO	constant = 0b0000000000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	8004141609010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54:63	RO	constant = 0b0000000000

Register Name	Transmit CNTL1G Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_CNTL1G_PL
Address	8004141709010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	NCX	Reserved field.
53	NCX	Reserved field.
54:63	RO	constant = 0b0000000000

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#0.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C0009010C3F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#0.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C0109010C3F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	TX_LANE_BIST_ERR: Indicates TXBIST has found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#0.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C0209010C3F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#0.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C0309010C3F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.

Bits	SCOM	Field Mnemonic: Description
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#1.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C0409010C3F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#1.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C0509010C3F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	**Transmit STAT1 Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#1.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C0609010C3F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	**SCOM**	**Field Mnemonic: Description**
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	**Transmit STAT1 Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#1.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C0709010C3F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	**SCOM**	**Field Mnemonic: Description**
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	**Transmit STAT1 Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#2.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C0809010C3F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	**SCOM**	**Field Mnemonic: Description**
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#2.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C0909010C3F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#2.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C0A09010C3F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.

Bits	SCOM	Field Mnemonic: Description
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#2.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C0B09010C3F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#3.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C0C09010C3F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#3.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C0D09010C3F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#3.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C0E09010C3F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#3.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C0F09010C3F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#4.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C1009010C3F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#4.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C1109010C3F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.

Bits	SCOM	Field Mnemonic: Description
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#4.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C1209010C3F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#4.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C1309010C3F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C1409010C3F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C1509010C3F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C1609010C3F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit STAT1 Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_STAT1_PL
Address	80041C1709010C3F (SCOM)
Description	This register contains the first set of transmit status fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: This bit indicates whether TXBIST found an error. 0b0 = No error. 0b1 = An error was found during TXBIST.
49	RWX	TX_LANE_BIST_ACTVITY_DET: This bit indicates whether activity was detected in the PRBS checker. 0b0 = No activity. 0b1 = Activity was found during TXBIST.
50:51	RWX	TX_SEG_TEST_STATUS: This field contains the driver segment test result. Bit 0 is used for PAD P. Bit 1 is used for PAD N.
52:62	RO	constant = 0b00000000000
63	ROX	Reserved field.

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#0.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_PL
Address	8004240009010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#0.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_PL
Address	8004240109010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#0.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_PL
Address	8004240209010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#0.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_PL
Address	8004240309010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#1.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_PL
Address	8004240409010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	**Transmit FIR Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#1.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_PL
Address	8004240509010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	**Transmit FIR Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#1.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_PL
Address	8004240609010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	**Transmit FIR Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#1.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_PL
Address	8004240709010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	**Transmit FIR Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#2.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_PL
Address	8004240809010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#2.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_PL
Address	8004240909010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#2.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_PL
Address	8004240A09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#2.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_PL
Address	8004240B09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#3.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_PL
Address	8004240C09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#3.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_PL
Address	8004240D09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#3.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_PL
Address	8004240E09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#3.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_PL
Address	8004240F09010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#4.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_PL
Address	8004241009010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#4.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_PL
Address	8004241109010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#4.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_PL
Address	8004241209010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#4.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_PL
Address	8004241309010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_PL
Address	8004241409010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_PL
Address	8004241509010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_PL
Address	8004241609010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_PL
Address	8004241709010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Mask Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#0.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C0009010C3F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Mask Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#0.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C0109010C3F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Mask Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#0.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C0209010C3F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Mask Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#0.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C0309010C3F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Mask Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#1.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C0409010C3F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.

Bits	SCOM	Field Mnemonic: Description
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Mask Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#1.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C0509010C3F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Mask Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#1.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C0609010C3F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Mask Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#1.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C0709010C3F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Mask Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#2.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C0809010C3F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Mask Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#2.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C0909010C3F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Mask Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#2.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C0A09010C3F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Mask Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#2.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C0B09010C3F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Mask Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#3.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C0C09010C3F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Mask Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#3.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C0D09010C3F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Mask Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#3.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C0E09010C3F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Mask Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#3.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C0F09010C3F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.

Bits	SCOM	Field Mnemonic: Description
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Mask Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#4.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C1009010C3F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Mask Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#4.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C1109010C3F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Mask Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#4.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C1209010C3F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Mask Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#4.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C1309010C3F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Mask Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C1409010C3F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Mask Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C1509010C3F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Mask Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C1609010C3F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Mask Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80042C1709010C3F (SCOM)
Description	This register masks transmit FIR per-lane errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: This bit is a FIR mask for all per-lane register, or per-lane state machine, parity errors.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#0.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	8004340009010C3F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#0.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	8004340109010C3F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#0.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	8004340209010C3F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.

Bits	SCOM	Field Mnemonic: Description
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#0.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	8004340309010C3F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#1.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	8004340409010C3F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#1.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	8004340509010C3F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#1.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	8004340609010C3F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#1.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	8004340709010C3F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#2.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	8004340809010C3F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#2.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	8004340909010C3F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#2.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	8004340A09010C3F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#2.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	8004340B09010C3F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#3.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	8004340C09010C3F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#3.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	8004340D09010C3F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.

Bits	SCOM	Field Mnemonic: Description
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#3.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	8004340E09010C3F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#3.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	8004340F09010C3F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#4.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	8004341009010C3F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#4.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	8004341109010C3F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#4.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	8004341209010C3F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#4.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	8004341309010C3F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	8004341409010C3F (SCOM)
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register	
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL	
Address	8004341509010C3F (SCOM)	
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.	
Bits	**SCOM**	**Field Mnemonic: Description**
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register	
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL	
Address	8004341609010C3F (SCOM)	
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.	
Bits	**SCOM**	**Field Mnemonic: Description**
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit FIR Error Inject Per-Lane Register	
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL	
Address	8004341709010C3F (SCOM)	
Description	This register is used to inject errors into the per-lane FIR Transmit Registers.	
Bits	**SCOM**	**Field Mnemonic: Description**
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: This bit is used for the tx_fir_error_inject_pl register.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL2 O Per-Lane Register	
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#0.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_CNTL2_O_PL	
Address	80044C0009010C3F (SCOM)	
Description	This register is used to reset the given transmit lane.	
Bits	**SCOM**	**Field Mnemonic: Description**
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_IORESET: This bit resets the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#0.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_CNTL2_O_PL
Address	80044C0109010C3F (SCOM)
Description	This register is used to reset the given transmit lane.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_IORESET: This bit resets the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#0.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_CNTL2_O_PL
Address	80044C0209010C3F (SCOM)
Description	This register is used to reset the given transmit lane.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_IORESET: This bit resets the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#0.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_CNTL2_O_PL
Address	80044C0309010C3F (SCOM)
Description	This register is used to reset the given transmit lane.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_IORESET: This bit resets the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#1.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_CNTL2_O_PL
Address	80044C0409010C3F (SCOM)
Description	This register is used to reset the given transmit lane.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_IORESET: This bit resets the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#1.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_CNTL2_O_PL
Address	80044C0509010C3F (SCOM)
Description	This register is used to reset the given transmit lane.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_IORESET: This bit resets the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#1.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_CNTL2_O_PL
Address	80044C0609010C3F (SCOM)
Description	This register is used to reset the given transmit lane.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_IORESET: This bit resets the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#1.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_CNTL2_O_PL
Address	80044C0709010C3F (SCOM)
Description	This register is used to reset the given transmit lane.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_IORESET: This bit resets the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#2.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_CNTL2_O_PL
Address	80044C0809010C3F (SCOM)
Description	This register is used to reset the given transmit lane.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_IORESET: This bit resets the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#2.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_CNTL2_O_PL
Address	80044C0909010C3F (SCOM)
Description	This register is used to reset the given transmit lane.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_IORESET: This bit resets the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#2.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_CNTL2_O_PL
Address	80044C0A09010C3F (SCOM)
Description	This register is used to reset the given transmit lane.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_IORESET: This bit resets the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#2.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_CNTL2_O_PL
Address	80044C0B09010C3F (SCOM)
Description	This register is used to reset the given transmit lane.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_IORESET: This bit resets the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#3.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_CNTL2_O_PL
Address	80044C0C09010C3F (SCOM)
Description	This register is used to reset the given transmit lane.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_IORESET: This bit resets the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#3.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_CNTL2_O_PL
Address	80044C0D09010C3F (SCOM)
Description	This register is used to reset the given transmit lane.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_IORESET: This bit resets the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#3.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_CNTL2_O_PL
Address	80044C0E09010C3F (SCOM)
Description	This register is used to reset the given transmit lane.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_IORESET: This bit resets the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#3.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_CNTL2_O_PL
Address	80044C0F09010C3F (SCOM)
Description	This register is used to reset the given transmit lane.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_IORESET: This bit resets the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#4.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_CNTL2_O_PL
Address	80044C1009010C3F (SCOM)
Description	This register is used to reset the given transmit lane.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_IORESET: This bit resets the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#4.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_CNTL2_O_PL
Address	80044C1109010C3F (SCOM)
Description	This register is used to reset the given transmit lane.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_IORESET: This bit resets the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#4.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_CNTL2_O_PL
Address	80044C1209010C3F (SCOM)
Description	This register is used to reset the given transmit lane.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_IORESET: This bit resets the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#4.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_CNTL2_O_PL
Address	80044C1309010C3F (SCOM)
Description	This register is used to reset the given transmit lane.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_IORESET: This bit resets the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_CNTL2_O_PL
Address	80044C1409010C3F (SCOM)
Description	This register is used to reset the given transmit lane.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_IORESET: This bit resets the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_CNTL2_O_PL
Address	80044C1509010C3F (SCOM)
Description	This register is used to reset the given transmit lane.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_IORESET: This bit resets the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_CNTL2_O_PL
Address	80044C1609010C3F (SCOM)
Description	This register is used to reset the given transmit lane.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_IORESET: This bit resets the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL2 O Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_CNTL2_O_PL
Address	80044C1709010C3F (SCOM)
Description	This register is used to reset the given transmit lane.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_IORESET: This bit resets the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#0.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	8004540009010C3F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#0.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	8004540109010C3F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#0.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	8004540209010C3F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#0.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	8004540309010C3F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#1.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	8004540409010C3F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#1.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	8004540509010C3F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#1.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	8004540609010C3F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#1.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	8004540709010C3F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#2.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	8004540809010C3F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#2.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	8004540909010C3F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#2.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	8004540A09010C3F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#2.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	8004540B09010C3F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#3.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	8004540C09010C3F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#3.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	8004540D09010C3F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#3.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	8004540E09010C3F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#3.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	8004540F09010C3F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#4.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	8004541009010C3F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#4.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	8004541109010C3F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#4.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	8004541209010C3F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#4.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	8004541309010C3F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	Transmit CNTL3 EO Per-Lane Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#0.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	8004541409010C3F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	**Transmit CNTL3 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#1.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	8004541509010C3F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	**Transmit CNTL3 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#2.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	8004541609010C3F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	**Transmit CNTL3 EO Per-Lane Register**
Mnemonic	IOO0.IOO_CPLT.TX0.TXPACKS#5.TXPACK.DD.SLICE#3.DD.TX_BIT_REGS.TX_CNTL3_EO_PL
Address	8004541709010C3F (SCOM)
Description	This register is used to enable TDR.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_TDR_ENABLE: This bit enables TDR on the given transmit lane.
49:63	RO	constant = 0b000000000000000

Register Name	**Receive Spare Mode Per-Group Register**
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_SPARE_MODE_PG
Address	8008000009010C3F (SCOM)
Description	This register contains per-group spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PG_SPARE_MODE_0: Per-group spare mode latch.
49	RWX	RX_PG_SPARE_MODE_1: Per-group spare mode latch.

Bits	SCOM	Field Mnemonic: Description
50	RWX	RX_PG_SPARE_MODE_2: Per-group spare mode latch.
51	RWX	RX_PG_SPARE_MODE_3: Per-group spare mode latch.
52	RWX	RX_PG_SPARE_MODE_4: This debug switch prevents the rx_sls_hndshk_state state machine and the rx_dyn_recal_hndshk_state state machine from ever being allowed to run at the same time. Setting this bit turns this feature off.
53:63	RO	constant = 0b00000000000

Register Name	Receive ID1 Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_ID1_PG
Address	8008080009010C3F (SCOM)
Description	This register is used to set the bus number of a clock group.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_BUS_ID: This field is used to programmatically set the bus number that a clock group belongs to.
54:63	RO	constant = 0b0000000000

Register Name	Receive CTL Mode 1 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE1_EO_PG
Address	8008100009010C3F (SCOM)
Description	This register contains the first set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_CLKDIST_PDWN: This field is used to disable the receive group clocks and put them into a low-power state. Bit 0 disables slices 0 - 7. Bit 1 disables slices 8 - 15. Bit 2 disables slices 16 - 23.
51:56	RWX	RX_BIST_MIN_EYE_WIDTH: Receive BIST minimum eye width. This field sets the minimum eye width value, in phase-rotator steps, that is considered acceptable in order to pass.
57	RWX	RX_A_BIST_EN: BIST enable pin.
58	RWX	RX_B_BIST_EN: BIST enable pin.
59	RWX	RX_E_BIST_EN: BIST enable pin.
60:61	RWX	RX_BISTCLK_EN: BIST clock enable pins.
62	RWX	RX_DISABLE_BANK_PDWN: This bit is used to disable power down of an unused (functionally) bank.
63	RO	constant = 0b0

Register Name	Receive CTL Mode 2 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE2_EO_PG
Address	8008180009010C3F (SCOM)
Description	This register contains the second set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_DFE_CA_CFG: Receive DFE clock adjustment settings. This 2-bit field contains an encoded value for K as follows: \n00 = 8 \n01 = 10 \n10 = 12 \n11 = 14 Lab testing is required to determine the proper value of K.
50:53	RWX	RX_SCOPE_CONTROL: This 4-bit value indicates which scope bit is being captured. Valid values are 0 - 9.
54	RO	constant = 0b0
55	RWX	RX_RECAL_REQ_DL_MASK: This bit masks rx_recal_req_dl primary inputs from the data layer.
56	RWX	RX_RECAL_DONE_DL_MASK: This bit masks rx_recal_done_dl primary inputs from the data layer.
57	RWX	RX_RUN_LANE_DL_MASK: This bit masks rx_run_lane_dl primary inputs from the data layer.
58	RWX	RX_RECAL_ABORT_DL_MASK: This bit masks rx_recal_abort_dl primary inputs from the data layer.
59	RWX	RX_INIT_DONE_DL_MASK: This bit masks rx_init_done_dl primary outputs to the data layer.
60	RWX	RX_DATA_PIPE_CLR_ON_READ_MODE: This bit sets the data pipe capture on read mode. When set, reading rx_data_pipe_16_31 automatically captures new data. Otherwise, rx_data_pipe_capture must be written.
61	RO	constant = 0b0
62:63	RWX	RX_CFG_LTE_MC:

Register Name	Receive CTL Mode 5 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE5_EO_PG
Address	8008300009010C3F (SCOM)
Description	This register contains the fifth set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56:59	RWX	RX_TRACKING_TIMEOUT_SEL: This field contains the time to wait for phase tracking to lock on the edge before proceeding in the state machine.
60:63	RO	constant = 0b0000

Register Name	Receive CTL Mode 6 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE6_EO_PG
Address	8008380009010C3F (SCOM)
Description	This register contains the sixth set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_EO_CONVERGED_END_COUNT: This field contains the end value of the receive eye-optimization convergence counter. This value represents the number of times through the vga + CTLE peaking substeps before giving up.
52:53	RWX	RX_HIST_MIN_EYE_WIDTH_MODE: This field indicates the receive historic eye width and height minimum measurement mode.
54:55	RWX	RX_HIST_MIN_EYE_HEIGHT_MODE: Receive historic eye-height minimum measurement mode. This field is inoperative on POWER8 processor with NVLink technology hardware. Use the rx_hist_min_eye_width_mode control instead. Set both the width and height_mode controls to the same value in test routines to maintain compatibility.
56:59	RWX	RX_AMP_GAIN_CNT_MAX: This field indicates the maximum number of attempts to adjust VGA gain before doing a peaking operation.
60:63	RO	constant = 0b0000

Register Name	Receive CTL Mode 7 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE7_EO_PG
Address	8008400009010C3F (SCOM)
Description	This register contains the seventh set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_ABORT_CHECK_TIMEOUT_SEL: This field selects the abort check timeout value.
52:55	RWX	RX_POLLING_TIMEOUT_SEL: This field selects the polling read timeout value.
56:63	RO	constant = 0b00000000

Register Name	Receive CTL Mode 9 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE9_EO_PG
Address	8008500009010C3F (SCOM)
Description	This register contains the ninth set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RX_MIN_EYE_WIDTH: This field indicates the minimum acceptable eye width used during initial or recalibration results checking. (EDI or EI4).
56:63	RWX	RX_MIN_EYE_HEIGHT: This field indicates the minimum acceptable eye height used during initial or recalibration results checking. (EDI only).

Register Name	Receive CTL Mode 10 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE10_EO_PG
Address	8008580009010C3F (SCOM)
Description	This register contains the tenth set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_AMP_INIT_CFG: This register controls the servo filter for amplitude measurements during initialization.
51:53	RWX	RX_AMP_RECAL_CFG: This register controls the servo filter for amplitude measurements during recalibration.
54:56	RWX	RX_PEAK_INIT_CFG: This register controls the servo filter for peaking during initialization.
57:59	RWX	RX_PEAK_RECAL_CFG: This register controls the servo filter for peaking during recalibration.
60:63	RWX	RX_AMP_CFG: This register controls the servo filter for rx_amp_0 and rx_amp_1 servo ops.

Register Name	Receive CTL Mode 11 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE11_EO_PG
Address	8008600009010C3F (SCOM)
Description	This register contains the 11th set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_OFF_INIT_CFG: This register controls the servo filter for offset measurements during initialization.
51:53	RWX	RX_OFF_RECAL_CFG: This register controls the servo filter for offset measurements during recalibration.
54:56	RWX	RX_CM_CFG: This register controls the servo during common-mode measurement.
57:59	RWX	RX_AMIN_CFG: This register controls the servo filtering used for amin measurements.
60:63	RWX	RX_USERDEF_CFG: This register controls the servo filtering when running the user-defined servo operations.

Register Name	Receive CTL Mode 12 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE12_EO_PG
Address	8008680009010C3F (SCOM)
Description	This register contains the 12th set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_SERVO_CHG_CFG: This register controls the minimum acceptable changes of the accumulator for a valid servo operation. It is used to assure that we have reached a stable point.
52:54	RWX	RX_DAC_BO_CFG: This register controls the time of the DAC black out time.
55:56	RWX	RX_FILTER_MODE: Servo filter mode. 00 = Normal filter during the entire operation. 01 = Use the 1/4 - 1/2 mode. 10 = 1/8 - 1/4 mode. 11 = Automatic convergence detect mode.
57:58	RWX	RX_MISC_CFG: These are per-group receive miscellaneous configuration bits. Bit 0 is used to re-enable the progressive filter mode for peaking. Bit 1, when 1, enables the clearing of H1 during the amp0, amp1, and user-defined servo operations.
59	RWX	RX_DISABLE_H1_CLEAR: Per group. When set, this bit disables the clearing when running servo operations that typically clear and restore the H1 registers.

Bits	SCOM	Field Mnemonic: Description
60:62	RWX	RX_VOFF_CFG: This is a per-group configuration register that is used for setting the filter value when running the VREF version of offset on edge latches.
63	RWX	RX_LOFF_AMP_EN: When set to 1, the amp DAC is enabled during the loff versions of local latch offset cancellation.

Register Name	Receive CTL Mode 13 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE13_EO_PG
Address	8008700009010C3F (SCOM)
Description	This register contains the 13^{th} set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant = 0b0000000000000000000000000000000000000000000000000
49:55	RWX	RX_CM_OFFSET_VAL: This field contains the value used to offset the amp DAC when running common mode.
56:59	RWX	RX_SERVO_THRESH1: This field contains the value used as a threshold of when to switch to normal filtering mode.
60:63	RWX	RX_SERVO_THRESH2: This field contains the value used as a threshold of when we think the servo has converged.

Register Name	Receive CTL Mode 14 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE14_EO_PG
Address	8008780009010C3F (SCOM)
Description	This register contains the 14^{th} set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_AMP_INIT_TIMEOUT: This field is used for amplitude measurements during initialization.
52:55	RWX	RX_AMP_RECAL_TIMEOUT: This field is used for amplitude measurements during recalibration.
56:59	RWX	RX_PEAK_INIT_TIMEOUT: This field is used for peaking measurements during initialization.
60:63	RWX	RX_PEAK_RECAL_TIMEOUT: This field is used for peaking measurements during recalibration

Register Name	Receive CTL Mode 15 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE15_EO_PG
Address	8008800009010C3F (SCOM)
Description	This register contains the 15^{th} set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_OFF_INIT_TIMEOUT: This field is used for offset measurements during initialization.
52:55	RWX	RX_OFF_RECAL_TIMEOUT: This field is used for offset measurements during recalibration.
56:59	RWX	RX_CM_TIMEOUT: This field is used for common-mode measurements.

Bits	SCOM	Field Mnemonic: Description
60:63	RWX	RX_AMIN_TIMEOUT: This field is used for Amin measurements.

Register Name	Receive CTL Mode 16 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE16_EO_PG
Address	8008880009010C3F (SCOM)
Description	This register contains the 16th set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_AMP_TIMEOUT: This timeout is used when running the generic amplitude servo operations.
52:55	RWX	RX_USERDEF_TIMEOUT: This timeout is used when using the user-defined servo operations.
56:59	RWX	RX_BER_TIMEOUT: This timeout is used when making bit error measurements with a servo operation.
60:63	RWX	RX_SPARE4_TIMEOUT: This timeout is currently a spare.

Register Name	Receive CTL Mode 17 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE17_EO_PG
Address	8008900009010C3F (SCOM)
Description	This register contains the 17th set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMAX_HIGH: This field contains the receive Amax high target in amplitude DAC steps (as measured by the 2Ap-Amin method). The default is d120.
56:63	RWX	RX_AMAX_LOW: This field contains the receive Amax low target in amplitude DAC steps (as measured by the 2Ap-Amin method). The default is d80.

Register Name	Receive CTL Mode 18 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE18_EO_PG
Address	8008980009010C3F (SCOM)
Description	This register contains the 18th set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMP0_FILTER_MASK: This register controls the filter and mask for the Amp_0 servo operations.
56:63	RWX	RX_AMP1_FILTER_MASK: This register controls the filter and mask for the Amp_1 servo operations.

Register Name	Receive CTL Mode 19 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE19_EO_PG
Address	8008A00009010C3F (SCOM)
Description	This register contains the 19th set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_CTLE_GAIN_MAX: This field contains the receive CTLE (VGA) gain maximum allowable gain value.
52:55	RO	constant = 0b0000
56:63	RWX	RX_AMP_START_VAL: This field contains the receive amp start value, used when making amplitude measurements as the starting point.

Register Name	Receive CTL Mode 20 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE20_EO_PG
Address	8008A80009010C3F (SCOM)
Description	This register contains the 20th set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_DFE_CONVERGED_CNT_MAX: This field contains the number of iterations through DFE H1 and kH1Ap adjustment before ending DFE, unless it is ended by the rx_ap110ap010_delta criteria being met.
52:55	RWX	RX_AP110_AP010_DELTA_MAX: This field contains the maximum delta between Apx110 and Apx010 measurements to end DFE H1 and kH1Ap adjustment, unless ended by dfe_converged_cnt_max.
56:63	RO	constant = 0b00000000

Register Name	Receive CTL Mode 21 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE21_EO_PG
Address	8008B00009010C3F (SCOM)
Description	This register contains the 21st set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_EO_ENABLE_INTEG_LATCH_OFFSET_CAL: This bit is the receive eye-optimization latch offset adjustment enable with an integrator-based disable.
49	RWX	RX_EO_ENABLE_CTLE_COARSE_CAL: This bit is the receive eye-optimization coarse CTLE/Peakin enable.
50	RWX	RX_EO_ENABLE_DAC_H1_CAL: This bit is the receive eye-optimization H! DAC calibration to reference.
51	RWX	RX_EO_ENABLE_VGA_CAL: This bit is the receive eye-optimization VGA gain and offset adjustment enable.
52	RWX	RX_EO_ENABLE_DFE_H1_CAL: This bit is the receive eye-optimization DFE H1 adjustment enable.
53	RWX	RX_EO_ENABLE_H1AP_TWEAK: This bit is the receive eye-optimization H1/AN PR adjust enable.
54	RWX	RX_EO_ENABLE_DDC: This bit is the receive eye-optimization dynamic data centering enable.

Bits	SCOM	Field Mnemonic: Description
55	RWX	RX_EO_ENABLE_CM_COARSE_CAL: This bit is the receive eye-optimization common-mode coarse calibration enable.
56	RWX	RX_EO_ENABLE_CM_FINE_CAL: This bit is the receive eye-optimization common-mode fine calibration enable.
57	RWX	RX_EO_ENABLE_VGA_EDGE_OFFSET_CAL: This bit is the receive eye-optimization edge-offset calibration enable during VGA calibration.
58	RWX	RX_EO_ENABLE_CTLE_EDGE_OFFSET_CAL: This bit is the receive eye-optimization edge-offset calibration enable during CTLE calibration.
59:63	RO	constant = 0b00000

Register Name	Receive CTL Mode 22 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE22_EO_PG
Address	8008B80009010C3F (SCOM)
Description	This register contains the 22nd set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_RC_ENABLE_INTEG_LATCH_OFFSET_CAL: This bit is the receive recalibration latch offset adjustment enable with integrator-based disable.
49	RWX	RX_RC_ENABLE_CTLE_COARSE_CAL: This bit is the receive recalibration coarse CTLE/Peakin enable.
50	RWX	RX_RC_ENABLE_DAC_H1_CAL: This bit is the receive recalibration H! DAC calibration to reference.
51	RWX	RX_RC_ENABLE_VGA_CAL: This bit is the receive recalibration VGA gain and offset adjustment enable.
52	RWX	RX_RC_ENABLE_DFE_H1_CAL: This bit is the receive recalibration DFE H1 adjustment enable.
53	RWX	RX_RC_ENABLE_H1AP_TWEAK: This bit is the receive recalibration H1/AN PR adjustment enable.
54	RWX	RX_RC_ENABLE_DDC: This bit is the receive recalibration dynamic data-centering enable.
55	RWX	RX_RC_ENABLE_CM_COARSE_CAL: This bit is the receive recalibration common-mode coarse calibration enable.
56	RWX	RX_RC_ENABLE_CM_FINE_CAL: This bit is the receive recalibration common-mode fine calibration enable.
57	RWX	RX_RC_ENABLE_VGA_EDGE_OFFSET_CAL: This bit is the receive recalibration edge-offset calibration enable during VGA calibration.
58	RWX	RX_RC_ENABLE_CTLE_EDGE_OFFSET_CAL: This bit is the receive recalibration edge-offset calibration enable during CTLE calibration.
59:63	RO	constant = 0b00000

Register Name	Receive CTL Mode 23 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE23_EO_PG
Address	8008C00009010C3F (SCOM)
Description	This register contains the 23rd set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:52	RWX	RX_IREF_RES_DAC: This field contains the twos complement control vector for setting the magnitude of the output current of res outputs.
53	RWX	RX_IREF_BYPASS: This bit is used to bypass the closed loop controller for an open loop bias.
54	RWX	RX_IREF_PDWN_B: This bit provides Iref power down control (active low).
55:63	RO	constant = 0b000000000

Register Name	Receive CTL Mode 24 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE24_EO_PG
Address	8008C80009010C3F (SCOM)
Description	This register contains the 24th set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_H1AP_CFG: This register controls the maximum allowed ration of H1 and Ap. This is not a servo setting, but rather the setting of a ration between H1 and the value of Ap.
50	RWX	RX_CTLE_UPDATE_MODE: This bit controls updating of the CTLE_COARSE (peaking) values.
51:55	RO	constant = 0b00000
56:63	RWX	RX_USER_FILTER_MASK: This register controls the filter and mask for user-defined servo operations.

Register Name	Receive CTL Mode 29 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE29_EO_PG
Address	8008D00009010C3F (SCOM)
Description	This register contains the 29th set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_APX111_HIGH: This field contains the receive Amax high target, in amplitude DAC steps (as measured by ap_x111 and an_x000). The default is d102.
56:63	RWX	RX_APX111_LOW: This field contains the receive Amax low target, in amplitude DAC steps (as measured by ap_x111 and an_x000). The default is d68.

Register Name	Receive CTL CNTL1 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL1_EO_PG
Address	8008D80009010C3F (SCOM)
Description	This register contains the first set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	RX_BER_EN: Diagnostic bit-error-rate (BER) error checking enable control. When 1, this bit enables error checking. When 0, the error checking is disabled. This control enables the BER timer. It also enables the error checker and BER counters. The assumption is that the drivers are currently driving PRBS23, and the link was trained before enabling BER checking.
49	RWX	RX_BER_TIMER_FREEZE_EN: Diagnostic bit-error-rate (BER) timer freeze enable. When set to 1, the timer is frozen when any lane error count saturates in that pack.
50	RWX	RX_BER_COUNT_FREEZE_EN: Diagnostic BER lane error counter freeze enable. When set to 1, the per-lane error counters are frozen when the timer saturates in that pack.
51:54	RWX	RX_BER_COUNT_SEL: Diagnostic BER lane error counter saturation select. This field selects the number of errors that saturates the counter and causes a freeze event. The default value is used during initialization and must only be changed post initialization. 0b0000 = 1. 0b0001 = 2. 0b0010 = 4. 0b0011 = 8. 0b0100 = 16. 0b0101 = 32. 0b0110 = 64. 0b0111 = 128. 0b1000 = 256. 0b1001 = 512. 0b1010 = 1024. 0b1011 = unused1. 0b1100 = unused2. 0b1101 = unused3. 0b1110 = unused4. 0b1111 = unused5.
55	RO	constant = 0b0
56:58	RWX	RX_BER_TIMER_SEL: Diagnostic BER timer saturation select. This field selects the timer value that saturates the timer and causes a freeze event. The default value is used during initialization and must only be changed post initialization. 0b000 = 2^{31}. 0b001 = 2^{27}. 0b010 = 2^{23}. 0b011 = 2^{19}. 0b100 = 2^{17}. 0b101 = 2^{13}. 0b110 = 2^{9}. 0b111 = 2^{5}.
59	RWX	RX_BER_CLR_COUNT_ON_READ_EN: Diagnostic BER lane error counter clear on read. When set to 1, this bit enables clearing a lane's error counter when it is read.
60	RWX	RX_BER_CLR_TIMER_ON_READ_EN: Diagnostic BER timer clear on read. When set to 1, this bit enables clearing a lane's timer when it is read from any lane in the pack.
61:63	RO	constant = 0b000

Register Name	Receive CTL CNTL2 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL2_EO_PG
Address	8008E00009010C3F (SCOM)
Description	This register contains the second set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_TRC_MODE: Receive trace mode. 0b0000 = Training state machines. 0b0001 = Dynamic repair state machines. 0b0010 = SLS handshake state machines with recovery. 0b0011 = Dynamic recalibration state machines. 0b0100 = Recalibration handshake state machine with recovery. 0b0101 = CRC or ECC tallying logic. 0b0110 = Receive SLS commands. 0b0111 = Receive bad lanes. 0b1000 = Receive SLS lanes. 0b1001 = GCR. 0b1010 = Per lane/per pack trace (see rx_pp_trc_mode for details). 0b1011 = TBD. 0b1100 = TBD. 0b1101 = TBD. 0b1110 = TBD. 0b1111 = TBD.
52:63	RO	constant = 0b000000000000

Register Name	Receive CTL CNTL3 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL3_EO_PG
Address	8008E80009010C3F (SCOM)
Description	This register contains the third set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_INT_MODE: This field contains the receive interrupt mode setting.
52:63	RWX	RX_INT_CURRENT_STATE: This field contains the receive interrupt current state to stop on.

Register Name	Receive CTL CNTL4 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL4_EO_PG
Address	8008F00009010C3F (SCOM)
Description	This register contains the fourth set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_INT_ENABLE_ENC: This field contains the receive interrupt encoded enable.
52:63	RWX	RX_INT_NEXT_STATE: This field contains the receive interrupt next state to stop on.

Register Name	Receive CTL CNTL5 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL5_EO_PG
Address	8008F80009010C3F (SCOM)
Description	This register contains the fifth set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:51	RO	constant = 0b0000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
52:63	RWX	RX_INT_GOTO_STATE: This field contains the receive interrupt state to go to upon an interrupt trigger.

Register Name	Receive CTL CNTL6 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL6_EO_PG
Address	8009000009010C3F (SCOM)
Description	This register contains the sixth set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:51	RO	constant = 0b0000000000000000000000000000000000000000000000000000
52:63	RWX	RX_INT_RETURN_STATE: This field contains the receive interrupt state to go to upon return from an interrupt code.

Register Name	Receive CTL CNTL7 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTLX7_EO_PG
Address	8009080009010C3F (SCOM)
Description	This register contains the seventh set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56:60	RWX	RX_CAL_LANE_PG_PHY_GCRMSG: This field contains the encoded calibration lane in relation to the local, physical group.
61:63	RO	constant = 0b000

Register Name	Receive CTL CNTL8 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL8_EO_PG
Address	8009100009010C3F (SCOM)
Description	This register contains the eighth set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:62	RWX	RX_SERVO_OP: This field contains the servo operation code. It is written by the global training state machine.
63	RWX	RX_SERVO_DONE: This bit indicates that the servo operation completed. It is read by the global training state machine.

Register Name	Receive CTL CNTL9 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL9_EO_PG
Address	8009180009010C3F (SCOM)
Description	This register contains the ninth set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BIST_EN: This bit enables the receive BIST state machine to begin testing. It is set by the BIST helper sequencer through a GCR message. To properly initialize and run the receive BIST, set the rx_start_bist register bit.
49	RWX	RX_BIST_EXT_START_MODE: This bit enables the receive BIST state machine to begin testing. It is set by the BIST helper sequencer through a GCR message. To properly initialize and run the receive BIST, set the rx_start_bist register bit.
50:52	RWX	RX_BIST_INIT_DISABLE: Each bit disables an individual step of the receive BIST initialization state machine when raised. Bit 0 disables the CU PLL lock. Bit 1 disables the receive FIFO initialization. Bit 2 disables eye optimization/training.
53	RWX	RX_BIST_CUPLL_LOCK_CHECK_EN: This bit enables the CU PLL lock check mode of the receive BIST initialization state machine. When set high, the test checks for the PLL lock signal and sets an error if it is not present.
54:59	RWX	RX_BIST_STORE_EYES_LANE_SEL: This register selects which lane to store receive BIST eye-width data from. The data is stored in the rx_bist_eye_a_width and rx_bist_eye_b_width registers.
60:61	RWX	RX_BIST_STORE_EYES_BANK_SEL: This register selects which bank to store receive BIST eye-width data from. 0b00 = Store bank A widths. 0b01 = Store bank B widths. 0b10 = Store bank E widths. 0b11 = EDI+ bank A.
62	RWX	RX_PERVASIVE_CAPT: This bit latches glb_ctl and jtag_bndy pervasive signals in iocrc_pervasive_capt when set high. RO register bit rx_prvcpt_change_det goes high when latched values differ from pervasive inputs.
63	RWX	RX_BIST_LL_TEST_EN: This bit enables the link test portion of RX BIST.

Register Name	Receive CTL CNTL10 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL10_EO_PG
Address	8009200009010C3F (SCOM)
Description	This register contains the tenth set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_BIST_PRBS_TEST_TIME: This field controls how long the receive BIST tests the PRBS7 data for errors.
52	RWX	RX_BIST_BUS_DATA_MODE: This bit enables a mode where the receive BIST tests data from the bus.
53:56	RWX	RX_BIST_PRBS_PROP_TIME: This field controls how long the receive BIST waits between incrementing a phase rotator and beginning to test the PRBS data.
57:63	RO	constant = 0b0000000

Register Name	Receive CTL CNTL11 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL11_EO_PG
Address	8009280009010C3F (SCOM)
Description	This register contains the 11th set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:56	RWX	RX_DACTEST_LLMT: This control register is used to lower the threshold limit.
57	RWX	RX_DACTEST_RESET: This control register is used to reset the DACTEST.
58	RWX	RX_DACTEST_START: This control register is used to start the DACTEST.
59:63	RO	constant = 0b00000

Register Name	Receive CTL CNTL12 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL12_EO_PG
Address	8009300009010C3F (SCOM)
Description	This register contains the 12th set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:56	RWX	RX_DACTEST_HLMT: This control register is used to set a higher threshold limit.
57:63	RO	constant = 0b0000000

Register Name	Receive CTL CNTL13 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL13_EO_PG
Address	8009380009010C3F (SCOM)
Description	This register contains the 13th set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_HIST_MIN_EYE_WIDTH_VALID: This bit indicates that the receive historic eye width minimum value and lane are valid.
49:53	RWX	RX_HIST_MIN_EYE_WIDTH_LANE: This field contains the receive historic eye width lane number.
54:61	RWX	RX_HIST_MIN_EYE_WIDTH: This field contains the receive historic eye width and height minimum measurement mode.
62:63	RO	constant = 0b00

Register Name	Receive CTL CNTL14 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_CNTL14_EO_PG
Address	8009400009010C3F (SCOM)
Description	This register contains the 14th set of CTL CNTL EO fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_HIST_MIN_EYE_HEIGHT_VALID: This bit indicates that the receive historic eye height minimum value and lane are valid.
49:53	RWX	RX_HIST_MIN_EYE_HEIGHT_LANE: This field contains the receive historic eye height lane number.

Bits	SCOM	Field Mnemonic: Description
54:61	RWX	RX_HIST_MIN_EYE_HEIGHT: This field contains the receive historic eye height minimum measurement mode. It is inoperative on POWER8 processor with NVLink technology hardware. Use the rx_hist_min_eye_width_mode control instead. Set both the width and height_mode controls to the same value in test routines to maintain compatibility.
62:63	RO	constant = 0b00

Register Name	Receive CTL STAT1 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_STAT1_EO_PG
Address	8009500009010C3F (SCOM)
Description	This register contains the servo operation result.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_SERVO_RESULT: This field contains the servo operation result. It is read by the global training state machine.
56:63	RO	constant = 0b00000000

Register Name	Receive CTL STAT2 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_STAT2_EO_PG
Address	8009580009010C3F (SCOM)
Description	This register contains the status of the receive BIST.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_BIST_INIT_DONE: This bit signals completion of the receive BIST initialization state machine.
49	RWX	RX_BIST_DONE: This bit signals completion of the entire receive BIST procedure.
50	RWX	RX_BIST_LL_ERR: This bit indicates an error was detected during the link layer test portion of the receive BIST.
51	RWX	RX_BIST_NO_EDGE_DET: This bit indicates that one eye was counted to be significantly large (over 60 phase rotator steps).
52:57	RWX	RX_BIST_EYE_A_WIDTH: This register holds the counted eye A width of one particular lane.
58:63	RWX	RX_BIST_EYE_B_WIDTH: This register holds the counted eye B width of one particular lane.

Register Name	Receive CTL Mode 26 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE26_EO_PG
Address	8009680009010C3F (SCOM)
Description	This register contains the 26th set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_EO_ENABLE_CTLE_1ST_LATCH_OFFSET_CAL: Receive eye-optimization; first latch offset adjustment enable with CTLE-based disable.

Bits	SCOM	Field Mnemonic: Description
49	RWX	RX_EO_ENABLE_CTLE_2ND_LATCH_OFFSET_CAL: Receive eye-optimization; second latch offset adjustment enable with CTLE-based disable.
50	RWX	RX_EO_ENABLE_VGA_AMAX_MODE: Receive eye-optimization; VGA Ap measurement mode.
51:63	RO	constant = 0b0000000000000

Register Name	Receive CTL Mode 27 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE27_EO_PG
Address	8009700009010C3F (SCOM)
Description	This register contains the 27th set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_RC_ENABLE_CTLE_1ST_LATCH_OFFSET_CAL: Receive recalibration; first latch offset adjustment enable with CTLE-based disable.
49	RWX	RX_RC_ENABLE_CTLE_2ND_LATCH_OFFSET_CAL: Receive recalibration; second latch offset adjustment enable with CTLE-based disable.
50	RWX	RX_RC_ENABLE_VGA_AMAX_MODE: Receive recalibration; VGA Ap measurement mode.
51	RWX	RX_RC_ENABLE_AUTO_RECAL: Receive recalibration; VGA Ap measurement mode.
52:63	RO	constant = 0b000000000000

Register Name	Receive CTL Mode 28 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE28_EO_PG
Address	8009780009010C3F (SCOM)
Description	This register contains the 28th set of receive CTL EO mode fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_DC_ENABLE_CM_COARSE_CAL: This bit enables receive DC calibration eye-optimization common-mode coarse calibration.
49	RWX	RX_DC_ENABLE_CM_FINE_CAL: This bit enables receive DC calibration eye-optimization common-mode fine calibration.
50	RWX	RX_DC_ENABLE_CTLE_1ST_LATCH_OFFSET_CAL: Receive DC calibration eye-optimization latch offset adjustment enable done prior to CTLE.
51	RWX	RX_DC_ENABLE_CTLE_2ND_LATCH_OFFSET_CAL: Receive DC calibration eye-optimization latch offset adjustment enable done after CTLE.
52	RWX	RX_DC_ENABLE_INTEG_LATCH_OFFSET_CAL: Receive DC calibration eye-optimization latch offset adjustment enable done prior to integrator.
53:63	RO	constant = 0b00000000000

Register Name	Receive CTL Mode 2 O Per-Group
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE2_O_PG
Address	8009880009010C3F (SCOM)
Description	This is a per-group receive CTL mode O register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_OCTANT_SELECT: This field selects which c16 clock is used on IOO.
51:52	RWX	RX_SPEED_SELECT: This field selects the IOO speed control.
53	RWX	RX_AC_COUPLED: This bit selects the IOO AC coupled mode in the receiver.
54:63	RO	constant = 0b0000000000

Register Name	Receive CTL Mode 1 O Per-Group
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.CTL_REGS.RX_CTL_REGS.RX_CTL_MODE1_O_PG
Address	8009B00009010C3F (SCOM)
Description	This register contains minikerf control bits.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	RWX	RX_MINIKERF: This field contains receive minikerf control bits. Bits 3:13 are only used when bits 0:2 = 001. Bits 14:15 are spare. Bits 0:2 are level 1 steering: 000 = Reserved. 001 = Use bits 3:5. 010= impedance control termref_mk_probe_ana(0:1) only for the POWER8 memory buffer. All other buses use the tx_minikerf_pb. 011 = Receive cleanup PLL atst on pad_io_p. Pad_io_n = 0. 100 = Reserved. 101 = Reserved. 110 = Receive cleanup PLL clock on C4 pads. 111= Reserved. Bits 3:5 are level 2 steering. Bits 6:13 are DAC controls. Bits 14:15 are spare.

Register Name	Receive GLBSM Spare Mode Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_SPARE_MODE_PG
Address	800A800009010C3F (SCOM)
Description	This register contains per-group spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PG_GLBSM_SPARE_MODE_0: Per-group spare mode latch.
49	RWX	RX_PG_GLBSM_SPARE_MODE_1: Per-group spare mode latch.
50	RWX	RX_PG_GLBSM_SPARE_MODE_2: Per-group spare mode latch.

Bits	SCOM	Field Mnemonic: Description
51	RWX	RX_PG_GLBSM_SPARE_MODE_3: Per-group spare mode latch.
52	RWX	RX_PG_GLBSM_SPARE_MODE_4: Per-group spare mode latch.
53	RWX	RX_PG_GLBSM_SPARE_MODE_5: Per-group spare mode latch.
54	RWX	RX_PG_GLBSM_SPARE_MODE_6: Per-group spare mode latch.
55	RWX	RX_PG_GLBSM_SPARE_MODE_7: Per-group spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Receive FIR1 Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.REGS.RX_FIR1_PG
Address	800A880009010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	ROX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60	ROX	Reserved field.
61	RO	constant = 0b0
62	ROX	Reserved field.
63	RO	constant = 0b0

Register Name	Receive FIR1 Mask Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.REGS.RX_FIR1_MASK_PG
Address	800A900009010C3F (SCOM)
Description	This register masks receive FIR per-group errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:62	RWX	RX_Per Group_FIR1_ERRS_MASK: This field provides a FIR mask for register or state-machine parity checkers in the per-group receive logic. A value of 1 masks the error from generating a FIR error. Bit 0 = (mask_pg_regs) RXCTL Register parity error mask. Bit 1 = Reserved. Bit 2 = Reserved. Bit 3 = (mask_gcrs_ld_sm) RXCTL GCR load state machine parity error mask. Bit 4 = (mask_gcrs_unld_sm) RXCTL GCR unload state machine parity error mask. Bit 5 = (mask_snd_msg_sm) RXCTL Send message parity error mask. Bit 6 = (mask_main_init_sm) RXCTL main init state machine parity error mask. Bit 7 = (mask_wtm_sm) RXCTL wire-test main state machine parity error mask.
63	RO	constant = 0b0

Register Name	Receive FIR1 Error Inject Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.REGS.RX_FIR1_ERROR_INJECT_PG
Address	800A980009010C3F (SCOM)
Description	This register is used to inject parity errors into the per-group receive registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:62	RWX	RX_PG_FIR1_ERR_INJ: IOTK ALIAS: Receive per-group parity error injection. This field enables the injection of non-destructive parity errors in either register or state-machine latch banks. The register or state value is not affected.
63	RO	constant = 0b0

Register Name	Receive GLBSM CNTLX1 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_CNTLX1_EO_PG
Address	800AB00009010C3F (SCOM)
Description	This register controls per-group latches.

Bits	SCOM	Field Mnemonic: Description
0:61	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000
62	RWX	RX_CLR_PAR_ERRS: Clear all receive parity error latches. Toggle this field 0→1-→0 to clear all receive parity error latches.
63	RWX	RX_FIR_RESET: FIR reset. Toggle this field 0→1→0 to reset all the receive FIR-related latches including the isolation and parity error latches.

Register Name	Receive GLBSM STAT1 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_STAT1_EO_PG
Address	800AB80009010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:59	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
60:63	RO	constant = 0b0000

Register Name	Receive GLBSM STAT2 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_STAT2_EO_PG
Address	800AC00009010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	ROX	Reserved field.

Register Name	Receive GLBSM STAT3 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_STAT3_EO_PG
Address	800AC80009010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51:59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Receive GLBSM STAT4 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_STAT4_EO_PG
Address	800AD00009010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	ROX	Reserved field.

Register Name	Receive GLBSM STAT5 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_STAT5_EO_PG
Address	800AD80009010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50:54	ROX	Reserved field.
55	ROX	Reserved field.
56:63	RO	constant = 0b00000000

Register Name	Receive GLBSM CNTL2 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_CNTL2_EO_PG
Address	800AE00009010C3F (SCOM)
Description	This register controls the single-lane recalibration monitor mode.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant = 0b0000000000000000000000000000000000000000000000000
49	RWX	RX_CNT_SINGLE_LANE_RECAL: This bit selects single-lane recalibration monitor mode.
50:54	RWX	RX_RECAL_LANE_TO_MONITOR: This field designates the lane to monitor when rx_cnt_single_lane_recal is 1.
55:63	RO	constant = 0b000000000

Register Name	Receive GLBSM CNTL3 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_CNTL3_EO_PG
Address	800AE80009010C3F (SCOM)
Description	This register controls manual recalibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_MANUAL_RECAL_REQUEST: This bit indicates a recalibration request from the microcontroller.
49:50	RO	constant = 0b00
51:55	RWX	RX_MANUAL_RECAL_LANE: This field specifies the recalibration lane from the microcontroller.
56:63	RO	constant = 0b00000000

Register Name	Receive GLBSM CNTL4 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.GLBSM.REGS.RX_GLBSM_CNTL4_EO_PG
Address	800AF00009010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	NCX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52:63	RO	constant = 0b000000000000

Register Name	Receive DATASM Spare Mode Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_SPARE_MODE_PG
Address	800B800009010C3F (SCOM)
Description	This register contains per-group spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	RX_PG_DATASM_SPARE_MODE_0: Per-group spare mode latch.
49	RWX	RX_PG_DATASM_SPARE_MODE_1: Per-group spare mode latch.
50	RWX	RX_PG_DATASM_SPARE_MODE_2: Per-group spare mode latch.
51	RWX	RX_PG_DATASM_SPARE_MODE_3: Per-group spare mode latch.
52	RWX	RX_PG_DATASM_SPARE_MODE_4: Per-group spare mode latch.
53	RWX	RX_PG_DATASM_SPARE_MODE_5: Per-group spare mode latch.
54	RWX	RX_PG_DATASM_SPARE_MODE_6: Per-group spare mode latch.
55	RWX	RX_PG_DATASM_SPARE_MODE_7: Per-group spare mode latch.
56:59	RWX	RX_SERVO_CONFIG: Per-group servo configuration bits.
60	RWX	RX_CTL_DATASM_CLKDIST_PDWN: This bit is used to put additional rx_ctl_datasm_mac logic into clock off mode.
61:63	RO	constant = 0b000

Register Name	Receive DATASM CNTLX1 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_CNTLX1_EO_PG
Address	800B880009010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant = 0b0000000000000000000000000000000000000000000000000
49	NCX	Reserved field.
50	NCX	Reserved field.
51	NCX	Reserved field.
52	NCX	Reserved field.
53	NCX	Reserved field.
54	NCX	Reserved field.
55:63	RO	constant = 0b000000000

Register Name	Receive DATASM STAT1 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT1_EO_PG
Address	800B900009010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:58	ROX	Reserved field.
59	ROX	Reserved field.
60	ROX	Reserved field.
61	ROX	Reserved field.
62	ROX	Reserved field.
63	RO	constant = 0b0

Register Name	Receive DATASM STAT2 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT2_EO_PG
Address	800B980009010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	ROX	Reserved field.

Register Name	Receive DATASM STAT3 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT3_EO_PG
Address	800BA00009010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	ROX	Reserved field.

Register Name	Receive DATASM STAT4 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT4_EO_PG
Address	800BA80009010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	ROX	Reserved field.

Register Name	Receive DATASM STAT5 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT5_EO_PG
Address	800BB00009010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	ROX	Reserved field.

Register Name	Receive DATASM STAT6 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT6_EO_PG
Address	800BB80009010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	ROX	Reserved field.

Register Name	Receive DATASM STAT7 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT7_EO_PG
Address	800BC00009010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:51	ROX	Reserved field.
52:58	RO	constant = 0b0000000
59:62	ROX	Reserved field.
63	ROX	Reserved field.

Register Name	Receive DATASM STAT8 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT8_EO_PG
Address	800BC80009010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	ROX	Reserved field.

Register Name	Receive DATASM STAT9 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT9_EO_PG
Address	800BD00009010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:56	ROX	Reserved field.
57:63	RO	constant = 0b0000000

Register Name	Receive DATASM STAT10 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT10_EO_PG
Address	800BD80009010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56:63	ROX	Reserved field.

Register Name	Receive DATASM STAT11 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.RX0.RXCTL.DATASM.DATASM_REGS.RX_DATASM_STAT11_EO_PG
Address	800BE00009010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:63	ROX	Reserved field.

Register Name	Transmit Spare Mode Per-Group Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXCTL.CTL_REGS.TX_CTL_REGS.TX_SPARE_MODE_PG
Address	800C040009010C3F (SCOM)
Description	This register contains per-group spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_PG_SPARE_MODE_0: Per-group spare mode latch.
49	RWX	TX_PG_SPARE_MODE_1: Per-group spare mode latch.
50	RWX	TX_PG_SPARE_MODE_2: Per-group spare mode latch.
51	RWX	TX_PG_SPARE_MODE_3: Per-group spare mode latch.
52	RWX	TX_PG_SPARE_MODE_4: Per-group spare mode latch.

Bits	SCOM	Field Mnemonic: Description
53	RWX	TX_PG_SPARE_MODE_5: Per-group spare mode latch.
54	RWX	TX_PG_SPARE_MODE_6: Per-group spare mode latch.
55	RWX	TX_PG_SPARE_MODE_7: Per-group spare mode latch.
56:57	RWX	TX_PG_SPARE_MODE_8_9: Per-group spare mode latch.
58:63	RO	constant = 0b000000

Register Name	Transmit ID1 Per-Group Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXCTL.CTL_REGS.TX_CTL_REGS.TX_ID1_PG
Address	800C0C0009010C3F (SCOM)
Description	This register is used to programmatically set the bus number that a group belongs to.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:53	RWX	TX_BUS_ID: This field is used to programmatically set the bus number that a group belongs to.
54:63	RO	constant = 0b0000000000

Register Name	Transmit CTL Mode 1 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_MODE1_EO_PG
Address	800C140009010C3F (SCOM)
Description	This register contains transmit control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	TX_CLKDIST_PDWN: This field is used to disable the transmit group clocks and put them into a low-power state. It does not control per-lane circuits or logic. Bit 0 disables slices 16 - 23. Bit 1 disables slices 8 - 15. Bit 2 disables slices 0 - 7.
51	RW	TX_BIST_EN: This bit enables the transmit BIST state machine to begin testing.
52	RW	TX_EXBIST_MODE: This bit is used to disable the BIST enable through external I/O.
53:63	RO	constant = 0b00000000000

Register Name	Transmit CTL CNTLG1 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_CNTLG1_EO_PG
Address	800C240009010C3F (SCOM)
Description	This register contains the transmit drive patterns.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:53	RWX	TX_DRV_DATA_PATTERN_GCRMSG: Transmit drive patterns. 0b0000 = Drive all 0s pattern. 0b0001 = Drive wire-test pattern. 0b0010 = Drive all 1s pattern. 0b0011 = Drive deskew pattern A. 0b0100 = Drive deskew pattern B. 0b0101 = PRBS full-speed scramble pattern (see tx_prbs_tap_id). 0b0110 = Alternate PRBS7 pattern for RX BIST. 0b0111 = PRBS calibration or 9th pattern. 0b1000 = PRBS7 pattern. 0b1001 = PRBS11 pattern. 0b1010 = Drives TDR pulse-square waves. 0b1011 = PRBS15 pattern. 0b1100 = Alternate PRBS23 for NVBUS. 0b1101 = PRBS31 pattern. 0b1110 = 1-to-1 clock pattern. 0b1111 = Unused.
54:63	RO	constant = 0b0000000000

Register Name	Transmit CTL CNTL2 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_CNTL2_EO_PG
Address	800C2C0009010C3F (SCOM)
Description	This register contains per-group transmit control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	TX_ERR_INJ_A_FINE_SEL: This field contains the random LSB/fine-grained cycle offset variation control for pattern A, where cycles are deserialized domain cycles. 0b000 = Random offset in the range of 1 - 32 cycles(default). 0b001 = Random offset in the range of 1 - 16 cycles. 0b010 = Random offset in the range of 1 - 8 cycles. 0b011 = Random offset in the range of 1 - 4 cycles. 0b100 = Random offset in the range of 1 - 2 cycles. 0b101 = Fixed offset of 1 cycle. 0b110 = Fixed offset of 3 cycles. 0b111 = Fixed offset of 7 cycles.
51:54	RWX	TX_ERR_INJ_A_COARSE_SEL: This field contains the random MSB/coarse-grained multiplier for the base error rate counter, which controls bit-error-rate variation for pattern A. There are also a number of nonrandom settings that are specifically chosen to avoid powers of two.
55:60	RWX	TX_ERR_INJ_A_BER_SEL: This field is used to set the random bit-error injection rate for pattern A. When set to a binary value of N, the average bit error rate is 1/(2^N x beats x mean(MSB)).
61	RWX	TX_ERR_INJ_ENABLE: This bit is the overall error injection enable. When set to 0, all other injection is gated.
62	RWX	TX_ERR_INJ_CLOCK_ENABLE: This bit enables clocks to larger counter and PRBS logic. Use this to stagger start times and effectively seed the injection mechanism randomly.
63	RO	constant = 0b0

Register Name	Transmit CTL CNTL3 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_CNTL3_EO_PG
Address	800C340009010C3F (SCOM)
Description	This register contains per-group transmit control fields.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:50	RWX	TX_ERR_INJ_B_FINE_SEL: This field contains the random LSB/fine-grained cycle offset variation control for pattern B, where cycles are deserialized domain cycles. 0b000 = Random offset in range of 1 - 32 cycles(default). 0b001 = Random offset in range of 1 - 16 cycles. 0b010 = Random offset in range of 1 - 8 cycles. 0b011 = Random offset in range of 1 - 4 cycles. 0b100 = Random offset in range of 1 - 2 cycles. 0b101 = Fixed offset of 1 cycle. 0b110 = Fixed offset of 3 cycles. 0b111 = Fixed offset of 7 cycles.
51:54	RWX	TX_ERR_INJ_B_COARSE_SEL: This field contains the random MSB/coarse-grained multiplier for the base error-rate counter, which controls the bit-error-rate variation for pattern B. There are also a number of nonrandom settings that are specifically chosen to avoid powers of two.
55:60	RWX	TX_ERR_INJ_B_BER_SEL: This field is used to set the random bit-error injection rate for pattern B. When set to a binary value of N, the average bit error rate is 1/(2^N x beats x mean(MSB)).
61:63	RO	constant = 0b000

Register Name	Transmit CTL CNTL8 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_CNTL8_EO_PG
Address	800CCC0009010C3F (SCOM)
Description	This register is used to control the TDR function.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	TX_TDR_DAC_CNTL: This field controls the variable threshold receiver for the TDR function.
56	RO	constant = 0b0
57	RWX	TX_TDR_PHASE_SEL: This field controls phase select for the TDR function. 0 = _n leg. 1 = _p leg.
58:63	RO	constant = 0b000000

Register Name	Transmit CTL CNTL9 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_CNTL9_EO_PG
Address	800CD40009010C3F (SCOM)
Description	This register is used to control the TDR function.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:61	RWX	TX_TDR_PULSE_OFFSET: This field contains the offset value for the TDR pulse.
62:63	RO	constant = 0b00

Register Name	Transmit CTL CNTL10 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXCTL.CTL_REGS.TX_CTL_REGS.TX_CTL_CNTL10_EO_PG
Address	800CDC0009010C3F (SCOM)
Description	This register is used to control the TDR function.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	TX_TDR_PULSE_WIDTH: The field controls the width of the TDR pulse.
56:63	RO	constant = 0b00000000

Register Name	Transmit Group FIR Error Source
Mnemonic	IOO0.IOO_CPLT.TX0.TXCTL.TX_CTL_SM.REGS.TX_FIR_Per Group
Address	800D040009010C3F (SCOM)
Description	This is an isolation register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	Reserved field.
49	ROX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53:62	RO	constant = 0b0000000000
63	ROX	Reserved field.

Register Name	Transmit Group FIR Error Mask Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXCTL.TX_CTL_SM.REGS.TX_FIR_MASK_PG
Address	800D0C0009010C3F (SCOM)
Description	This register masks transmit FIR per-group errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:52	RWX	TX_Per Group_FIR_ERRS_MASK: This field contains the FIR mask for register or state-machine parity checkers in the per-group TXCTL logic. A value of 1 masks the error from generating a FIR error. Bit 0 = par_err_mask_txctl_regs. Bit 1 = par_err_mask_gcr_buff. Bit 2 = Reserved. Bit 3 = par_err_mask_tx_stt_rpr_snd_msg_state. Bit 4 = par_err_mask_gcrs_ld_state. Bit 5 = par_err_mask_gcrs_unld_state. Bit 6 = Reserved. Bit 7 = Reserved.
53:62	RO	constant = 0b0000000000
63	RWX	TX_PL_FIR_ERR_MASK: IOTK ALIAS: This bit is a FIR mask for the per-lane transmit register checker.

Register Name	Transmit Reset Control Action Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXCTL.TX_CTL_SM.REGS.TX_FIR_RESET_PG
Address	800D140009010C3F (SCOM)
Description	This register controls per-group transmit latches.

Bits	SCOM	Field Mnemonic: Description
0:61	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000
62	RWX	TX_CLR_PAR_ERRS: Clear all transmit parity error latches. Toggle this field 0→1→0 to clear all transmit parity error latches.
63	RWX	TX_FIR_RESET: FIR reset. Toggle this field 0→1→0 to reset all transmit FIR-related latches including parity error latches.

Register Name	Transmit Per-Group FIR Error Injection Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXCTL.TX_CTL_SM.REGS.TX_FIR_ERROR_INJECT_PG
Address	800D1C0009010C3F (SCOM)
Description	This register is used to inject errors into per-group transmit registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	TX_PG_FIR_ERR_INJ: IOTK ALIAS: While 1, inverts the parity check bit to force an error on the per-group TXCTL register or the state-machine parity checkers.
53:63	RO	constant = 0b00000000000

Register Name	Transmit CTLSM Spare Mode Per-Group Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_SPARE_MODE_PG
Address	800D240009010C3F (SCOM)
Description	This register contains per-group spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	TX_PG_CTL_SM_SPARE_MODE_0: Per-group spare mode latch.
49	RWX	TX_PG_CTL_SM_SPARE_MODE_1: Per-group spare mode latch.
50	RWX	TX_PG_CTL_SM_SPARE_MODE_2: Per-group spare mode latch.
51	RWX	TX_PG_CTL_SM_SPARE_MODE_3: Per-group spare mode latch.
52	RWX	TX_PG_CTL_SM_SPARE_MODE_4: Per-group spare mode latch.
53	RWX	TX_PG_CTL_SM_SPARE_MODE_5: Per-group spare mode latch.
54	RWX	TX_PG_CTL_SM_SPARE_MODE_6: Per-group spare mode latch.
55	RWX	TX_PG_CTL_SM_SPARE_MODE_7: Per-group spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	**Transmit CTLSM Mode 1 EO Per-Group Register**
Mnemonic	IOO0.IOO_CPLT.TX0.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_MODE1_EO_PG
Address	800D2C0009010C3F (SCOM)
Description	This register controls the driver segment test.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50:57	RWX	TX_SEG_TEST_MODE: Driver segment test mode. When this field is all 0s, it means normal function mode. When this field is not all 0s, the segment test begins.
58	RO	constant = 0b0
59	RWX	TX_FFE_BOOST_EN: Driver segment test. This bit enables the boost function of the NVLink transmit.
60	RO	constant = 0b0
61	RWX	TX_SEG_TEST_LEAKAGE_CTRL: This bit controls txr_txc_sst_ctl_dc in every transmit slice. 1 = Run the segment test in low-leakage mode.
62:63	RO	constant = 0b00

Register Name	**Transmit CTLSM CNTL1 EO Per-Group Register**
Mnemonic	IOO0.IOO_CPLT.TX0.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_CNTL1_EO_PG
Address	800D340009010C3F (SCOM)
Description	This register contains transmit pseg controls.

Bits	SCOM	Field Mnemonic: Description
0:50	RO	constant = 0b000000000000000000000000000000000000000000000000000
51:55	RWX	TX_PSEG_PRE_EN: This field is used for pre-bank pseg enable.
56:60	RWX	TX_PSEG_PRE_SEL: This field is used for pre-bank pseg mode selection.
61:63	RO	constant = 0b000

Register Name	Transmit CTLSM CNTL2 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_CNTL2_EO_PG
Address	800D3C0009010C3F (SCOM)
Description	This register contains transmit per-group controls.

Bits	SCOM	Field Mnemonic: Description
0:50	RO	constant = 0b000000000000000000000000000000000000000000000000000
51:55	RWX	TX_NSEG_PRE_EN: This field is used for pre-bank nseg enable.
56:60	RWX	TX_NSEG_PRE_SEL: This field is used for pre-bank nseg mode selection.
61:63	RO	constant = 0b000

Register Name	Transmit CTLSM CNTL3 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_CNTL3_EO_PG
Address	800D440009010C3F (SCOM)
Description	This register contains transmit per-group controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	TX_PSEG_MARGINPU_EN: This field is used for margin pull-up bank pseg enable.
56:63	RWX	TX_PSEG_MARGINPD_EN: This field is used for margin pull-down bank pseg enable.

Register Name	Transmit CTLSM CNTL4 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_CNTL4_EO_PG
Address	800D4C0009010C3F (SCOM)
Description	This register contains transmit per-group controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	TX_NSEG_MARGINPU_EN: This field is used for margin pull-up bank nseg enable.
56:63	RWX	TX_NSEG_MARGINPD_EN: This field is used for margin pull-down bank nseg enable.

Register Name	Transmit CTLSM CNTL5 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_CNTL5_EO_PG
Address	800D540009010C3F (SCOM)
Description	This register contains transmit per-group controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	TX_MARGINPU_SEL: This field is used for margin pull-up bank mode selection.
56:63	RWX	TX_MARGINPD_SEL: This field is used for margin pull-down bank mode selection.

Register Name	Transmit CTLSM CNTL6 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_CNTL6_EO_PG
Address	800D5C0009010C3F (SCOM)
Description	This register contains transmit per-group controls.

Bits	SCOM	Field Mnemonic: Description
0:50	RO	constant = 0b000000000000000000000000000000000000000000000000000
51:57	RWX	TX_PSEG_MAIN_EN: This field is used for main bank pseg enable.
58:63	RO	constant = 0b000000

Register Name	Transmit CTLSM CNTL7 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_CNTL7_EO_PG
Address	800D640009010C3F (SCOM)
Description	This register contains transmit per-group controls.

Bits	SCOM	Field Mnemonic: Description
0:50	RO	constant = 0b000000000000000000000000000000000000000000000000000
51:57	RWX	TX_NSEG_MAIN_EN: This field is used for main bank nseg enable.
58:63	RO	constant = 0b000000

Register Name	Transmit CTLSM STAT1 EO Per-Group Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_STAT1_EO_PG
Address	800D6C0009010C3F (SCOM)
Description	This is a reserved field.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant = 0b00000000000000000000000000000000000000000000000000
50	ROX	Reserved field.
51:63	RO	constant = 0b0000000000000

Register Name	Transmit CTLSM CNTL1 O Per-Group Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_CNTL1_O_PG
Address	800D840009010C3F (SCOM)
Description	This register contains transmit per-group controls.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant = 0b0000000000000000000000000000000000000000000000000
49:55	RWX	TX_PSEG_POST_EN: This field is used for post bank pseg enable.
56:62	RWX	TX_PSEG_POST_SEL: This field is used for post bank pseg mode selection.
63	RO	constant = 0b0

Register Name	Transmit CTLSM CNTL2 O Per-Group Register
Mnemonic	IOO0.IOO_CPLT.TX0.TXCTL.TX_CTL_SM.REGS.TX_CTLSM_CNTL2_O_PG
Address	800D8C0009010C3F (SCOM)
Description	This register contains transmit per-group controls.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant = 0b0000000000000000000000000000000000000000000000000
49:55	RWX	TX_NSEG_POST_EN: This field is used for post bank nseg enable.
56:62	RWX	TX_NSEG_POST_SEL: This field is used for post bank nseg mode selection.
63	RO	constant = 0b0

Register Name	Transmit Impedance Calibration Per-Bus Register
Mnemonic	IOO0.IOO_CPLT.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.TX_IMPCAL_PB
Address	800F040009010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant = 0b0000000000000000000000000000000000000000000000000
49	NCX	Reserved field.
50	ROX	Reserved field.
51	ROX	Reserved field.
52	ROX	Reserved field.
53	NCX	Reserved field.
54	ROX	Reserved field.
55:63	ROX	Reserved field.

Register Name	Transmit Impedance Calibration NVAL Per-Bus Register
Mnemonic	IOO0.IOO_CPLT.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.TX_IMPCAL_NVAL_PB
Address	800F0C0009010C3F (SCOM)
Description	This register is used for impedance calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:56	RWX	TX_ZCAL_N: Calibration circuit NSeg enable value. This field holds the current value of the enabled segments. It is a 4x multiple of the actual segment count. It can be read for the current calibration result set during the calibration sequence. It can be written to immediately update circuit enables on each write. It is used with tx_zcal_swo_* for manual calibration. Do not write to this field when tx_zcal_req = 1. (binary code - 0x00 is zero slices, and 0xA1 is maximum slices).
57:63	RO	constant = 0b0000000

Register Name	Transmit Impedance Calibration PVAL Per-Bus Register
Mnemonic	IOO0.IOO_CPLT.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.TX_IMPCAL_PVAL_PB
Address	800F140009010C3F (SCOM)
Description	This register is used for impedance calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:56	RWX	TX_ZCAL_P: Calibration circuit PSeg enable value. This field holds the current value of the enabled segments. It is a 4x multiple of the actual segment count. It can be read for the current calibration result set during the calibration sequence. It can be written to immediately update circuit enables on each write. It is used with tx_zcal_swo_* for manual calibration. Do not write this field when tx_zcal_req = 1. (binary code - 0x00 is zero slices, and 0xA1 is maximum slices).
57:63	RO	constant = 0b0000000

Register Name	Transmit Impedance Calibration P 4X Per-Bus Register
Mnemonic	IOO0.IOO_CPLT.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.TX_IMPCAL_P_4X_PB
Address	800F1C0009010C3F (SCOM)
Description	This register is used for impedance calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:52	RWX	TX_ZCAL_P_4X: Calibration circuit PSeg-4X enable value. This field holds the current value of the enabled segments. It is a 2x multiple of the actual segment count. It can be read for the current calibration result set during the calibration sequence. It can be written to immediately update circuit enables on each write. It is used with tx_zcal_swo_* for manual calibration. Do not write this field when tx_zcal_req = 1. (binary code - 0x00 is zero slices and 0x15 is maximum slices).
53:63	RO	constant = 0b00000000000

Register Name	Transmit Impedance Calibration SWO1 Per-Bus Register
Mnemonic	IOO0.IOO_CPLT.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.TX_IMPCAL_SWO1_PB
Address	800F240009010C3F (SCOM)
Description	This register is used for impedance calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	TX_ZCAL_SWO_EN: Impedance calibration software override. This bit steers all calibration controls directly from these register fields. It effectively disables the state-machine logic (default). 0b0 = Inactive. 0b1 = Enable.
49	RWX	TX_ZCAL_SWO_CAL_SEGS: Impedance calibration software bank select. This bit enables PSeg calibration (default). 0b0 = Select NSeg bank comparison. 0b1 = Select PSeg bank comparison.

Bits	SCOM	Field Mnemonic: Description
50	RWX	TX_ZCAL_SWO_CMP_INV: Impedance calibration software compare invert. This bit swaps calibration circuit comparator inputs (default). 0b0 = Select NSeg bank comparison. 0b1 = Select PSeg bank comparison.
51	RWX	TX_ZCAL_SWO_CMP_OFFSET: Impedance calibration software offset flush. This bit equalizes the comparator offset in the calibration circuit (default). 0b0 = Disable offset. 0b1 = Enable offset.
52	RWX	TX_ZCAL_SWO_CMP_RESET: Impedance calibration software comparator reset. This bit resets the comparator in the calibration circuit (default). 0b0 = Disable reset. 0b1 = Enable reset.
53	RWX	TX_ZCAL_SWO_POWERDOWN: Impedance calibration software circuit power down. This bit enables the power-down calibration circuit (default). 0b0 = Disable power down. 0b1 = Enable power down.
54	RWX	TX_ZCAL_SWO_TCOIL: Impedance calibration software circuit TCoil.
55	RWX	TX_ZCAL_RANGE_CHECK: This bit controls the usage of tx_zcal_sm_min/max_val. 0 = These two registers are used to define the range of zcal. 1 = The calibration range is 1 - 80, and the minimum/maximum registers are only used to check whether the result is in range.
56	RWX	TX_ZCAL_CYA_DATA_INV: Impedance calibration CYA sample inversion. This bit selects inverted comparator values in case of a hardware error (default). 0b0 = No sample inversion. 0b1 = Invert samples.
57	RWX	TX_ZCAL_TEST_OVR_2R: Impedance calibration test-only 2R segment override.
58	RWX	TX_ZCAL_TEST_OVR_1R: Impedance calibration test-only 1R segment override.
59	RWX	TX_ZCAL_TEST_OVR_4X_SEG: Impedance calibration test-only 4x segment override.
60	RWX	TX_ZCAL_TEST_CLK_DIV: This register controls the clock for impedance BIST. 1 = The clock is divided by 32. 0 = PLL bypass mode is needed.
61:63	RO	constant = 0b000

Register Name	Transmit Impedance Calibration SWO2 Per-Bus Register
Mnemonic	IOO0.IOO_CPLT.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.TX_IMPCAL_SWO2_PB
Address	800F2C0009010C3F (SCOM)
Description	This register is used for impedance calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:54	RWX	TX_ZCAL_SM_MIN_VAL: Impedance calibration minimum search threshold. This low-side segment count limit is used in the calibration process. (binary code - 0x00 is zero slices, and 0x50 is maximum slices).
55:61	RWX	TX_ZCAL_SM_MAX_VAL: Impedance calibration maximum search threshold. This high-side segment count limit is used in the calibration process. (binary code - 0x00 is zero slices and 0x50 is maximum slices).
62:63	RO	constant = 0b00

Register Name	Spare Mode Per-Bus Register
Mnemonic	IOO0.IOO_CPLT.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.SPARE_MODE_PB
Address	800F340009010C3F (SCOM)
Description	This register contains per-bus spare mode latches.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	RWX	PB_SPARE_MODE_0: Per-bus spare mode latch.
49	RWX	PB_SPARE_MODE_1: Per-bus spare mode latch.
50	RWX	PB_SPARE_MODE_2: Per-bus spare mode latch.
51	RWX	PB_SPARE_MODE_3: Per-bus spare mode latch.
52	RWX	PB_SPARE_MODE_4: Per-bus spare mode latch.
53	RWX	PB_SPARE_MODE_5: Per-bus spare mode latch.
54	RWX	PB_SPARE_MODE_6: Per-bus spare mode latch.
55	RWX	PB_SPARE_MODE_7: Per-bus spare mode latch.
56:63	RO	constant = 0b00000000

Register Name	Transmit IMPCAL2 Per-Bus Register
Mnemonic	IOO0.IOO_CPLT.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.TX_IMPCAL2_PB
Address	800F3C0009010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant = 0b0000000000000000000000000000000000000000000000000
49	ROX	Reserved field.
50	ROX	Reserved field.
51:52	RO	constant = 0b00
53	NCX	Reserved field.
54	ROX	Reserved field.
55	ROX	Reserved field.
56:63	RO	constant = 0b00000000

Register Name	Receive FIR Reset Per-Bus Register
Mnemonic	IOO0.IOO_CPLT.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.RX_FIR_RESET_PB
Address	800F800009010C3F (SCOM)
Description	This register controls per-bus transmit latches.

Bits	SCOM	Field Mnemonic: Description
0:61	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000
62	RWX	RX_PB_CLR_PAR_ERRS: Clear all receive parity error latches. Toggle this field 0→1→0 to clear parity-error latches in the BUSCTL logic.

Bits	SCOM	Field Mnemonic: Description
63	RWX	RX_PB_FIR_RESET: FIR reset. Toggle this field 0→1→0 to reset the BUSCTL logic FIR-related latches, including the isolation and parity-error latches.

Register Name	Receive FIR Per-Bus Register
Mnemonic	IOO0.IOO_CPLT.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.RX_FIR_PB
Address	800F880009010C3F (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:57	ROX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	Receive FIR Mask Per-Bus Register
Mnemonic	IOO0.IOO_CPLT.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.RX_FIR_MASK_PB
Address	800F900009010C3F (SCOM)
Description	This register masks receive FIR per-bus errors.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:57	RWX	RX_PB_FIR_ERRS_MASK: IOTK ALIAS: This field is a FIR mask for rx_fir_pb errors.
58:63	RO	constant = 0b000000

Register Name	Receive FIR Error Inject Per-Bus Register
Mnemonic	IOO0.IOO_CPLT.BUSCTL.BUS_REG_IF.BUS_CTL_REGS.RX_FIR_ERROR_INJECT_PB
Address	800F980009010C3F (SCOM)
Description	This register is used to inject errors into the per-bus receive registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48:57	RWX	RX_PB_FIR_ERRS_INJ: IOTK ALIAS: Receive per-bus parity error injection. This field allows injection of non-destructive parity errors in either register or state-machine latch banks. The register or state value is not affected.
58:63	RO	constant = 0b000000

8. PCI 0 Chiplet

The POWER9 processor registers are listed alphabetically by mnemonic in the following address table.

Mnemonic	Address	Page
IOP0.IOP_X844.IOP_SCOM.FIR_ACTION0_REG	0x000000000D010C06	1907
IOP0.IOP_X844.IOP_SCOM.FIR_ACTION1_REG	0x000000000D010C07	1907
IOP0.IOP_X844.IOP_SCOM.FIR_MASK_REG	0x000000000D010C03	1905
IOP0.IOP_X844.IOP_SCOM.FIR_STATUS_REG	0x000000000D010C00	1903
IOP0.IOP_X844.IOP_SCOM.FIR_WOF_REG	0x000000000D010C08	1907
PE0.PB0.PBAIB.REGS.PBAIBHWCFG_REG	0x000000000D010800	1881
PE0.PB0.PBAIB.REGS.PECAPP_SEC_BAR	0x000000000D010801	1882
PE0.PB0.PBAIB.REGS.STACK#0.REGS.PBAIB_CERR_RPT_REG	0x000000000D01084B	1885
PE0.PB0.PBAIB.REGS.STACK#0.REGS.PFIRACTION0_REG	0x000000000D010846	1883
PE0.PB0.PBAIB.REGS.STACK#0.REGS.PFIRACTION1_REG	0x000000000D010847	1884
PE0.PB0.PBAIB.REGS.STACK#0.REGS.PFIRMASK_REG	0x000000000D010843	1883
PE0.PB0.PBAIB.REGS.STACK#0.REGS.PFIRWOF_REG	0x000000000D010848	1884
PE0.PB0.PBAIB.REGS.STACK#0.REGS.PFIR_REG	0x000000000D010840	1883
PE0.PB0.PBAIB.REGS.STACK#0.REGS.PHBRESET_REG	0x000000000D01084A	1885
PE0.PB0.PBAIB.REGS.STACK#1.REGS.PBAIB_CERR_RPT_REG	0x000000000D01088B	1888
PE0.PB0.PBAIB.REGS.STACK#1.REGS.PFIRACTION0_REG	0x000000000D010886	1886
PE0.PB0.PBAIB.REGS.STACK#1.REGS.PFIRACTION1_REG	0x000000000D010887	1887
PE0.PB0.PBAIB.REGS.STACK#1.REGS.PFIRMASK_REG	0x000000000D010883	1886
PE0.PB0.PBAIB.REGS.STACK#1.REGS.PFIRWOF_REG	0x000000000D010888	1887
PE0.PB0.PBAIB.REGS.STACK#1.REGS.PFIR_REG	0x000000000D010880	1886
PE0.PB0.PBAIB.REGS.STACK#1.REGS.PHBRESET_REG	0x000000000D01088A	1888
PE0.PB0.PBAIB.REGS.STACK#2.REGS.PBAIB_CERR_RPT_REG	0x000000000D0108CB	1891
PE0.PB0.PBAIB.REGS.STACK#2.REGS.PFIRACTION0_REG	0x000000000D0108C6	1889
PE0.PB0.PBAIB.REGS.STACK#2.REGS.PFIRACTION1_REG	0x000000000D0108C7	1890
PE0.PB0.PBAIB.REGS.STACK#2.REGS.PFIRMASK_REG	0x000000000D0108C3	1889
PE0.PB0.PBAIB.REGS.STACK#2.REGS.PFIRWOF_REG	0x000000000D0108C8	1890
PE0.PB0.PBAIB.REGS.STACK#2.REGS.PFIR_REG	0x000000000D0108C0	1889
PE0.PB0.PBAIB.REGS.STACK#2.REGS.PHBRESET_REG	0x000000000D0108CA	1891
PE0.PHB0.ETUX16.RSB_PHB03.RSB.REGS.ACT0_REG	0x000000000D01090E	1897
PE0.PHB0.ETUX16.RSB_PHB03.RSB.REGS.ACTION1_REG	0x000000000D01090F	1899
PE0.PHB0.ETUX16.RSB_PHB03.RSB.REGS.FIR_REG	0x000000000D010908	1892
PE0.PHB0.ETUX16.RSB_PHB03.RSB.REGS.MASK_REG	0x000000000D01090B	1895
PE0.PHB0.ETUX16.RSB_PHB03.RSB.REGS.WOF_REG	0x000000000D010910	1901
TP.TCPCI0.PCI0.BIST	0x000000000D03000B	1917
TP.TCPCI0.PCI0.CC_ATOMIC_LOCK_REG	0x000000000D0303FF	1926
TP.TCPCI0.PCI0.CC_PROTECT_MODE_REG	0x000000000D0303FE	1925
TP.TCPCI0.PCI0.CLK_REGION	0x000000000D030006	1913
TP.TCPCI0.PCI0.CLOCK_STAT_ARY	0x000000000D03000A	1916
TP.TCPCI0.PCI0.CLOCK_STAT_NSL	0x000000000D030009	1915
TP.TCPCI0.PCI0.CLOCK_STAT_SL	0x000000000D030008	1914
TP.TCPCI0.PCI0.CPLT_CONF0	0x000000000D000008	1855
TP.TCPCI0.PCI0.CPLT_CONF1	0x000000000D000009	1856

Mnemonic	Address	Page
TP.TCPCI0.PCI0.CPLT_CTRL0	0x000000000D000000	1852
TP.TCPCI0.PCI0.CPLT_CTRL1	0x000000000D000001	1854
TP.TCPCI0.PCI0.CPLT_MASK0	0x000000000D000101	1858
TP.TCPCI0.PCI0.CPLT_STAT0	0x000000000D000100	1857
TP.TCPCI0.PCI0.CTRL_ATOMIC_LOCK_REG	0x000000000D0003FF	1858
TP.TCPCI0.PCI0.CTRL_PROTECT_MODE_REG	0x000000000D0003FE	1858
TP.TCPCI0.PCI0.DBG_CBS_CC	0x000000000D030013	1924
TP.TCPCI0.PCI0.EPS.DBG.DBG_INST1_COND_REG_1	0x000000000D0107C1	1869
TP.TCPCI0.PCI0.EPS.DBG.DBG_INST1_COND_REG_2	0x000000000D0107C2	1871
TP.TCPCI0.PCI0.EPS.DBG.DBG_INST1_COND_REG_3	0x000000000D0107C3	1872
TP.TCPCI0.PCI0.EPS.DBG.DBG_INST2_COND_REG_1	0x000000000D0107C4	1873
TP.TCPCI0.PCI0.EPS.DBG.DBG_INST2_COND_REG_2	0x000000000D0107C5	1875
TP.TCPCI0.PCI0.EPS.DBG.DBG_INST2_COND_REG_3	0x000000000D0107C6	1876
TP.TCPCI0.PCI0.EPS.DBG.DBG_MODE_REG	0x000000000D0107C0	1868
TP.TCPCI0.PCI0.EPS.DBG.DBG_TRACE_MODE_REG_2	0x000000000D0107CF	1880
TP.TCPCI0.PCI0.EPS.DBG.DBG_TRACE_REG_0	0x000000000D0107CD	1877
TP.TCPCI0.PCI0.EPS.DBG.DBG_TRACE_REG_1	0x000000000D0107CE	1879
TP.TCPCI0.PCI0.EPS.DBG.DEBUG_TRACE_CONTROL	0x000000000D0107D0	1881
TP.TCPCI0.PCI0.EPS.DBG.XTRA_TRACE_MODE	0x000000000D0107D1	1881
TP.TCPCI0.PCI0.EPS.FIR.GXSTOP0_MASK_REG	0x000000000D040014	1932
TP.TCPCI0.PCI0.EPS.FIR.GXSTOP1_MASK_REG	0x000000000D040015	1933
TP.TCPCI0.PCI0.EPS.FIR.GXSTOP2_MASK_REG	0x000000000D040016	1933
TP.TCPCI0.PCI0.EPS.FIR.GXSTOP_TRIG_REG	0x000000000D040013	1931
TP.TCPCI0.PCI0.EPS.FIR.LOCAL_FIR_ACTION0	0x000000000D040010	1931
TP.TCPCI0.PCI0.EPS.FIR.LOCAL_FIR_ACTION1	0x000000000D040011	1931
TP.TCPCI0.PCI0.EPS.FIR.LOCAL_FIR_MASK	0x000000000D04000D	1931
TP.TCPCI0.PCI0.EPS.FIR.MODE_REG	0x000000000D040008	1928
TP.TCPCI0.PCI0.EPS.FIR.SUM_MASK_REG	0x000000000D040017	1934
TP.TCPCI0.PCI0.EPS.PSC.PSC.ADDR_TRAP_REG	0x000000000D010003	1861
TP.TCPCI0.PCI0.EPS.PSC.PSC.ATOMIC_LOCK_MASK_LATCH_REG	0x000000000D010007	1863
TP.TCPCI0.PCI0.EPS.PSC.PSC.PSCOM_ERROR_MASK	0x000000000D010002	1861
TP.TCPCI0.PCI0.EPS.PSC.PSC.PSCOM_MODE_REG	0x000000000D010000	1859
TP.TCPCI0.PCI0.EPS.PSC.PSC.PSCOM_STATUS_ERROR_REG	0x000000000D010001	1859
TP.TCPCI0.PCI0.EPS.PSC.PSC.RING_FENCE_MASK_LATCH_REG	0x000000000D010008	1863
TP.TCPCI0.PCI0.EPS.PSC.PSC.WRITE_PROTECT_ENABLE_REG	0x000000000D010005	1862
TP.TCPCI0.PCI0.EPS.PSC.PSC.WRITE_PROTECT_RINGS_REG	0x000000000D010006	1862
TP.TCPCI0.PCI0.EPS.THERM.CONTROL_REG	0x000000000D050012	1939
TP.TCPCI0.PCI0.EPS.THERM.DTS_RESULT0	0x000000000D050000	1935
TP.TCPCI0.PCI0.EPS.THERM.DTS_TRC_RESULT	0x000000000D050003	1936
TP.TCPCI0.PCI0.EPS.THERM.ERR_STATUS_REG	0x000000000D050013	1939
TP.TCPCI0.PCI0.EPS.THERM.INJECT_REG	0x000000000D050011	1938
TP.TCPCI0.PCI0.EPS.THERM.SKITTER_CLKSRC_REG	0x000000000D050016	1941
TP.TCPCI0.PCI0.EPS.THERM.SKITTER_DATA0	0x000000000D050019	1941
TP.TCPCI0.PCI0.EPS.THERM.SKITTER_DATA1	0x000000000D05001A	1942
TP.TCPCI0.PCI0.EPS.THERM.SKITTER_DATA2	0x000000000D05001B	1942
TP.TCPCI0.PCI0.EPS.THERM.SKITTER_FORCE_REG	0x000000000D050014	1941
TP.TCPCI0.PCI0.EPS.THERM.SKITTER_MODE_REG	0x000000000D050010	1937
TP.TCPCI0.PCI0.EPS.THERM.THERM_MODE_REG	0x000000000D05000F	1936

Mnemonic	Address	Page
TP.TCPCI0.PCI0.EPS.THERM.TIMESTAMP_COUNTER_READ	0x000000000D05001C	1942
TP.TCPCI0.PCI0.ERROR_STATUS	0x000000000D03000F	1921
TP.TCPCI0.PCI0.FIR_MASK	0x000000000D040002	1927
TP.TCPCI0.PCI0.HOSTATTN	0x000000000D040009	1928
TP.TCPCI0.PCI0.HOSTATTN_MASK	0x000000000D04001A	1935
TP.TCPCI0.PCI0.LOCAL_FIR	0x000000000D04000A	1929
TP.TCPCI0.PCI0.LOCAL_XSTOP_ERR	0x000000000D040018	1934
TP.TCPCI0.PCI0.LOCAL_XSTOP_MASK	0x000000000D040019	1935
TP.TCPCI0.PCI0.OPCG_ALIGN	0x000000000D030001	1909
TP.TCPCI0.PCI0.OPCG_CAPT1	0x000000000D030010	1922
TP.TCPCI0.PCI0.OPCG_CAPT2	0x000000000D030011	1923
TP.TCPCI0.PCI0.OPCG_CAPT3	0x000000000D030012	1924
TP.TCPCI0.PCI0.OPCG_REG0	0x000000000D030002	1909
TP.TCPCI0.PCI0.OPCG_REG1	0x000000000D030003	1910
TP.TCPCI0.PCI0.OPCG_REG2	0x000000000D030004	1911
TP.TCPCI0.PCI0.RFIR	0x000000000D040001	1926
TP.TCPCI0.PCI0.SCAN_REGION_TYPE	0x000000000D030005	1912
TP.TCPCI0.PCI0.SPATTN	0x000000000D040004	1927
TP.TCPCI0.PCI0.SPA_MASK	0x000000000D040007	1928
TP.TCPCI0.PCI0.SYNC_CONFIG	0x000000000D030000	1908
TP.TCPCI0.PCI0.TRA0.TR0.TRACE_HI_DATA_REG	0x000000000D010400	1863
TP.TCPCI0.PCI0.TRA0.TR0.TRACE_LO_DATA_REG	0x000000000D010401	1863
TP.TCPCI0.PCI0.TRA0.TR0.TRACE_TRCTRL_CONFIG	0x000000000D010402	1864
TP.TCPCI0.PCI0.TRA0.TR0.TRACE_TRDATA_CONFIG_0	0x000000000D010403	1864
TP.TCPCI0.PCI0.TRA0.TR0.TRACE_TRDATA_CONFIG_1	0x000000000D010404	1865
TP.TCPCI0.PCI0.TRA0.TR0.TRACE_TRDATA_CONFIG_2	0x000000000D010405	1865
TP.TCPCI0.PCI0.TRA0.TR0.TRACE_TRDATA_CONFIG_3	0x000000000D010406	1865
TP.TCPCI0.PCI0.TRA0.TR0.TRACE_TRDATA_CONFIG_4	0x000000000D010407	1866
TP.TCPCI0.PCI0.TRA0.TR0.TRACE_TRDATA_CONFIG_5	0x000000000D010408	1866
TP.TCPCI0.PCI0.TRA0.TR0.TRACE_TRDATA_CONFIG_9	0x000000000D010409	1866
TP.TCPCI0.PCI0.XFIR	0x000000000D040000	1926
TP.TCPCI0.PCI0.XSTOP1	0x000000000D03000C	1918
TP.TCPCI0.PCI0.XSTOP2	0x000000000D03000D	1919
TP.TCPCI0.PCI0.XSTOP3	0x000000000D03000E	1920

The POWER9 processor registers are listed in the following tables.

Register Name	Chiplet Control Register 0		
Mnemonic	TP.TCPCI0.PCI0.CPLT_CTRL0		
Address	PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
	000000000D000000 (SCOM) 000000000D000010 (SCOM1) 000000000D000020 (SCOM2)	000000000E000000 (SCOM) 000000000E000010 (SCOM1) 000000000E000020 (SCOM2)	000000000F000000 (SCOM) 000000000F000010 (SCOM1) 000000000F000020 (SCOM2)
Description	This register contains the first set of vital chiplet controls.		

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_OR	WO_CLEAR	CTRL_CC_ABSTCLK_MUXSEL_DC: Select ABIST clock source for the arrays on the chiplet boundary. When this bit is set to 1, clocks are used from from the chiplet with ABIST.
1	RW	WO_OR	WO_CLEAR	TC_UNIT_SYNCCLK_MUXSEL_DC: Select the sync clock for asynchronous latches (initialization value = 1).
2	RW	WO_OR	WO_CLEAR	CTRL_CC_FLUSHMODE_INH_DC: Prevent pipeline latches from going into flush mode (initialization value = 1).
3	RW	WO_OR	WO_CLEAR	CTRL_CC_FORCE_ALIGN_DC: Force the align signal to be sent (initialization value = 1, drop before dropping flushmode_inh).
4	RW	WO_OR	WO_CLEAR	TC_UNIT_ARY_WRT_THRU_DC: Set array into write-through mode, used for LBIST.
5	RW	WO_OR	WO_CLEAR	TC_UNIT_AVP_MODE: AVP mode. Switches the refresh pulse to phase counter.
6	RW	WO_OR	WO_CLEAR	FREE_USAGE_6A: Free usage.
7	RW	WO_OR	WO_CLEAR	FREE_USAGE_7A: Free usage.
8	RW	WO_OR	WO_CLEAR	CTRL_CC_ABIST_RECOV_DISABLE_DC: New signal to disable recovery.
9	RW	WO_OR	WO_CLEAR	FREE_USAGE_9A: Free usage.
10	RW	WO_OR	WO_CLEAR	TC_UNIT_IOBIST_TX_WRAP_ENABLE_DC:
11	RW	WO_OR	WO_CLEAR	RESERVED_11A: Reserved.
12	RW	WO_OR	WO_CLEAR	TC_SKIT_MODE_BIST_DC:
13	RW	WO_OR	WO_CLEAR	TC_UNIT_DETERMINISTIC_TEST_ENABLE_DC: Forces login into deterministic test mode; for example, for LBIST.
14	RW	WO_OR	WO_CLEAR	TC_UNIT_CONSTRAIN_SAFESCAN_DC: Safe scan of N1L latches. Prevent a lock when switching SE.
15	RW	WO_OR	WO_CLEAR	TC_UNIT_RRFA_TEST_ENABLE_DC:
16	RW	WO_OR	WO_CLEAR	TC_NBTI_HDR_ENABLE_OVR_DC: NBTI.
17	RW	WO_OR	WO_CLEAR	TC_NBTI_PROBE_GATE_DC: NBTI.
18	RW	WO_OR	WO_CLEAR	RESERVED_18A: Reserved.
19	RW	WO_OR	WO_CLEAR	RESERVED_19A: Reserved.
20:27	RW	WO_OR	WO_CLEAR	TC_PSRO_SEL_DC: PSRO select.
28	RW	WO_OR	WO_CLEAR	TC_BSC_WRAPSEL_DC: Wrap select for BSC.
29	RW	WO_OR	WO_CLEAR	TC_BSC_INTMODE_DC: INT Mode for BSC.
30	RW	WO_OR	WO_CLEAR	TC_BSC_INV_DC: INV for BSC mode.
31	RW	WO_OR	WO_CLEAR	TC_BSC_EXTMODE_DC: EXT mode for BSC.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
32	RW	WO_OR	WO_CLEAR	TC_REFCLK_DRVR_EN_DC: Reference clock driver enable.
33	RW	WO_OR	WO_CLEAR	RESERVED_33A: Reserved.
34	RW	WO_OR	WO_CLEAR	RESERVED_34A: Reserved.
35	RW	WO_OR	WO_CLEAR	RESERVED_35A: Reserved.
36	RW	WO_OR	WO_CLEAR	TC_OELCC_EDGE_DELAYED_DC: Allows to delay the align by one fast cycle. Only used in dual-mesh chiplets.
37	RW	WO_OR	WO_CLEAR	TC_OELCC_ALIGN_FLUSH_DC: Forces the alignment and odd/even toggling latch into flush state. For DFT only.
38	RW	WO_OR	WO_CLEAR	RESERVED_38A: Reserved.
39	RW	WO_OR	WO_CLEAR	RESERVED_39A: Reserved.
40:41	RW	WO_OR	WO_CLEAR	CTRL_MISC_CLKDIV_SEL_DC: Clock divider select 00 = 1024:1 01 = 64:1 10 = 16:1 11 = 4:1
42	RW	WO_OR	WO_CLEAR	RESERVED_42A: Reserved.
43	RW	WO_OR	WO_CLEAR	RESERVED_43A: Reserved.
44	RW	WO_OR	WO_CLEAR	CTRL_CC_DCTEST_DC: TE = 1 only; enable DCTEST.
45	RW	WO_OR	WO_CLEAR	CTRL_CC_OTP_PRGMODE_DC: TE = 1 only; OTP ROM program mode.
46	RW	WO_OR	WO_CLEAR	CTRL_CC_SSS_CALIBRATE_DC: TE = 1 only; sensors calibration.
47	RW	WO_OR	WO_CLEAR	CTRL_CC_PIN_LBIST_DC: TE = 1 only; PIN LBIST mode. LBIST is controlled via PIN, not by OPCG.
48	RW	WO_OR	WO_CLEAR	FREE_USAGE_48A: Free usage.
49	RW	WO_OR	WO_CLEAR	FREE_USAGE_49A: Free usage.
50	RW	WO_OR	WO_CLEAR	FREE_USAGE_50A: Free usage.
51	RW	WO_OR	WO_CLEAR	FREE_USAGE_51A: Free usage.
52	RW	WO_OR	WO_CLEAR	FREE_USAGE_52A: Free usage.
53	RW	WO_OR	WO_CLEAR	FREE_USAGE_53A: Free usage.
54	RW	WO_OR	WO_CLEAR	FREE_USAGE_54A: Free usage.
55	RW	WO_OR	WO_CLEAR	FREE_USAGE_55A: Free usage.
56	RW	WO_OR	WO_CLEAR	FREE_USAGE_56A: Free usage.
57	RW	WO_OR	WO_CLEAR	FREE_USAGE_57A: Free usage.
58	RW	WO_OR	WO_CLEAR	FREE_USAGE_58A: Free usage.
59	RW	WO_OR	WO_CLEAR	FREE_USAGE_59A: Free usage.
60	RW	WO_OR	WO_CLEAR	FREE_USAGE_60A: Free usage.
61	RW	WO_OR	WO_CLEAR	FREE_USAGE_61A: Free usage.
62	RW	WO_OR	WO_CLEAR	FREE_USAGE_62A: Free usage.
63	RW	WO_OR	WO_CLEAR	FREE_USAGE_63A: Free usage.

Register Name	Chiplet Control Register 1
Mnemonic	TP.TCPCI0.PCI0.CPLT_CTRL1
Address	
Description	This register contains the second set of vital chiplet controls.

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D000001 (SCOM) 000000000D000011 (SCOM1) 000000000D000021 (SCOM2)	000000000E000001 (SCOM) 000000000E000011 (SCOM1) 000000000E000021 (SCOM2)	000000000F000001 (SCOM) 000000000F000011 (SCOM1) 000000000F000021 (SCOM2)

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_OR	WO_CLEAR	UNUSED_0B: Unused.
1	RW	WO_OR	WO_CLEAR	UNUSED_1B: Unused.
2	RW	WO_OR	WO_CLEAR	UNUSED_2B: Unused.
3	RW	WO_OR	WO_CLEAR	TC_VITL_REGION_FENCE: VITL Fence. Protect bleeding into VITL during LBIST, or when the chiplet is not yet initialized and running.
4	RW	WO_OR	WO_CLEAR	TC_PERV_REGION_FENCE: Fence for the pervasive region.
5	RW	WO_OR	WO_CLEAR	TC_REGION1_FENCE: Fence for region unit1.
6	RW	WO_OR	WO_CLEAR	TC_REGION2_FENCE: Fence for region unit2.
7	RW	WO_OR	WO_CLEAR	UNUSED_7B: Unused.
8	RW	WO_OR	WO_CLEAR	UNUSED_8B: Unused.
9	RW	WO_OR	WO_CLEAR	UNUSED_9B: Unused.
10	RW	WO_OR	WO_CLEAR	UNUSED_10B: Unused.
11	RW	WO_OR	WO_CLEAR	UNUSED_11B: Unused.
12	RW	WO_OR	WO_CLEAR	UNUSED_12B: Unused.
13	RW	WO_OR	WO_CLEAR	UNUSED_13B: Unused.
14	RW	WO_OR	WO_CLEAR	UNUSED_14B: Unused.
15	RW	WO_OR	WO_CLEAR	Reserved.
16	RW	WO_OR	WO_CLEAR	TC_UNIT_MULTICYCLE_TEST_FENCE:
17	RW	WO_OR	WO_CLEAR	UNUSED_17B: Unused.
18	RW	WO_OR	WO_CLEAR	UNUSED_18B: Unused.
19	RW	WO_OR	WO_CLEAR	UNUSED_19B: Unused.
20	RW	WO_OR	WO_CLEAR	UNUSED_20B: Unused.
21	RW	WO_OR	WO_CLEAR	UNUSED_21B: Unused.
22	RW	WO_OR	WO_CLEAR	UNUSED_22B: Unused.
23	RW	WO_OR	WO_CLEAR	UNUSED_23B: Unused.
24	RW	WO_OR	WO_CLEAR	UNUSED_24B: Unused.
25	RW	WO_OR	WO_CLEAR	UNUSED_25B: Unused.
26	RW	WO_OR	WO_CLEAR	UNUSED_26B: Unused.
27	RW	WO_OR	WO_CLEAR	UNUSED_27B: Unused.
28	RW	WO_OR	WO_CLEAR	UNUSED_28B: Unused.
29	RW	WO_OR	WO_CLEAR	UNUSED_29B: Unused.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
30	RW	WO_OR	WO_CLEAR	UNUSED_30B: Unused.
31	RW	WO_OR	WO_CLEAR	UNUSED_31B: Unused.

Register Name	Chiplet Configuration Register 0
Mnemonic	TP.TCPCI0.PCI0.CPLT_CONF0
Address	
Description	This register contains the first set of vital chiplet configuration functions.

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D000008 (SCOM) 000000000D000018 (SCOM1) 000000000D000028 (SCOM2)	000000000E000008 (SCOM) 000000000E000018 (SCOM1) 000000000E000028 (SCOM2)	000000000F000008 (SCOM) 000000000F000018 (SCOM1) 000000000F000028 (SCOM2)

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:5	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE0_SEL_DC: Probe 0 select.
6	RW	WO_OR	WO_CLEAR	RESERVED_6C: Reserved.
7	RW	WO_OR	WO_CLEAR	RESERVED_7C: Reserved.
8:13	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE1_SEL_DC: Probe 1 select.
14	RW	WO_OR	WO_CLEAR	RESERVED_14C: Reserved.
15	RW	WO_OR	WO_CLEAR	RESERVED_15C: Reserved.
16:21	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE2_SEL_DC: Probe 2 select.
22	RW	WO_OR	WO_CLEAR	RESERVED_22C: Reserved.
23	RW	WO_OR	WO_CLEAR	RESERVED_23C: Reserved.
24:29	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE3_SEL_DC: Probe 3 select.
30	RW	WO_OR	WO_CLEAR	RESERVED_30C: Reserved.
31	RW	WO_OR	WO_CLEAR	RESERVED_31C: Reserved.
32	RW	WO_OR	WO_CLEAR	CTRL_CC_OFLOW_FEH_SEL_DC: Selects an ABIST overflow or failure indication.
33	RW	WO_OR	WO_CLEAR	CTRL_CC_SCAN_PROTECT_DC: Enables scan protection;enables the scan collision error mechanism.
34	RW	WO_OR	WO_CLEAR	CTRL_CC_SDIS_DC_N: Disables the scan diagnostic scan path.
35	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_35C: Reserved for test control.
36	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_36C: Reserved for test control.
37	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_37C: Reserved for test control.
38	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_38C: Reserved for test control.
39	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_39C: Reserved for test control.
40	RW	WO_OR	WO_CLEAR	CTRL_EPS_MASK_VITL_PCB_ERR_DC: Mask VITL PCB errors from the CC or CPLT_CTRL.
41	RW	WO_OR	WO_CLEAR	CTRL_CC_MASK_VITL_SCAN_OPCG_ERR_DC: Mask VITL errors in the CC that are not PCB related.
42	RW	WO_OR	WO_CLEAR	RESERVED_42C: Reserved.
43	RW	WO_OR	WO_CLEAR	RESERVED_43C: Reserved.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
44	RW	WO_OR	WO_CLEAR	FREE_USAGE_44C: Free usage.
45	RW	WO_OR	WO_CLEAR	FREE_USAGE_45C: Free usage.
46	RW	WO_OR	WO_CLEAR	FREE_USAGE_46C: Free usage.
47	RW	WO_OR	WO_CLEAR	FREE_USAGE_47C: Free usage.
48:51	RW	WO_OR	WO_CLEAR	TC_UNIT_GROUP_ID_DC: Group ID.
52:54	RW	WO_OR	WO_CLEAR	TC_UNIT_CHIP_ID_DC: Chip ID.
55	RW	WO_OR	WO_CLEAR	RESERVED_ID_55C: Reserved ID.
56:60	RW	WO_OR	WO_CLEAR	TC_UNIT_SYS_ID_DC: System ID.
61	RW	WO_OR	WO_CLEAR	RESERVED_ID_61C: Reserved ID.
62	RW	WO_OR	WO_CLEAR	RESERVED_ID_62C: Reserved ID.
63	RW	WO_OR	WO_CLEAR	RESERVED_ID_63C: Reserved ID.

Register Name	Chiplet Configuration Register 1		
Mnemonic	TP.TCPCI0.PCI0.CPLT_CONF1		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D000009 (SCOM) 000000000D000019 (SCOM1) 000000000D000029 (SCOM2)	000000000E000009 (SCOM) 000000000E000019 (SCOM1) 000000000E000029 (SCOM2)	000000000F000009 (SCOM) 000000000F000019 (SCOM1) 000000000F000029 (SCOM2)
Description	This register contains the second set of vital chiplet configuration functions.		

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_OR	WO_CLEAR	UNUSED_0D: Unused.
1	RW	WO_OR	WO_CLEAR	UNUSED_1D: Unused.
2	RW	WO_OR	WO_CLEAR	UNUSED_2D: Unused.
3	RW	WO_OR	WO_CLEAR	UNUSED_3D: Unused.
4	RW	WO_OR	WO_CLEAR	TC_PCI0_IOVALID:
5	RW	WO_OR	WO_CLEAR	IOVALID_5D:
6	RW	WO_OR	WO_CLEAR	IOVALID_6D:
7	RW	WO_OR	WO_CLEAR	IOVALID_7D:
8	RW	WO_OR	WO_CLEAR	IOVALID_8D:
9	RW	WO_OR	WO_CLEAR	IOVALID_9D:
10	RW	WO_OR	WO_CLEAR	IOVALID_10D:
11	RW	WO_OR	WO_CLEAR	IOVALID_11D:
12	RW	WO_OR	WO_CLEAR	TC_PCI0_SWAP_DC:
13:14	RW	WO_OR	WO_CLEAR	TC_PCI0_LANE_CFG_DC:
15	RW	WO_OR	WO_CLEAR	TC_PCI0_RATIO_OVERRIDE:
16:18	RW	WO_OR	WO_CLEAR	TC_PCI0_RATIO_DC:
19	RW	WO_OR	WO_CLEAR	FREE_USAGE_19D: Free usage.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
20	RW	WO_OR	WO_CLEAR	FREE_USAGE_20D: Free usage.
21	RW	WO_OR	WO_CLEAR	FREE_USAGE_21D: Free usage.
22	RW	WO_OR	WO_CLEAR	FREE_USAGE_22D: Free usage.
23	RW	WO_OR	WO_CLEAR	FREE_USAGE_23D: Free usage.
24	RW	WO_OR	WO_CLEAR	FREE_USAGE_24D: Free usage.
25	RW	WO_OR	WO_CLEAR	FREE_USAGE_25D: Free usage.
26	RW	WO_OR	WO_CLEAR	FREE_USAGE_26D: Free usage.
27	RW	WO_OR	WO_CLEAR	FREE_USAGE_27D: Free usage.
28	RW	WO_OR	WO_CLEAR	TC_IOP_SYS_RESET_PCS: For chiplets with NBTI.
29	RW	WO_OR	WO_CLEAR	TC_IOP_SYS_RESET_PMA: For chiplets with NBTI.
30	RW	WO_OR	WO_CLEAR	TC_IOP_HSSPORWREN: For chiplets with NBTI.
31	RW	WO_OR	WO_CLEAR	FREE_USAGE_31D: Free usage.

Register Name	**Chiplet Status Register**
Mnemonic	TP.TCPCI0.PCI0.CPLT_STAT0
Address	**PCI0 (PE0)**: 000000000D000100 (SCOM) **PCI1 (PE1)**: 000000000E000100 (SCOM) **PCI2 (PE2)**: 000000000F000100 (SCOM)
Description	An interrupt is sent out on a bit change if not masked by the Chiplet Mask Register. A mask only masks the interrupt, not the status register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	SRAM_ABIST_DONE_DC: SRAM and eDRAM ABIST done.
1	ROX	DRAM_ABIST_DONE_DC: Unused in POWER9 DD1.
2	ROX	RESERVED_2E: Reserved.
3	ROX	RESERVED_3E: Reserved.
4	ROX	TC_DIAG_PORT0_OUT: Diagnostic output port.
5	ROX	TC_DIAG_PORT1_OUT: Diagnostic output port.
6	ROX	RESERVED_6E: Reserved.
7	ROX	PLL_DESTOUT: Reserved.
8	ROX	CC_CTRL_OPCG_DONE_DC: OPCG done. Used for LBIST, ABIST, or other OPCG runs.
9	ROX	CC_CTRL_CHIPLET_IS_ALIGNED_DC: Indicates that chiplet is aligned.
10	ROX	FREE_USAGE_10E: Free usage.
11	ROX	FREE_USAGE_11E: Free usage.
12	ROX	FREE_USAGE_12E: Free usage.
13	ROX	FREE_USAGE_13E: Free usage.
14	ROX	FREE_USAGE_14E: Free usage.
15	ROX	FREE_USAGE_15E: Free usage.
16	ROX	FREE_USAGE_16E: Free usage.

Bits	SCOM	Field Mnemonic: Description
17	ROX	FREE_USAGE_17E: Free usage.
18	ROX	FREE_USAGE_18E: Free usage.
19	ROX	FREE_USAGE_19E: Free usage.
20	ROX	FREE_USAGE_20E: Free usage.
21	ROX	FREE_USAGE_21E: Free usage.
22	ROX	FREE_USAGE_22E: Free usage.
23	ROX	FREE_USAGE_23E: Free usage.

Register Name	**Chiplet Mask Register**
Mnemonic	TP.TCPCI0.PCI0.CPLT_MASK0
Address	
Description	This register masks an interrupt when a bit changes in the Chiplet Status Register. It does not mask the status itself.

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D000101 (SCOM)	000000000E000101 (SCOM)	000000000F000101 (SCOM)

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CPLTMASK0: This field provides bitwise masking of the Chiplet Status Register.

Register Name	**Control Protect Mode Register**
Mnemonic	TP.TCPCI0.PCI0.CTRL_PROTECT_MODE_REG
Address	
Description	This register enables read and write protection.

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D0003FE (SCOM)	000000000E0003FE (SCOM)	000000000F0003FE (SCOM)

Bits	SCOM	Field Mnemonic: Description
0	RW	CTRL_READ_PROTECT_ENABLE: This bit enables read protection.
1	RW	CTRL_WRITE_PROTECT_ENABLE: This bit enables write protection.

Register Name	**Atomic Lock Register**
Mnemonic	TP.TCPCI0.PCI0.CTRL_ATOMIC_LOCK_REG
Address	
Description	This register enables an atomic lock and an atomic lock counter.

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D0003FF (SCOM)	000000000E0003FF (SCOM)	000000000F0003FF (SCOM)

Bits	SCOM	Field Mnemonic: Description
0	RW	CTRL_ATOMIC_LOCK_ENABLE: This bit enables an atomic lock.
1:4	ROX	CTRL_ATOMIC_ID: This field contains the atomic ID.
5:7	RO	Constant = 0b000
8:15	ROX	CTRL_ATOMIC_ACTIVITY: This field is an atomic lock counter.

Register Name	PSCOMLE Mode Register
Mnemonic	TP.TCPCI0.PCI0.EPS.PSC.PSC.PSCOM_MODE_REG
Address	<table><tr><th>PCI0 (PE0)</th><th>PCI1 (PE1)</th><th>PCI2 (PE2)</th></tr><tr><td>000000000D010000 (SCOM)</td><td>000000000E010000 (SCOM)</td><td>000000000F010000 (SCOM)</td></tr></table>
Description	This is the parallel-to-serial communication light edition (PSCOMLE) mode register.

Bits	SCOM	Field Mnemonic: Description
0	RW	ABORT_ON_PCB_ADDR_PARITY_ERROR: Abort on a PCB address parity error.
1	RW	ABORT_ON_PCB_WDATA_PARITY_ERROR: Abort on a PCB write data parity error.
2	RW	ABORT_ON_DL_RETURN_P0_ERROR: Abort on a DL return P0 error.
3	RW	ABORT_ON_DL_RETURN_WDATA_PARITY_ERROR: Abort on a DL return write data parity error.
4	RW	WATCHDOG_ENABLE: Watchdog enable.
5:6	RW	SCOM_HANG_LIMIT: 11 = 256 10 = 512 01 = 768 00 = 1023
7	RW	FORCE_ALL_RINGS: This bit is set to a logical '1' if all rings must be enable independent of the ring address.
8	RW	FSM_SELFRESET_ON_STATEVEC_PARITYERROR_ENABLE: FSM self-reset on statevec parity error enable.
9:11	RW	RESERVED_PSCOM_MODE_LT: Reserved.

Register Name	PSCOMLE Error Register
Mnemonic	TP.TCPCI0.PCI0.EPS.PSC.PSC.PSCOM_STATUS_ERROR_REG
Address	<table><tr><th>PCI0 (PE0)</th><th>PCI1 (PE1)</th><th>PCI2 (PE2)</th></tr><tr><td>000000000D010001 (SCOM)</td><td>000000000E010001 (SCOM)</td><td>000000000F010001 (SCOM)</td></tr></table>
Description	This is the parallel-to-serial communication light edition (PSCOMLE) error register.

Bits	SCOM	Field Mnemonic: Description
0	RWX	ACCUMULATED_PCB_WDATA_PARITY_ERROR: Accumulated PCB write data parity error.
1	RWX	ACCUMULATED_PCB_ADDRESS_PARITY_ERROR: Accumulated PCB address parity error.
2	RWX	ACCUMULATED_DL_RETURN_WDATA_PARITY_ERROR: Accumulated DL return write data parity error.

Bits	SCOM	Field Mnemonic: Description
3	RWX	ACCUMULATED_DL_RETURN_P0_ERROR: Accumulated DL return P0 error.
4	RWX	ACCUMULATED_UL_RDATA_PARITY_ERROR: Accumulated UL read data parity error.
5	RWX	ACCUMULATED_UL_P0_ERROR: Accumulated UL P0 error.
6	RWX	ACCUMULATED_PARITY_ERROR_ON_INTERFACE_MACHINE: Accumulated parity error on the interface machine.
7	RWX	ACCUMULATED_PARITY_ERROR_ON_P2S_MACHINE: Accumulated parity error on the parallel-to-serial (p2s) machine.
8	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_ULCCH: Accumulated timeout while waiting for ULCCH.
9	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: Accumulated timeout while waiting for DLDCH return.
10	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_ULDCH: Accumulated timeout while waiting for ULDCH.
11	RWX	ACCUMULATED_PSCOM_PARALLEL_WRITE_NVLD: Accumulated PSCOM parallel write NVLD.
12	RWX	ACCUMULATED_PSCOM_PARALLEL_READ_NVLD: Accumulated PSCOM parallel read NVLD.
13	RWX	ACCUMULATED_PSCOM_PARALLEL_ADDR_INVALID: Accumulated PSCOM parallel address invalid.
14	RWX	ACCUMULATED_PCB_COMMAND_PARITY_ERROR: Accumulated PCB command parity error.
15	RWX	ACCUMULATED_GENERAL_TIMEOUT: Accumulated general timeout.
16	RWX	ACCUMULATED_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: Accumulated satellite acknowledge access violation.
17	RWX	ACCUMULATED_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: Accumulated satellite acknowledge invalid register.
18	RWX	TRAPPED_PCB_WDATA_PARITY_ERROR: Trapped PCB write data parity error.
19	RWX	TRAPPED_PCB_ADDRESS_PARITY_ERROR: Trapped PCB address parity error.
20	RWX	TRAPPED_DL_RETURN_WDATA_PARITY_ERROR: Trapped DL return write data parity error.
21	RWX	TRAPPED_DL_RETURN_P0_ERROR: Trapped DL return P0 error.
22	RWX	TRAPPED_UL_RDATA_PARITY_ERROR: Trapped UL read data parity error.
23	RWX	TRAPPED_UL_P0_ERROR: Trapped UL P0 error.
24	RWX	TRAPPED_PARITY_ERROR_ON_INTERFACE_MACHINE: Trapped parity error on the interface machine.
25	RWX	TRAPPED_PARITY_ERROR_ON_P2S_MACHINE: Trapped parity error on the parallel-to-serial (p2s) machine.
26	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_ULCCH: Trapped timeout while waiting for ULCCH.
27	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: Trapped timeout while waiting for DLDCH return.
28	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_ULDCH: Trapped timeout while waiting for ULDCH.
29	RWX	TRAPPED_PSCOM_PARALLEL_WRITE_NVLD: Trapped PSCOM parallel write NVLD.
30	RWX	TRAPPED_PSCOM_PARALLEL_READ_NVLD: Trapped PSCOM parallel read NVLD.
31	RWX	TRAPPED_PSCOM_PARALLEL_ADDR_INVALID: Trapped PSCOM parallel address invalid.
32	RWX	TRAPPED_PCB_COMMAND_PARITY_ERROR: Trapped PCB command parity error.
33	RWX	TRAPPED_GENERAL_TIMEOUT: Trapped general timeout.
34	RWX	TRAPPED_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: Trapped satellite acknowledge access violation.

Bits	SCOM	Field Mnemonic: Description
35	RWX	TRAPPED_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: Trapped satellite acknowledge invalid register.

Register Name	PSCOMLE Error Mask Register
Mnemonic	TP.TCPCI0.PCI0.EPS.PSC.PSC.PSCOM_ERROR_MASK
Address	PCI0 (PE0): 000000000D010002 (SCOM) PCI1 (PE1): 000000000E010002 (SCOM) PCI2 (PE2): 000000000F010002 (SCOM)
Description	This is the parallel-to-serial communication light edition (PSCOMLE) error mask register.

Bits	SCOM	Field Mnemonic: Description
0	RW	MASK_PCB_WDATA_PARITY_ERROR: Mask PCB write data parity error.
1	RW	MASK_PCB_ADDRESS_PARITY_ERROR: Mask PCB address parity error.
2	RW	MASK_DL_RETURN_WDATA_PARITY_ERROR: Mask DL return write data parity error.
3	RW	MASK_DL_RETURN_P0_ERROR: Mask DL return P0 error.
4	RW	MASK_UL_RDATA_PARITY_ERROR: Mask UL read data parity error.
5	RW	MASK_UL_P0_ERROR: Mask UL P0 error.
6	RW	MASK_PARITY_ERROR_ON_INTERFACE_MACHINE: Mask parity error on interface machine.
7	RW	MASK_PARITY_ERROR_ON_P2S_MACHINE: Mask parity error on the parallel-to-serial (p2s) machine.
8	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_ULCCH: Mask timeout while waiting for ULCCH.
9	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: Mask timeout while waiting for DLDCH return.
10	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_ULDCH: Mask timeout while waiting for ULDCH.
11	RW	MASK_PSCOM_PARALLEL_WRITE_NVLD: Mask PSCOM parallel write NVLD.
12	RW	MASK_PSCOM_PARALLEL_READ_NVLD: Mask PSCOM parallel read NVLD.
13	RW	MASK_PSCOM_PARALLEL_ADDR_INVALID: Mask PSCOM parallel address invalid.
14	RW	MASK_PCB_COMMAND_PARITY_ERROR: Mask PCB command parity error.
15	RW	MASK_GENERAL_TIMEOUT: Mask general timeout.
16	RW	MASK_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: Mask satellite acknowledge access violation.
17	RW	MASK_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: Mask satellite acknowledge invalid register.

Register Name	PSCOMLE Address Trap Register
Mnemonic	TP.TCPCI0.PCI0.EPS.PSC.PSC.ADDR_TRAP_REG
Address	PCI0 (PE0): 000000000D010003 (SCOM) PCI1 (PE1): 000000000E010003 (SCOM) PCI2 (PE2): 000000000F010003 (SCOM)
Description	This is the parallel-to-serial communication light edition (PSCOMLE) address trap register.

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	PCB_ADDRESS_OF_LAST_TRANSACTION_WITH_ERROR: This field contains the PCB address of the last transaction with an error.
16	ROX	PCB_READ_NOTWRITE_OF_LAST_TRANSACTION_WITH_ERROR: PCB read, not write, of the last transaction with an error.
17	ROX	RESERVED_ADDR_LAST_TRAP_LT: Reserved 0.
18:30	ROX	SERIAL2PARALLEL_STATE_MACHINE_AT_TIME_OF_ERROR: Serial-to-parallel state machine at the time of the error.
31	ROX	SATELLITE_ACKNOWLEDGE_BIT_RETURN_PARITY: Satellite acknowledge bit. This bit is set to 1 if no parity error is detected in the satellite number or acknowledgment bits.
32	ROX	SATELLITE_ACKNOWLEDGE_BIT_WRITE_PARITY_ERROR: This bit is set if a write parity error is detected by the satellite.
33	ROX	SATELLITE_ACKNOWLEDGE_BIT_ACCESS_VIOLATION: This bit is set if an invalid read or write access is detected by the satellite.
34	ROX	SATELLITE_ACKNOWLEDGE_BIT_INVALID_REGISTER: This bit is set if an invalid register address is detected by the satellite.

Register Name	**Ring Lock Enable Register**
Mnemonic	TP.TCPCI0.PCI0.EPS.PSC.PSC.WRITE_PROTECT_ENABLE_REG
Address	
Description	This register enables the ring lock.

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D010005 (SCOM)	000000000E010005 (SCOM)	000000000F010005 (SCOM)

Bits	SCOM	Field Mnemonic: Description
0	RW	ENABLE_RING_LOCKING: General enable of ring locking upon a write to a specific ring.
1	RW	RESERVED_RING_LOCKING: Reserved.

Register Name	**Write Protect Rings Register**
Mnemonic	TP.TCPCI0.PCI0.EPS.PSC.PSC.WRITE_PROTECT_RINGS_REG
Address	
Description	This register writes ring-protect bit maps.

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D010006 (SCOM)	000000000E010006 (SCOM)	000000000F010006 (SCOM)

Bits	SCOM	Field Mnemonic: Description
0:15	RW	WRITE_PROTECT_RINGS: Writes a protect bit map for each ring.

Register Name	Atomic Lock Mask Register		
Mnemonic	TP.TCPCI0.PCI0.EPS.PSC.PSC.ATOMIC_LOCK_MASK_LATCH_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D010007 (SCOM)	000000000E010007 (SCOM)	000000000F010007 (SCOM)
Description	This register provides a bit mask for atomic locking.		

Bits	SCOM	Field Mnemonic: Description
0:15	RW	ATOMIC_LOCK_MASK: This field provides a bit mask for atomic locking on a ring-by-ring basis.

Register Name	Ring Fence Enable Mask Register		
Mnemonic	TP.TCPCI0.PCI0.EPS.PSC.PSC.RING_FENCE_MASK_LATCH_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D010008 (SCOM)	000000000E010008 (SCOM)	000000000F010008 (SCOM)
Description	This register provides a bit mask for ring fencing.		

Bits	SCOM	Field Mnemonic: Description
0	RO	Constant = 0b0
1:15	RW	RING_FENCE_ENABLE_MASK: This field provides a bit mask for ring fencing on a ring-by-ring basis.

Register Name	Trace Array High Data Register		
Mnemonic	TP.TCPCI0.PCI0.TRA0.TR0.TRACE_HI_DATA_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D010400 (SCOM)	000000000E010400 (SCOM)	000000000F010400 (SCOM)
Description	This register provides the high trace array data.		

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: This field contains trace array data 0:63.

Register Name	Trace Array Low Data Register		
Mnemonic	TP.TCPCI0.PCI0.TRA0.TR0.TRACE_LO_DATA_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D010401 (SCOM)	000000000E010401 (SCOM)	000000000F010401 (SCOM)
Description	This register provides the low trace array data.		

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: These are the bits for the trace array data bits 64:95.
32:41	ROX	TRACE_ADDRESS: Trace address.
42:50	ROX	TRACE_LAST_BANK: Trace last bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace last bank valid.
52	ROX	TRACE_WRITE_ON_RUN: Trace write-on-run indicator.
53	ROX	TRACE_RUNNING: Trace run indicator.
54:63	ROX	TRACE_HOLD_ADDRESS: Trace hold address (pointing to last entry).

Register Name	Trace Control Configuration Register
Mnemonic	TP.TCPCI0.PCI0.TRA0.TR0.TRACE_TRCTRL_CONFIG
Address	PCI0 (PE0): 000000000D010402 (SCOM) PCI1 (PE1): 000000000E010402 (SCOM) PCI2 (PE2): 000000000F010402 (SCOM)
Description	This register contains trace control configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	STORE_ON_TRIG_MODE: This bit enables store-on-trigger mode.
1	RW	WRITE_ON_RUN_MODE: Not implemented. Use bit 0 of TRACE_TRDATA_CONFIG_9 instead. Force an unconditional write when trace_run.
2:9	RW	EXTEND_TRIG_MODE: This field contains the counter value for extended trigger mode.
10	RW	BANK_MODE: This bit enables bank mode.
11	RW	ENH_TRACE_MODE: This bit suppresses writing timestamps in store-on-trigger mode.
12:13	RW	LOCAL_CLOCK_GATE_CONTROL: Local clock gate control selection. x0 = Normal clock gating. x1 = rd_act to trace array turned off.
14:17	RW	TRACE_SELECT_CONTROL: This field is a selector for two sets of external trace bus multiplexers: tra_mux0_sel(0:1) and tra_mux1_sel(0:1).
18:21	RW	SPARE_CONTROL: This field contains spare control bits.

Register Name	Trace Data Configuration Register 0
Mnemonic	TP.TCPCI0.PCI0.TRA0.TR0.TRACE_TRDATA_CONFIG_0
Address	PCI0 (PE0): 000000000D010403 (SCOM) PCI1 (PE1): 000000000E010403 (SCOM) PCI2 (PE2): 000000000F010403 (SCOM)
Description	This register contains a trace data compare mask for bits 0 - 63.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: This field contains a trace data compression mask for trace bus bits 0 - 63. 1 = Record an entry when this bit changes, 0 = Ignore this bit. Setting the mask to all zeros results in no trace entries being recorded just from bit changes.

Register Name	**Trace Data Configuration Register 1**
Mnemonic	TP.TCPCI0.PCI0.TRA0.TR0.TRACE_TRDATA_CONFIG_1
Address	
Description	This register contains a trace data compare mask for bits 64 - 87.

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D010404 (SCOM)	000000000E010404 (SCOM)	000000000F010404 (SCOM)

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: This field contains a trace data compression mask for bits 64 - 87. 1 = Record an entry when this bit changes, 0 = Ignore this bit. Setting the mask to all zeros results in no trace entries being recorded just from bit changes.

Register Name	**Trace Data Configuration Register 2**
Mnemonic	TP.TCPCI0.PCI0.TRA0.TR0.TRACE_TRDATA_CONFIG_2
Address	
Description	This register contains patterns A and B.

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D010405 (SCOM)	000000000E010405 (SCOM)	000000000F010405 (SCOM)

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: Pattern match pattern a 0 - 23.
24:47	RW	PATTERNB: Pattern_match_pattern b 0 - 23.

Register Name	**Trace Data Configuration Register 3**
Mnemonic	TP.TCPCI0.PCI0.TRA0.TR0.TRACE_TRDATA_CONFIG_3
Address	
Description	This register contains patterns C and D.

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D010406 (SCOM)	000000000E010406 (SCOM)	000000000F010406 (SCOM)

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNC: Pattern match pattern C 0 - 23.
24:47	RW	PATTERND: Pattern match pattern D 0 - 23.

Register Name	Trace Data Configuration Register 4		
Mnemonic	TP.TCPCI0.PCI0.TRA0.TR0.TRACE_TRDATA_CONFIG_4		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D010407 (SCOM)	000000000E010407 (SCOM)	000000000F010407 (SCOM)
Description	This register contains masks A and B.		

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: Mask A. These are the mask bits for the pattern A trace data compare function. They are set to 1 to mask off individual bits.
24:47	RW	MASKB: Mask B. These are the mask bits for the pattern B trace data compare function. They are set to 1 to mask off individual bits.

Register Name	Trace Data Configuration Register 5		
Mnemonic	TP.TCPCI0.PCI0.TRA0.TR0.TRACE_TRDATA_CONFIG_5		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D010408 (SCOM)	000000000E010408 (SCOM)	000000000F010408 (SCOM)
Description	This register contains masks C and D.		

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: Mask C.
24:47	RW	MASKD: Mask D.

Register Name	Trace Data Configuration Register 9		
Mnemonic	TP.TCPCI0.PCI0.TRA0.TR0.TRACE_TRDATA_CONFIG_9		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D010409 (SCOM)	000000000E010409 (SCOM)	000000000F010409 (SCOM)
Description	This register contains trace data configuration fields.		

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disable trace data compression (store data every cycle).
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Take into account (care about) changes in the error bit for trace data compression (default = 0).
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 00 = Trace bus bits (00:23). 01 = Trace bus bits (24:47). 10 = Trace bus bits (48:71). 11 = Trace bus bits (72:87) | 8 zeros.

Bits	SCOM	Field Mnemonic: Description
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 00 = Trace bus bits (00:23). 01 = Trace bus bits (24:47). 10 = Trace bus bits (48:71). 11 = Trace bus bits (72:87) | 8 zeros.
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 00 = Trace bus bits (00:23). 01 = Trace bus bits (24:47). 10 = Trace bus bits (48:71). 11 = Trace bus bits (72:87) | 8 zeros.
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 00 = Trace bus bits (00:23). 01 = Trace bus bits (24:47). 10 = Trace bus bits (48:71). 11 = Trace bus bits (72:87) | 8 zeros.
10:13	RW	TRIG0_OR_MASK: Note: The OR of all selected MATCHes is ORd with result of TRIG0_AND. 0b1XXX selects MATCHA OR. 0bX1XX selects MATCHB OR. 0bXX1X selects MATCHC OR. 0bXXX1 selects MATCHD OR. 0b0000 selects to not OR any MATCHes.
14:17	RW	TRIG0_AND_MASK: Note: The AND of following selected MATCHes is ORd with result of TRIG0_OR. 0b1XXX selects MATCHA AND. 0bX1XX selects MATCHB AND. 0bXX1X selects MATCHC AND. 0bXXX1 selects MATCHD AND. 0b0000 selects to not AND any MATCHes together to form TRIG0.
18:21	RW	TRIG1_OR_MASK: Note: The OR of all selected MATCHes is ORd with result of TRIG1_AND. 0b1XXX selects MATCHA OR. 0bX1XX selects MATCHB OR. 0bXX1X selects MATCHC OR. 0bXXX1 selects MATCHD OR. 0b0000 selects to not OR any MATCHes to form TRIG1.
22:25	RW	TRIG1_AND_MASK: Note: The AND of following selected MATCHes is ORd with result of TRIG1_OR. 0b1XXX selects MATCHA AND. 0bX1XX selects MATCHB AND. 0bXX1X selects MATCHC AND. 0bXXX1 selects MATCHD AND. 0b0000 selects to not AND any MATCHes together to form TRIG1.
26	RW	TRIG0_NOT_MODE: Invert TRIG0 before using it.
27	RW	TRIG1_NOT_MODE: Invert TRIG1 before using it.
28:31	RW	MATCH_NOT_MODE: Invert the match polarity before using it to form a TRIGger. 0b1000 inverts MATCHA. 0b0100 inverts MATCHB. 0b0010 inverts MATCHC. 0b0001 inverts MATCHD.
32	RW	ERROR_CMP_MASK: Leave this at 0. It is a trap. (DD1 bug).
33	RW	ERROR_CMP_PATTERN: Value to a compare trace error against.
34	RW	TRIG0_ERR_CMP: Include (via OR) the error comparison result into trig0.

Bits	SCOM	Field Mnemonic: Description
35	RW	TRIG1_ERR_CMP: Include (via OR) the error comparison result into trig1.
36	RW	DD1_STRETCH_TRIGGER_PULSES: (DD1 workaround) Stretches the trigger output pulses to two clocks. This bit must be enabled for MCFAST and L2FAST traces.
37	RW	Spare lt.

Register Name	**Debug Mode Register**
Mnemonic	TP.TCPCI0.PCI0.EPS.DBG.DBG_MODE_REG
Address	
Description	This is debug macro configuration register 0 for the configuration component.

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D0107C0 (SCOM)	000000000E0107C0 (SCOM)	000000000F0107C0 (SCOM)

Bits	SCOM	Field Mnemonic: Description
0:2	RW	GLB_BRCST_MODE: Global broadcast mode (0 - 2): 100 = Debug trace run and debug trace freeze. 101 = Pc tcdbg trace run fncd and debug trace freeze. 110 = Debug triggers out(0 - 1). 111 = Pc tcdbg triggers(0 - 1) (from core).
3:5	RW	TRACE_SEL_MODE: Selects the source for trace_run and bank. 001 = core trace run and bank. 010 = tp broadcast run and 0. 011 = tc_dbg_inter_brcst latched. 100 = tc_dbg_dbg_sync_brcst_rcv. Else = dbg_trace_run and dbg_trace_bank.
6:7	RW	TRIG_SEL_MODE: Selects the source for tcdbg_trigger(0). 10 = global broadcast. 11 = pc_tcdbg_trigger (from core). Else = dbg_triggers_out(0:1).
8	RW	STOP_ON_XSTOP_SELECTION: This bit enables a trace stop on a checkstop.
9	RW	STOP_ON_RECOV_ERR_SELECTION: This bit enables a trace stop on a recoverable error.
10	RW	STOP_ON_SPATTN_SELECTION: This bit enables a trace stop on special attention.
11	RW	FREEZE_SEL_MODE: Select freeze source: 0 = Local debug freeze. 1 = Via broadcast: tp_tcdbg_glb_brcst(1).
12:13	RW	SYNC_BRCST_MODE: Originally used for synchronous broadcast mode; currently unused because obsolete. See trace_sel_mode.
14	RO	Constant = 0b0 sync_brcst_mode.
15	RO	Constant = 0b0
16:31	ROX	dbg_status.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Debug Instance 1 Condition 1 Register		
Mnemonic	TP.TCPCI0.PCI0.EPS.DBG.DBG_INST1_COND_REG_1		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D0107C1 (SCOM)	000000000E0107C1 (SCOM)	000000000F0107C1 (SCOM)
Description	This is debug macro configuration register 1 for front-end component 1.		

Bits	SCOM	Field Mnemonic: Description
0:7	RW	INST1_COND1_SEL_A: Multiplexer for cond1_trig_in(0). 000 = select constant 0 001 = select constant 1 -- CONDITION FEEDBACK -- 002 = select inst1_dbg_cond1. 003 = select inst1_dbg_cond2. 004 = select inst1_dbg_cond3. 005 = select inst1_dbg_cond2timeout. 006 = select inst2_dbg_cond1. 007 = select inst2_dbg_cond2. 008 = select inst2_dbg_cond3. 009 = select inst2_dbg_cond2timeout. 010 = select inst3_dbg_cond1 - unused, tied down. 011 = select inst3_dbg_cond2 - unused, tied down. 012 = select inst3_dbg_cond3 - unused, tied down. 013 = select inst3_dbg_cond2timeout - unused, tied down. 014 = select inst4_dbg_cond1 - unused, tied down. 015 = select inst4_dbg_cond2 - unused, tied down. 016 = select inst4_dbg_cond3 - unused, tied down. 017 = select inst4_dbg_cond2timeout - unused, tied down. 018 = select inst1_dbg_trig_sp. 019 = select inst2_dbg_trig_sp. 020 = select inst3_dbg_trig_sp - unused, tied down. 021 = select inst4_dbg_trig_sp - unused, tied down. 022 = select tctrc_tcdbg_trigger_a(0). 023 = select tctrc_tcdbg_trigger_b(0). 024 = select tctrc_tcdbg_trigger_a(0) and tctrc_tcdbg_trigger_b(0). 025 = select tctrc_tcdbg_trigger_a(1). 026 = select tctrc_tcdbg_trigger_b(1). 027 = select tctrc_tcdbg_trigger_a(1) and tctrc_tcdbg_trigger_b(1). 028 = select tctrc_tcdbg_trigger_a(2). 029 = select tctrc_tcdbg_trigger_b(2). 030 = select tctrc_tcdbg_trigger_a(2) and tctrc_tcdbg_trigger_b(2). 031 = select tctrc_tcdbg_trigger_a(3). 032 = select tctrc_tcdbg_trigger_b(3). 033 = select tctrc_tcdbg_trigger_a(3) and tctrc_tcdbg_trigger_b(3). 034 = select tctrc_tcdbg_trigger_a(4). 035 = select tctrc_tcdbg_trigger_b(4). 036 = select tctrc_tcdbg_trigger_a(4) and tctrc_tcdbg_trigger_b(4). 037 = select tctrc_tcdbg_trigger_a(5). 038 = select tctrc_tcdbg_trigger_b(5). 039 = select tctrc_tcdbg_trigger_a(5) and tctrc_tcdbg_trigger_b(5). 040 = select tctrc_tcdbg_trigger_a(6). 041 = select tctrc_tcdbg_trigger_b(6). 042 = select tctrc_tcdbg_trigger_a(6) and tctrc_tcdbg_trigger_b(6). 043 = select tctrc_tcdbg_trigger_a(7). 044 = select tctrc_tcdbg_trigger_b(7). 045 = select tctrc_tcdbg_trigger_a(7) and tctrc_tcdbg_trigger_b(7). 046 = select tctrc_tcdbg_trigger_a(8). 047 = select tctrc_tcdbg_trigger_b(8). 048 = select tctrc_tcdbg_trigger_a(8) and tctrc_tcdbg_trigger_b(8). 049 = select tctrc_tcdbg_trigger_a(9). 050 = select tctrc_tcdbg_trigger_b(9). 051 = select tctrc_tcdbg_trigger_a(9) and tctrc_tcdbg_trigger_b(9). 052 = select tctrc_tcdbg_trigger_a(10). 053 = select tctrc_tcdbg_trigger_b(10). 054 = select tctrc_tcdbg_trigger_a(10) and tctrc_tcdbg_trigger_b(10). 055 = select tctrc_tcdbg_trigger_a(11). 056 = select tctrc_tcdbg_trigger_b(11). 057 = select tctrc_tcdbg_trigger_a(11) and tctrc_tcdbg_trigger_b(11). 058 = select tctrc_tcdbg_trigger_a(12). 059 = select tctrc_tcdbg_trigger_b(12).

Bits	SCOM	Field Mnemonic: Description
8:15	RW	INST1_COND1_SEL_B: Multiplexer for cond1_trig_in(1). Selection as cond1_trig_in(0).
16:23	RW	INST1_COND2_SEL_A: Multiplexer for cond2_trig_in(0). Selection as cond1_trig_in(0).
24:31	RW	INST1_COND2_SEL_B: Multiplexer for cond2_trig_in(1). Selection as cond1_trig_in(0).
32	RW	INST1_C1_INAROW_MODE: Counter 1 in-a-row mode for front-end instance (or component) 1.
33	RW	INST1_AND_TRIGGER_MODE1: Front-end instance 1 and trigger mode condition 1.
34	RW	INST1_NOT_TRIGGER_MODE1: Front-end instance 1 inverted trigger mode condition 1.
35	RW	INST1_EDGE_TRIGGER_MODE1: Front-end instance 1 edge trigger mode condition 1.
36:38	RWX	INST1_UNUSED_1: UNUSED.
39	RW	INST1_C2_INAROW_MODE: Counter 2 in-a-row mode for front-end instance (or component) 1.
40	RW	INST1_AND_TRIGGER_MODE2: Front-end instance 1 and trigger mode2.
41	RW	INST1_NOT_TRIGGER_MODE2: Front-end instance 1 inverted (not) trigger.
42	RW	INST1_EDGE_TRIGGER_MODE2: Front-end instance 1edge trigger.
43:45	RWX	INST1_UNUSED_2: UNUSED.
46	RW	INST1_COND3_ENABLE_RESET: Front-end instance 1 condition3 enable.
47	RW	INST1_EXACT_TO_MODE: Front-end instance 1 exact timeout mode.
48	RW	INST1_RESET_C2TIMER_ON_C1: Front-end instance 1 reset condition 2 timer on condition 1.
49	RW	INST1_RESET_C3_ON_C0: Front-end instance 1 reset condition 3 on condition 0.
50	RW	INST1_SLOW_TO_MODE: Front-end instance 1 slow timeout mode.
51	RW	INST1_EXACT_RESET_C3_ON_TO: Front-end instance 1 exact reset condition3 on timeout.
52:55	RW	INST1_C1_COUNT_LT: Instance 1 condition 1 counter compare value.
56:59	RW	INST1_C2_COUNT_LT: Instance 1 condition 2 counter compare value.
60:62	RW	INST1_RESET_C3_SELECT: Front-end instance 1: Reset condition 3 for reset_c3_on_c0. 0b100: dbg_cross_couple_triggers(4). 0b101: dbg_cross_couple_triggers(12). 0b110: dbg_cross_couple_triggers(20). 0b111: dbg_cross_couple_triggers(28).

Register Name	**Debug Instance 1 Condition 2 Register**
Mnemonic	TP.TCPCI0.PCI0.EPS.DBG.DBG_INST1_COND_REG_2
Address	
Description	This is debug macro configuration register 2 for front-end component 1.

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D0107C2 (SCOM)	000000000E0107C2 (SCOM)	000000000F0107C2 (SCOM)

Bits	SCOM	Field Mnemonic: Description
0:4	RW	INST1_CROSS_COUPLE_SELECT_1_A: Cross coupling is the same for all selectors: 00000 = selects inst1_cond1_trig_a. 00001 = selects inst1_cond1_trig_b. 00010 = selects inst1_cond2_trig_a. 00011 = selects inst1_cond2_trig_b. 00100 = selects inst1_condition1. 00101 = selects inst1_condition2. 00110 = selects inst1_condition3. 00111 = selects inst1_cond2_timeout. 01000 = selects inst2_cond1_trig_a. 01001 = selects inst2_cond1_trig_b. 01010 = selects inst2_cond2_trig_a. 01011 = selects inst2_cond2_trig_b. 01100 = selects inst2_condition1. 01101 = selects inst2_condition2. 01110 = selects inst2_condition3. 01111 = selects inst2_cond2_timeout. 10000 = selects inst3_cond1_trig_a. 10001 = selects inst3_cond1_trig_b. 10010 = selects inst3_cond2_trig_a. 10011 = selects inst3_cond2_trig_b. 10100 = selects inst3_condition1. 10101 = selects inst3_condition2. 10110 = selects inst3_condition3. 10111 = selects inst3_cond2_timeout. 11000 = selects inst4_cond1_trig_a. 11001 = selects inst4_cond1_trig_b. 11010 = selects inst4_cond2_trig_a. 11011 = selects inst4_cond2_trig_b. 11100 = selects inst4_condition1. 11101 = selects inst4_condition2. 11110 = selects inst4_condition3. 11111 = selects inst4_cond2_timeout.
5:9	RW	INST1_CROSS_COUPLE_SELECT_1_B: Instance 1 cross couple select 1 b.
10:14	RW	INST1_CROSS_COUPLE_SELECT_2_A: Instance 1 cross couple select 2 a.
15:19	RW	INST1_CROSS_COUPLE_SELECT_2_B: Instance 1 cross couple select 2 b.
20:43	RW	INST1_TO_CMP_LT: Compare value for special counter sp_cnt_lt in debug component 1.
44	RW	INST1_FORCE_TEST_MODE: Force test mode to indicate to compare without actual compare.

Register Name	**Debug Instance 1 Condition 3 Register**
Mnemonic	TP.TCPCI0.PCI0.EPS.DBG.DBG_INST1_COND_REG_3
Address	**PCI0 (PE0)**: 000000000D0107C3 (SCOM) **PCI1 (PE1)**: 000000000E0107C3 (SCOM) **PCI2 (PE2)**: 000000000F0107C3 (SCOM)
Description	This is debug macro configuration register 2 for the front-end 1 component.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	INST1_SP_COUNT_LT: Timeout counter to compare value for debug condition component 1.

Register Name	**Debug Instance 2 Condition 1 Register**
Mnemonic	TP.TCPCI0.PCI0.EPS.DBG.DBG_INST2_COND_REG_1
Address	<table><tr><th>PCI0 (PE0)</th><th>PCI1 (PE1)</th><th>PCI2 (PE2)</th></tr><tr><td>000000000D0107C4 (SCOM)</td><td>000000000E0107C4 (SCOM)</td><td>000000000F0107C4 (SCOM)</td></tr></table>
Description	This is debug macro configuration register 1 for the front-end 1 component.

Bits	SCOM	Field Mnemonic: Description
0:7	RW	INST2_COND1_SEL_A: Multiplexer for cond1_trig_in(0). 000 = select constant 0 001 = select constant 1 -- CONDITION FEEDBACK -- 002 = select inst2_dbg_cond1. 003 = select inst2_dbg_cond2. 004 = select inst2_dbg_cond3. 005 = select inst2_dbg_cond2timeout. 006 = select inst2_dbg_cond1. 007 = select inst2_dbg_cond2. 008 = select inst2_dbg_cond3. 009 = select inst2_dbg_cond2timeout. 010 = select inst3_dbg_cond1 - unused, tied down. 011 = select inst3_dbg_cond2 - unused, tied down. 012 = select inst3_dbg_cond3 - unused, tied down. 013 = select inst3_dbg_cond2timeout - unused, tied down. 014 = select inst4_dbg_cond1 - unused, tied down. 015 = select inst4_dbg_cond2 - unused, tied down. 016 = select inst4_dbg_cond3 - unused, tied down. 017 = select inst4_dbg_cond2timeout - unused, tied down. 018 = select inst2_dbg_trig_sp. 019 = select inst2_dbg_trig_sp. 020 = select inst3_dbg_trig_sp - unused, tied down. 021 = select inst4_dbg_trig_sp - unused, tied down. 022 = select tctrc_tcdbg_trigger_a(0). 023 = select tctrc_tcdbg_trigger_b(0). 024 = select tctrc_tcdbg_trigger_a(0) and tctrc_tcdbg_trigger_b(0). 025 = select tctrc_tcdbg_trigger_a(1). 026 = select tctrc_tcdbg_trigger_b(1). 027 = select tctrc_tcdbg_trigger_a(1) and tctrc_tcdbg_trigger_b(1). 028 = select tctrc_tcdbg_trigger_a(2). 029 = select tctrc_tcdbg_trigger_b(2). 030 = select tctrc_tcdbg_trigger_a(2) and tctrc_tcdbg_trigger_b(2). 031 = select tctrc_tcdbg_trigger_a(3). 032 = select tctrc_tcdbg_trigger_b(3). 033 = select tctrc_tcdbg_trigger_a(3) and tctrc_tcdbg_trigger_b(3). 034 = select tctrc_tcdbg_trigger_a(4). 035 = select tctrc_tcdbg_trigger_b(4). 026 = select tctrc_tcdbg_trigger_a(4) and tctrc_tcdbg_trigger_b(4). 027 = select tctrc_tcdbg_trigger_a(5). 028 = select tctrc_tcdbg_trigger_b(5). 029 = select tctrc_tcdbg_trigger_a(5) and tctrc_tcdbg_trigger_b(5). 030 = select tctrc_tcdbg_trigger_a(6). 031 = select tctrc_tcdbg_trigger_b(6). 032 = select tctrc_tcdbg_trigger_a(6) and tctrc_tcdbg_trigger_b(6). 033 = select tctrc_tcdbg_trigger_a(7). 034 = select tctrc_tcdbg_trigger_b(7). 035 = select tctrc_tcdbg_trigger_a(7) and tctrc_tcdbg_trigger_b(7). 036 = select tctrc_tcdbg_trigger_a(8). 037 = select tctrc_tcdbg_trigger_b(8). 038 = select tctrc_tcdbg_trigger_a(8) and tctrc_tcdbg_trigger_b(8). 039 = select tctrc_tcdbg_trigger_a(9). 040 = select tctrc_tcdbg_trigger_b(9). 041 = select tctrc_tcdbg_trigger_a(9) and tctrc_tcdbg_trigger_b(9). 042 = select xstop_err. 043 = select recov_err. 044 = select spattn. 045 = select fir_dbg_local_xstop_err. 046 = select tc_dbg_inter_brcst(0). 047 = select tc_dbg_inter_brcst(1). -- LOGIC (UNIT) TRIGGERS -- EP: 0:3 L3C0, 4:7 L3C1, 8:9 GX, 10 TP (hang), 11 spare, 12:13 MCA, 14:15 spare.

Bits	SCOM	Field Mnemonic: Description
8:15	RW	INST2_COND1_SEL_B: Multiplexer for cond1_trig_in(1). Selection as cond1_trig_in(0).
16:23	RW	INST2_COND2_SEL_A: Multiplexer for cond2_trig_in(0). Selection as cond1_trig_in(0).
24:31	RW	INST2_COND2_SEL_B: Multiplexer for cond2_trig_in(1). Selection as cond1_trig_in(0).
32	RW	INST2_C1_INAROW_MODE: Front-end instance 1 counter 1 in-a-row mode.
33	RW	INST2_AND_TRIGGER_MODE1: Front-end instance 1 and trigger mode condition 1.
34	RW	INST2_NOT_TRIGGER_MODE1: Front-end instance 1 inverted trigger mode condition 1.
35	RW	INST2_EDGE_TRIGGER_MODE1: Front-end instance 1 edge trigger mode condition 1.
36:38	RWX	INST2_UNUSED_1: UNUSED.
39	RW	INST2_C2_INAROW_MODE: Front-end instance 1 counter 2 in-a-row mode.
40	RW	INST2_AND_TRIGGER_MODE2: Front-end instance 1 and trigger mode 2.
41	RW	INST2_NOT_TRIGGER_MODE2: Front-end instance 1 inverted (not) trigger.
42	RW	INST2_EDGE_TRIGGER_MODE2: Front-end instance 1 edge trigger.
43:45	RWX	INST2_UNUSED_2: UNUSED.
46	RW	INST2_COND3_ENABLE_RESET: Front-end instance 1 condition 3 enable.
47	RW	INST2_EXACT_TO_MODE: Front-end instance 1 exact timeout mode.
48	RW	INST2_RESET_C2TIMER_ON_C1: Front-end instance 1 reset condition 2 timer on condition 1.
49	RW	INST2_RESET_C3_ON_C0: Front-end instance 1 reset condition 3 on condition 0.
50	RW	INST2_SLOW_TO_MODE: Front-end instance 1 slow timeout mode.
51	RW	INST2_EXACT_RESET_C3_ON_TO: Front-end instance 1 exact reset condition 3 on timeout.
52:55	RW	INST2_C1_COUNT_LT: Instance 2 condition 1 counter compare value.
56:59	RW	INST2_C2_COUNT_LT: Instance 2 condition 2 counter compare value.
60:62	RW	INST2_RESET_C3_SELECT: Front-end instance 1: Reset condition 3 for reset_c3_on_c0. 100 = dbg_cross_couple_triggers(4). 101 = dbg_cross_couple_triggers(12). 110 = dbg_cross_couple_triggers(20). 111 = dbg_cross_couple_triggers(28).

Register Name	**Debug Instance 2 Condition 2 Register**
Mnemonic	TP.TCPCI0.PCI0.EPS.DBG.DBG_INST2_COND_REG_2
Address	**PCI0 (PE0)**: 000000000D0107C5 (SCOM) **PCI1 (PE1)**: 000000000E0107C5 (SCOM) **PCI2 (PE2)**: 000000000F0107C5 (SCOM)
Description	This is debug macro configuration register 2 for the front-end 1 component.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	INST2_CROSS_COUPLE_SELECT_1_A: Cross coupling is the same for all selectors: 00000 = selects inst2_cond1_trig_a. 00001 = selects inst2_cond1_trig_b. 00010 = selects inst2_cond2_trig_a. 00011 = selects inst2_cond2_trig_b. 00100 = selects inst2_condition1. 00101 = selects inst2_condition2. 00110 = selects inst2_condition3. 00111 = selects inst2_cond2_timeout. 01000 = selects inst2_cond1_trig_a. 01001 = selects inst2_cond1_trig_b. 01010 = selects inst2_cond2_trig_a. 01011 = selects inst2_cond2_trig_b. 01100 = selects inst2_condition1. 01101 = selects inst2_condition2. 01110 = selects inst2_condition3. 01111 = selects inst2_cond2_timeout. 10000 = selects inst3_cond1_trig_a. 10001 = selects inst3_cond1_trig_b. 10010 = selects inst3_cond2_trig_a. 10011 = selects inst3_cond2_trig_b. 10100 = selects inst3_condition1. 10101 = selects inst3_condition2. 10110 = selects inst3_condition3. 10111 = selects inst3_cond2_timeout. 11000 = selects inst4_cond1_trig_a. 11001 = selects inst4_cond1_trig_b. 11010 = selects inst4_cond2_trig_a. 11011 = selects inst4_cond2_trig_b. 11100 = selects inst4_condition1. 11101 = selects inst4_condition2. 11110 = selects inst4_condition3. 11111 = selects inst4_cond2_timeout.
5:9	RW	INST2_CROSS_COUPLE_SELECT_1_B: Instance 2 cross couple select 1 b.
10:14	RW	INST2_CROSS_COUPLE_SELECT_2_A: Instance 2 cross couple select 2 a.
15:19	RW	INST2_CROSS_COUPLE_SELECT_2_B: Instance 2 cross couple select 2 b.
20:43	RW	INST2_TO_CMP_LT: Compare value for special counter sp_cnt_lt in debug component 2.
44	RW	INST2_FORCE_TEST_MODE: Force test mode to indicate to compare without actual compare.

Register Name	Debug Instance 2 Condition 3 Register
Mnemonic	TP.TCPCI0.PCI0.EPS.DBG.DBG_INST2_COND_REG_3
Address	PCI0 (PE0): 000000000D0107C6 (SCOM) PCI1 (PE1): 000000000E0107C6 (SCOM) PCI2 (PE2): 000000000F0107C6 (SCOM)
Description	This is debug macro configuration register 2 for the front-end 1 component.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	INST2_SP_COUNT_LT: Timeout counter to compare value for dbg_cond_comp_1.

Register Name	Debug Trace 0 Register
Mnemonic	TP.TCPCI0.PCI0.EPS.DBG.DBG_TRACE_REG_0
Address	**PCI0 (PE0)**: 000000000D0107CD (SCOM) **PCI1 (PE1)**: 000000000E0107CD (SCOM) **PCI2 (PE2)**: 000000000F0107CD (SCOM)
Description	This is debug macro configuration register 0 for the debug back-end component.

Bits	SCOM	Field Mnemonic: Description
0	RW	INST1_COND3_ENABLE: Enable of instance 1 condition 3.
1	RW	INST2_COND3_ENABLE: Enable of instance 2 condition 3.
2	RW	INST3_COND3_ENABLE: Unused.
3	RW	INST4_COND3_ENABLE: Unused.
4	RW	INST1_SLOW_LFSR_MODE: This bit enables slow LFSR mode for front-end instance 1.
5	RW	INST2_SLOW_LFSR_MODE: This bit enables slow LFSR mode for front-end instance 2.
6	RW	INST3_SLOW_LFSR_MODE: Unused.
7	RW	INST4_SLOW_LFSR_MODE: Unused.
8:9	RW	INST1_CONDITION1_TRIG_SEL: This field selects instance 1 condition 1 for output (external) triggers: 00 = do nothing. 01 = trigger_out(0). 10 = trigger_out(1). 11 = trigger_out(2).
10:11	RW	INST1_CONDITION2_TRIG_SEL: This field selects instance 1 condition 2 for output (external) triggers: 00 = do nothing. 01 = trigger_out(0). 10 = trigger_out(1). 11 = trigger_out(2).
12:13	RW	INST1_C2_TIMEOUT_TRIG_SEL: This field selects instance 1 condition 2 time-out counter for output: 00 = do nothing. 01 = trigger_out(0). 10 = trigger_out(1). 11 = trigger_out(2).
14:15	RW	INST2_CONDITION1_TRIG_SEL: This field selects instance 2 condition 1 for output (external) triggers: 00 = do nothing. 01 = trigger_out(0). 10 = trigger_out(1). 11 = trigger_out(2).
16:17	RW	INST2_CONDITION2_TRIG_SEL: This field selects instance 2 condition 2 trigger for output (external) triggers: 00 = do nothing. 01 = trigger_out(0). 10 = trigger_out(1). 11 = trigger_out(2).
18:19	RW	INST2_C2_TIMEOUT_TRIG_SEL: This field selects instance 2 condition 2 time-out counter for output (external) triggers: 00 = do nothing. 01 = trigger_out(0). 10 = trigger_out(1). 11 = trigger_out(2).
20:31	RO	Constant = 0b000000000000

Bits	SCOM	Field Mnemonic: Description
32	RW	EXT_TRIG_ON_STOP: This bit enables a trigger on stop.
33	RW	EXT_TRIG_ON_FREEZE: This bit enables a trigger on freeze.
34:38	RW	CORE_RAS0_TRIG_SEL:
39:43	RW	CORE_RAS1_TRIG_SEL:
44:45	RW	PC_TP_TRIG_SEL:
46:49	RW	DBG_ARM_SEL:
50:53	RW	TRIG0_LEVEL_SEL: This field selects additional conditions for output (external) trigger signal trigger_out(0). Note: Some are N/A (inst3/4 conditions are tied to zero). 0001 = inst1_cond3_state_int(1). 0010 = inst1_cond3_state_int(0). 0011 = inst2_cond3_state_int(1). 0100 = inst2_cond3_state_int(0). 0101 = inst3_cond3_state_int(1). 0110 = inst3_cond3_state_int(0). 0111 = inst4_cond3_state_int(1). 1000 = inst4_cond3_state_int(0). 1001 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1). 1010 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1). 1011 = inst3_cond3_state_int(1) or inst4_cond3_state_int(1). 1100 = inst3_cond3_state_int(1) and inst4_cond3_state_int(1). 1101 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1). 1110 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1) and inst3_cond3_state_int(1). 1111 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1) or inst4_cond3_state_int(1).
54:57	RW	TRIG1_LEVEL_SEL: This field selects additional conditions for output (external) trigger signal trigger_out(1). Note: Some are N/A (inst3/4 conditions are tied to zero). 0001 = inst1_cond3_state_int(1). 0010 = inst1_cond3_state_int(0). 0011 = inst2_cond3_state_int(1). 0100 = inst2_cond3_state_int(0). 0101 = inst3_cond3_state_int(1). 0110 = inst3_cond3_state_int(0). 0111 = inst4_cond3_state_int(1). 1000 = inst4_cond3_state_int(0). 1001 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1). 1010 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1). 1011 = inst3_cond3_state_int(1) or inst4_cond3_state_int(1). 1100 = inst3_cond3_state_int(1) and inst4_cond3_state_int(1). 1101 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1). 1110 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1) and inst3_cond3_state_int(1). 1111 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1) or inst4_cond3_state_int(1).
58:63	RO	Constant = 0b000000

Register Name	**Debug Trace 1 Register**
Mnemonic	TP.TCPCI0.PCI0.EPS.DBG.DBG_TRACE_REG_1
Address	**PCI0 (PE0)**: 000000000D0107CE (SCOM) **PCI1 (PE1)**: 000000000E0107CE (SCOM) **PCI2 (PE2)**: 000000000F0107CE (SCOM)
Description	This is debug macro configuration register 1 for the back-end component.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	INST1_CONDITION1_ACTION_DO: Instance 1 action selection , condition 1: 00 = Nothing 01 = Start 10 = Stop 11 = Run-N: Start now, stop after n cycles.
2:3	RW	INST1_CONDITION2_ACTION_DO: Instance 1 action selection , condition 2: 00 = Nothing 01 = Start 10 = Stop 11 = Run-N: Start now, stop after n cycles.
4:5	RW	INST1_C2_TIMEOUT_ACTION_DO: Instance 1 action selection , c2_timeout: 00 = Nothing 01 = Start 10 = Stop 11 = Run-N: Start now, stop after n cycles.
6:7	RW	INST2_CONDITION1_ACTION_DO: Instance 2 action selection , condition1: 00 = Nothing 01 = Start 10 = Stop 11 = Run-N: Start now, stop after n cycles.
8:9	RW	INST2_CONDITION2_ACTION_DO: Instance 2 action selection, condition 2: 00 = Nothing 01 = Start 10 = Stop 11 = Run-N: Start now, stop after n cycles.
10:11	RW	INST2_C2_TIMEOUT_ACTION_DO: Instance 2 action selection, c2_timeout: 00 = Nothing 01 = Start 10 = Stop 11 = Run-N: Start now, stop after n cycles.
12:23	RO	Constant = 0b000000000000
24	RW	INST1_CONDITION1_ACTION_WAITN: For wait-N.
25	RW	INST1_CONDITION2_ACTION_WAITN: For wait-N.
26	RW	INST1_C2_TIMEOUT_ACTION_WAITN: For wait-N.
27	RW	INST2_CONDITION1_ACTION_WAITN: For wait-N.
28	RW	INST2_CONDITION2_ACTION_WAITN: For wait-N.
29	RW	INST2_C2_TIMEOUT_ACTION_WAITN: For wait-N.
30:35	RO	Constant = 0b000000
36	RW	INST1_CONDITION1_ACTION_BANK: Trace bank switch (instance 1, condition1).
37	RW	INST1_CONDITION2_ACTION_BANK: Trace bank switch (instance 1, condition2).

Bits	SCOM	Field Mnemonic: Description
38	RW	INST1_C2_TIMEOUT_ACTION_BANK: Trace bank switch (instance 1, c2_timeout).
39	RW	INST2_CONDITION1_ACTION_BANK: Trace bank switch (instance 2, condition1).
40	RW	INST2_CONDITION2_ACTION_BANK: Trace bank switch (instance 2, condition2).
41	RW	INST2_C2_TIMEOUT_ACTION_BANK: Trace bank switch (instance 2, c2_timeout).
42:47	RO	Constant = 0b000000
48:50	RW	INST1_CHECKSTOP_MODE_LT: Select an additional condition with fir_error_lt for dbg_fir_xstop_on_trig output: 000 = inst1_condition1_lt. 001 = inst1_condition2_lt. 010 = inst1_condition3_lt. 011 = inst1_cond2_timeout_lt. 1XX = Disable checkstop_mode.
51	RW	INST1_CHECKSTOP_MODE_SELECTOR: enable_fir_trig_xstop: Enable a checkstop on the debug trigger: 0 = Disable a checkstop on the debug trigger. 1 = Enable a checkstop on the debug trigger.
52:54	RW	INST2_CHECKSTOP_MODE_LT: Select an additional condition with fir_error_lt for dbg_fir_xstop_on_trig output: 000 = inst2_condition1_lt. 001 = inst2_condition2_lt. 010 = inst2_condition3_lt. 011 = inst2_cond2_timeout_lt. 1XX = Disable checkstop_mode.
55	RW	INST2_CHECKSTOP_MODE_SELECTOR: enable_fir_error_xstop: Enable a checkstop on a FIR error: 0 = Disable a checkstop on a FIR error. 1 = Enable a checkstop on a FIR error.
56:63	RO	Constant = 0b00000000

Register Name	**Debug Trace Mode 2 Register**
Mnemonic	TP.TCPCI0.PCI0.EPS.DBG.DBG_TRACE_MODE_REG_2
Address	
Description	This is debug macro configuration register 2 for the back-end component.

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D0107CF (SCOM)	000000000E0107CF (SCOM)	000000000F0107CF (SCOM)

Bits	SCOM	Field Mnemonic: Description
0:15	RW	RUNN_COUNT_COMPARE_VALUE: Compare value for the run-N counter used in trace modes run-N and wait-N.
16	RW	IMM_FREEZE_MODE: Immediate freeze mode.
17	RW	STOP_ON_ERR: Stop and freeze on a checkstop.
18	RW	BANK_ON_RUNN_MATCH: Bank switch on run-N match.
19	RW	FORCE_TEST_MODE: Force run-N condition to be true.
20	RW	ACCUM_HIST_MODE: Accumulate history mode; do not clear history mode when trace_run active.
21	RW	FRZ_COUNT_ON_FRZ: Freeze condition counters on trace freeze.

Register Name	Debug Trace Control Register		
Mnemonic	TP.TCPCI0.PCI0.EPS.DBG.DEBUG_TRACE_CONTROL		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D0107D0 (SCOM)	000000000E0107D0 (SCOM)	000000000F0107D0 (SCOM)
Description	This is the trace start/stop/reset using SCOM command register. Use write data(0/1/2) = 1.		

Bits	SCOM	Field Mnemonic: Description
0	WOX	scom_trace_start. Set to 1 to start a SCOM trace.
1	WOX	scom_trace_stop. Set to 1 to stop a SCOM trace.
2	WOX	scom_trace_reset. Set to 1 to reset a SCOM trace.

Register Name	Extra Trace Mode Register		
Mnemonic	TP.TCPCI0.PCI0.EPS.DBG.XTRA_TRACE_MODE		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D0107D1 (SCOM)	000000000E0107D1 (SCOM)	000000000F0107D1 (SCOM)
Description	This register provides an extra or dedicated trace mode register for core triggers.		

Bits	SCOM	Field Mnemonic: Description
0:37	RW	XTRA_TRACE_MODE_DATA: Extra or dedicated trace mode register for core triggers.

Register Name	PE Bus AIB Mode Bits Register		
Mnemonic	PE0.PB0.PBAIB.REGS.PBAIBHWCFG_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D010800 (SCOM)	000000000E010800 (SCOM)	000000000F010800 (SCOM)
Description	PE Bus AIB Mode Bits		

Bits	SCOM	Field Mnemonic: Description
0:15	RW	Reserved0.
16:18	RW	PE_OSMB_DATASTART_MODE: Mode bits for allowing overcommit of the outbound speed-matching buffer. StartAfterFourBeats (000): Start next packet after 4 data beats. StartAfterFiveBeats (100): Start next packet after 5 data beats. StartAfterSixBeats (101): Start next packet after 6 data beats. StartAfterSevenBeats (110): Start next packet after 7 data beats. StartAfterEightBeats (111): Start next packet after 8 data beats. All others are reserved.
19	RW	Reserved1.

Bits	SCOM	Field Mnemonic: Description
20:23	RW	PE_TX_RESP_HWM: Mode bits for the high water mark for stalling outbound commands. The default is 10.
24:27	RW	PE_TX_RESP_LWM: Mode bits for the low water mark for stalling outbound commands. The default is 0x02.
28:29	RW	PE_OSMB_EARLYEMPTY_MODE: Mode bits for allowing sending outbound SMB empty early. NoEarlyOSMBEmpty (00): Do not send empty toggle early. ThreeEarlyOSMBEmpty (01): Send empty toggle 3 cycles early. FourEarlyOSMBEmpty (10): Send empty toggle 4 cycles early. FiveEarlyOSMBEmpty (11: Send empty toggle 5 cycles early.
30	RW	PE_PCIE_CLK_TRACE_EN: Enable debug tracing of PCI clock signals.
31	RW	PE_SELECT_ETU_TRACE: Choose the debug bus controlled by the ETU register.
32:35	RW	PE_PCI_CLK_TRACE_SEL: Mode bits for selecting what PCI clock domain trace function. Tx_AIB (01): Trace outbound AIB information. Rx_AIB (10): Trace inbound AIB information. ASB (11): Trace ASB transactions.
36:38	RW	PE_ISMB_ERROR_INJECT: Mode bits for injecting inbound SMB errors. NoInject_iSMB (000): No Inject on the inbound the iSMB. Inject_iSMB_parity_error(111): Inject a parity error into the iSMB(control). Inject_iSMB_ECC_ce (100): Inject a correctable ECC error into the iSMB(data). Inject_iSMB_ECC_ue (101): Inject an uncorrectable ECC error into the iSMB(data). Inject_iSMB_ECC_sue (110): Inject a special uncorrectable ECC error into the iSMB(data).
39	RW	Reserved2.
40:42	RW	PE_OSMB_HOL_BLK_CNT: Mode bits for allowing the outbound speed-matching buffer to the head-of-line (HOL) block for a programmable number of cycles. Disabled (000): Disabled. No HOL blocking; if no AIB credit is available, reject the command. Wait04Clocks(100): Enabled. Wait 4 PCI clocks for a credit to become available, then reject. Wait08Clocks(101): Enabled. Wait 8 PCI clocks for a credit to become available, then reject. Wait16Clocks(110): Enabled. Wait 16 PCI clocks for a credit to become available, then reject. Wait32Clocks(111): Enabled. Wait 32 PCI clocks for a credit to become available, then reject.
43:63	RO	Constant = 0b000000000000000000000

Register Name	**PE Secure CAPP SEC Timer BAR Register**
Mnemonic	PE0.PB0.PBAIB.REGS.PECAPP_SEC_BAR
Address	
Description	PE Secure CAPP SEC Timer BAR Register

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D010801 (SCOM)	000000000E010801 (SCOM)	000000000F010801 (SCOM)

Bits	SCOM	Field Mnemonic: Description
0:25	RW	PE_CAPP_SEC_BAR: CAPP SEC Timer Compare Address Register. The address must be on a 1 GB boundary with an offset = 0x00000018.
26:63	RO	Constant = 0b00000000000000000000000000000000000000

Register Name	PCI FIR Register		
Mnemonic	PE0.PB0.PBAIB.REGS.STACK#0.REGS.PFIR_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D010840 (SCOM) 000000000D010841 (SCOM1) 000000000D010842 (SCOM2)	000000000E010840 (SCOM) 000000000E010841 (SCOM1) 000000000E010842 (SCOM2)	000000000F010840 (SCOM) 000000000F010841 (SCOM1) 000000000F010842 (SCOM2)
Description	PCI FIR Register		

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:6	RWX	WOX_AND	WOX_OR	PFIRPFIR: PCI FIR.
7:63	RO	RO	RO	Constant = 0b000000000000000000000000000000000000000000000000000000000

Register Name	PCI FIR Mask Register		
Mnemonic	PE0.PB0.PBAIB.REGS.STACK#0.REGS.PFIRMASK_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D010843 (SCOM) 000000000D010844 (SCOM1) 000000000D010845 (SCOM2)	000000000E010843 (SCOM) 000000000E010844 (SCOM1) 000000000E010845 (SCOM2)	000000000F010843 (SCOM) 000000000F010844 (SCOM1) 000000000F010845 (SCOM2)
Description	PCI FIR Mask Register 0 = No mask. 1 = Mask error.		

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:6	RW	WO_AND	WO_OR	PFIRMASK: PCI FIR mask.
7:63	RO	RO	RO	Constant = 0b000000000000000000000000000000000000000000000000000000000

Register Name	PCI FIR Action0 Register		
Mnemonic	PE0.PB0.PBAIB.REGS.STACK#0.REGS.PFIRACTION0_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D010846 (SCOM)	000000000E010846 (SCOM)	000000000F010846 (SCOM)
Description	PCI FIR Action0 Register		

Bits	SCOM	Field Mnemonic: Description
0:6	RW	PFIRACTION0: Action0 select for the corresponding bit in the FIR. (Action0,Mask) = Action Select. (0,0) = Checkstop error. (0,1) = Recoverable error. (1,0) = No action. (1,1) = Freeze.
7:63	RO	Constant = 0b000000000000000000000000000000000000000000000000000000000

Register Name	PCI FIR Action1 Register		
Mnemonic	PE0.PB0.PBAIB.REGS.STACK#0.REGS.PFIRACTION1_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D010847 (SCOM)	000000000E010847 (SCOM)	000000000F010847 (SCOM)
Description	PCI FIR Action1 Register		

Bits	SCOM	Field Mnemonic: Description
0:6	RW	PFIRACTION1: Action1 select for the corresponding bit in the FIR. (Action1,Mask) = Action Select. (0,0) = Checkstop error. (0,1) = Recoverable error. (1,0) = No action. (1,1) = Freeze.
7:63	RO	Constant = 0b000000000000000000000000000000000000000000000000000000000

Register Name	PCI FIR WOF Register		
Mnemonic	PE0.PB0.PBAIB.REGS.STACK#0.REGS.PFIRWOF_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D010848 (SCOM)	000000000E010848 (SCOM)	000000000F010848 (SCOM)
Description	PCI FIR WOF Register		

Bits	SCOM	Field Mnemonic: Description
0:6	RWX_WCLRREG	Reserved.
7:63	RO	Constant = 0b000000000000000000000000000000000000000000000000000000000

Register Name	ETU Reset Register		
Mnemonic	PE0.PB0.PBAIB.REGS.STACK#0.REGS.PHBRESET_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D01084A (SCOM)	000000000E01084A (SCOM)	000000000F01084A (SCOM)
Description	ETU Reset Register		

Bits	SCOM	Field Mnemonic: Description
0	RW	PE_ETU_RESET: PE ETU global reset.
1:59	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000

Register Name	PBAIB CERR Report Hold Register		
Mnemonic	PE0.PB0.PBAIB.REGS.STACK#0.REGS.PBAIB_CERR_RPT_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D01084B (SCOM)	000000000E01084B (SCOM)	000000000F01084B (SCOM)
Description	PBAIB CERR Report Hold Register		

Bits	SCOM	Field Mnemonic: Description
0	ROX	pbaibhwcfg_pe.
1	ROX	phbreset_pe.
2	ROX	pbaibtxcitr_pe.
3	ROX	pbaibtxccr_pe.
4	ROX	pbaibtxdcr_pe.
5	ROX	peaib_overrun.
6	ROX	peaib_qcnt_err.
7	ROX	peaib_tx_dat_err.
8	ROX	peaib_cmd_pe.
9	ROX	peaib_dat_pe.
10	ROX	peaib_cmd_crd_avail_pe.
11	ROX	peaib_dat_crd_avail_pe.
12	ROX	peaib_cmd_crd_pe.
13	ROX	peaib_dat_crd_pe.
14	ROX	phbreset_scom_err.
15	ROX	async_error.
16	ROX	aib_stack_scom_err.
17	ROX	aib_pec_scom_err.
18	ROX	pbaib_fence_pcie.
19:63	RO	Constant = 0b000000000000000000000000000000000000000000000

Register Name	**PCI FIR Register**
Mnemonic	PE0.PB0.PBAIB.REGS.STACK#1.REGS.PFIR_REG
Address	

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D010880 (SCOM) 000000000D010881 (SCOM1) 000000000D010882 (SCOM2)	000000000E010880 (SCOM) 000000000E010881 (SCOM1) 000000000E010882 (SCOM2)	000000000F010880 (SCOM) 000000000F010881 (SCOM1) 000000000F010882 (SCOM2)

Description	PCI FIR Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:6	RWX	WOX_AND	WOX_OR	PFIRPFIR: PCI FIR.
7:63	RO	RO	RO	Constant = 0b000000000000000000000000000000000000000000000000000000000

Register Name	**PCI FIR Mask Register**
Mnemonic	PE0.PB0.PBAIB.REGS.STACK#1.REGS.PFIRMASK_REG
Address	

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D010883 (SCOM) 000000000D010884 (SCOM1) 000000000D010885 (SCOM2)	000000000E010883 (SCOM) 000000000E010884 (SCOM1) 000000000E010885 (SCOM2)	000000000F010883 (SCOM) 000000000F010884 (SCOM1) 000000000F010885 (SCOM2)

Description	PCI FIR Mask Register 0 = No mask. 1 = Mask error.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:6	RW	WO_AND	WO_OR	PFIRMASK: PCI FIR mask.
7:63	RO	RO	RO	Constant = 0b000000000000000000000000000000000000000000000000000000000

Register Name	**PCI FIR Action0 Register**
Mnemonic	PE0.PB0.PBAIB.REGS.STACK#1.REGS.PFIRACTION0_REG
Address	

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D010886 (SCOM)	000000000E010886 (SCOM)	000000000F010886 (SCOM)

Description	PCI FIR Action0 Register

Bits	SCOM	Field Mnemonic: Description
0:6	RW	PFIRACTION0: Action0 select for the corresponding bit in the FIR. (Action0,Mask) = Action Select. (0,0) = Checkstop error. (0,1) = Recoverable error. (1,0) = No action. (1,1) = Freeze.
7:63	RO	Constant = 0b000000000000000000000000000000000000000000000000000000000

Register Name	**PCI FIR Action1 Register**
Mnemonic	PE0.PB0.PBAIB.REGS.STACK#1.REGS.PFIRACTION1_REG
Address	**PCI0 (PE0)**: 000000000D010887 (SCOM) **PCI1 (PE1)**: 000000000E010887 (SCOM) **PCI2 (PE2)**: 000000000F010887 (SCOM)
Description	PCI FIR Action1 Register

Bits	SCOM	Field Mnemonic: Description
0:6	RW	PFIRACTION1: Action1 select for the corresponding bit in the FIR. (Action1,Mask) = Action Select. (0,0) = Checkstop error. (0,1) = Recoverable error. (1,0) = No action. (1,1) = Freeze.
7:63	RO	Constant = 0b000000000000000000000000000000000000000000000000000000000

Register Name	**PCI FIR WOF Register**
Mnemonic	PE0.PB0.PBAIB.REGS.STACK#1.REGS.PFIRWOF_REG
Address	**PCI0 (PE0)**: 000000000D010888 (SCOM) **PCI1 (PE1)**: 000000000E010888 (SCOM) **PCI2 (PE2)**: 000000000F010888 (SCOM)
Description	PCI FIR WOF register

Bits	SCOM	Field Mnemonic: Description
0:6	RWX_WCLRREG	Reserved.
7:63	RO	Constant = 0b000000000000000000000000000000000000000000000000000000000

Register Name	ETU Reset Register		
Mnemonic	PE0.PB0.PBAIB.REGS.STACK#1.REGS.PHBRESET_REG		
Address	PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
	000000000D01088A (SCOM)	000000000E01088A (SCOM)	000000000F01088A (SCOM)
Description	ETU Reset Register		

Bits	SCOM	Field Mnemonic: Description
0	RW	PE_ETU_RESET: PE ETU global reset.
1:59	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000

Register Name	PBAIB CERR Report Hold Register		
Mnemonic	PE0.PB0.PBAIB.REGS.STACK#1.REGS.PBAIB_CERR_RPT_REG		
Address	PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
	000000000D01088B (SCOM)	000000000E01088B (SCOM)	000000000F01088B (SCOM)
Description	PBAIB CERR Report Hold Register		

Bits	SCOM	Field Mnemonic: Description
0	ROX	pbaibhwcfg_pe.
1	ROX	phbreset_pe.
2	ROX	pbaibtxcitr_pe.
3	ROX	pbaibtxccr_pe.
4	ROX	pbaibtxdcr_pe.
5	ROX	peaib_overrun.
6	ROX	peaib_qcnt_err.
7	ROX	peaib_tx_dat_err.
8	ROX	peaib_cmd_pe.
9	ROX	peaib_dat_pe.
10	ROX	peaib_cmd_crd_avail_pe.
11	ROX	peaib_dat_crd_avail_pe.
12	ROX	peaib_cmd_crd_pe.
13	ROX	peaib_dat_crd_pe.
14	ROX	phbreset_scom_err.
15	ROX	async_error.
16	ROX	aib_stack_scom_err.
17	ROX	aib_pec_scom_err.
18	ROX	pbaib_fence_pcie.
19:63	RO	Constant = 0b000000000000000000000000000000000000000000000

Register Name	PCI FIR Register
Mnemonic	PE0.PB0.PBAIB.REGS.STACK#2.REGS.PFIR_REG
Address	
Description	PCI FIR Register

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D0108C0 (SCOM) 000000000D0108C1 (SCOM1) 000000000D0108C2 (SCOM2)	000000000E0108C0 (SCOM) 000000000E0108C1 (SCOM1) 000000000E0108C2 (SCOM2)	000000000F0108C0 (SCOM) 000000000F0108C1 (SCOM1) 000000000F0108C2 (SCOM2)

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:6	RWX	WOX_AND	WOX_OR	PFIRPFIR: PCI FIR.
7:63	RO	RO	RO	Constant = 0b000000000000000000000000000000000000000000000000000000000

Register Name	PCI FIR Mask Register
Mnemonic	PE0.PB0.PBAIB.REGS.STACK#2.REGS.PFIRMASK_REG
Address	
Description	PCI FIR Mask Register 0 = No mask 1 = Mask error

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D0108C3 (SCOM) 000000000D0108C4 (SCOM1) 000000000D0108C5 (SCOM2)	000000000E0108C3 (SCOM) 000000000E0108C4 (SCOM1) 000000000E0108C5 (SCOM2)	000000000F0108C3 (SCOM) 000000000F0108C4 (SCOM1) 000000000F0108C5 (SCOM2)

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:6	RW	WO_AND	WO_OR	PFIRMASK: PCI FIR mask.
7:63	RO	RO	RO	Constant = 0b000000000000000000000000000000000000000000000000000000000

Register Name	PCI FIR Action0 Register
Mnemonic	PE0.PB0.PBAIB.REGS.STACK#2.REGS.PFIRACTION0_REG
Address	
Description	PCI FIR Action0 Register

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D0108C6 (SCOM)	000000000E0108C6 (SCOM)	000000000F0108C6 (SCOM)

Bits	SCOM	Field Mnemonic: Description
0:6	RW	PFIRACTION0: Action0 select for the corresponding bit in the FIR. (Action0,Mask) = Action Select. (0,0) = Checkstop error. (0,1) = Recoverable error. (1,0) = No action. (1,1) = Freeze.
7:63	RO	Constant = 0b000000000000000000000000000000000000000000000000000000000

Register Name	PCI FIR Action1 Register		
Mnemonic	PE0.PB0.PBAIB.REGS.STACK#2.REGS.PFIRACTION1_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D0108C7 (SCOM)	000000000E0108C7 (SCOM)	000000000F0108C7 (SCOM)
Description	PCI FIR Action1 Register		

Bits	SCOM	Field Mnemonic: Description
0:6	RW	PFIRACTION1: Action1 select for the corresponding bit in the FIR. (Action1,Mask) = Action Select. (0,0) = Checkstop error. (0,1) = Recoverable error. (1,0) = No action. (1,1) = Freeze.
7:63	RO	Constant = 0b000000000000000000000000000000000000000000000000000000000

Register Name	PCI FIR WOF Register		
Mnemonic	PE0.PB0.PBAIB.REGS.STACK#2.REGS.PFIRWOF_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D0108C8 (SCOM)	000000000E0108C8 (SCOM)	000000000F0108C8 (SCOM)
Description	PCI FIR WOF Register		

Bits	SCOM	Field Mnemonic: Description
0:6	RWX_WCLRREG	RESERVED.
7:63	RO	Constant = 0b000000000000000000000000000000000000000000000000000000000

Register Name	**ETU Reset Register**		
Mnemonic	PE0.PB0.PBAIB.REGS.STACK#2.REGS.PHBRESET_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D0108CA (SCOM)	000000000E0108CA (SCOM)	000000000F0108CA (SCOM)
Description	ETU Reset Register		

Bits	SCOM	Field Mnemonic: Description
0	RW	PE_ETU_RESET: PE ETU Global Reset.
1:59	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000

Register Name	**PBAIB CERR Report Hold Register**		
Mnemonic	PE0.PB0.PBAIB.REGS.STACK#2.REGS.PBAIB_CERR_RPT_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D0108CB (SCOM)	000000000E0108CB (SCOM)	000000000F0108CB (SCOM)
Description	PBAIB CERR Report Hold Register		

Bits	SCOM	Field Mnemonic: Description
0	ROX	pbaibhwcfg_pe.
1	ROX	phbreset_pe.
2	ROX	pbaibtxcitr_pe.
3	ROX	pbaibtxccr_pe.
4	ROX	pbaibtxdcr_pe.
5	ROX	peaib_overrun.
6	ROX	peaib_qcnt_err.
7	ROX	peaib_tx_dat_err.
8	ROX	peaib_cmd_pe.
9	ROX	peaib_dat_pe.
10	ROX	peaib_cmd_crd_avail_pe.
11	ROX	peaib_dat_crd_avail_pe.
12	ROX	peaib_cmd_crd_pe.
13	ROX	peaib_dat_crd_pe.
14	ROX	phbreset_scom_err.
15	ROX	async_error.
16	ROX	aib_stack_scom_err.
17	ROX	aib_pec_scom_err.
18	ROX	pbaib_fence_pcie.
19:63	RO	Constant = 0b000000000000000000000000000000000000000000000

Register Name	**ETU FIR Register**
Mnemonic	PE0.PHB0.ETUX16.RSB_PHB03.RSB.REGS.FIR_REG
Address	
Description	ETU FIR Register

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D010908 (SCOM) 000000000D010909 (SCOM1) 000000000D01090A (SCOM2)	000000000E010908 (SCOM) 000000000E010909 (SCOM1) 000000000E01090A (SCOM2)	000000000F010908 (SCOM) 000000000F010909 (SCOM1) 000000000F01090A (SCOM2)

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	AIB_COMMAND_INVALID: See Outbound Error Status Register, bit 0 for details.
1	RWX	WOX_AND	WOX_OR	AIB_ADDRESS_INVALID: See Outbound Error Status Register, bit 1/2 for details.
2	RWX	WOX_AND	WOX_OR	AIB_ACCESS_ERROR: See Outbound Error Status Register, bit 3/8 for details.
3	RWX	WOX_AND	WOX_OR	PAPR_OUTBOUND_INJECT_ERROR: See Outbound Error Status Register, bit 28 for details.
4	RWX	WOX_AND	WOX_OR	AIB_FATAL_CLASS_ERROR: See Outbound Error Status Register, bit 4/5/9/10/11/14/15 for details.
5	RWX	WOX_AND	WOX_OR	AIB_INF_Class_Error.
6	RWX	WOX_AND	WOX_OR	AIB_INF_CLASS_ERROR: See Outbound Error Status Register, bit 6 for details.
7	RWX	WOX_AND	WOX_OR	PE_STOP_STATE_SIGNALED: See Outbound Error Status Register, bit 13/22 for details.
8	RWX	WOX_AND	WOX_OR	OUT_COMMON_ARRAY_FATAL_ERROR: See Outbound Error Status Register, bit 23/37/38/40/43/44/45/47/48/49 for details.
9	RWX	WOX_AND	WOX_OR	OUT_COMMON_LATCH_FATAL_ERROR: See Outbound Error Status Register, bit 50/51/52 for details.
10	RWX	WOX_AND	WOX_OR	OUT_COMMON_LOGIC_FATAL_ERROR: See Outbound Error Status Register, bit 19/20/21/53/54/55 for details.
11	RWX	WOX_AND	WOX_OR	BLIF_OUT_INTERFACE_PARITY_ERROR: See Outbound Error Status Register, bit 16 for details.
12	RWX	WOX_AND	WOX_OR	CFG_WRITE_CA_OR_UR_RESPONSE: See Outbound Error Status Register, bit 17 for details.
13	RWX	WOX_AND	WOX_OR	MMIO_REQUEST_TIMEOUT: See Outbound Error Status Register, bit 18 for details.
14	RWX	WOX_AND	WOX_OR	OUT_RRB_SOURCED_ERROR: See Outbound Error Status Register, bit 56/57 for details.
15	RWX	WOX_AND	WOX_OR	CFG_LOGIC_SIGNALED_ERROR: See Outbound Error Status Register, bit 17 for details.
16	RWX	WOX_AND	WOX_OR	RSB_REG_REQUEST_ADDRESS_ERROR: See RSB Error Status Register, bit 00 for details.
17	RWX	WOX_AND	WOX_OR	RSB_FDA_FATAL_ERROR: See RSB Error Status Register, bit 2/3/5 for details.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
18	RWX	WOX_AND	WOX_OR	RSB_FDA_INF_ERROR: See RSB Error Status Register, bit 1/4 for details.
19	RWX	WOX_AND	WOX_OR	RSB_FDB_FATAL_ERROR: See RSB Error Status Register, bit 9/10 for details.
20	RWX	WOX_AND	WOX_OR	RSB_FDB_INF_ERROR: See RSB Error Status Register, bit 8 for details.
21	RWX	WOX_AND	WOX_OR	RSB_ERR_FATAL_ERROR: See RSB Error Status Register, bit 7 for details.
22	RWX	WOX_AND	WOX_OR	RSB_ERR_INF_ERROR: See RSB Error Status Register, bit 6 for details.
23	RWX	WOX_AND	WOX_OR	RSB_DBG_FATAL_ERROR: See RSB Error Status Register, bit 13/14 for details.
24	RWX	WOX_AND	WOX_OR	RSB_DBG_INF_ERROR: See RSB Error Status Register, bit 12 for details.
25	RWX	WOX_AND	WOX_OR	PCIE_REQUEST_ACCESS_ERROR: See Outbound Error Status Register, bit 11 for details.
26	RWX	WOX_AND	WOX_OR	RSB_BUS_LOGIC_ERROR: See Outbound Error Status Register, bit 15/27 for details.
27	RWX	WOX_AND	WOX_OR	RSB_UVI_FATAL_ERROR: See RSB Error Status Register, bit 17/19 for details.
28	RWX	WOX_AND	WOX_OR	RSB_UVI_INF_ERROR: See RSB Error Status Register, bit 16/18 for details.
29	RWX	WOX_AND	WOX_OR	SCOM_FATAL_ERROR: See RSB Error Status Register, bit 30/31 for details.
30	RWX	WOX_AND	WOX_OR	SCOM_INF_ERROR: See RSB Error Status Register, bit 28/29 for details.
31	RWX	WOX_AND	WOX_OR	PCIE_MACRO_ERROR_ACTIVE_STATUS: See RSB Error Status Register, bit 24/25/26 for details.
32	RWX	WOX_AND	WOX_OR	ARB_IODA_FATAL_ERROR: See ARB Error Status Register, bit 33 for details.
33	RWX	WOX_AND	WOX_OR	ARB_MSI_PE_MATCH_ERROR: See ARB Error Status Register, bit 27 for details.
34	RWX	WOX_AND	WOX_OR	ARB_MSI_ADDRESS_ERROR: See ARB Error Status Register, bit 02/03 for details.
35	RWX	WOX_AND	WOX_OR	ARB_TVT_ERROR: See ARB Error Status Register, bit 26/28 for details.
36	RWX	WOX_AND	WOX_OR	ARB_RCVD_FATAL_ERROR_MSG: See ARB Error Status Register, bit 57 for details.
37	RWX	WOX_AND	WOX_OR	ARB_RCVD_NONFATAL_ERROR_MSG: See ARB Error Status Register, bit 58 for details.
38	RWX	WOX_AND	WOX_OR	ARB_RCVD_CORRECTIBLE_ERROR_MSG: See ARB Error Status Register, bit 59 for details.
39	RWX	WOX_AND	WOX_OR	PAPR_INBOUND_INJECT_ERROR: See Outbound Error Status Register, bit 39 for details.
40	RWX	WOX_AND	WOX_OR	ARB_COMMON_FATAL_ERROR: See ARB Error Status Register, bit 4/7/8/9/10/11/12/13/14/15/16/17/18/22/23/36/37/38/42/43/44/45/46/47/48/59/55/56 for details.
41	RWX	WOX_AND	WOX_OR	ARB_TABLE_BAR_DISABLED_ERROR: See ARB Error Status Register, bit 32/41 for details.
42	RWX	WOX_AND	WOX_OR	ARB_BLIF_COMPLETION_ERROR: See ARB Error Status Register, bit 00/01/19 for details.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
43	RWX	WOX_AND	WOX_OR	ARB_PCT_TIMEOUT_ERROR: See ARB Error Status Register, bit 34/35 for details.
44	RWX	WOX_AND	WOX_OR	ARB_ECC_CORRECTABLE_ERROR: See ARB Error Status Register, bit 5/20/25/29 for details.
45	RWX	WOX_AND	WOX_OR	ARB_ECC_UNCORRECTABLE_ERROR: See ARB Error Status Register, bit 6/26/30/31 for details.
46	RWX	WOX_AND	WOX_OR	ARB_TLP_POISON_SIGNALED: See ARB Error Status Register, bit 24 for details.
47	RWX	WOX_AND	WOX_OR	ARB_RTT_PENUM_INVALID_ERROR: See ARB Error Status Register, bit 40 for details.
48	RWX	WOX_AND	WOX_OR	MRG_COMMON_FATAL_ERROR: See MRG Error Status Register, bit 08-16/22/23/26/28/30-37/40-50 for details.
49	RWX	WOX_AND	WOX_OR	MRG_TABLE_BAR_DISABLED_ERROR: See MRG Error Status Register, bit 51 for details.
50	RWX	WOX_AND	WOX_OR	MRG_ECC_CORRECTABLE_ERROR: See MRG Error Status Register, bit 40/56/58/60 for details.
51	RWX	WOX_AND	WOX_OR	MRG_ECC_UNCORRECTABLE_ERROR: See MRG Error Status Register, bit 41/57/59/61 for details.
52	RWX	WOX_AND	WOX_OR	MRG_AIB2_TX_TIMEOUT_ERROR: See MRG Error Status Register, bit 24 for details.
53	RWX	WOX_AND	WOX_OR	MRG_MRT_ERROR: See MRG Error Status Register, bit 17/18 for details.
54	RWX	WOX_AND	WOX_OR	MRG_Reserved01.
55	RWX	WOX_AND	WOX_OR	MRG_Reserved02.
56	RWX	WOX_AND	WOX_OR	TCE_IODA_PAGE_ACCESS_ERROR: See TCE Error Status Register, bit 01/02 for details.
57	RWX	WOX_AND	WOX_OR	TCE_REQUEST_TIMEOUT_ERROR: See TCE Error Status Register, bit 08 for details.
58	RWX	WOX_AND	WOX_OR	TCE_UNEXPECTED_RESPONSE_ERROR: See TCE Error Status Register, bit 13 for details.
59	RWX	WOX_AND	WOX_OR	TCE_COMMON_FATAL_ERROR: See TCE Error Status Register for details.
60	RWX	WOX_AND	WOX_OR	TCE_ECC_CORRECTABLE_ERROR: See TCE Error Status Register, bit 09/11/25/27 for details.
61	RWX	WOX_AND	WOX_OR	TCE_ECC_UNCORRECTABLE_ERROR: See TCE Error Status Register, bit 10/12/26/28 for details.
62	RWX	WOX_AND	WOX_OR	TCE_Reserved01.
63	RWX	WOX_AND	WOX_OR	FIR_INTERNAL_PARITY_ERROR: FIR Internal Parity Error.

Register Name	ETU FIR MASK Register		
Mnemonic	PE0.PHB0.ETUX16.RSB_PHB03.RSB.REGS.MASK_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D01090B (SCOM) 000000000D01090C (SCOM1) 000000000D01090D (SCOM2)	000000000E01090B (SCOM) 000000000E01090C (SCOM1) 000000000E01090D (SCOM2)	000000000F01090B (SCOM) 000000000F01090C (SCOM1) 000000000F01090D (SCOM2)
Description	ETU FIR MASK Register		

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	AIB_COMMAND_INVALID.
1	RWX	WOX_AND	WOX_OR	AIB_Addressing_Error.
2	RWX	WOX_AND	WOX_OR	AIB_Access_Error.
3	RWX	WOX_AND	WOX_OR	PAPR_Outbound_Injection_Error_Triggered.
4	RWX	WOX_AND	WOX_OR	AIB_Fatal_Class_Error.
5	RWX	WOX_AND	WOX_OR	AIB_INF_Class_Error.
6	RWX	WOX_AND	WOX_OR	PE_Stop_State_Error.
7	RWX	WOX_AND	WOX_OR	AIB_Dat_Err_Signaled.
8	RWX	WOX_AND	WOX_OR	OUT_Common_Array_Fatal_Error.
9	RWX	WOX_AND	WOX_OR	OUT_Common_Latch_Fatal_Error.
10	RWX	WOX_AND	WOX_OR	OUT_Common_Logic_Fatal_Error.
11	RWX	WOX_AND	WOX_OR	BLIF_OUT_Interface_Parity_Error.
12	RWX	WOX_AND	WOX_OR	PCIE_CFG_Write_CA_or_UR_Response.
13	RWX	WOX_AND	WOX_OR	MMIO_Request_Timeout.
14	RWX	WOX_AND	WOX_OR	OUT_RRB_Sourced_Error.
15	RWX	WOX_AND	WOX_OR	CFG_Logic_Signaled_Error.
16	RWX	WOX_AND	WOX_OR	RSB_Reg_Request_Address_Error.
17	RWX	WOX_AND	WOX_OR	RSB_FDA_Fatal_Error.
18	RWX	WOX_AND	WOX_OR	RSB_FDA_INF_Error.
19	RWX	WOX_AND	WOX_OR	RSB_FDB_Fatal_Error.
20	RWX	WOX_AND	WOX_OR	RSB_FDB_INF_Error.
21	RWX	WOX_AND	WOX_OR	RSB_ERR_Fatal_Error.
22	RWX	WOX_AND	WOX_OR	RSB_ERR_INF_Error.
23	RWX	WOX_AND	WOX_OR	RSB_DBG_Fatal_Error.
24	RWX	WOX_AND	WOX_OR	RSB_DBG_INF_Error.
25	RWX	WOX_AND	WOX_OR	RSB_PCIE_Request_Access_Error.
26	RWX	WOX_AND	WOX_OR	RSB_Bus_Logic_Error.
27	RWX	WOX_AND	WOX_OR	RSB_UVI_Fatal_Error.
28	RWX	WOX_AND	WOX_OR	RSB_UVI_INF_Error.
29	RWX	WOX_AND	WOX_OR	SCOM_Fatal_Error.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
30	RWX	WOX_AND	WOX_OR	SCOM_INF_Error.
31	RWX	WOX_AND	WOX_OR	PCIE_Macro_Error_Active_Status.
32	RWX	WOX_AND	WOX_OR	ARB_IODA_Fatal_Error.
33	RWX	WOX_AND	WOX_OR	ARB_MSI_PE_Match_Error.
34	RWX	WOX_AND	WOX_OR	ARB_MSI_Address_Error.
35	RWX	WOX_AND	WOX_OR	ARB_TVT_Error.
36	RWX	WOX_AND	WOX_OR	ARB_Rcvd_Fatal_Error_Msg.
37	RWX	WOX_AND	WOX_OR	ARB_Rcvd_Nonfatal_Error_Msg.
38	RWX	WOX_AND	WOX_OR	ARB_Rcvd_Correctible_Error_Msg.
39	RWX	WOX_AND	WOX_OR	PAPR_Inbound_Injection_Error_Triggered.
40	RWX	WOX_AND	WOX_OR	ARB_Common_Fatal_Error.
41	RWX	WOX_AND	WOX_OR	ARB_Table_BAR_Disabled_Error.
42	RWX	WOX_AND	WOX_OR	ARB_BLIF_Completion_Error.
43	RWX	WOX_AND	WOX_OR	ARB_PCT_Timeout_Error.
44	RWX	WOX_AND	WOX_OR	ARB_ECC_Correctable_Error.
45	RWX	WOX_AND	WOX_OR	ARB_ECC_Uncorrectable_Error.
46	RWX	WOX_AND	WOX_OR	ARB_TLP_Poison_Signaled.
47	RWX	WOX_AND	WOX_OR	ARB_RTT_PENUM_invalid_Error.
48	RWX	WOX_AND	WOX_OR	MRG_Common_Fatal_Error.
49	RWX	WOX_AND	WOX_OR	MRG_Table_BAR_Disabled_Error.
50	RWX	WOX_AND	WOX_OR	MRG_ECC_Correctable_Error.
51	RWX	WOX_AND	WOX_OR	MRG_ECC_Uncorrectable_Error.
52	RWX	WOX_AND	WOX_OR	MRG_AIB2_TX_Timeout_Error.
53	RWX	WOX_AND	WOX_OR	MRG_MRT_Error.
54	RWX	WOX_AND	WOX_OR	MRG_Reserved01.
55	RWX	WOX_AND	WOX_OR	MRG_Reserved02.
56	RWX	WOX_AND	WOX_OR	TCE_IODA_Page_Access_Error.
57	RWX	WOX_AND	WOX_OR	TCE_Request_Timeout_Error.
58	RWX	WOX_AND	WOX_OR	TCE_Unexpected_Response_Error.
59	RWX	WOX_AND	WOX_OR	TCE_COMMON_Fatal_Errors.
60	RWX	WOX_AND	WOX_OR	TCE_ECC_Correctable_Error.
61	RWX	WOX_AND	WOX_OR	TCE_ECC_Uncorrectable_Error.
62	RWX	WOX_AND	WOX_OR	TCE_Reserved01.
63	RWX	WOX_AND	WOX_OR	LEM_FIR_Internal_Parity_Error..

Register Name	ETU FIR ACTION0 Register
Mnemonic	PE0.PHB0.ETUX16.RSB_PHB03.RSB.REGS.ACT0_REG
Address	PCI0 (PE0): 000000000D01090E (SCOM) PCI1 (PE1): 000000000E01090E (SCOM) PCI2 (PE2): 000000000F01090E (SCOM)
Description	ETU FIR ACTION0 Register

Bits	SCOM	Field Mnemonic: Description
0	RWX	AIB_Command_Invalid.
1	RWX	AIB_Addressing_Error.
2	RWX	AIB_Access_Error.
3	RWX	PAPR_Outbound_Injection_Error_Triggered.
4	RWX	AIB_Fatal_Class_Error.
5	RWX	AIB_INF Class_Error.
6	RWX	PE_Stop_State_Error.
7	RWX	AIB_Dat_Err_Signaled.
8	RWX	OUT_Common_Array_Fatal_Error.
9	RWX	OUT_Common_Latch_Fatal_Error.
10	RWX	OUT_Common_Logic_Fatal_Error.
11	RWX	BLIF_OUT_Interface_Parity_Error.
12	RWX	PCIe_CFG_Write_CA_or_UR_Response.
13	RWX	MMIO_Request_Timeout.
14	RWX	OUT_RRB_Sourced_Error.
15	RWX	CFG_Logic_Signaled_Error.
16	RWX	RSB_Reg_Request_Address_Error.
17	RWX	RSB_FDA_Fatal_Error.
18	RWX	RSB_FDA_INF_Error.
19	RWX	RSB_FDB_Fatal_Error.
20	RWX	RSB_FDB_INF_Error.
21	RWX	RSB_ERR_Fatal_Error.
22	RWX	RSB_ERR_INF_Error.
23	RWX	RSB_DBG_Fatal_Error.
24	RWX	RSB_DBG_INF_Error.
25	RWX	RSB_PCIE_Request_Access_Error.
26	RWX	RSB_Bus_Logic_Error.
27	RWX	RSB_UVI_Fatal_Error.
28	RWX	RSB_UVI_INF_Error.
29	RWX	SCOM_Fatal_Error.
30	RWX	SCOM_INF_Error.
31	RWX	PCIE Macro_Error_Active_Status.

Bits	SCOM	Field Mnemonic: Description
32	RWX	ARB_IODA_Fatal_Error.
33	RWX	ARB_MSI_PE_Match_Error.
34	RWX	ARB_MSI_Address_Error.
35	RWX	ARB_TVT_Error.
36	RWX	ARB_Rcvd_Fatal_Error_Msg .
37	RWX	ARB_Rcvd_Nonfatal_Error_ Msg .
38	RWX	ARB_Rcvd_Correctible_Error_ Msg.
39	RWX	PAPR_Inbound_Injection_Error_Triggered.
40	RWX	ARB_Common_Fatal_Error.
41	RWX	ARB_Table_BAR_Disabled_Error.
42	RWX	ARB_BLIF_Completion_Error.
43	RWX	ARB_PCT_Timeout_Error.
44	RWX	ARB_ECC_Correctable_Error.
45	RWX	ARB_ECC_Uncorrectable_Error.
46	RWX	ARB_TLP_Poison_Signaled.
47	RWX	ARB_RTT_PENUM_Invalid_Error.
48	RWX	MRG_Common_Fatal_Error.
49	RWX	MRG_Table_BAR_Disabled_Error.
50	RWX	MRG_ECC_Correctable_Error.
51	RWX	MRG_ECC_Uncorrectable_Error.
52	RWX	MRG_AIB2_TX_Timeout_Error.
53	RWX	MRG_MRT_Error.
54	RWX	MRG_Reserved01.
55	RWX	MRG_Reserved02.
56	RWX	TCE_IODA_Page_Access_Error.
57	RWX	TCE_Request_Timeout_Error.
58	RWX	TCE_Unexpected_Response_Error.
59	RWX	TCE_Common_Fatal_Errors.
60	RWX	TCE_ECC_Correctable_Error.
61	RWX	TCE_ECC_Uncorrectable_Error.
62	RWX	TCE_Reserved01.
63	RWX	LEM_FIR_Internal_Parity_Error.

Register Name	ETU FIR ACTION1 Register
Mnemonic	PE0.PHB0.ETUX16.RSB_PHB03.RSB.REGS.ACTION1_REG
Address	
Description	ETU FIR ACTION1 Register

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D01090F (SCOM)	000000000E01090F (SCOM)	000000000F01090F (SCOM)

Bits	SCOM	Field Mnemonic: Description
0	RWX	AIB_Command_Invalid.
1	RWX	AIB_Addressing_Error.
2	RWX	AIB_Access_Error.
3	RWX	PAPR_Outbound_Injection_Error_Triggered.
4	RWX	AIB_Fatal_Class_Error.
5	RWX	AIB_INF_Class_Error.
6	RWX	PE_Stop_State_Error.
7	RWX	AIB_Dat_Err_Signaled.
8	RWX	OUT_Common_Array_Fatal_Error.
9	RWX	OUT_Common_Latch_Fatal_Error.
10	RWX	OUT_Common_Logic_Fatal_Error.
11	RWX	BLIF_OUT_Interface_Parity_Error.
12	RWX	PCIE_CFG_Write_CA_or_UR_Response.
13	RWX	MMIO_Request_Timeout.
14	RWX	OUT_RRB_Sourced_Error.
15	RWX	CFG_Logic_Signaled_Error.
16	RWX	RSB_Reg_Request_Address_Error.
17	RWX	RSB_FDA_Fatal_Error.
18	RWX	RSB_FDA_INF_Error.
19	RWX	RSB_FDB_Fatal_Error.
20	RWX	RSB_FDB_INF_Error.
21	RWX	RSB_ERR_Fatal_Error.
22	RWX	RSB_ERR_INF_Error.
23	RWX	RSB_DBG_Fatal_Error.
24	RWX	RSB_DBG_INF_Error.
25	RWX	RSB_PCIE_Request_Access_Error.
26	RWX	RSB_Bus_Logic_Error.
27	RWX	RSB_UVI_Fatal_Error.
28	RWX	RSB_UVI_INF_Error.
29	RWX	SCOM_Fatal_Error.
30	RWX	SCOM_INF_Error.
31	RWX	PCIE_Macro_Error_Active_Status.

Bits	SCOM	Field Mnemonic: Description
32	RWX	ARB_IODA_Fatal_Error.
33	RWX	ARB_MSI_PE_Match_Error.
34	RWX	ARB_MSI_Address_Error.
35	RWX	ARB_TVT_Error.
36	RWX	ARB_Rcvd_Fatal_Error_Msg.
37	RWX	ARB_Rcvd_Nonfatal_Error Msg.
38	RWX	ARB_Rcvd_Correctible_Error_Msg.
39	RWX	PAPR_Inbound_Injection_Error_Triggered.
40	RWX	ARB_Common_Fatal_Error.
41	RWX	ARB_Table_BAR_Disabled_Error.
42	RWX	ARB_BLIF_Completion_Error.
43	RWX	ARB_PCT_Timeout_Error.
44	RWX	ARB_ECC_Correctable_Error.
45	RWX	ARB_ECC_Uncorrectable_Error.
46	RWX	ARB_TLP_Poison_Signaled.
47	RWX	ARB_RTT_PENUM_Invalid_Error.
48	RWX	MRG_Common_Fatal_Error.
49	RWX	MRG_Table_BAR_Disabled_Error.
50	RWX	MRG_ECC_Correctable_Error.
51	RWX	MRG_ECC_Uncorrectable_Error.
52	RWX	MRG_AIB2_TX_Timeout_Error.
53	RWX	MRG_MRT_Error.
54	RWX	MRG_Reserved01.
55	RWX	MRG_Reserved02.
56	RWX	TCE_IODA_Page_Access_Error.
57	RWX	TCE_Request_Timeout_Error.
58	RWX	TCE_Unexpected_Response_Error.
59	RWX	TCE_Common_Fatal_Errors.
60	RWX	TCE_ECC_Correctable_Error.
61	RWX	TCE_ECC_Uncorrectable_Error.
62	RWX	TCE_Reserved01.
63	RWX	LEM_FIR_Internal_Parity_Error.

Register Name	ETU FIR WOF Register
Mnemonic	PE0.PHB0.ETUX16.RSB_PHB03.RSB.REGS.WOF_REG
Address	
Description	ETU FIR WOF Register

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D010910 (SCOM)	000000000E010910 (SCOM)	000000000F010910 (SCOM)

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	AIB_Command_Invalid.
1	RWX_WCLRREG	AIB_Addressing_Error.
2	RWX_WCLRREG	AIB_Access_Error.
3	RWX_WCLRREG	PAPR_Outbound_Injection_Error_Triggered.
4	RWX_WCLRREG	AIB_Fatal_Class_Error.
5	RWX_WCLRREG	AIB_INF_Class_Error.
6	RWX_WCLRREG	PE_Stop_State_Error.
7	RWX_WCLRREG	AIB_Dat_Err_Signaled.
8	RWX_WCLRREG	OUT_Common_Array_Fatal_Error.
9	RWX_WCLRREG	OUT_Common_Latch_Fatal_Error.
10	RWX_WCLRREG	OUT_Common_Logic_Fatal_Error.
11	RWX_WCLRREG	BLIF_OUT_Interface_Parity_Error.
12	RWX_WCLRREG	PCIE_CFG_Write_CA_or_UR_Response.
13	RWX_WCLRREG	MMIO_Request_Timeout.
14	RWX_WCLRREG	OUT_RRB_Sourced_Error.
15	RWX_WCLRREG	CFG_Logic_Signaled_Error.
16	RWX_WCLRREG	RSB_Reg_Request_Address_Error.
17	RWX_WCLRREG	RSB_FDA_Fatal_Error.
18	RWX_WCLRREG	RSB_FDA_INF_Error.
19	RWX_WCLRREG	RSB_FDB_Fatal_Error.
20	RWX_WCLRREG	RSB_FDB_INF_Error.
21	RWX_WCLRREG	RSB_ERR_Fatal_Error.
22	RWX_WCLRREG	RSB_ERR_INF_Error.
23	RWX_WCLRREG	RSB_DBG_Fatal_Error.
24	RWX_WCLRREG	RSB_DBG_INF_Error.
25	RWX_WCLRREG	RSB_PCIE_Request_Access_Error.
26	RWX_WCLRREG	RSB_Bus_Logic_Error.
27	RWX_WCLRREG	RSB_UVI_Fatal_Error.
28	RWX_WCLRREG	RSB_UVI_INF_Error.
29	RWX_WCLRREG	SCOM_Fatal_Error.
30	RWX_WCLRREG	SCOM_INF_Error.
31	RWX_WCLRREG	PCIE_Macro_Error_Active_Status.

Bits	SCOM	Field Mnemonic: Description
32	RWX_WCLRREG	ARB_IODA_Fatal_Error.
33	RWX_WCLRREG	ARB_MSI_PE_Match_Error.
34	RWX_WCLRREG	ARB_MSI_Address_Error.
35	RWX_WCLRREG	ARB_TVT_Error.
36	RWX_WCLRREG	ARB_Rcvd_Fatal_Error_Msg.
37	RWX_WCLRREG	ARB_Rcvd_Nonfatal_Error_Msg.
38	RWX_WCLRREG	ARB_Rcvd_Correctible_Error_Msg.
39	RWX_WCLRREG	PAPR_Inbound_Injection_Error_Triggered.
40	RWX_WCLRREG	ARB_Common_Fatal_Error.
41	RWX_WCLRREG	ARB_Table_BAR_Disabled_Error.
42	RWX_WCLRREG	ARB_BLIF_Completion_Error.
43	RWX_WCLRREG	ARB_PCT_Timeout_Error.
44	RWX_WCLRREG	ARB_ECC_Correctable_Error.
45	RWX_WCLRREG	ARB_ECC_Uncorrectable_Error.
46	RWX_WCLRREG	ARB_TLP_Poison_Signaled.
47	RWX_WCLRREG	ARB_RTT_PENUM_Invalid_Error.
48	RWX_WCLRREG	MRG_Common_Fatal_Error.
49	RWX_WCLRREG	MRG_Table_BAR_Disabled_Error.
50	RWX_WCLRREG	MRG_ECC_Correctable_Error.
51	RWX_WCLRREG	MRG_ECC_Uncorrectable_Error.
52	RWX_WCLRREG	MRG_AIB2_TX_Timeout_Error.
53	RWX_WCLRREG	MRG_MRT_Error.
54	RWX_WCLRREG	MRG_Reserved01.
55	RWX_WCLRREG	MRG_Reserved02.
56	RWX_WCLRREG	TCE_IODA_Page_Access_Error.
57	RWX_WCLRREG	TCE_Request_Timeout_Error.
58	RWX_WCLRREG	TCE_Unexpected_Response_Error.
59	RWX_WCLRREG	TCE_COMMON_Fatal_Errors.
60	RWX_WCLRREG	TCE_ECC_Correctable_Error.
61	RWX_WCLRREG	TCE_ECC_UnCorrectable_Error.
62	RWX_WCLRREG	TCE_Reserved01.
63	RWX_WCLRREG	LEM_FIR_Internal_Parity_Error.

Register Name	FIR Status Register
Mnemonic	IOP0.IOP_X844.IOP_SCOM.FIR_STATUS_REG
Address	
Description	Fault Isolation Status Register: Address = 00h: RW, Address = 01h: Clear, Address = 02h: Set

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D010C00 (SCOM) 000000000D010C01 (SCOM1) 000000000D010C02 (SCOM2)	000000000E010C00 (SCOM) 000000000E010C01 (SCOM1) 000000000E010C02 (SCOM2)	000000000F010C00 (SCOM) 000000000F010C01 (SCOM1) 000000000F010C02 (SCOM2)

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_STATUS_REG_HSSCALERR_STATUS: FIR Status Register: HSS ZCAL calibration error.
1	RWX	WOX_AND	WOX_OR	FIR_STATUS_REG_HSSPLLAERR_STATUS: FIR Status Register: HSS PLL A calibration error.
2	RWX	WOX_AND	WOX_OR	FIR_STATUS_REG_HSSPLLBERR_STATUS: FIR Status Register: HSS PLL B calibration error.
3	RWX	WOX_AND	WOX_OR	FIR_STATUS_REG_TXAERR_STATUS: FIR Status Register: TX Lane A calibration error.
4	RWX	WOX_AND	WOX_OR	FIR_STATUS_REG_TXBERR_STATUS: FIR Status Register: TX Lane B calibration error.
5	RWX	WOX_AND	WOX_OR	FIR_STATUS_REG_TXCERR_STATUS: FIR Status Register: TX Lane C calibration error.
6	RWX	WOX_AND	WOX_OR	FIR_STATUS_REG_TXDERR_STATUS: FIR Status Register: TX Lane D calibration error.
7	RWX	WOX_AND	WOX_OR	FIR_STATUS_REG_TXEERR_STATUS: FIR Status Register: TX Lane E calibration error.
8	RWX	WOX_AND	WOX_OR	FIR_STATUS_REG_TXFERR_STATUS: FIR Status Register: TX Lane F calibration error.
9	RWX	WOX_AND	WOX_OR	FIR_STATUS_REG_TXGERR_STATUS: FIR Status Register: TX Lane G calibration error.
10	RWX	WOX_AND	WOX_OR	FIR_STATUS_REG_TXHERR_STATUS: FIR Status Register: TX Lane H calibration error.
11	RWX	WOX_AND	WOX_OR	FIR_STATUS_REG_TXIERR_STATUS: FIR Status Register: TX Lane I calibration error.
12	RWX	WOX_AND	WOX_OR	FIR_STATUS_REG_TXJERR_STATUS: FIR Status Register: TX Lane J calibration error.
13	RWX	WOX_AND	WOX_OR	FIR_STATUS_REG_TXKERR_STATUS: FIR Status Register: TX Lane K calibration error.
14	RWX	WOX_AND	WOX_OR	FIR_STATUS_REG_TXLERR_STATUS: FIR Status Register: TX Lane L calibration error.
15	RWX	WOX_AND	WOX_OR	FIR_STATUS_REG_TXMERR_STATUS: FIR Status Register: TX Lane M calibration error.
16	RWX	WOX_AND	WOX_OR	FIR_STATUS_REG_TXNERR_STATUS: FIR Status Register: TX Lane N calibration error.
17	RWX	WOX_AND	WOX_OR	FIR_STATUS_REG_TXOERR_STATUS: FIR Status Register: TX Lane O calibration error.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
18	RWX	WOX_AND	WOX_OR	FIR_STATUS_REG_TXPERR_STATUS: FIR Status Register: TX Lane P calibration error.
19	RWX	WOX_AND	WOX_OR	FIR_STATUS_REG_RXAERR_STATUS: FIR Status Register: RX Lane A calibration error.
20	RWX	WOX_AND	WOX_OR	FIR_STATUS_REG_RXBERR_STATUS: FIR Status Register: RX Lane B calibration error.
21	RWX	WOX_AND	WOX_OR	FIR_STATUS_REG_RXCERR_STATUS: FIR Status Register: RX Lane C calibration error.
22	RWX	WOX_AND	WOX_OR	FIR_STATUS_REG_RXDERR_STATUS: FIR Status Register: RX Lane D calibration error.
23	RWX	WOX_AND	WOX_OR	FIR_STATUS_REG_RXEERR_STATUS: FIR Status Register: RX Lane E calibration error.
24	RWX	WOX_AND	WOX_OR	FIR_STATUS_REG_RXFERR_STATUS: FIR Status Register: RX Lane F calibration error.
25	RWX	WOX_AND	WOX_OR	FIR_STATUS_REG_RXGERR_STATUS: FIR Status Register: RX Lane G calibration error.
26	RWX	WOX_AND	WOX_OR	FIR_STATUS_REG_RXHERR_STATUS: FIR Status Register: RX Lane H calibration error.
27	RWX	WOX_AND	WOX_OR	FIR_STATUS_REG_RXIERR_STATUS: FIR Status Register: RX Lane I calibration error.
28	RWX	WOX_AND	WOX_OR	FIR_STATUS_REG_RXJERR_STATUS: FIR Status Register: RX Lane J calibration error.
29	RWX	WOX_AND	WOX_OR	FIR_STATUS_REG_RXKERR_STATUS: FIR Status Register: RX Lane K calibration error.
30	RWX	WOX_AND	WOX_OR	FIR_STATUS_REG_RXLERR_STATUS: FIR Status Register: RX Lane L calibration error.
31	RWX	WOX_AND	WOX_OR	FIR_STATUS_REG_RXMERR_STATUS: FIR Status Register: RX Lane M calibration error.
32	RWX	WOX_AND	WOX_OR	FIR_STATUS_REG_RXNERR_STATUS: FIR Status Register: RX Lane N calibration error.
33	RWX	WOX_AND	WOX_OR	FIR_STATUS_REG_RXOERR_STATUS: FIR Status Register: RX Lane O calibration error.
34	RWX	WOX_AND	WOX_OR	FIR_STATUS_REG_RXPERR_STATUS: FIR Status Register: RX Lane P calibration error.
35	RWX	WOX_AND	WOX_OR	FIR_STATUS_REG_SCOM_FIR_PERR0_STATUS: FIR Status Register: SCOM FIR parity error 0.
36	RWX	WOX_AND	WOX_OR	FIR_STATUS_REG_SCOM_FIR_PERR1_STATUS: FIR Status Register: SCOM FIR parity error 1.
37:63	RO	RO	RO	Constant = 0b000000000000000000000000000

Register Name	FIR Mask Register		
Mnemonic	IOP0.IOP_X844.IOP_SCOM.FIR_MASK_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D010C03 (SCOM) 000000000D010C04 (SCOM1) 000000000D010C05 (SCOM2)	000000000E010C03 (SCOM) 000000000E010C04 (SCOM1) 000000000E010C05 (SCOM2)	000000000F010C03 (SCOM) 000000000F010C04 (SCOM1) 000000000F010C05 (SCOM2)
Description	Fault Isolation Mask Register: Address = 03h: RW, Address = 04h: Clear, Address = 05h: Set		

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_MASK_REG_HSSCALERR_MASK: FIR Mask Register: HSS ZCAL calibration error mask.
1	RWX	WOX_AND	WOX_OR	FIR_MASK_REG_HSSPLLAERR_MASK: FIR Mask Register: HSS PLL A calibration error mask.
2	RWX	WOX_AND	WOX_OR	FIR_MASK_REG_HSSPLLBERR_MASK: FIR Mask Register: HSS PLL B calibration error mask.
3	RWX	WOX_AND	WOX_OR	FIR_MASK_REG_TXAERR_MASK: FIR Mask Register: TX Lane A calibration error mask.
4	RWX	WOX_AND	WOX_OR	FIR_MASK_REG_TXBERR_MASK: FIR Mask Register: TX Lane B calibration error mask.
5	RWX	WOX_AND	WOX_OR	FIR_MASK_REG_TXCERR_MASK: FIR Mask Register: TX Lane C calibration error mask.
6	RWX	WOX_AND	WOX_OR	FIR_MASK_REG_TXDERR_MASK: FIR Mask Register: TX Lane D calibration error mask.
7	RWX	WOX_AND	WOX_OR	FIR_MASK_REG_TXEERR_MASK: FIR Mask Register: TX Lane E calibration error mask.
8	RWX	WOX_AND	WOX_OR	FIR_MASK_REG_TXFERR_MASK: FIR Mask Register: TX Lane F calibration error mask.
9	RWX	WOX_AND	WOX_OR	FIR_MASK_REG_TXGERR_MASK: FIR Mask Register: TX Lane G calibration error mask.
10	RWX	WOX_AND	WOX_OR	FIR_MASK_REG_TXHERR_MASK: FIR Mask Register: TX Lane H calibration error mask.
11	RWX	WOX_AND	WOX_OR	FIR_MASK_REG_TXIERR_MASK: FIR Mask Register: TX Lane I calibration error mask.
12	RWX	WOX_AND	WOX_OR	FIR_MASK_REG_TXJERR_MASK: FIR Mask Register: TX Lane J calibration error mask.
13	RWX	WOX_AND	WOX_OR	FIR_MASK_REG_TXKERR_MASK: FIR Mask Register: TX Lane K calibration error mask.
14	RWX	WOX_AND	WOX_OR	FIR_MASK_REG_TXLERR_MASK: FIR Mask Register: TX Lane L calibration error mask.
15	RWX	WOX_AND	WOX_OR	FIR_MASK_REG_TXMERR_MASK: FIR Mask Register: TX Lane M calibration error mask.
16	RWX	WOX_AND	WOX_OR	FIR_MASK_REG_TXNERR_MASK: FIR Mask Register: TX Lane N calibration error mask.
17	RWX	WOX_AND	WOX_OR	FIR_MASK_REG_TXOERR_MASK: FIR Mask Register: TX Lane O calibration error mask.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
18	RWX	WOX_AND	WOX_OR	FIR_MASK_REG_TXPERR_MASK: FIR Mask Register: TX Lane P calibration error mask.
19	RWX	WOX_AND	WOX_OR	FIR_MASK_REG_RXAERR_MASK: FIR Mask Register: RX Lane A calibration error mask.
20	RWX	WOX_AND	WOX_OR	FIR_MASK_REG_RXBERR_MASK: FIR Mask Register: RX Lane B calibration error mask.
21	RWX	WOX_AND	WOX_OR	FIR_MASK_REG_RXCERR_MASK: FIR Mask Register: RX Lane C calibration error mask.
22	RWX	WOX_AND	WOX_OR	FIR_MASK_REG_RXDERR_MASK: FIR Mask Register: RX Lane D calibration error mask.
23	RWX	WOX_AND	WOX_OR	FIR_MASK_REG_RXEERR_MASK: FIR Mask Register: RX Lane E calibration error mask.
24	RWX	WOX_AND	WOX_OR	FIR_MASK_REG_RXFERR_MASK: FIR Mask Register: RX Lane F calibration error mask.
25	RWX	WOX_AND	WOX_OR	FIR_MASK_REG_RXGERR_MASK: FIR Mask Register: RX Lane G calibration error mask.
26	RWX	WOX_AND	WOX_OR	FIR_MASK_REG_RXHERR_MASK: FIR Mask Register: RX Lane H calibration error mask.
27	RWX	WOX_AND	WOX_OR	FIR_MASK_REG_RXIERR_MASK: FIR Mask Register: RX Lane I calibration error mask.
28	RWX	WOX_AND	WOX_OR	FIR_MASK_REG_RXJERR_MASK: FIR Mask Register: RX Lane J calibration error mask.
29	RWX	WOX_AND	WOX_OR	FIR_MASK_REG_RXKERR_MASK: FIR Mask Register: RX Lane K calibration error mask.
30	RWX	WOX_AND	WOX_OR	FIR_MASK_REG_RXLERR_MASK: FIR Mask Register: RX Lane L calibration error mask.
31	RWX	WOX_AND	WOX_OR	FIR_MASK_REG_RXMERR_MASK: FIR Mask Register: RX Lane M calibration error mask.
32	RWX	WOX_AND	WOX_OR	FIR_MASK_REG_RXNERR_MASK: FIR Mask Register: RX Lane N calibration error mask.
33	RWX	WOX_AND	WOX_OR	FIR_MASK_REG_RXOERR_MASK: FIR Mask Register: RX Lane O calibration error mask.
34	RWX	WOX_AND	WOX_OR	FIR_MASK_REG_RXPERR_MASK: FIR Mask Register: RX Lane P calibration error mask.
35	RWX	WOX_AND	WOX_OR	FIR_MASK_REG_SCOM_FIR_PERR0_MASK: FIR Mask Register: SCOM FIR parity 0 error mask.
36	RWX	WOX_AND	WOX_OR	FIR_MASK_REG_SCOM_FIR_PERR1_MASK: FIR Mask Register: SCOM FIR parity 1 error mask.
37:63	RO	RO	RO	Constant = 0b000000000000000000000000000

Register Name	FIR Action 0 Register		
Mnemonic	IOP0.IOP_X844.IOP_SCOM.FIR_ACTION0_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D010C06 (SCOM)	000000000E010C06 (SCOM)	000000000F010C06 (SCOM)
Description	Action 0 select for the FIR bits.		

Bits	SCOM	Field Mnemonic: Description
0:36	RO	FIR_ACTION0_REG_ACTION0: Fault Isolation Action 0 Register. MSB of the action select for the corresponding bit in the FIR. (Action0, Action1, Mask) = Action Select. (0,0,x) = Checkstop error. (0,1,0) = Recoverable error. (1,0,0) = Recoverable interrupt. (1,1,0) = Machine check. (x,x,1) = Masked.
37:63	RO	Constant = 0b000000000000000000000000000

Register Name	FIR Action 1 Register		
Mnemonic	IOP0.IOP_X844.IOP_SCOM.FIR_ACTION1_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D010C07 (SCOM)	000000000E010C07 (SCOM)	000000000F010C07 (SCOM)
Description	Action 1 Select for the FIR bits.		

Bits	SCOM	Field Mnemonic: Description
0:36	RO	FIR_ACTION1_REG_ACTION1: Fault Isolation Action 1 Register. MSB of the action select for the corresponding bit in the FIR. (Action0, Action1, Mask) = Action Select. (0,0,x) = Checkstop error. (0,1,0) = Recoverable error. (1,0,0) = Recoverable interrupt. (1,1,0) = Machine check. (x,x,1) = Masked.
37:63	RO	Constant = 0b000000000000000000000000000

Register Name	FIR WOF Register		
Mnemonic	IOP0.IOP_X844.IOP_SCOM.FIR_WOF_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D010C08 (SCOM)	000000000E010C08 (SCOM)	000000000F010C08 (SCOM)
Description	The Who is on first register indicates which error occurred first		

Bits	SCOM	Field Mnemonic: Description
0:36	RWX_WCLRREG	FIR_WOF_REG_WOF: The WOF Register locks on the first error.
37:63	RO	Constant = 0b000000000000000000000000000

Register Name	Configuration of CC Counters Register		
Mnemonic	TP.TCPCI0.PCI0.SYNC_CONFIG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D030000 (SCOM)	000000000E030000 (SCOM)	000000000F030000 (SCOM)
Description	Configuration of CC counters		

Bits	SCOM	Field Mnemonic: Description
0:3	RW	SYNC_PULSE_DELAY: Delay the incoming sync pulse. The default is 8 latches including asynchronous. 0000 = 8 0001 = 2 0010 = 3 0011 = 4 0100 = 5 0101 = 6 0110 = 7 0111 = 8 cycles 1000 = 9 1001 = 10 1010 = 11 1011 = 12 1100 = 13 1101 = 14 1110 = 15 1111 = 16 delay of the reset of the phase counter.
4	RW	LISTEN_TO_SYNC_PULSE_DIS: Disable phase counter synchronization by the sync_pulse signal. (The default is enabled.) Attention: When you enable listen_to_sync, the chiplet gets corrupted for 200 cycles.
5	RW	SYNC_PULSE_INPUT_SEL: The default is 0. When set to 1, the alternative input of the sync_pulse is used. Attention: When you toggle the input select, the chiplet gets corrupted for 200 cycles.
6	RW	USE_SYNC_FOR_SCAN: If set, use OPCG initial alignment for scan requests.
7	RW	CLEAR_CHIPLET_IS_ALIGNED: This bit clears the chiplet_is_aligned bit. See the cplt_stat register.
8	RW	UNIT_REGION_CLKCMD_ENABLE: Enable the unit interface to start or stop one dedicate region. Used for the POWER9 cache or core.
9	RW	DISABLE_PCB_ITR: Disable interrupt generation within the CC. An interrupt is sent on each HLD event.
10	RW	ENABLE_VITL_ALIGN_CHECK: Enable the VITL align check to compare alignment of an incoming sync pulse with 2:1 VITL LCB.
11	RW	SYNC_PULSE_OUT_DIS: Disable sync_pulse output. When set to 1, the master chiplet does not send sync pulses to slave chiplets anymore.
12:19	RW	UNUSED1219: Unused.

Register Name	OPCG Alignment Register		
Mnemonic	TP.TCPCI0.PCI0.OPCG_ALIGN		
Address	PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
	000000000D030001 (SCOM)	000000000E030001 (SCOM)	000000000F030001 (SCOM)
Description	OPCG ALIGN		

Bits	SCOM	Field Mnemonic: Description
0:3	RW	INOP_ALIGN: INOP phase alignment (0: none, 1: 2:1, 2: 3:1, 3: 4:1, 4: 6:1, 5: 8:1, 6: 12:1, 7: 16:1, 8: 24:1, 9-15: 48:1).
4:7	RW	SNOP_ALIGN: SNOP phase alignment (0: none, 1: 2:1, 2: 3:1, 3: 4:1, 4: 6:1, 5: 8:1, 6: 12:1, 7: 16:1, 8: 24:1, 9-15: 48:1).
8:11	RW	ENOP_ALIGN: ENOP phase alignment (0: none, 1: 2:1, 2: 3:1, 3: 4:1, 4: 6:1, 5: 8:1, 6: 12:1, 7: 16:1, 8: 24:1, 9-15: 48:1).
12:19	RW	INOP_WAIT: INOP cycle delay (0 - 255).
20:31	RW	SNOP_WAIT: SNOP cycle delay (0 - 4095).
32:39	RW	ENOP_WAIT: ENOP cycle delay (0 - 255).
40	RW	INOP_FORCE_SG: INOP: Set SG high during INOP.
41	RW	SNOP_FORCE_SG: SNOP: Set SG high during SNOP.
42	RW	ENOP_FORCE_SG: ENOP: Set SG high during ENOP (including LOOP phase).
43	RW	NO_WAIT_ON_CLK_CMD: 0 = A clock change request first waits the OPCG_WAIT cycles. 1 = A clock change request does not wait when not in flush.
44:45	RW	ALIGN_SOURCE_SELECT: 0: Use the inopa setting from opcg_reg0. 1: Use the rising edge of the sync pulse. 2: Use unit0_sync_lvl to align (for AVP - refresh0). 3: Use unit1_sync_lvl to align (for AVP - refresh1).
46	RW	UNUSED46: Unused.
47:51	RW	SCAN_RATIO: scan_ratio (n = 0 - 15: (n+1):1, 16: 24:1, 17: 32:1, 18: 48:1, 19: 64:1, 20: 128:1). The default is 4:1 = 00011.
52:63	RW	OPCG_WAIT_CYCLES: Old PAD value. Delay at the beginning and end of the OPCG run to enable DC signals to be there at the correct time (0 = 4095). Must be higher than the pipeline-latch depth. The default is 0x020.

Register Name	OPCG Control Register 0		
Mnemonic	TP.TCPCI0.PCI0.OPCG_REG0		
Address	PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
	000000000D030002 (SCOM)	000000000E030002 (SCOM)	000000000F030002 (SCOM)
Description	OPCG Control Register 0		

Bits	SCOM	Field Mnemonic: Description
0	RW	RUNN_MODE: 0 = BIST mode used for LBIST. 1 = Run-N mode used for ABIST/IOBIST.
1	RWX	OPCG_GO: OPCG go (start OPCG). This bit is cleared when the OPCG is done. Poll for opcg_done in the cplt_start register
2	RWX	RUN_SCAN0: Run scan0 (overrides all BIST mode settings but the scan_ratio). Starts a scan0 run. The bit gets cleared when OPCG is done. Poll for opcg_done in the cplt_start register.
3	RW	SCAN0_MODE: Set PRPGs in scan0_mode but do not run the automatic scan0 sequence.
4	RWX	OPCG_IN_SLAVE_MODE: When selected, the OPCG waits for the master chiplet to get started. When Keep_MS_Mode is 0, SLAVE_MODE is cleared after the incoming trigger.
5	RWX	OPCG_IN_MASTER_MODE: When selected, the OPCG sends out a trigger to all slave chiplets. When Keep_MS_MODE = 0, MASTER_MODE is cleared after sending out one master trigger.
6	RW	KEEP_MS_MODE: When set to 1, the OPCG in M/S mode bits are not cleared after one incoming OPCG trigger. The default is clear the M/S mode bits.
7	RW	TRIGGER_OPCG_ON_UNIT0_SYNC_LVL: The unit pin used for AVP can trigger OPCG (unit0_sync_lvl).
8	RW	TRIGGER_OPCG_ON_UNIT1_SYNC_LVL: The unit pin used for AVP can trigger OPCG (unit1_sync_lvl).
9	RWX	RUN_CHIPLET_SCAN0: Run scan0 on all regions and types. The clears the chiplet.
10	RWX	RUN_CHIPLET_SCAN0_NO_PLL: Run scan0 on all regions and types. This clears the chiplet excluding the PLL region. The PLL can keep running.
11	RW	RUN_OPCG_ON_UPDATE_DR: Start the OPCG engine when scan updated (update_dr) is received (set pulse). Cronus requires this bit = 1 for a setpulse WRITE.
12	RW	RUN_OPCG_ON_CAPTURE_DR: Start the OPCG engine when scan updated (capture_dr) is received (set pulse). Cronus requires this bit = 1 for a setpulse READ.
13	RW	STOP_RUNN_ON_XSTOP: Run-N mode: Stop run-n on a checkstop.
14	RW	OPCG_STARTS_BIST: Run-N mode: The OPCG engine controls start_bist for ABIST or IOBIST (see BIST register).
15:20	RW	UNUSED1520: Unused.
21:63	RWX	LOOP_COUNT: Loop counter for LBIST and RUN-N. Write: Target value. Read: Current counter value. Counts from 0 to the target value.

Register Name	OPCG Control Register 1
Mnemonic	TP.TCPCI0.PCI0.OPCG_REG1
Address	
Description	OPCG Control Register 1

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D030003 (SCOM)	000000000E030003 (SCOM)	000000000F030003 (SCOM)

Bits	SCOM	Field Mnemonic: Description
0:11	RW	SCAN_COUNT: BIST mode: Channel scan count (s = 0 - 4095) Run-N mode: The start_bist match value (0:11).

Bits	SCOM	Field Mnemonic: Description
12:23	RW	MISR_A_VAL: BIST mode: The a value for the MISR aperture. Run-N mode: The start_bist match value (12:23).
24:35	RW	MISR_B_VAL: BIST mode: The b value for the MISR aperture. Run-N mode: The start_bist match value (24:35).
36:47	RW	MISR_INIT_WAIT: BIST mode: Delay MISR aperture. MISRs get active after this number of loops.
48	RW	OPCG_SUPPRESS_LAST_RUNN_CLK: OPCG suppresses the last RUNN clock. Normal slow mesh sees N cycles instead of N+1. Fast mesh sees 2 ´ (N +1) -1 cycles.
49	RW	SCAN_CLK_USE_EVEN: Generate a scan clock in an even cycle instead of an odd. The default is 0 = odd for scan.
50:51	RW	UNUSED2: Unused.
52	RW	RTIM_THOLD_FORCE: Force rtim_thold low when not in test_dc mode (must be 0 at all time).
53	RW	DISABLE_ARY_CLK_DURING_FILL: LBIST and SCAN0: Prevent the fire of ARY HLD during an NSL fill.
54	RW	SG_HIGH_DURING_FILL: LBIST and SCAN0: Hold SG high during an NSL fill.
55:56	RW	LBIST_SKITTER_CTL: BIST mode: 00 = Enable skitter during lbist_ip. 01 = Enable skitter when misr_active. See misr_init_wait. 10 = Skitter OPCG_GO mode. The falling edge equals start; the rising edge equals stop. 11 = Unused.
57	RW	MISR_MODE: BIST mode: MISR aperture mode 0 = a-1 to b-1. 1 = Start to a and b to end.
58	RW	INFINITE_MODE: Infinite mode. RUN-N and LBIST run forever and ignore the loop count.
59:63	RW	NSL_FILL_COUNT: BIST mode: NSL-fill count (0 - 31).

Register Name	**OPCG Control Register 2**
Mnemonic	TP.TCPCI0.PCI0.OPCG_REG2
Address	
Description	OPCG Control Register 2

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D030004 (SCOM)	000000000E030004 (SCOM)	000000000F030004 (SCOM)

Bits	SCOM	Field Mnemonic: Description
0	RWX	OPCG_GO2: OPCG go for broadcast sequences (start sequence).
1:3	RW	PRPG_WEIGHTING: prpg_activate: 1/2, 1/4, 1/8, 1/16, 1/2, 3/4, 7/8, 15/16.
4:15	RWX	PRPG_VALUE: Set to 0 for PRPG always on; else seed.
16:27	RW	PRPG_A_VAL: The a value for the PRPG aperture.
28:39	RW	PRPG_B_VAL: The b value for the PRPG aperture.
40	RW	PRPG_MODE: PRPG aperture mode: 0 = a-1 to b-1. 1 = Start to a and b to end.
41:63	RW	UNUSED41_63: Unused.

Register Name	Scan Region and Type Register
Mnemonic	TP.TCPCI0.PCI0.SCAN_REGION_TYPE
Address	PCI0 (PE0): 000000000D030005 (SCOM) PCI1 (PE1): 000000000E030005 (SCOM) PCI2 (PE2): 000000000F030005 (SCOM)
Description	Scan Region and Type

Bits	SCOM	Field Mnemonic: Description
0	RWX	SYSTEM_FAST_INIT: The default is 0. When it is set to 1, the MASK bits in the CMSK chain decide which part will be scanned or scan0. MASK = 1 = scan0. MASK = 0 = part or scan chain.
1:2	RO	Constant = 0b00
3	NCX	SCAN_REGION_VITL: Scan clock region VITL (Vital = Clock).
4	RWX	SCAN_REGION_PERV: Scan clock region perv (Pervasive).
5	RWX	SCAN_REGION_UNIT1: Scan clock region pci00 - PCI.
6	RWX	SCAN_REGION_UNIT2: Scan clock region iopci0 - IOP.
7	RWX	SCAN_REGION_UNIT3: Scan clock region unused.
8	RWX	SCAN_REGION_UNIT4: Scan clock region unused.
9	RWX	SCAN_REGION_UNIT5: Scan clock region unused.
10	RWX	SCAN_REGION_UNIT6: Scan clock region unused.
11	RWX	SCAN_REGION_UNIT7: Scan clock region unused.
12	RWX	SCAN_REGION_UNIT8: Scan clock region unused.
13	RWX	SCAN_REGION_UNIT9: Scan clock region unused.
14	RWX	SCAN_REGION_UNIT10: Scan clock region PLL.
15:47	RO	Constant = 0b000000000000000000000000000000000
48	RW	SCAN_TYPE_FUNC: Scan chain functional.
49	RW	SCAN_TYPE_CFG: Scan chain mode (boot configuration and debug configuration).
50	RW	SCAN_TYPE_CCFG_GPTR: Scan chain CCFG / GPTR (Pervasive: CC configuration, Others: GPTR).
51	RW	SCAN_TYPE_REGF: Scan chain register files.
52	RW	SCAN_TYPE_LBIST: Scan chain lbst (LBIST).
53	RW	SCAN_TYPE_ABIST: Scan chain abst (ABIST).
54	RW	SCAN_TYPE_REPR: Scan chain repr (Array Repair).
55	RW	SCAN_TYPE_TIME: Scan chain time (Array Timing).
56	RW	SCAN_TYPE_BNDY: Scan chain bndy (Boundary I/Os).
57	RW	SCAN_TYPE_FARR: Scan chain FARR (fast array unload).
58	RW	SCAN_TYPE_CMSK: Scan chain CMSK (LBIST channel mask).
59	RW	SCAN_TYPE_INEX: Scan chain index (c14 ASIC).
60:63	RO	Constant = 0b0000

Register Name	Start/Stop Clocks Register
Mnemonic	TP.TCPCI0.PCI0.CLK_REGION
Address	PCI0 (PE0): 000000000D030006 (SCOM) PCI1 (PE1): 000000000E030006 (SCOM) PCI2 (PE2): 000000000F030006 (SCOM)
Description	Start/stop of clocks

Bits	SCOM	Field Mnemonic: Description
0:1	RWX	CLOCK_CMD: Command for clock control: 00 = NOP 01 = Start 10 = Stop 11 = Pulse (one pulse)
2	RWX	SLAVE_MODE: When selected, the clock command waits for the master chiplet to get started. The bit gets cleared after the incoming slave trigger, and Keep_MS_Mode_after_trigger is set to 0.
3	RWX	MASTER_MODE: When selected, the clock command sends out a trigger to all the slave chiplets. The bit gets cleared after sending out one master trigger, and Keep_MS_Mode_after_trigger is set to 0.
4	RWX	CLOCK_REGION_PERV: For clock region perv (Pervasive).
5	RWX	CLOCK_REGION_UNIT1: For clock region pci00 - PCI.
6	RWX	CLOCK_REGION_UNIT2: For clock region iopci0 - IOP.
7	RWX	CLOCK_REGION_UNIT3: For clock region unused.
8	RWX	CLOCK_REGION_UNIT4: For clock region unused.
9	RWX	CLOCK_REGION_UNIT5: For clock region unused.
10	RWX	CLOCK_REGION_UNIT6: For clock region unused.
11	RWX	CLOCK_REGION_UNIT7: For clock region unused.
12	RWX	CLOCK_REGION_UNIT8: For clock region unused.
13	RWX	CLOCK_REGION_UNIT9: For clock region unused.
14	RWX	CLOCK_REGION_UNIT10: For clock region PLL.
15:47	RO	Constant = 0b000000000000000000000000000000000
48	RWX	SEL_THOLD_SL: Select sl tholds.
49	RWX	SEL_THOLD_NSL: Select nsl tholds.
50	RWX	SEL_THOLD_ARY: Select array thold.
51	RO	Constant = 0b0
52	RW	CLOCK_PULSE_USE_EVEN: For dual mesh support. The default for pulse is an odd phase. When this bit is set, the pulse is applied on an even phase.
53:63	RO	Constant = 0b00000000000

Register Name	**Clocks Running SL Register**
Mnemonic	TP.TCPCI0.PCI0.CLOCK_STAT_SL
Address	
Description	Clocks running SL

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D030008 (SCOM)	000000000E030008 (SCOM)	000000000F030008 (SCOM)

Bits	SCOM	Field Mnemonic: Description
0:3	RO	Constant = 0b1111
4	ROX	CLOCK_STATUS_PERV_SL: Status of pervasive sl hld. 0 = Run 1 = Stop
5	ROX	CLOCK_STATUS_UNIT1_SL: Status of pci00 - pci sl hld. 0 = Run 1 = Stop
6	ROX	CLOCK_STATUS_UNIT2_SL: Status of iopci0 - iop sl hld. 0 = Run 1 = Stop
7	ROX	CLOCK_STATUS_UNIT3_SL: Status of unused sl hld. 0 = Run 1 = Stop
8	ROX	CLOCK_STATUS_UNIT4_SL: Status of unused sl hld. 0 = Run 1 = Stop
9	ROX	CLOCK_STATUS_UNIT5_SL: Status of unused sl hld. 0 = Run 1 = Stop
10	ROX	CLOCK_STATUS_UNIT6_SL: Status of unused sl hld. 0 = Run 1 = Stop
11	ROX	CLOCK_STATUS_UNIT7_SL: Status of unused sl hld. 0 = Run 1 = Stop
12	ROX	CLOCK_STATUS_UNIT8_SL: Status of unused sl hld. 0 = Run 1 = Stop
13	ROX	CLOCK_STATUS_UNIT9_SL: Status of unused sl hld. 0 = Run 1 = Stop
14	ROX	CLOCK_STATUS_UNIT10_SL: Status of pll sl hld. 0 = Run 1 = Stop
15:63	RO	Constant = 0b1111111111111111111111111111111111111111111111111

Register Name	Clocks Running NSLRegister		
Mnemonic	TP.TCPCI0.PCI0.CLOCK_STAT_NSL		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D030009 (SCOM)	000000000E030009 (SCOM)	000000000F030009 (SCOM)
Description	Clocks running NSL		

Bits	SCOM	Field Mnemonic: Description
0:3	RO	Constant = 0b1111
4	ROX	CLOCK_STATUS_PERV_NSL: Status of pervasive nsl hld. 0 = Run 1 = Stop
5	ROX	CLOCK_STATUS_UNIT1_NSL: Status of pci00 - pci nsl hld. 0 = Run 1 = Stop
6	ROX	CLOCK_STATUS_UNIT2_NSL: Status of iopci0 - iop nsl hld. 0 = Run 1 = Stop
7	ROX	CLOCK_STATUS_UNIT3_NSL: Status of unused nsl hld. 0 = Run 1 = Stop
8	ROX	CLOCK_STATUS_UNIT4_NSL: Status of unused nsl hld. 0 = Run 1 = Stop
9	ROX	CLOCK_STATUS_UNIT5_NSL: Status of unused nsl hld. 0 = Run 1 = Stop
10	ROX	CLOCK_STATUS_UNIT6_NSL: Status of unused nsl hld. 0 = Run 1 = Stop
11	ROX	CLOCK_STATUS_UNIT7_NSL: Status of unused nsl hld. 0 = Run 1 = Stop
12	ROX	CLOCK_STATUS_UNIT8_NSL: Status of unused nsl hld. 0 = Run 1 = Stop
13	ROX	CLOCK_STATUS_UNIT9_NSL: Status of unused nsl hld. 0 = Run 1 = Stop
14	ROX	CLOCK_STATUS_UNIT10_NSL: Status of pll nsl hld. 0 = Run 1 = Stop
15:63	RO	Constant = 0b1111111111111111111111111111111111111111111111111

Register Name	Clocks Running ARY Register
Mnemonic	TP.TCPCI0.PCI0.CLOCK_STAT_ARY
Address	**PCI0 (PE0)**: 000000000D03000A (SCOM) **PCI1 (PE1)**: 000000000E03000A (SCOM) **PCI2 (PE2)**: 000000000F03000A (SCOM)
Description	Clocks running ARY

Bits	SCOM	Field Mnemonic: Description
0:3	RO	Constant = 0b1111
4	ROX	CLOCK_STATUS_PERV_ARY: Status of pervasive ary hld . 0 = Run 1 = Stop
5	ROX	CLOCK_STATUS_UNIT1_ARY: Status of pci00 - pci ary hld. 0 = Run 1 = Stop
6	ROX	CLOCK_STATUS_UNIT2_ARY: Status of iopci0 - iop ary hld. 0 = Run 1 = Stop
7	ROX	CLOCK_STATUS_UNIT3_ARY: Status of unused ary hld. 0 = Run 1 = Stop
8	ROX	CLOCK_STATUS_UNIT4_ARY: Status of unused ary hld. 0 = Run 1 = Stop
9	ROX	CLOCK_STATUS_UNIT5_ARY: Status of unused ary hld. 0 = Run 1 = Stop
10	ROX	CLOCK_STATUS_UNIT6_ARY: Status of unused ary hld. 0 = Run 1 = Stop
11	ROX	CLOCK_STATUS_UNIT7_ARY: Status of unused ary hld. 0 = Run 1 = Stop
12	ROX	CLOCK_STATUS_UNIT8_ARY: Status of unused ary hld. 0 = Run 1 = Stop
13	ROX	CLOCK_STATUS_UNIT9_ARY: Status of unused ary hld. 0 = Run 1 = Stop
14	ROX	CLOCK_STATUS_UNIT10_ARY: Status of pll ary hld. 0 = Run 1 = Stop
15:63	RO	Constant = 0b1111111111111111111111111111111111111111111111111

Register Name	ABIST and IOBIST per Region Register		
Mnemonic	TP.TCPCI0.PCI0.BIST		
Address	PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
	000000000D03000B (SCOM)	000000000E03000B (SCOM)	000000000F03000B (SCOM)
Description	ABIST and IOBIST per region register.		

Bits	SCOM	Field Mnemonic: Description
0	RW	TC_BIST_START_TEST_DC: Keep this bit 0 during ABIST/IOBIST. It can be used to bypass the Run-N start. When this bit is set, the BIST_START_TEST goes high immediately without waiting for Run-N. BIST starts with the first hld clock cycle.
1	RW	TC_SRAM_ABIST_MODE_DC: Select the ABIST engines for SRAMs.
2	RW	TC_EDRAM_ABIST_MODE_DC: Select the ABIST engines for eDRAMs.
3	RW	TC_IOBIST_MODE_DC: Select the IOBIST engines.
4	RW	BIST_PERV: Region perv: 1 = BIST_START_TEST for this region is triggered. 0 = Region take not part of the ABIST/IOBIST run.
5	RW	BIST_UNIT1: Region pci00 - pci: 1 = BIST_START_TEST for this region is triggered. 0 = Region take not part of the ABIST/IOBIST run.
6	RW	BIST_UNIT2: Region iopci0 - iop: 1 = BIST_START_TEST for this region is triggered. 0 = Region take not part of the ABIST/IOBIST run.
7	RW	BIST_UNIT3: Region unused: 1 = BIST_START_TEST for this region is triggered. 0 = Region take not part of the ABIST/IOBIST run.
8	RW	BIST_UNIT4: Region unused: 1 = BIST_START_TEST for this region is triggered. 0 = Region take not part of the ABIST/IOBIST run.
9	RW	BIST_UNIT5: Region unused: 1 = BIST_START_TEST for this region is triggered. 0 = Region take not part of the ABIST/IOBIST run.
10	RW	BIST_UNIT6: Region unused: 1 = BIST_START_TEST for this region is triggered. 0 = region take not part of the ABIST/IOBIST run.
11	RW	BIST_UNIT7: Region unused: 1 = BIST_START_TEST for this region is triggered. 0 = Region take not part of the ABIST/IOBIST run.
12	RW	BIST_UNIT8: Region unused: 1 = BIST_START_TEST for this region is triggered. 0 = Region take not part of the ABIST/IOBIST run.
13	RW	BIST_UNIT9: Region unused: 1 = BIST_START_TEST for this region is triggered. 0 = Region take not part of the ABIST/IOBIST run.
14	RW	BIST_UNIT10: Region PLL: 1 = BIST_START_TEST for this region is triggered. 0 = Region take not part of the ABIST/IOBIST run.
15:47	RO	Constant = 0b000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RW	BIST_STROBE_WINDOW_EN: Enable Strobe window only in TE = 1 mode OPCGGO tester pin is enabling ABIST compare, once ABIST has been started. Special setup in ABIST engine is required. default is 0. System mode can not enable this feature.
49:63	RO	Constant = 0b000000000000000

Register Name	Checkstop per Region Register		
Mnemonic	TP.TCPCI0.PCI0.XSTOP1		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D03000C (SCOM)	000000000E03000C (SCOM)	000000000F03000C (SCOM)
Description	Checkstop per region register.		

Bits	SCOM	Field Mnemonic: Description
0	RW	XSTOP1_MASK_B: Mask for a checkstop to a clockstop of select regions (see xstop_perv,xstop_unit0..n). 0 = Ignore checkstop. 1 = Stop on checkstop.
1	RW	XSTOP1_UNUSED: Unused.
2	RW	TRIGGER_OPCG_ON_XSTOP1: Trigger an OPCG on a checkstop instead of performing a clockstop.
3	RW	XSTOP1_WAIT_ALLWAYS: When set to 1, a checkstop waits independent from the flush. The default is no wait, when flush in not set.
4	RW	XSTOP1_PERV: Region pervasive: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
5	RW	XSTOP1_UNIT1: Region pci00 - pci: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
6	RW	XSTOP1_UNIT2: Region iopci0 - iop: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
7	RW	XSTOP1_UNIT3: Region unused: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
8	RW	XSTOP1_UNIT4: Region unused: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
9	RW	XSTOP1_UNIT5: Region unused: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
10	RW	XSTOP1_UNIT6: Region unused: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
11	RW	XSTOP1_UNIT7: Region unused: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
12	RW	XSTOP1_UNIT8: Region unused: 1 = Region is stopped. 0 = Region keeps running on a checkstop.

Bits	SCOM	Field Mnemonic: Description
13	RW	XSTOP1_UNIT9: Region unused: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
14	RW	XSTOP1_UNIT10: Region PLL: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
15:47	RO	Constant = 0b000000000000000000000000000000000
48:59	RW	XSTOP1_WAIT_CYCLES: Defines how many cycles a checkstop waits after dropping a flush, before tholds get dropped. 0 - 4095 cycles are possible.
60:63	RO	Constant = 0b0000

Register Name	**Checkstop per Region Register**
Mnemonic	TP.TCPCI0.PCI0.XSTOP2
Address	<table><tr><th>PCI0 (PE0)</th><th>PCI1 (PE1)</th><th>PCI2 (PE2)</th></tr><tr><td>000000000D03000D (SCOM)</td><td>000000000E03000D (SCOM)</td><td>000000000F03000D (SCOM)</td></tr></table>
Description	Checkstop per region register

Bits	SCOM	Field Mnemonic: Description
0	RW	XSTOP2_MASK_B: Mask for a checkstop to a clockstop of select regions (see xstop_perv,xstop_unit0..n). 0 = Ignore checkstop. 1 = Stop on checkstop.
1	RW	XSTOP2_UNUSED: Unused.
2	RW	TRIGGER_OPCG_ON_XSTOP2: Trigger an OPCG on a checkstop instead of performing a clockstop.
3	RW	XSTOP2_WAIT_ALLWAYS: When set to 1, a checkstop waits independent from a flush. The default is no wait, when the flush in not set.
4	RW	XSTOP2_PERV: Region pervasive: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
5	RW	XSTOP2_UNIT1: Region pci00 - pci: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
6	RW	XSTOP2_UNIT2: Region iopci0 - iop: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
7	RW	XSTOP2_UNIT3: Region unused: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
8	RW	XSTOP2_UNIT4: Region unused: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
9	RW	XSTOP2_UNIT5: Region unused: 1 = Region is stopped. 0 = Region keeps running on a checkstop.

Bits	SCOM	Field Mnemonic: Description
10	RW	XSTOP2_UNIT6: Region unused: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
11	RW	XSTOP2_UNIT7: Region unused: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
12	RW	XSTOP2_UNIT8: Region unused: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
13	RW	XSTOP2_UNIT9: Region unused: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
14	RW	XSTOP2_UNIT10: Region PLL: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
15:47	RO	Constant = 0b000000000000000000000000000000000
48:59	RW	XSTOP2_WAIT_CYCLES: Defines how many cycle the checkstop waits after dropping flush, before tholds get dropped. 0 - 4095 cycles are possible.
60:63	RO	Constant = 0b0000

Register Name	**Checkstop per Region Register**
Mnemonic	TP.TCPCI0.PCI0.XSTOP3
Address	
Description	Checkstop per region register.

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D03000E (SCOM)	000000000E03000E (SCOM)	000000000F03000E (SCOM)

Bits	SCOM	Field Mnemonic: Description
0	RW	XSTOP3_MASK_B: Mask for a checkstop to a clockstop of select regions (see xstop_perv, xstop_unit0..n). 0 = Ignore checkstop. 1= Stop on checkstop.
1	RW	XSTOP3_UNUSED: Unused.
2	RW	TRIGGER_OPCG_ON_XSTOP3: Trigger an OPCG on a checkstop instead of performing a clockstop.
3	RW	XSTOP3_WAIT_ALLWAYS: When set to 1, a checkstop waits independent from a flush. The default is no wait, when flush in not set.
4	RW	XSTOP3_PERV: Region pervasive: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
5	RW	XSTOP3_UNIT1: Region pci00 - pci: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
6	RW	XSTOP3_UNIT2: Region iopci0 - iop: 1 = Region is stopped. 0 = Region keeps running on a checkstop.

Bits	SCOM	Field Mnemonic: Description
7	RW	XSTOP3_UNIT3: Region unused: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
8	RW	XSTOP3_UNIT4: Region unused: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
9	RW	XSTOP3_UNIT5: Region unused: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
10	RW	XSTOP3_UNIT6: Region unused: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
11	RW	XSTOP3_UNIT7: Region unused: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
12	RW	XSTOP3_UNIT8: Region unused: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
13	RW	XSTOP3_UNIT9: Region unused: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
14	RW	XSTOP3_UNIT10: Region PLL: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
15:47	RO	Constant = 0b000000000000000000000000000000000
48:59	RW	XSTOP3_WAIT_CYCLES: Defines how many cycle a checkstop waits after dropping a flush, before tholds get dropped. 0 - 4095 cycles are possible.
60:63	RO	Constant = 0b0000

Register Name	**Error Status of CC Register**
Mnemonic	TP.TCPCI0.PCI0.ERROR_STATUS
Address	**PCI0 (PE0)**: 000000000D03000F (SCOM) **PCI1 (PE1)**: 000000000E03000F (SCOM) **PCI2 (PE2)**: 000000000F03000F (SCOM)
Description	Error Status of CC register.

Bits	SCOM	Field Mnemonic: Description
0	RWX	PCB_WRITE_NOT_ALLOWED_ERR: Write on a read-only register.
1	RWX	PCB_READ_NOT_ALLOWED_ERR: Read not allowed; might be a write-only register.
2	RWX	PCB_PARITY_ON_CMD_ERR: Parity error on a command.
3	RWX	PCB_ADDRESS_NOT_VALID_ERR: Invalid address.
4	RWX	PCB_PARITY_ON_ADDR_ERR: Parity error on an address.
5	RWX	PCB_PARITY_ON_DATA_ERR: Parity error on data.
6	RWX	PCB_PROTECTED_ACCESS_INVALID_ERR: Protection violation.
7	RWX	PCB_PARITY_ON_SPCIF_ERR: Parity error on SPCIF.

Bits	SCOM	Field Mnemonic: Description
8	RWX	PCB_WRITE_AND_OPCG_IP_ERR: PCB write while the OPCG is running.
9	RWX	SCAN_READ_AND_OPCG_IP_ERR: Scan read when the OPCG is running.
10	RWX	CLOCK_CMD_CONFLICT_ERR: Clock command in progress.
11	RWX	SCAN_COLLISION_ERR: Scan region selected of running region.
12	RWX	PREVENTED_SCAN_COLLISION_ERR: PCB request to set the scan region that is running.
13	RWX	OPCG_TRIGGER_ERR: OPCG gets triggered while the OPCG is running.
14	RWX	PHASE_CNT_CORRUPTION_ERR: Phase counters inside the chiplet are out of sync.
15	RWX	CLOCK_CMD_PREVENTED_ERR: Security or scan collision prevented a clock start.
16	RWX	PARITY_ON_OPCG_SM_ERR: Parity error on an OPCG state machine.
17	RWX	PARITY_ON_CLOCK_MUX_REG_ERR: Parity error on a scan, clock region, or type or the clock status register.
18	RWX	PARITY_ON_OPCG_REG_ERR: Parity error on OPCG registers.
19	RWX	PARITY_ON_SYNC_CONFIG_REG_ERR: Parity error on the sync configuration register.
20	RWX	PARITY_ON_XSTOP_REG_ERR: Parity error on a checkstop register.
21	RWX	PARITY_ON_GPIO_REG_ERR: Parity error on GP0, 4, 5, 6 registers.
22	RWX	CLKCMD_REQUEST_ERR: Region clkcmd has one request pending but get a second one.
23	RWX	CBS_PROTOCOL_ERR: CBS protocol error. The REQ/ACK sequence is wrong.
24	RWX	VITL_ALIGN_ERR: VITL alignment is out of sync to the sync pulse.
25	RWX	UNIT_SYNC_LVL_ERR: Unit0 and Unit1 sync lvl pulses are not in sync. The AVP is broken.
26	RWX	PARITY_ON_SELFBOOT_CMD_STATE_ERR: Parity error on the selfboot command state.
27	RWX	UNUSED_ERROR27: Unused.
28	RWX	UNUSED_ERROR28: Unused.
29	RWX	UNUSED_ERROR29: Unused.
30	RWX	UNUSED_ERROR30: Unused.
31	RWX	UNUSED_ERROR31: Unused.

Register Name	OPCG Control Register Capture1		
Mnemonic	TP.TCPCI0.PCI0.OPCG_CAPT1		
Address	PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
	000000000D030010 (SCOM)	000000000E030010 (SCOM)	000000000F030010 (SCOM)
Description	OPCG Control Register Capture1 Register		

Bits	SCOM	Field Mnemonic: Description
0:3	RW	COUNT: 0000 = 12 cycles 0001 - 1100 = Cycles 1 - 12 1101 - 1111 = 24 normal, no fast.
4:8	RW	SEQ_01: Sequence cycle 1 for normal/slow region (sl, nsl, ary, se, fce).
9:13	RW	SEQ_02: Sequence cycle 2 for normal/slow region (sl, nsl, ary, se, fce).

Bits	SCOM	Field Mnemonic: Description
14:18	RW	SEQ_03: Sequence cycle 3 for normal/slow region (sl, nsl, ary, se, fce).
19:23	RW	SEQ_04: Sequence cycle 4 for normal/slow region (sl, nsl, ary, se, fce).
24:28	RW	SEQ_05: Sequence cycle 5 for normal/slow region (sl, nsl, ary, se, fce).
29:33	RW	SEQ_06: Sequence cycle 6 for normal/slow region (sl, nsl, ary, se, fce).
34:38	RW	SEQ_07: Sequence cycle 7 for normal/slow region (sl, nsl, ary, se, fce).
39:43	RW	SEQ_08: Sequence cycle 8 for normal/slow region (sl, nsl, ary, se, fce).
44:48	RW	SEQ_09: Sequence cycle 9 for normal/slow region (sl, nsl, ary, se, fce).
49:53	RW	SEQ_10: Sequence cycle 10 for normal/slow region (sl, nsl, ary, se, fce).
54:58	RW	SEQ_11: Sequence cycle 11 for normal/slow region (sl, nsl, ary, se, fce).
59:63	RW	SEQ_12: Sequence cycle 12 for normal/slow region (sl, nsl, ary, se, fce).

Register Name	OPCG Control Register Capture 2		
Mnemonic	TP.TCPCI0.PCI0.OPCG_CAPT2		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D030011 (SCOM)	000000000E030011 (SCOM)	000000000F030011 (SCOM)
Description	OPCG Control Register Capture 2		

Bits	SCOM	Field Mnemonic: Description
0:3	RW	UNUSED_CAPT2:
4:8	RW	SEQ_13_01EVEN: Sequence cycle 1: Even for fast region or cycle 13 for normal region (sl, nsl, ary, se, fce).
9:13	RW	SEQ_14_01ODD: Sequence cycle 1: Odd for fast region or cycle 14 for normal region (sl, nsl, ary, se, fce).
14:18	RW	SEQ_15_02EVEN: Sequence cycle 2: Even for fast region or cycle 15 for normal region (sl, nsl, ary, se, fce).
19:23	RW	SEQ_16_02ODD: Sequence cycle 2: Odd for fast region or cycle 16 for normal region (sl, nsl, ary, se, fce).
24:28	RW	SEQ_17_03EVEN: Sequence cycle 3: Even for fast region or cycle 17 for normal region (sl, nsl, ary, se, fce).
29:33	RW	SEQ_18_03ODD: Sequence cycle 3: Odd for fast region or cycle 18 for normal region (sl, nsl, ary, se, fce).
34:38	RW	SEQ_19_04EVEN: Sequence cycle 4: Even for fast region or cycle 19 for normal region (sl, nsl, ary, se, fce).
39:43	RW	SEQ_20_04ODD: Sequence cycle 4: Odd for fast region or cycle 20 for normal region (sl, nsl, ary, se, fce).
44:48	RW	SEQ_21_05EVEN: Sequence cycle 5: Even for fast region or cycle 21 for normal region (sl, nsl, ary, se, fce).
49:53	RW	SEQ_22_05ODD: Sequence cycle 5: Odd for fast region or cycle 22 for normal region (sl, nsl, ary, se, fce).
54:58	RW	SEQ_23_06EVEN: Sequence cycle 6: Even for fast region or cycle 23 for normal region (sl, nsl, ary, se, fce).
59:63	RW	SEQ_24_06ODD: Sequence cycle 6: Odd for fast region or cycle 24 for normal region (sl, nsl, ary, se, fce).

Register Name	OPCG Control Register Capture 3		
Mnemonic	TP.TCPCI0.PCI0.OPCG_CAPT3		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D030012 (SCOM)	000000000E030012 (SCOM)	000000000F030012 (SCOM)
Description	OPCG Control Register Capture 3 Register		

Bits	SCOM	Field Mnemonic: Description
0:3	RW	UNUSED_CAPT3:
4:8	RW	SEQ_07EVEN: Sequence cycle 7: Even for fast region (sl, nsl, ary, se, fce).
9:13	RW	SEQ_07ODD: Sequence cycle 7: Odd for fast region (sl, nsl, ary, se, fce).
14:18	RW	SEQ_08EVEN: Sequence cycle 8: Even for fast region (sl, nsl, ary, se, fce).
19:23	RW	SEQ_08ODD: Sequence cycle 8: Odd for fast region (sl, nsl, ary, se, fce).
24:28	RW	SEQ_09EVEN: Sequence cycle 9: Even for fast region (sl, nsl, ary, se, fce).
29:33	RW	SEQ_09ODD: Sequence cycle 9: Odd for fast region (sl, nsl, ary, se, fce).
34:38	RW	SEQ_10EVEN: Sequence cycle 10: Even for fast region (sl, nsl, ary, se, fce).
39:43	RW	SEQ_10ODD: Sequence cycle 10: Odd for fast region (sl, nsl, ary, se, fce).
44:48	RW	SEQ_11EVEN: Sequence cycle 11: Even for fast region (sl, nsl, ary, se, fce).
49:53	RW	SEQ_11ODD: Sequence cycle 11: Odd for fast region (sl, nsl, ary, se, fce).
54:58	RW	SEQ_12EVEN: Sequence cycle 12: Even for fast region (sl, nsl, ary, se, fce).
59:63	RW	SEQ_12ODD: Sequence cycle 12: Odd for fast region (sl, nsl, ary, se, fce).

Register Name	Debug CBS CC Register		
Mnemonic	TP.TCPCI0.PCI0.DBG_CBS_CC		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D030013 (SCOM)	000000000E030013 (SCOM)	000000000F030013 (SCOM)
Description	Debug CBS CC Register		

Bits	SCOM	Field Mnemonic: Description
0	ROX	DBG_RESET_EP: Reset endpoint. Are the CC and CTRL in a reset state?
1	ROX	DBG_OPCG_IP: OPCG in progress, not in idle.
2	ROX	DBG_VITL_CLKOFF: VITL HLD stopped when enabled. Need pipeline-latch-depth cycles to switch this latch.
3	ROX	DBG_TEST_ENABLE: Test enable.
4	ROX	DBG_CBS_REQ: CBS interface: request (latched).
5:7	ROX	DBG_CBS_CMD: CBS interface: command (latched).
8:12	ROX	DBG_CBS_STATE: CBS command state machine. 00000 = Idle.
13	ROX	DBG_SECURITY_DEBUG_MODE: Status of the security mode bit.

Bits	SCOM	Field Mnemonic: Description
14	ROX	DBG_CBS_PROTOCOL_ERROR: CBS protocol error. REQ raised, although the state machine is not in IDLE. Need reset_ep to clear this bit. There is no impact on IPL.
15	ROX	DBG_PCB_IDLE: The PCB interface is in the IDLE state.
16:19	ROX	DBG_CURRENT_OPCG_MODE: Current or latest OPCG MODE: 0 = NOP 1 = LBIST 2 = ABIST 3 = Run-N 4 = SCAN0 5 = SCAN 6 = SCAN rotate 7 = SCAN with UpdateDR 8 = SCAN with CaptureDR 9 = CLK change request 10 - 15 = Unused.
20:23	ROX	DBG_LAST_OPCG_MODE: Previous OPCG MODE.
24	ROX	DBG_PCB_ERROR: PCB interface error. Read the CC Error Register or set CBS_CMD = 001 to switch FSI CBS debug information to the CC Error Register.
25	ROX	DBG_PARITY_ERROR: Any parity error or non-PCB parity. Read the CC Error Register or set CBS_CMD = 001 to switch FSI CBS Debug Information to the CC Error Register.
26	ROX	DBG_CC_ERROR: Any other CC error. Read the CC Error Register or set CBS_CMD = 001 to switch FSI CBS Debug Information to the CC Error Register.
27	ROX	DBG_CHIPLET_IS_ALIGNED: This bit is 1 when a valid align pulse was send out.
28	ROX	DBG_PCB_REQUEST_SINCE_RESET: Reset clears this bit; the first PCB request sets it.
29	ROX	DBG_PARANOIA_TEST_ENABLE_CHANGE: The rising or falling edge on test enable, after reset - need reset_ep to clear, no impact on IPL.
30	ROX	DBG_PARANOIA_VITL_CLKOFF_CHANGE: Rising or falling edge on vitl_clkoff, after reset. Need reset_ep to clear. There is no impact on IPL.
31	ROX	TP_TPFSI_CBS_ACK: Only representation of CC ACK signal going to the FSI.

Register Name	CC Protect Mode Register
Mnemonic	TP.TCPCI0.PCI0.CC_PROTECT_MODE_REG
Address	<table><tr><th>PCI0 (PE0)</th><th>PCI1 (PE1)</th><th>PCI2 (PE2)</th></tr><tr><td>000000000D0303FE (SCOM)</td><td>000000000E0303FE (SCOM)</td><td>000000000F0303FE (SCOM)</td></tr></table>
Description	This register enables read and write protection.

Bits	SCOM	Field Mnemonic: Description
0	RW	CC_READ_PROTECT_ENABLE: Enable read protection.
1	RW	CC_WRITE_PROTECT_ENABLE: Enable write protection.

Register Name	Atomic Lock Register
Mnemonic	TP.TCPCI0.PCI0.CC_ATOMIC_LOCK_REG
Address	

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D0303FF (SCOM)	000000000E0303FF (SCOM)	000000000F0303FF (SCOM)

Description	This register enables an atomic lock.

Bits	SCOM	Field Mnemonic: Description
0	RW	CC_ATOMIC_LOCK_ENABLE: This bit enables an atomic lock.
1:4	ROX	CC_ATOMIC_ID: This field contains the atomic ID.
5:7	RO	Constant = 0b000
8:15	ROX	CC_ATOMIC_ACTIVITY: This field is the atomic lock counter.

Register Name	Global Checkstop FIR
Mnemonic	TP.TCPCI0.PCI0.XFIR
Address	

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D040000 (SCOM)	000000000E040000 (SCOM)	000000000F040000 (SCOM)

Description	This is a fault-isolation register for global FIRs.

Bits	SCOM	Field Mnemonic: Description
0	RWX	XFIR_IN0: Summary bit (any checkstop).
1	RWX	XFIR_IN1: Checkstop broadcast via OOB.
2	RWX	XFIR_IN2: Unused.
3	RWX	XFIR_IN3: Checkstop from the pervasive unit.
4	RWX	XFIR_IN4: Checkstop from ETU FIR in PCI0.
5	RWX	XFIR_IN5: Checkstop from IOPCI0.
6	RWX	XFIR_IN6: Checkstop from PBPCI0.
7:25	RWX	XFIR_IN7: Unused.
26	RWX	XFIR_IN26: Checkstop on debug trigger.

Register Name	Global Recoverable FIR
Mnemonic	TP.TCPCI0.PCI0.RFIR
Address	

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D040001 (SCOM)	000000000E040001 (SCOM)	000000000F040001 (SCOM)

Description	This is a fault-isolation register for global recoverable errors.

Bits	SCOM	Field Mnemonic: Description
0	ROX	RFIR_IN0: Local checkstop summary bit.
1	ROX	LFIR_RECOV_ERR: Recoverable error from the pervasive unit.
2	ROX	RFIR_IN4: Recover from the ETU FIR Register.
3	ROX	RFIR_IN5: Recover from the IOPCI0.
4	ROX	RFIR_IN6: Recover from the PBPCI0.
5:23	ROX	RFIR_IN7: Unused.

Register Name	**FIR Mask Register**
Mnemonic	TP.TCPCI0.PCI0.FIR_MASK
Address	
Description	FIR Mask

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D040002 (SCOM)	000000000E040002 (SCOM)	000000000F040002 (SCOM)

Bits	SCOM	Field Mnemonic: Description
0	RW	FIR_MASK_IN0: Mask for the XFIR summary bit (any checkstop).
1	RW	FIR_MASK_IN1: Mask for XFIR from other chiplets.
2	RW	FIR_MASK_IN2: Unused.
3	RW	FIR_MASK_IN3: Mask for XFIR/RFIR from the pervasive unit.
4	RW	FIR_MASK_IN4: Mask for PCI0 XFIR and RFIR.
5	RW	FIR_MASK_IN5: Mask for IOPCI0 XFIR and RFIR.
6	RW	FIR_MASK_IN6: Mask for IOPCI0 XFIR and RFIR.
7:25	RW	FIR_MASK_IN7: Unused.
26	RW	FIR_MASK_IN26: Mask for the debug trigger.

Register Name	**Special Attention Register**
Mnemonic	TP.TCPCI0.PCI0.SPATTN
Address	
Description	This register contains special attention fields.

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D040004 (SCOM) 000000000D040005 (SCOM1) 000000000D040006 (SCOM2)	000000000E040004 (SCOM) 000000000E040005 (SCOM1) 000000000E040006 (SCOM2)	000000000F040004 (SCOM) 000000000F040005 (SCOM1) 000000000F040006 (SCOM2)

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:9	ROX	NCX	NCX	SPATTN_IN: Unused special attentions.

Register Name	Special Attention Mask Register		
Mnemonic	TP.TCPCI0.PCI0.SPA_MASK		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D040007 (SCOM)	000000000E040007 (SCOM)	000000000F040007 (SCOM)
Description	This register provides a special attention mask.		

Bits	SCOM	Field Mnemonic: Description
0:9	RW	SPA_MASK_IN: Special attention mask.

Register Name	Mode Register		
Mnemonic	TP.TCPCI0.PCI0.EPS.FIR.MODE_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D040008 (SCOM)	000000000E040008 (SCOM)	000000000F040008 (SCOM)
Description	This register contains mode bits.		

Bits	SCOM	Field Mnemonic: Description
0	RW	MODE_IN0: Unused.
1	RW	MODE_IN1: Unused.
2	RW	MODE_IN2: Unused.
3	RW	MODE_IN3: Unused.
4	RW	MODE_IN4: Stop chip TOD on checkstop. (Unused in POWER9.)
5	RW	MODE_IN5: Stop chip TOD on recoverable. (Unused in POWER9.)
6	RW	MODE_IN6: Disable propagation of the checkstop to other chips.
7	RW	MODE_IN7: Unused.
8	RW	MODE_IN8: Enable a checkstop on special attention.
9	RW	MODE_IN9: Mask direct or local error.
10	RW	MODE_IN10: Unused.
11	RW	MODE_IN11: Unused.
12:15	RW	MODE_IN: Unused.

Register Name	Host Attention Register		
Mnemonic	TP.TCPCI0.PCI0.HOSTATTN		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D040009 (SCOM)	000000000E040009 (SCOM)	000000000F040009 (SCOM)
Description	This register contains host attention bits.		

Bits	SCOM	Field Mnemonic: Description
0	ROX	HOSTATTN_IN0: Host attention summary bit.
1	ROX	HOSTATTN_IN1: Unused.
2	ROX	HOSTATTN_IN2: Unused.
3	ROX	HOSTATTN_IN3: Unused.
4	ROX	HOSTATTN_IN4: Unused.
5	ROX	HOSTATTN_IN5: Unused.
6	ROX	HOSTATTN_IN6: Unused.
7	ROX	HOSTATTN_IN7: Unused.
8	ROX	HOSTATTN_IN8: Unused.
9	ROX	HOSTATTN_IN9: Unused.
10	ROX	HOSTATTN_IN10: Unused.
11	ROX	HOSTATTN_IN11: Unused.
12	ROX	HOSTATTN_IN12: Unused.
13	ROX	HOSTATTN_IN13: Unused.
14	ROX	HOSTATTN_IN14: Unused.
15	ROX	HOSTATTN_IN15: Unused.
16	ROX	HOSTATTN_IN16: Unused.
17	ROX	HOSTATTN_IN17: Unused.
18	ROX	HOSTATTN_IN18: Unused.
19	ROX	HOSTATTN_IN19: Unused.
20	ROX	HOSTATTN_IN20: Unused.
21	ROX	HOSTATTN_IN21: Unused.
22	ROX	HOSTATTN_IN22: Unused.

Register Name	**Local FIR**
Mnemonic	TP.TCPCI0.PCI0.LOCAL_FIR
Address	<table><tr><th>PCI0 (PE0)</th><th>PCI1 (PE1)</th><th>PCI2 (PE2)</th></tr><tr><td>000000000D04000A (SCOM) 000000000D04000B (SCOM1) 000000000D04000C (SCOM2)</td><td>000000000E04000A (SCOM) 000000000E04000B (SCOM1) 000000000E04000C (SCOM2)</td><td>000000000F04000A (SCOM) 000000000F04000B (SCOM1) 000000000F04000C (SCOM2)</td></tr></table>
Description	This is a fault-isolation register for local errors.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_IN0: CFIR internal parity error.
1	RWX	WOX_AND	WOX_OR	FIR_IN1: Chiplet Control Register: PCB access error.
2	RWX	WOX_AND	WOX_OR	FIR_IN2: Clock controller: PCB access error.
3	RWX	WOX_AND	WOX_OR	FIR_IN3: Clock controller: Summarized error. Read the ERROR_STATUS Register with SCOM address nn3000F for details.
4	RWX	WOX_AND	WOX_OR	FIR_IN4: PSCOM logic: PCB access error.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
5	RWX	WOX_AND	WOX_OR	FIR_IN5: PSCOM logic: Summarized internal errors.
6	RWX	WOX_AND	WOX_OR	FIR_IN6: Thermal logic: Summarized internal errors.
7	RWX	WOX_AND	WOX_OR	FIR_IN7: Thermal logic: PCB access error.
8	RWX	WOX_AND	WOX_OR	FIR_IN8: Thermal logic: Temperature critical trip error.
9	RWX	WOX_AND	WOX_OR	FIR_IN9: Thermal logic: Temperature fatal trip error.
10	RWX	WOX_AND	WOX_OR	FIR_IN10: Thermal logic: Voltage trip error. Unused in the POWER9 processor.
11	RWX	WOX_AND	WOX_OR	FIR_IN11: Debug logic: SCOM satellite error.
12	RWX	WOX_AND	WOX_OR	FIR_IN12: Trace logic: SCOM satellite error: Trace0.
13	RWX	WOX_AND	WOX_OR	FIR_IN13: Trace logic: SCOM satellite error: Trace0.
14	RWX	WOX_AND	WOX_OR	FIR_IN14: Unused.
15	RWX	WOX_AND	WOX_OR	FIR_IN15: Unused.
16	RWX	WOX_AND	WOX_OR	FIR_IN16: Unused.
17	RWX	WOX_AND	WOX_OR	FIR_IN17: Unused.
18	RWX	WOX_AND	WOX_OR	FIR_IN18: Unused.
19	RWX	WOX_AND	WOX_OR	FIR_IN19: Unused.
20	RWX	WOX_AND	WOX_OR	FIR_IN20: Unused.
21	RWX	WOX_AND	WOX_OR	FIR_IN21: Unused.
22	RWX	WOX_AND	WOX_OR	FIR_IN22: Unused.
23	RWX	WOX_AND	WOX_OR	FIR_IN23: Unused.
24	RWX	WOX_AND	WOX_OR	FIR_IN24: Unused.
25	RWX	WOX_AND	WOX_OR	FIR_IN25: Unused.
26	RWX	WOX_AND	WOX_OR	FIR_IN26: Unused.
27	RWX	WOX_AND	WOX_OR	FIR_IN27: Unused.
28	RWX	WOX_AND	WOX_OR	FIR_IN28: Unused.
29	RWX	WOX_AND	WOX_OR	FIR_IN29: Unused.
30	RWX	WOX_AND	WOX_OR	FIR_IN30: Unused.
31	RWX	WOX_AND	WOX_OR	FIR_IN31: Unused.
32	RWX	WOX_AND	WOX_OR	FIR_IN32: Unused.
33	RWX	WOX_AND	WOX_OR	FIR_IN33: Unused.
34	RWX	WOX_AND	WOX_OR	FIR_IN34: Unused.
35	RWX	WOX_AND	WOX_OR	FIR_IN35: Unused.
36	RWX	WOX_AND	WOX_OR	FIR_IN36: Unused.
37	RWX	WOX_AND	WOX_OR	FIR_IN37: Unused.
38	RWX	WOX_AND	WOX_OR	FIR_IN38: Unused.
39	RWX	WOX_AND	WOX_OR	FIR_IN39: Unused.
40	RWX	WOX_AND	WOX_OR	FIR_IN40: Unused.
41	RWX	WOX_AND	WOX_OR	FIR_IN41: Malfunction alert broadcast via the OOB.

Register Name	Local FIR Mask Register		
Mnemonic	TP.TCPCI0.PCI0.EPS.FIR.LOCAL_FIR_MASK		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D04000D (SCOM) 000000000D04000E (SCOM1) 000000000D04000F (SCOM2)	000000000E04000D (SCOM) 000000000E04000E (SCOM1) 000000000E04000F (SCOM2)	000000000F04000D (SCOM) 000000000F04000E (SCOM1) 000000000F04000F (SCOM2)
Description	This register masks the local FIR bits.		

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:41	RW	WO_AND	WO_OR	LFIR_MASK_IN: Mask for the LEM error collection vector.

Register Name	Local FIR Action0 Register		
Mnemonic	TP.TCPCI0.PCI0.EPS.FIR.LOCAL_FIR_ACTION0		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D040010 (SCOM)	000000000E040010 (SCOM)	000000000F040010 (SCOM)
Description	Local FIR Action0		

Bits	SCOM	Field Mnemonic: Description
0:41	RW	FIR_ACTION0_IN: Action0 mask.

Register Name	Local FIR Action1 Register		
Mnemonic	TP.TCPCI0.PCI0.EPS.FIR.LOCAL_FIR_ACTION1		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D040011 (SCOM)	000000000E040011 (SCOM)	000000000F040011 (SCOM)
Description	Local FIR Action1		

Bits	SCOM	Field Mnemonic: Description
0:41	RW	FIR_ACTION1_IN: Action1 mask.

Register Name	Group Checkstop Mask Register		
Mnemonic	TP.TCPCI0.PCI0.EPS.FIR.GXSTOP_TRIG_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D040013 (SCOM)	000000000E040013 (SCOM)	000000000F040013 (SCOM)
Description	This register masks group checkstops.		

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP_TRIG_IN0: Mask bit for a system checkstop.
1	RW	GXSTP_TRIG_IN1: Mask bit for a recoverable error.
2	RW	GXSTP_TRIG_IN2: Mask bit for special attention.
3	RW	GXSTP_TRIG_IN3: Mask bit for a local checkstop.
4	RW	GXSTP_TRIG_IN4: Mask bit for a type 4 error (host attention).
5	RW	GXSTP_TRIG_IN5: Mask bit for an OOB sys_checkstop input (0).
6	RW	GXSTP_TRIG_IN6: Mask bit for an OOB sys_checkstop input (1).
7	RW	GXSTP_TRIG_IN7: Mask bit for a group checkstop input (0).
8	RW	GXSTP_TRIG_IN8: Mask bit for a group checkstop input (1).
9	RW	GXSTP_TRIG_IN9: Mask bit for a debug checkstop on a trigger.
10	RW	GXSTP_TRIG_IN10: Unused.
11	RW	GXSTP_TRIG_IN11: Unused.

Register Name	**Group0 Checkstop Mask Register**		
Mnemonic	TP.TCPCI0.PCI0.EPS.FIR.GXSTOP0_MASK_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D040014 (SCOM)	000000000E040014 (SCOM)	000000000F040014 (SCOM)
Description	This register masks group 0 checkstops.		

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP0_TRIG_IN0: Mask bit for a system checkstop.
1	RW	GXSTP0_TRIG_IN1: Mask bit for a recoverable error.
2	RW	GXSTP0_TRIG_IN2: Mask bit for special attention.
3	RW	GXSTP0_TRIG_IN3: Mask bit for a local checkstop.
4	RW	GXSTP0_TRIG_IN4: Mask bit for a type 4 error (host attention).
5	RW	GXSTP0_TRIG_IN5: Mask bit for an OOB sys_checkstop input (0).
6	RW	GXSTP0_TRIG_IN6: Mask bit for an OOB sys_checkstop input (1).
7	RW	GXSTP0_TRIG_IN7: Mask bit for a group checkstop input (0).
8	RW	GXSTP0_TRIG_IN8: Mask bit for a group checkstop input (1).
9	RW	GXSTP0_TRIG_IN9: Mask bit for a debug checkstop on a trigger.
10	RW	GXSTP0_TRIG_IN10: Unused.
11	RW	GXSTP0_TRIG_IN11: Unused.

Register Name	Group1 Checkstop Mask Register		
Mnemonic	TP.TCPCI0.PCI0.EPS.FIR.GXSTOP1_MASK_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D040015 (SCOM)	000000000E040015 (SCOM)	000000000F040015 (SCOM)
Description	This register masks group 1 checkstops.		

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP1_TRIG_IN0: Mask bit for a system checkstop.
1	RW	GXSTP1_TRIG_IN1: Mask bit for a recoverable error.
2	RW	GXSTP1_TRIG_IN2: Mask bit for special attention.
3	RW	GXSTP1_TRIG_IN3: Mask bit for a local checkstop.
4	RW	GXSTP1_TRIG_IN4: Mask bit for a type 4 error (host attention).
5	RW	GXSTP1_TRIG_IN5: Mask bit for an OOB sys_checkstop input (0).
6	RW	GXSTP1_TRIG_IN6: Mask bit for an OOB sys_checkstop input (1).
7	RW	GXSTP1_TRIG_IN7: Mask bit for a group checkstop input (0).
8	RW	GXSTP1_TRIG_IN8: Mask bit for a group checkstop input (1).
9	RW	GXSTP1_TRIG_IN9: Mask bit for a debug checkstop on a trigger.
10	RW	GXSTP1_TRIG_IN10: Unused.
11	RW	GXSTP1_TRIG_IN11: Unused.

Register Name	Group2 Checkstop Mask Register		
Mnemonic	TP.TCPCI0.PCI0.EPS.FIR.GXSTOP2_MASK_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D040016 (SCOM)	000000000E040016 (SCOM)	000000000F040016 (SCOM)
Description	This register masks group 2 checkstops.		

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP2_TRIG_IN0: Mask bit for a system checkstop.
1	RW	GXSTP2_TRIG_IN1: Mask bit for a recoverable error.
2	RW	GXSTP2_TRIG_IN2: Mask bit for special attention.
3	RW	GXSTP2_TRIG_IN3: Mask bit for a local checkstop.
4	RW	GXSTP2_TRIG_IN4: Mask bit for a type 4 error (host attention).
5	RW	GXSTP2_TRIG_IN5: Mask bit for an OOB sys_checkstop input (0).
6	RW	GXSTP2_TRIG_IN6: Mask bit for an OOB sys_checkstop input (1).
7	RW	GXSTP2_TRIG_IN7: Mask bit for a group checkstop input (0).
8	RW	GXSTP2_TRIG_IN8: Mask bit for a group checkstop input (1).
9	RW	GXSTP2_TRIG_IN9: Mask bit for a debug checkstop on a trigger.

Bits	SCOM	Field Mnemonic: Description
10	RW	GXSTP2_TRIG_IN10: Unused.
11	RW	GXSTP2_TRIG_IN11: Unused.

Register Name	Summary Mask Register		
Mnemonic	TP.TCPCI0.PCI0.EPS.FIR.SUM_MASK_REG		
Address	PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
	000000000D040017 (SCOM)	000000000E040017 (SCOM)	000000000F040017 (SCOM)
Description	This register contains summary bits.		

Bits	SCOM	Field Mnemonic: Description
0	RW	SMASK_IN0: System checkstop summary bit.
1	RW	SMASK_IN1: Recoverable summary bit.
2	RW	SMASK_IN2: Special attention summary bit.
3	RW	SMASK_IN3: Local checkstop summary bit.
4	RW	SMASK_IN4: Type4 (host attention summary bit.

Register Name	Local Checkstop Register		
Mnemonic	TP.TCPCI0.PCI0.LOCAL_XSTOP_ERR		
Address	PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
	000000000D040018 (SCOM)	000000000E040018 (SCOM)	000000000F040018 (SCOM)
Description	This register contains local checkstop bits.		

Bits	SCOM	Field Mnemonic: Description
0	ROX	LOCAL_XSTOP_IN0: Local checkstop summary bit.
1	ROX	LOCAL_XSTOP_IN1: Unused.
2	ROX	LOCAL_XSTOP_IN2: Unused.
3	ROX	LOCAL_XSTOP_IN3: Unused.
4	ROX	LOCAL_XSTOP_IN4: Unused.
5	ROX	LOCAL_XSTOP_IN5: Unused.
6	ROX	LOCAL_XSTOP_IN6: Unused.
7	ROX	LOCAL_XSTOP_IN7: Unused.
8	ROX	LOCAL_XSTOP_IN8: Unused.
9	ROX	LOCAL_XSTOP_IN9: Unused.
10	ROX	LOCAL_XSTOP_IN10: Unused.
11	ROX	LOCAL_XSTOP_IN11: Unused.
12	ROX	LOCAL_XSTOP_IN12: Unused.

Bits	SCOM	Field Mnemonic: Description
13	ROX	LOCAL_XSTOP_IN13: Unused.
14	ROX	LOCAL_XSTOP_IN14: Unused.
15	ROX	LOCAL_XSTOP_IN15: Unused.
16	ROX	LOCAL_XSTOP_IN16: Unused.
17	ROX	LOCAL_XSTOP_IN17: Unused.
18	ROX	LOCAL_XSTOP_IN18: Unused.
19	ROX	LOCAL_XSTOP_IN19: Unused.
20	ROX	LOCAL_XSTOP_IN20: Unused.
21	ROX	LOCAL_XSTOP_IN21: Unused.
22	ROX	LOCAL_XSTOP_IN22: Unused.

Register Name	**Local Checkstop Mask Register**
Mnemonic	TP.TCPCI0.PCI0.LOCAL_XSTOP_MASK
Address	
Description	This register masks local checkstops.

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D040019 (SCOM)	000000000E040019 (SCOM)	000000000F040019 (SCOM)

Bits	SCOM	Field Mnemonic: Description
0:21	RW	LOCAL_XSTOP_MASK_IN: Local checkstop mask.

Register Name	**Host Attention Mask Register**
Mnemonic	TP.TCPCI0.PCI0.HOSTATTN_MASK
Address	
Description	This register masks host attention.

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D04001A (SCOM)	000000000E04001A (SCOM)	000000000F04001A (SCOM)

Bits	SCOM	Field Mnemonic: Description
0:21	RW	HOSTATTN_MASK_IN: Host attention mask.

Register Name	**DTS Thermal Sensor Loop1 Results Register**
Mnemonic	TP.TCPCI0.PCI0.EPS.THERM.DTS_RESULT0
Address	
Description	This register contains the DTS thermal sensor loop1 results.

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D050000 (SCOM)	000000000E050000 (SCOM)	000000000F050000 (SCOM)

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	DTS_0_RESULT: Calibrated DTS result of the sensor with ID 0.
16:31	ROX	DTS_1_RESULT: Calibrated DTS result of the sensor with ID 1.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	DTS Trace Results Register
Mnemonic	TP.TCPCI0.PCI0.EPS.THERM.DTS_TRC_RESULT
Address	**PCI0 (PE0)**: 000000000D050003 (SCOM) **PCI1 (PE1)**: 000000000E050003 (SCOM) **PCI2 (PE2)**: 000000000F050003 (SCOM)
Description	This register contains DTS trace results.

Bits	SCOM	Field Mnemonic: Description
0:43	ROX	TIMESTAMP_COUNTER_VALUE: Time stamp counter value during DTS trace mode.
44	ROX	TIMESTAMP_COUNTER_OVERFLOW_ERR: Overflow error bit of the time stamp counter value during DTS trace mode.
45:47	RO	Constant = 0b000
48:63	ROX	DTS_1_RESULT: Calibrated DTS result of the sensor with ID 1.

Register Name	CPM and DTS Enables and Controls Register
Mnemonic	TP.TCPCI0.PCI0.EPS.THERM.THERM_MODE_REG
Address	**PCI0 (PE0)**: 000000000D05000F (SCOM) **PCI1 (PE1)**: 000000000E05000F (SCOM) **PCI2 (PE2)**: 000000000F05000F (SCOM)
Description	This register is used to enable and control the critical path monitor (CPM) and digital thermal sensor (DTS).

Bits	SCOM	Field Mnemonic: Description
0	RW	THERM_DIS_CPM_BUBBLE_CORR: Critical path result bubble correction active.
1	RW	THERM_FORCE_THRES_ACT: This bit forces tpc_therm_thres_mac clock gating off and activates the clocks.
2:4	RW	THERM_THRES_TRIP_ENA: Enables therm_thres_trip compare. 1xx = trip0 - warning. x1x = trip1 - critical. xx1 = trip2 - fatal.
5	RW	THERM_DTS_SAMPLE_ENA: 0 = No DTS sampling. 1 = DTS sampling is enabled and a below-counter compare match can occur.

Bits	SCOM	Field Mnemonic: Description
6:9	RW	THERM_SAMPLE_PULSE_CNT: A 16 MHz sample pulse is fed into an 18-bit counter. With the therm_sample_pulse_cnt , it is possible to select a high-order bit of the counter to enable resolutions of sampling DTSs between 2.5 µs and 80 ms. An edge-detection circuit detects the rising edge of the selected counter bit, and this triggers a DTS sample. 0000 = 16 ms. 0001 = 8 ms. 0010 = 4 ms. 0011 = 2 ms. 0100 = 1 ms. 0101 = 0.5 ms. 0110 = 250 µs. 0111 = 125 µs. 1000 = 62.5 µs. 1001 = 31.3 µs. 1010 = 15.6 µs. 1011 = 7.8 µs. 1100 = 3.9 µs. 1101 = 2 µs. 1110 = 1 µs. 1111 = 0.5 µs.
10:11	RW	THERM_THRES_MODE_ENA: Forces maximum or minimum mode in the threshold unit: 00 = Off. 11 = Illegal. 10 = Maximum mode. 01 = Minimum mode.
12	RW	DTS_TRIGGER_MODE: Unused.
13	RW	DTS_TRIGGER_SEL: Unused.
14	RW	THERM_THRES_OVERFLOW_MASK: 0 = therm_overflow_err is enabled. 1 = therm_overflow_err is disabled.
15	RW	THERM_MODE_UNUSED: Unused.
16:19	RW	THERM_DTS_READ_SEL: Selects which DTS result is provided with PCB read addr_v(4): 0000 = DTS 0. 0001 = DTS 1. 0010 = DTS 2. 0100 = DTS 4. 1111 = Worst-case sensor.
20:21	RW	THERM_DTS_ENABLE_L1: Loop1 DTS enables: 1x = DTS 0 available. x1 = DTS 1 available.
22:34	RO	Constant = 0b0000000000000
35:36	RW	therm_cpm_enable_l1.

Register Name	Skitter Control Register
Mnemonic	TP.TCPCI0.PCI0.EPS.THERM.SKITTER_MODE_REG
Address	

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D050010 (SCOM)	000000000E050010 (SCOM)	000000000F050010 (SCOM)

Description	This register controls skitter.

Bits	SCOM	Field Mnemonic: Description
0	RW	SKITTER_HOLD_SAMPLE: Forces skitter to hold the current sample.
1	RW	DISABLE_SKITTER_STICKINESS: A value of '0' specifies accumulation mode. A value of '1' samples a new value on each cycle and resets the sticky value.
2:3	RW	SKITTER_MODE_UNUSED1: Unused.
4:5	RW	SKITTER_HOLD_DBGTRIG_SEL: bit0 = hold_on_trigger0 bit1 = hold_on_trigger1
6:7	RW	SKITTER_RESET_TRIG_SEL: bit0 = reset_sticky_on_trigger0 bit1 = reset_sticky_on_trigger1
8:9	RW	SKITTER_SAMPLE_GUTS: Selects which guts to measure: 00 = guts1. 01 = guts2. 10 = guts3. 11 = guts4.
10:43	RO	Constant = 0b0000000000000000000000000000000000
44	ROX	SKITTER_HOLD_SAMPLE_WITH_TRIGGER: Forces skitter to hold the current sample on the DBG trigger. This has the highest priority.
45	ROX	SKITTER_DATA_V_LT: If set to '1', the data requested by a skitter force read register has finished and data is present in skitter data register in the collector macro. The data be read by any combination of V25, V26, or V27 PCB reads.

Register Name	**Error Injection Control Register**
Mnemonic	TP.TCPCI0.PCI0.EPS.THERM.INJECT_REG
Address	
Description	This register controls error injection.

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D050011 (SCOM)	000000000E050011 (SCOM)	000000000F050011 (SCOM)

Bits	SCOM	Field Mnemonic: Description
0:1	RW	THERM_INJECT_TRIP: 00 = No injection. 01 = Warning trip-level injection. 10 = Critical trip-level injection. 11 = Fatal trip-level injection.
2:3	RW	THERM_INJECT_MODE: 00 = No injection. 01 = Injection on the next DTS sample. 10 = Solid injection for the next DTS samples until the bit setting changes. 11 = Not used.

Register Name	Control/Force Reset Register
Mnemonic	TP.TCPCI0.PCI0.EPS.THERM.CONTROL_REG
Address	
Description	Control/Force Reset Register

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D050012 (SCOM)	000000000E050012 (SCOM)	000000000F050012 (SCOM)

Bits	SCOM	Field Mnemonic: Description
0	WO_1P	reset_trip_history.
1	WO_1P	reset_sample_pulse_cnt.
2	WO_1P	f_reset_cpm_rd.
3	WO_1P	f_reset_cpm_wr.
4	WO_1P	reset_sample_dts.
5	WO_1P	force_sample_dts.
6	WO_1P	force_sample_dts_interruptible.
7	WO_1P	force_reset_thres_l1results.
8	WO_1P	force_reset_thres_l2results.
9	WO_1P	force_reset_thres_l3results.
10	WO_1P	force_measure_volt_interruptible.
11	WO_1P	force_reset_measure_volt.
12	WO_1P	force_shift_sensor.

Register Name	Thermal Error Status Register
Mnemonic	TP.TCPCI0.PCI0.EPS.THERM.ERR_STATUS_REG
Address	
Description	This register contains error status information.

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D050013 (SCOM)	000000000E050013 (SCOM)	000000000F050013 (SCOM)

Bits	SCOM	Field Mnemonic: Description
0	ROX	serial_shiftcnt_modereg_parity_err_hold.
1	ROX	therm_modereg_parity_err_hold.
2	ROX	skitter_modereg_parity_err_hold.
3	ROX	skitter_forcereg_parity_err_hold.
4	ROX	scan_init_version_reg_parity_err_hold.
5	ROX	volt_modereg_parity_err_hold.
6	ROX	skitter_clksrcreg_parity_err_hold.
7	ROX	count_state_err_hold.
8	ROX	run_state_err_hold.

Bits	SCOM	Field Mnemonic: Description
9	ROX	thres_therm_state_err_hold.
10	ROX	thres_therm_overflow_err_hold.
11	ROX	shifter_parity_err_hold.
12	ROX	shifter_valid_err_hold.
13	ROX	timeout_err_hold.
14	ROX	f_skitter_err_hold.
15	ROX	pcb_err_hold_out.
16	ROX	SERIAL_SHIFTCNT_MODEREG_PARITY_ERR_MASK: Serial shift count parity error mask.
17	ROX	THERM_MODEREG_PARITY_ERR_MASK: Thermal Mode Register parity error mask.
18	ROX	SKITTER_MODEREG_PARITY_ERR_MASK: Skitter Mode Register parity error mask.
19	ROX	SKITTER_FORCEREG_PARITY_ERR_MASK: Skitter Force Register parity error mask.
20	ROX	SCAN_INIT_VERSION_REG_PARITY_ERR_MASK: Scan Initial Version Register parity error mask.
21	ROX	VOLT_MODEREG_PARITY_ERR_MASK: Volt Mode Register parity error mask.
22	RO	Constant = 0b0
23	ROX	COUNT_STATE_ERR_MASK: Count state machine error mask.
24	ROX	RUN_STATE_ERR_MASK: Run state machine error mask.
25	ROX	THRES_STATE_ERR_MASK: Threshold state machine error mask.
26	ROX	OVERFLOW_ERR_MASK: DTS calibration calculation overflow error mask.
27	ROX	SHIFTER_PARITY_ERR_MASK: Shifter parity error mask.
28	ROX	SHIFTER_VALID_ERR_MASK: Shifter valid error mask.
29	ROX	TIMEOUT_ERR_MASK: Timeout error mask.
30	ROX	F_SKITTER_READ_ERR_MASK: Force skitter read error mask.
31	ROX	PCB_ERR_MASK: Pervasive control bus error mask.
32:39	RO	Constant = 0b00000000
40:43	ROX	count_state_lt.
44:46	ROX	run_state_lt.
47	ROX	shift_dts_lt.
48	ROX	shift_volt_lt.
49:50	ROX	read_state_lt.
51:54	ROX	write_state_lt.
55	ROX	sample_dts_lt.
56	ROX	measure_volt_lt.
57	ROX	read_cpm_lt.
58	ROX	write_cpm_lt.
59	ROX	Unused.
60:63	RO	Constant = 0b0000

Register Name	Skitter Force Read Register
Mnemonic	TP.TCPCI0.PCI0.EPS.THERM.SKITTER_FORCE_REG
Address	

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D050014 (SCOM)	000000000E050014 (SCOM)	000000000F050014 (SCOM)

Description	This register forces a skitter read.

Bits	SCOM	Field Mnemonic: Description
0	RW	F_SKITTER_READ: Forces the read of that particular skitter.

Register Name	Skitter Clock Source Control Register
Mnemonic	TP.TCPCI0.PCI0.EPS.THERM.SKITTER_CLKSRC_REG
Address	

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D050016 (SCOM)	000000000E050016 (SCOM)	000000000F050016 (SCOM)

Description	This register contains skitter controls.

Bits	SCOM	Field Mnemonic: Description
0:2	RW	SKITTER0_CLKSRC: Selects the clock to measure: 000 = Local mesh clock. 001 = External pin skitter_c1_1_in. 010 = Local d1clk only if d_mode = 1. 011 = External pin skitter_c1_2_in. 100 = Local lclk only if d_mode = 1. 101 = External pin skitter_c1_3_in. 110 = Unused. 111 = External pin skitter_c1_4_in.
3:35	RO	Constant = 0b000000000000000000000000000000000
36:37	RW	SKITTER0_DELAY_SELECT: Selects the delay to be added between the skitter0 clock source multiplexer and the inverter chain. The base line delay is 12.2 psec. 00 = No delay. 01 = 0.6 psec. 10 = 1.8 psec. 11 = 5 psec.

Register Name	Skitter Data Register Read Bits 0:63
Mnemonic	TP.TCPCI0.PCI0.EPS.THERM.SKITTER_DATA0
Address	

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D050019 (SCOM)	000000000E050019 (SCOM)	000000000F050019 (SCOM)

Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved.

Register Name	Skitter Data Register Read Bits 32:95		
Mnemonic	TP.TCPCI0.PCI0.EPS.THERM.SKITTER_DATA1		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D05001A (SCOM)	000000000E05001A (SCOM)	000000000F05001A (SCOM)
Description	This is a reserved register.		

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved.

Register Name	Skitter Data Register Read Bits 64:127		
Mnemonic	TP.TCPCI0.PCI0.EPS.THERM.SKITTER_DATA2		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D05001B (SCOM)	000000000E05001B (SCOM)	000000000F05001B (SCOM)
Description	This is a reserved register.		

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved.

Register Name	Timestamp Counter Read Register		
Mnemonic	TP.TCPCI0.PCI0.EPS.THERM.TIMESTAMP_COUNTER_READ		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D05001C (SCOM)	000000000E05001C (SCOM)	000000000F05001C (SCOM)
Description	This register contains the time-stamp counter value during DTS trace mode and an overflow error bit.		

Bits	SCOM	Field Mnemonic: Description
0:43	ROX	TIMESTAMP_COUNTER_VALUE: Time stamp counter value during DTS trace mode.
44	ROX	TIMESTAMP_COUNTER_OVERFLOW_ERR: Overflow error bit of the time-stamp counter value during DTS trace mode.

9. PCI 0 Chiplet PCB Slave

The POWER9 processor registers are listed alphabetically by mnemonic in the following address table.

Mnemonic	Address	Page
TP.TPCHIP.NET.PCBSLPCI0.ASSIST_INTERRUPT_REG	0x000000000D0F0011	1947
TP.TPCHIP.NET.PCBSLPCI0.ATOMIC_LOCK_REG	0x000000000D0F03FF	1957
TP.TPCHIP.NET.PCBSLPCI0.ATTN_INTERRUPT_REG	0x000000000D0F001A	1948
TP.TPCHIP.NET.PCBSLPCI0.EDRAM_STATUS	0x000000000D0F0029	1953
TP.TPCHIP.NET.PCBSLPCI0.ERROR_REG	0x000000000D0F001F	1950
TP.TPCHIP.NET.PCBSLPCI0.HANG_PULSE_0_REG	0x000000000D0F0020	1951
TP.TPCHIP.NET.PCBSLPCI0.HANG_PULSE_1_REG	0x000000000D0F0021	1951
TP.TPCHIP.NET.PCBSLPCI0.HANG_PULSE_2_REG	0x000000000D0F0022	1951
TP.TPCHIP.NET.PCBSLPCI0.HANG_PULSE_3_REG	0x000000000D0F0023	1952
TP.TPCHIP.NET.PCBSLPCI0.HANG_PULSE_4_REG	0x000000000D0F0024	1952
TP.TPCHIP.NET.PCBSLPCI0.HANG_PULSE_5_REG	0x000000000D0F0025	1952
TP.TPCHIP.NET.PCBSLPCI0.HANG_PULSE_6_REG	0x000000000D0F0026	1953
TP.TPCHIP.NET.PCBSLPCI0.HEARTBEAT_REG	0x000000000D0F0018	1948
TP.TPCHIP.NET.PCBSLPCI0.MULTICAST_GROUP_1	0x000000000D0F0001	1944
TP.TPCHIP.NET.PCBSLPCI0.MULTICAST_GROUP_2	0x000000000D0F0002	1945
TP.TPCHIP.NET.PCBSLPCI0.MULTICAST_GROUP_3	0x000000000D0F0003	1945
TP.TPCHIP.NET.PCBSLPCI0.MULTICAST_GROUP_4	0x000000000D0F0004	1946
TP.TPCHIP.NET.PCBSLPCI0.NET_CTRL0	0x000000000D0F0040	1954
TP.TPCHIP.NET.PCBSLPCI0.NET_CTRL1	0x000000000D0F0044	1955
TP.TPCHIP.NET.PCBSLPCI0.PLL_LOCK_REG	0x000000000D0F0019	1948
TP.TPCHIP.NET.PCBSLPCI0.PRE_COUNTER_REG	0x000000000D0F0028	1953
TP.TPCHIP.NET.PCBSLPCI0.PRIMARY_ADDRESS_REG	0x000000000D0F0000	1944
TP.TPCHIP.NET.PCBSLPCI0.PROTECT_MODE_REG	0x000000000D0F03FE	1957
TP.TPCHIP.NET.PCBSLPCI0.RECOV_INTERRUPT_REG	0x000000000D0F001B	1948
TP.TPCHIP.NET.PCBSLPCI0.SLAVE_CONFIG_REG	0x000000000D0F001E	1949
TP.TPCHIP.NET.PCBSLPCI0.TIMEOUT_REG	0x000000000D0F0010	1947
TP.TPCHIP.NET.PCBSLPCI0.VITAL_SCAN_OUT	0x000000000D0F0017	1947
TP.TPCHIP.NET.PCBSLPCI0.XSTOP_INTERRUPT_REG	0x000000000D0F001C	1949

The POWER9 processor registers are listed in the following tables.

Register Name	Primary PCB Slave Address Register		
Mnemonic	TP.TPCHIP.NET.PCBSLPCI0.PRIMARY_ADDRESS_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D0F0000 (SCOM)	000000000E0F0000 (SCOM)	000000000F0F0000 (SCOM)
Description	This register contains the slave's primary address.		

Bits	SCOM	Field Mnemonic: Description
0:5	RO	Reserved. This is the primary_address setting.

Register Name	Multicast Group 1 Register		
Mnemonic	TP.TPCHIP.NET.PCBSLPCI0.MULTICAST_GROUP_1		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D0F0001 (SCOM)	000000000E0F0001 (SCOM)	000000000F0F0001 (SCOM)
Description	Multicast Group Registers 1 – 4 are used to are used to assign chiplets to a specific multicast group within the pervasive connect bus (PCB). Multicast groups make it possible to address more than a single chiplet at a time. They are used to read or write the same resource in multiple chiplets at the same time. Note: Multicast groups are initially set up at IPL, but they can be modified at any time by firmware or power management code.		

Bits	SCOM	Field Mnemonic: Description
0:2	RO	Constant = 111
3:5	RW	MULTICAST1_GROUP: Multicast group1 setting. Set this field to a multicast group that this chiplet should be a member of. The chiplet can be assigned to up to four multicast groups by setting this field in the four multicast group registers to the corresponding multicast group numbers. If the chiplet is member of less than four multicast groups, set this field to 0b111 in the multicast group register that is not required. The 0b111 setting indicates multicast group 7; all chiplets are members of multicast group 7 regardless of any multicast register being set to 0b111. 000: Multicast group 0. 001: Multicast group 1. 010: Multicast group 2. 011: Multicast group 3. 100: Multicast group 4 – unused. 101: Multicast group 5 – unused. 110: Multicast group 6 – unused. 111: Multicast group 7.

Register Name	Multicast Group 2 Register
Mnemonic	TP.TPCHIP.NET.PCBSLPCI0.MULTICAST_GROUP_2

Address

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D0F0002 (SCOM)	000000000E0F0002 (SCOM)	000000000F0F0002 (SCOM)

Description

Multicast Group Registers 1 – 4 are used to are used to assign chiplets to a specific multicast group within the pervasive connect bus (PCB). Multicast groups make it possible to address more than a single chiplet at a time. They are used to read or write the same resource in multiple chiplets at the same time.
Note: Multicast groups are initially set up at IPL, but they can be modified at any time by firmware or power management code.

Bits	SCOM	Field Mnemonic: Description
0:2	RO	Constant = 111
3:5	RW	MULTICAST2_GROUP: Multicast group2 setting. Set this field to a multicast group that this chiplet should be a member of. The chiplet can be assigned to up to four multicast groups by setting this field in the four multicast group registers to the corresponding multicast group numbers. If the chiplet is member of less than four multicast groups, set this field to 0b111 in the multicast group register that is not required. The 0b111 setting indicates multicast group 7; all chiplets are members of multicast group 7 regardless of any multicast register being set to 0b111. 000: Multicast group 0. 001: Multicast group 1. 010: Multicast group 2. 011: Multicast group 3. 100: Multicast group 4 – unused. 101: Multicast group 5 – unused. 110: Multicast group 6 – unused. 111: Multicast group 7.

Register Name	Multicast Group 3
Mnemonic	TP.TPCHIP.NET.PCBSLPCI0.MULTICAST_GROUP_3

Address

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D0F0003 (SCOM)	000000000E0F0003 (SCOM)	000000000F0F0003 (SCOM)

Description

Multicast Group Registers 1 – 4 are used to are used to assign chiplets to a specific multicast group within the pervasive connect bus (PCB). Multicast groups make it possible to address more than a single chiplet at a time. They are used to read or write the same resource in multiple chiplets at the same time.
Note: Multicast groups are initially set up at IPL, but they can be modified at any time by firmware or power management code.

Bits	SCOM	Field Mnemonic: Description
0:2	RO	Constant = 111

Bits	SCOM	Field Mnemonic: Description
3:5	RW	MULTICAST3_GROUP: Multicast group3 setting. Set this field to a multicast group that this chiplet should be a member of. The chiplet can be assigned to up to four multicast groups by setting this field in the four multicast group registers to the corresponding multicast group numbers. If the chiplet is member of less than four multicast groups, set this field to 0b111 in the multicast group register that is not required. The 0b111 setting indicates multicast group 7; all chiplets are members of multicast group 7 regardless of any multicast register being set to 0b111. 000: Multicast group 0. 001: Multicast group 1. 010: Multicast group 2. 011: Multicast group 3. 100: Multicast group 4 – unused. 101: Multicast group 5 – unused. 110: Multicast group 6 – unused. 111: Multicast group 7.

Register Name	Multicast Group 4 Register
Mnemonic	TP.TPCHIP.NET.PCBSLPCI0.MULTICAST_GROUP_4
Address	PCI0 (PE0): 000000000D0F0004 (SCOM) PCI1 (PE1): 000000000E0F0004 (SCOM) PCI2 (PE2): 000000000F0F0004 (SCOM)
Description	Multicast Group Registers 1 – 4 are used to are used to assign chiplets to a specific multicast group within the pervasive connect bus (PCB). Multicast groups make it possible to address more than a single chiplet at a time. They are used to read or write the same resource in multiple chiplets at the same time. Note: Multicast groups are initially set up at IPL, but they can be modified at any time by firmware or power management code.

Bits	SCOM	Field Mnemonic: Description
0:2	RO	Constant = 111
3:5	RW	MULTICAST4_GROUP: Multicast group4 setting. Set this field to a multicast group that this chiplet should be a member of. The chiplet can be assigned to up to four multicast groups by setting this field in the four multicast group registers to the corresponding multicast group numbers. If the chiplet is member of less than four multicast groups, set this field to 0b111 in the multicast group register that is not required. The 0b111 setting indicates multicast group 7; all chiplets are members of multicast group 7 regardless of any multicast register being set to 0b111. 000: Multicast group 0. 001: Multicast group 1. 010: Multicast group 2. 011: Multicast group 3. 100: Multicast group 4 – unused. 101: Multicast group 5 – unused. 110: Multicast group 6 – unused. 111: Multicast group 7.

Register Name	Timeout Select Register		
Mnemonic	TP.TPCHIP.NET.PCBSLPCI0.TIMEOUT_REG		
Address	PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
	000000000D0F0010 (SCOM)	000000000E0F0010 (SCOM)	000000000F0F0010 (SCOM)
Description	This register contains the int_timeout setting.		

Bits	SCOM	Field Mnemonic: Description
0:1	RW	Reserved. This is the int_timeout setting.

Register Name	Assist Interrupt Register		
Mnemonic	TP.TPCHIP.NET.PCBSLPCI0.ASSIST_INTERRUPT_REG		
Address	PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
	000000000D0F0011 (SCOM)	000000000E0F0011 (SCOM)	000000000F0F0011 (SCOM)
Description	This register contains the attn, recov, and xstop (checkstop) settings.		

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved. This is the attn setting.
1	ROX	Reserved. This is the recov setting.
2	ROX	Reserved. This is the xstop setting.

Register Name	Vital Scan Out Register		
Mnemonic	TP.TPCHIP.NET.PCBSLPCI0.VITAL_SCAN_OUT		
Address	PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
	000000000D0F0017 (SCOM)	000000000E0F0017 (SCOM)	000000000F0F0017 (SCOM)
Description	This register contains the vital scan out settings.		

Bits	SCOM	Field Mnemonic: Description
0	ROX	RESERVED.

Register Name	Chiplet Heartbeat Register
Mnemonic	TP.TPCHIP.NET.PCBSLPCI0.HEARTBEAT_REG
Address	

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D0F0018 (SCOM)	000000000E0F0018 (SCOM)	000000000F0F0018 (SCOM)

Description	This register indicates whether a chiplet heartbeat is detected.

Bits	SCOM	Field Mnemonic: Description
0	ROX	HEARTBEAT_DEAD: A chiplet heartbeat is not detected.

Register Name	PLL Lock indications Register
Mnemonic	TP.TPCHIP.NET.PCBSLPCI0.PLL_LOCK_REG
Address	

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D0F0019 (SCOM)	000000000E0F0019 (SCOM)	000000000F0F0019 (SCOM)

Description	This register contains lock indications from the PLLs,

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	Reserved field.. This is the lock setting.

Register Name	Attention Interrupt Register
Mnemonic	TP.TPCHIP.NET.PCBSLPCI0.ATTN_INTERRUPT_REG
Address	

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D0F001A (SCOM)	000000000E0F001A (SCOM)	000000000F0F001A (SCOM)

Description	This register contains the attn setting.

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved. This is the attn setting.

Register Name	Recovery Interrupt Register
Mnemonic	TP.TPCHIP.NET.PCBSLPCI0.RECOV_INTERRUPT_REG
Address	

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D0F001B (SCOM)	000000000E0F001B (SCOM)	000000000F0F001B (SCOM)

Description	This register contains the recoverable interrupt setting.

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. This is the recov setting.

Register Name	Checkstop Interrupt Register
Mnemonic	TP.TPCHIP.NET.PCBSLPCI0.XSTOP_INTERRUPT_REG
Address	PCI0 (PE0): 000000000D0F001C (SCOM) PCI1 (PE1): 000000000E0F001C (SCOM) PCI2 (PE2): 000000000F0F001C (SCOM)
Description	This register contains the checkstop interrupt setting.

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. This is the checkstop setting.

Register Name	Slave Configuration Register
Mnemonic	TP.TPCHIP.NET.PCBSLPCI0.SLAVE_CONFIG_REG
Address	PCI0 (PE0): 000000000D0F001E (SCOM) PCI1 (PE1): 000000000E0F001E (SCOM) PCI2 (PE2): 000000000F0F001E (SCOM)
Description	This is the slave configuration register.

Bits	SCOM	Field Mnemonic: Description
0	RW	CFG_DISABLE_PERV_THOLD_CHECK: This bit disables the pervasive threshold check.
1	RW	CFG_DISABLE_MALF_PULSE_GEN: This bit disables pulse generation for a malfunction alert. Switch back to level.
2	RW	CFG_STOP_HANG_CNT_SYS_XSTP: This bit disables the hang counter stop for a system checkstop.
3	RW	CFG_DISABLE_CL_ATOMIC_LOCK: This bit disables the atomic lock for chiplet accesses.
4	RW	CFG_DISABLE_HEARTBEAT: This bit disables the check for voltage and gridclock in the chiplet.
5	RW	CFG_DISABLE_FORCE_TO_ZERO: This bit disables the force to zero for error cases.
6	RW	CFG_PM_DISABLE: This bit disables the power management set/reset interface for net_ctrl registers.
7	RW	CFG_PM_MUX_DISABLE: This bit disables the power-management multiplex request signal.
8:13	RW	ERROR_MASK: These are mask bits for slave error reporting.
14:15	RW	RESERVED.

Register Name	**Error Capture Register**
Mnemonic	TP.TPCHIP.NET.PCBSLPCI0.ERROR_REG
Address	**PCI0 (PE0)**: 000000000D0F001F (SCOM) **PCI1 (PE1)**: 000000000E0F001F (SCOM) **PCI2 (PE2)**: 000000000F0F001F (SCOM)
Description	This register is used to capture errors.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	CE_ERROR: Correctable error on the PCB bus.
1:3	RWX_WCLEAR	CHIPLET_ERRORS: Errors reported by the chiplet. 000 = No error. 001 = XSCOM command blocked due to pending errors. 010 = Chiplet offline. 011 = Partial good. 100 = Invalid address, address error, or bad access type. 101 = Clock error. 110 = Parity error, received unexpected packet, or wrong packet number. 111 = Timeout. This register is for debug purposes only. It only holds meaningful data if it is cleared after each error.
4	RWX_WCLEAR	PARITY_ERROR: Parity error on the PCB interface.
5	RWX_WCLEAR	DATA_BUFFER_ERROR: Parity error in the data buffer.
6	RWX_WCLEAR	ADDR_BUFFER_ERROR: Parity error in the address buffer.
7	RWX_WCLEAR	PCB_FSM_ERROR: Invalid state error in the PCB FSM.
8	RWX_WCLEAR	CL_FSM_ERROR: Invalid state error in the chiplet FSM.
9	RWX_WCLEAR	INT_RX_FSM_ERROR: Invalid state error in the interrupt RX FSM.
10	RWX_WCLEAR	INT_TX_FSM_ERROR: Invalid state error in the interrupt TX FSM.
11	RWX_WCLEAR	INT_TYPE_ERROR: Invalid interrupt type.
12	RWX_WCLEAR	CL_DATA_ERROR: Parity error on the chiplet interface.
13	RWX_WCLEAR	INFO_ERROR: Parity error on the chiplet information lines.
14	RWX_WCLEAR	UNUSED_0:
15	RWX_WCLEAR	CHIPLET_ATOMIC_LOCK_ERROR: Chiplet atomic lock error.
16	RWX_WCLEAR	PCB_INTERFACE_ERROR: Error on the PCB interface component for the internal endpoint.
17	RWX_WCLEAR	CHIPLET_OFFLINE: A heartbeat check indicated that the chiplet is offline.
18	RWX_WCLEAR	EDRAM_SEQUENCE_ERR: Error in the eDRAM power-up sequence.
19	RWX_WCLEAR	CTRL_REG_PARITY_ERROR: The control register parity is bad.
20	RWX_WCLEAR	ADDRESS_REG_PARITY_ERROR: The address register parity is bad.
21	RWX_WCLEAR	TIMEOUT_REG_PARITY_ERROR: The timeout select register parity is bad.
22	RWX_WCLEAR	CONFIG_REG_PARITY_ERROR: The slave configuration register parity is bad.
23	RWX_WCLEAR	UNUSED_1:
24	RWX_WCLEAR	DIV_REG_PARITY_ERROR: The divider register parity is bad.
25:28	RWX_WCLEAR	PLL_UNLOCK_ERROR: Unlock from the chiplet PLL.

Register Name	Hang Pulse Generation Register 0		
Mnemonic	TP.TPCHIP.NET.PCBSLPCI0.HANG_PULSE_0_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D0F0020 (SCOM)	000000000E0F0020 (SCOM)	000000000F0F0020 (SCOM)
Description	This register contains hang pulse 0 information.		

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_0: This field contains the value of hang pulse 0. The time period equals 2value x (precounter_reg + 1) / pcb_freq. The range of valid values is 34 – 0.
6	RW	SUPPRESS_HANG_0: If set to '1', hang pulses are suppressed in case of a checkstop.

Register Name	Hang Pulse Generation Register 1		
Mnemonic	TP.TPCHIP.NET.PCBSLPCI0.HANG_PULSE_1_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D0F0021 (SCOM)	000000000E0F0021 (SCOM)	000000000F0F0021 (SCOM)
Description	This register contains hang pulse 1 information.		

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_1: This field contains the value of hang pulse 1. The time period equals 2value x (precounter_reg + 1) / pcb_freq. The range of valid values is 34 – 0.
6	RW	SUPPRESS_HANG_1: If set to '1', hang pulses are suppressed in case of a checkstop.

Register Name	Hang Pulse Generation Register 2		
Mnemonic	TP.TPCHIP.NET.PCBSLPCI0.HANG_PULSE_2_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D0F0022 (SCOM)	000000000E0F0022 (SCOM)	000000000F0F0022 (SCOM)
Description	This register contains hang pulse 2 information.		

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_2: This field contains the value of hang pulse 2. The time period equals 2value x (precounter_reg + 1) / pcb_freq. The range of valid values is 34 – 0.
6	RW	SUPPRESS_HANG_2: If set to '1', hang pulses are suppressed in case of a checkstop.

Register Name	Hang Pulse Generation Register 3		
Mnemonic	TP.TPCHIP.NET.PCBSLPCI0.HANG_PULSE_3_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D0F0023 (SCOM)	000000000E0F0023 (SCOM)	000000000F0F0023 (SCOM)
Description	This register contains hang pulse 3 information.		

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_3: This field contains the value of hang pulse 3. The time period equals 2value x (precounter_reg + 1) / pcb_freq. The range of valid values is 34 – 0.
6	RW	SUPPRESS_HANG_3: If set to '1', hang pulses are suppressed in case of a checkstop.

Register Name	Hang Pulse Generation Register 4		
Mnemonic	TP.TPCHIP.NET.PCBSLPCI0.HANG_PULSE_4_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D0F0024 (SCOM)	000000000E0F0024 (SCOM)	000000000F0F0024 (SCOM)
Description	This register contains hang pulse 4 information.		

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_4: This field contains the value of hang pulse 4. The time period equals 2value x (precounter_reg + 1) / pcb_freq. The range of valid values is 34 – 0.
6	RW	SUPPRESS_HANG_4: If set to '1', hang pulses are suppressed in case of a checkstop.

Register Name	Hang Pulse Generation Register 5		
Mnemonic	TP.TPCHIP.NET.PCBSLPCI0.HANG_PULSE_5_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D0F0025 (SCOM)	000000000E0F0025 (SCOM)	000000000F0F0025 (SCOM)
Description	This register contains hang pulse 5 information. This hang counter is exclusively used to generate the malfunction alert pulse.		

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_5: This field contains the value of hang pulse 5. The time period equals 2value x (precounter_reg + 1) / pcb_freq. The range of valid values is 34 – 0.
6	RW	SUPPRESS_HANG_5: If set to '1', hang pulses are suppressed in case of a checkstop.

Register Name	Hang Pulse Generation Register 6		
Mnemonic	TP.TPCHIP.NET.PCBSLPCI0.HANG_PULSE_6_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D0F0026 (SCOM)	000000000E0F0026 (SCOM)	000000000F0F0026 (SCOM)
Description	This register contains hang pulse 6 information. This hang counter is exclusively used for heartbeat generation.		

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_6: This field contains the value of hang pulse 6. The time period equals 2value x (precounter_reg + 1) / pcb_freq. The range of valid values is 34 – 0.
6	RW	SUPPRESS_HANG_6: If set to '1', hang pulses are suppressed in case of a checkstop.

Register Name	Hang Counter Clock Divider Register		
Mnemonic	TP.TPCHIP.NET.PCBSLPCI0.PRE_COUNTER_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D0F0028 (SCOM)	000000000E0F0028 (SCOM)	000000000F0F0028 (SCOM)
Description	This register is the divider for the hang counter clock.		

Bits	SCOM	Field Mnemonic: Description
0:7	RW	PRE_COUNTER: This field is the divider for the hang counter clock. It divides the clock by n + 1. (The default is n = 0).

Register Name	eDRAM Control Status Register		
Mnemonic	TP.TPCHIP.NET.PCBSLPCI0.EDRAM_STATUS		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D0F0029 (SCOM)	000000000E0F0029 (SCOM)	000000000F0F0029 (SCOM)
Description	This register contains the eDRAM control status.		

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	EDRAM_STAT: This field contains the eDRAM control status.

Register Name	NET CTRL0 Register (NA in PERV CPLT)
Mnemonic	TP.TPCHIP.NET.PCBSLPCI0.NET_CTRL0
Address	

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
000000000D0F0040 (SCOM) 000000000D0F0041 (SCOM1) 000000000D0F0042 (SCOM2)	000000000E0F0040 (SCOM) 000000000E0F0041 (SCOM1) 000000000E0F0042 (SCOM2)	000000000F0F0040 (SCOM) 000000000F0F0041 (SCOM1) 000000000F0F0042 (SCOM2)

Description	NET CTRL0 Register (NA in PERV CPLT)

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	CHIPLET_ENABLE: This bit is set if the chiplet is good.
1	RWX	RWX_WAND	RWX_WOR	PCB_EP_RESET: The output is ORed to the global EP reset.
2	RWX	RWX_WAND	RWX_WOR	CLK_ASYNC_RESET: POWER9 cache chiplet: EQ skew adjust reset. POWER9 core chiplet: Core duty cycle adjust reset. POWER9 memory chiplet: Memory glitchless multiplexer asynchronous reset.
3	RWX	RWX_WAND	RWX_WOR	PLL_TEST_EN: Test enable for the chiplet PLL.
4	RWX	RWX_WAND	RWX_WOR	PLL_RESET: Reset for the chiplet PLL.
5	RWX	RWX_WAND	RWX_WOR	PLL_BYPASS: Enable bypass for chiplet PLL.
6	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN: Scan control for chiplet vital domain.
7	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN_IN: Scan in for the chiplet vital domain.
8	RWX	RWX_WAND	RWX_WOR	VITAL_PHASE: Phase for vital domain.
9	RWX	RWX_WAND	RWX_WOR	FLUSH_ALIGN_OVR: When set to 1, this mechanism overrides automatic control by the clock controller of the flush, flush_nto1, and align signals in the chiplet.
10	RWX	RWX_WAND	RWX_WOR	VITAL_AL: Align for vital domain.
11	RWX	RWX_WAND	RWX_WOR	ACT_DIS: ACT disable control for LCBs in the vital logic.
12	RWX	RWX_WAND	RWX_WOR	MPW1: Modify pulse width 1 (MPW1) control for LCBs in the vital logic.
13	RWX	RWX_WAND	RWX_WOR	MPW2: Modify pulse width 2 (MPW2) control for LCBs in the vital logic.
14	RWX	RWX_WAND	RWX_WOR	MPW3: Modify pulse width 3 (MPW3) control for LCBs in the vital logic.
15	RWX	RWX_WAND	RWX_WOR	DELAY_LCLKR: LCB control signal for the vital logic.
16	RWX	RWX_WAND	RWX_WOR	VITAL_THOLD: Threshold for the chiplet vital domain.
17	RWX	RWX_WAND	RWX_WOR	FLUSH_SCAN_N: Flush scan control.
18	RWX	RWX_WAND	RWX_WOR	FENCE_EN: Fencing signal for the chiplet.
19	RWX	RWX_WAND	RWX_WOR	CPLT_RCTRL: Chiplet receiver enable.
20	RWX	RWX_WAND	RWX_WOR	CPLT_DCTRL: Chiplet driver enable.
21	RWX	RWX_WAND	RWX_WOR	Reserved. This is the pm_access setting.
22	RWX	RWX_WAND	RWX_WOR	ADJ_FUNC_CLKSEL: POWER9 cache chiplet: Clock select for the skew adjust/duty cycle adjust logic. POWER9 core chiplet: Skew sense to skew adjust fencing.
23:24	RWX	RWX_WAND	RWX_WOR	Reserved. This is the pm_access setting.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
25	RWX	RWX_WAND	RWX_WOR	TP_FENCE_PCB: Fence the chiplet from the PCB bus. If set, the PCB slave reports “Chiplet Offline.”
26	RWX	RWX_WAND	RWX_WOR	LVLTRANS_FENCE: Fence control for the level translators.
27	RWX	RWX_WAND	RWX_WOR	ARRAY_WRITE_ASSIST_EN: Array write assist.
28	RWX	RWX_WAND	RWX_WOR	HTB_INTEST: HTB intest mode.
29	RWX	RWX_WAND	RWX_WOR	HTB_EXTEST: HTB intest mode.
30	RWX	RWX_WAND	RWX_WOR	Reserved. This is the pm_access setting.
31	RWX	RWX_WAND	RWX_WOR	PLLFORCE_OUT_EN: PLL force out enable.

Register Name	NET CTRL1 Register (NA in PERV CPLT)
Mnemonic	TP.TPCHIP.NET.PCBSLPCI0.NET_CTRL1
Address	<table><tr><th>PCI0 (PE0)</th><th>PCI1 (PE1)</th><th>PCI2 (PE2)</th></tr><tr><td>000000000D0F0044 (SCOM) 000000000D0F0045 (SCOM1) 000000000D0F0046 (SCOM2)</td><td>000000000E0F0044 (SCOM) 000000000E0F0045 (SCOM1) 000000000E0F0046 (SCOM2)</td><td>000000000F0F0044 (SCOM) 000000000F0F0045 (SCOM1) 000000000F0F0046 (SCOM2)</td></tr></table>
Description	NET CTRL1 Register (NA in PERV CPLT)

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	PLL_CLKIN_SEL: PLL clkin select. POWER9 Memory chiplet (mux3): Selects the reference clock source for the DDR reference clock. 0 = SSCG enabled, 1 = SSCG disabled. POWER9 XBus chiplet (mux8): Selects the reference clock source for the Xbus PLLs. 0 = SSCG enabled. 1 = SSCG disabled. POWER9 PCIe chiplet (PCI0 = mux5, PCI2 = mux4): Selects the reference clock source for the PCIe PHY E2 (PCI2), PCIe PHY E0 and E2 (PCI0). 0 = SSCG enabled. 1 = SSCG disabled. POWER9 OBus chiplet (OB0 = mux6, OB3 = mux7): Selects the reference clock source for the combo PHY 0 (OB0) and PHY 3 (OB3). 0 = NVLink. 1 = Optics.
1	RWX	RWX_WAND	RWX_WOR	CLK_DCC_BYPASS_EN: POWER9 cache chiplet: L2-0, L2-1, L3 duty cycle control bypass. POWER9 core chiplet: Core duty cycle control bypass. POWER9 memory chiplet: Memory duty cycle control bypass.
2	RWX	RWX_WAND	RWX_WOR	CLK_PDLY_BYPASS_EN: POWER9 cache chiplet: L2-0, L2-1, L3 programmable delay bypass. POWER9 core chiplet: Core programmable delay bypass. POWER9 memory chiplet: Memory programmable delay bypass.
3	RWX	RWX_WAND	RWX_WOR	CLK_DIV_BYPASS_EN: Enable clock divider bypass.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
4	RWX	RWX_WAND	RWX_WOR	REFCLK_CLKMUX0_SEL: Selects the reference clock input. POWER9 OB0 chiplet (mux13): Selects the reference clock source for the Optics 156.25 MHz reference clock. 0 = SSCG enabled. 1 = SSCG disabled, POWER9 OB3 chiplet (mux9): Selects the reference clock source for the NVLink 133 1/3 MHz reference clock. 0 = SSCG enabled. 1 = SSCG disabled. POWER9 PCI0 chiplet (mux10): Selects the 100 MHz SSCG reference clock source for the PCIe PHYs. 0 = CP Filter PLL 2. 1 = SSCG PLL 1.
5	RWX	RWX_WAND	RWX_WOR	REFCLK_CLKMUX1_SEL: Selects the reference clock input. POWER9 OB0 chiplet (mux15): Selects the reference clock source for the NVLink reference clock. 0 = 133 1/3 MHz. 1 = 156.25 MHz. POWER9 OB3 chiplet (mux14): Selects the reference clock source for NVLink 156.25 MHz reference clock. 0 = SSCG enabled. 1 = SSCG disabled. POWER9 PCI0 chiplet (mux11): Selects 100 MHz non-SSCG reference clock source for PCIe PHYs. 0 = I/O filter PLL 3. 1 = Unfiltered.
6	RWX	RWX_WAND	RWX_WOR	PLL_BNDY_BYPASS_EN: Bypass for IOP PLL.
7	RWX	RWX_WAND	RWX_WOR	Reserved. This is the pcb_access setting.
8:15	RWX	RWX_WAND	RWX_WOR	DPLL_TEST_SEL: DPLL testout multiplexing.
16:19	RWX	RWX_WAND	RWX_WOR	SB_STRENGTH: Sector buffer driver strength.
20	RWX	RWX_WAND	RWX_WOR	ASYNC_TYPE: This is a control signal for testing latches with asynchronous set and reset capabilities.
21	RWX	RWX_WAND	RWX_WOR	ASYNC_OBS: This is a control signal for testing latches with asynchronous set and reset capabilities.
22	RWX	RWX_WAND	RWX_WOR	CPM_CAL_SET: CPM calibrate.
23	RWX	RWX_WAND	RWX_WOR	SENSEADJ_RESET0: POWER9 cache chiplet: L2-0 duty cycle adjust reset.
24	RWX	RWX_WAND	RWX_WOR	SENSEADJ_RESET1: POWER9 cache chiplet: L2-1 duty cycle adjust reset.
25	RWX	RWX_WAND	RWX_WOR	CLK_PULSE_EN: Clock pulse mode enable.
26:27	RWX	RWX_WAND	RWX_WOR	CLK_PULSE_MODE: Clock pulse mode setting.
28:31	RWX	RWX_WAND	RWX_WOR	Reserved. This is the pcb_access setting.

Register Name	Protect Mode Register		
Mnemonic	TP.TPCHIP.NET.PCBSLPCI0.PROTECT_MODE_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D0F03FE (SCOM)	000000000E0F03FE (SCOM)	000000000F0F03FE (SCOM)
Description	This register is used to enable read and write protection.		

Bits	SCOM	Field Mnemonic: Description
0	RW	READ_PROTECT_ENABLE: Enable read protection.
1	RW	WRITE_PROTECT_ENABLE: Enable write protection.

Register Name	Atomic Lock Register		
Mnemonic	TP.TPCHIP.NET.PCBSLPCI0.ATOMIC_LOCK_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
	000000000D0F03FF (SCOM)	000000000E0F03FF (SCOM)	000000000F0F03FF (SCOM)
Description	This register contains atomic lock information.		

Bits	SCOM	Field Mnemonic: Description
0	RW	ATOMIC_LOCK_ENABLE: Enable the atomic lock.
1:4	ROX	ATOMIC_ID: This field contains the atomic ID.
5:7	RO	constant = 0b000
8:15	ROX	ATOMIC_ACTIVITY: This is the atomic lock counter.

10. PCI 1 and PCI 2 Chiplet

The POWER9 processor registers are listed alphabetically by mnemonic in the following address table.

Mnemonic	Address	Page
PE1.PHB2.ETUX08.RSB.RSB.REGS.ACT0_REG	0x000000000E01094E	1965
PE1.PHB2.ETUX08.RSB.RSB.REGS.ACTION1_REG	0x000000000E01094F	1967
PE1.PHB2.ETUX08.RSB.RSB.REGS.FIR_REG	0x000000000E010948	1960
PE1.PHB2.ETUX08.RSB.RSB.REGS.MASK_REG	0x000000000E01094B	1963
PE1.PHB2.ETUX08.RSB.RSB.REGS.PERF_CFG_REG	0x000000000E010957	1971
PE1.PHB2.ETUX08.RSB.RSB.REGS.PERF_CNT0_REG	0x000000000E010958	1971
PE1.PHB2.ETUX08.RSB.RSB.REGS.PERF_CNT1_REG	0x000000000E010959	1972
PE1.PHB2.ETUX08.RSB.RSB.REGS.PERF_CNT2_REG	0x000000000E01095A	1972
PE1.PHB2.ETUX08.RSB.RSB.REGS.PERF_CNT3_REG	0x000000000E01095B	1972
PE1.PHB2.ETUX08.RSB.RSB.REGS.WOF_REG	0x000000000E010950	1969
PE1.PHB2.ETUX08.RSB.RSB.SCOM.SSR.PHB4_SCOM_HVIAR	0x000000000E010940	1958
PE1.PHB2.ETUX08.RSB.RSB.SCOM.SSR.PHB4_SCOM_HVIDR	0x000000000E010941	1959
PE1.PHB2.ETUX08.RSB.RSB.SCOM.SSR.PHB4_SCOM_HVIDWR	0x000000000E010941	1959

Mnemonic	Address	Page
PE1.PHB2.ETUX08.RSB.RSB.SCOM.SSR.PHB4_SCOM_UVIAR	0x000000000E010942	1959
PE1.PHB2.ETUX08.RSB.RSB.SCOM.SSR.PHB4_SCOM_UVIDR	0x000000000E010943	1960
PE1.PHB2.ETUX08.RSB.RSB.SCOM.SSR.PHB4_SCOM_UVIDWR	0x000000000E010943	1960
PE2.PHB5.ETUX08.RSB.RSB.REGS.ACT0_REG	0x000000000F01098E	1979
PE2.PHB5.ETUX08.RSB.RSB.REGS.ACTION1_REG	0x000000000F01098F	1981
PE2.PHB5.ETUX08.RSB.RSB.REGS.FIR_REG	0x000000000F010988	1975
PE2.PHB5.ETUX08.RSB.RSB.REGS.MASK_REG	0x000000000F01098B	1977
PE2.PHB5.ETUX08.RSB.RSB.REGS.PERF_CFG_REG	0x000000000F010997	1985
PE2.PHB5.ETUX08.RSB.RSB.REGS.PERF_CNT0_REG	0x000000000F010998	1986
PE2.PHB5.ETUX08.RSB.RSB.REGS.PERF_CNT1_REG	0x000000000F010999	1986
PE2.PHB5.ETUX08.RSB.RSB.REGS.PERF_CNT2_REG	0x000000000F01099A	1986
PE2.PHB5.ETUX08.RSB.RSB.REGS.PERF_CNT3_REG	0x000000000F01099B	1987
PE2.PHB5.ETUX08.RSB.RSB.REGS.WOF_REG	0x000000000F010990	1983
PE2.PHB5.ETUX08.RSB.RSB.SCOM.SSR.PHB4_SCOM_HVIAR	0x000000000F010980	1973
PE2.PHB5.ETUX08.RSB.RSB.SCOM.SSR.PHB4_SCOM_HVIDR	0x000000000F010981	1973
PE2.PHB5.ETUX08.RSB.RSB.SCOM.SSR.PHB4_SCOM_HVIDWR	0x000000000F010981	1973
PE2.PHB5.ETUX08.RSB.RSB.SCOM.SSR.PHB4_SCOM_UVIAR	0x000000000F010982	1974
PE2.PHB5.ETUX08.RSB.RSB.SCOM.SSR.PHB4_SCOM_UVIDR	0x000000000F010983	1974
PE2.PHB5.ETUX08.RSB.RSB.SCOM.SSR.PHB4_SCOM_UVIDWR	0x000000000F010983	1974

Register Name	**PHB4 SCOM HV Indirect Address Register**		
Mnemonic	PE1.PHB2.ETUX08.RSB.RSB.SCOM.SSR.PHB4_SCOM_HVIAR		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
		000000000E010940 (SCOM)	000000000F010940 (SCOM)
Description	This register contains the PHB4 SCOM HV request indirect address value.		

Bits	SCOM	Field Mnemonic: Description
0	RW	HV_REQ_ADDR_VLD: SCOM HV request valid.
1	RW	HV_REQ_4B: SCOM HV request 4B access.
2	RW	HV_AUTO_INC: SCOM HV request address auto increment.
3:50	RO	Constant = 0b000000000000000000000000000000000000000000000000
51:61	RW	HV_REQ_ADDR_VALUE: SCOM HV request indirect address value.
62:63	RO	Constant = 0b00

Register Name	PHB4 SCOM HV Indirect Address Register Read Port		
Mnemonic	PE1.PHB2.ETUX08.RSB.RSB.SCOM.SSR.PHB4_SCOM_HVIDR		
Address	PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
		000000000E010941 (SCOM)	000000000F010941 (SCOM)
Description	PHB4 SCOM HV Indirect Address Register Read Port		

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	scom_hv_req_read_data.

Register Name	PHB4 SCOM HV Indirect Address Register Write Port		
Mnemonic	PE1.PHB2.ETUX08.RSB.RSB.SCOM.SSR.PHB4_SCOM_HVIDWR		
Address	PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
		000000000E010941 (SCOM)	000000000F010941 (SCOM)
Description	PHB4 SCOM HV Indirect Address Register Write Port		

Bits	SCOM	Field Mnemonic: Description
0:63	WOX	scom_hv_req_write_data.

Register Name	PHB4 SCOM HV Indirect Address Register		
Mnemonic	PE1.PHB2.ETUX08.RSB.RSB.SCOM.SSR.PHB4_SCOM_UVIAR		
Address	PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
		000000000E010942 (SCOM)	000000000F010942 (SCOM)
Description	PHB4 SCOM HV Indirect Address Register		

Bits	SCOM	Field Mnemonic: Description
0	RW	UV_REQ_ADDR_VLD: SCOM UV request valid.
1	RO	Constant = 0b0
2	RW	UV_AUTO_INC: SCOM UV request address auto increment.
3:51	RO	Constant = 0b0000000000000000000000000000000000000000000000000
52:60	RW	UV_REQ_ADDR_VALUE: SCOM UV request indirect address value.
61:63	RO	Constant = 0b000

Register Name	PHB4 SCOM UV Indirect Address Register Read Port		
Mnemonic	PE1.PHB2.ETUX08.RSB.RSB.SCOM.SSR.PHB4_SCOM_UVIDR		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
		000000000E010943 (SCOM)	000000000F010943 (SCOM)
Description	PHB4 SCOM UV Indirect Address Register Read Port		

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	scom_uv_req_read_data.

Register Name	PHB4 SCOM UV Indirect Address Register Write Port		
Mnemonic	PE1.PHB2.ETUX08.RSB.RSB.SCOM.SSR.PHB4_SCOM_UVIDWR		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
		000000000E010943 (SCOM)	000000000F010943 (SCOM)
Description	PHB4 SCOM UV Indirect Address Register Write Port		

Bits	SCOM	Field Mnemonic: Description
0:63	WOX	scom_uv_req_write_data.

Register Name	ETU FIR Register		
Mnemonic	PE1.PHB2.ETUX08.RSB.RSB.REGS.FIR_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
		000000000E010948 (SCOM) 000000000E010949 (SCOM1) 000000000E01094A (SCOM2)	000000000F010948 (SCOM) 000000000F010949 (SCOM1) 000000000F01094A (SCOM2)
Description	ETU FIR Register		

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	AIB_COMMAND_INVALID: See Outbound Error Status Register, bit 0 for details.
1	RWX	WOX_AND	WOX_OR	AIB_ADDRESS_INVALID: See Outbound Error Status Register, bit 1/2 for details.
2	RWX	WOX_AND	WOX_OR	AIB_ACCESS_ERROR: See Outbound Error Status Register, bit 3/8 for details.
3	RWX	WOX_AND	WOX_OR	PAPR_OUTBOUND_INJECT_ERROR: See Outbound Error Status Register, bit 28 for details.
4	RWX	WOX_AND	WOX_OR	AIB_FATAL_CLASS_ERROR: See Outbound Error Status Register, bit 4/5/9/10/11/14/15 for details.
5	RWX	WOX_AND	WOX_OR	AIB_INF_Class_Error.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
6	RWX	WOX_AND	WOX_OR	AIB_INF_CLASS_ERROR: See Outbound Error Status Register, bit 6 for details.
7	RWX	WOX_AND	WOX_OR	PE_STOP_STATE_SIGNALED: See Outbound Error Status Register, bit 13/22 for details.
8	RWX	WOX_AND	WOX_OR	OUT_COMMON_ARRAY_FATAL_ERROR: See Outbound Error Status Register, bit 23/37/38/40/43/44/45/47/48/49 for details.
9	RWX	WOX_AND	WOX_OR	OUT_COMMON_LATCH_FATAL_ERROR: See Outbound Error Status Register, bit 50/51/52 for details.
10	RWX	WOX_AND	WOX_OR	OUT_COMMON_LOGIC_FATAL_ERROR: See Outbound Error Status Register, bit 19/20/21/53/54/55 for details.
11	RWX	WOX_AND	WOX_OR	BLIF_OUT_INTERFACE_PARITY_ERROR: See Outbound Error Status Register, bit 16 for details.
12	RWX	WOX_AND	WOX_OR	CFG_WRITE_CA_OR_UR_RESPONSE: See Outbound Error Status Register, bit 17 for details.
13	RWX	WOX_AND	WOX_OR	MMIO_REQUEST_TIMEOUT: See Outbound Error Status Register, bit 18 for details.
14	RWX	WOX_AND	WOX_OR	OUT_RRB_SOURCED_ERROR: See Outbound Error Status Register, bit 56/57 for details.
15	RWX	WOX_AND	WOX_OR	CFG_LOGIC_SIGNALED_ERROR: See Outbound Error Status Register, bit 17 for details.
16	RWX	WOX_AND	WOX_OR	RSB_REG_REQUEST_ADDRESS_ERROR: See RSB Error Status Register, bit 00 for details.
17	RWX	WOX_AND	WOX_OR	RSB_FDA_FATAL_ERROR: See RSB Error Status Register, bit 2/3/5 for details.
18	RWX	WOX_AND	WOX_OR	RSB_FDA_INF_ERROR: See RSB Error Status Register, bit 1/4 for details.
19	RWX	WOX_AND	WOX_OR	RSB_FDB_FATAL_ERROR: See RSB Error Status Register, bit 9/10 for details.
20	RWX	WOX_AND	WOX_OR	RSB_FDB_INF_ERROR: See RSB Error Status Register, bit 8 for details.
21	RWX	WOX_AND	WOX_OR	RSB_ERR_FATAL_ERROR: See RSB Error Status Register, bit 7 for details.
22	RWX	WOX_AND	WOX_OR	RSB_ERR_INF_ERROR: See RSB Error Status Register, bit 6 for details.
23	RWX	WOX_AND	WOX_OR	RSB_DBG_FATAL_ERROR: See RSB Error Status Register, bit 13/14 for details.
24	RWX	WOX_AND	WOX_OR	RSB_DBG_INF_ERROR: See RSB Error Status Register, bit 12 for details.
25	RWX	WOX_AND	WOX_OR	PCIE_REQUEST_ACCESS_ERROR: See Outbound Error Status Register, bit 11 for details.
26	RWX	WOX_AND	WOX_OR	RSB_BUS_LOGIC_ERROR: See Outbound Error Status Register, bit 15/27 for details.
27	RWX	WOX_AND	WOX_OR	RSB_UVI_FATAL_ERROR: See RSB Error Status Register, bit 17/19 for details.
28	RWX	WOX_AND	WOX_OR	RSB_UVI_INF_ERROR: See RSB Error Status Register, bit 16/18 for details.
29	RWX	WOX_AND	WOX_OR	SCOM_FATAL_ERROR: See RSB Error Status Register, bit 30/31 for details.
30	RWX	WOX_AND	WOX_OR	SCOM_INF_ERROR: See RSB Error Status Register, bit 28/29 for details.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
31	RWX	WOX_AND	WOX_OR	PCIE_MACRO_ERROR_ACTIVE_STATUS: See RSB Error Status Register, bit 24/25/26 for details.
32	RWX	WOX_AND	WOX_OR	ARB_IODA_FATAL_ERROR: See ARB Error Status Register, bit 33 for details.
33	RWX	WOX_AND	WOX_OR	ARB_MSI_PE_MATCH_ERROR: See ARB Error Status Register, bit 27 for details.
34	RWX	WOX_AND	WOX_OR	ARB_MSI_ADDRESS_ERROR: See ARB Error Status Register, bit 02/03 for details.
35	RWX	WOX_AND	WOX_OR	ARB_TVT_ERROR: See ARB Error Status Register, bit 26/28 for details.
36	RWX	WOX_AND	WOX_OR	ARB_RCVD_FATAL_ERROR_MSG: See ARB Error Status Register, bit 57 for details.
37	RWX	WOX_AND	WOX_OR	ARB_RCVD_NONFATAL_ERROR_MSG: See ARB Error Status Register, bit 58 for details.
38	RWX	WOX_AND	WOX_OR	ARB_RCVD_CORRECTIBLE_ERROR_MSG: See ARB Error Status Register, bit 59 for details.
39	RWX	WOX_AND	WOX_OR	PAPR_INBOUND_INJECT_ERROR: See Outbound Error Status Register, bit 39 for details.
40	RWX	WOX_AND	WOX_OR	ARB_COMMON_FATAL_ERROR: See ARB Error Status Register, bit 4/7/8/9/10/11/12/13/14/15/16/17/18/22/23/36/37/38/42/43/44/45/46/47/48/59/55/56 for details.
41	RWX	WOX_AND	WOX_OR	ARB_TABLE_BAR_DISABLED_ERROR: See ARB Error Status Register, bit 32/41 for details.
42	RWX	WOX_AND	WOX_OR	ARB_BLIF_COMPLETION_ERROR: See ARB Error Status Register, bit 00/01/19 for details.
43	RWX	WOX_AND	WOX_OR	ARB_PCT_TIMEOUT_ERROR: See ARB Error Status Register, bit 34/35 for details.
44	RWX	WOX_AND	WOX_OR	ARB_ECC_CORRECTABLE_ERROR: See ARB Error Status Register, bit 5/20/25/29 for details.
45	RWX	WOX_AND	WOX_OR	ARB_ECC_UNCORRECTABLE_ERROR: See ARB Error Status Register, bit 6/26/30/31 for details.
46	RWX	WOX_AND	WOX_OR	ARB_TLP_POISON_SIGNALED: See ARB Error Status Register, bit 24 for details.
47	RWX	WOX_AND	WOX_OR	ARB_RTT_PENUM_INVALID_ERROR: See ARB Error Status Register, bit 40 for details.
48	RWX	WOX_AND	WOX_OR	MRG_COMMON_FATAL_ERROR: See MRG Error Status Register, bit 08-16/22/23/26/28/30-37/40-50 for details.
49	RWX	WOX_AND	WOX_OR	MRG_TABLE_BAR_DISABLED_ERROR: See MRG Error Status Register, bit 51 for details.
50	RWX	WOX_AND	WOX_OR	MRG_ECC_CORRECTABLE_ERROR: See MRG Error Status Register, bit 40/56/58/60 for details.
51	RWX	WOX_AND	WOX_OR	MRG_ECC_UNCORRECTABLE_ERROR: See MRG Error Status Register, bit 41/57/59/61 for details.
52	RWX	WOX_AND	WOX_OR	MRG_AIB2_TX_TIMEOUT_ERROR: See MRG Error Status Register, bit 24 for details.
53	RWX	WOX_AND	WOX_OR	MRG_MRT_ERROR: See MRG Error Status Register, bit 17/18 for details.
54	RWX	WOX_AND	WOX_OR	MRG_Reserved01.
55	RWX	WOX_AND	WOX_OR	MRG_Reserved02.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
56	RWX	WOX_AND	WOX_OR	TCE_IODA_PAGE_ACCESS_ERROR: See TCE Error Status Register, bit 01/02 for details.
57	RWX	WOX_AND	WOX_OR	TCE_REQUEST_TIMEOUT_ERROR: See TCE Error Status Register, bit 08 for details.
58	RWX	WOX_AND	WOX_OR	TCE_UNEXPECTED_RESPONSE_ERROR: See TCE Error Status Register, bit 13 for details.
59	RWX	WOX_AND	WOX_OR	TCE_COMMON_FATAL_ERROR: See TCE Error Status Register for details.
60	RWX	WOX_AND	WOX_OR	TCE_ECC_CORRECTABLE_ERROR: See TCE Error Status Register, bit 09/11/25/27 for details.
61	RWX	WOX_AND	WOX_OR	TCE_ECC_UNCORRECTABLE_ERROR: See TCE Error Status Register, bit 10/12/26/28 for details.
62	RWX	WOX_AND	WOX_OR	TCE_Reserved01.
63	RWX	WOX_AND	WOX_OR	FIR_INTERNAL_PARITY_ERROR: FIR Internal Parity Error.

Register Name	**ETU FIR MASK Register**
Mnemonic	PE1.PHB2.ETUX08.RSB.RSB.REGS.MASK_REG
Address	

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
	000000000E01094B (SCOM) 000000000E01094C (SCOM1) 000000000E01094D (SCOM2)	000000000F01094B (SCOM) 000000000F01094C (SCOM1) 000000000F01094D (SCOM2)

Description	ETU FIR MASK Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	AIB_Command_Invalid.
1	RWX	WOX_AND	WOX_OR	AIB_Addressing_Error.
2	RWX	WOX_AND	WOX_OR	AIB_Access_Error.
3	RWX	WOX_AND	WOX_OR	PAPR_Outbound_Injection_Error_Triggered.
4	RWX	WOX_AND	WOX_OR	AIB_Fatal_Class_Error.
5	RWX	WOX_AND	WOX_OR	AIB_INF_Class_Error.
6	RWX	WOX_AND	WOX_OR	PE_Stop_State_Error.
7	RWX	WOX_AND	WOX_OR	AIB_Dat_Err_Signaled.
8	RWX	WOX_AND	WOX_OR	OUT_Common_Array_Fatal_Error.
9	RWX	WOX_AND	WOX_OR	OUT_Common_Latch_Fatal_Error.
10	RWX	WOX_AND	WOX_OR	OUT_Common_Logic_Fatal_Error.
11	RWX	WOX_AND	WOX_OR	BLIF_OUT_Interface_Parity_Error.
12	RWX	WOX_AND	WOX_OR	PCIE_CFG_Write_CA_or_UR_Response.
13	RWX	WOX_AND	WOX_OR	MMIO_Request_Timeout.
14	RWX	WOX_AND	WOX_OR	OUT_RRB_Sourced_Error.
15	RWX	WOX_AND	WOX_OR	CFG_Logic_Signaled_Error.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
16	RWX	WOX_AND	WOX_OR	RSB_Reg_Request_Address_Error.
17	RWX	WOX_AND	WOX_OR	RSB_FDA_Fatal_Error.
18	RWX	WOX_AND	WOX_OR	RSB_FDA_INF_Error.
19	RWX	WOX_AND	WOX_OR	RSB_FDB_Fatal_Error.
20	RWX	WOX_AND	WOX_OR	RSB_FDB_INF_Error.
21	RWX	WOX_AND	WOX_OR	RSB_ERR_Fatal_Error.
22	RWX	WOX_AND	WOX_OR	RSB_ERR_INF_Error.
23	RWX	WOX_AND	WOX_OR	RSB_DBG_Fatal_Error.
24	RWX	WOX_AND	WOX_OR	RSB_DBG_INF_Error.
25	RWX	WOX_AND	WOX_OR	RSB_PCIE_Request_Access_Error.
26	RWX	WOX_AND	WOX_OR	RSB_Bus_Logic_Error.
27	RWX	WOX_AND	WOX_OR	RSB_UVI_Fatal_Error.
28	RWX	WOX_AND	WOX_OR	RSB_UVI_INF_Error.
29	RWX	WOX_AND	WOX_OR	SCOM_Fatal_Error.
30	RWX	WOX_AND	WOX_OR	SCOM_INF_Error.
31	RWX	WOX_AND	WOX_OR	PCIE_Macro_Error_Active_Status.
32	RWX	WOX_AND	WOX_OR	ARB_IODA_Fatal_Error.
33	RWX	WOX_AND	WOX_OR	ARB_MSI_PE_Match_Error.
34	RWX	WOX_AND	WOX_OR	ARB_MSI_Address_Error.
35	RWX	WOX_AND	WOX_OR	ARB_TVT_Error.
36	RWX	WOX_AND	WOX_OR	ARB_Rcvd_Fatal_Error_Msg.
37	RWX	WOX_AND	WOX_OR	ARB_Rcvd_Nonfatal_Error_Msg.
38	RWX	WOX_AND	WOX_OR	ARB_Rcvd_Correctible_Error_Msg.
39	RWX	WOX_AND	WOX_OR	PAPR_Inbound_Injection_Error_Triggered.
40	RWX	WOX_AND	WOX_OR	ARB_Common_Fatal_Error.
41	RWX	WOX_AND	WOX_OR	ARB_Table_BAR_Disabled_Error.
42	RWX	WOX_AND	WOX_OR	ARB_BLIF_Completion_Error.
43	RWX	WOX_AND	WOX_OR	ARB_PCT_Timeout_Error.
44	RWX	WOX_AND	WOX_OR	ARB_ECC_Correctable_Error.
45	RWX	WOX_AND	WOX_OR	ARB_ECC_Uncorrectable_Error.
46	RWX	WOX_AND	WOX_OR	ARB_TLP_Poison_Signaled.
47	RWX	WOX_AND	WOX_OR	ARB_RTT_PENUM_Invalid_Error.
48	RWX	WOX_AND	WOX_OR	MRG_Common_Fatal_Error.
49	RWX	WOX_AND	WOX_OR	MRG_Table_BAR_Disabled_Error.
50	RWX	WOX_AND	WOX_OR	MRG_ECC_Correctable_Error.
51	RWX	WOX_AND	WOX_OR	MRG_ECC_Uncorrectable_Error.
52	RWX	WOX_AND	WOX_OR	MRG_AIB2_TX_Timeout_Error.
53	RWX	WOX_AND	WOX_OR	MRG_MRT_Error.
54	RWX	WOX_AND	WOX_OR	MRG_Reserved01.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
55	RWX	WOX_AND	WOX_OR	MRG_Reserved02.
56	RWX	WOX_AND	WOX_OR	TCE_IODA_Page_Access_Error.
57	RWX	WOX_AND	WOX_OR	TCE_Request_Timeout_Error.
58	RWX	WOX_AND	WOX_OR	TCE_Unexpected_Response_Error.
59	RWX	WOX_AND	WOX_OR	TCE_COMMON_Fatal_Errors.
60	RWX	WOX_AND	WOX_OR	TCE_ECC_Correctable_Error.
61	RWX	WOX_AND	WOX_OR	TCE_ECC_UnCorrectable_Error.
62	RWX	WOX_AND	WOX_OR	TCE_Reserved01.
63	RWX	WOX_AND	WOX_OR	LEM_FIR_Internal_Parity_Error.

Register Name	ETU FIR ACTION0 Register		
Mnemonic	PE1.PHB2.ETUX08.RSB.RSB.REGS.ACT0_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
		000000000E01094E (SCOM)	000000000F01094E (SCOM)
Description	ETU FIR ACTION0 Register		

Bits	SCOM	Field Mnemonic: Description
0	RWX	AIB_Command_Invalid.
1	RWX	AIB_Addressing_Error.
2	RWX	AIB_Access_Error.
3	RWX	PAPR_Outbound_Injection_Error_Triggered.
4	RWX	AIB_Fatal_Class_Error.
5	RWX	AIB_INF_Class_Error.
6	RWX	PE_Stop_State_Error.
7	RWX	AIB_Dat_Err_Signaled.
8	RWX	OUT_Common_Array_Fatal_Error.
9	RWX	OUT_Common_Latch_Fatal_Error.
10	RWX	OUT_Common_Logic_Fatal_Error.
11	RWX	BLIF_OUT_Interface_Parity_Error.
12	RWX	PCIE_CFG_Write_CA_or_UR_Response.
13	RWX	MMIO_Request_Timeout.
14	RWX	OUT_RRB_Sourced_Error.
15	RWX	CFG_Logic_Signaled_Error.
16	RWX	RSB_Reg_Request_Address_Error.
17	RWX	RSB_FDA_Fatal_Error.
18	RWX	RSB_FDA_INF_Error.
19	RWX	RSB_FDB_Fatal_Error.
20	RWX	RSB_FDB_INF_Error.

Bits	SCOM	Field Mnemonic: Description
21	RWX	RSB_ERR_Fatal_Error.
22	RWX	RSB_ERR_INF_Error.
23	RWX	RSB_DBG_Fatal_Error.
24	RWX	RSB_DBG_INF_Error.
25	RWX	RSB_PCIE_Request_Access_Error.
26	RWX	RSB_Bus_Logic_Error.
27	RWX	RSB_UVI_Fatal_Error.
28	RWX	RSB_UVI_INF_Error.
29	RWX	SCOM_Fatal_Error.
30	RWX	SCOM_INF_Error.
31	RWX	PCIE_Macro_Error_Active_Status.
32	RWX	ARB_IODA_Fatal_Error.
33	RWX	ARB_MSI_PE_Match_Error.
34	RWX	ARB_MSI_Address_Error.
35	RWX	ARB_TVT_Error.
36	RWX	ARB_Rcvd_Fatal_Error_Msg.
37	RWX	ARB_Rcvd_Nonfatal_Error_Msg.
38	RWX	ARB_Rcvd_Correctible_Error_Msg.
39	RWX	PAPR_Inbound_Injection_Error_Triggered.
40	RWX	ARB_Common_Fatal_Error.
41	RWX	ARB_Table_BAR_Disabled_Error.
42	RWX	ARB_BLIF_Completion_Error.
43	RWX	ARB_PCT_Timeout_Error.
44	RWX	ARB_ECC_Correctable_Error.
45	RWX	ARB_ECC_Uncorrectable_Error.
46	RWX	ARB_TLP_Poison_Signaled.
47	RWX	ARB_RTT_PENUM_Invalid_Error.
48	RWX	MRG_Common_Fatal_Error.
49	RWX	MRG_Table_BAR_Disabled_Error.
50	RWX	MRG_ECC_Correctable_Error.
51	RWX	MRG_ECC_Uncorrectable_Error.
52	RWX	MRG_AIB2_TX_Timeout_Error.
53	RWX	MRG_MRT_Error.
54	RWX	MRG_Reserved01.
55	RWX	MRG_Reserved02.
56	RWX	TCE_IODA_Page_Access_Error.
57	RWX	TCE_Request_Timeout_Error.
58	RWX	TCE_Unexpected_Response_Error.
59	RWX	TCE_COMMON_Fatal_Errors.

Bits	SCOM	Field Mnemonic: Description
60	RWX	TCE_ECC_Correctable_Error.
61	RWX	TCE_ECC_UnCorrectable_Error.
62	RWX	TCE_Reserved01.
63	RWX	LEM_FIR_Internal_Parity_Error.

Register Name	**ETU FIR ACTION1 Register**
Mnemonic	PE1.PHB2.ETUX08.RSB.RSB.REGS.ACTION1_REG
Address	<table><tr><th>PCI0 (PE0)</th><th>PCI1 (PE1)</th><th>PCI2 (PE2)</th></tr><tr><td></td><td>000000000E01094F (SCOM)</td><td>000000000F01094F (SCOM)</td></tr></table>
Description	ETU FIR ACTION1 Register

Bits	SCOM	Field Mnemonic: Description
0	RWX	AIB_Command_Invalid.
1	RWX	AIB_Addressing_Error.
2	RWX	AIB_Access_Error.
3	RWX	PAPR_Outbound_Injection_Error_Triggered.
4	RWX	AIB_Fatal_Class_Error.
5	RWX	AIB_INF_Class_Error.
6	RWX	PE_Stop_State_Error.
7	RWX	AIB_Dat_Err_Signaled.
8	RWX	OUT_Common_Array_Fatal_Error.
9	RWX	OUT_Common_Latch_Fatal_Error.
10	RWX	OUT_Common_Logic_Fatal_Error.
11	RWX	BLIF_OUT_Interface_Parity_Error.
12	RWX	PCIE_CFG_Write_CA_or_UR_Response.
13	RWX	MMIO_Request_Timeout.
14	RWX	OUT_RRB_Sourced_Error.
15	RWX	CFG_Logic_Signaled_Error.
16	RWX	RSB_Reg_Request_Address_Error.
17	RWX	RSB_FDA_Fatal_Error.
18	RWX	RSB_FDA_INF_Error.
19	RWX	RSB_FDB_Fatal_Error.
20	RWX	RSB_FDB_INF_Error.
21	RWX	RSB_ERR_Fatal_Error.
22	RWX	RSB_ERR_INF_Error.
23	RWX	RSB_DBG_Fatal_Error.
24	RWX	RSB_DBG_INF_Error.
25	RWX	RSB_PCIE_Request_Access_Error.

Bits	SCOM	Field Mnemonic: Description
26	RWX	RSB_Bus_Logic_Error.
27	RWX	RSB_UVI_Fatal_Error.
28	RWX	RSB_UVI_INF_Error.
29	RWX	SCOM_Fatal_Error.
30	RWX	SCOM_INF_Error.
31	RWX	PCIE_Macro_Error_Active_Status.
32	RWX	ARB_IODA_Fatal_Error.
33	RWX	ARB_MSI_PE_Match_Error.
34	RWX	ARB_MSI_Address_Error.
35	RWX	ARB_TVT_Error.
36	RWX	ARB_Rcvd_Fatal_Error_Msg.
37	RWX	ARB_Rcvd_Nonfatal_Error_Msg.
38	RWX	ARB_Rcvd_Correctible_Error_Msg.
39	RWX	PAPR_Inbound_Injection_Error_Triggered.
40	RWX	ARB_Common_Fatal_Error.
41	RWX	ARB_Table_BAR_Disabled_Error.
42	RWX	ARB_BLIF_Completion_Error.
43	RWX	ARB_PCT_Timeout_Error.
44	RWX	ARB_ECC_Correctable_Error.
45	RWX	ARB_ECC_Uncorrectable_Error.
46	RWX	ARB_TLP_Poison_Signaled.
47	RWX	ARB_RTT_PENUM_Invalid_Error.
48	RWX	MRG_Common_Fatal_Error.
49	RWX	MRG_Table_BAR_Disabled_Error.
50	RWX	MRG_ECC_Correctable_Error.
51	RWX	MRG_ECC_Uncorrectable_Error.
52	RWX	MRG_AIB2_TX_Timeout_Error.
53	RWX	MRG_MRT_Error.
54	RWX	MRG_Reserved01.
55	RWX	MRG_Reserved02.
56	RWX	TCE_IODA_Page_Access_Error.
57	RWX	TCE_Request_Timeout_Error.
58	RWX	TCE_Unexpected_Response_Error.
59	RWX	TCE_COMMON_Fatal_Errors.
60	RWX	TCE_ECC_Correctable_Error.
61	RWX	TCE_ECC_UnCorrectable_Error.
62	RWX	TCE_Reserved01.
63	RWX	LEM_FIR_Internal_Parity_Error.

Register Name	ETU FIR WOF Register		
Mnemonic	PE1.PHB2.ETUX08.RSB.RSB.REGS.WOF_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
		000000000E010950 (SCOM)	000000000F010950 (SCOM)
Description	ETU FIR WOF Register		

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	AIB_Command_Invalid.
1	RWX_WCLRREG	AIB_Addressing_Error.
2	RWX_WCLRREG	AIB_Access_Error.
3	RWX_WCLRREG	PAPR_Outbound_Injection_Error_Triggered.
4	RWX_WCLRREG	AIB_Fatal_Class_Error.
5	RWX_WCLRREG	AIB_INF_Class_Error.
6	RWX_WCLRREG	PE_Stop_State_Error.
7	RWX_WCLRREG	AIB_Dat_Err_Signaled.
8	RWX_WCLRREG	OUT_Common_Array_Fatal_Error.
9	RWX_WCLRREG	OUT_Common_Latch_Fatal_Error.
10	RWX_WCLRREG	OUT_Common_Logic_Fatal_Error.
11	RWX_WCLRREG	BLIF_OUT_Interface_Parity_Error.
12	RWX_WCLRREG	PCIE_CFG_Write_CA_or_UR_Response.
13	RWX_WCLRREG	MMIO_Request_Timeout.
14	RWX_WCLRREG	OUT_RRB_Sourced_Error.
15	RWX_WCLRREG	CFG_Logic_Signaled_Error.
16	RWX_WCLRREG	RSB_Reg_Request_Address_Error.
17	RWX_WCLRREG	RSB_FDA_Fatal_Error.
18	RWX_WCLRREG	RSB_FDA_INF_Error.
19	RWX_WCLRREG	RSB_FDB_Fatal_Error.
20	RWX_WCLRREG	RSB_FDB_INF_Error.
21	RWX_WCLRREG	RSB_ERR_Fatal_Error.
22	RWX_WCLRREG	RSB_ERR_INF_Error.
23	RWX_WCLRREG	RSB_DBG_Fatal_Error.
24	RWX_WCLRREG	RSB_DBG_INF_Error.
25	RWX_WCLRREG	RSB_PCIE_Request_Access_Error.
26	RWX_WCLRREG	RSB_Bus_Logic_Error.
27	RWX_WCLRREG	RSB_UVI_Fatal_Error.
28	RWX_WCLRREG	RSB_UVI_INF_Error.
29	RWX_WCLRREG	SCOM_Fatal_Error.
30	RWX_WCLRREG	SCOM_INF_Error.
31	RWX_WCLRREG	PCIE_Macro_Error_Active_Status.

Bits	SCOM	Field Mnemonic: Description
32	RWX_WCLRREG	ARB_IODA_Fatal_Error.
33	RWX_WCLRREG	ARB_MSI_PE_Match_Error.
34	RWX_WCLRREG	ARB_MSI_Address_Error.
35	RWX_WCLRREG	ARB_TVT_Error.
36	RWX_WCLRREG	ARB_Rcvd_Fatal_Error_Msg.
37	RWX_WCLRREG	ARB_Rcvd_Nonfatal_Error_Msg.
38	RWX_WCLRREG	ARB_Rcvd_Correctible_Error_Msg.
39	RWX_WCLRREG	PAPR_Inbound_Injection_Error_Triggered.
40	RWX_WCLRREG	ARB_Common_Fatal_Error.
41	RWX_WCLRREG	ARB_Table_BAR_Disabled_Error.
42	RWX_WCLRREG	ARB_BLIF_Completion_Error.
43	RWX_WCLRREG	ARB_PCT_Timeout_Error.
44	RWX_WCLRREG	ARB_ECC_Correctable_Error.
45	RWX_WCLRREG	ARB_ECC_Uncorrectable_Error.
46	RWX_WCLRREG	ARB_TLP_Poison_Signaled.
47	RWX_WCLRREG	ARB_RTT_PENUM_Invalid_Error.
48	RWX_WCLRREG	MRG_Common_Fatal_Error.
49	RWX_WCLRREG	MRG_Table_BAR_Disabled_Error.
50	RWX_WCLRREG	MRG_ECC_Correctable_Error.
51	RWX_WCLRREG	MRG_ECC_Uncorrectable_Error.
52	RWX_WCLRREG	MRG_AIB2_TX_Timeout_Error.
53	RWX_WCLRREG	MRG_MRT_Error.
54	RWX_WCLRREG	MRG_Reserved01.
55	RWX_WCLRREG	MRG_Reserved02.
56	RWX_WCLRREG	TCE_IODA_Page_Access_Error.
57	RWX_WCLRREG	TCE_Request_Timeout_Error.
58	RWX_WCLRREG	TCE_Unexpected_Response_Error.
59	RWX_WCLRREG	TCE_COMMON_Fatal_Errors.
60	RWX_WCLRREG	TCE_ECC_Correctable_Error.
61	RWX_WCLRREG	TCE_ECC_UnCorrectable_Error.
62	RWX_WCLRREG	TCE_Reserved01.
63	RWX_WCLRREG	LEM_FIR_Internal_Parity_Error.

Register Name	PHB4 Performance Configuration Register		
Mnemonic	PE1.PHB2.ETUX08.RSB.RSB.REGS.PERF_CFG_REG		
Address	PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
		000000000E010957 (SCOM)	000000000F010957 (SCOM)
Description	This register configures PHB4 performance.		

Bits	SCOM	Field Mnemonic: Description
0	RW	PERF_CFG_CNT_EN: Performance count enable.
1:3	RW	RESERVED.
4	RW	PERF_CFG_STOP_CORR_EN: Performance stop correlation enable.
5	RW	RESERVED.
6	RW	PERF_CFG_CNT0_LE_EN: Performance count 0 leading edge enable.
7	RW	PERF_CFG_CNT1_LE_EN: Performance count 1 leading edge enable.
8	RW	PERF_CFG_CNT2_LE_EN: Performance count 2 leading edge enable.
9	RW	PERF_CFG_CNT3_LE_EN: Performance count 3 leading edge enable.
10	RW	PERF_CFG_CNT0_TE_EN: Performance count 0 leading edge enable.
11	RW	PERF_CFG_CNT1_TE_EN: Performance count 1 leading edge enable.
12	RW	PERF_CFG_CNT2_TE_EN: Performance count 2 leading edge enable.
13	RW	PERF_CFG_CNT3_TE_EN: Performance count 3 leading edge enable.
14:17	RW	RESERVED.
18:23	RW	PERF_CFG_COUNT0_EVENT: Performance count 0 event select.
24:25	RW	RESERVED.
26:31	RW	PERF_CFG_COUNT1_EVENT: Performance count 1 event select.
32	RW	RESERVED.
33:39	RW	PERF_CFG_COUNT2_EVENT: Performance count 2 event select.
40:41	RW	RESERVED.
42:47	RW	PERF_CFG_COUNT3_EVENT: Performance count 3 event select.
48:63	RO	Constant = 0b0000000000000000

Register Name	PHB4 Performance Count0 Register		
Mnemonic	PE1.PHB2.ETUX08.RSB.RSB.REGS.PERF_CNT0_REG		
Address	PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
		000000000E010958 (SCOM)	000000000F010958 (SCOM)
Description	PHB4 Performance Count0 Register		

Bits	SCOM	Field Mnemonic: Description
0:47	RW	Count0_Value.

Bits	SCOM	Field Mnemonic: Description
48:63	RO	Constant = 0b0000000000000000

Register Name	PHB4 Performance Count1 Register
Mnemonic	PE1.PHB2.ETUX08.RSB.RSB.REGS.PERF_CNT1_REG
Address	
Description	PHB4 Performance Count1 Register

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
	000000000E010959 (SCOM)	000000000F010959 (SCOM)

Bits	SCOM	Field Mnemonic: Description
0:47	RW	Count1_Value.
48:63	RO	Constant = 0b0000000000000000

Register Name	PHB4 Performance Count2 Register
Mnemonic	PE1.PHB2.ETUX08.RSB.RSB.REGS.PERF_CNT2_REG
Address	
Description	PHB4 Performance Count2 Register

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
	000000000E01095A (SCOM)	000000000F01095A (SCOM)

Bits	SCOM	Field Mnemonic: Description
0:47	RW	Count2_Value.
48:63	RO	Constant = 0b0000000000000000

Register Name	PHB4 Performance Count3 Register
Mnemonic	PE1.PHB2.ETUX08.RSB.RSB.REGS.PERF_CNT3_REG
Address	
Description	PHB4 Performance Count3 Register

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
	000000000E01095B (SCOM)	000000000F01095B (SCOM)

Bits	SCOM	Field Mnemonic: Description
0:47	RW	Count3_Value.
48:63	RO	Constant = 0b0000000000000000

Register Name	PHB4 SCOM HV Indirect Address Register		
Mnemonic	PE2.PHB5.ETUX08.RSB.RSB.SCOM.SSR.PHB4_SCOM_HVIAR		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
			000000000F010980 (SCOM)
Description	PHB4 SCOM HV Indirect Address Register		

Bits	SCOM	Field Mnemonic: Description
0	RW	HV_REQ_ADDR_VLD: SCOM HV Request Valid.
1	RW	HV_REQ_4B: SCOM HV Request 4B Access.
2	RW	HV_AUTO_INC: SCOM HV Request Address Auto Increment.
3:50	RO	Constant = 0b000000000000000000000000000000000000000000000000
51:61	RW	HV_REQ_ADDR_VALUE: SCOM HV Request Indirect Address Value.
62:63	RO	Constant = 0b00

Register Name	PHB4 SCOM HV Indirect Address Register Read Port		
Mnemonic	PE2.PHB5.ETUX08.RSB.RSB.SCOM.SSR.PHB4_SCOM_HVIDR		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
			000000000F010981 (SCOM)
Description	PHB4 SCOM HV Indirect Address Register Read Port		

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	scom_hv_req_read_data.

Register Name	PHB4 SCOM HV Indirect Address Register Write Port		
Mnemonic	PE2.PHB5.ETUX08.RSB.RSB.SCOM.SSR.PHB4_SCOM_HVIDWR		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
			000000000F010981 (SCOM)
Description	PHB4 SCOM HV Indirect Address Register Write Port		

Bits	SCOM	Field Mnemonic: Description
0:63	WOX	scom_hv_req_write_data.

Register Name	PHB4 SCOM HV Indirect Address Register		
Mnemonic	PE2.PHB5.ETUX08.RSB.RSB.SCOM.SSR.PHB4_SCOM_UVIAR		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
			000000000F010982 (SCOM)
Description	PHB4 SCOM HV Indirect Address Register		

Bits	SCOM	Field Mnemonic: Description
0	RW	UV_REQ_ADDR_VLD: SCOM UV Request Valid.
1	RO	Constant = 0b0
2	RW	UV_AUTO_INC: SCOM UV Request Address Auto Increment.
3:51	RO	Constant = 0b0000000000000000000000000000000000000000000000000
52:60	RW	UV_REQ_ADDR_VALUE: SCOM UV Request Indirect Address Value.
61:63	RO	Constant = 0b000

Register Name	PHB4 SCOM UV Indirect Address Register Read Port		
Mnemonic	PE2.PHB5.ETUX08.RSB.RSB.SCOM.SSR.PHB4_SCOM_UVIDR		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
			000000000F010983 (SCOM)
Description	PHB4 SCOM UV Indirect Address Register Read Port		

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	scom_uv_req_read_data.

Register Name	PHB4 SCOM UV Indirect Address Register Write Port		
Mnemonic	PE2.PHB5.ETUX08.RSB.RSB.SCOM.SSR.PHB4_SCOM_UVIDWR		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
			000000000F010983 (SCOM)
Description	PHB4 SCOM UV Indirect Address Register Write Port		

Bits	SCOM	Field Mnemonic: Description
0:63	WOX	scom_uv_req_write_data.

Register Name	ETU FIR Register
Mnemonic	PE2.PHB5.ETUX08.RSB.RSB.REGS.FIR_REG
Address	
Description	ETU FIR Register

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
		000000000F010988 (SCOM) 000000000F010989 (SCOM1) 000000000F01098A (SCOM2)

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	AIB_COMMAND_INVALID: See Outbound Error Status Register, bit 0 for details.
1	RWX	WOX_AND	WOX_OR	AIB_ADDRESS_INVALID: See Outbound Error Status Register, bit 1/2 for details.
2	RWX	WOX_AND	WOX_OR	AIB_ACCESS_ERROR: See Outbound Error Status Register, bit 3/8 for details.
3	RWX	WOX_AND	WOX_OR	PAPR_OUTBOUND_INJECT_ERROR: See Outbound Error Status Register, bit 28 for details.
4	RWX	WOX_AND	WOX_OR	AIB_FATAL_CLASS_ERROR: See Outbound Error Status Register, bit 4/5/9/10/11/14/15 for details.
5	RWX	WOX_AND	WOX_OR	AIB_INF_Class_Error.
6	RWX	WOX_AND	WOX_OR	AIB_INF_CLASS_ERROR: See Outbound Error Status Register, bit 6 for details.
7	RWX	WOX_AND	WOX_OR	PE_STOP_STATE_SIGNALED: See Outbound Error Status Register, bit 13/22 for details.
8	RWX	WOX_AND	WOX_OR	OUT_COMMON_ARRAY_FATAL_ERROR: See Outbound Error Status Register, bit 23/37/38/40/43/44/45/47/48/49 for details.
9	RWX	WOX_AND	WOX_OR	OUT_COMMON_LATCH_FATAL_ERROR: See Outbound Error Status Register, bit 50/51/52 for details.
10	RWX	WOX_AND	WOX_OR	OUT_COMMON_LOGIC_FATAL_ERROR: See Outbound Error Status Register, bit 19/20/21/53/54/55 for details.
11	RWX	WOX_AND	WOX_OR	BLIF_OUT_INTERFACE_PARITY_ERROR: See Outbound Error Status Register, bit 16 for details.
12	RWX	WOX_AND	WOX_OR	CFG_WRITE_CA_OR_UR_RESPONSE: See Outbound Error Status Register, bit 17 for details.
13	RWX	WOX_AND	WOX_OR	MMIO_REQUEST_TIMEOUT: See Outbound Error Status Register, bit 18 for details.
14	RWX	WOX_AND	WOX_OR	OUT_RRB_SOURCED_ERROR: See Outbound Error Status Register, bit 56/57 for details.
15	RWX	WOX_AND	WOX_OR	CFG_LOGIC_SIGNALED_ERROR: See Outbound Error Status Register, bit 17 for details.
16	RWX	WOX_AND	WOX_OR	RSB_REG_REQUEST_ADDRESS_ERROR: See RSB Error Status Register, bit 00 for details.
17	RWX	WOX_AND	WOX_OR	RSB_FDA_FATAL_ERROR: See RSB Error Status Register, bit 2/3/5 for details.
18	RWX	WOX_AND	WOX_OR	RSB_FDA_INF_ERROR: See RSB Error Status Register, bit 1/4 for details.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
19	RWX	WOX_AND	WOX_OR	RSB_FDB_FATAL_ERROR: See RSB Error Status Register, bit 9/10 for details.
20	RWX	WOX_AND	WOX_OR	RSB_FDB_INF_ERROR: See RSB Error Status Register, bit 8 for details.
21	RWX	WOX_AND	WOX_OR	RSB_ERR_FATAL_ERROR: See RSB Error Status Register, bit 7 for details.
22	RWX	WOX_AND	WOX_OR	RSB_ERR_INF_ERROR: See RSB Error Status Register, bit 6 for details.
23	RWX	WOX_AND	WOX_OR	RSB_DBG_FATAL_ERROR: See RSB Error Status Register, bit 13/14 for details.
24	RWX	WOX_AND	WOX_OR	RSB_DBG_INF_ERROR: See RSB Error Status Register, bit 12 for details.
25	RWX	WOX_AND	WOX_OR	PCIE_REQUEST_ACCESS_ERROR: See Outbound Error Status Register, bit 11 for details.
26	RWX	WOX_AND	WOX_OR	RSB_BUS_LOGIC_ERROR: See Outbound Error Status Register, bit 15/27 for details.
27	RWX	WOX_AND	WOX_OR	RSB_UVI_FATAL_ERROR: See RSB Error Status Register, bit 17/19 for details.
28	RWX	WOX_AND	WOX_OR	RSB_UVI_INF_ERROR: See RSB Error Status Register, bit 16/18 for details.
29	RWX	WOX_AND	WOX_OR	SCOM_FATAL_ERROR: See RSB Error Status Register, bit 30/31 for details.
30	RWX	WOX_AND	WOX_OR	SCOM_INF_ERROR: See RSB Error Status Register, bit 28/29 for details.
31	RWX	WOX_AND	WOX_OR	PCIE_MACRO_ERROR_ACTIVE_STATUS: See RSB Error Status Register, bit 24/25/26 for details.
32	RWX	WOX_AND	WOX_OR	ARB_IODA_FATAL_ERROR: See ARB Error Status Register, bit 33 for details.
33	RWX	WOX_AND	WOX_OR	ARB_MSI_PE_MATCH_ERROR: See ARB Error Status Register, bit 27 for details.
34	RWX	WOX_AND	WOX_OR	ARB_MSI_ADDRESS_ERROR: See ARB Error Status Register, bit 02/03 for details.
35	RWX	WOX_AND	WOX_OR	ARB_TVT_ERROR: See ARB Error Status Register, bit 26/28 for details.
36	RWX	WOX_AND	WOX_OR	ARB_RCVD_FATAL_ERROR_MSG: See ARB Error Status Register, bit 57 for details.
37	RWX	WOX_AND	WOX_OR	ARB_RCVD_NONFATAL_ERROR_MSG: See ARB Error Status Register, bit 58 for details.
38	RWX	WOX_AND	WOX_OR	ARB_RCVD_CORRECTIBLE_ERROR_MSG: See ARB Error Status Register, bit 59 for details.
39	RWX	WOX_AND	WOX_OR	PAPR_INBOUND_INJECT_ERROR: See Outbound Error Status Register, bit 39 for details.
40	RWX	WOX_AND	WOX_OR	ARB_COMMON_FATAL_ERROR: See ARB Error Status Register, bit 4/7/8/9/10/11/12/13/14/15/16/17/18/22/23/36/37/38/42/43/44/45/46/47/48/59/55/56 for details.
41	RWX	WOX_AND	WOX_OR	ARB_TABLE_BAR_DISABLED_ERROR: See ARB Error Status Register, bit 32/41 for details.
42	RWX	WOX_AND	WOX_OR	ARB_BLIF_COMPLETION_ERROR: See ARB Error Status Register, bit 00/01/19 for details.
43	RWX	WOX_AND	WOX_OR	ARB_PCT_TIMEOUT_ERROR: See ARB Error Status Register, bit 34/35 for details.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
44	RWX	WOX_AND	WOX_OR	ARB_ECC_CORRECTABLE_ERROR: See ARB Error Status Register, bit 5/20/25/29 for details.
45	RWX	WOX_AND	WOX_OR	ARB_ECC_UNCORRECTABLE_ERROR: See ARB Error Status Register, bit 6/26/30/31 for details.
46	RWX	WOX_AND	WOX_OR	ARB_TLP_POISON_SIGNALED: See ARB Error Status Register, bit 24 for details.
47	RWX	WOX_AND	WOX_OR	ARB_RTT_PENUM_INVALID_ERROR: See ARB Error Status Register, bit 40 for details.
48	RWX	WOX_AND	WOX_OR	MRG_COMMON_FATAL_ERROR: See MRG Error Status Register, bit 08-16/22/23/26/28/30-37/40-50 for details.
49	RWX	WOX_AND	WOX_OR	MRG_TABLE_BAR_DISABLED_ERROR: See MRG Error Status Register, bit 51 for details.
50	RWX	WOX_AND	WOX_OR	MRG_ECC_CORRECTABLE_ERROR: See MRG Error Status Register, bit 40/56/58/60 for details.
51	RWX	WOX_AND	WOX_OR	MRG_ECC_UNCORRECTABLE_ERROR: See MRG Error Status Register, bit 41/57/59/61 for details.
52	RWX	WOX_AND	WOX_OR	MRG_AIB2_TX_TIMEOUT_ERROR: See MRG Error Status Register, bit 24 for details.
53	RWX	WOX_AND	WOX_OR	MRG_MRT_ERROR: See MRG Error Status Register, bit 17/18 for details.
54	RWX	WOX_AND	WOX_OR	MRG_Reserved01.
55	RWX	WOX_AND	WOX_OR	MRG_Reserved02.
56	RWX	WOX_AND	WOX_OR	TCE_IODA_PAGE_ACCESS_ERROR: See TCE Error Status Register, bit 01/02 for details.
57	RWX	WOX_AND	WOX_OR	TCE_REQUEST_TIMEOUT_ERROR: See TCE Error Status Register, bit 08 for details.
58	RWX	WOX_AND	WOX_OR	TCE_UNEXPECTED_RESPONSE_ERROR: See TCE Error Status Register, bit 13 for details.
59	RWX	WOX_AND	WOX_OR	TCE_COMMON_FATAL_ERROR: See TCE Error Status Register for details.
60	RWX	WOX_AND	WOX_OR	TCE_ECC_CORRECTABLE_ERROR: See TCE Error Status Register, bit 09/11/25/27 for details.
61	RWX	WOX_AND	WOX_OR	TCE_ECC_UNCORRECTABLE_ERROR: See TCE Error Status Register, bit 10/12/26/28 for details.
62	RWX	WOX_AND	WOX_OR	TCE_Reserved01.
63	RWX	WOX_AND	WOX_OR	FIR_INTERNAL_PARITY_ERROR: FIR Internal Parity Error.

Register Name	**ETU FIR MASK Register**
Mnemonic	PE2.PHB5.ETUX08.RSB.RSB.REGS.MASK_REG
Address	

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
		000000000F01098B (SCOM) 000000000F01098C (SCOM1) 000000000F01098D (SCOM2)

Description	ETU FIR MASK Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	AIB_Command_Invalid.
1	RWX	WOX_AND	WOX_OR	AIB_Addressing_Error.
2	RWX	WOX_AND	WOX_OR	AIB_Access_Error.
3	RWX	WOX_AND	WOX_OR	PAPR_Outbound_Injection_Error_Triggered.
4	RWX	WOX_AND	WOX_OR	AIB_Fatal_Class_Error.
5	RWX	WOX_AND	WOX_OR	AIB_INF_Class_Error.
6	RWX	WOX_AND	WOX_OR	PE_Stop_State_Error.
7	RWX	WOX_AND	WOX_OR	AIB_Dat_Err_Signaled.
8	RWX	WOX_AND	WOX_OR	OUT_Common_Array_Fatal_Error.
9	RWX	WOX_AND	WOX_OR	OUT_Common_Latch_Fatal_Error.
10	RWX	WOX_AND	WOX_OR	OUT_Common_Logic_Fatal_Error.
11	RWX	WOX_AND	WOX_OR	BLIF_OUT_Interface_Parity_Error.
12	RWX	WOX_AND	WOX_OR	PCIE_CFG_Write_CA_or_UR_Response.
13	RWX	WOX_AND	WOX_OR	MMIO_Request_Timeout.
14	RWX	WOX_AND	WOX_OR	OUT_RRB_Sourced_Error.
15	RWX	WOX_AND	WOX_OR	CFG_Logic_Signaled_Error.
16	RWX	WOX_AND	WOX_OR	RSB_Reg_Request_Address_Error.
17	RWX	WOX_AND	WOX_OR	RSB_FDA_Fatal_Error.
18	RWX	WOX_AND	WOX_OR	RSB_FDA_INF_Error.
19	RWX	WOX_AND	WOX_OR	RSB_FDB_Fatal_Error.
20	RWX	WOX_AND	WOX_OR	RSB_FDB_INF_Error.
21	RWX	WOX_AND	WOX_OR	RSB_ERR_Fatal_Error.
22	RWX	WOX_AND	WOX_OR	RSB_ERR_INF_Error.
23	RWX	WOX_AND	WOX_OR	RSB_DBG_Fatal_Error.
24	RWX	WOX_AND	WOX_OR	RSB_DBG_INF_Error.
25	RWX	WOX_AND	WOX_OR	RSB_PCIE_Request_Access_Error.
26	RWX	WOX_AND	WOX_OR	RSB_Bus_Logic_Error.
27	RWX	WOX_AND	WOX_OR	RSB_UVI_Fatal_Error.
28	RWX	WOX_AND	WOX_OR	RSB_UVI_INF_Error.
29	RWX	WOX_AND	WOX_OR	SCOM_Fatal_Error.
30	RWX	WOX_AND	WOX_OR	SCOM_INF_Error.
31	RWX	WOX_AND	WOX_OR	PCIE_Macro_Error_Active_Status.
32	RWX	WOX_AND	WOX_OR	ARB_IODA_Fatal_Error.
33	RWX	WOX_AND	WOX_OR	ARB_MSI_PE_Match_Error.
34	RWX	WOX_AND	WOX_OR	ARB_MSI_Address_Error.
35	RWX	WOX_AND	WOX_OR	ARB_TVT_Error.
36	RWX	WOX_AND	WOX_OR	ARB_Rcvd_Fatal_Error_Msg.
37	RWX	WOX_AND	WOX_OR	ARB_Rcvd_Nonfatal_Error_Msg.
38	RWX	WOX_AND	WOX_OR	ARB_Rcvd_Correctible_Error_Msg.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
39	RWX	WOX_AND	WOX_OR	PAPR_Inbound_Injection_Error_Triggered.
40	RWX	WOX_AND	WOX_OR	ARB_Common_Fatal_Error.
41	RWX	WOX_AND	WOX_OR	ARB_Table_BAR_Disabled_Error.
42	RWX	WOX_AND	WOX_OR	ARB_BLIF_Completion_Error.
43	RWX	WOX_AND	WOX_OR	ARB_PCT_Timeout_Error.
44	RWX	WOX_AND	WOX_OR	ARB_ECC_Correctable_Error.
45	RWX	WOX_AND	WOX_OR	ARB_ECC_Uncorrectable_Error.
46	RWX	WOX_AND	WOX_OR	ARB_TLP_Poison_Signaled.
47	RWX	WOX_AND	WOX_OR	ARB_RTT_PENUM_Invalid_Error.
48	RWX	WOX_AND	WOX_OR	MRG_Common_Fatal_Error.
49	RWX	WOX_AND	WOX_OR	MRG_Table_BAR_Disabled_Error.
50	RWX	WOX_AND	WOX_OR	MRG_ECC_Correctable_Error.
51	RWX	WOX_AND	WOX_OR	MRG_ECC_Uncorrectable_Error.
52	RWX	WOX_AND	WOX_OR	MRG_AIB2_TX_Timeout_Error.
53	RWX	WOX_AND	WOX_OR	MRG_MRT_Error.
54	RWX	WOX_AND	WOX_OR	MRG_Reserved01.
55	RWX	WOX_AND	WOX_OR	MRG_Reserved02.
56	RWX	WOX_AND	WOX_OR	TCE_IODA_Page_Access_Error.
57	RWX	WOX_AND	WOX_OR	TCE_Request_Timeout_Error.
58	RWX	WOX_AND	WOX_OR	TCE_Unexpected_Response_Error.
59	RWX	WOX_AND	WOX_OR	TCE_COMMON_Fatal_Errors.
60	RWX	WOX_AND	WOX_OR	TCE_ECC_Correctable_Error.
61	RWX	WOX_AND	WOX_OR	TCE_ECC_UnCorrectable_Error.
62	RWX	WOX_AND	WOX_OR	TCE_Reserved01.
63	RWX	WOX_AND	WOX_OR	LEM_FIR_Internal_Parity_Error.

Register Name	ETU FIR ACTION0 Register
Mnemonic	PE2.PHB5.ETUX08.RSB.RSB.REGS.ACT0_REG
Address	PCI0 (PE0): — ; PCI1 (PE1): — ; PCI2 (PE2): 000000000F01098E (SCOM)
Description	ETU FIR ACTION0 Register

Bits	SCOM	Field Mnemonic: Description
0	RWX	AIB_Command_Invalid.
1	RWX	AIB_Addressing_Error.
2	RWX	AIB_Access_Error.
3	RWX	PAPR_Outbound_Injection_Error_Triggered.
4	RWX	AIB_Fatal_Class_Error.

Bits	SCOM	Field Mnemonic: Description
5	RWX	AIB_INF_Class_Error.
6	RWX	PE_Stop_State_Error.
7	RWX	AIB_Dat_Err_Signaled.
8	RWX	OUT_Common_Array_Fatal_Error.
9	RWX	OUT_Common_Latch_Fatal_Error.
10	RWX	OUT_Common_Logic_Fatal_Error.
11	RWX	BLIF_OUT_Interface_Parity_Error.
12	RWX	PCIE_CFG_Write_CA_or_UR_Response.
13	RWX	MMIO_Request_Timeout.
14	RWX	OUT_RRB_Sourced_Error.
15	RWX	CFG_Logic_Signaled_Error.
16	RWX	RSB_Reg_Request_Address_Error.
17	RWX	RSB_FDA_Fatal_Error.
18	RWX	RSB_FDA_INF_Error.
19	RWX	RSB_FDB_Fatal_Error.
20	RWX	RSB_FDB_INF_Error.
21	RWX	RSB_ERR_Fatal_Error.
22	RWX	RSB_ERR_INF_Error.
23	RWX	RSB_DBG_Fatal_Error.
24	RWX	RSB_DBG_INF_Error.
25	RWX	RSB_PCIE_Request_Access_Error.
26	RWX	RSB_Bus_Logic_Error.
27	RWX	RSB_UVI_Fatal_Error.
28	RWX	RSB_UVI_INF_Error.
29	RWX	SCOM_Fatal_Error.
30	RWX	SCOM_INF_Error.
31	RWX	PCIE_Macro_Error_Active_Status.
32	RWX	ARB_IODA_Fatal_Error.
33	RWX	ARB_MSI_PE_Match_Error.
34	RWX	ARB_MSI_Address_Error.
35	RWX	ARB_TVT_Error.
36	RWX	ARB_Rcvd_Fatal_Error_Msg.
37	RWX	ARB_Rcvd_Nonfatal_Error_Msg.
38	RWX	ARB_Rcvd_Correctible_Error_Msg.
39	RWX	PAPR_Inbound_Injection_Error_Triggered.
40	RWX	ARB_Common_Fatal_Error.
41	RWX	ARB_Table_BAR_Disabled_Error.
42	RWX	ARB_BLIF_Completion_Error.
43	RWX	ARB_PCT_Timeout_Error.

Bits	SCOM	Field Mnemonic: Description
44	RWX	ARB_ECC_Correctable_Error.
45	RWX	ARB_ECC_Uncorrectable_Error.
46	RWX	ARB_TLP_Poison_Signaled.
47	RWX	ARB_RTT_PENUM_Invalid_Error.
48	RWX	MRG_Common_Fatal_Error.
49	RWX	MRG_Table_BAR_Disabled_Error.
50	RWX	MRG_ECC_Correctable_Error.
51	RWX	MRG_ECC_Uncorrectable_Error.
52	RWX	MRG_AIB2_TX_Timeout_Error.
53	RWX	MRG_MRT_Error.
54	RWX	MRG_Reserved01.
55	RWX	MRG_Reserved02.
56	RWX	TCE_IODA_Page_Access_Error.
57	RWX	TCE_Request_Timeout_Error.
58	RWX	TCE_Unexpected_Response_Error.
59	RWX	TCE_COMMON_Fatal_Errors.
60	RWX	TCE_ECC_Correctable_Error.
61	RWX	TCE_ECC_UnCorrectable_Error.
62	RWX	TCE_Reserved01.
63	RWX	LEM_FIR_Internal_Parity_Error.

Register Name	**ETU FIR ACTION1 Register**		
Mnemonic	PE2.PHB5.ETUX08.RSB.RSB.REGS.ACTION1_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
			000000000F01098F (SCOM)
Description	ETU FIR ACTION1 Register		

Bits	SCOM	Field Mnemonic: Description
0	RWX	AIB_Command_Invalid.
1	RWX	AIB_Addressing_Error.
2	RWX	AIB_Access_Error.
3	RWX	PAPR_Outbound_Injection_Error_Triggered.
4	RWX	AIB_Fatal_Class_Error.
5	RWX	AIB_INF_Class_Error.
6	RWX	PE_Stop_State_Error.
7	RWX	AIB_Dat_Err_Signaled.
8	RWX	OUT_Common_Array_Fatal_Error.
9	RWX	OUT_Common_Latch_Fatal_Error.

Bits	SCOM	Field Mnemonic: Description
10	RWX	OUT_Common_Logic_Fatal_Error.
11	RWX	BLIF_OUT_Interface_Parity_Error.
12	RWX	PCIE_CFG_Write_CA_or_UR_Response.
13	RWX	MMIO_Request_Timeout.
14	RWX	OUT_RRB_Sourced_Error.
15	RWX	CFG_Logic_Signaled_Error.
16	RWX	RSB_Reg_Request_Address_Error.
17	RWX	RSB_FDA_Fatal_Error.
18	RWX	RSB_FDA_INF_Error.
19	RWX	RSB_FDB_Fatal_Error.
20	RWX	RSB_FDB_INF_Error.
21	RWX	RSB_ERR_Fatal_Error.
22	RWX	RSB_ERR_INF_Error.
23	RWX	RSB_DBG_Fatal_Error.
24	RWX	RSB_DBG_INF_Error.
25	RWX	RSB_PCIE_Request_Access_Error.
26	RWX	RSB_Bus_Logic_Error.
27	RWX	RSB_UVI_Fatal_Error.
28	RWX	RSB_UVI_INF_Error.
29	RWX	SCOM_Fatal_Error.
30	RWX	SCOM_INF_Error.
31	RWX	PCIE_Macro_Error_Active_Status.
32	RWX	ARB_IODA_Fatal_Error.
33	RWX	ARB_MSI_PE_Match_Error.
34	RWX	ARB_MSI_Address_Error.
35	RWX	ARB_TVT_Error.
36	RWX	ARB_Rcvd_Fatal_Error_Msg.
37	RWX	ARB_Rcvd_Nonfatal_Error_Msg.
38	RWX	ARB_Rcvd_Corrictible_Error_Msg.
39	RWX	PAPR_Inbound_Injection_Error_Triggered.
40	RWX	ARB_Common_Fatal_Error.
41	RWX	ARB_Table_BAR_Disabled_Error.
42	RWX	ARB_BLIF_Completion_Error.
43	RWX	ARB_PCT_Timeout_Error.
44	RWX	ARB_ECC_Correctable_Error.
45	RWX	ARB_ECC_Uncorrectable_Error.
46	RWX	ARB_TLP_Poison_Signaled.
47	RWX	ARB_RTT_PENUM_Invalid_Error.
48	RWX	MRG_Common_Fatal_Error.

Bits	SCOM	Field Mnemonic: Description
49	RWX	MRG_Table_BAR_Disabled_Error.
50	RWX	MRG_ECC_Correctable_Error.
51	RWX	MRG_ECC_Uncorrectable_Error.
52	RWX	MRG_AIB2_TX_Timeout_Error.
53	RWX	MRG_MRT_Error.
54	RWX	MRG_Reserved01.
55	RWX	MRG_Reserved02.
56	RWX	TCE_IODA_Page_Access_Error.
57	RWX	TCE_Request_Timeout_Error.
58	RWX	TCE_Unexpected_Response_Error.
59	RWX	TCE_COMMON_Fatal_Errors.
60	RWX	TCE_ECC_Correctable_Error.
61	RWX	TCE_ECC_UnCorrectable_Error.
62	RWX	TCE_Reserved01.
63	RWX	LEM_FIR_Internal_Parity_Error.

Register Name	**ETU FIR WOF Register**
Mnemonic	PE2.PHB5.ETUX08.RSB.RSB.REGS.WOF_REG
Address	
Description	ETU FIR WOF Register

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
		000000000F010990 (SCOM)

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	AIB_Command_Invalid.
1	RWX_WCLRREG	AIB_Addressing_Error.
2	RWX_WCLRREG	AIB_Access_Error.
3	RWX_WCLRREG	PAPR_Outbound_Injection_Error_Triggered.
4	RWX_WCLRREG	AIB_Fatal_Class_Error.
5	RWX_WCLRREG	AIB_INF_Class_Error.
6	RWX_WCLRREG	PE_Stop_State_Error.
7	RWX_WCLRREG	AIB_Dat_Err_Signaled.
8	RWX_WCLRREG	OUT_Common_Array_Fatal_Error.
9	RWX_WCLRREG	OUT_Common_Latch_Fatal_Error.
10	RWX_WCLRREG	OUT_Common_Logic_Fatal_Error.
11	RWX_WCLRREG	BLIF_OUT_Interface_Parity_Error.
12	RWX_WCLRREG	PCIE_CFG_Write_CA_or_UR_Response.
13	RWX_WCLRREG	MMIO_Request_Timeout.
14	RWX_WCLRREG	OUT_RRB_Sourced_Error.

Bits	SCOM	Field Mnemonic: Description
15	RWX_WCLRREG	CFG_Logic_Signaled_Error.
16	RWX_WCLRREG	RSB_Reg_Request_Address_Error.
17	RWX_WCLRREG	RSB_FDA_Fatal_Error.
18	RWX_WCLRREG	RSB_FDA_INF_Error.
19	RWX_WCLRREG	RSB_FDB_Fatal_Error.
20	RWX_WCLRREG	RSB_FDB_INF_Error.
21	RWX_WCLRREG	RSB_ERR_Fatal_Error.
22	RWX_WCLRREG	RSB_ERR_INF_Error.
23	RWX_WCLRREG	RSB_DBG_Fatal_Error.
24	RWX_WCLRREG	RSB_DBG_INF_Error.
25	RWX_WCLRREG	RSB_PCIE_Request_Access_Error.
26	RWX_WCLRREG	RSB_Bus_Logic_Error.
27	RWX_WCLRREG	RSB_UVI_Fatal_Error.
28	RWX_WCLRREG	RSB_UVI_INF_Error.
29	RWX_WCLRREG	SCOM_Fatal_Error.
30	RWX_WCLRREG	SCOM_INF_Error.
31	RWX_WCLRREG	PCIE_Macro_Error_Active_Status.
32	RWX_WCLRREG	ARB_IODA_Fatal_Error.
33	RWX_WCLRREG	ARB_MSI_PE_Match_Error.
34	RWX_WCLRREG	ARB_MSI_Address_Error.
35	RWX_WCLRREG	ARB_TVT_Error.
36	RWX_WCLRREG	ARB_Rcvd_Fatal_Error_Msg.
37	RWX_WCLRREG	ARB_Rcvd_Nonfatal_Error_Msg.
38	RWX_WCLRREG	ARB_Rcvd_Correctible_Error_Msg.
39	RWX_WCLRREG	PAPR_Inbound_Injection_Error_Triggered.
40	RWX_WCLRREG	ARB_Common_Fatal_Error.
41	RWX_WCLRREG	ARB_Table_BAR_Disabled_Error.
42	RWX_WCLRREG	ARB_BLIF_Completion_Error.
43	RWX_WCLRREG	ARB_PCT_Timeout_Error.
44	RWX_WCLRREG	ARB_ECC_Correctable_Error.
45	RWX_WCLRREG	ARB_ECC_Uncorrectable_Error.
46	RWX_WCLRREG	ARB_TLP_Poison_Signaled.
47	RWX_WCLRREG	ARB_RTT_PENUM_Invalid_Error.
48	RWX_WCLRREG	MRG_Common_Fatal_Error.
49	RWX_WCLRREG	MRG_Table_BAR_Disabled_Error.
50	RWX_WCLRREG	MRG_ECC_Correctable_Error.
51	RWX_WCLRREG	MRG_ECC_Uncorrectable_Error.
52	RWX_WCLRREG	MRG_AIB2_TX_Timeout_Error.
53	RWX_WCLRREG	MRG_MRT_Error.

Bits	SCOM	Field Mnemonic: Description
54	RWX_WCLRREG	MRG_Reserved01.
55	RWX_WCLRREG	MRG_Reserved02.
56	RWX_WCLRREG	TCE_IODA_Page_Access_Error.
57	RWX_WCLRREG	TCE_Request_Timeout_Error.
58	RWX_WCLRREG	TCE_Unexpected_Response_Error.
59	RWX_WCLRREG	TCE_COMMON_Fatal_Errors.
60	RWX_WCLRREG	TCE_ECC_Correctable_Error.
61	RWX_WCLRREG	TCE_ECC_UnCorrectable_Error.
62	RWX_WCLRREG	TCE_Reserved01.
63	RWX_WCLRREG	LEM_FIR_Internal_Parity_Error.

Register Name	**PHB4 Performance Configuration Register**
Mnemonic	PE2.PHB5.ETUX08.RSB.RSB.REGS.PERF_CFG_REG
Address	PCI0 (PE0): ; PCI1 (PE1): ; PCI2 (PE2): 000000000F010997 (SCOM)
Description	PHB4 Performance Configuration Register

Bits	SCOM	Field Mnemonic: Description
0	RW	PERF_CFG_CNT_EN: Performance count enable.
1:3	RW	RESERVED.
4	RW	PERF_CFG_STOP_CORR_EN: Performance stop correlation enable.
5	RW	RESERVED.
6	RW	PERF_CFG_CNT0_LE_EN: Performance count 0 leading edge enable.
7	RW	PERF_CFG_CNT1_LE_EN: Performance count 1 leading edge enable.
8	RW	PERF_CFG_CNT2_LE_EN: Performance count 2 leading edge enable.
9	RW	PERF_CFG_CNT3_LE_EN: Performance count 3 leading edge enable.
10	RW	PERF_CFG_CNT0_TE_EN: Performance count 0 leading edge enable.
11	RW	PERF_CFG_CNT1_TE_EN: Performance count 1 leading edge enable.
12	RW	PERF_CFG_CNT2_TE_EN: Performance count 2 leading edge enable.
13	RW	PERF_CFG_CNT3_TE_EN: Performance count 3 leading edge enable.
14:17	RW	RESERVED.
18:23	RW	PERF_CFG_COUNT0_EVENT: Performance count 0 event select.
24:25	RW	RESERVED.
26:31	RW	PERF_CFG_COUNT1_EVENT: Performance count 1 event select.
32	RW	RESERVED.
33:39	RW	PERF_CFG_COUNT2_EVENT: Performance count 2 event select.
40:41	RW	RESERVED.
42:47	RW	PERF_CFG_COUNT3_EVENT: Performance count 3 event select.

Bits	SCOM	Field Mnemonic: Description
48:63	RO	Constant = 0b0000000000000000

Register Name	PHB4 Performance Count0 Register		
Mnemonic	PE2.PHB5.ETUX08.RSB.RSB.REGS.PERF_CNT0_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
			000000000F010998 (SCOM)
Description	PHB4 Performance Count0 Register		

Bits	SCOM	Field Mnemonic: Description
0:47	RW	Count0_Value.
48:63	RO	Constant = 0b0000000000000000

Register Name	PHB4 Performance Count1 Register		
Mnemonic	PE2.PHB5.ETUX08.RSB.RSB.REGS.PERF_CNT1_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
			000000000F010999 (SCOM)
Description	PHB4 Performance Count1 Register		

Bits	SCOM	Field Mnemonic: Description
0:47	RW	Count1_Value.
48:63	RO	Constant = 0b0000000000000000

Register Name	PHB4 Performance Count2 Register		
Mnemonic	PE2.PHB5.ETUX08.RSB.RSB.REGS.PERF_CNT2_REG		
Address	**PCI0 (PE0)**	**PCI1 (PE1)**	**PCI2 (PE2)**
			000000000F01099A (SCOM)
Description	PHB4 Performance Count2 Register		

Bits	SCOM	Field Mnemonic: Description
0:47	RW	Count2_Value.
48:63	RO	Constant = 0b0000000000000000

Register Name	PHB4 Performance Count3 Register
Mnemonic	PE2.PHB5.ETUX08.RSB.RSB.REGS.PERF_CNT3_REG
Address	
Description	PHB4 Performance Count3 Register

PCI0 (PE0)	PCI1 (PE1)	PCI2 (PE2)
		000000000F01099B (SCOM)

Bits	SCOM	Field Mnemonic: Description
0:47	RW	Count3_Value.
48:63	RO	Constant = 0b0000000000000000

11. CACHE Chiplet

The POWER9 processor registers are listed alphabetically by mnemonic in the following address table.

Mnemonic	Address	Page
TP.TCEP03.FIR_MASK	0x0000000013040002	2018
TP.TCEP03.HOSTATTN	0x0000000013040009	2020
TP.TCEP03.HOSTATTN_MASK	0x000000001304001A	2026
TP.TCEP03.LOCAL_FIR	0x000000001304000A	2021
TP.TCEP03.LOCAL_XSTOP_ERR	0x0000000013040018	2025
TP.TCEP03.LOCAL_XSTOP_MASK	0x0000000013040019	2026
TP.TCEP03.RFIR	0x0000000013040001	2018
TP.TCEP03.SPATTN	0x0000000013040004	2019
TP.TCEP03.SPA_MASK	0x0000000013040007	2019
TP.TCEP03.TPCL3.BIST	0x000000001303000B	2008
TP.TCEP03.TPCL3.CC_ATOMIC_LOCK_REG	0x00000000130303FF	2017
TP.TCEP03.TPCL3.CC_PROTECT_MODE_REG	0x00000000130303FE	2017
TP.TCEP03.TPCL3.CLK_REGION	0x0000000013030006	2005
TP.TCEP03.TPCL3.CLOCK_STAT_ARY	0x000000001303000A	2007
TP.TCEP03.TPCL3.CLOCK_STAT_NSL	0x0000000013030009	2006
TP.TCEP03.TPCL3.CLOCK_STAT_SL	0x0000000013030008	2006
TP.TCEP03.TPCL3.CPLT_CONF0	0x0000000013000008	1992
TP.TCEP03.TPCL3.CPLT_CONF1	0x0000000013000009	1994
TP.TCEP03.TPCL3.CPLT_CTRL0	0x0000000013000000	1989
TP.TCEP03.TPCL3.CPLT_CTRL1	0x0000000013000001	1991
TP.TCEP03.TPCL3.CPLT_MASK0	0x0000000010000101	1995
TP.TCEP03.TPCL3.CPLT_STAT0	0x0000000010000100	1994
TP.TCEP03.TPCL3.CTRL_ATOMIC_LOCK_REG	0x00000000130003FF	1996
TP.TCEP03.TPCL3.CTRL_PROTECT_MODE_REG	0x00000000130003FE	1995
TP.TCEP03.TPCL3.DBG_CBS_CC	0x0000000013030013	2016
TP.TCEP03.TPCL3.EPS.FIR.GXSTOP0_MASK_REG	0x0000000013040014	2023
TP.TCEP03.TPCL3.EPS.FIR.GXSTOP1_MASK_REG	0x0000000013040015	2024
TP.TCEP03.TPCL3.EPS.FIR.GXSTOP2_MASK_REG	0x0000000013040016	2024
TP.TCEP03.TPCL3.EPS.FIR.GXSTOP_TRIG_REG	0x0000000013040013	2023
TP.TCEP03.TPCL3.EPS.FIR.LOCAL_FIR_ACTION0	0x0000000013040010	2022
TP.TCEP03.TPCL3.EPS.FIR.LOCAL_FIR_ACTION1	0x0000000013040011	2022
TP.TCEP03.TPCL3.EPS.FIR.LOCAL_FIR_MASK	0x000000001304000D	2022
TP.TCEP03.TPCL3.EPS.FIR.MODE_REG	0x0000000013040008	2019
TP.TCEP03.TPCL3.EPS.FIR.SUM_MASK_REG	0x0000000013040017	2025
TP.TCEP03.TPCL3.EPS.PSC.PSC.ADDR_TRAP_REG	0x0000000013010003	1998
TP.TCEP03.TPCL3.EPS.PSC.PSC.ATOMIC_LOCK_MASK_LATCH_REG	0x0000000013010007	1999
TP.TCEP03.TPCL3.EPS.PSC.PSC.PSCOM_ERROR_MASK	0x0000000013010002	1998
TP.TCEP03.TPCL3.EPS.PSC.PSC.PSCOM_MODE_REG	0x0000000013010000	1996
TP.TCEP03.TPCL3.EPS.PSC.PSC.PSCOM_STATUS_ERROR_REG	0x0000000013010001	1996
TP.TCEP03.TPCL3.EPS.PSC.PSC.RING_FENCE_MASK_LATCH_REG	0x0000000013010008	1999
TP.TCEP03.TPCL3.EPS.PSC.PSC.WRITE_PROTECT_ENABLE_REG	0x0000000013010005	1999
TP.TCEP03.TPCL3.EPS.PSC.PSC.WRITE_PROTECT_RINGS_REG	0x0000000013010006	1999

Mnemonic	Address	Page
TP.TCEP03.TPCL3.EPS.THERM.CONTROL_REG	0x0000000013050012	2029
TP.TCEP03.TPCL3.EPS.THERM.DTS_RESULT0	0x0000000013050000	2026
TP.TCEP03.TPCL3.EPS.THERM.DTS_TRC_RESULT	0x0000000013050003	2026
TP.TCEP03.TPCL3.EPS.THERM.ERR_STATUS_REG	0x0000000013050013	2029
TP.TCEP03.TPCL3.EPS.THERM.INJECT_REG	0x0000000013050011	2028
TP.TCEP03.TPCL3.EPS.THERM.SKITTER_CLKSRC_REG	0x0000000013050016	2031
TP.TCEP03.TPCL3.EPS.THERM.SKITTER_DATA0	0x0000000013050019	2031
TP.TCEP03.TPCL3.EPS.THERM.SKITTER_DATA1	0x000000001305001A	2031
TP.TCEP03.TPCL3.EPS.THERM.SKITTER_DATA2	0x000000001305001B	2032
TP.TCEP03.TPCL3.EPS.THERM.SKITTER_FORCE_REG	0x0000000013050014	2031
TP.TCEP03.TPCL3.EPS.THERM.SKITTER_MODE_REG	0x0000000013050010	2028
TP.TCEP03.TPCL3.EPS.THERM.THERM_MODE_REG	0x000000001305000F	2027
TP.TCEP03.TPCL3.EPS.THERM.TIMESTAMP_COUNTER_READ	0x000000001305001C	2032
TP.TCEP03.TPCL3.ERROR_STATUS	0x000000001303000F	2013
TP.TCEP03.TPCL3.OPCG_ALIGN	0x0000000013030001	2000
TP.TCEP03.TPCL3.OPCG_CAPT1	0x0000000013030010	2014
TP.TCEP03.TPCL3.OPCG_CAPT2	0x0000000013030011	2015
TP.TCEP03.TPCL3.OPCG_CAPT3	0x0000000013030012	2015
TP.TCEP03.TPCL3.OPCG_REG0	0x0000000013030002	2002
TP.TCEP03.TPCL3.OPCG_REG1	0x0000000013030003	2003
TP.TCEP03.TPCL3.OPCG_REG2	0x0000000013030004	2003
TP.TCEP03.TPCL3.SCAN_REGION_TYPE	0x0000000013030005	2004
TP.TCEP03.TPCL3.SYNC_CONFIG	0x0000000013030000	2000
TP.TCEP03.TPCL3.XSTOP1	0x000000001303000C	2009
TP.TCEP03.TPCL3.XSTOP2	0x000000001303000D	2010
TP.TCEP03.TPCL3.XSTOP3	0x000000001303000E	2012
TP.TCEP03.XFIR	0x0000000013040000	2017

The POWER9 processor registers are listed in the following tables.

Register Name	Chiplet Control Register 0
Mnemonic	TP.TCEP03.TPCL3.CPLT_CTRL0
Address	0000000013000000 (SCOM) 0000000013000010 (SCOM1) 0000000013000020 (SCOM2)
Description	This register contains the first set of vital chiplet controls.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_OR	WO_CLEAR	CTRL_CC_ABSTCLK_MUXSEL_DC: Select the ABIST clock source for arrays on a chiplet boundary. When set to 1, clocks are used from a chiplet with ABIST.
1	RW	WO_OR	WO_CLEAR	TC_UNIT_SYNCCLK_MUXSEL_DC: Select the synchronous clock for asynchronous latches. (The initial value is 1.)

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
2	RW	WO_OR	WO_CLEAR	CTRL_CC_FLUSHMODE_INH_DC: Prevent pipeline latches from going into flush mode. (The initial value is 1.)
3	RW	WO_OR	WO_CLEAR	CTRL_CC_FORCE_ALIGN_DC: Force an alignment signal to be sent. (The initial value is 1. Drop before dropping flushmode_inh.)
4	RW	WO_OR	WO_CLEAR	TC_UNIT_ARY_WRT_THRU_DC: Set the array into write-through mode. Used for LBIST.
5	RW	WO_OR	WO_CLEAR	TC_UNIT_AVP_MODE: AVP mode. Switches from refresh pulse to phase counter.
6	RW	WO_OR	WO_CLEAR	FREE_USAGE_6A: Free usage.
7	RW	WO_OR	WO_CLEAR	FREE_USAGE_7A: Free usage.
8	RW	WO_OR	WO_CLEAR	CTRL_CC_ABIST_RECOV_DISABLE_DC: New signal to disable recovery.
9	RW	WO_OR	WO_CLEAR	FREE_USAGE_9A: Free usage.
10	RW	WO_OR	WO_CLEAR	TC_UNIT_IOBIST_TX_WRAP_ENABLE_DC:
11	RW	WO_OR	WO_CLEAR	RESERVED_11A: Reserved.
12	RW	WO_OR	WO_CLEAR	TC_SKIT_MODE_BIST_DC:
13	RW	WO_OR	WO_CLEAR	TC_UNIT_DETERMINISTIC_TEST_ENABLE_DC: Forces login into deterministic test mode. For example, for LBIST.
14	RW	WO_OR	WO_CLEAR	TC_UNIT_CONSTRAIN_SAFESCAN_DC: Safe scan of N1L latches. Prevent lock when switching SE.
15	RW	WO_OR	WO_CLEAR	TC_UNIT_RRFA_TEST_ENABLE_DC:
16	RW	WO_OR	WO_CLEAR	TC_NBTI_HDR_ENABLE_OVR_DC: NBTI.
17	RW	WO_OR	WO_CLEAR	TC_NBTI_PROBE_GATE_DC: NBTI.
18	RW	WO_OR	WO_CLEAR	RESERVED_18A: Reserved.
19	RW	WO_OR	WO_CLEAR	RESERVED_19A: Reserved.
20:27	RW	WO_OR	WO_CLEAR	TC_PSRO_SEL_DC: PSRO select.
28	RW	WO_OR	WO_CLEAR	TC_BSC_WRAPSEL_DC: Wrap select for BSC.
29	RW	WO_OR	WO_CLEAR	TC_BSC_INTMODE_DC: INT mode for BSC.
30	RW	WO_OR	WO_CLEAR	TC_BSC_INV_DC: INV for BSC mode.
31	RW	WO_OR	WO_CLEAR	TC_BSC_EXTMODE_DC: EXT mode for BSC.
32	RW	WO_OR	WO_CLEAR	TC_REFCLK_DRVR_EN_DC: Reference clock driver enable.
33	RW	WO_OR	WO_CLEAR	RESERVED_33A: Reserved.
34	RW	WO_OR	WO_CLEAR	RESERVED_34A: Reserved.
35	RW	WO_OR	WO_CLEAR	RESERVED_35A: Reserved.
36	RW	WO_OR	WO_CLEAR	TC_OELCC_EDGE_DELAYED_DC: Allows to delay the alignment by one fast cycle. Only used in dual mesh chiplets.
37	RW	WO_OR	WO_CLEAR	TC_OELCC_ALIGN_FLUSH_DC: Forces the alignment and odd/even toggling latch into a flush state. For DFT only.
38	RW	WO_OR	WO_CLEAR	RESERVED_38A: Reserved.
39	RW	WO_OR	WO_CLEAR	RESERVED_39A: Reserved.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
40:41	RW	WO_OR	WO_CLEAR	CTRL_MISC_CLKDIV_SEL_DC: Clock divider select. 00 = 1024:1 01 = 64:1 10 = 16:1 11 = 4:1
42	RW	WO_OR	WO_CLEAR	RESERVED_42A: Reserved.
43	RW	WO_OR	WO_CLEAR	RESERVED_43A: Reserved.
44	RW	WO_OR	WO_CLEAR	CTRL_CC_DCTEST_DC: TE = 1 only. Enable DCTEST.
45	RW	WO_OR	WO_CLEAR	CTRL_CC_OTP_PRGMODE_DC: TE = 1 only. OTP ROM program mode.
46	RW	WO_OR	WO_CLEAR	CTRL_CC_SSS_CALIBRATE_DC: TE = 1 only. Sensors calibration.
47	RW	WO_OR	WO_CLEAR	CTRL_CC_PIN_LBIST_DC: TE = 1 only. PIN LBIST mode. The LBIST is controlled by the pin, not by the OPCG.
48	RW	WO_OR	WO_CLEAR	FREE_USAGE_48A: Free usage.
49	RW	WO_OR	WO_CLEAR	FREE_USAGE_49A: Free usage.
50	RW	WO_OR	WO_CLEAR	FREE_USAGE_50A: Free usage.
51	RW	WO_OR	WO_CLEAR	FREE_USAGE_51A: Free usage.
52	RW	WO_OR	WO_CLEAR	FREE_USAGE_52A: Free usage.
53	RW	WO_OR	WO_CLEAR	FREE_USAGE_53A: Free usage.
54	RW	WO_OR	WO_CLEAR	FREE_USAGE_54A: Free usage.
55	RW	WO_OR	WO_CLEAR	FREE_USAGE_55A: Free usage.
56	RW	WO_OR	WO_CLEAR	FREE_USAGE_56A: Free usage.
57	RW	WO_OR	WO_CLEAR	FREE_USAGE_57A: Free usage.
58	RW	WO_OR	WO_CLEAR	FREE_USAGE_58A: Free usage.
59	RW	WO_OR	WO_CLEAR	FREE_USAGE_59A: Free usage.
60	RW	WO_OR	WO_CLEAR	FREE_USAGE_60A: Free usage.
61	RW	WO_OR	WO_CLEAR	FREE_USAGE_61A: Free usage.
62	RW	WO_OR	WO_CLEAR	FREE_USAGE_62A: Free usage.
63	RW	WO_OR	WO_CLEAR	FREE_USAGE_63A: Free usage.

Register Name	**Chiplet Control Register 1**
Mnemonic	TP.TCEP03.TPCL3.CPLT_CTRL1
Address	0000000013000001 (SCOM) 0000000013000011 (SCOM1) 0000000013000021 (SCOM2)
Description	This register contains the second set of vital chiplet controls.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_OR	WO_CLEAR	UNUSED_0B: Unused.
1	RW	WO_OR	WO_CLEAR	UNUSED_1B: Unused.
2	RW	WO_OR	WO_CLEAR	UNUSED_2B: Unused.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
3	RW	WO_OR	WO_CLEAR	TC_VITL_REGION_FENCE: VITL fence. Protect the VITL region logic from pollution by other regions during LBIST, or when the chiplet is not initialized and running yet.
4	RW	WO_OR	WO_CLEAR	TC_PERV_REGION_FENCE: Fence for pervasive region.
5	RW	WO_OR	WO_CLEAR	TC_REGION1_FENCE: Fence for region unit1.
6	RW	WO_OR	WO_CLEAR	TC_REGION2_FENCE: Fence for region unit2.
7	RW	WO_OR	WO_CLEAR	TC_REGION3_FENCE: Fence for region unit3.
8	RW	WO_OR	WO_CLEAR	TC_REGION4_FENCE: Fence for region unit4.
9	RW	WO_OR	WO_CLEAR	TC_REGION5_FENCE: Fence for region unit5.
10	RW	WO_OR	WO_CLEAR	TC_REGION6_FENCE: Fence for region unit6.
11	RW	WO_OR	WO_CLEAR	TC_REGION7_FENCE: Fence for region unit7.
12	RW	WO_OR	WO_CLEAR	TC_REGION8_FENCE: Fence for region unit8.
13	RW	WO_OR	WO_CLEAR	TC_REGION9_FENCE: Fence for region unit9.
14	RW	WO_OR	WO_CLEAR	UNUSED_14B: Unused.
15	RW	WO_OR	WO_CLEAR	RESERVED: Reserved.
16	RW	WO_OR	WO_CLEAR	TC_UNIT_MULTICYCLE_TEST_FENCE:
17	RW	WO_OR	WO_CLEAR	UNUSED_17B: Unused.
18	RW	WO_OR	WO_CLEAR	UNUSED_18B: Unused.
19	RW	WO_OR	WO_CLEAR	UNUSED_19B: Unused.
20	RW	WO_OR	WO_CLEAR	UNUSED_20B: Unused.
21	RW	WO_OR	WO_CLEAR	UNUSED_21B: Unused.
22	RW	WO_OR	WO_CLEAR	UNUSED_22B: Unused.
23	RW	WO_OR	WO_CLEAR	UNUSED_23B: Unused.
24	RW	WO_OR	WO_CLEAR	UNUSED_24B: Unused.
25	RW	WO_OR	WO_CLEAR	UNUSED_25B: Unused.
26	RW	WO_OR	WO_CLEAR	UNUSED_26B: Unused.
27	RW	WO_OR	WO_CLEAR	UNUSED_27B: Unused.
28	RW	WO_OR	WO_CLEAR	UNUSED_28B: Unused.
29	RW	WO_OR	WO_CLEAR	UNUSED_29B: Unused.
30	RW	WO_OR	WO_CLEAR	UNUSED_30B: Unused.
31	RW	WO_OR	WO_CLEAR	UNUSED_31B: Unused.

Register Name	Chiplet Configuration Register 0
Mnemonic	TP.TCEP03.TPCL3.CPLT_CONF0
Address	0000000013000008 (SCOM) 0000000013000018 (SCOM1) 0000000013000028 (SCOM2)
Description	This register contains the first set of vital chiplet configuration functions.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:5	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE0_SEL_DC: Probe 0 select.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
6	RW	WO_OR	WO_CLEAR	RESERVED_6C: Reserved.
7	RW	WO_OR	WO_CLEAR	RESERVED_7C: Reserved.
8:13	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE1_SEL_DC: Probe 1 select.
14	RW	WO_OR	WO_CLEAR	RESERVED_14C: Reserved.
15	RW	WO_OR	WO_CLEAR	RESERVED_15C: Reserved.
16:21	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE2_SEL_DC: Probe 2 select.
22	RW	WO_OR	WO_CLEAR	RESERVED_22C: Reserved.
23	RW	WO_OR	WO_CLEAR	RESERVED_23C: Reserved.
24:29	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE3_SEL_DC: Probe 3 select.
30	RW	WO_OR	WO_CLEAR	RESERVED_30C: Reserved.
31	RW	WO_OR	WO_CLEAR	RESERVED_31C: Reserved.
32	RW	WO_OR	WO_CLEAR	CTRL_CC_OFLOW_FEH_SEL_DC: Enables ABIST overflow or failure indication.
33	RW	WO_OR	WO_CLEAR	CTRL_CC_SCAN_PROTECT_DC: Enables scan protection and the scan collision error mechanism.
34	RW	WO_OR	WO_CLEAR	CTRL_CC_SDIS_DC_N: Disables the scan diagnostic scan path.
35	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_35C: Reserved for test control.
36	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_36C: Reserved for test control.
37	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_37C: Reserved for test control.
38	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_38C: Reserved for test control.
39	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_39C: Reserved for test control.
40	RW	WO_OR	WO_CLEAR	CTRL_EPS_MASK_VITL_PCB_ERR_DC: Mask VITL PCB errors from CC or CPLT_CTRL.
41	RW	WO_OR	WO_CLEAR	CTRL_CC_MASK_VITL_SCAN_OPCG_ERR_DC: Mask VITL errors in CC, which are not PCB related.
42	RW	WO_OR	WO_CLEAR	RESERVED_42C: Reserved.
43	RW	WO_OR	WO_CLEAR	RESERVED_43C: Reserved.
44	RW	WO_OR	WO_CLEAR	FREE_USAGE_44C: Free usage.
45	RW	WO_OR	WO_CLEAR	FREE_USAGE_45C: Free usage.
46	RW	WO_OR	WO_CLEAR	FREE_USAGE_46C: Free usage.
47	RW	WO_OR	WO_CLEAR	FREE_USAGE_47C: Free usage.
48:51	RW	WO_OR	WO_CLEAR	TC_UNIT_GROUP_ID_DC: Group ID.
52:54	RW	WO_OR	WO_CLEAR	TC_UNIT_CHIP_ID_DC: Chip ID.
55	RW	WO_OR	WO_CLEAR	RESERVED_ID_55C: Reserved ID.
56:60	RW	WO_OR	WO_CLEAR	TC_UNIT_SYS_ID_DC: System ID.
61	RW	WO_OR	WO_CLEAR	RESERVED_ID_61C: Reserved ID.
62	RW	WO_OR	WO_CLEAR	RESERVED_ID_62C: Reserved ID.
63	RW	WO_OR	WO_CLEAR	RESERVED_ID_63C: Reserved ID.

Register Name	Chiplet Configuration Register 1
Mnemonic	TP.TCEP03.TPCL3.CPLT_CONF1
Address	0000000013000009 (SCOM) 0000000013000019 (SCOM1) 0000000013000029 (SCOM2)
Description	This register contains the second set of vital chiplet configuration functions.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:3	RW	WO_OR	WO_CLEAR	TCEP_AMUX_VSELECT_EQ: AMUX control.
4:5	RW	WO_OR	WO_CLEAR	TCEP_AMUX_VSELECT_PWR_UP:
6:7	RW	WO_OR	WO_CLEAR	TCEP_AMUX_VSELECT_PWR_DN:
8:11	RW	WO_OR	WO_CLEAR	TCEP_AMUX_VSELECT_L3_UP:
12:15	RW	WO_OR	WO_CLEAR	TCEP_AMUX_VSELECT_L3_DN:
16	RW	WO_OR	WO_CLEAR	FREE_USAGE_16D: Free usage.
17	RW	WO_OR	WO_CLEAR	FREE_USAGE_17D: Free usage.
18	RW	WO_OR	WO_CLEAR	FREE_USAGE_18D: Free usage.
19	RW	WO_OR	WO_CLEAR	FREE_USAGE_19D: Free usage.
20	RW	WO_OR	WO_CLEAR	FREE_USAGE_20D: Free usage.
21	RW	WO_OR	WO_CLEAR	FREE_USAGE_21D: Free usage.
22	RW	WO_OR	WO_CLEAR	FREE_USAGE_22D: Free usage.
23	RW	WO_OR	WO_CLEAR	FREE_USAGE_23D: Free usage.
24	RW	WO_OR	WO_CLEAR	FREE_USAGE_24D: Free usage.
25	RW	WO_OR	WO_CLEAR	FREE_USAGE_25D: Free usage.
26	RW	WO_OR	WO_CLEAR	FREE_USAGE_26D: Free usage.
27	RW	WO_OR	WO_CLEAR	FREE_USAGE_27D: Free usage.
28	RW	WO_OR	WO_CLEAR	FREE_USAGE_28D: Free usage.
29	RW	WO_OR	WO_CLEAR	FREE_USAGE_29D: Free usage.
30	RW	WO_OR	WO_CLEAR	FREE_USAGE_30D: Free usage.
31	RW	WO_OR	WO_CLEAR	FREE_USAGE_31D: Free usage.

Register Name	Chiplet Status Register
Mnemonic	TP.TCEP03.TPCL3.CPLT_STAT0
Address	0000000010000100 (SCOM)
Description	An interrupt is sent out on a bit change if not masked by the Chiplet Mask Register. A mask only masks the interrupt, not the status register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	SRAM_ABIST_DONE_DC: SRAM and eDRAM ABIST done.
1	ROX	DRAM_ABIST_DONE_DC: Unused in POWER9 DD1.
2	ROX	RESERVED_2E: Reserved.
3	ROX	RESERVED_3E: Reserved.
4	ROX	TC_DIAG_PORT0_OUT: Diagnostic output port.

Bits	SCOM	Field Mnemonic: Description
5	ROX	TC_DIAG_PORT1_OUT: Diagnostic output port.
6	ROX	RESERVED_6E: Reserved.
7	ROX	PLL_DESTOUT: Reserved.
8	ROX	CC_CTRL_OPCG_DONE_DC: OPCG done. For LBIST, ABIST, or other OPCG runs.
9	ROX	CC_CTRL_CHIPLET_IS_ALIGNED_DC: Indicates that a chiplet is aligned.
10	ROX	FREE_USAGE_10E: Free usage.
11	ROX	FREE_USAGE_11E: Free usage.
12	ROX	FREE_USAGE_12E: Free usage.
13	ROX	FREE_USAGE_13E: Free usage.
14	ROX	FREE_USAGE_14E: Free usage.
15	ROX	FREE_USAGE_15E: Free usage.
16	ROX	FREE_USAGE_16E: Free usage.
17	ROX	FREE_USAGE_17E: Free usage.
18	ROX	FREE_USAGE_18E: Free usage.
19	ROX	FREE_USAGE_19E: Free usage.
20	ROX	FREE_USAGE_20E: Free usage.
21	ROX	FREE_USAGE_21E: Free usage.
22	ROX	FREE_USAGE_22E: Free usage.
23	ROX	FREE_USAGE_23E: Free usage.

Register Name	Chiplet Mask Register
Mnemonic	TP.TCEP03.TPCL3.CPLT_MASK0
Address	0000000010000101 (SCOM)
Description	This register masks an interrupt when a bit changes in the Chiplet Status Register. It does not mask the status itself.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CPLTMASK0: Bitwise masking of the Chiplet Status Register.

Register Name	Control Protect Mode Register
Mnemonic	TP.TCEP03.TPCL3.CTRL_PROTECT_MODE_REG
Address	00000000130003FE (SCOM)
Description	This register enables read and write protection.

Bits	SCOM	Field Mnemonic: Description
0	RW	CTRL_READ_PROTECT_ENABLE: Enable read protection.
1	RW	CTRL_WRITE_PROTECT_ENABLE: Enable write protection.

Register Name	Atomic Lock Register
Mnemonic	TP.TCEP03.TPCL3.CTRL_ATOMIC_LOCK_REG
Address	00000000130003FF (SCOM)
Description	This register enables an atomic lock and an atomic lock counter.

Bits	SCOM	Field Mnemonic: Description
0	RW	CTRL_ATOMIC_LOCK_ENABLE: Enable atomic lock.
1:4	ROX	CTRL_ATOMIC_ID: Atomic ID.
5:7	RO	constant = 0b000
8:15	ROX	CTRL_ATOMIC_ACTIVITY: Atomic lock counter.

Register Name	PSCOMLE Mode Register
Mnemonic	TP.TCEP03.TPCL3.EPS.PSC.PSC.PSCOM_MODE_REG
Address	0000000013010000 (SCOM)
Description	This is the parallel-to-serial communication light edition (PSCOMLE) mode register.

Bits	SCOM	Field Mnemonic: Description
0	RW	ABORT_ON_PCB_ADDR_PARITY_ERROR: Abort on PCB address parity error.
1	RW	ABORT_ON_PCB_WDATA_PARITY_ERROR: Abort on PCB write data parity error.
2	RW	ABORT_ON_DL_RETURN_P0_ERROR: Unused.
3	RW	ABORT_ON_DL_RETURN_WDATA_PARITY_ERROR: Abort on DL return write data parity error.
4	RW	WATCHDOG_ENABLE: Enable watchdog.
5:6	RW	SCOM_HANG_LIMIT: 0b11 = 256 0b10 = 512 0b01 = 768 0b00 = 1023
7	RW	FORCE_ALL_RINGS: Set to a logical 1 if all rings should be enabled independent of the ring address.
8	RW	FSM_SELFRESET_ON_STATEVEC_PARITYERROR_ENABLE: FSM self reset on statevec parity error enable.
9:11	RW	RESERVED_PSCOM_MODE_LT: Reserved.

Register Name	PSCOMLE Error Register
Mnemonic	TP.TCEP03.TPCL3.EPS.PSC.PSC.PSCOM_STATUS_ERROR_REG
Address	0000000013010001 (SCOM)
Description	This is the parallel-to-serial communication light edition (PSCOMLE) error register.

Bits	SCOM	Field Mnemonic: Description
0	RWX	ACCUMULATED_PCB_WDATA_PARITY_ERROR: Accumulated PCB write data parity error.
1	RWX	ACCUMULATED_PCB_ADDRESS_PARITY_ERROR: Accumulated PCB address parity error.
2	RWX	ACCUMULATED_DL_RETURN_WDATA_PARITY_ERROR: Accumulated DL return write data parity error.
3	RWX	ACCUMULATED_DL_RETURN_P0_ERROR: Accumulated DL return P0 error.

Bits	SCOM	Field Mnemonic: Description
4	RWX	ACCUMULATED_UL_RDATA_PARITY_ERROR: Accumulated UL read data parity error.
5	RWX	ACCUMULATED_UL_P0_ERROR: Accumulated UL P0 error.
6	RWX	ACCUMULATED_PARITY_ERROR_ON_INTERFACE_MACHINE: Accumulated parity error on interface machine.
7	RWX	ACCUMULATED_PARITY_ERROR_ON_P2S_MACHINE: Accumulated parity error on p2s machine.
8	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_ULCCH: Accumulated timeout while waiting for ULCCH.
9	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: Accumulated timeout while waiting for DLDCH return.
10	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_ULDCH: Accumulated timeout while waiting for ULDCH.
11	RWX	ACCUMULATED_PSCOM_PARALLEL_WRITE_NVLD: Accumulated PSCOM parallel write NVLD.
12	RWX	ACCUMULATED_PSCOM_PARALLEL_READ_NVLD: Accumulated PSCOM parallel read NVLD.
13	RWX	ACCUMULATED_PSCOM_PARALLEL_ADDR_INVALID: Accumulated PSCOM parallel address invalid.
14	RWX	ACCUMULATED_PCB_COMMAND_PARITY_ERROR: Accumulated PCB command parity error.
15	RWX	ACCUMULATED_GENERAL_TIMEOUT: Accumulated general timeout.
16	RWX	ACCUMULATED_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: Accumulated satellite acknowledge access violation.
17	RWX	ACCUMULATED_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: Accumulated satellite acknowledge invalid register.
18	RWX	TRAPPED_PCB_WDATA_PARITY_ERROR: Trapped PCB write data parity error.
19	RWX	TRAPPED_PCB_ADDRESS_PARITY_ERROR: Trapped PCB address parity error.
20	RWX	TRAPPED_DL_RETURN_WDATA_PARITY_ERROR: Trapped DL return write data parity error.
21	RWX	TRAPPED_DL_RETURN_P0_ERROR: Trapped DL return P0 error.
22	RWX	TRAPPED_UL_RDATA_PARITY_ERROR: Trapped UL read data parity error.
23	RWX	TRAPPED_UL_P0_ERROR: Trapped UL P0 error.
24	RWX	TRAPPED_PARITY_ERROR_ON_INTERFACE_MACHINE: Trapped parity error on interface machine.
25	RWX	TRAPPED_PARITY_ERROR_ON_P2S_MACHINE: Trapped parity error on p2s machine.
26	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_ULCCH: Trapped timeout while waiting for ULCCH.
27	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: Trapped timeout while waiting for DLDCH return.
28	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_ULDCH: Trapped timeout while waiting for ULDCH.
29	RWX	TRAPPED_PSCOM_PARALLEL_WRITE_NVLD: Trapped PSCOM parallel write NVLD.
30	RWX	TRAPPED_PSCOM_PARALLEL_READ_NVLD: Trapped PSCOM parallel read NVLD.
31	RWX	TRAPPED_PSCOM_PARALLEL_ADDR_INVALID: Trapped PSCOM parallel address invalid.
32	RWX	TRAPPED_PCB_COMMAND_PARITY_ERROR: Trapped PCB command parity error.
33	RWX	TRAPPED_GENERAL_TIMEOUT: Trapped general timeout.
34	RWX	TRAPPED_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: Trapped satellite acknowledge access violation.
35	RWX	TRAPPED_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: Trapped satellite acknowledge invalid register.

Register Name	PSCOMLE Error Mask Register
Mnemonic	TP.TCEP03.TPCL3.EPS.PSC.PSC.PSCOM_ERROR_MASK
Address	0000000013010002 (SCOM)
Description	This is the parallel-to-serial communication light edition (PSCOMLE) error mask register.

Bits	SCOM	Field Mnemonic: Description
0	RW	MASK_PCB_WDATA_PARITY_ERROR: Mask PCB write data parity error.
1	RW	MASK_PCB_ADDRESS_PARITY_ERROR: Mask PCB address parity error.
2	RW	MASK_DL_RETURN_WDATA_PARITY_ERROR: Mask DL return write data parity error.
3	RW	MASK_DL_RETURN_P0_ERROR: Mask DL return P0 error.
4	RW	MASK_UL_RDATA_PARITY_ERROR: Mask UL read data parity error.
5	RW	MASK_UL_P0_ERROR: Mask UL P0 error.
6	RW	MASK_PARITY_ERROR_ON_INTERFACE_MACHINE: Mask parity error on interface machine.
7	RW	MASK_PARITY_ERROR_ON_P2S_MACHINE: Mask parity error on p2s machine.
8	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_ULCCH: Mask timeout while waiting for ULCCH.
9	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: Mask timeout while waiting for DLDCH return.
10	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_ULDCH: Mask timeout while waiting for ULDCH.
11	RW	MASK_PSCOM_PARALLEL_WRITE_NVLD: Mask PSCOM parallel write NVLD.
12	RW	MASK_PSCOM_PARALLEL_READ_NVLD: Mask PSCOM parallel read NVLD.
13	RW	MASK_PSCOM_PARALLEL_ADDR_INVALID: Mask PSCOM parallel address invalid.
14	RW	MASK_PCB_COMMAND_PARITY_ERROR: Mask PCB command parity error.
15	RW	MASK_GENERAL_TIMEOUT: Mask general timeout.
16	RW	MASK_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: Mask satellite acknowledge access violation.
17	RW	MASK_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: Mask satellite acknowledge invalid register.

Register Name	PSCOMLE Address Trap Register
Mnemonic	TP.TCEP03.TPCL3.EPS.PSC.PSC.ADDR_TRAP_REG
Address	0000000013010003 (SCOM)
Description	This is the parallel-to-serial communication light edition (PSCOMLE) address trap register.

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	PCB_ADDRESS_OF_LAST_TRANSACTION_WITH_ERROR: PCB address of the last transaction with an error.
16	ROX	PCB_READ_NOTWRITE_OF_LAST_TRANSACTION_WITH_ERROR: PCB read, not write, of the last transaction with an error.
17	ROX	RESERVED_ADDR_LAST_TRAP_LT: reserved_0.
18:30	ROX	SERIAL2PARALLEL_STATE_MACHINE_AT_TIME_OF_ERROR: Serial2 parallel state machine at the time of the error.
31	ROX	SATELLITE_ACKNOWLEDGE_BIT_RETURN_PARITY: This bit is set to 1 if no parity error is detected in the satellite number or acknowledgment bits.

Bits	SCOM	Field Mnemonic: Description
32	ROX	SATELLITE_ACKNOWLEDGE_BIT_WRITE_PARITY_ERROR: Set if a write parity error is detected by the satellite.
33	ROX	SATELLITE_ACKNOWLEDGE_BIT_ACCESS_VIOLATION: Set if an invalid read or write access is detected by the satellite.
34	ROX	SATELLITE_ACKNOWLEDGE_BIT_INVALID_REGISTER: Set if an invalid register address is detected by the satellite.

Register Name	Ring Lock Enable Register
Mnemonic	TP.TCEP03.TPCL3.EPS.PSC.PSC.WRITE_PROTECT_ENABLE_REG
Address	0000000013010005 (SCOM)
Description	This register enables the ring lock.

Bits	SCOM	Field Mnemonic: Description
0	RW	ENABLE_RING_LOCKING: General enable of ring locking upon a write to a specific ring.
1	RW	RESERVED_RING_LOCKING: Reserved.

Register Name	Write Protect Rings Register
Mnemonic	TP.TCEP03.TPCL3.EPS.PSC.PSC.WRITE_PROTECT_RINGS_REG
Address	0000000013010006 (SCOM)
Description	This register writes ring protect bit maps.

Bits	SCOM	Field Mnemonic: Description
0:15	RW	WRITE_PROTECT_RINGS: Write a protect bit map for each ring.

Register Name	Atomic Lock Mask Register
Mnemonic	TP.TCEP03.TPCL3.EPS.PSC.PSC.ATOMIC_LOCK_MASK_LATCH_REG
Address	0000000013010007 (SCOM)
Description	This register provides a bit mask for atomic locking.

Bits	SCOM	Field Mnemonic: Description
0:15	RW	ATOMIC_LOCK_MASK: A bit mask for atomic locking on a ring-by-ring basis.

Register Name	Ring Fence Enable Mask Register
Mnemonic	TP.TCEP03.TPCL3.EPS.PSC.PSC.RING_FENCE_MASK_LATCH_REG
Address	0000000013010008 (SCOM)
Description	This register provides a bit mask for ring fencing.

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:15	RW	RING_FENCE_ENABLE_MASK: Enable bit mask for ring fencing on a ring-by-ring basis.

Register Name	Synchronous Configuration Register
Mnemonic	TP.TCEP03.TPCL3.SYNC_CONFIG
Address	0000000013030000 (SCOM)
Description	Configuration of CC counters.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	SYNC_PULSE_DELAY: Delay the incoming synchronous pulse. The default is 8 latches including asynchronous. 0000 = Delay by 8 latches (default). 0001 = Delay by 2 latches. 0010 = Delay by 3 latches. 0011 = Delay by 4 latches. 0100 = Delay by 5 latches. 0101 = Delay by 6 latches. 0110 = Delay by 7 latches. 0111 = Delay by 8 latches. 1000 = Delay by 9 latches. 1001 = Delay by 10 latches. 1010 = Delay by 11 latches. 1011 = Delay by 12 latches. 1100 = Delay by 13 latches. 1101 = Delay by 14 latches. 1110 = Delay by 15 latches. 1111 = Delay by 16 latches.
4	RW	LISTEN_TO_SYNC_PULSE_DIS: Disable phase counter synchronization by sync_pulse signal (default is enabled). **Note:** When listen_to_sync is enabled, the chiplet becomes corrupted for 200 cycles.
5	RW	SYNC_PULSE_INPUT_SEL: The default is 0. When set to 1, the alternative input of the sync_pulse will be used. **Note:** When toggling the input select, the chiplet becomes corrupted for 200 cycles.
6	RW	USE_SYNC_FOR_SCAN: When set, use OPCG initial alignment for scan requests.
7	RW	CLEAR_CHIPLET_IS_ALIGNED: This bit clears the chiplet_is_aligned bit. See the Chiplet Status Register.
8	RW	UNIT_REGION_CLKCMD_ENABLE: Enable the unit interface to start or stop one dedicated region. Used for POWER9 cache/core.
9	RW	DISABLE_PCB_ITR: Disable interrupt generation within CC. Interrupt sent on each HLD event.
10	RW	ENABLE_VITL_ALIGN_CHECK: Enable the VITL align check to compare alignment of incoming synchronous pulse with 2:1 VITL LCB.
11	RW	SYNC_PULSE_OUT_DIS: Disables sync_pulse output when set to 1. The master chiplet will no longer send synchronous pulses to slave chiplets.
12:19	RW	UNUSED1219: Unused.

Register Name	OPCG Alignment Register
Mnemonic	TP.TCEP03.TPCL3.OPCG_ALIGN
Address	0000000013030001 (SCOM)
Description	OPCG alignment

Bits	SCOM	Field Mnemonic: Description
0:3	RW	INOP_ALIGN: INOP phase alignment: 0 = None 1 = 2:1 2 = 3:1 3 = 4:1 4 = 6:1 5 = 8:1 6 = 12:1 7 = 16:1 8 = 24:1 9-15 = 48:1
4:7	RW	SNOP_ALIGN: SNOP phase alignment: 0 = None 1 = 2:1 2 = 3:1 3 = 4:1 4 = 6:1 5 = 8:1 6 = 12:1 7 = 16:1 8 = 24:1 9-15 = 48:1
8:11	RW	ENOP_ALIGN: ENOP phase alignment: 0 = None 1 = 2:1 2 = 3:1 3 = 4:1 4 = 6:1 5 = 8:1 6 = 12:1 7 = 16:1 8 = 24:1 9-15 = 48:1
12:19	RW	INOP_WAIT: INOP cycle delay (0-255).
20:31	RW	SNOP_WAIT: SNOP cycle delay (0-4095).
32:39	RW	ENOP_WAIT: ENOP cycle delay (0-255).
40	RW	INOP_FORCE_SG: Set SG high during INOP.
41	RW	SNOP_FORCE_SG: Set SG high during SNOP.
42	RW	ENOP_FORCE_SG: Set SG high during ENOP (including LOOP phase).
43	RW	NO_WAIT_ON_CLK_CMD: 0 = A clock change request will first wait the OPCG_WAIT cycles. 1 = A clock change request will not wait, when not in flush.
44:45	RW	ALIGN_SOURCE_SELECT: 0: 0 = Use inopa setting from opcg_reg0. 1 = Use rising edge of synchronous pulse. 2 = Use unit0_sync_lvl to align (for AVP: refresh0). 3 = Use unit1_sync_lvl to align (for AVP: refresh1).

Bits	SCOM	Field Mnemonic: Description
46	RW	UNUSED46: Unused.
47:51	RW	SCAN_RATIO: Scan ratio. The default is 4:1 = 00011. 0 to 15 = (n+1):1 16 = 24:1 17 = 32:1 18 = 48:1 19 = 64:1 20 = 128:1
52:63	RW	OPCG_WAIT_CYCLES: Old PAD value; delay at the beginning and end of the OPCG run, to allow DC signals to be there at the right time (0-4095). The default is 0x020. **Note:** Must be higher than plat depth.

Register Name	**OPCG Control 0 Register**
Mnemonic	TP.TCEP03.TPCL3.OPCG_REG0
Address	0000000013030002 (SCOM)
Description	OPCG control register 0

Bits	SCOM	Field Mnemonic: Description
0	RW	RUNN_MODE: 0 = BIST-mode; used for LBIST. 1 = RUNN-mode; used for ABIST/IOBIST.
1	RWX	OPCG_GO: Start OPCG. The bit is cleared when OPCG completes. Poll for opcg_done in the Chiplet Status Register.
2	RWX	RUN_SCAN0: Run scan0 (overrides all BIST mode settings but the scan_ratio). Starts a scan0 run, and the bit is cleared when OPCG is done. Poll for opcg_done in the Chiplet Status Register.
3	RW	SCAN0_MODE: Sets PRPGs in scan0_mode but does not run the automatic scan0 sequence.
4	RWX	OPCG_IN_SLAVE_MODE: When selected, OPCG waits for the master chiplet to get started. When Keep_MS_Mode is 0, SLAVE_MODE is cleared after the incoming trigger.
5	RWX	OPCG_IN_MASTER_MODE: When selected, OPCG sends out a trigger to all slave chiplets. When Keep_MS_Mode is 0, MASTER_MODE is cleared after sending out one master trigger.
6	RW	KEEP_MS_MODE: When set to 1, OPCG in master and slave mode bits are not cleared after one incoming OPCG trigger. The default is to clear master and slave mode bits.
7	RW	TRIGGER_OPCG_ON_UNIT0_SYNC_LVL: Unit pin used for AVP can trigger OPCG (unit0_sync_lvl).
8	RW	TRIGGER_OPCG_ON_UNIT1_SYNC_LVL: Unit pin used for AVP can trigger OPCG (unit1_sync_lvl).
9	RWX	RUN_CHIPLET_SCAN0: Run scan0 on all regions and types, will clear the chiplet at all.
10	RWX	RUN_CHIPLET_SCAN0_NO_PLL: Run scan0 on all regions and types; clears the chiplet at all exclude-PLL regions. PLL can continue to run.
11	RW	RUN_OPCG_ON_UPDATE_DR: Start the OPCG engine when scan update (update_dr) is received (set pulse). Cronus requires this bit to be set at 1 for a set pulse WRITE.
12	RW	RUN_OPCG_ON_CAPTURE_DR: Start the OPCG engine when scan update (capture_dr) is received (set pulse). Cronus requires this bit to be set at 1 for a set pulse READ.
13	RW	STOP_RUNN_ON_XSTOP: RUNN mode. Stops RUNN on checkstop.
14	RW	OPCG_STARTS_BIST: RUNN mode. The OPCG engine controls start_bist for ABIST or IOBIST (see the BIST Register).
15:20	RW	UNUSED1520: Unused.

Bits	SCOM	Field Mnemonic: Description
21:63	RWX	LOOP_COUNT: Loop counter for LBIST and RUNN. write = Target value. read = Current counter value. Counts from 0 to the target value.

Register Name	OPCG Control 1 Register
Mnemonic	TP.TCEP03.TPCL3.OPCG_REG1
Address	0000000013030003 (SCOM)
Description	OPCG Control Register 1

Bits	SCOM	Field Mnemonic: Description
0:11	RW	SCAN_COUNT: BIST mode: Channel scan count (s = 0-4095) RUNN-mode: start_bist match value (0:11)
12:23	RW	MISR_A_VAL: BIST mode: a value for MISR aperture RUNN-mode: start_bist match value (12:23)
24:35	RW	MISR_B_VAL: BIST mode: b value for MISR aperture RUNN-mode: start_bist match value (24:35)
36:47	RW	MISR_INIT_WAIT: BIST mode: delay MISR aperture; MISRs become active after this number of loops.
48	RW	OPCG_SUPPRESS_EVEN_CLK: OPCG creates only even, and not odd, clocks. Used for RUNN to create only one clock in fast domain. The default is 0.
49	RW	SCAN_CLK_USE_EVEN: Generate scan clock in an even cycle instead of an odd cycle. The default is 0 (odd cycle).
50:51	RW	UNUSED2: Unused.
52	RW	RTIM_THOLD_FORCE: Force rtim_thold low when not in test_dc mode (must be 0 at all times).
53	RW	DISABLE_ARY_CLK_DURING_FILL: LBIST and SCAN0. Prevent the firing of the ARY HLD bit during NSL fill.
54	RW	SG_HIGH_DURING_FILL: LBIST and SCAN0. Hold SG high during NSL fill.
55:56	RW	LBIST_SKITTER_CTL: BIST mode: 00 = Enable skitter during lbist_ip 01 = Enable skitter when misr_active; see misr_init_wait 10 = Skitter OPCG_GO mode; falling edge = start, rising edge = stop 11 = Unused
57	RW	MISR_MODE: BIST mode. MISR aperture mode (0: a-1 to b-1, 1: Start to a and b to end).
58	RW	INFINITE_MODE: Infinite mode. RUNN and LBIST will run indefinitely and ignore the loop count.
59:63	RW	NSL_FILL_COUNT: BIST mode. NSL-fill count (0-31).

Register Name	OPCG Control 2 Register
Mnemonic	TP.TCEP03.TPCL3.OPCG_REG2
Address	0000000013030004 (SCOM)
Description	OPCG control register 2

Bits	SCOM	Field Mnemonic: Description
0	RWX	OPCG_GO2: Start OPCG for broadcast sequences (start sequence).
1:3	RW	PRPG_WEIGHTING: prpg_activate: 1/2, 1/4, 1/8, 1/16, 1/2, 3/4, 7/8, 15/16.
4:15	RWX	PRPG_VALUE: Set to 0 to keep PRPG always on, else seed.
16:27	RW	PRPG_A_VAL: a value for PRPG aperture.
28:39	RW	PRPG_B_VAL: b value for PRPG aperture.
40	RW	PRPG_MODE: PRPG aperture mode (0: a-1 to b-1, 1: Start to a and b to end).
41:63	RW	UNUSED41_63: Unused.

Register Name	**Scan Region and Type Register**
Mnemonic	TP.TCEP03.TPCL3.SCAN_REGION_TYPE
Address	0000000013030005 (SCOM)
Description	Sets the scan region and type.

Bits	SCOM	Field Mnemonic: Description
0	RWX	SYSTEM_FAST_INIT: Default is 0. When set to 1, the MASK bits in the CMSK chain govern which part will be scanned or scan0. MASK = 1: scan0. MASK = 0: Partial or scan chain.
1:2	RO	constant = 0b00
3	NCX	SCAN_REGION_VITL: Scan clock region vitl (vital = clock).
4	RWX	SCAN_REGION_PERV: Scan clock region perv (pervasive).
5	RWX	SCAN_REGION_UNIT1: Scan clock region eqpb (PB).
6	RWX	SCAN_REGION_UNIT2: Scan clock region l30 (L3, NC).
7	RWX	SCAN_REGION_UNIT3: Scan clock region l31 (L3, NC).
8	RWX	SCAN_REGION_UNIT4: Scan clock region l20 (L2, CC).
9	RWX	SCAN_REGION_UNIT5: Scan clock region l21 (L2, CC).
10	RWX	SCAN_REGION_UNIT6: Scan clock region anep, e9_an (iVRM, VDM, DCC, SKEW).
11	RWX	SCAN_REGION_UNIT7: Scan clock region pbieq (PB).
12	RWX	SCAN_REGION_UNIT8: Scan clock region refr0 (L3).
13	RWX	SCAN_REGION_UNIT9: Scan clock region refr1 (L3).
14	RWX	SCAN_REGION_UNIT10: Scan clock region dpll (CLK).
15:47	RO	constant = 0b000000000000000000000000000000000
48	RW	SCAN_TYPE_FUNC: Scan chain func (functional).
49	RW	SCAN_TYPE_CFG: Scan chain mode (boot configuration and debug configuration).
50	RW	SCAN_TYPE_CCFG_GPTR: Scan chain ccfg / gptr (pervasive: CC configuration; others: GPTR).
51	RW	SCAN_TYPE_REGF: Scan chain regf (register files).
52	RW	SCAN_TYPE_LBIST: Scan chain lbst (LBIST).
53	RW	SCAN_TYPE_ABIST: Scan chain abst (ABIST).
54	RW	SCAN_TYPE_REPR: Scan chain repr (array repair).
55	RW	SCAN_TYPE_TIME: Scan chain time (array timing).

Bits	SCOM	Field Mnemonic: Description
56	RW	SCAN_TYPE_BNDY: Scan chain bndy (boundary IOs).
57	RW	SCAN_TYPE_FARR: Scan chain farr (fast array unload).
58	RW	SCAN_TYPE_CMSK: Scan chain cmsk (LBIST channel mask).
59	RW	SCAN_TYPE_INEX: Scan chain idex (c14 ASIC).
60:63	RO	constant = 0b0000

Register Name	Clock Region Register
Mnemonic	TP.TCEP03.TPCL3.CLK_REGION
Address	0000000013030006 (SCOM)
Description	Start and stop clocks.

Bits	SCOM	Field Mnemonic: Description
0:1	RWX	CLOCK_CMD: Command for clock control: 00 = NOP 01 = Start 10 = Stop 11 = Pulse (one pulse)
2	RWX	SLAVE_MODE: When selected, the clock command waits for the master chiplet to start. The bit is cleared after the incoming slave trigger and Keep_MS_Mode_after_trigger is set to 0.
3	RWX	MASTER_MODE: When selected, the clock command sends out a trigger to all slave chiplets. The bit is cleared after sending out one master trigger and Keep_MS_Mode_after_trigger is set to 0.
4	RWX	CLOCK_REGION_PERV: For clock region perv (pervasive).
5	RWX	CLOCK_REGION_UNIT1: For clock region eqpb (PB).
6	RWX	CLOCK_REGION_UNIT2: For clock region l30 (L3, NC).
7	RWX	CLOCK_REGION_UNIT3: For clock region l31 (L3, NC).
8	RWX	CLOCK_REGION_UNIT4: For clock region l20 (L2, CC).
9	RWX	CLOCK_REGION_UNIT5: For clock region l21 (L2, CC).
10	RWX	CLOCK_REGION_UNIT6: For clock region anep, e9_an (iVRM, VDM, DCC, SKEW).
11	RWX	CLOCK_REGION_UNIT7: For clock region pbieq (PB).
12	RWX	CLOCK_REGION_UNIT8: For clock region refr0 (L3).
13	RWX	CLOCK_REGION_UNIT9: For clock region refr1 (L3).
14	RWX	CLOCK_REGION_UNIT10: For clock region dpll (CLK).
15:47	RO	constant = 0b000000000000000000000000000000000
48	RWX	SEL_THOLD_SL: Select SL tholds.
49	RWX	SEL_THOLD_NSL: Select NSL tholds.
50	RWX	SEL_THOLD_ARY: Select array thold.
51	RO	constant = 0b0
52	RW	CLOCK_PULSE_USE_EVEN: For dual mesh support. The default for pulse is ODD phase; when this bit is set, pulse is applied on EVEN phase.
53:63	RO	constant = 0b00000000000

Register Name	Clock Status SL Register
Mnemonic	TP.TCEP03.TPCL3.CLOCK_STAT_SL
Address	0000000013030008 (SCOM)
Description	Clocks running SL

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b1111
4	ROX	CLOCK_STATUS_PERV_SL: Status of perv (SL, HLD). 0 = Run. 1 = Stop.
5	ROX	CLOCK_STATUS_UNIT1_SL: Status of eqpb (PB, SL, HLD). 0 = Run. 1 = Stop.
6	ROX	CLOCK_STATUS_UNIT2_SL: Status of l30 (L3, NC, SL, HLD). 0 = Run. 1 = Stop.
7	ROX	CLOCK_STATUS_UNIT3_SL: Status of l31 (L3, NC, SL, HLD). 0 = Run. 1 = Stop.
8	ROX	CLOCK_STATUS_UNIT4_SL: Status of l20 (L2, CC, SL, HLD). 0 = Run. 1 = Stop.
9	ROX	CLOCK_STATUS_UNIT5_SL: Status of l21 (L2, CC, SL, HLD). 0 = Run. 1 = Stop.
10	ROX	CLOCK_STATUS_UNIT6_SL: Status of anep, e9_an (iVRM, VDM, DCC, SKEW, SL, HLD). 0 = Run. 1 = Stop.
11	ROX	CLOCK_STATUS_UNIT7_SL: Status of pbieq (PB, SL, HLD). 0 = Run. 1 = Stop.
12	ROX	CLOCK_STATUS_UNIT8_SL: Status of refr0 (L3, SL, HLD). 0 = Run. 1 = Stop.
13	ROX	CLOCK_STATUS_UNIT9_SL: Status of refr1 (L3, SL, HLD). 0 = Run. 1 = Stop.
14	ROX	CLOCK_STATUS_UNIT10_SL: Status of dpll (CLK, SL, HLD). 0 = Run. 1 = Stop.
15:63	RO	constant = 0b1111111111111111111111111111111111111111111111111

Register Name	Clock Status NLS Register
Mnemonic	TP.TCEP03.TPCL3.CLOCK_STAT_NSL
Address	0000000013030009 (SCOM)
Description	Clocks running NSL

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b1111
4	ROX	CLOCK_STATUS_PERV_NSL: Status of perv (SL, HLD). 0 = Run. 1 = Stop.
5	ROX	CLOCK_STATUS_UNIT1_NSL: Status of eqpb (PB, NSL, HLD). 0 = Run. 1 = Stop.
6	ROX	CLOCK_STATUS_UNIT2_NSL: Status of l30 (L3, NC, NSL, HLD). 0 = Run. 1 = Stop.
7	ROX	CLOCK_STATUS_UNIT3_NSL: Status of l31 (L3, NC, NSL, HLD). 0 = Run. 1 = Stop.
8	ROX	CLOCK_STATUS_UNIT4_NSL: Status of l20 (L2, CC, NSL, HLD). 0 = Run. 1 = Stop.
9	ROX	CLOCK_STATUS_UNIT5_NSL: Status of l21 (L2, CC, NSL, HLD). 0 = Run. 1 = Stop.
10	ROX	CLOCK_STATUS_UNIT6_NSL: Status of anep - e9_an (iVRM, VDM, DCC, SKEW, NSL, HLD). 0 = Run. 1 = Stop.
11	ROX	CLOCK_STATUS_UNIT7_NSL: Status of pbieq (PB, NSL, HLD). 0 = Run. 1 = Stop.
12	ROX	CLOCK_STATUS_UNIT8_NSL: Status of refr0 (L3, NSL, HLD). 0 = Run. 1 = Stop.
13	ROX	CLOCK_STATUS_UNIT9_NSL: Status of refr1 (L3, NSL, HLD). 0 = Run. 1 = Stop.
14	ROX	CLOCK_STATUS_UNIT10_NSL: Status of dpll (CLK, NSL, HLD). 0 = Run. 1 = Stop.
15:63	RO	constant = 0b1111111111111111111111111111111111111111111111111

Register Name	Clock Status ARY Register
Mnemonic	TP.TCEP03.TPCL3.CLOCK_STAT_ARY
Address	000000001303000A (SCOM)
Description	Clocks running ARY

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b1111
4	ROX	CLOCK_STATUS_PERV_ARY: Status of perv (ARY, HLD). 0 = Run. 1 = Stop.

Bits	SCOM	Field Mnemonic: Description
5	ROX	CLOCK_STATUS_UNIT1_ARY: Status of eqpb (PB, ARY, HLD). 0 = Run. 1 = Stop.
6	ROX	CLOCK_STATUS_UNIT2_ARY: Status of l30 (L3, NC, ARY, HLD). 0 = Run. 1 = Stop.
7	ROX	CLOCK_STATUS_UNIT3_ARY: Status of l31 (L3, NC, ARY, HLD). 0 = Run. 1 = Stop.
8	ROX	CLOCK_STATUS_UNIT4_ARY: Status of l20 (L2, CC, ARY, HLD). 0 = Run. 1 = Stop.
9	ROX	CLOCK_STATUS_UNIT5_ARY: Status of l21 (L2, CC, ARY, HLD). 0 = Run. 1 = Stop.
10	ROX	CLOCK_STATUS_UNIT6_ARY: Status of anep - e9_an (iVRM, VDM, DCC, SKEW, ARY, HLD). 0 = Run. 1 = Stop.
11	ROX	CLOCK_STATUS_UNIT7_ARY: Status of pbieq (PB, ARY, HLD). 0 = Run. 1 = Stop.
12	ROX	CLOCK_STATUS_UNIT8_ARY: Status of refr0 (L3, ARY, HLD). 0 = Run. 1 = Stop.
13	ROX	CLOCK_STATUS_UNIT9_ARY: Status of refr1 (L3, ARY, HLD). 0 = Run. 1 = Stop.
14	ROX	CLOCK_STATUS_UNIT10_ARY: Status of dpll (CLK, ARY, HLD). 0 = Run. 1 = Stop.
15:63	RO	constant = 0b1111111111111111111111111111111111111111111111111

Register Name	BIST Register
Mnemonic	TP.TCEP03.TPCL3.BIST
Address	000000001303000B (SCOM)
Description	ABIST and IOBIST per region

Bits	SCOM	Field Mnemonic: Description
0	RW	TC_BIST_START_TEST_DC: Keep this field set at 0 during ABIST/IOBIST. It could be used to bypass the RUNN start. When this bit is set, the BIST_START_TEST will go high immediately without waiting for RUNN. BIST will start with the first HLD clock cycle.
1	RW	TC_SRAM_ABIST_MODE_DC: Select the ABIST engines for SRAMs.
2	RW	TC_EDRAM_ABIST_MODE_DC: Select the ABIST engines for eDRAMs.
3	RW	TC_IOBIST_MODE_DC: Select the IOBIST engines.
4	RW	BIST_PERV: Region perv: 1 = BIST_START_TEST for this region is triggered. 0 = The region is not part of the ABIST/IOBIST run.

Bits	SCOM	Field Mnemonic: Description
5	RW	BIST_UNIT1: Region eqpb (PB): 1 = BIST_START_TEST for this region is triggered. 0 = The region is not part of the ABIST/IOBIST run.
6	RW	BIST_UNIT2: Region l30 (L3, NC): 1 = BIST_START_TEST for this region is triggered. 0 = The region is not part of the ABIST/IOBIST run.
7	RW	BIST_UNIT3: Region l31 (L3, NC): 1 = BIST_START_TEST for this region is triggered. 0 = The region is not part of the ABIST/IOBIST run.
8	RW	BIST_UNIT4: Region l20 (L2, CC): 1 = BIST_START_TEST for this region is triggered. 0 = The region is not part of the ABIST/IOBIST run.
9	RW	BIST_UNIT5: Region l21 (L2, CC): 1 = BIST_START_TEST for this region is triggered. 0 = The region is not part of the ABIST/IOBIST run.
10	RW	BIST_UNIT6: Region anep - e9_an (iVRM, VDM, DCC, SKEW): 1 = BIST_START_TEST for this region is triggered. 0 = The region is not part of the ABIST/IOBIST run.
11	RW	BIST_UNIT7: Region pbieq (PB): 1 = BIST_START_TEST for this region is triggered. 0 = The region is not part of the ABIST/IOBIST run.
12	RW	BIST_UNIT8: Region refr0 (L3): 1 = BIST_START_TEST for this region is triggered. 0 = The region is not part of the ABIST/IOBIST run.
13	RW	BIST_UNIT9: Region refr1 (L3): 1 = BIST_START_TEST for this region is triggered. 0 = The region is not part of the ABIST/IOBIST run.
14	RW	BIST_UNIT10: Region dpll (CLK): 1 = BIST_START_TEST for this region is triggered. 0 = The region is not part of the ABIST/IOBIST run.
15:47	RO	constant = 0b000000000000000000000000000000000
48	RW	BIST_STROBE_WINDOW_EN: Enable strobe window only in TE = 1 mode. The OPCGGO tester pin enables the ABIST compare, once ABIST has been started. Special setup in the ABIST engine is required. The default is 0. System mode cannot enable this feature.
49:63	RO	constant = 0b000000000000000

Register Name	Checkstop 1 Register
Mnemonic	TP.TCEP03.TPCL3.XSTOP1
Address	000000001303000C (SCOM)
Description	Checkstop per region

Bits	SCOM	Field Mnemonic: Description
0	RW	XSTOP1_MASK_B: mask for checkstop to clockstop of select regions (see xstop_perv,xstop_unit0..n), 0 = Ignore checkstop. 1= Stop on checkstop.
1	RW	XSTOP1_UNUSED: Unused.
2	RW	TRIGGER_OPCG_ON_XSTOP1: Trigger OPCG on checkstop instead of performing clockstop.

Bits	SCOM	Field Mnemonic: Description
3	RW	XSTOP1_WAIT_ALLWAYS: When set to 1, checkstop waits independently of flush. The default is to not wait when flush is not set.
4	RW	XSTOP1_PERV: Region perv: 1 = The region is stopped. 0 = The region continues to run on checkstop.
5	RW	XSTOP1_UNIT1: Region eqpb (PB): 1 = The region is stopped. 0 = The region continues to run on checkstop.
6	RW	XSTOP1_UNIT2: Region l30 (L3, NC): 1 = The region is stopped. 0 = The region continues to run on checkstop.
7	RW	XSTOP1_UNIT3: Region l31 (L3, NC): 1 = The region is stopped. 0 = The region continues to run on checkstop.
8	RW	XSTOP1_UNIT4: Region l20 (L2, CC): 1 = The region is stopped. 0 = The region continues to run on checkstop.
9	RW	XSTOP1_UNIT5: Region l21 (L2, CC): 1 = The region is stopped. 0 = The region continues to run on checkstop.
10	RW	XSTOP1_UNIT6: Region anep - e9_an (iVRM, VDM, DCC, SKEW): 1 = The region is stopped. 0 = The region continues to run on checkstop.
11	RW	XSTOP1_UNIT7: Region pbieq (PB): 1 = The region is stopped. 0 = The region continues to run on checkstop.
12	RW	XSTOP1_UNIT8: Region refr0 (L3): 1 = The region is stopped. 0 = The region continues to run on checkstop.
13	RW	XSTOP1_UNIT9: Region refr1 (L3): 1 = The region is stopped. 0 = The region continues to run on checkstop.
14	RW	XSTOP1_UNIT10: Region dpll (CLK): 1 = The region is stopped. 0 = The region continues to run on checkstop.
15:47	RO	constant = 0b000000000000000000000000000000000
48:59	RW	XSTOP1_WAIT_CYCLES: Specifies how many cycles checkstop waits (0 - 4095) after dropping flush before tholds are dropped.
60:63	RO	constant = 0b0000

Register Name	Checkstop 2 Register
Mnemonic	TP.TCEP03.TPCL3.XSTOP2
Address	000000001303000D (SCOM)
Description	Checkstop per region

Bits	SCOM	Field Mnemonic: Description
0	RW	XSTOP2_MASK_B: Mask for checkstop to clockstop of select regions (see xstop_perv, xstop_unit0..n). 0 = Ignore checkstop 1 = Stop on checkstop
1	RW	XSTOP2_UNUSED: Unused.
2	RW	TRIGGER_OPCG_ON_XSTOP2: Trigger OPCG on checkstop instead of performing clockstop.
3	RW	XSTOP2_WAIT_ALLWAYS: When set to 1, checkstop waits independently of flush. The default is to not wait when flush is not set.
4	RW	XSTOP2_PERV: Region perv: 1 = The region is stopped. 0 = The region continues to run on checkstop.
5	RW	XSTOP2_UNIT1: Region eqpb (PB): 1 = The region is stopped. 0 = The region continues to run on checkstop.
6	RW	XSTOP2_UNIT2: Region l30 (L3, NC): 1 = The region is stopped. 0 = The region continues to run on checkstop.
7	RW	XSTOP2_UNIT3: Region l31 ()l3, nc: 1 = The region is stopped. 0 = The region continues to run on checkstop.
8	RW	XSTOP2_UNIT4: Region l20 (L2, CC): 1 = The region is stopped. 0 = The region continues to run on checkstop.
9	RW	XSTOP2_UNIT5: Region l21 (L2, CC): 1 = The region is stopped. 0 = The region continues to run on checkstop.
10	RW	XSTOP2_UNIT6: Region anep - e9_an (iVRM, VDM, DCC, SKEW): 1 = The region is stopped. 0 = The region continues to run on checkstop.

Bits	SCOM	Field Mnemonic: Description
11	RW	XSTOP2_UNIT7: Region pbieq (PB): 1 = The region is stopped. 0 = The region continues to run on checkstop.
12	RW	XSTOP2_UNIT8: Region refr0 (L3): 1 = The region is stopped. 0 = The region continues to run on checkstop.
13	RW	XSTOP2_UNIT9: Region refr1 (L3): 1 = The region is stopped. 0 = The region continues to run on checkstop.
14	RW	XSTOP2_UNIT10: Region dpll (CLK): 1 = The region is stopped. 0 = The region continues to run on checkstop.
15:47	RO	constant = 0b000000000000000000000000000000000
48:59	RW	XSTOP2_WAIT_CYCLES: Specifies how many cycles checkstop waits (0 - 4095) after dropping flush before tholds are dropped.
60:63	RO	constant = 0b0000

Register Name	Checkstop 3 Register
Mnemonic	TP.TCEP03.TPCL3.XSTOP3
Address	000000001303000E (SCOM)
Description	Checkstop per region

Bits	SCOM	Field Mnemonic: Description
0	RW	XSTOP3_MASK_B: Mask for checkstop to clockstop of select regions. (See xstop_perv, xstop_unit0..n). 0 = Ignore checkstop. 1 = Stop on checkstop.
1	RW	XSTOP3_UNUSED: Unused.
2	RW	TRIGGER_OPCG_ON_XSTOP3: Trigger OPCG on checkstop instead of performing clockstop.
3	RW	XSTOP3_WAIT_ALLWAYS: When set to 1, checkstop waits independently of flush. The default is to not wait when flush is not set.
4	RW	XSTOP3_PERV: Region perv: 1 = The region is stopped. 0 = The region continues to run on checkstop.
5	RW	XSTOP3_UNIT1: Region eqpb (PB): 1 = The region is stopped. 0 = The region continues to run on checkstop.
6	RW	XSTOP3_UNIT2: Region l30 (L3, NC): 1 = The region is stopped. 0 = The region continues to run on checkstop.
7	RW	XSTOP3_UNIT3: Region l31 (L3, NC): 1 = The region is stopped. 0 = The region continues to run on checkstop.
8	RW	XSTOP3_UNIT4: Region l20 (L2, CC): 1 = The region is stopped. 0 = The region continues to run on checkstop.
9	RW	XSTOP3_UNIT5: Region l21 (L2, CC): 1 = The region is stopped. 0 = The region continues to run on checkstop.

Bits	SCOM	Field Mnemonic: Description
10	RW	XSTOP3_UNIT6: Region anep - e9_an (iVRM, VDM, DCC, SKEW): 1 = The region is stopped. 0 = The region continues to run on checkstop.
11	RW	XSTOP3_UNIT7: Region pbieq (PB): 1 = The region is stopped. 0 = The region continues to run on checkstop.
12	RW	XSTOP3_UNIT8: Region refr0 (L3): 1 = The region is stopped. 0 = The region continues to run on checkstop.
13	RW	XSTOP3_UNIT9: Region refr1 (L3): 1 = The region is stopped. 0 = The region continues to run on checkstop.
14	RW	XSTOP3_UNIT10: Region dpll (CLK): 1 = The region is stopped. 0 = The region continues to run on checkstop.
15:47	RO	constant = 0b000000000000000000000000000000000
48:59	RW	XSTOP3_WAIT_CYCLES: Specifies how many cycles checkstop waits (0 - 4095) after dropping flush before tholds are dropped.
60:63	RO	constant = 0b0000

Register Name	Error Status Register
Mnemonic	TP.TCEP03.TPCL3.ERROR_STATUS
Address	000000001303000F (SCOM)
Description	Error status of CC

Bits	SCOM	Field Mnemonic: Description
0	RWX	PCB_WRITE_NOT_ALLOWED_ERR: A write was attempted on a read only register.
1	RWX	PCB_READ_NOT_ALLOWED_ERR: A read is not allowed; the register might be write only.
2	RWX	PCB_PARITY_ON_CMD_ERR: A parity error on the command.
3	RWX	PCB_ADDRESS_NOT_VALID_ERR: Invalid address.
4	RWX	PCB_PARITY_ON_ADDR_ERR: Parity error on the address.
5	RWX	PCB_PARITY_ON_DATA_ERR: Parity error on data.
6	RWX	PCB_PROTECTED_ACCESS_INVALID_ERR: Protection violation.
7	RWX	PCB_PARITY_ON_SPCIF_ERR: Parity error on spcif.
8	RWX	PCB_WRITE_AND_OPCG_IP_ERR: A PCB write was attempted while OPCG is running.
9	RWX	SCAN_READ_AND_OPCG_IP_ERR: A scan read was attempted while OPCG is running.
10	RWX	CLOCK_CMD_CONFLICT_ERR: A clock command is in progress.
11	RWX	SCAN_COLLISION_ERR: Scan region was selected on a running region.
12	RWX	PREVENTED_SCAN_COLLISION_ERR: PCB request to set a scan region that is running.
13	RWX	OPCG_TRIGGER_ERR: OPCG was triggered while OPCG is running.
14	RWX	PHASE_CNT_CORRUPTION_ERR: The phase counters inside the chiplet are out of sync.
15	RWX	CLOCK_CMD_PREVENTED_ERR: Security or scan collision prevented a clock start.
16	RWX	PARITY_ON_OPCG_SM_ERR: Parity error on the OPCG state machine.

Bits	SCOM	Field Mnemonic: Description
17	RWX	PARITY_ON_CLOCK_MUX_REG_ERR: Parity error on scan/clock region/type or clock status register.
18	RWX	PARITY_ON_OPCG_REG_ERR: Parity error on OPCG registers.
19	RWX	PARITY_ON_SYNC_CONFIG_REG_ERR: Parity error on synchronization configuration register.
20	RWX	PARITY_ON_XSTOP_REG_ERR: Parity error on checkstop register.
21	RWX	PARITY_ON_GPIO_REG_ERR: Parity error on GP0,4,5,6 registers.
22	RWX	CLKCMD_REQUEST_ERR: Region clkcmd has one request pending but received a second one.
23	RWX	CBS_PROTOCOL_ERR: CBS protocol error. The REQ / ACK sequence is wrong.
24	RWX	VITL_ALIGN_ERR: VITL alignment is out of sync to sync pulse.
25	RWX	UNIT_SYNC_LVL_ERR: Unit0 and Unit1 sync lvl pulse are not in sync. AVP is broken.
26	RWX	PARITY_ON_SELFBOOT_CMD_STATE_ERR: Parity error on selfboot cmd state.
27	RWX	UNUSED_ERROR27: Unused.
28	RWX	UNUSED_ERROR28: Unused.
29	RWX	UNUSED_ERROR29: Unused.
30	RWX	UNUSED_ERROR30: Unused.
31	RWX	UNUSED_ERROR31: Unused.

Register Name	OPCG Capture 1 Register
Mnemonic	TP.TCEP03.TPCL3.OPCG_CAPT1
Address	0000000013030010 (SCOM)
Description	OPCG capture 1 control.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	COUNT: 0000 = 12 cycles 0001 – 1100 = Cycles 1-12 1101-1111 = 24 cycles for normal, slow regions
4:8	RW	SEQ_01: Sequence cycle 1 for normal/slow region (SL, NSL, ARY, SE, FCE).
9:13	RW	SEQ_02: Sequence cycle 2 for normal/slow region (SL, NSL, ARY, SE, FCE).
14:18	RW	SEQ_03: Sequence cycle 3 for normal/slow region (SL, NSL, ARY, SE, FCE).
19:23	RW	SEQ_04: Sequence cycle 4 for normal/slow region (SL, NSL, ARY, SE, FCE).
24:28	RW	SEQ_05: Sequence cycle 5 for normal/slow region (SL, NSL, ARY, SE, FCE).
29:33	RW	SEQ_06: Sequence cycle 6 for normal/slow region (SL, NSL, ARY, SE, FCE).
34:38	RW	SEQ_07: Sequence cycle 7 for normal/slow region (SL, NSL, ARY, SE, FCE).
39:43	RW	SEQ_08: Sequence cycle 8 for normal/slow region (SL, NSL, ARY, SE, FCE).
44:48	RW	SEQ_09: Sequence cycle 9 for normal/slow region (SL, NSL, ARY, SE, FCE).
49:53	RW	SEQ_10: Sequence cycle 10 for normal/slow region (SL, NSL, ARY, SE, FCE).
54:58	RW	SEQ_11: Sequence cycle 11 for normal/slow region (SL, NSL, ARY, SE, FCE).
59:63	RW	SEQ_12: Sequence cycle 12 for normal/slow region (SL, NSL, ARY, SE, FCE).

Register Name	OPCG Capture 2 Register
Mnemonic	TP.TCEP03.TPCL3.OPCG_CAPT2
Address	0000000013030011 (SCOM)
Description	OPCG control capture 2.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	UNUSED_CAPT2:
4:8	RW	SEQ_13_01EVEN: Sequence cycle 1 is even for fast region or cycle 13 for normal region (SL, NSL, ARY, SE, FCE).
9:13	RW	SEQ_14_01ODD: Sequence cycle 1 is odd for fast region or cycle 14 for normal region (SL, NSL, ARY, SE, FCE).
14:18	RW	SEQ_15_02EVEN: Sequence cycle 2 is even for fast region or cycle 15 for normal region (SL, NSL, ARY, SE, FCE).
19:23	RW	SEQ_16_02ODD: Sequence cycle 2 is odd for fast region or cycle 16 for normal region (SL, NSL, ARY, SE, FCE).
24:28	RW	SEQ_17_03EVEN: Sequence cycle 3 is even for fast region or cycle 17 for normal region (SL, NSL, ARY, SE, FCE).
29:33	RW	SEQ_18_03ODD: Sequence cycle 3 is odd for fast region or cycle 18 for normal region (SL, NSL, ARY, SE, FCE).
34:38	RW	SEQ_19_04EVEN: Sequence cycle 4 is even for fast region or cycle 19 for normal region (SL, NSL, ARY, SE, FCE).
39:43	RW	SEQ_20_04ODD: Sequence cycle 4 is odd for fast region or cycle 20 for normal region (SL, NSL, ARY, SE, FCE).
44:48	RW	SEQ_21_05EVEN: Sequence cycle 5 is even for fast region or cycle 21 for normal region (SL, NSL, ARY, SE, FCE).
49:53	RW	SEQ_22_05ODD: Sequence cycle 5 is odd for fast region or cycle 22 for normal region (SL, NSL, ARY, SE, FCE).
54:58	RW	SEQ_23_06EVEN: Sequence cycle 6 is even for fast region or cycle 23 for normal region (SL, NSL, ARY, SE, FCE).
59:63	RW	SEQ_24_06ODD: Sequence cycle 6 is odd for fast region or cycle 24 for normal region (SL, NSL, ARY, SE, FCE).

Register Name	OPCG Capture 3 Register
Mnemonic	TP.TCEP03.TPCL3.OPCG_CAPT3
Address	0000000013030012 (SCOM)
Description	OPCG control capture 3.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	UNUSED_CAPT3:
4:8	RW	SEQ_07EVEN: Sequence cycle 7 is even for fast region (SL, NSL, ARY, SE, FCE).
9:13	RW	SEQ_07ODD: Sequence cycle 7 is odd for fast region (SL, NSL, ARY, SE, FCE).
14:18	RW	SEQ_08EVEN: Sequence cycle 8 is even for fast region (SL, NSL, ARY, SE, FCE).
19:23	RW	SEQ_08ODD: Sequence cycle 8 is odd for fast region (SL, NSL, ARY, SE, FCE).
24:28	RW	SEQ_09EVEN: Sequence cycle 9 is even for fast region (SL, NSL, ARY, SE, FCE).
29:33	RW	SEQ_09ODD: Sequence cycle 9 is odd for fast region (SL, NSL, ARY, SE, FCE).

Bits	SCOM	Field Mnemonic: Description
34:38	RW	SEQ_10EVEN: Sequence cycle 10 is even for fast region (SL, NSL, ARY, SE, FCE).
39:43	RW	SEQ_10ODD: Sequence cycle 10 is odd for fast region (SL, NSL, ARY, SE, FCE).
44:48	RW	SEQ_11EVEN: Sequence cycle 11 is even for fast region (SL, NSL, ARY, SE, FCE).
49:53	RW	SEQ_11ODD: Sequence cycle 11 is odd for fast region (SL, NSL, ARY, SE, FCE).
54:58	RW	SEQ_12EVEN: Sequence cycle 12 is even for fast region (SL, NSL, ARY, SE, FCE).
59:63	RW	SEQ_12ODD: Sequence cycle 12 is odd for fast region (SL, NSL, ARY, SE, FCE).

Register Name	**Debug CBS CC Register**
Mnemonic	TP.TCEP03.TPCL3.DBG_CBS_CC
Address	0000000013030013 (SCOM)
Description	Debug CBS CC Register

Bits	SCOM	Field Mnemonic: Description
0	ROX	DBG_RESET_EP: Reset endpoint.
1	ROX	DBG_OPCG_IP: OPCG in progress, not in idle state.
2	ROX	DBG_VITL_CLKOFF: VITL HLD stopped. When enabled, plat-depth cycles are needed to switch this latch.
3	ROX	DBG_TEST_ENABLE: Test enable.
4	ROX	DBG_CBS_REQ: CBS Interface. Request (latched).
5:7	ROX	DBG_CBS_CMD: CBS Interface. Command (latched).
8:12	ROX	DBG_CBS_STATE: CBS Command State Machine 00000=Idle.
13	ROX	DBG_SECURITY_DEBUG_MODE: Status of the security mode bit.
14	ROX	DBG_CBS_PROTOCOL_ERROR: CBS protocol error. Request raised, although state machine is not in idle state. Need reset_ep to clear this bit. No impact on IPL.
15	ROX	DBG_PCB_IDLE: PCB Interface in idle state.
16:19	ROX	DBG_CURRENT_OPCG_MODE: The current (latest) OPCG mode: 0 = NOP 1 = LBIST 2 = ABIST 3 = RUNN 4 = SCAN0 5 = SCAN 6 = SCAN rotate 7 = SCAN with UpdateDR 8 = SCAN with CaptureDR 9 = CLK Change Request 10-15 = Unused
20:23	ROX	DBG_LAST_OPCG_MODE: Previous OPCG mode.
24	ROX	DBG_PCB_ERROR: PCB interface error. Read the CC error register or set CBS_CMD = 001 to switch the FSI CBS debug information to the CC error register.
25	ROX	DBG_PARITY_ERROR: Any parity error, non-PCB parity. Read the CC error register or set CBS_CMD = 001 to switch the FSI CBS debug information to the CC error register.
26	ROX	DBG_CC_ERROR: Any other CC error. Read the CC error register or set CBS_CMD = 001 to switch the FSI CBS debug information to the CC error register.
27	ROX	DBG_CHIPLET_IS_ALIGNED: Set to 1 when a valid align pulse was sent out.

Bits	SCOM	Field Mnemonic: Description
28	ROX	DBG_PCB_REQUEST_SINCE_RESET: Reset clears this bit, and the first PCB request sets it.
29	ROX	DBG_PARANOIA_TEST_ENABLE_CHANGE: Rising or falling edge on test enable, after reset. Need reset_ep to clear. No impact on IPL.
30	ROX	DBG_PARANOIA_VITL_CLKOFF_CHANGE: Rising or falling edge on vitl_clkoff, after reset. Need reset_ep to clear. No impact on IPL.
31	ROX	TP_TPFSI_CBS_ACK: This is the only representation of the CC acknowledge signal that is sent to FSI.

Register Name	CC Protect Mode Register
Mnemonic	TP.TCEP03.TPCL3.CC_PROTECT_MODE_REG
Address	00000000130303FE (SCOM)
Description	Enables read and write protection.

Bits	SCOM	Field Mnemonic: Description
0	RW	CC_READ_PROTECT_ENABLE: Enables read protection.
1	RW	CC_WRITE_PROTECT_ENABLE: Enables write protection.

Register Name	Atomic Lock Register
Mnemonic	TP.TCEP03.TPCL3.CC_ATOMIC_LOCK_REG
Address	00000000130303FF (SCOM)
Description	Enables an atomic lock and an atomic lock counter.

Bits	SCOM	Field Mnemonic: Description
0	RW	CC_ATOMIC_LOCK_ENABLE: Enables atomic lock.
1:4	ROX	CC_ATOMIC_ID: Atomic ID.
5:7	RO	constant = 0b000
8:15	ROX	CC_ATOMIC_ACTIVITY: Atomic lock counter.

Register Name	Global Checkstop FIR Register
Mnemonic	TP.TCEP03.XFIR
Address	0000000013040000 (SCOM)
Description	Global checkstop FIR

Bits	SCOM	Field Mnemonic: Description
0	RWX	XFIR_IN0: Summary bit (any checkstop).
1	RWX	XFIR_IN1: Checkstop broadcast via OOB.
2	RWX	XFIR_IN2: Unused.
3	RWX	XFIR_IN3: Checkstop from pervasive unit.
4	RWX	XFIR_IN4: Checkstop from L30.
5	RWX	XFIR_IN5: Checkstop from L31.
6	RWX	XFIR_IN6: Checkstop from L20.

Bits	SCOM	Field Mnemonic: Description
7	RWX	XFIR_IN7: Checkstop from L21.
8	RWX	XFIR_IN8: Checkstop from NC0.
9	RWX	XFIR_IN9: Checkstop from NC1.
10	RWX	XFIR_IN10: Unused.
11	RWX	XFIR_IN11: Checkstop from CME0.
12	RWX	XFIR_IN12: Checkstop from CME1.
13:25	RWX	XFIR_IN13: Unused.
26	RWX	XFIR_IN26: Checkstop on debug trigger.

Register Name	Global Recoverable FIR Register
Mnemonic	TP.TCEP03.RFIR
Address	0000000013040001 (SCOM)
Description	Global recoverable FIR

Bits	SCOM	Field Mnemonic: Description
0	ROX	RFIR_IN0: Local checkstop from NX and CXA0.
1	ROX	LFIR_RECOV_ERR: Recoverable error from pervasive unit.
2	ROX	RFIR_IN4: Recovery from L30.
3	ROX	RFIR_IN5: Recovery from L31.
4	ROX	RFIR_IN6: Recovery from L20.
5	ROX	RFIR_IN7: Recovery from L21.
6	ROX	RFIR_IN8: Recovery from NC0.
7	ROX	RFIR_IN9: Recovery from NC1.
8	ROX	RFIR_IN10: Unused.
9	ROX	RFIR_IN11: Recovery from CME0.
10	ROX	RFIR_IN12: Recovery from CME1.
11:23	ROX	RFIR_IN13: Unused.

Register Name	FIR Mask Register
Mnemonic	TP.TCEP03.FIR_MASK
Address	0000000013040002 (SCOM)
Description	FIR mask

Bits	SCOM	Field Mnemonic: Description
0	RW	FIR_MASK_IN0: Mask for XFIR summary bit.
1	RW	FIR_MASK_IN1: Mask for XFIR broadcast via OOB.
2	RW	FIR_MASK_IN2: Unused.
3	RW	FIR_MASK_IN3: Mask for XFIR/RFIR from pervasive unit.
4	RW	FIR_MASK_IN4: Mask for CX XFIR and RFIR.

Bits	SCOM	Field Mnemonic: Description
5:25	RW	FIR_MASK_IN5: Unused.
26	RW	FIR_MASK_IN26: Mask for debug trigger and local checkstop to recoverable error.

Register Name	Special Attention Register
Mnemonic	TP.TCEP03.SPATTN
Address	0000000013040004 (SCOM) 0000000013040005 (SCOM1) 0000000013040006 (SCOM2)
Description	Special attention

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	ROX	NCX	NCX	SPATTN_IN0: Unused special attentions.
1	ROX	NCX	NCX	SPATTN_IN1: Unused special attentions.
2	ROX	NCX	NCX	SPATTN_IN2: Unused special attentions.
3	ROX	NCX	NCX	SPATTN_IN3: Unused special attentions.
4	ROX	NCX	NCX	SPATTN_IN4: Unused special attentions.
5	ROX	NCX	NCX	SPATTN_IN5: Unused special attentions.
6	ROX	NCX	NCX	SPATTN_IN6: Unused special attentions.
7	ROX	NCX	NCX	SPATTN_IN7: Unused special attentions.
8	ROX	NCX	NCX	SPATTN_IN8: Unused special attentions.
9	ROX	NCX	NCX	SPATTN_IN9: Unused special attentions.

Register Name	Special Attention Mask Register
Mnemonic	TP.TCEP03.SPA_MASK
Address	0000000013040007 (SCOM)
Description	Special attention mask

Bits	SCOM	Field Mnemonic: Description
0:9	RW	SPA_MASK_IN: Special attention mask.

Register Name	Mode Register
Mnemonic	TP.TCEP03.TPCL3.EPS.FIR.MODE_REG
Address	0000000013040008 (SCOM)
Description	Mode register

Bits	SCOM	Field Mnemonic: Description
0	RW	MODE_IN0: Unused.
1	RW	MODE_IN1: Unused.
2	RW	MODE_IN2: Unused.
3	RW	MODE_IN3: Unused.

Bits	SCOM	Field Mnemonic: Description
4	RW	MODE_IN4: Stop chip TOD on checkstop. (Unused in POWER9.)
5	RW	MODE_IN5: Stop chip TOD on recoverable. (Unused in POWER9.)
6	RW	MODE_IN6: Disable propagation of checkstop to other chips.
7	RW	MODE_IN7: Unused.
8	RW	MODE_IN8: Enable checkstop on special attention.
9	RW	MODE_IN9: mask_direct/local_error.
10	RW	MODE_IN10: Unused.
11	RW	MODE_IN11: Unused.
12:15	RW	MODE_IN: Unused.

Register Name	Host Attention Register
Mnemonic	TP.TCEP03.HOSTATTN
Address	0000000013040009 (SCOM)
Description	Host attention

Bits	SCOM	Field Mnemonic: Description
0	ROX	HOSTATTN_IN0: Host attention summary bit.
1	ROX	HOSTATTN_IN1: Unused.
2	ROX	HOSTATTN_IN2: Unused.
3	ROX	HOSTATTN_IN3: Unused.
4	ROX	HOSTATTN_IN4: Unused.
5	ROX	HOSTATTN_IN5: Unused.
6	ROX	HOSTATTN_IN6: Unused.
7	ROX	HOSTATTN_IN7: Unused.
8	ROX	HOSTATTN_IN8: Unused.
9	ROX	HOSTATTN_IN9: Unused.
10	ROX	HOSTATTN_IN10: Unused.
11	ROX	HOSTATTN_IN11: Unused.
12	ROX	HOSTATTN_IN12: Unused.
13	ROX	HOSTATTN_IN13: Unused.
14	ROX	HOSTATTN_IN14: Unused.
15	ROX	HOSTATTN_IN15: Unused.
16	ROX	HOSTATTN_IN16: Unused.
17	ROX	HOSTATTN_IN17: Unused.
18	ROX	HOSTATTN_IN18: Unused.
19	ROX	HOSTATTN_IN19: Unused.
20	ROX	HOSTATTN_IN20: Unused.
21	ROX	HOSTATTN_IN21: Unused.
22	ROX	HOSTATTN_IN22: Unused.

Register Name	Local FIR Register
Mnemonic	TP.TCEP03.LOCAL_FIR
Address	000000001304000A (SCOM) 000000001304000B (SCOM1) 000000001304000C (SCOM2)
Description	Local FIR

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_IN0: CFIR internal parity error.
1	RWX	WOX_AND	WOX_OR	FIR_IN1: Errors from Control.
2	RWX	WOX_AND	WOX_OR	FIR_IN2: Local errors from CC (PCB error).
3	RWX	WOX_AND	WOX_OR	FIR_IN3: Local errors from CC (OPCG, parity, scan collision, and so on).
4	RWX	WOX_AND	WOX_OR	FIR_IN4: Local errors from PSC (PCB error).
5	RWX	WOX_AND	WOX_OR	FIR_IN5: Local errors from PSC (parity error).
6	RWX	WOX_AND	WOX_OR	FIR_IN6: Local errors from Thermal (parity error).
7	RWX	WOX_AND	WOX_OR	FIR_IN7: Local errors from Thermal (PCB error).
8	RWX	WOX_AND	WOX_OR	FIR_IN8: Local errors from Thermal (Trip error critical).
9	RWX	WOX_AND	WOX_OR	FIR_IN9: Local errors from Thermal (Trip error fatal).
10	RWX	WOX_AND	WOX_OR	FIR_IN10: therm volttrip error.
11	RWX	WOX_AND	WOX_OR	FIR_IN11: Local errors from Debug (error).
12	RWX	WOX_AND	WOX_OR	FIR_IN12: Local errors from L3 Trace Array0 (SCOM error).
13	RWX	WOX_AND	WOX_OR	FIR_IN13: Local errors from L3 Trace Array0.
14	RWX	WOX_AND	WOX_OR	FIR_IN14: Local errors from L3 Trace Array1 (SCOM error).
15	RWX	WOX_AND	WOX_OR	FIR_IN15: Local errors from L3 Trace Array1.
16	RWX	WOX_AND	WOX_OR	FIR_IN16: Local errors from L20 Trace Array (SCOM error).
17	RWX	WOX_AND	WOX_OR	FIR_IN17: Local errors from L20 Trace Array.
18	RWX	WOX_AND	WOX_OR	FIR_IN18: Local errors from L21 Trace Array (SCOM error).
19	RWX	WOX_AND	WOX_OR	FIR_IN19: Local errors from L21 Trace Array.
20	RWX	WOX_AND	WOX_OR	FIR_IN20: Unused.
21	RWX	WOX_AND	WOX_OR	FIR_IN21: Local errors from duty cycle adjustment ex00_c0.
22	RWX	WOX_AND	WOX_OR	FIR_IN22: Local errors from duty cycle adjustment ex00_c1.
23	RWX	WOX_AND	WOX_OR	FIR_IN23: Local errors from duty cycle adjustment ex00_l2.
24	RWX	WOX_AND	WOX_OR	FIR_IN24: Local errors from duty cycle adjustment ex01_c0.
25	RWX	WOX_AND	WOX_OR	FIR_IN25: Local errors from duty cycle adjustment ex01_c1.
26	RWX	WOX_AND	WOX_OR	FIR_IN26: Local errors from duty cycle adjustment ex01_l2.
27	RWX	WOX_AND	WOX_OR	FIR_IN27: Local errors from skew adjustment skewadj6way.
28	RWX	WOX_AND	WOX_OR	FIR_IN28: Unused.
29	RWX	WOX_AND	WOX_OR	FIR_IN29: Unused.
30	RWX	WOX_AND	WOX_OR	FIR_IN30: Unused.
31	RWX	WOX_AND	WOX_OR	FIR_IN31: Unused.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
32	RWX	WOX_AND	WOX_OR	FIR_IN32: Unused.
33	RWX	WOX_AND	WOX_OR	FIR_IN33: Unused.
34	RWX	WOX_AND	WOX_OR	FIR_IN34: Unused.
35	RWX	WOX_AND	WOX_OR	FIR_IN35: Unused.
36	RWX	WOX_AND	WOX_OR	FIR_IN36: Unused.
37	RWX	WOX_AND	WOX_OR	FIR_IN37: Unused.
38	RWX	WOX_AND	WOX_OR	FIR_IN38: Unused.
39	RWX	WOX_AND	WOX_OR	FIR_IN39: Unused.
40	RWX	WOX_AND	WOX_OR	FIR_IN40: Unused.
41	RWX	WOX_AND	WOX_OR	FIR_IN41: Malfunction alert broadcast via OOB.

Register Name	Local FIR Mask Register
Mnemonic	TP.TCEP03.TPCL3.EPS.FIR.LOCAL_FIR_MASK
Address	000000001304000D (SCOM) 000000001304000E (SCOM1) 000000001304000F (SCOM2)
Description	Local FIR mask

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:41	RW	WO_AND	WO_OR	LFIR_MASK_IN: Mask for LEM error collection vector.

Register Name	Local FIR Action 0 Register
Mnemonic	TP.TCEP03.TPCL3.EPS.FIR.LOCAL_FIR_ACTION0
Address	0000000013040010 (SCOM)
Description	Local FIR action 0

Bits	SCOM	Field Mnemonic: Description
0:41	RW	FIR_ACTION0_IN: action0 mask.

Register Name	Local FIR Action 1 Register
Mnemonic	TP.TCEP03.TPCL3.EPS.FIR.LOCAL_FIR_ACTION1
Address	0000000013040011 (SCOM)
Description	Local FIR action 1

Bits	SCOM	Field Mnemonic: Description
0:41	RW	FIR_ACTION1_IN: action1 mask.

Register Name	Group Checkstop Trigger Register
Mnemonic	TP.TCEP03.TPCL3.EPS.FIR.GXSTOP_TRIG_REG
Address	0000000013040013 (SCOM)
Description	Group checkstop trigger register

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP_TRIG_IN0: Mask bit for system checkstop.
1	RW	GXSTP_TRIG_IN1: Mask bit for recoverable error.
2	RW	GXSTP_TRIG_IN2: Mask bit for special attention.
3	RW	GXSTP_TRIG_IN3: Mask bit for local checkstop.
4	RW	GXSTP_TRIG_IN4: Mask bit for type 4 error (host attention).
5	RW	GXSTP_TRIG_IN5: Mask bit for OOB sys_checkstop input (0).
6	RW	GXSTP_TRIG_IN6: Mask bit for OOB sys_checkstop input (1).
7	RW	GXSTP_TRIG_IN7: Mask bit for group checkstop input (0).
8	RW	GXSTP_TRIG_IN8: Mask bit for group checkstop input (1).
9	RW	GXSTP_TRIG_IN9: Mask bit for debug checkstop on trigger.
10	RW	GXSTP_TRIG_IN10: Unused.
11	RW	GXSTP_TRIG_IN11: Unused.

Register Name	Group 0 Checkstop Mask Register
Mnemonic	TP.TCEP03.TPCL3.EPS.FIR.GXSTOP0_MASK_REG
Address	0000000013040014 (SCOM)
Description	Group 0 checkstop mask

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP0_TRIG_IN0: Mask bit for system checkstop.
1	RW	GXSTP0_TRIG_IN1: Mask bit for recoverable error.
2	RW	GXSTP0_TRIG_IN2: Mask bit for special attention.
3	RW	GXSTP0_TRIG_IN3: Mask bit for local checkstop.
4	RW	GXSTP0_TRIG_IN4: Mask bit for type 4 error (host attention).
5	RW	GXSTP0_TRIG_IN5: Mask bit for OOB sys_checkstop input (0).
6	RW	GXSTP0_TRIG_IN6: Mask bit for OOB sys_checkstop input (1).
7	RW	GXSTP0_TRIG_IN7: Mask bit for group checkstop input (0).
8	RW	GXSTP0_TRIG_IN8: Mask bit for group checkstop input (1).
9	RW	GXSTP0_TRIG_IN9: Mask bit for debug checkstop on trigger.
10	RW	GXSTP0_TRIG_IN10: Unused.
11	RW	GXSTP0_TRIG_IN11: Unused.

Register Name	Group 1 Checkstop Mask Register
Mnemonic	TP.TCEP03.TPCL3.EPS.FIR.GXSTOP1_MASK_REG
Address	0000000013040015 (SCOM)
Description	Group 1 checkstop mask

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP1_TRIG_IN0: Mask bit for system checkstop.
1	RW	GXSTP1_TRIG_IN1: Mask bit for recoverable error.
2	RW	GXSTP1_TRIG_IN2: Mask bit for special attention.
3	RW	GXSTP1_TRIG_IN3: Mask bit for local checkstop.
4	RW	GXSTP1_TRIG_IN4: Mask bit for type 4 error (host attention).
5	RW	GXSTP1_TRIG_IN5: Mask bit for OOB sys_checkstop input (0).
6	RW	GXSTP1_TRIG_IN6: Mask bit for OOB sys_checkstop input (1).
7	RW	GXSTP1_TRIG_IN7: Mask bit for group checkstop input (0).
8	RW	GXSTP1_TRIG_IN8: Mask bit for group checkstop input (1).
9	RW	GXSTP1_TRIG_IN9: Mask bit for debug checkstop on trigger.
10	RW	GXSTP1_TRIG_IN10: Unused.
11	RW	GXSTP1_TRIG_IN11: Unused.

Register Name	Group 2 Checkstop Mask Register
Mnemonic	TP.TCEP03.TPCL3.EPS.FIR.GXSTOP2_MASK_REG
Address	0000000013040016 (SCOM)
Description	Group 2 checkstop mask

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP2_TRIG_IN0: Mask bit for system checkstop.
1	RW	GXSTP2_TRIG_IN1: Mask bit for recoverable error.
2	RW	GXSTP2_TRIG_IN2: Mask bit for special attention.
3	RW	GXSTP2_TRIG_IN3: Mask bit for local checkstop.
4	RW	GXSTP2_TRIG_IN4: Mask bit for type 4 error (host attention).
5	RW	GXSTP2_TRIG_IN5: Mask bit for OOB sys_checkstop input (0).
6	RW	GXSTP2_TRIG_IN6: Mask bit for OOB sys_checkstop input (1).
7	RW	GXSTP2_TRIG_IN7: Mask bit for group checkstop input (0).
8	RW	GXSTP2_TRIG_IN8: Mask bit for group checkstop input (1).
9	RW	GXSTP2_TRIG_IN9: Mask bit for debug checkstop on trigger.
10	RW	GXSTP2_TRIG_IN10: Unused.
11	RW	GXSTP2_TRIG_IN11: Unused.

Register Name	Summary Mask Register
Mnemonic	TP.TCEP03.TPCL3.EPS.FIR.SUM_MASK_REG
Address	0000000013040017 (SCOM)
Description	Summary mask register

Bits	SCOM	Field Mnemonic: Description
0	RW	SMASK_IN0: System checkstop summary bit.
1	RW	SMASK_IN1: Recoverable summary bit.
2	RW	SMASK_IN2: Special Attention summary bit.
3	RW	SMASK_IN3: Local checkstop summary bit.
4	RW	SMASK_IN4: Type 4 (host attention summary bit.

Register Name	Local Checkstop Error Register
Mnemonic	TP.TCEP03.LOCAL_XSTOP_ERR
Address	0000000013040018 (SCOM)
Description	Local checkstop error

Bits	SCOM	Field Mnemonic: Description
0	ROX	LOCAL_XSTOP_IN0: Local checkstop summary bit.
1	ROX	LOCAL_XSTOP_IN1: Unused.
2	ROX	LOCAL_XSTOP_IN2: Unused.
3	ROX	LOCAL_XSTOP_IN3: Unused.
4	ROX	LOCAL_XSTOP_IN4: Unused.
5	ROX	LOCAL_XSTOP_IN5: Unused.
6	ROX	LOCAL_XSTOP_IN6: Unused.
7	ROX	LOCAL_XSTOP_IN7: Unused.
8	ROX	LOCAL_XSTOP_IN8: Unused.
9	ROX	LOCAL_XSTOP_IN9: Unused.
10	ROX	LOCAL_XSTOP_IN10: Unused.
11	ROX	LOCAL_XSTOP_IN11: Unused.
12	ROX	LOCAL_XSTOP_IN12: Unused.
13	ROX	LOCAL_XSTOP_IN13: Unused.
14	ROX	LOCAL_XSTOP_IN14: Unused.
15	ROX	LOCAL_XSTOP_IN15: Unused.
16	ROX	LOCAL_XSTOP_IN16: Unused.
17	ROX	LOCAL_XSTOP_IN17: Unused.
18	ROX	LOCAL_XSTOP_IN18: Unused.
19	ROX	LOCAL_XSTOP_IN19: Unused.
20	ROX	LOCAL_XSTOP_IN20: Unused.
21	ROX	LOCAL_XSTOP_IN21: Unused.

Bits	SCOM	Field Mnemonic: Description
22	ROX	LOCAL_XSTOP_IN22: Unused.

Register Name	Local Checkstop Mask Register
Mnemonic	TP.TCEP03.LOCAL_XSTOP_MASK
Address	0000000013040019 (SCOM)
Description	Local checkstop mask

Bits	SCOM	Field Mnemonic: Description
0:21	RW	LOCAL_XSTOP_MASK_IN: Local checkstop mask.

Register Name	Host Attention Mask Register
Mnemonic	TP.TCEP03.HOSTATTN_MASK
Address	000000001304001A (SCOM)
Description	Host attention mask

Bits	SCOM	Field Mnemonic: Description
0:21	RW	HOSTATTN_MASK_IN: Host attention mask.

Register Name	DTS Thermal Sensor Result 0 Register
Mnemonic	TP.TCEP03.TPCL3.EPS.THERM.DTS_RESULT0
Address	0000000013050000 (SCOM)
Description	DTS thermal sensor results 0

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	DTS_0_RESULT: Calibrated DTS result of sensor with ID 0.
16:31	ROX	DTS_1_RESULT: Calibrated DTS result of sensor with ID 1.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	DTS Trace Results Register
Mnemonic	TP.TCEP03.TPCL3.EPS.THERM.DTS_TRC_RESULT
Address	0000000013050003 (SCOM)
Description	DTS trace results

Bits	SCOM	Field Mnemonic: Description
0:43	ROX	TIMESTAMP_COUNTER_VALUE: Time stamp counter value during DTS trace mode.
44	ROX	TIMESTAMP_COUNTER_OVERFLOW_ERR: Overflow error bit of the time stamp counter value during DTS trace mode.
45:47	RO	constant = 0b000
48:63	ROX	DTS_1_RESULT: Calibrated DTS result of sensor with ID 1.

Register Name	Thermal Mode Register
Mnemonic	TP.TCEP03.TPCL3.EPS.THERM.THERM_MODE_REG
Address	000000001305000F (SCOM)
Description	Enables and controls CPM and DTS.

Bits	SCOM	Field Mnemonic: Description
0	RW	THERM_DIS_CPM_BUBBLE_CORR: Critical path result bubble correction active.
1	RW	THERM_FORCE_THRES_ACT: Forces tpc_therm_thres_mac clock gating off and activates clocks.
2:4	RW	THERM_THRES_TRIP_ENA: Enables therm_thres_trip compare. 1xx = trip0, warning. x1x = trip1, critical. xx1 = trip2, fatal.
5	RW	THERM_DTS_SAMPLE_ENA: 0 = No DTS sampling. 1 = DTS sampling is enabled and a below-counter compare match can occur.
6:9	RW	THERM_SAMPLE_PULSE_CNT: A 16 MHz sample pulse is fed into an 18-bit counter. therm_sample_pulse_cnt enables the selection of a high order bit of the counter to enable resolution of sampling DTSs between 2.5 µs and 80 ms. An edge detection circuit detects the rising edge of the selected counter bit and this triggers a DTS sample. 0000 = 16 ms. 0001 = 8 ms. 0010 = 4 ms. 0011 = 2 ms. 0100 = 1 ms. 0101 = 0.5 ms. 0110 = 250 µs. 0111 = 125 µs. 1000 = 62 .5 µs. 1001 = 31.3 µs. 1010 = 15.6 µs. 1011 = 7.8 µs. 1100 = 3.9 µs. 1101 = 2 µs. 1110 = 1 µs. 1111 = 0.5 µs.
10:11	RW	THERM_THRES_MODE_ENA: Forces maximum or minimum mode in the threshold unit: 00 = Off. 11 = Illegal. 10 = Maximum mode. 01 = Minimum mode.
12	RW	DTS_TRIGGER_MODE: Unused.
13	RW	DTS_TRIGGER_SEL: Unused.
14	RW	THERM_THRES_OVERFLOW_MASK: 0 = therm_overflow_err is enabled. 1 = therm_overflow_err is disabled.
15	RW	THERM_MODE_UNUSED: Unused.
16:19	RW	THERM_DTS_READ_SEL: Selects which DTS result will be provided with PCB read addr_v(4): 0000 = DTS 0. 0001 = DTS 1. 0010 = DTS 2. 0100 = DTS 4. 1111 = Worst case sensor.

Bits	SCOM	Field Mnemonic: Description
20:21	RW	THERM_DTS_ENABLE_L1: loop1 DTS enables: 1x = DTS 0 available. x1 = DTS 1 available.
22:34	RO	constant = 0b0000000000000
35:36	RW	Reserved field.

Register Name	Skitter Control Register
Mnemonic	TP.TCEP03.TPCL3.EPS.THERM.SKITTER_MODE_REG
Address	0000000013050010 (SCOM)
Description	Skitter control register

Bits	SCOM	Field Mnemonic: Description
0	RW	SKITTER_HOLD_SAMPLE: Forces skitter to hold the current sample.
1	RW	DISABLE_SKITTER_STICKINESS: A value of '0' specifies accumulation mode. A value of '1' samples a new value on each cycle and resets the sticky value.
2:3	RW	SKITTER_MODE_UNUSED1: Unused.
4:5	RW	SKITTER_HOLD_DBGTRIG_SEL: bit0 = hold_on_trigger0 bit1 = hold_on_trigger1
6:7	RW	SKITTER_RESET_TRIG_SEL: bit0 = reset_sticky_on_trigger0. bit1 = reset_sticky_on_trigger1.
8:9	RW	SKITTER_SAMPLE_GUTS: Selects which guts to measure: 00 = guts1. 01 = guts2. 10 = guts3. 11 = guts4.
10:43	RO	constant = 0b0000000000000000000000000000000000
44	ROX	SKITTER_HOLD_SAMPLE_WITH_TRIGGER: Forces skitter to hold the current sample on debug trigger; this has highest priority.
45	ROX	SKITTER_DATA_V_LT: If set to '1', the data requested by a skitter force read register has finished and data is present in the skitter data register in the collector macro. The data be read by any combination of V25/V26/V27 PCB reads.

Register Name	Error Injection Control Register
Mnemonic	TP.TCEP03.TPCL3.EPS.THERM.INJECT_REG
Address	0000000013050011 (SCOM)
Description	Error injection control register

Bits	SCOM	Field Mnemonic: Description
0:1	RW	THERM_INJECT_TRIP: 00 = No injection. 01 = Warning trip level injection. 10 = Critical trip level injection. 11 = Fatal trip level injection.

Bits	SCOM	Field Mnemonic: Description
2:3	RW	THERM_INJECT_MODE: 00 = No injection. 01 = Injection on the next DTS sample. 10 = Solid injection for the next DTS samples till bit setting changes. 11 = Not used.

Register Name	Thermal Control Register
Mnemonic	TP.TCEP03.TPCL3.EPS.THERM.CONTROL_REG
Address	0000000013050012 (SCOM)
Description	Control / force reset register

Bits	SCOM	Field Mnemonic: Description
0	WO_1P	Reserved field.
1	WO_1P	Reserved field.
2	WO_1P	Reserved field.
3	WO_1P	Reserved field.
4	WO_1P	Reserved field.
5	WO_1P	Reserved field.
6	WO_1P	Reserved field.
7	WO_1P	Reserved field.
8	WO_1P	Reserved field.
9	WO_1P	Reserved field.
10	WO_1P	Reserved field.
11	WO_1P	Reserved field.
12	WO_1P	Reserved field.

Register Name	Thermal Error Status Register
Mnemonic	TP.TCEP03.TPCL3.EPS.THERM.ERR_STATUS_REG
Address	0000000013050013 (SCOM)
Description	Thermal error status register

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	Reserved field.
2	ROX	Reserved field.
3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.
7	ROX	Reserved field.
8	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
9	ROX	Reserved field.
10	ROX	Reserved field.
11	ROX	Reserved field.
12	ROX	Reserved field.
13	ROX	Reserved field.
14	ROX	Reserved field.
15	ROX	Reserved field.
16	ROX	SERIAL_SHIFTCNT_MODEREG_PARITY_ERR_MASK: Serial shift count parity error mask.
17	ROX	THERM_MODEREG_PARITY_ERR_MASK: Thermal Mode Register parity error mask.
18	ROX	SKITTER_MODEREG_PARITY_ERR_MASK: Skitter Mode Register parity error mask.
19	ROX	SKITTER_FORCEREG_PARITY_ERR_MASK: Skitter Force Register parity error mask.
20	ROX	SCAN_INIT_VERSION_REG_PARITY_ERR_MASK: Scan Initial Version Register parity error mask.
21	ROX	VOLT_MODEREG_PARITY_ERR_MASK: Volt Mode Register parity error mask.
22	RO	constant = 0b0
23	ROX	COUNT_STATE_ERR_MASK: Count state machine error mask.
24	ROX	RUN_STATE_ERR_MASK: Run state machine error mask.
25	ROX	THRES_STATE_ERR_MASK: Threshold state machine error mask.
26	ROX	OVERFLOW_ERR_MASK: DTS calibration calculation overflow error mask.
27	ROX	SHIFTER_PARITY_ERR_MASK: Shifter parity error mask.
28	ROX	SHIFTER_VALID_ERR_MASK: Shifter valid error mask.
29	ROX	TIMEOUT_ERR_MASK: Timeout error mask.
30	ROX	F_SKITTER_READ_ERR_MASK: Force skitter read error mask.
31	ROX	PCB_ERR_MASK: Pervasive control bus error mask.
32:39	RO	constant = 0b00000000
40:43	ROX	Reserved field.
44:46	ROX	Reserved field.
47	ROX	Reserved field.
48	ROX	Reserved field.
49:50	ROX	Reserved field.
51:54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Skitter Force Read Register
Mnemonic	TP.TCEP03.TPCL3.EPS.THERM.SKITTER_FORCE_REG
Address	0000000013050014 (SCOM)
Description	Skitter Force Read Register

Bits	SCOM	Field Mnemonic: Description
0	RW	F_SKITTER_READ: Forces the read of a particular skitter.

Register Name	Skitter Clock Source Control Register
Mnemonic	TP.TCEP03.TPCL3.EPS.THERM.SKITTER_CLKSRC_REG
Address	0000000013050016 (SCOM)
Description	Skitter clock source control register

Bits	SCOM	Field Mnemonic: Description
0:2	RW	SKITTER0_CLKSRC: Selects the clock to measure: 000 = Local mesh clock. 001 = External pin skitter_c1_1_in. 010 = Local d1clk only if d_mode = 1. 011 = External pin skitter_c1_2_in. 100 = Local lclk only if d_mode = 1. 101 = External pin skitter_c1_3_in. 110 = Unused. 111 = External pin skitter_c1_4_in.
3:35	RO	constant = 0b000000000000000000000000000000000
36:37	RW	SKITTER0_DELAY_SELECT: Selects the delay to be added between the skitter0 clock source multiplexer and the inverter chain. The base line delay is 12.2 psec. 00 = No delay. 01 = 0.6 psec. 10 = 1.8 psec. 11 = 5 psec.

Register Name	Skitter Data 0 Register
Mnemonic	TP.TCEP03.TPCL3.EPS.THERM.SKITTER_DATA0
Address	0000000013050019 (SCOM)
Description	Skitter data register read bit0:63

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved.

Register Name	Skitter Data 1 Register
Mnemonic	TP.TCEP03.TPCL3.EPS.THERM.SKITTER_DATA1
Address	000000001305001A (SCOM)
Description	Skitter data register read bit32:95

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved.

Register Name	Skitter Data 2 Register
Mnemonic	TP.TCEP03.TPCL3.EPS.THERM.SKITTER_DATA2
Address	000000001305001B (SCOM)
Description	Skitter data register read bit64:127

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved.

Register Name	Timestamp Counter Read Register
Mnemonic	TP.TCEP03.TPCL3.EPS.THERM.TIMESTAMP_COUNTER_READ
Address	000000001305001C (SCOM)
Description	Timestamp counter read

Bits	SCOM	Field Mnemonic: Description
0:43	ROX	TIMESTAMP_COUNTER_VALUE: Time stamp counter value during DTS trace mode.
44	ROX	TIMESTAMP_COUNTER_OVERFLOW_ERR: Overflow error bit of the time stamp counter value during DTS trace mode.

12. CACHE Chiplet PCB Slave

The POWER9 processor registers are listed alphabetically by mnemonic in the following address table.

Mnemonic	Address	Page
TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.ASSIST_INTERRUPT_REG	0x00000000130F0011	2036
TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.ATOMIC_LOCK_REG	0x00000000130F03FF	2070
TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.ATTN_INTERRUPT_REG	0x00000000130F001A	2036
TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.EDRAM_STATUS	0x00000000130F0029	2041
TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.ERROR_REG	0x00000000130F001F	2038
TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.HANG_PULSE_0_REG	0x00000000130F0020	2039
TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.HANG_PULSE_1_REG	0x00000000130F0021	2039
TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.HANG_PULSE_2_REG	0x00000000130F0022	2039
TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.HANG_PULSE_3_REG	0x00000000130F0023	2039
TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.HANG_PULSE_4_REG	0x00000000130F0024	2040
TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.HANG_PULSE_5_REG	0x00000000130F0025	2040
TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.HANG_PULSE_6_REG	0x00000000130F0026	2040
TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.HEARTBEAT_REG	0x00000000130F0018	2036
TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.MULTICAST_GROUP_1	0x00000000130F0001	2034
TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.MULTICAST_GROUP_2	0x00000000130F0002	2035
TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.MULTICAST_GROUP_3	0x00000000130F0003	2035
TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.MULTICAST_GROUP_4	0x00000000130F0004	2035
TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.NET_CTRL0	0x00000000130F0040	2041
TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.NET_CTRL1	0x00000000130F0044	2042
TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.PLL_LOCK_REG	0x00000000130F0019	2036
TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.PRE_COUNTER_REG	0x00000000130F0028	2040
TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.PRIMARY_ADDRESS_REG	0x00000000130F0000	2034
TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.PROTECT_MODE_REG	0x00000000130F03FE	2069
TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.RECOV_INTERRUPT_REG	0x00000000130F001B	2037
TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.SLAVE_CONFIG_REG	0x00000000130F001E	2037
TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.TIMEOUT_REG	0x00000000130F0010	2035
TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.VITAL_SCAN_OUT	0x00000000130F0017	2036
TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.XSTOP_INTERRUPT_REG	0x00000000130F001C	2037
TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_CGCR	0x00000000130F0164	2061
TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_GPMMR	0x00000000130F0100	2043
TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_IVRMAVR	0x00000000130F01B5	2066
TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_IVRMCR	0x00000000130F01B0	2064
TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_IVRMDVR	0x00000000130F01B4	2065
TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_IVRMST	0x00000000130F01B3	2065
TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_PFCS	0x00000000130F0118	2048
TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_PFDLY	0x00000000130F011B	2051
TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_PFOFF	0x00000000130F011D	2052
TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_PFSNS	0x00000000130F011C	2052
TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_PIG	0x00000000130F0180	2063
TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_SCRATCH0	0x00000000130F011E	2052
TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_SCRATCH1	0x00000000130F011F	2053
TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_SPWKUP_FSP	0x00000000130F010B	2045

Mnemonic	Address	Page
TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_SPWKUP_HYP	0x00000000130F010D	2046
TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_SPWKUP_OCC	0x00000000130F010C	2046
TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_SPWKUP_OTR	0x00000000130F010A	2045
TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_SSHFSP	0x00000000130F0111	2047
TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_SSHHYP	0x00000000130F0114	2048
TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_SSHOCC	0x00000000130F0112	2047
TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_SSHOTR	0x00000000130F0113	2047
TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_SSHSRC	0x00000000130F0110	2046
TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_VDMCR	0x00000000130F01B8	2067
TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_QUAD_REGS.QPPM_DPLL_CTRL	0x00000000130F0152	2056
TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_QUAD_REGS.QPPM_DPLL_FREQ	0x00000000130F0151	2055
TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_QUAD_REGS.QPPM_DPLL_ICHAR	0x00000000130F0157	2058
TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_QUAD_REGS.QPPM_DPLL_OCHAR	0x00000000130F0156	2057
TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_QUAD_REGS.QPPM_DPLL_STAT	0x00000000130F0155	2057
TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_QUAD_REGS.QPPM_ERR	0x00000000130F0121	2053
TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_QUAD_REGS.QPPM_ERRMSK	0x00000000130F0122	2054
TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_QUAD_REGS.QPPM_ERRSUM	0x00000000130F0120	2053
TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_QUAD_REGS.QPPM_EXCGCR	0x00000000130F0165	2061
TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_QUAD_REGS.QPPM_OCCHB	0x00000000130F015F	2059
TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_QUAD_REGS.QPPM_QACCR	0x00000000130F0160	2059
TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_QUAD_REGS.QPPM_QACSR	0x00000000130F0163	2060
TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_QUAD_REGS.QPPM_QCCR	0x00000000130F01BD	2068
TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_QUAD_REGS.QPPM_QPMMR	0x00000000130F0103	2043
TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_QUAD_REGS.QPPM_VDMCFGR	0x00000000130F01B6	2066
TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_QUAD_REGS.QPPM_VOLT_CHAR	0x00000000130F01BB	2068

The POWER9 processor registers are listed in the following tables.

Register Name	Primary Address Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.PRIMARY_ADDRESS_REG
Address	00000000130F0000 (SCOM)
Description	Contains the slave's primary address

Bits	SCOM	Field Mnemonic: Description
0:5	RO	Reserved field.

Register Name	Multicast Group 1 Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.MULTICAST_GROUP_1
Address	00000000130F0001 (SCOM)
Description	Multicast group 1

Bits	SCOM	Field Mnemonic: Description
0:2	RO	constant = 0b111
3:5	RW	MULTICAST1_GROUP: Multicast group1 setting.

Register Name	Multicast Group 2 Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.MULTICAST_GROUP_2
Address	00000000130F0002 (SCOM)
Description	Multicast group 2

Bits	SCOM	Field Mnemonic: Description
0:2	RO	constant = 0b111
3:5	RW	MULTICAST2_GROUP: Multicast group2 setting.

Register Name	Multicast Group 3 Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.MULTICAST_GROUP_3
Address	00000000130F0003 (SCOM)
Description	Multicast group 3

Bits	SCOM	Field Mnemonic: Description
0:2	RO	constant = 0b111
3:5	RW	MULTICAST3_GROUP: Multicast group3 setting.

Register Name	Multicast Group 4 Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.MULTICAST_GROUP_4
Address	00000000130F0004 (SCOM)
Description	Multicast group 4

Bits	SCOM	Field Mnemonic: Description
0:2	RO	constant = 0b111
3:5	RW	MULTICAST4_GROUP: Multicast group4 setting.

Register Name	Timeout Select Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.TIMEOUT_REG
Address	00000000130F0010 (SCOM)
Description	Timeout select register

Bits	SCOM	Field Mnemonic: Description
0:1	RW	Reserved field.

Register Name	Assist Interrupt Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.ASSIST_INTERRUPT_REG
Address	00000000130F0011 (SCOM)
Description	Assist interrupt register

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	Reserved field.
2	ROX	Reserved field.

Register Name	Vital Scan Out Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.VITAL_SCAN_OUT
Address	00000000130F0017 (SCOM)
Description	Vital scan out

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved.

Register Name	Chiplet Heartbeat Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.HEARTBEAT_REG
Address	00000000130F0018 (SCOM)
Description	Chiplet heartbeat register

Bits	SCOM	Field Mnemonic: Description
0	ROX	HEARTBEAT_DEAD: Chiplet heartbeat not detected.

Register Name	PLL Lock Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.PLL_LOCK_REG
Address	00000000130F0019 (SCOM)
Description	Lock indications from PLLs

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	Reserved field.

Register Name	Attention Interrupt Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.ATTN_INTERRUPT_REG
Address	00000000130F001A (SCOM)
Description	Attention interrupt

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.

Register Name	Recoverable Interrupt Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.RECOV_INTERRUPT_REG
Address	00000000130F001B (SCOM)
Description	Recoverable interrupt

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.

Register Name	Checkstop Interrupt Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.XSTOP_INTERRUPT_REG
Address	00000000130F001C (SCOM)
Description	Checkstop interrupt

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.

Register Name	Slave Configuration Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.SLAVE_CONFIG_REG
Address	00000000130F001E (SCOM)
Description	Slave configuration register

Bits	SCOM	Field Mnemonic: Description
0	RW	CFG_DISABLE_PERV_THOLD_CHECK: Disables the pervasive thold check.
1	RW	CFG_DISABLE_MALF_PULSE_GEN: Disables pulse generation for a malfunction alert. Switches back to level.
2	RW	CFG_STOP_HANG_CNT_SYS_XSTP: Disables a hang counter stop for system checkstop.
3	RW	CFG_DISABLE_CL_ATOMIC_LOCK: Disables the atomic lock for chiplet accesses.
4	RW	CFG_DISABLE_HEARTBEAT: Disables a check for voltage and grid clock in the chiplet.
5	RW	CFG_DISABLE_FORCE_TO_ZERO: Disables force to zero for error cases.
6	RW	CFG_PM_DISABLE: Disables the power management set/reset interface for the NET CNTRLx Registers.
7	RW	CFG_PM_MUX_DISABLE: Disables the PM multiplexer request signal.
8:13	RW	ERROR_MASK: Mask bits for slave error reporting.
14:15	RW	Reserved.

Register Name	Error Capture Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.ERROR_REG
Address	00000000130F001F (SCOM)
Description	Error capture register

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	CE_ERROR: Correctable error on the PCB bus.
1:3	RWX_WCLEAR	CHIPLET_ERRORS: Errors reported by chiplet. This register is for debug purposes only. It holds meaningful data only if it is cleared after each error. 000 = No error. 001 = XSCOM command blocked due to pending errors. 010 = Chiplet offline. 011 = Partial good. 100 = Invalid address / address error / bad access type. 101 = Clock error. 110 = Parity error / received unexpected packet / wrong packet number. 111 = Timeout.
4	RWX_WCLEAR	PARITY_ERROR: Parity error on the PCB Interface.
5	RWX_WCLEAR	DATA_BUFFER_ERROR: Parity error in the data buffer.
6	RWX_WCLEAR	ADDR_BUFFER_ERROR: Parity error in the address buffer.
7	RWX_WCLEAR	PCB_FSM_ERROR: Invalid state error in the PCB FSM.
8	RWX_WCLEAR	CL_FSM_ERROR: Invalid state error in the chiplet FSM.
9	RWX_WCLEAR	INT_RX_FSM_ERROR: Invalid state error in the interrupt RX FSM.
10	RWX_WCLEAR	INT_TX_FSM_ERROR: Invalid state error in the interrupt TX FSM.
11	RWX_WCLEAR	INT_TYPE_ERROR: Invalid interrupt type.
12	RWX_WCLEAR	CL_DATA_ERROR: Parity error on the chiplet interface.
13	RWX_WCLEAR	INFO_ERROR: Parity error on the chiplet information lines.
14	RWX_WCLEAR	UNUSED_0: Unused.
15	RWX_WCLEAR	CHIPLET_ATOMIC_LOCK_ERROR: Chiplet atomic lock error.
16	RWX_WCLEAR	PCB_INTERFACE_ERROR: Error of the PCB interface component for the internal endpoint.
17	RWX_WCLEAR	CHIPLET_OFFLINE: Heartbeat check indicated that the chiplet is offline.
18	RWX_WCLEAR	EDRAM_SEQUENCE_ERR: Error in the eDRAM power up sequence.
19	RWX_WCLEAR	CTRL_REG_PARITY_ERROR: Control register parity is bad.
20	RWX_WCLEAR	ADDRESS_REG_PARITY_ERROR: Address register parity is bad.
21	RWX_WCLEAR	TIMEOUT_REG_PARITY_ERROR: Timeout select register parity is bad.
22	RWX_WCLEAR	CONFIG_REG_PARITY_ERROR: Slave configuration register parity is bad.
23	RWX_WCLEAR	UNUSED_1:
24	RWX_WCLEAR	DIV_REG_PARITY_ERROR: Register parity is bad.
25:28	RWX_WCLEAR	PLL_UNLOCK_ERROR: Unlock from a chiplet PLL.

Register Name	Hang Pulse 0 Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.HANG_PULSE_0_REG
Address	00000000130F0020 (SCOM)
Description	Hang pulse generation register 0

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_0: Value of hang pulse 0. Time period = 2^{value} x (precounter_reg + 1) / pcb_freq, where 34 ≥ value > 0.
6	RW	SUPPRESS_HANG_0: If set to 1, hang pulses are suppressed in case of a checkstop.

Register Name	Hang Pulse 1 Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.HANG_PULSE_1_REG
Address	00000000130F0021 (SCOM)
Description	Hang pulse generation register 1

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_1: Value of hang pulse 1. Time period = 2^{value} x (precounter_reg + 1) / pcb_freq, where 34 ≥ value > 0.
6	RW	SUPPRESS_HANG_1: If set to 1, hang pulses are suppressed in case of a checkstop.

Register Name	Hang Pulse 2 Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.HANG_PULSE_2_REG
Address	00000000130F0022 (SCOM)
Description	Hang pulse generation register 2

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_2: Value of hang pulse 2. Time period = 2^{value} x (precounter_reg + 1) / pcb_freq, where 34 ≥ value > 0.
6	RW	SUPPRESS_HANG_2: If set to 1, hang pulses are suppressed in case of a checkstop.

Register Name	Hang Pulse 3 Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.HANG_PULSE_3_REG
Address	00000000130F0023 (SCOM)
Description	Hang pulse generation register 3

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_3: Value of hang pulse 3. Time period = 2^{value} x (precounter_reg + 1) / pcb_freq, where 34 ≥ value > 0.
6	RW	SUPPRESS_HANG_3: If set to 1, hang pulses are suppressed in case of a checkstop.

Register Name	Hang Pulse 4 Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.HANG_PULSE_4_REG
Address	00000000130F0024 (SCOM)
Description	Hang pulse generation register 4

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_4: Value of hang pulse 4. Time period = 2^{value} x (precounter_reg + 1) / pcb_freq, where 34 ≥ value > 0.
6	RW	SUPPRESS_HANG_4: If set to 1, hang pulses are suppressed in case of a checkstop.

Register Name	Hang Pulse 5 Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.HANG_PULSE_5_REG
Address	00000000130F0025 (SCOM)
Description	Hang pulse generation register 5. This hang counter is used exclusively to generate the malfunction alert pulse.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_5: Value of hang pulse 5. Time period = 2^{value} x (precounter_reg + 1) / pcb_freq, where 34 ≥ value > 0.
6	RW	SUPPRESS_HANG_5: If set to 1, hang pulses are suppressed in case of a checkstop.

Register Name	Hang Pulse 6 Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.HANG_PULSE_6_REG
Address	00000000130F0026 (SCOM)
Description	Hang pulse generation register 6. This hang counter is used exclusively for the heartbeat generation.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_6: Value of hang pulse 6. Time period = 2^{value} x (precounter_reg + 1) / pcb_freq, where 34 ≥ value > 0.
6	RW	SUPPRESS_HANG_6: If set to 1, hang pulses are suppressed in case of a checkstop.

Register Name	Pre-Counter Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.PRE_COUNTER_REG
Address	00000000130F0028 (SCOM)
Description	Divider for hang counter clock

Bits	SCOM	Field Mnemonic: Description
0:7	RW	PRE_COUNTER: Divider for hang counter clock. Divides clock by n + 1. The default value is n = 0.

Register Name	eDRAM Status Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.EDRAM_STATUS
Address	00000000130F0029 (SCOM)
Description	eDRAM control status register

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	EDRAM_STAT: eDRAM control status.

Register Name	NET CTRL0 Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.NET_CTRL0
Address	00000000130F0040 (SCOM) 00000000130F0041 (SCOM1) 00000000130F0042 (SCOM2)
Description	NET CTRL0 register. (N/A in pervasive chiplets.)

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	CHIPLET_ENABLE: Set if chiplet is good.
1	RWX	RWX_WAND	RWX_WOR	PCB_EP_RESET: Output is ORed to the global EP reset.
2	RWX	RWX_WAND	RWX_WOR	CLK_ASYNC_RESET: For a POWER9 cache chiplet, the EQ skew adjustment is reset. For a POWER9 core chiplet, the core duty cycle adjustment is reset. For a POWER9 memory chiplet, the memory asynchronous glitchless multiplexer is reset.
3	RWX	RWX_WAND	RWX_WOR	PLL_TEST_EN: Test enable for chiplet PLL.
4	RWX	RWX_WAND	RWX_WOR	PLL_RESET: Reset for chiplet PLL.
5	RWX	RWX_WAND	RWX_WOR	PLL_BYPASS: Enable bypass for chiplet PLL.
6	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN: Scan control for chiplet vital domain.
7	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN_IN: Scan in for the chiplet vital domain.
8	RWX	RWX_WAND	RWX_WOR	VITAL_PHASE: Phase for vital domain.
9	RWX	RWX_WAND	RWX_WOR	FLUSH_ALIGN_OVR: Override flush, flush_nto1, align in chiplet to 1.
10	RWX	RWX_WAND	RWX_WOR	VITAL_AL: Align for vital domain.
11	RWX	RWX_WAND	RWX_WOR	ACT_DIS: LCB control signal for vital logic.
12	RWX	RWX_WAND	RWX_WOR	MPW1: LCB control signal for vital logic.
13	RWX	RWX_WAND	RWX_WOR	MPW2: LCB control signal for vital logic.
14	RWX	RWX_WAND	RWX_WOR	MPW3: LCB control signal for vital logic.
15	RWX	RWX_WAND	RWX_WOR	DELAY_LCLKR: LCB control signal for vital logic.
16	RWX	RWX_WAND	RWX_WOR	VITAL_THOLD: Thold for the chiplet vital domain.
17	RWX	RWX_WAND	RWX_WOR	FLUSH_SCAN_N: Flush scan control.
18	RWX	RWX_WAND	RWX_WOR	FENCE_EN: Fencing signal for chiplet.
19	RWX	RWX_WAND	RWX_WOR	CPLT_RCTRL: Chiplet receiver enable.
20	RWX	RWX_WAND	RWX_WOR	CPLT_DCTRL: Chiplet driver enable.
21	RWX	RWX_WAND	RWX_WOR	Reserved field.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
22	RWX	RWX_WAND	RWX_WOR	ADJ_FUNC_CLKSEL: POWER9 cache chiplet: Clock select for skew adjustment/duty cycle adjustment logic. POWER9 core chiplet: Skew sense to skew adjustment fencing.
23:24	RWX	RWX_WAND	RWX_WOR	Reserved field.
25	RWX	RWX_WAND	RWX_WOR	TP_FENCE_PCB: Fence the Chiplet from the PCB Bus. If set, PCB Slave will report *Chiplet Offline*.
26	RWX	RWX_WAND	RWX_WOR	LVLTRANS_FENCE: Fence control for level translators.
27	RWX	RWX_WAND	RWX_WOR	ARRAY_WRITE_ASSIST_EN: Array write assist.
28	RWX	RWX_WAND	RWX_WOR	HTB_INTEST: HTB in test mode.
29	RWX	RWX_WAND	RWX_WOR	HTB_EXTEST: HTB in test mode.
30	RWX	RWX_WAND	RWX_WOR	Reserved field.
31	RWX	RWX_WAND	RWX_WOR	PLLFORCE_OUT_EN: PLL force out enable.

Register Name	NET CTRL1 Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.NET_CTRL1
Address	00000000130F0044 (SCOM) 00000000130F0045 (SCOM1) 00000000130F0046 (SCOM2)
Description	NET CTRL1 register. (N/A in pervasive chiplets.)

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	PLL_CLKIN_SEL: PLL CLKIN select.
1	RWX	RWX_WAND	RWX_WOR	CLK_DCC_BYPASS_EN: POWER9 cache chiplet: L2-0, L2-1, L3 duty cycle control bypass. POWER9 core chiplet: Core duty cycle control bypass. POWER9 memory chiplet: Memory duty cycle control bypass.
2	RWX	RWX_WAND	RWX_WOR	CLK_PDLY_BYPASS_EN: POWER9 cache chiplet: L2-0, L2-1, L3 progdly bypass. POWER9 core chiplet: Core progdly bypass. POWER9 memory chiplet: Memory progdly bypass.
3	RWX	RWX_WAND	RWX_WOR	CLK_DIV_BYPASS_EN: Enables clock divider bypass.
4	RWX	RWX_WAND	RWX_WOR	REFCLK_CLKMUX0_SEL: Select for reference clock mux0.
5	RWX	RWX_WAND	RWX_WOR	REFCLK_CLKMUX1_SEL: Select for reference clock mux1.
6	RWX	RWX_WAND	RWX_WOR	PLL_BNDY_BYPASS_EN: Bypass for IOP PLL.
7	RWX	RWX_WAND	RWX_WOR	Reserved field.
8:15	RWX	RWX_WAND	RWX_WOR	DPLL_TEST_SEL: DPLL test out multiplexing.
16:19	RWX	RWX_WAND	RWX_WOR	SB_STRENGTH: Sector buffer driver strength.
20	RWX	RWX_WAND	RWX_WOR	ASYNC_TYPE:
21	RWX	RWX_WAND	RWX_WOR	ASYNC_OBS:
22	RWX	RWX_WAND	RWX_WOR	CPM_CAL_SET: CPM calibrate.
23	RWX	RWX_WAND	RWX_WOR	SENSEADJ_RESET0: POWER9 cache chiplet: L2-0 duty cycle adjustment reset.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
24	RWX	RWX_WAND	RWX_WOR	SENSEADJ_RESET1: POWER9 cache chiplet: L2-1 duty cycle adjustment reset.
25	RWX	RWX_WAND	RWX_WOR	CLK_PULSE_EN: Clock pulse mode enable.
26:27	RWX	RWX_WAND	RWX_WOR	CLK_PULSE_MODE: Clock pulse mode setting.
28:31	RWX	RWX_WAND	RWX_WOR	Reserved field.

Register Name	PPM General Power Management Mode Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_GPMMR
Address	00000000130F0100 (SCOM) 00000000130F0101 (SCOM1) 00000000130F0102 (SCOM2)
Description	PPM general power management mode register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_CLEAR	WOX_OR	Reserved field.
1	ROX	NCX	NCX	Reserved field.
2	ROX	NCX	NCX	Reserved field.
3	ROX	NCX	NCX	Reserved field.
4	ROX	NCX	NCX	Reserved field.
5	ROX	NCX	NCX	Reserved field.
6	RW	WO_CLEAR	WO_OR	Reserved field.
7	RW	WO_CLEAR	WO_OR	Reserved field.
8	RW	WO_CLEAR	WO_OR	Reserved field.
9	RW	WO_CLEAR	WO_OR	Reserved field.
10	RW	WO_CLEAR	WO_OR	Reserved field.
11	RO	NC	NC	Reserved field.
12:14	RW	WO_CLEAR	WO_OR	Reserved field.
15	RW	WO_CLEAR	WO_OR	Reserved field.
16:63	RO	RO	RO	constant = 0b000000000000000000000000000000000000000000000000

Register Name	QPPM QUAD Power Management Mode Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_QUAD_REGS.QPPM_QPMMR
Address	00000000130F0103 (SCOM) 00000000130F0104 (SCOM1) 00000000130F0105 (SCOM2)
Description	QPPM QUAD power management mode register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_CLEAR	WO_OR	QPPM_QPMMR_FORCE_FSAFE: Forces the FSAFE frequency override to occur as described in the next field.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
1:11	RW	WO_CLEAR	WO_OR	QPPM_QPMMR_FSAFE: Safe frequency. This field establishes the frequency to which the DPLL (and therefore QUAD) will be forced in SAFE mode (for example, if loss of the OCC heartbeat is detected and OCC_HEARTBEAT_EN is set). In this event, the hardware overrides the FMIN, FMAX, and FREQ_MULT fields in the QPPM DPLL Frequency Control Register to send this value to the DPLL instead. Note that when this occurs the HIRES portions of those frequency fields are overridden to zeroes. Firmware must ensure that this frequency is supported by all possible voltages (external and internal) and analog clocking circuits at the time. Failure to do so can result in unpredictable machine behavior.
12	RW	WO_CLEAR	WO_OR	QPPM_QPMMR_ENABLE_FSAFE_UPON_HEARTBEAT_LOSS:
13	RW	WO_CLEAR	WO_OR	QPPM_QPMMR_ENABLE_DROOP_PROTECT_UPON_HEARTBEAT_LOSS: When set, the QCCR[DROOP_PROTECT_DATA] is used based on the setting of ERR_REG [OCC_HEARTBEAT_LOSS].
14	RW	WO_CLEAR	WO_OR	QPPM_QPMMR_ENABLE_PFETS_UPON_IVRM_DROPOUT: **Note:** This bit must *always* be 0, such that this function is never used.
15	RO	RO	RO	constant = 0b0
16	RW	WO_CLEAR	WO_OR	QPPM_QPMMR_ENABLE_PCB_INTR_UPON_HEARTBEAT_LOSS: When set, the rising edge of OCC_HEARTBEAT_LOSS will cause an interrupt to the OCC complex.
17	RW	WO_CLEAR	WO_OR	QPPM_QPMMR_ENABLE_PCB_INTR_UPON_IVRM_DROPOUT: When set, the rising edge of IVRM_DROPOUT_ERR will cause an interrupt to the OCC complex.
18	RW	WO_CLEAR	WO_OR	QPPM_QPMMR_ENABLE_PCB_INTR_UPON_LARGE_DROOP: Final VDM data bit 1 (large droop detect).
19	RW	WO_CLEAR	WO_OR	QPPM_QPMMR_ENABLE_PCB_INTR_UPON_EXTREME_DROOP: Final VDM data bit 0 (extreme droop detect).
20	RW	WO_CLEAR	WO_OR	QPPM_QPMMR_CME_INTERPPM_IVRM_ENABLE: CME inter-PPM communication enable. iVRM enablement (including iVRM control and PFET control register addresses 0x01B0 – 0x01B2 and 0x0118 – 0x01A): 0 = Write access to the iVRM enablement subset of QUAD PPM registers from Core PPMs is disabled. 1 = Write access to the iVRM enablement subset of QUAD PPM registers from Core PPMs is enabled. CME_INTERPPM_IVRM_SEL selects between CorePPM1 and CorePPM2.
21	RW	WO_CLEAR	WO_OR	QPPM_QPMMR_CME_INTERPPM_IVRM_SEL: CME inter-PPM communication select. iVRM enablement: 0 = If CME_INTERPPM_IVRM_ENABLE = 1, CorePPM1 is enabled. 1 = If CME_INTERPPM_IVRM_ENABLE = 1, CorePPM2 is enabled. **Note:** If CME_INTERPPM_IVRM_ENABLE = 0, this bit has no effect.
22	RW	WO_CLEAR	WO_OR	QPPM_QPMMR_CME_INTERPPM_ACLK_ENABLE: CME inter-PPM communication enable. Analog clock controls (register addresses 0x0160 – 0x0162): 0 = Write access to the analog clock control subset of QUAD PPM registers from Core PPMs is disabled. 1 = Write access to the Analog Clock Control subset of QUAD PPM registers from Core PPMs is enabled. CME_INTERPPM_ANACLK_SEL selects between CorePPM1 and CorePPM2.
23	RW	WO_CLEAR	WO_OR	QPPM_QPMMR_CME_INTERPPM_ACLK_SEL: CME inter-PPM communication select. Analog clock controls: 0 = If CME_INTERPPM_ANACLK_ENABLE = 1, CorePPM1 is enabled. 1 = If CME_INTERPPM_ANACLK_ENABLE = 1, CorePPM2 is enabled. **Note:** If CME_INTERPPM_ANACLK_ENABLE = 0, this bit has no effect.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
24	RW	WO_CLEAR	WO_OR	QPPM_QPMMR_CME_INTERPPM_VDATA_ENABLE: CME inter-PPM communication enable. Voltage data control (PPM iVRM Data Value Register 0x01B4 and VDM Configuration and Control Registers 0x01B6 – 0x01BA). 0 = Write access to the voltage data control subset of QUAD PPM registers from Core PPMs is disabled. 1 = Write access to the voltage data control subset of QUAD PPM registers from Core PPMs is enabled. CME_INTERPPM_VDATA_SEL selects between CorePPM1 and CorePPM2.
25	RW	WO_CLEAR	WO_OR	QPPM_QPMMR_CME_INTERPPM_VDATA_SEL: CME inter-PPM communication select. Voltage data control: 0 = If CME_INTERPPM_VDATA_ENABLE = 1, CorePPM1 is enabled. 1 = If CME_INTERPPM_VDATA_ENABLE = 1, CorePPM2 is enabled. **Note:** If CME_INTERPPM_VDATA_ENABLE = 0, this bit has no effect.
26	RW	WO_CLEAR	WO_OR	QPPM_QPMMR_CME_INTERPPM_DPLL_ENABLE: CME inter-PPM communication enable. DPLL control registers (addresses 0x0151 – 0x0154): 0 = Write access to the DPLL control subset of QUAD PPM registers from Core PPMs is disabled. 1 = Write access to the DPLL control subset of QUAD PPM registers from Core PPMs is enabled. CME_INTERPPM_DPLL_SEL selects between CorePPM1 and CorePPM2.
27	RW	WO_CLEAR	WO_OR	QPPM_QPMMR_CME_INTERPPM_DPLL_SEL: CME inter-PPM communication select. DPLL control: 0 = If CME_INTERPPM_DPLL_ENABLE = 1, CorePPM1 is enabled 1 = If CME_INTERPPM_DPLL_ENABLE = 1, CorePPM2 is enabled **Note:** If CME_INTERPPM_ DPLL_ENABLE = 0, this bit has no effect.
28:31	RW	WO_CLEAR	WO_OR	QPPM_QPMMR_RESERVED28_31: Implemented but unused.
32:63	RO	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	PPM Special Wake-Up OTR Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_SPWKUP_OTR
Address	00000000130F010A (SCOM)
Description	PPM special wake-up OTR register

Bits	SCOM	Field Mnemonic: Description
0	RW	PPM_SPWKUP_OTR_OTR_SPECIAL_WKUP: Chiplet special wake-up for other firmware use. **Note:** Protocol is required when setting this bit.
1:63	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000000

Register Name	PPM Special Wake-Up FSP Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_SPWKUP_FSP
Address	00000000130F010B (SCOM)
Description	PPM special wake-up FSP register

Bits	SCOM	Field Mnemonic: Description
0	RW	PPM_SPWKUP_FSP_FSP_SPECIAL_WKUP: Chiplet special wake-up for FSP firmware use. **Note:** Protocol is required when setting this bit.

Bits	SCOM	Field Mnemonic: Description
1:63	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000000

Register Name	PPM Special Wake-Up OCC Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_SPWKUP_OCC
Address	00000000130F010C (SCOM)
Description	PPM special wake-up OCC register

Bits	SCOM	Field Mnemonic: Description
0	RW	PPM_SPWKUP_OCC_OCC_SPECIAL_WKUP: Chiplet special wake-up for OCC firmware use. **Note:** Protocol is required when setting this bit.
1:63	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000000

Register Name	PPM Special Wake-Up HYP Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_SPWKUP_HYP
Address	00000000130F010D (SCOM)
Description	PPM special wake-up HYP register

Bits	SCOM	Field Mnemonic: Description
0	RW	PPM_SPWKUP_HYP_HYP_SPECIAL_WKUP: Chiplet special wake-up for HYP firmware use. **Note:** Protocol is required when setting this bit.
1:63	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000000

Register Name	PPM Stop State History SRC Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_SSHSRC
Address	00000000130F0110 (SCOM)
Description	PPM stop state history SRC

Bits	SCOM	Field Mnemonic: Description
0	RW	Reserved field.
1	ROX	Reserved field.
2:3	RW	Reserved field.
4:7	RW	Reserved field.
8:11	RW	Reserved field.
12	WO_4P	Reserved field.
13	WO_4P	Reserved field.
14:63	RO	constant = 0b00000000000000000000000000000000000000000000000000

Register Name	PPM Stop State History FSP Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_SSHFSP
Address	00000000130F0111 (SCOM)
Description	PPM stop state history FSP

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	Reserved field.
2:3	ROX	Reserved field.
4:7	ROX	Reserved field.
8:11	ROX	Reserved field.
12:15	ROX_CLRPART	Reserved field.
16:19	ROX_CLRPART	Reserved field.
20	ROX_CLRPART	Reserved field.
21:63	RO	constant = 0b0000000000000000000000000000000000000000000

Register Name	PPM Stop State History OCC Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_SSHOCC
Address	00000000130F0112 (SCOM)
Description	PPM stop state history OCC

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	Reserved field.
2:3	ROX	Reserved field.
4:7	ROX	Reserved field.
8:11	ROX	Reserved field.
12:15	ROX_CLRPART	Reserved field.
16:19	ROX_CLRPART	Reserved field.
20	ROX_CLRPART	Reserved field.
21:63	RO	constant = 0b0000000000000000000000000000000000000000000

Register Name	PPM Stop State History OTR Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_SSHOTR
Address	00000000130F0113 (SCOM)
Description	PPM stop state history OTR

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	Reserved field.
2:3	ROX	Reserved field.
4:7	ROX	Reserved field.
8:11	ROX	Reserved field.
12:15	ROX_CLRPART	Reserved field.
16:19	ROX_CLRPART	Reserved field.
20	ROX_CLRPART	Reserved field.
21:63	RO	constant = 0b0000000000000000000000000000000000000000000

Register Name	PPM Stop State History HYP Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_SSHHYP
Address	00000000130F0114 (SCOM)
Description	PPM stop state history HYP

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	Reserved field.
2:3	ROX	Reserved field.
4:7	ROX	Reserved field.
8:11	ROX	Reserved field.
12:15	ROX_CLRPART	Reserved field.
16:19	ROX_CLRPART	Reserved field.
20	ROX_CLRPART	Reserved field.
21:63	RO	constant = 0b0000000000000000000000000000000000000000000

Register Name	PPM PFET Control State Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_PFCS
Address	00000000130F0118 (SCOM) 00000000130F0119 (SCOM1) 00000000130F011A (SCOM2)
Description	PPM PFET control state

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:1	RW	WO_CLEAR	WO_OR	PPM_PFCS_VDD_PFET_FORCE_STATE: Domain V_{DD} PFET force state. Provides a means for firmware to force the domain V_{DD} PFETs to well known end states using the hardware sequencing mechanisms: b00 = No operation. b01 = Force V_{off}. b10 = No operation (reserved). b11 = Force V_{on}. This field is valid only if bits 4:5 = 00 (that is, both vdd_pfet_val_override *and* vdd_pfet_sel_override are disabled).
2:3	RW	WO_CLEAR	WO_OR	PPM_PFCS_VCS_PFET_FORCE_STATE: Domain V_{CS} PFET force state. This field is used only in QUAD PPM; it is unused in Core PPM. It provides a means for firmware to force the domain V_{CS} PFETs to well known end states using the hardware sequencing mechanisms: b00 = No operation. b01 = Force V_{off}. b10 = No operation (reserved). b11 = Force V_{on}. This field is valid only if bits 6:7 = 00 (that is, both vcs_pfet_val_override *and* vcs_pfet_sel_override are disabled).
4	RW	WO_CLEAR	WO_OR	PPM_PFCS_VDD_PFET_VAL_OVERRIDE: Domain V_{DD} PFET value override.
5	RW	WO_CLEAR	WO_OR	PPM_PFCS_VDD_PFET_SEL_OVERRIDE: Domain V_{DD} PFET stage select override.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
6	RW	WO_CLEAR	WO_OR	PPM_PFCS_VCS_PFET_VAL_OVERRIDE: Domain V_{CS} PFET value override. For QUAD PPM use only. Unused in Core PPM.
7	RW	WO_CLEAR	WO_OR	PPM_PFCS_VCS_PFET_SEL_OVERRIDE: Domain V_{CS} PFET stage select override. For QUAD PPM use only. Unused in Core PPM.
8	RW	WO_CLEAR	WO_OR	PPM_PFCS_VDD_PFET_REGULATION_FINGER_EN: Domain V_{DD} PFET regulation finger enable. Intended to be used to control the regulation PFET enable when iVRMs are enabled. If this bit is asserted, the value of the PFET finger (eg pfet_enable(0)) is controlled by vdd_pfet_regulation_finger_value. If this bit is not asserted, the PFET finger is controlled by the PFET FSM and/or any relevant overrides in place.
9	RW	WO_CLEAR	WO_OR	PPM_PFCS_VDD_PFET_REGULATION_FINGER_VALUE: Domain V_{DD} PFET regulation finger value. Intended to be used to control the regulation PFET enable when iVRMs are enabled. If vdd_pfet_regulation_finger_enable = 1, a write to this bit sets the state of the V_{DD} PFET enable(0) regardless of the setting of the regular pfet_enable FSM. If it is not asserted, the PFET sequencer controls this finger with the vdd_pfet_enable_value.
10:11	RW	WO_CLEAR	WO_OR	PPM_PFCS_RESERVED_10_11: Implemented but unused.
12:19	RW	WO_CLEAR	WO_OR	PPM_PFCS_VDD_PFET_ENABLE_VALUE: V_{DD} PFET enable value. Intended for manual control override usage. A write to this field sets the state of the Core Domain PFET Enables directly. If vdd_pfet_val_override = 1, a write to this field sets the state of the core PFET Enables until core_vdd_pfet_val_override is cleared. If vdd_pfet_val_override = 0, a write to this field takes on the value for one cycle and then returns to the value produced by the core_vdd_pfet_valN hard-coded facilities. A write of this type is not recommended and might produce undefined results. Reads will return the present state.

20:23	RW	WO_CLEAR	WO_OR	PPM_PFCS_VDD_PFET_SEL_VALUE: V_{DD} PFET select value. Intended for manual control override usage. A write to this field will index value N into the vdd_power_enable register, where N is 0 to 8, if vdd_pfet_sel_override = 1. If vdd_pfet_sel_override = 0, the field is written but no further action is taken. 0x0 = 0b11111111 # On.
				0x1 = 0b01111111.
				0x2 = 0b00111111.
				0x3 = 0b00011111.
				0x4 = 0b00001111.
				0x5 = 0b00000111.
				0x6 = 0b00000011.
				0x7 = 0b00000001.
				0x8 = 0b00000000 # Off.
				0x9 to 0xF = Reserved reads will return the present state of the field.

24:31	RW	WO_CLEAR	WO_OR	PPM_PFCS_VCS_PFET_ENABLE_VALUE: V_{CS} PFET enable value. This field is used only in QUAD PPM; it is unused in Core PPM. It is intended for manual control override usage. A write to this field sets the state of the V_{CS} PFET Enables directly. If vcs_pfet_val_override = 1, a write to this field sets the state of the V_{CS} PFET Enables until vcs_pfet_val_override is cleared. If eco_vdd_pfet_val_override = 0, a write to this field takes on the value for one cycle and then returns to the value produced by the eco_vdd_pfet_valN_slat registers. A write of this type is not recommended and might produce undefined results. Reads will return the present state.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description

32:35	RW	WO_CLEAR	WO_OR	PPM_PFCS_VCS_PFET_SEL_VALUE: V_{CS} PFET select value. This field is used only in QUAD PPM; it is unused in Core PPM. It is intended for manual control override usage. A write to this field will index value N into the vcs_power_enable register, where N is 0 to 8, if vcs_pfet_sel_override = 1. If vcs_pfet_sel_override = 0, the field is written but no further action is taken.
				0x0 = 0b11111111 # On.
				0x1 = 0b01111111.
				0x2 = 0b00111111.
				0x3 = 0b00011111.
				0x4 = 0b00001111.
				0x5 = 0b00000111.
				0x6 = 0b00000011.
				0x7 = 0b00000001.
				0x8 = 0b00000000 # Off.
				0x9 to 0xF = Reserved. Reads will return the present state of the field.

36:41	RO	RO	RO	constant = 0b000000
42:45	ROX	NCX	NCX	PPM_PFCS_VDD_PG_STATE: Logic voltage power gate sequencer FSM (one hot): 0x8 = Idle. 0x4 = Increment. 0x2 = Decrement. 0x1 = Wait.
46:49	ROX	NCX	NCX	PPM_PFCS_VDD_PG_SEL: For debug, contains the actual index N of the domain V_{DD} PFET select value. See VDD_PFET_SEL_VALUE for encoding of N to power enable value.
50:53	ROX	NCX	NCX	PPM_PFCS_VCS_PG_STATE: Cache voltage domain power gate sequencer FSM (one hot). This field is used only in QUAD PPM; it is unused in Core PPM. 0x8 = Idle. 0x4 = Increment. 0x2 = Decrement. 0x1 = Wait.
54:57	ROX	NCX	NCX	PPM_PFCS_VCS_PG_SEL: This field is used only in QUAD PPM; it is unused in Core PPM. For debug, contains the actual index N of the domain V_{CS} PFET select value. See VCS_PFET_SEL_VALUE for encoding of N to power enable value.
58:63	RO	RO	RO	constant = 0b000000

Register Name	**PPM PFET Delay Register**
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_PFDLY
Address	00000000130F011B (SCOM)
Description	PPM PFET delay

Bits	SCOM	Field Mnemonic: Description
0:3	RW	PPM_PFDLY_POWDN_DLY: Delay used between steps powering down the domain. The delays in this register are in terms of the PPM clock period (2 ns) $\times 2^{(15 \text{ minus this value})}$. **Note:** Chooses the power of 2 bit position of pfet_pg_timer(0:15) which is running off pcb_nclk.
4:7	RW	PPM_PFDLY_POWUP_DLY: Delay used between steps powering up the domain. The delays in this register are in terms of the PPM clock period (2 ns) $\times 2^{(15 \text{ minus this value})}$. **Note:** Chooses the power of 2 bit position of pfet_pg_timer(0:15) which is running off pcb_nclk.
8:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	PPM PFET Sense Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_PFSNS
Address	00000000130F011C (SCOM)
Description	PPM PFET sense

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	Reserved field.
2	ROX	Reserved field.
3	ROX	Reserved field.
4:15	RO	Reserved field.
16:23	ROX	Reserved field.
24:31	ROX	Reserved field.
32:41	RO	constant = 0b0000000000
42:45	ROX	Reserved field.
46:49	ROX	Reserved field.
50:53	ROX	Reserved field.
54:57	ROX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	PPM PFET Off Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_PFOFF
Address	00000000130F011D (SCOM)
Description	PPM PFET off

Bits	SCOM	Field Mnemonic: Description
0:3	RW	PPM_PFOFF_VDD_VOFF_SEL: Pointer to the stage representing the V_{off} value for the V_{DD} PFETs. Power down sequences will stop after enabling this stage. Valid values: 0x0 through 0x8.
4:7	RW	PPM_PFOFF_VCS_VOFF_SEL: Pointer to the stage representing the V_{off} value for the V_{CS} PFETs. Power down sequences will stop after enabling this stage. Valid values: 0x0 through 0x8. This field is used only in QUAD PPM; it is unused in Core PPM.
8:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	PPM SCRATCH0 Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_SCRATCH0
Address	00000000130F011E (SCOM)
Description	PPM scratch0

Bits	SCOM	Field Mnemonic: Description
0:63	RW	PPM_SCRATCH0_DATA: Scratch Data 0.

Register Name	PPM SCRATCH1 Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_SCRATCH1
Address	00000000130F011F (SCOM)
Description	PPM scratch1

Bits	SCOM	Field Mnemonic: Description
0:63	RW	PPM_SCRATCH1_DATA: Scratch Data 1.

Register Name	QPPM ERRSUM Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_QUAD_REGS.QPPM_ERRSUM
Address	00000000130F0120 (SCOM)
Description	QPPM ERRSUM

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	QPPM_ERRSUM_PM_ERROR: An unmasked PPM error is present. Intended for use by special PCB multicast to see the error state of all QUAD chiplets with a single read.
1:63	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000000

Register Name	QPPM Error Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_QUAD_REGS.QPPM_ERR
Address	00000000130F0121 (SCOM)
Description	QPPM errors

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	QPPM_ERR_PCB_INTERRUPT_PROTOCOL_ERR: Firmware wrote the PPMPIG to request a PCB interrupt before its previously requested interrupt had been completed (meaning PPMPIG[PENDING_SOURCE(0)] = 1 OR (PPMPIG[INTR_GRANTED] AND [GRANTED_SOURCE](0)) = 1.
1	RWX_WCLEAR	QPPM_ERR_SPECIAL_WKUP_PROTOCOL_ERR: Firmware cleared its special wake-up request (indicated by GPMMR[SPECIAL_WKUP_REQUESTED] before GPMMR[SPECIAL_WKUP_DONE] was set. This violates our agreed upon protocol and potentially confuses the Hcode managing the state of the QUAD chiplets.
2	RWX_WCLEAR	QPPM_ERR_SPECIAL_WKUP_DONE_PROTOCOL_ERR: Hardware or firmware cleared the special wake-up done indicator after it was set although a special wake-up request was still active (indicated by GPMMR[SPECIAL_WKUP_REQUESTED] . This violates our agreed upon protocol and potentially confuses the Hcode managing the state of the QUAD (cache and core) chiplets.
3	RWX_WCLEAR	QPPM_ERR_PFET_SEQ_PROGRAM_ERR: The PFET sequencer reached an invalid state due to incorrect configuration by a program.
4	RWX_WCLEAR	QPPM_ERR_OCC_HEARTBEAT_LOSS: OCC heartbeat lost event occurred. When enabled in the QPMMR, this will bit will engage the FSAFE mode or cause an interrupt to the OCC complex.
5	RWX_WCLEAR	QPPM_ERR_L2_EX0_CLK_SYNC_ERR: The SKEWADJ macro violated the agreed protocol by changing the value of the CLK_SYNC_DONE without a corresponding CLK_SYNC_ENABLE change (that is, a rising edge of the DONE when ENABLE = 0 or a falling edge of the DONE when ENABLE = 1).

Bits	SCOM	Field Mnemonic: Description
6	RWX_WCLEAR	QPPM_ERR_L2_EX1_CLK_SYNC_ERR: The SKEWADJ macro violated the agreed protocol by changing the value of the CLK_SYNC_DONE without a corresponding CLK_SYNC_ENABLE change (that is, a rising edge of the DONE when ENABLE = 0 or a falling edge of the DONE when ENABLE = 1).
7	RWX_WCLEAR	QPPM_ERR_EDRAM_SEQUENCE_ERR: The user wrote an invalid sequence into either the EX0 or EX1 EDRAM_ENABLE_ENCODE fields of the EDRAM_CTRL_REG, but the resulting decoded ACTUAL controls remained unchanged to protect the eDRAM circuitry.
8	RWX_WCLEAR	QPPM_ERR_EDRAM_PGATE_ERR: The user tried to power gate either V_{DD} or V_{CS} in the cache chiplet when the ERAM was enabled, but the hardware forced PFET enable bit0 to keep power on to protect the eDRAM circuitry.
9	RWX_WCLEAR	QPPM_ERR_DPLL_INT_ERR: DPLL internal error.
10	RWX_WCLEAR	QPPM_ERR_DPLL_DYN_FMIN_ERR: DPLL Dynamic Fmin error.
11	RWX_WCLEAR	QPPM_ERR_DPLL_DCO_FULL_ERR: DPLL DCO full.
12	RWX_WCLEAR	QPPM_ERR_DPLL_DCO_EMPTY_ERR: DPLL DCO empty.
13:16	RWX_WCLEAR	QPPM_ERR_INVERTED_VDM_DATA: Final VDM droop data summary bits 0:3. These are the same as what feeds the DPLL dynamic encode data input, but inverted to create positive active signals.
17	RWX_WCLEAR	QPPM_ERR_CME0_IVRM_DROPOUT_ERR: CME0 signaled a dropout threshold condition, which is enabled via QPMMR. When enabled in QPMMR, this bit engages the IVRM_PROTECT mechanism or causes an interrupt to the OCC complex.
18	RWX_WCLEAR	QPPM_ERR_CME1_IVRM_DROPOUT_ERR: CME1 signaled a dropout threshold condition (which is then ORed with the above bit).
19	RWX_WCLEAR	QPPM_ERR_SPARE_19: Spare error bit.
20:23	RWX_WCLEAR	QPPM_ERR_SPARE_20_23: Spare error bits.
24:63	RO	constant = 0b0000000000000000000000000000000000000000

Register Name	QPPM Error Mask Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_QUAD_REGS.QPPM_ERRMSK
Address	00000000130F0122 (SCOM)
Description	QPPM error mask

Bits	SCOM	Field Mnemonic: Description
0:23	RW	QPPM_ERRMSK_RESERVED_0_23: Mask for this error: 0 = Not masked. 1 = Masked. When set, the corresponding bit is set in the Error Register but masked from being reported in the ERRSUM Register and to the FIR.
24:63	RO	constant = 0b0000000000000000000000000000000000000000

Register Name	QPPM DPLL Frequency Control Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_QUAD_REGS.QPPM_DPLL_FREQ
Address	00000000130F0151 (SCOM)
Description	QPPM DPLL frequency control

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:11	RW	QPPM_DPLL_FREQ_FMAX: When DPLL_PARM_CTRL_REG (ENABLE_FMAX_TARGET) = 1, this field contains the requested maximum DPLL frequency target. Otherwise, this field should be set to match the FREQ_MULT field below. This field is ignored by hardware and the value sent to the DPLL is replaced with the FSAFE value in the event of a OCC_HEARTBEAT_LOSS ERR when ENABLE_FSAFE_UPON_HEARTBEAT_LOSS is set (as reflected in DPLLSTAT[FSAFE_ACTIVE]).The frequency equation is the same as FREQ_MULT below. **Hardware Implementation Note:** Anticipating a divider of 8: FMAX(0:7), corresponding to bits 1:8 of this register, connect to: DPLL.FF_FMAX_MULT_INTG(0:7). FMAX(8:10), corresponding to bits 9:11 of this register, connect to: DPLL.FF_FMAX_MULT_FRAC(0:2).
12:15	RW	QPPM_DPLL_FREQ_HIRES_FMAX: Same description as HIRES_FREQ_MULT, below, but for FMAX control. In response to FSAFE activation, this field is ignored by hardware and the value sent to the DPLL is replaced by all zeroes. **Hardware Implementation Note:** Anticipating a divider of 8: HIRES_FMAX(0:4), corresponding to bits 12:15 of this register, connect to: DPLL.FF_FMAX_MULT_FRAC(3:6). Note that this excludes DPLL.FF_FMAX_MULT_FRAC(7), which is tied to zero.
16	RO	constant = 0b0
17:27	RW	QPPM_DPLL_FREQ_FMULT: Primary DPLL frequency multiplier input, used to define the DPLL frequency target. This value is used in the absence of droop events when DPLL_PARM_CTRL_REG [ENABLE_JUMP_PROTECT] = 1 and in the absence of voltage overshoot or undershoot when DPLL_PARM_CTRL_REG [ENABLE_FMAX_TARGET] = 1 or DPLL_PARM_CTRL_REG [ENABLE_FMIN_TARGET] = 1, respectively. This field is ignored by hardware and the value sent to the DPLL is replaced with the FSAFE value in response to FSAFE activation. The frequency given is FMULT x (REFCLK DPLL_DIVIDER). With a REFCLK of 133 MHz and DPLL_DIVIDER of 8 yields FMAX x 16.667 MHz. This allows a range from 0 to 8.5GHz to be set although practical timing limits will not allow this full range to be realized. **Hardware Implementation Note:** Anticipating a divider of 8: FMULT(0:7), corresponding to bits 17:24 of this register, connect to: DPLL.MULT_INTG(0:7). FMULT(8:10), corresponding to bits 25:27 of this register, connect to: DPLL.MULT_FRAC(0:2).
28:31	RW	QPPM_DPLL_FREQ_HIRES_FMULT: This field provides frequency control with a resolution greater than 16.67 Mhz such that all DPLL inputs can be controlled. However, this field is anticipated to be all zero since the Pstate resolution planned to be 16.67Mhz. **Hardware Implementation Note:** Anticipating a divider of 8: HIRES_FMULT(0:4), corresponding to bits 28:31 of this register, connect to: DPLL.MULT_FRAC(3:6). Note that this excludes FF_MULT_FRAC(7), which is tied to zero.
32	RO	constant = 0b0
33:43	RW	QPPM_DPLL_FREQ_FMIN: Minimum DPLL frequency only used in Dynamic DPLL mode when DPLL_PARM_CTRL_REG[ENABLE_FMIN_TARGET] = 1'. Note that this field is *not* honored when DPLL_PARM_CTRL_REG[ENABLE_JUMP_PROTECT] = 1 and a droop event occurs. This field is ignored by hardware and the value sent to the DPLL is replaced with the FSAFE value in response to FSAFE activation. The frequency equation is the same as FMAX. **Hardware Implementation Note:** Anticipating a divider of 8: FMIN(0:7), corresponding to bits 33:40 of this register, connect to: DPLL.FMIN_MULT_INTG(0:7). FMIN(8:10), corresponding to bits 41:43 of this register, connect to: DPLL.FMIN_MULT_FRAC(0:2).
44:47	RW	QPPM_DPLL_FREQ_HIRES_FMIN: Same description as HIRES_FREQ_MULT, but for FMIN control. **Hardware Implementation Note:** Anticipating a divider of 8: HIRES_FMIN(0:4), corresponding to bits 44:47 of this register, connect to: DPLL.FMIN_MULT_FRAC(3:6). Note that this excludes FF_MULT_FRAC(7), which is tied to zero.

Bits	SCOM	Field Mnemonic: Description
48:62	RO	constant = 0b000000000000000

Register Name	QPPM DPLL Control Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_QUAD_REGS.QPPM_DPLL_CTRL
Address	00000000130F0152 (SCOM) 00000000130F0153 (SCOM1) 00000000130F0154 (SCOM2)
Description	QPPM DPLL control

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_CLEAR	WO_OR	QPPM_DPLL_CTRL_DPLL_LOCK_SEL: DPLL lock sensitivity select.
1	RW	WO_CLEAR	WO_OR	QPPM_DPLL_CTRL_ENABLE_JUMP_PROTECT: Allow the DPLL to instantly drop frequency by a configured amount in response to the dynamic encoded input bits.
2	RW	WO_CLEAR	WO_OR	QPPM_DPLL_CTRL_FF_BYPASS: Enables frequency filter bypass.
3	RW	WO_CLEAR	WO_OR	QPPM_DPLL_CTRL_DCO_OVERRIDE: Enables the following two fields to control the DCO manually in a special manufacturing test mode for DPLL characterization.
4	RW	WO_CLEAR	WO_OR	QPPM_DPLL_CTRL_DCO_INCR: Increments DCO control logic for manufacturing test mode.
5	RW	WO_CLEAR	WO_OR	QPPM_DPLL_CTRL_DCO_DECR: Decrements DCO control logic for manufacturing test mode.
6:15	RW	WO_CLEAR	WO_OR	QPPM_DPLL_CTRL_FF_SLEWRATE: Out of lock slew rate for DPLL to use when changing frequency (when not performing droop recovery).
16	RW	WO_CLEAR	WO_OR	QPPM_DPLL_CTRL_SS_ENABLE: Spread spectrum mode enable. Not planned for use on POWER9. Should be left as 0. Causes DPLL to oscillate between ff_min_[intg|frac] and mult_[intg|frac] settings.
17:19	RW	WO_CLEAR	WO_OR	QPPM_DPLL_CTRL_RESERVED_17_19: Implemented but not used.
20	RW	WO_CLEAR	WO_OR	QPPM_DPLL_CTRL_SLEW_DN_SEL: When set, the scan-only slew_rate_dn latches in the DPLL control the slew down rate such that it can react faster.
21	RW	WO_CLEAR	WO_OR	QPPM_DPLL_CTRL_ENABLE_JUMP_TARGET_UPDATE: If this bit is set, the DPLL constantly samples the DCO to calculate the jump amount, meaning it jumps relative to the present frequency on the cycle the droop happens, not relative to the nominal frequency (Fmult). Therefore, if this bit is not set and ENABLE_FMIN_TARGET is set, then guardbanding must be done against Fmin (instead of Fmult) minus the large drop amount.
22	RW	WO_CLEAR	WO_OR	QPPM_DPLL_CTRL_ENABLE_FMIN_TARGET: When set, causes DPLL to slew down to Fmin when dynamic encoded data = 0xC. If ENABLE_JUMP_PROTECT is also set, dynamic encoded data of 0x8 causes a small (instead of large) drop amount . When this bit is not set and ENABLE_JUMP_PROTECT = 1, then 0xC causes a small drop and 0x8 causes a large drop instead.
23	RW	WO_CLEAR	WO_OR	QPPM_DPLL_CTRL_ENABLE_FMAX_TARGET: When set, causes DPLL to slew up to Fmax when dynamic encoded data = 0xF, and Fmult when 0xE.
24:63	RO	RO	RO	constant = 0b0000000000000000000000000000000000000000

Register Name	QPPM DPLL Output Status Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_QUAD_REGS.QPPM_DPLL_STAT
Address	00000000130F0155 (SCOM)
Description	QPPM DPLL output status register

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:11	ROX	QPPM_DPLL_STAT_FREQOUT: Digital numeric output from the DPLL indicating what full speed frequency it is currently driving on the Core and L2 clock grids. (The L3 grid is driven by this frequency / 2.) This register bits 0:11 are scaled the same as the FMIN and FMAX settings in the DPLL_FREQ register, so the same equation can be used to convert this number to MHz. **Hardware Implementation Note:** FREQOUT(0:7), corresponding to bits 1:8 of this register, connect to FF_MULT_INTG_OUT(0:7) FREQOUT(8:10), corresponding to bits 9:11 of this register, connect to FF_MULT_FRAC_OUT(0:2).
12:16	ROX	QPPM_DPLL_STAT_HIRES_FREQOUT: Higher resolution, extended portion of the frequency output of the DPLL. **Hardware Implementation Note:** Connected to FF_MULT_FRAC_OUT(3:7).
17:56	RO	constant = 0b0000000000000000000000000000000000000000
57:58	RO	QPPM_DPLL_STAT_RESERVED_57_59: Implemented but not used.
59	ROX	QPPM_DPLL_STAT_FSAFE_ACTIVE: Set when (ERR[OCC_HEARTBEAT_LOSS] *and* QPMMR[ENABLE_FSAFE_UPON_HEARTBEAT_LOSS]) = 1, indicating that the hardware is forcing the frequency inputs of the DPLL to FSAFE instead of the values in the DPLL Frequency Control Register.
60	ROX	QPPM_DPLL_STAT_UPDATE_COMPLETE: Indicates that the internal DPLL save point is at the requested FNOM target.
61	ROX	QPPM_DPLL_STAT_FREQ_CHANGE: DPLL Frequency change is ongoing (output of DPLL). **Note:** This is asserted whenever the DPLL is slewing to a new target.
62	ROX	QPPM_DPLL_STAT_BLOCK_ACTIVE: DPLL output indicating that a droop recovery is in progress and no frequency updates are being processed.
63	ROX	QPPM_DPLL_STAT_LOCK: DPLL Lock Indicator (flock output from DPLL).

Register Name	QPPM DPLL Output Characterization Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_QUAD_REGS.QPPM_DPLL_OCHAR
Address	00000000130F0156 (SCOM)
Description	QPPM DPLL output characterization register

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:11	ROX	QPPM_DPLL_OCHAR_FREQOUT_MAX: Contains the largest value of the DPLL frequency output seen since the last read of this register (updated every cycle). This field is set to FF_MULT_INTG_OUT(0:7) : FF_MULT_FRAC_OUT(0:2) when this register is read or if that value is larger than this field.
12:16	ROX	QPPM_DPLL_OCHAR_HIRES_FREQOUT_MAX: Contains the largest value of the DPLL frequency output seen since the last read of this register (updated every cycle). This field is set to FF_MULT_FRAC_OUT(3:7) when this register is read or if FF_MULT_INTG_OUT(0:7) : FF_MULT_FRAC_OUT(0:7) is larger than FREQOUT_MAX : HIRES_FREQOUT_MAX.
17:20	RO	constant = 0b0000

Bits	SCOM	Field Mnemonic: Description
21:31	ROX	QPPM_DPLL_OCHAR_FREQOUT_AVG: Contains a running average of the value of the DPLL frequency output. On a read, this field is set to the DPLL FF_MULT_INTG_OUT(0:7) : FF_MULT_FRAC_OUT(0:2). Otherwise, this field updates (increments or decrements) based on the signed carryout of the next field.
32:36	ROX	QPPM_DPLL_OCHAR_HIRES_FREQOUT_AVG: Contains a running average of the value of the DPLL frequency HIRES_FREQ_MULT input. On a read to this register, this field is set to FF_MULT_FRAC_OUT(3:7). Otherwise, this field increments by 1 if the FF_MULT_INTG_OUT(0:7) : FF_MULT_FRAC_OUT(0:7) is greater than FREQOUT_AVG : HIRES_FREQOUT_AVG or decrements by 1 if the value is less.
37:40	RO	constant = 0b0000
41:51	ROX	QPPM_DPLL_OCHAR_FREQOUT_MIN: Contains the smallest value of the DPLL frequency output seen since the last read of this register (updated every cycle). This field is set to FF_MULT_INTG_OUT(0:7) : FF_MULT_FRAC_OUT(0:2) when this register is read or if that value is smaller than this field.
52:56	ROX	QPPM_DPLL_OCHAR_HIRES_FREQOUT_MIN: Contains the smallest value of the DPLL frequency output seen since the last read of this register (updated every cycle). This field is set to FF_MULT_FRAC_OUT(3:7) when this register is read or if FF_MULT_INTG_OUT(0:7) : FF_MULT_FRAC_OUT(0:7) is smaller than FREQOUT_MIN : HIRES_FREQOUT_MIN.
57:63	RO	constant = 0b0000000

Register Name	QPPM DPLL Input Characterization Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_QUAD_REGS.QPPM_DPLL_ICHAR
Address	00000000130F0157 (SCOM)
Description	QPPM DPLL input characterization register

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:11	ROX	QPPM_DPLL_ICHAR_FREQIN_AVG: Contains a running average of the value of the DPLL Frequency FREQ_MULT Input. On a read to this register, this field is set to DPLL_FREQ[FREQIN] . Otherwise, this field updates (increments or decrements) based on the signed carryout of the next field.
12:16	ROX	QPPM_DPLL_ICHAR_HIRES_FREQIN_AVG: Contains a running average of the value of the DPLL Frequency HIRES_FREQ_MULT Input. On a read to this register, this field is set to DPLL_FREQ[HIRES_FREQIN] . Otherwise, this field increments by 1 if the MULT : HIRES_MULT is greater than FREQIN_AVG : HIRES_FREQIN_AVG or decrements by 1 if the value is less.
17:20	RO	constant = 0b0000
21:31	ROX	QPPM_DPLL_ICHAR_FREQIN_MAX: Contains the largest value provided to the DPLL frequency MULT input since the last read of this register. This field is set to DPLL_FREQ[FREQIN] when this register is read or if that field is written with a value larger than this field.
32:36	ROX	QPPM_DPLL_ICHAR_HIRES_FREQIN_MAX: Contains the largest value of the DPLL frequency output seen since the last read of this register (updated every cycle). This field is set to HIRES_FREQIN when this register is read or if FREQIN : HIRES_FREQIN is larger than FREQIN_MAX : HIRES_FREQIN_MAX.
37:40	RO	constant = 0b0000
41:51	ROX	QPPM_DPLL_ICHAR_FREQIN_MIN: Contains the smallest value of the DPLL frequency MULT input since the last read of this register. This field is set to DPLL_FREQ[FREQIN] when this register is read or if that field is written with a value smaller than this field.
52:56	ROX	QPPM_DPLL_ICHAR_HIRES_FREQIN_MIN: Contains the smallest value of the DPLL frequency output seen since the last read of this register (updated every cycle). This field is set to HIRES_FREQIN when this register is read or if FREQIN : HIRES_FREQIN is smaller than FREQIN_MIN : HIRES_FREQIN_MIN.
57:63	RO	constant = 0b0000000

Register Name	QPPM OCC Heartbeat Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_QUAD_REGS.QPPM_OCCHB
Address	00000000130F015F (SCOM)
Description	QPPM OCC heartbeat

Bits	SCOM	Field Mnemonic: Description
0:15	RW	QPPM_OCCHB_OCC_HEARTBEAT_COUNT: When written, this field defines the starting value for a counter that increments at ~1 µs if OCC_HEARTBEAT_EN = 1 and the counter value is non-zero. If OCC_HEARTBEAT_EN = 0 or the counter value is 0, the counter does not increment. A heartbeat lost event occurs if OCC_HEARTBEAT_EN = 1 and this counter becomes 0 (as a result of either a written value or counter wrapping). The pulses used by this counter come from a free running pervasive hang timer pulse (PM_Hang_Pulse) programmed to be ~32 ns that has a 5-bit precounter whose carryout forms a resultant ~1 µs decremented pulse. Upon writing this register with OCC_HEARTBEAT_EN = 1, the precounter is cleared and will begin counting upon the next PM_Hang_Pulse. This PM_Hang_Pulse might arrive immediately or a full duration later. With a (215 - 1) range and a ~1µs incremented time yields a heartbeat range of 1 µs (+ 0 to 32 ns) (value 0xFFFF) to 65.535 µs (+ 0 to 32 ns) (value 0x0001). The value chosen to be written for debug purposes only, writing 0x0000 will cause an immediate heartbeat_lost if OCC_HEARTBEAT_EN = 1. Reads return the current value of the counter. Firmware must establish the PPM_DPLL_PARM_REG[FSAFE] frequency value before writing this field with OCC_HEARTBEAT_EN = 1. A heartbeat lost event causes the following action: Force the DPLL to the frequency defined in QPMMR[FSAFE] if enabled by QPMMR[ENABLE_FSAFE_UPON_HEARTBEAT_LOSS].
16	RW	QPPM_OCCHB_OCC_HEARTBEAT_ENABLE:
17:63	RO	constant = 0b00000000000000000000000000000000000000000000000

Register Name	QPPM QUAD Analog Clock Control Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_QUAD_REGS.QPPM_QACCR
Address	00000000130F0160 (SCOM) 00000000130F0161 (SCOM1) 00000000130F0162 (SCOM2)
Description	QPPM QUAD analog clock control register. **Notes:** 1. The first 8 bits (0:7) are sent to the core PPMs, where they are only used if CACCR [QUAD_CLK_SB_OVERRIDE] is set, and used by the L2 clock grid controls based on EXCGCR[L2_EX[01]_CLK_SB_OVERRIDE]. 2. The next 5 bits (8:12) are sent to the core PPMs, where they are only used if CACCR [QUAD_CLK_SW_OVERRIDE] is set, and used by the L2 clock grid controls if EXCGCR[L2_EX[01]_CLK_SW_OVERRIDE].

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:3	RW	WO_CLEAR	WO_OR	QPPM_QACCR_COMMON_CLK_SB_STRENGTH: Common clock sector buffer strength(0:3) selectively distributed to the core chiplets and L2 clock regions.
4	RW	WO_CLEAR	WO_OR	QPPM_QACCR_COMMON_CLK_SB_SPARE: Reserved for future use; available as a common spare.
5	RW	WO_CLEAR	WO_OR	QPPM_QACCR_COMMON_CLK_SB_PULSE_MODE_EN: Common pulse mode enable to clock sector buffers.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
6:7	RW	WO_CLEAR	WO_OR	QPPM_QACCR_COMMON_CLK_SB_PULSE_MODE: Common pulse mode(0:1) to clock sector buffers: 00 = Safest (Widest) Pulse. 01 = Wide Pulse. 10 = Narrow Pulse. 11 = Medium Pulse.
8:11	RW	WO_CLEAR	WO_OR	QPPM_QACCR_COMMON_CLK_SW_RESCLK: Common resonant clock inductor switch(0:3).
12	RW	WO_CLEAR	WO_OR	QPPM_QACCR_COMMON_CLK_SW_SPARE: Reserved for future use; available as a common spare.
13:15	RW	WO_CLEAR	WO_OR	QPPM_QACCR_RESERVED_13_15: Implemented but not used.
16:19	RW	WO_CLEAR	WO_OR	QPPM_QACCR_L3_CLK_SB_STRENGTH: Clock sector buffer strength(0:3) for the cache chiplet L3 grid.
20	RW	WO_CLEAR	WO_OR	QPPM_QACCR_L3_CLK_SB_SPARE0: Implemented but not used.
21	RW	WO_CLEAR	WO_OR	QPPM_QACCR_L3_CLK_SB_PULSE_MODE_EN: Pulse mode enable to clock sector buffers for the cache chiplet L3 grid.
22:23	RW	WO_CLEAR	WO_OR	QPPM_QACCR_L3_CLK_SB_PULSE_MODE: Pulse mode(0:1) to clock sector buffers for the cache chiplet L3 grid. 00 = Safest (Widest) Pulse. 01 = Wide Pulse. 10 = Narrow Pulse. 11 = Medium Pulse.
24:63	RO	RO	RO	constant = 0b0000000000000000000000000000000000000000

Register Name	QPPM QUAD Analog Clock Status Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_QUAD_REGS.QPPM_QACSR
Address	00000000130F0163 (SCOM)
Description	QPPM QUAD analog clock status register

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	QPPM_QACSR_ACTUAL_L2_EX0_CLK_SB_STRENGTH: Actual value being driven on the sector buffer strength(0:3) output for the L2 EX0 subdomain.
4	ROX	QPPM_QACSR_ACTUAL_L2_EX0_CLK_SB_SPARE0: Spare. (Not used.)
5	ROX	QPPM_QACSR_ACTUAL_L2_EX0_CLK_SB_PULSE_MODE_EN: Actual value being driven on the pulse mode enable output for this core chiplet.
6:7	ROX	QPPM_QACSR_ACTUAL_L2_EX0_CLK_SB_PULSE_MODE: Actual value being driven on the pulse mode(0:1) output for this core chiplet.
8:11	ROX	QPPM_QACSR_ACTUAL_L2_EX0_CLK_SW_RESCLK: Actual value being driven on the resonant clock inductor switch(0:3) output for this core chiplet.
12	ROX	QPPM_QACSR_ACTUAL_L2_EX0_CLK_SW_SPARE1: Spare. (Not used.)
13:15	RO	constant = 0b000
16:19	ROX	QPPM_QACSR_ACTUAL_L2_EX1_CLK_SB_STRENGTH: Actual value being driven on the sector buffer strength(0:3) output for this core chiplet.
20	ROX	QPPM_QACSR_ACTUAL_L2_EX1_CLK_SB_SPARE0: Spare. (Not used.)
21	ROX	QPPM_QACSR_ACTUAL_L2_EX1_CLK_SB_PULSE_MODE_EN: Actual Value being driven on the Pulse Mode Enable output for this Core chiplet.

Bits	SCOM	Field Mnemonic: Description
22:23	ROX	QPPM_QACSR_ACTUAL_L2_EX1_CLK_SB_PULSE_MODE: Actual value being driven on the pulse mode(0:1) output for this core chiplet.
24:27	ROX	QPPM_QACSR_ACTUAL_L2_EX1_CLK_SW_RESCLK: Actual value being driven on the resonant clock inductor switch(0:3) output for this core chiplet.
28	ROX	QPPM_QACSR_ACTUAL_L2_EX1_CLK_SW_SPARE1: Spare. (Not used.)
29:35	RO	constant = 0b0000000
36	ROX	QPPM_QACSR_L2_EX0_CLK_SYNC_DONE: Clock sync enable to the analog clock SKEWADJ macro for the L2 EX0 clock grid. When changing the corresponding EXCGCR[SYNC_ENABLE] bit, code must wait for this bit to transition to the same value before proceeding. The SKEWADJ macro is not allowed to change the value of this signal unless the corresponding enable changes first; otherwise, the corresponding ERR[L2_EX0_CLK_SYNC_ERR] will be set. **Note:** When SKEWADJ is in hold mode, this signal will be asserted all the time.
37	ROX	QPPM_QACSR_L2_EX1_CLK_SYNC_DONE: Clock sync enable to the analog clock SKEWADJ macro for the L2 EX1 clock grid. Same as above.
38:63	RO	constant = 0b00000000000000000000000000

Register Name	PPM Clock Grid Control Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_CGCR
Address	00000000130F0164 (SCOM)
Description	PPM clock grid control register

Bits	SCOM	Field Mnemonic: Description
0	RW	PPM_CGCR_CLKGLM_ASYNC_RESET: Glitchless clock multiplexer asynchronous reset for this chiplet.
1:2	RW	PPM_CGCR_RESERVED_1_2: Implemented but not used.
3	RW	PPM_CGCR_CLKGLM_SEL: Glitchless clock multiplexer select for this chiplet. 0 = Reference clock. 1 = DPLL output (full speed Div1 for core, half speed Div2 for cache).
4:63	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000

Register Name	QPPM EX Clock Grid Control Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_QUAD_REGS.QPPM_EXCGCR
Address	00000000130F0165 (SCOM) 00000000130F0166 (SCOM1) 00000000130F0167 (SCOM2)
Description	QPPM EX clock grid control register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:3	RW	WO_CLEAR	WO_OR	QPPM_EXCGCR_L2_EX0_CLK_SB_STRENGTH: Clock sector buffer strength(0:3) for the L2 EX0 clock grid.
4	RW	WO_CLEAR	WO_OR	QPPM_EXCGCR_L2_EX0_CLK_SB_SPARE0: Implemented but not used. Reserved for future use.
5	RW	WO_CLEAR	WO_OR	QPPM_EXCGCR_L2_EX0_CLK_SB_PULSE_MODE_EN: Pulse mode enable to clock sector buffers for the L2 EX0 clock grid.26:27.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
6:7	RW	WO_CLEAR	WO_OR	QPPM_EXCGCR_L2_EX0_CLK_SB_PULSE_MODE: Pulse mode(0:1) to Clock sector buffers for the L2 EX0 clock grid. 00 = Safest (Widest) Pulse. 01 = Wide Pulse. 10 = Narrow Pulse. 11 = Medium Pulse.
8:11	RW	WO_CLEAR	WO_OR	QPPM_EXCGCR_L2_EX0_CLK_SW_RESCLK: Resonant clock inductor switch(0:3) for the L2 EX0 clock grid.
12	RW	WO_CLEAR	WO_OR	QPPM_EXCGCR_L2_EX0_CLK_SW_SPARE1: Implemented but not used. Reserved for future use.
13:15	RW	WO_CLEAR	WO_OR	QPPM_EXCGCR_RESERVED_13_15: Implemented but not used.
16:19	RW	WO_CLEAR	WO_OR	QPPM_EXCGCR_L2_EX1_CLK_SB_STRENGTH: Clock sector buffer strength(0:3) for the L2 EX1 clock grid.
20	RW	WO_CLEAR	WO_OR	QPPM_EXCGCR_L2_EX1_CLK_SB_SPARE0: Implemented but not used.
21	RW	WO_CLEAR	WO_OR	QPPM_EXCGCR_L2_EX1_CLK_SB_PULSE_MODE_EN: Pulse mode enable to clock sector buffers for the L2 EX1 clock grid.
22:23	RW	WO_CLEAR	WO_OR	QPPM_EXCGCR_L2_EX1_CLK_SB_PULSE_MODE: Pulse mode(0:1) to clock sector buffers for the L2 EX1 clock grid. 00 = Safest (Widest) Pulse. 01 = Wide Pulse. 10 = Narrow Pulse. 11 = Medium Pulse.
24:27	RW	WO_CLEAR	WO_OR	QPPM_EXCGCR_L2_EX1_CLK_SW_RESCLK: Resonant clock inductor switch(0:3) for the L2 EX1 clock grid.
28	RW	WO_CLEAR	WO_OR	QPPM_EXCGCR_L2_EX1_CLK_SW_SPARE1: Implemented but not used. Reserved for future use.
29:31	RW	WO_CLEAR	WO_OR	QPPM_EXCGCR_RESERVED_29_31: Implemented but not used.
32	RW	WO_CLEAR	WO_OR	QPPM_EXCGCR_L2_EX0_CLKGLM_ASYNC_RESET: Glitchless clock multiplexer asynchronous reset for the L2 cache EX0 domain.
33	RW	WO_CLEAR	WO_OR	QPPM_EXCGCR_L2_EX1_CLKGLM_ASYNC_RESET: Glitchless clock multiplexer asynchronous reset for the L2 cache EX1 domain.
34	RW	WO_CLEAR	WO_OR	QPPM_EXCGCR_L2_EX0_CLKGLM_SEL: Glitchless clock multiplexer select for the L2 cache EX0 domain. 0 = Reference clock. 1 = DPLL output (full speed Div1 for core, half speed Div2 for cache).
35	RW	WO_CLEAR	WO_OR	QPPM_EXCGCR_L2_EX1_CLKGLM_SEL: Glitchless clock multiplexer select for the L2 cache EX1 domain. 0 = Reference clock. 1 = DPLL output (full speed Div1 for core, half speed Div2 for cache).
36	RW	WO_CLEAR	WO_OR	QPPM_EXCGCR_L2_EX0_CLK_SYNC_ENABLE: Clock sync enable to the analog clock SKEWADJ macro for the L2 EX0 clock grid. Firmware must assert, then wait for the corresponding QACSR bit to assert, before enabling at-speed (non reference clock) functional clocks on the grid. Likewise, firmware must de-assert, and wait for the corresponding QACSR bit to de-assert, before switching the clock grid away from full speed clocks (that is, DPLL). This signal must remain asserted for the clock grid to remain synchronous with the other (core and L3) grids in the QUAD.
37	RW	WO_CLEAR	WO_OR	QPPM_EXCGCR_L2_EX1_CLK_SYNC_ENABLE: Clock sync enable to the analog clock SKEWADJ macro for the L2 EX1 clock grid. The same requirements as L2_EX0_CLK_SYNC_ENABLE apply.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
38	RW	WO_CLEAR	WO_OR	QPPM_EXCGCR_L2_EX0_CLK_SB_OVERRIDE: When set, use QACCR(0:7) instead of this register (0:7) to feed the clock sector buffer controls for the L2 EX0 clock grid.
39	RW	WO_CLEAR	WO_OR	QPPM_EXCGCR_L2_EX1_CLK_SB_OVERRIDE: When set, use QACCR(0:7) instead of this register(16:23) to feed the clock sector buffer controls for the L2 EX1 clock grid.
40	RW	WO_CLEAR	WO_OR	QPPM_EXCGCR_L2_EX0_CLK_SW_OVERRIDE: When set, use QACCR(8:12) instead of this register (8:12) to feed the resonant clock switch controls for the L2 EX0 clock grid.
41	RW	WO_CLEAR	WO_OR	QPPM_EXCGCR_L2_EX1_CLK_SW_OVERRIDE: When set, use QACCR(8:12) instead of this register (24:28) to feed the resonant clock switch controls for the L2 EX1 clock grid.
42:63	RO	RO	RO	constant = 0b0000000000000000000000

Register Name	**PPM PCB Interrupt Generation Register**
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_PIG
Address	00000000130F0180 (SCOM)
Description	PPM PCB interrupt generation register

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b1
1:3	RW	PPM_PIG_REQ_INTR_TYPE: PCB interrupt request type (written by Hcode).
4:15	RW	PPM_PIG_REQ_INTR_PAYLOAD: PCB interrupt request payload (written by Hcode).
16:31	ROX	PPM_PIG_GRANTED_PACKET: Granted interrupt packet content. If INTR_GRANTED is 1, this field contains the interrupt currently being sent; otherwise, it contains the interrupt most recently sent. The format depends on the value of the GRANTED_SOURCE field: 01 = Copied from bits 0:15 of this register. 10 = Core = 0x[AB]YXW; QUAD = 0xE80W. 11 = Core = 0xD801; QUAD = 0xF80Z. where: [A or B] is decided by CPMMR[STOP_EXIT_TYPE_SEL]. Y = 0x8, or 0xC if malfunction alert is present. X = The state of the external interrupts (MSGSND, OS, HYP, '0'). W = The state of the four special wake-up sources (OTR, FSP, OCC, HYP). Z = Encoded hardware error indication (0; voltage droop; iVRM dropout; OCC heartbeat loss). **Note:** By convention, bit 4, when set, typically indicates a hardware-generated interrupt, although for the QUAD type 6 and 7, this bit is not latched in the OCB.
32	ROX	PPM_PIG_INTR_GRANTED: An interrupt request is in process. The value of this bit determines the meaning of the other bits in this register: 0 = Contains information about the most recent interrupt that was sent. 1 = Reflects the interrupt currently being sent. This bit is set when the arbiter issues a grant to the source reflected in the GRANTED_SOURCE field. This bit is cleared when the granted interrupt receives a Receive ACK.
33	RO	constant = 0b0
34:35	ROX	PPM_PIG_GRANTED_SOURCE: Interrupt source currently or most recently granted to place an interrupt on the PCB network (encoded). 00 = No interrupt has ever been processed. 01 = SCOM request (Maps to PENDING_SOURCE 001). 10 = Hardware stop exit (maps to PENDING_SOURCE 010). 11 = Hardware error notification (maps to PENDING_SOURCE 100).

Bits	SCOM	Field Mnemonic: Description
36	RO	constant = 0b0
37:39	ROX	PPM_PIG_PENDING_SOURCE: Bit per interrupt source indicating which are currently waiting for arbitration. xx1 = SCOM request from CME (in bits 0:15 of this register). x1x = Hardware stop exit. 1xx = Hardware error (CPPM: CME; QPPM: OCC heartbeat).
40	RWX_WCLEAR	PPM_PIG_NETWORK_RESET_OCCURRED: Sticky bit set when a network reset occurs (debug use only) and cleared only on SCOM write of this bit to one. **Note:** For indication only; network reset has no other effect on PPM.
41:63	RO	constant = 0b00000000000000000000000

Register Name	**PPM iVRM Control Register**
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_IVRMCR
Address	00000000130F01B0 (SCOM) 00000000130F01B1 (SCOM1) 00000000130F01B2 (SCOM2)
Description	PPM iVRM control register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_CLEAR	WO_OR	PPM_IVRMCR_IVRM_VID_VALID: VID valid signal. 0 = Deassert valid signal. 1 = Assert valid signal. Upon rising edge of this signal, the iVRM circuit samples the VID and PFET_STRENGTH values provided by the IVRMDVR. QUAD PPM usage: These bits are always sent to the cache iVRM and all core PPMs, where it is forwarded to each core chiplet iVRM unless it is locally overridden in its core PPM. Core PPM usage: If CIVRMLCR[IVRM_LOCAL_CONTROL] = 1, these values are driven to the Core iVRM. Otherwise, the value driven comes from input pins from the QUAD PPM IVRMDVR.
1	RW	WO_CLEAR	WO_OR	PPM_IVRMCR_IVRM_BYPASS_B: Internal VRM V_{DD} bypass (negative active). QUAD PPM usage: These bits are always sent to the cache iVRM and all core PPMs, where it is forwarded to each core chiplet iVRM unless it is locally overridden in its core PPM. Core PPM usage: If CIVRMLCR[IVRM_LOCAL_CONTROL] = 1, these values are driven to the core iVRM. Otherwise, the value driven comes from input pins from the QUAD PPM IVRMDVR.
2	RW	WO_CLEAR	WO_OR	PPM_IVRMCR_IVRM_POWERON: Internal VRM V_{DD} power on. QUAD PPM usage: These bits are always sent to the cache iVRM and all core PPMs, where it is forwarded to each core chiplet iVRM unless it is locally overridden in its core PPM. Core PPM usage: If CIVRMLCR[IVRM_LOCAL_CONTROL] = 1, these values are driven to the core iVRM. Otherwise, the value driven comes from input pins from the QUAD PPM IVRMDVR.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
3	RW	WO_CLEAR	WO_OR	PPM_IVRMCR_IVRM_VREG_SLOW_DC: Must be set before doing rapid changes (for example, dropping to V_{min}), even after turning off clocks. This is needed to avoid trying to get there too fast and losing stability of the internal iVRM VID movement loop. QUAD PPM usage: These bits are always sent to the cache iVRM and all core PPMs, where it is forwarded to each core chiplet iVRM unless it is locally overridden in its core PPM. Core PPM usage: If CIVRMLCR[IVRM_LOCAL_CONTROL] = 1, these values are driven to the core iVRM. Otherwise, the value driven comes input pins from the QUAD PPM IVRMDVR.
4:7	RW	WO_CLEAR	WO_OR	PPM_IVRMCR_RESERVED_4_7: Implemented but unused.
8:63	RO	RO	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	**PPM iVRM Status Register**
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_IVRMST
Address	00000000130F01B3 (SCOM)
Description	PPM iVRM status register

Bits	SCOM	Field Mnemonic: Description
0	ROX	PPM_IVRMST_IVRM_VID_DONE: V_{DD} iVRM done indicator. Raises when the iVRM circuits are done processing a change request, triggered by a rising edge of IVRMCR[IVRM_VID_VALID] and stays set until the VALID is cleared.
1:63	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000000

Register Name	**PPM iVRM Data Value Register**
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_IVRMDVR
Address	00000000130F01B4 (SCOM)
Description	PPM iVRM data value register

Bits	SCOM	Field Mnemonic: Description
0:7	RW	PPM_IVRMDVR_IVRM_IVID: Writes to this field will drive the VID value representing the requested voltage to the QUAD iVRMs (4 Core V_{DD} and Cache V_{DD}) 0:7 = ivid(0:7). Encoded based on zero origin at 512 mV with 4 mV granularity. 0x00 = 512 mV. 0x01 = 516 mV. 0x7F = 1.532 mV. QUAD PPM usage: These bits are always sent to the cache iVRM and all core PPMs, where it is forwarded to each core chiplet iVRM unless it is locally overridden in its core PPM. Core PPM usage: If CIVRMLCR[IVRM_LOCAL_CONTROL] = 1, these values are driven to the core iVRM. Otherwise, the value driven comes from input pins from the QUAD PPM IVRMDVR.
8:10	RW	PPM_IVRMDVR_RESERVED_8_10: Implemented but not used.
11:15	RW	PPM_IVRMDVR_IVRM_PFET_STRENGTH_CORE: PFET strength value driven to this chiplet's iVRMs. This value written is dependent on the current input voltage, the requested output voltage (IVRM_IVID), and the ratio of the power needed at the requested voltage to the maximum power. QUAD PPM usage: This value is sent to all core PPMs, where it is forwarded to each core chiplet iVRM unless it is locally overridden in its core PPM. Core PPM usage: If CIVRMLCR[IVRM_LOCAL_CONTROL] = 1, these values are driven to the core iVRM. Otherwise, the value driven comes from QUAD PPM IVRMDVR.

Bits	SCOM	Field Mnemonic: Description
16:18	RW	PPM_IVRMDVR_RESERVED_16_18: Implemented but not used.
19:23	RW	PPM_IVRMDVR_IVRM_PFET_STRENGTH_CACHE: QUAD PPM usage: PFET strength value driven to the cache iVRMs. The written value is dependent on the current input voltage, the requested output voltage (IVRM_IVID), and the ratio of the power needed at the request voltage to the maximum power. Core PPM usage: This field is unused.
24:63	RO	constant = 0b0000000000000000000000000000000000000000

Register Name	PPM iVRM Actual Value Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_IVRMAVR
Address	00000000130F01B5 (SCOM)
Description	PPM iVRM actual value register

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	Reserved field.
8	ROX	Reserved field.
9:10	RO	constant = 0b00
11:15	ROX	Reserved field.
16:23	RO	constant = 0b00000000
24	ROX	Reserved field.
25	ROX	Reserved field.
26	ROX	Reserved field.
27	ROX	Reserved field.
28:63	RO	constant = 0b000000000000000000000000000000000000

Register Name	QPPM VDM Configuration Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_QUAD_REGS.QPPM_VDMCFGR
Address	00000000130F01B6 (SCOM)
Description	QPPM VDM configuration register

Bits	SCOM	Field Mnemonic: Description
0:7	RW	QPPM_VDMCFGR_VDM_VID_COMPARE: Writes to this field will drive VID value representing the requested compare voltage to the QUAD VDMs (four Core and Cache). Encoded based on zero origin at 512 mV with 4 mV granularity. 0x00 = 512 mV. 0x01 = 516 mV. 0x7F = 1.532 mV. **Note:** The actual maximum voltage supported is 0xBF (1.276 mV) and the minimum voltage is 0x10 (576 mV). Attempts to set a voltage outside of this supported range will clip at the minimum or maximum value. Also note that the iVRM clips at a lower maximum voltage value.

Bits	SCOM	Field Mnemonic: Description
8:11	RW	QPPM_VDMCFGR_VDM_OVERVOLT: Voltage droop monitor (VDM) over voltage threshold select value. 0x0 = Forces VDM output active (logic 1) 0x1 = 8 mV 0x2 = 16 mV 0x3 = 24 mV 0x4 = 32 mV 0x5 = 40 mV 0x6 = 48 mV 0x7 = 56 mV 0x8 to 0xF = 64 mV
12:15	RW	QPPM_VDMCFGR_VDM_DROOP_SMALL: Voltage droop monitor (VDM) small threshold select value. 0x0 = Forces VDM output inactive (logic 1) 0x1 = -8 mV 0x2 = -16 mV 0x3 = -24 mV 0x4 = -32 mV 0x5 = -40 mV 0x6 = -48 mV 0x7 = -56 mV 0x8 = -64 mV 0x9 = -72 mV 0xA = -80 mV 0xB = -88 mV 0xC = -92 mV 0xD = -96 mV 0xE = -96 mV 0xF = -96 mV
16:19	RW	QPPM_VDMCFGR_VDM_DROOP_LARGE: Voltage droop monitor (VDM) large threshold select value. This field uses the same encoding as the previous field.
20:23	RW	QPPM_VDMCFGR_VDM_DROOP_XTREME: Voltage droop monitor (VDM) extreme threshold select value. This field uses the same encoding as the QPPM_VDMCFGR_VDM_DROOP_SMALL field.
24:63	RO	constant = 0b0000000000000000000000000000000000000000

Register Name	PPM VDM Control Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_COMMON_REGS.PPM_VDMCR
Address	00000000130F01B8 (SCOM) 00000000130F01B9 (SCOM1) 00000000130F01BA (SCOM2)
Description	PPM VDM control register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_CLEAR	WO_OR	PPM_VDMCR_VDM_POWERON: Enables analog circuits in the VDM for this chiplet to burn power (0.6 mW). Once this bit is set, it takes 10 µs for VDM output indicators to be valid.
1	RW	WO_CLEAR	WO_OR	PPM_VDMCR_VDM_DISABLE: VDM disable for this chiplet. Like a logical fence, setting this bit forces VDM droop indication outputs to all 1.
2:63	RO	RO	RO	constant = 0b000000000000000000000000000000000000000000000000000000000 00000

Register Name	QPPM QUAD Voltage Characterization Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_QUAD_REGS.QPPM_VOLT_CHAR
Address	00000000130F01BB (SCOM)
Description	QPPM QUAD voltage characterization register

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	QPPM_VOLT_CHAR_VID_COMPARE_MAX: Maximum value of the QUAD voltage compare value since the last read. Resets to VDMCFGR[VDM_VID_COMPARE] on read.
8:15	ROX	QPPM_VOLT_CHAR_VID_COMPARE_MIN: Minimum value of the QUAD voltage compare value since the last read. Resets to VDMCFGR[VDM_VID_COMPARE] on read.
16	ROX	QPPM_VOLT_CHAR_IVRM_ENABLED_HISTORY: Sticky latch that indicates if IVRM_VID_VALID has been set to the QUAD chiplet since this register was last read. On read, resets to the value of IVRMAVR[IVRM_VID_VALID].
17:63	RO	constant = 0b00000000000000000000000000000000000000000000000

Register Name	QPPM QUAD Control Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMQ.PPM_QUAD_REGS.QPPM_QCCR
Address	00000000130F01BD (SCOM) 00000000130F01BE (SCOM1) 00000000130F01BF (SCOM2)
Description	QPPM QUAD control register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:3	RW	WO_CLEAR	WO_OR	QPPM_QCCR_L3_EX0_EDRAM_ENABLE_ENCODE: Enables the eDRAM charge pumps in L3 EX0. On power-on, the bits must be asserted in order from 0 -> 3 (0x0, 8, C, E, F), and on power down they must be de-asserted in the opposite order from 3 -> 0 (0xF, E, C, 8, 0); this means that a thermometer encode is required in sequencing these bits. Any attempt to sequence them in a different order will update this field, but will not change the *actual* value being driven to the L3 and will set a bit in the Error Register. These bits (0:3) correspond to EDRAM_ENABLE_DC, EDRAM_VWL_ENABLE_DC, L3_EX0_EDRAM_VROW_VBLH_ENABLE_DC, and EDRAM_VPP_ENABLE_DC outputs.
4:7	RW	WO_CLEAR	WO_OR	QPPM_QCCR_L3_EX1_EDRAM_ENABLE_ENCODE: Enables the eDRAM charge pumps in L3 EX1. See the previous field for details.
8:11	RW	WO_CLEAR	WO_OR	QPPM_QCCR_SPARE_8_11: Implemented but not used (spare).
12:15	RW	WO_CLEAR	WO_OR	QPPM_QCCR_DROOP_PROTECT_DATA: These bits are ANDed with FORCE_DROOP_DATA in response to the setting of ERR_REG [OCC_HEARTBEAT_LOSS] when QPMMR[ENABLE_DROOP_PROTECT_UPON_HEARTBEAT_LOSS] is set.
16:19	RW	WO_CLEAR	WO_OR	QPPM_QCCR_FORCE_DROOP_DATA: These bits are used to drive the steady state value of the vdm_droop_inject, unless overridden by PULSE_DROOP_ENABLE or by DROOP_PROTECT_DATA if enabled in response to heartbeat loss. **Note:** For this data, a zero indicates a droop occurred, in thermometer code format.
20:23	WO_4P	NC	WO_4P	QPPM_QCCR_PULSE_DROOP_DATA: These bits can be used to pulse the vdm_droop_inject, based on PULSE_DROOP_ENABLE.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
24	WO_4P	NC	WO_4P	QPPM_QCCR_PULSE_DROOP_ENABLE: This field (intended to be set with the WO_OR address) chooses what value drives the vdm_droop_inject output to the QUAD. Based on this value: 0 = vdm_droop_inject is driven only with FORCE_DROOP_DATA. 1 = Causes the PULSE_DROOP_DATA to be ANDed with the FORCE_DROOP_DATA before driving vdm_droop_inject.
25:29	RO	RO	RO	constant = 0b00000
30	RW	WO_CLEAR	WO_OR	QPPM_QCCR_PB_PURGE_REQ: Pulse to the power bus logic in the cache clock domain to request them to purge their asynchronous buffers in preparation to power off the QUAD. Stop Hcode must wait for PB_PURGE_DONE_LVL before continuing. **Note:** This is a pulse and therefore does not use a CCFG latch.
31	ROX	NCX	NCX	QPPM_QCCR_PB_PURGE_DONE_LVL: Acknowledgment from power bus that the buffers are empty and can safely be fenced and clocked off. Note: This signal is from the cache clock domain and must be latched with metastability hardened latches before feeding this SCOM bit (not latched into the CCFG ring).
32:35	ROX	NCX	NCX	QPPM_QCCR_L3_EX0_EDRAM_ENABLE_ACTUAL: Actual decoded values being driven to EX0 on the EDRAM_ENABLE_DC, EDRAM_VWL_ENABLE_DC, EDRAM_VROW_VBLH_ENABLE_DC, and EDRAM_VPP_ENABLE_DC outputs. **Note:** Captured by a scannable latch placed on the CCFG ring.
36:39	ROX	NCX	NCX	QPPM_QCCR_L3_EX1_EDRAM_ENABLE_ACTUAL: Actual decoded values being driven to EX1 on the EDRAM_ENABLE_DC, EDRAM_VWL_ENABLE_DC, EDRAM_VROW_VBLH_ENABLE_DC, and EDRAM_VPP_ENABLE_DC outputs. **Note:** Captured by a scannable latch placed on the CCFG ring.
40	ROX	NCX	NCX	QPPM_QCCR_L3_EDRAM_SEQ_ERR: Value of ERR_REG[EDRAM_SEQ_ERR] for convenience. **Note:** Captured by a scannable latch placed on the CCFG ring.
41	ROX	NCX	NCX	QPPM_QCCR_L3_EDRAM_PGATE_ERR: Value of ERR_REG[EDRAM_PGATE_ERR] for convenience. **Note:** Captured by a scannable latch placed on the CCFG ring.
42	ROX	NCX	NCX	QPPM_QCCR_L3_EX0_EDRAM_UNLOCKED: Value of the input from EX0 L3 that is used to suppress eDRAM enable changes until a scan flush has occurred. **Note:** Captured by a scannable latch placed on the CCFG ring.
43	ROX	NCX	NCX	QPPM_QCCR_L3_EX1_EDRAM_UNLOCKED: Value of the input from EX1 L3 that is used to suppress eDRAM enable changes until a scan flush has occurred. **Note:** Captured by a scannable latch placed on the CCFG ring.
44:63	RO	RO	RO	constant = 0b00000000000000000000

Register Name	Protect Mode Register
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.PROTECT_MODE_REG
Address	00000000130F03FE (SCOM)
Description	Enables read and write protection.

Bits	SCOM	Field Mnemonic: Description
0	RW	READ_PROTECT_ENABLE: Enable read protection.

Bits	SCOM	Field Mnemonic: Description
1	RW	WRITE_PROTECT_ENABLE: Enable write protection.

Register Name	**Atomic Lock Register**
Mnemonic	TP.TPCHIP.NET.PCBSLEP03.PPMPCBSLV.ATOMIC_LOCK_REG
Address	00000000130F03FF (SCOM)
Description	A bit mask for atomic locking on a ring-by-ring basis.

Bits	SCOM	Field Mnemonic: Description
0	RW	ATOMIC_LOCK_ENABLE: Enable atomic lock.
1:4	ROX	ATOMIC_ID: Atomic ID.
5:7	RO	constant = 0b000
8:15	ROX	ATOMIC_ACTIVITY: Atomic lock counter.

13. CACHE Core Chiplet

The POWER9 processor registers are listed alphabetically by mnemonic in the following address table.

Mnemonic	Address	Page
EX07.L2.L2MISC.L2CERRS.ERR_RPT0	0x0000000013010C12	2111
EX07.L2.L2MISC.L2CERRS.ERR_RPT1	0x0000000013010C13	2112
EX07.L2.L2MISC.L2CERRS.FIR_ACTION0_REG	0x0000000013010C06	2106
EX07.L2.L2MISC.L2CERRS.FIR_ACTION1_REG	0x0000000013010C07	2106
EX07.L2.L2MISC.L2CERRS.FIR_MASK_REG	0x0000000013010C03	2105
EX07.L2.L2MISC.L2CERRS.FIR_REG	0x0000000013010C00	2104
EX07.L2.L2MISC.L2CERRS.LINEDEL_TRIG_REG	0x0000000013010C0D	2108
EX07.L2.L2MISC.L2CERRS.MODE_REG0	0x0000000013010C0A	2106
EX07.L2.L2MISC.L2CERRS.MODE_REG1	0x0000000013010C0B	2107
EX07.L2.L2MISC.L2CERRS.PHYP_PURGE_CMD_REG	0x0000000013010C0F	2110
EX07.L2.L2MISC.L2CERRS.PRD_PURGE_CMD_REG	0x0000000013010C0E	2109
EX07.L2.L2MISC.L2CERRS.RD_EPS_REG	0x0000000013010C10	2110
EX07.L2.L2MISC.L2CERRS.WR_EPS_REG	0x0000000013010C11	2111
EX07.L3.L3_CARB.L3CACTL.DRAM_REF_REG	0x0000000013011C0F	2125
EX07.L3.L3_MISC.L3CERRS.EDRAM_BANK_FAIL_SCOM_RD	0x0000000013011C1B	2131
EX07.L3.L3_MISC.L3CERRS.EDRAM_BANK_SOFT_DIS	0x0000000013011C0B	2123
EX07.L3.L3_MISC.L3CERRS.EDRAM_REG	0x0000000013011C0C	2124
EX07.L3.L3_MISC.L3CERRS.ED_RD_ERR_STAT_REG0	0x0000000013011C19	2130
EX07.L3.L3_MISC.L3CERRS.ED_RD_ERR_STAT_REG1	0x0000000013011C1A	2131
EX07.L3.L3_MISC.L3CERRS.ERR_INJ_REG	0x0000000013011C0D	2124
EX07.L3.L3_MISC.L3CERRS.FIR_ACTION0_REG	0x0000000013011C06	2122
EX07.L3.L3_MISC.L3CERRS.FIR_ACTION1_REG	0x0000000013011C07	2122
EX07.L3.L3_MISC.L3CERRS.FIR_MASK_REG	0x0000000013011C03	2121
EX07.L3.L3_MISC.L3CERRS.FIR_REG	0x0000000013011C00	2119
EX07.L3.L3_MISC.L3CERRS.L3_ERR_RPT0_REG	0x0000000013011C10	2126
EX07.L3.L3_MISC.L3CERRS.L3_ERR_RPT1_REG	0x0000000013011C17	2129
EX07.L3.L3_MISC.L3CERRS.L3_RD_EPSILON_CFG_REG	0x0000000013011C29	2131
EX07.L3.L3_MISC.L3CERRS.L3_RTIM_PERIOD_MONITOR	0x0000000013011C12	2127
EX07.L3.L3_MISC.L3CERRS.L3_WR_EPSILON_CFG_REG	0x0000000013011C2A	2132
EX07.L3.L3_MISC.L3CERRS.LINE_DELETED_MEMBERS_REG	0x0000000013011C15	2128
EX07.L3.L3_MISC.L3CERRS.LRU_VIC_ALLOC_REG	0x0000000013011C11	2127
EX07.L3.L3_MISC.L3CERRS.MODE_REG0	0x0000000013011C2B	2132
EX07.L3.L3_MISC.L3CERRS.MODE_REG1	0x0000000013011C0A	2123
EX07.L3.L3_MISC.L3CERRS.PHYP_PURGE_REG	0x0000000013011C14	2128
EX07.L3.L3_MISC.L3CERRS.PM_L2_RCMD_DIS_REG	0x0000000013011C18	2130
EX07.L3.L3_MISC.L3CERRS.PM_LCO_DIS_REG	0x0000000013011C16	2129
EX07.L3.L3_MISC.L3CERRS.PM_PURGE_REG	0x0000000013011C13	2127
EX07.L3.L3_MISC.L3CERRS.PRD_PURGE_REG	0x0000000013011C0E	2124
EX07.NC.NCMISC.NCSCOMS.ERR_RPT_REG	0x000000001301140E	2117
EX07.NC.NCMISC.NCSCOMS.FIR_ACTION0_REG	0x0000000013011406	2114
EX07.NC.NCMISC.NCSCOMS.FIR_ACTION1_REG	0x0000000013011407	2115
EX07.NC.NCMISC.NCSCOMS.FIR_MASK_REG	0x0000000013011403	2114

Mnemonic	Address	Page
EX07.NC.NCMISC.NCSCOMS.FIR_REG	0x0000000013011400	2113
EX07.NC.NCMISC.NCSCOMS.INJ_REG	0x000000001301140D	2116
EX07.NC.NCMISC.NCSCOMS.NCU_DARN_BAR_REG	0x0000000013011411	2118
EX07.NC.NCMISC.NCSCOMS.NCU_MODE_REG	0x000000001301140A	2115
EX07.NC.NCMISC.NCSCOMS.NCU_MODE_REG2	0x000000001301140B	2116
EX07.NC.NCMISC.NCSCOMS.NCU_MODE_REG3	0x000000001301140C	2116
EX07.NC.NCMISC.NCSCOMS.NCU_SLOW_LPAR_REG0	0x0000000013011412	2118
EX07.NC.NCMISC.NCSCOMS.NCU_SLOW_LPAR_REG1	0x0000000013011413	2119
EX07.NC.NCMISC.NCSCOMS.NCU_SPEC_BAR_REG	0x0000000013011410	2118
EX07.NC.NCMISC.NCSCOMS.NCU_STATUS_REG	0x000000001301140F	2118
TP.TCEP03.TPCL3.EPS.DBG.DBG_INST1_COND_REG_1	0x00000000130107C1	2091
TP.TCEP03.TPCL3.EPS.DBG.DBG_INST1_COND_REG_2	0x00000000130107C2	2094
TP.TCEP03.TPCL3.EPS.DBG.DBG_INST1_COND_REG_3	0x00000000130107C3	2095
TP.TCEP03.TPCL3.EPS.DBG.DBG_INST2_COND_REG_1	0x00000000130107C4	2096
TP.TCEP03.TPCL3.EPS.DBG.DBG_INST2_COND_REG_2	0x00000000130107C5	2098
TP.TCEP03.TPCL3.EPS.DBG.DBG_INST2_COND_REG_3	0x00000000130107C6	2099
TP.TCEP03.TPCL3.EPS.DBG.DBG_MODE_REG	0x00000000130107C0	2091
TP.TCEP03.TPCL3.EPS.DBG.DBG_TRACE_MODE_REG_2	0x00000000130107CF	2103
TP.TCEP03.TPCL3.EPS.DBG.DBG_TRACE_REG_0	0x00000000130107CD	2100
TP.TCEP03.TPCL3.EPS.DBG.DBG_TRACE_REG_1	0x00000000130107CE	2101
TP.TCEP03.TPCL3.EPS.DBG.DEBUG_TRACE_CONTROL	0x00000000130107D0	2103
TP.TCEP03.TPCL3.EPS.DBG.XTRA_TRACE_MODE	0x00000000130107D1	2104
TP.TCEP03.TPCL3.L3TRA0.TR0.TRACE_HI_DATA_REG	0x0000000013010400	2076
TP.TCEP03.TPCL3.L3TRA0.TR0.TRACE_LO_DATA_REG	0x0000000013010401	2076
TP.TCEP03.TPCL3.L3TRA0.TR0.TRACE_TRCTRL_CONFIG	0x0000000013010402	2077
TP.TCEP03.TPCL3.L3TRA0.TR0.TRACE_TRDATA_CONFIG_0	0x0000000013010403	2077
TP.TCEP03.TPCL3.L3TRA0.TR0.TRACE_TRDATA_CONFIG_1	0x0000000013010404	2077
TP.TCEP03.TPCL3.L3TRA0.TR0.TRACE_TRDATA_CONFIG_2	0x0000000013010405	2078
TP.TCEP03.TPCL3.L3TRA0.TR0.TRACE_TRDATA_CONFIG_3	0x0000000013010406	2078
TP.TCEP03.TPCL3.L3TRA0.TR0.TRACE_TRDATA_CONFIG_4	0x0000000013010407	2078
TP.TCEP03.TPCL3.L3TRA0.TR0.TRACE_TRDATA_CONFIG_5	0x0000000013010408	2078
TP.TCEP03.TPCL3.L3TRA0.TR0.TRACE_TRDATA_CONFIG_9	0x0000000013010409	2078
TP.TCEP03.TPCL3.L3TRA0.TR1.TRACE_HI_DATA_REG	0x0000000013010440	2080
TP.TCEP03.TPCL3.L3TRA0.TR1.TRACE_LO_DATA_REG	0x0000000013010441	2080
TP.TCEP03.TPCL3.L3TRA0.TR1.TRACE_TRCTRL_CONFIG	0x0000000013010442	2080
TP.TCEP03.TPCL3.L3TRA0.TR1.TRACE_TRDATA_CONFIG_0	0x0000000013010443	2081
TP.TCEP03.TPCL3.L3TRA0.TR1.TRACE_TRDATA_CONFIG_1	0x0000000013010444	2081
TP.TCEP03.TPCL3.L3TRA0.TR1.TRACE_TRDATA_CONFIG_2	0x0000000013010445	2081
TP.TCEP03.TPCL3.L3TRA0.TR1.TRACE_TRDATA_CONFIG_3	0x0000000013010446	2081
TP.TCEP03.TPCL3.L3TRA0.TR1.TRACE_TRDATA_CONFIG_4	0x0000000013010447	2082
TP.TCEP03.TPCL3.L3TRA0.TR1.TRACE_TRDATA_CONFIG_5	0x0000000013010448	2082
TP.TCEP03.TPCL3.L3TRA0.TR1.TRACE_TRDATA_CONFIG_9	0x0000000013010449	2082
TP.TCEP03.TPCL3.L3TRA1.TR0.TRACE_HI_DATA_REG	0x0000000013010480	2083
TP.TCEP03.TPCL3.L3TRA1.TR0.TRACE_LO_DATA_REG	0x0000000013010481	2084
TP.TCEP03.TPCL3.L3TRA1.TR0.TRACE_TRCTRL_CONFIG	0x0000000013010482	2084
TP.TCEP03.TPCL3.L3TRA1.TR0.TRACE_TRDATA_CONFIG_0	0x0000000013010483	2084
TP.TCEP03.TPCL3.L3TRA1.TR0.TRACE_TRDATA_CONFIG_1	0x0000000013010484	2085
TP.TCEP03.TPCL3.L3TRA1.TR0.TRACE_TRDATA_CONFIG_2	0x0000000013010485	2085

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TP.TCEP03.TPCL3.L3TRA1.TR0.TRACE_TRDATA_CONFIG_3	0x0000000013010486	2085
TP.TCEP03.TPCL3.L3TRA1.TR0.TRACE_TRDATA_CONFIG_4	0x0000000013010487	2085
TP.TCEP03.TPCL3.L3TRA1.TR0.TRACE_TRDATA_CONFIG_5	0x0000000013010488	2085
TP.TCEP03.TPCL3.L3TRA1.TR0.TRACE_TRDATA_CONFIG_9	0x0000000013010489	2086
TP.TCEP03.TPCL3.L3TRA1.TR1.TRACE_HI_DATA_REG	0x00000000130104C0	2087
TP.TCEP03.TPCL3.L3TRA1.TR1.TRACE_LO_DATA_REG	0x00000000130104C1	2087
TP.TCEP03.TPCL3.L3TRA1.TR1.TRACE_TRCTRL_CONFIG	0x00000000130104C2	2088
TP.TCEP03.TPCL3.L3TRA1.TR1.TRACE_TRDATA_CONFIG_0	0x00000000130104C3	2088
TP.TCEP03.TPCL3.L3TRA1.TR1.TRACE_TRDATA_CONFIG_1	0x00000000130104C4	2088
TP.TCEP03.TPCL3.L3TRA1.TR1.TRACE_TRDATA_CONFIG_2	0x00000000130104C5	2088
TP.TCEP03.TPCL3.L3TRA1.TR1.TRACE_TRDATA_CONFIG_3	0x00000000130104C6	2089
TP.TCEP03.TPCL3.L3TRA1.TR1.TRACE_TRDATA_CONFIG_4	0x00000000130104C7	2089
TP.TCEP03.TPCL3.L3TRA1.TR1.TRACE_TRDATA_CONFIG_5	0x00000000130104C8	2089
TP.TCEP03.TPCL3.L3TRA1.TR1.TRACE_TRDATA_CONFIG_9	0x00000000130104C9	2089
TP.TCEP03.TPCL3.PPE.CME0.CHTMLBS0.CHTM.SC.HTM_CTRL	0x0000000013012205	2178
TP.TCEP03.TPCL3.PPE.CME0.CHTMLBS0.CHTM.SC.HTM_IMA_PDBAR	0x000000001301220B	2180
TP.TCEP03.TPCL3.PPE.CME0.CHTMLBS0.CHTM.SC.HTM_IMA_STATUS	0x000000001301220A	2179
TP.TCEP03.TPCL3.PPE.CME0.CHTMLBS0.CHTM.SC.HTM_LAST	0x0000000013012203	2178
TP.TCEP03.TPCL3.PPE.CME0.CHTMLBS0.CHTM.SC.HTM_MEM	0x0000000013012201	2175
TP.TCEP03.TPCL3.PPE.CME0.CHTMLBS0.CHTM.SC.HTM_MODE	0x0000000013012200	2174
TP.TCEP03.TPCL3.PPE.CME0.CHTMLBS0.CHTM.SC.HTM_STAT	0x0000000013012202	2177
TP.TCEP03.TPCL3.PPE.CME0.CHTMLBS0.CHTM.SC.HTM_TRIG	0x0000000013012204	2178
TP.TCEP03.TPCL3.PPE.CME0.CME.CMEARB.CSAR	0x000000001301200D	2137
TP.TCEP03.TPCL3.PPE.CME0.CME.CMEARB.CSCR	0x000000001301200A	2136
TP.TCEP03.TPCL3.PPE.CME0.CME.CMEARB.CSDR	0x000000001301200E	2137
TP.TCEP03.TPCL3.PPE.CME0.CME.CMEPPE.MIB.MIB_XIICAC	0x0000000013012019	2142
TP.TCEP03.TPCL3.PPE.CME0.CME.CMEPPE.MIB.MIB_XIMEM	0x0000000013012017	2141
TP.TCEP03.TPCL3.PPE.CME0.CME.CMEPPE.MIB.MIB_XISGB	0x0000000013012018	2142
TP.TCEP03.TPCL3.PPE.CME0.CME.CMEPPE.PPE.PPE_XIDBGPRO	0x0000000013012015	2140
TP.TCEP03.TPCL3.PPE.CME0.CME.CMEPPE.PPE.PPE_XIRAMDBG	0x0000000013012013	2139
TP.TCEP03.TPCL3.PPE.CME0.CME.CMEPPE.PPE.PPE_XIRAMEDR	0x0000000013012014	2140
TP.TCEP03.TPCL3.PPE.CME0.CME.CMEPPE.PPE.PPE_XIRAMGA	0x0000000013012012	2139
TP.TCEP03.TPCL3.PPE.CME0.CME.CMEPPE.PPE.PPE_XIRAMRA	0x0000000013012011	2139
TP.TCEP03.TPCL3.PPE.CME0.CME.CMEPPE.PPE.PPE_XIXCR	0x0000000013012010	2138
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_LCL_EIMR	0x0000000013012026	2147
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_LCL_EINR	0x000000001301202A	2148
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_LCL_EIPR	0x0000000013012027	2147
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_LCL_EISR	0x0000000013012025	2145
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_LCL_EISTR	0x0000000013012029	2148
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_LCL_EITR	0x0000000013012028	2147
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_LCL_ICRR	0x000000001301204D	2174
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_LCL_SISR	0x000000001301204C	2172
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_AFSR	0x0000000013012033	2154
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_AFTR	0x0000000013012034	2155
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_BCEBAR0	0x0000000013012030	2153
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_BCEBAR1	0x0000000013012031	2153
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_BCECSR	0x000000001301200F	2137
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_CIDSR	0x000000001301202E	2152

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TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_EIIR	0x000000001301202B	2148
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_FLAGS	0x0000000013012020	2144
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_IDCR	0x000000001301202D	2151
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_LFIR	0x0000000013012000	2133
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_LFIRACT0	0x0000000013012006	2135
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_LFIRACT1	0x0000000013012007	2135
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_LFIRMASK	0x0000000013012003	2135
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_LMCR	0x000000001301203A	2158
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_PMCRS0	0x0000000013012042	2163
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_PMCRS1	0x0000000013012043	2163
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_PMSRS0	0x0000000013012040	2162
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_PMSRS1	0x0000000013012041	2162
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_PSCRS00	0x0000000013012044	2163
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_PSCRS01	0x0000000013012045	2164
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_PSCRS02	0x0000000013012046	2165
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_PSCRS03	0x0000000013012047	2167
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_PSCRS10	0x0000000013012048	2168
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_PSCRS11	0x0000000013012049	2169
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_PSCRS12	0x000000001301204A	2170
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_PSCRS13	0x000000001301204B	2171
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_QFMR	0x0000000013012032	2154
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_QIDSR	0x000000001301202F	2152
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_SICR	0x000000001301203D	2161
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_SRTCH0	0x0000000013012023	2144
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_SRTCH1	0x0000000013012024	2145
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_VCCR	0x000000001301202C	2150
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_VCTR	0x0000000013012039	2157
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_VDCR	0x0000000013012035	2155
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_VDSR	0x0000000013012037	2156
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_VECR	0x0000000013012038	2157
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_VNCR	0x0000000013012036	2156
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_XIPCBMD0	0x000000001301201C	2143
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_XIPCBMD1	0x000000001301201D	2143
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_XIPCBMI0	0x000000001301201E	2144
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_XIPCBMI1	0x000000001301201F	2144
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_XIPCBQ0	0x000000001301201A	2143
TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_XIPCBQ1	0x000000001301201B	2143
TP.TCEP03.TPCL3.PPE.CME1.CHTMLBS0.CHTM.SC.HTM_CTRL	0x0000000013012605	2224
TP.TCEP03.TPCL3.PPE.CME1.CHTMLBS0.CHTM.SC.HTM_IMA_PDBAR	0x000000001301260B	2225
TP.TCEP03.TPCL3.PPE.CME1.CHTMLBS0.CHTM.SC.HTM_IMA_STATUS	0x000000001301260A	2225
TP.TCEP03.TPCL3.PPE.CME1.CHTMLBS0.CHTM.SC.HTM_LAST	0x0000000013012603	2223
TP.TCEP03.TPCL3.PPE.CME1.CHTMLBS0.CHTM.SC.HTM_MEM	0x0000000013012601	2222
TP.TCEP03.TPCL3.PPE.CME1.CHTMLBS0.CHTM.SC.HTM_MODE	0x0000000013012600	2220
TP.TCEP03.TPCL3.PPE.CME1.CHTMLBS0.CHTM.SC.HTM_STAT	0x0000000013012602	2222
TP.TCEP03.TPCL3.PPE.CME1.CHTMLBS0.CHTM.SC.HTM_TRIG	0x0000000013012604	2223
TP.TCEP03.TPCL3.PPE.CME1.CHTMLBS1.CHTM.SC.HTM_CTRL	0x0000000013012705	2229
TP.TCEP03.TPCL3.PPE.CME1.CHTMLBS1.CHTM.SC.HTM_IMA_PDBAR	0x000000001301270B	2230
TP.TCEP03.TPCL3.PPE.CME1.CHTMLBS1.CHTM.SC.HTM_IMA_STATUS	0x000000001301270A	2230

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TP.TCEP03.TPCL3.PPE.CME1.CHTMLBS1.CHTM.SC.HTM_LAST	0x0000000013012703	2228
TP.TCEP03.TPCL3.PPE.CME1.CHTMLBS1.CHTM.SC.HTM_MEM	0x0000000013012701	2227
TP.TCEP03.TPCL3.PPE.CME1.CHTMLBS1.CHTM.SC.HTM_MODE	0x0000000013012700	2225
TP.TCEP03.TPCL3.PPE.CME1.CHTMLBS1.CHTM.SC.HTM_STAT	0x0000000013012702	2227
TP.TCEP03.TPCL3.PPE.CME1.CHTMLBS1.CHTM.SC.HTM_TRIG	0x0000000013012704	2228
TP.TCEP03.TPCL3.PPE.CME1.CME.CMEARB.CSAR	0x000000001301240D	2183
TP.TCEP03.TPCL3.PPE.CME1.CME.CMEARB.CSCR	0x000000001301240A	2182
TP.TCEP03.TPCL3.PPE.CME1.CME.CMEARB.CSDR	0x000000001301240E	2183
TP.TCEP03.TPCL3.PPE.CME1.CME.CMEPPE.MIB.MIB_XIICAC	0x0000000013012419	2189
TP.TCEP03.TPCL3.PPE.CME1.CME.CMEPPE.MIB.MIB_XIMEM	0x0000000013012417	2188
TP.TCEP03.TPCL3.PPE.CME1.CME.CMEPPE.MIB.MIB_XISGB	0x0000000013012418	2189
TP.TCEP03.TPCL3.PPE.CME1.CME.CMEPPE.PPE.PPE_XIDBGPRO	0x0000000013012415	2187
TP.TCEP03.TPCL3.PPE.CME1.CME.CMEPPE.PPE.PPE_XIRAMDBG	0x0000000013012413	2186
TP.TCEP03.TPCL3.PPE.CME1.CME.CMEPPE.PPE.PPE_XIRAMEDR	0x0000000013012414	2187
TP.TCEP03.TPCL3.PPE.CME1.CME.CMEPPE.PPE.PPE_XIRAMGA	0x0000000013012412	2186
TP.TCEP03.TPCL3.PPE.CME1.CME.CMEPPE.PPE.PPE_XIRAMRA	0x0000000013012411	2185
TP.TCEP03.TPCL3.PPE.CME1.CME.CMEPPE.PPE.PPE_XIXCR	0x0000000013012410	2185
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_LCL_EIMR	0x0000000013012426	2194
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_LCL_EINR	0x000000001301242A	2195
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_LCL_EIPR	0x0000000013012427	2194
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_LCL_EISR	0x0000000013012425	2192
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_LCL_EISTR	0x0000000013012429	2195
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_LCL_EITR	0x0000000013012428	2194
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_LCL_ICRR	0x000000001301244D	2220
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_LCL_SISR	0x000000001301244C	2219
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_AFSR	0x0000000013012433	2201
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_AFTR	0x0000000013012434	2201
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_BCEBAR0	0x0000000013012430	2199
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_BCEBAR1	0x0000000013012431	2200
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_BCECSR	0x000000001301240F	2184
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_CIDSR	0x000000001301242E	2198
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_EIIR	0x000000001301242B	2195
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_FLAGS	0x0000000013012420	2191
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_IDCR	0x000000001301242D	2197
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_LFIR	0x0000000013012400	2180
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_LFIRACT0	0x0000000013012406	2182
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_LFIRACT1	0x0000000013012407	2182
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_LFIRMASK	0x0000000013012403	2182
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_LMCR	0x000000001301243A	2204
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_PMCRS0	0x0000000013012442	2209
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_PMCRS1	0x0000000013012443	2209
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_PMSRS0	0x0000000013012440	2209
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_PMSRS1	0x0000000013012441	2209
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_PSCRS00	0x0000000013012444	2210
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_PSCRS01	0x0000000013012445	2211
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_PSCRS02	0x0000000013012446	2212
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_PSCRS03	0x0000000013012447	2213
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_PSCRS10	0x0000000013012448	2214

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TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_PSCRS11	0x0000000013012449	2215
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_PSCRS12	0x000000001301244A	2217
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_PSCRS13	0x000000001301244B	2218
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_QFMR	0x0000000013012432	2200
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_QIDSR	0x000000001301242F	2199
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_SICR	0x000000001301243D	2207
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_SRTCH0	0x0000000013012423	2191
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_SRTCH1	0x0000000013012424	2191
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_VCCR	0x000000001301242C	2196
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_VCTR	0x0000000013012439	2204
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_VDCR	0x0000000013012435	2202
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_VDSR	0x0000000013012437	2202
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_VECR	0x0000000013012438	2203
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_VNCR	0x0000000013012436	2202
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_XIPCBMD0	0x000000001301241C	2190
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_XIPCBMD1	0x000000001301241D	2190
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_XIPCBMI0	0x000000001301241E	2190
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_XIPCBMI1	0x000000001301241F	2191
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_XIPCBQ0	0x000000001301241A	2190
TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_XIPCBQ1	0x000000001301241B	2190

The POWER9 processor registers are listed in the following tables.

Register Name	Trace Array High Data Register
Mnemonic	TP.TCEP03.TPCL3.L3TRA0.TR0.TRACE_HI_DATA_REG
Address	0000000013010400 (SCOM)
Description	This register provides the high trace array data.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace array data 0:63.

Register Name	Trace Array Low Data Register
Mnemonic	TP.TCEP03.TPCL3.L3TRA0.TR0.TRACE_LO_DATA_REG
Address	0000000013010401 (SCOM)
Description	This register provides the low trace array data.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace array data 64:95.
32:41	ROX	TRACE_ADDRESS: Trace address.
42:50	ROX	TRACE_LAST_BANK: Trace last bank.

Bits	SCOM	Field Mnemonic: Description
51	ROX	TRACE_LAST_BANK_VALID: Trace last bank valid.
52	ROX	TRACE_WRITE_ON_RUN: Trace write-on-run indicator.
53	ROX	TRACE_RUNNING: Trace run indicator.
54:63	ROX	TRACE_HOLD_ADDRESS: Trace hold address (pointing to last entry).

Register Name	Trace Control Configuration Register
Mnemonic	TP.TCEP03.TPCL3.L3TRA0.TR0.TRACE_TRCTRL_CONFIG
Address	0000000013010402 (SCOM)
Description	This register contains trace control configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	STORE_ON_TRIG_MODE: Enable store on trigger mode.
1	RW	WRITE_ON_RUN_MODE: Enable unconditional forced write when trace_run.
2:9	RW	EXTEND_TRIG_MODE: Counter value for extended trigger mode.
10	RW	BANK_MODE: Enable bank mode.
11	RW	ENH_TRACE_MODE: Enable enhanced trace mode.
12	RW	LOCAL_CLOCK_GATE_CONTROL: When this bit is set, internal clock gating is disabled. The trace control logic and the trace data pipeline are always clocked.
13	RW	UNUSED_13B: Unused.
14:17	RW	TRACE_SELCT_CONTROL: Selector for two sets of external trace bus multiplexers. tra_mux0_sel(0:1) and tra_mux1_sel(0:1).
18:21	RW	SPARE_CONTROL: Spare control bits.

Register Name	Trace Data Configuration Register 0
Mnemonic	TP.TCEP03.TPCL3.L3TRA0.TR0.TRACE_TRDATA_CONFIG_0
Address	0000000013010403 (SCOM)
Description	This register contains a trace data compare mask for bits 0 – 63.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: Trace data compare mask for bits 0 to 63.

Register Name	Trace Data Configuration Register 1
Mnemonic	TP.TCEP03.TPCL3.L3TRA0.TR0.TRACE_TRDATA_CONFIG_1
Address	0000000013010404 (SCOM)
Description	This register contains a trace data compare mask for bits 64 – 87.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: Trace data compare mask for bits 64 to 87.

Register Name	Trace Data Configuration Register 2
Mnemonic	TP.TCEP03.TPCL3.L3TRA0.TR0.TRACE_TRDATA_CONFIG_2
Address	0000000013010405 (SCOM)
Description	This register contains patterns A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: pattern_match_pata_0_to_23.
24:47	RW	PATTERNB: pattern_match_patb_0_to_23.

Register Name	Trace Data Configuration Register 3
Mnemonic	TP.TCEP03.TPCL3.L3TRA0.TR0.TRACE_TRDATA_CONFIG_3
Address	0000000013010406 (SCOM)
Description	This register contains patterns C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNC: pattern_match_patc_0_to_23.
24:47	RW	PATTERND: pattern_match_patd_0_to_23.

Register Name	Trace Data Configuration Register 4
Mnemonic	TP.TCEP03.TPCL3.L3TRA0.TR0.TRACE_TRDATA_CONFIG_4
Address	0000000013010407 (SCOM)
Description	This register contains masks A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: mska.
24:47	RW	MASKB: mskb.

Register Name	Trace Data Configuration Register 5
Mnemonic	TP.TCEP03.TPCL3.L3TRA0.TR0.TRACE_TRDATA_CONFIG_5
Address	0000000013010408 (SCOM)
Description	This register contains masks C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: mskc.
24:47	RW	MASKD: mskd.

Register Name	Trace Data Configuration Register 9
Mnemonic	TP.TCEP03.TPCL3.L3TRA0.TR0.TRACE_TRDATA_CONFIG_9
Address	0000000013010409 (SCOM)
Description	This register contains trace data configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disable trace data compression (store data every cycle).
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Take into account changes in the error bit for trace data compression (default = 0).
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.
10:13	RW	TRIG0_OR_MASK: The OR of all selected MATCHes is ORed with result of TRIG0_AND. 0b1xxx = Select MATCHA OR. 0bx1xx = Select MATCHB OR. 0bxx1x = Select MATCHC OR. 0bxxx1 = Select MATCHD OR. 0b0000 = Select to not OR any MATCHes.
14:17	RW	TRIG0_AND_MASK: The AND of following selected MATCHes is ORed with result of TRIG0_OR. 0b1xxx = Select MATCHA AND. 0bx1xx = Select MATCHB AND. 0bxx1x = Select MATCHC AND. 0bxxx1 = Select MATCHD AND. 0b0000 = Select to not AND any MATCHes together to form TRIG0.
18:21	RW	TRIG1_OR_MASK: The OR of all selected MATCHes is ORed with result of TRIG1_AND. 0b1xxx = Select MATCHA OR. 0bx1xx = Select MATCHB OR. 0bxx1x = Select MATCHC OR. 0bxxx1 = Select MATCHD OR. 0b0000 = Select to not OR any MATCHes to form TRIG1.
22:25	RW	TRIG1_AND_MASK: The AND of following selected MATCHes is ORed with result of TRIG1_OR. 0b1xxx = Select MATCHA AND. 0bx1xx = Select MATCHB AND. 0bxx1x = Select MATCHC AND. 0bxxx1 = Select MATCHD AND. 0b0000 = Select to not AND any MATCHes together to form TRIG1.
26	RW	TRIG0_NOT_MODE: Invert TRIG0 before using it.
27	RW	TRIG1_NOT_MODE: Invert TRIG1 before using it.
28:31	RW	MATCH_NOT_MODE: Invert the match polarity before using it to form a trigger. 0b1000 inverts MATCHA. 0b0100 inverts MATCHB. 0b0010 inverts MATCHC. 0b0001 inverts MATCHD.

Bits	SCOM	Field Mnemonic: Description
32:35	RW	Reserved field.
36	RW	DD1_STRETCH_TRIGGER_PULSES: (DD1 workaround.) Stretch trigger output pulses to two clocks. Must be enabled for MCFAST and L2FAST traces.
37	RW	Reserved field.

Register Name	Trace Array High Data Register
Mnemonic	TP.TCEP03.TPCL3.L3TRA0.TR1.TRACE_HI_DATA_REG
Address	0000000013010440 (SCOM)
Description	This register provides the high trace array data.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace array data 0:63.

Register Name	Trace Array Low Data Register
Mnemonic	TP.TCEP03.TPCL3.L3TRA0.TR1.TRACE_LO_DATA_REG
Address	0000000013010441 (SCOM)
Description	This register provides the low trace array data.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace array data 64:95.
32:41	ROX	TRACE_ADDRESS: Trace address.
42:50	ROX	TRACE_LAST_BANK: Trace last bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace last bank valid.
52	ROX	TRACE_WRITE_ON_RUN: Trace write-on-run indicator.
53	ROX	TRACE_RUNNING: Trace run indicator.
54:63	ROX	TRACE_HOLD_ADDRESS: Trace hold address (pointing to last entry).

Register Name	Trace Control Configuration Register
Mnemonic	TP.TCEP03.TPCL3.L3TRA0.TR1.TRACE_TRCTRL_CONFIG
Address	0000000013010442 (SCOM)
Description	This register contains trace control configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	STORE_ON_TRIG_MODE: Enable store on trigger mode.
1	RW	WRITE_ON_RUN_MODE: Enable unconditional forced write when trace_run.
2:9	RW	EXTEND_TRIG_MODE: Counter value for extended trigger mode.
10	RW	BANK_MODE: Enable bank mode.
11	RW	ENH_TRACE_MODE: Enable enhanced trace mode.
12	RW	LOCAL_CLOCK_GATE_CONTROL: When this bit is set, internal clock gating is disabled. The trace control logic and the trace data pipeline are always clocked.

Bits	SCOM	Field Mnemonic: Description
13	RW	UNUSED_13B: Unused.
14:17	RW	TRACE_SELCT_CONTROL: Selector for two sets of external trace bus multiplexers, tra_mux0_sel(0:1) and tra_mux1_sel(0:1).
18:21	RW	SPARE_CONTROL: Spare control bits.

Register Name	Trace Data Configuration Register 0
Mnemonic	TP.TCEP03.TPCL3.L3TRA0.TR1.TRACE_TRDATA_CONFIG_0
Address	0000000013010443 (SCOM)
Description	This register contains a trace data compare mask for bits 0 – 63.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: Trace data compare mask for bits 0 to 63.

Register Name	Trace Data Configuration Register 1
Mnemonic	TP.TCEP03.TPCL3.L3TRA0.TR1.TRACE_TRDATA_CONFIG_1
Address	0000000013010444 (SCOM)
Description	This register contains a trace data compare mask for bits 64 – 87.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: Trace data compare mask for bits 64 to 87.

Register Name	Trace Data Configuration Register 2
Mnemonic	TP.TCEP03.TPCL3.L3TRA0.TR1.TRACE_TRDATA_CONFIG_2
Address	0000000013010445 (SCOM)
Description	This register contains patterns A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: pattern_match_pata_0_to_23.
24:47	RW	PATTERNB: pattern_match_patb_0_to_23.

Register Name	Trace Data Configuration Register 3
Mnemonic	TP.TCEP03.TPCL3.L3TRA0.TR1.TRACE_TRDATA_CONFIG_3
Address	0000000013010446 (SCOM)
Description	This register contains patterns C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNC: pattern_match_patc_0_to_23.
24:47	RW	PATTERND: pattern_match_patd_0_to_23.

Register Name	Trace Data Configuration Register 4
Mnemonic	TP.TCEP03.TPCL3.L3TRA0.TR1.TRACE_TRDATA_CONFIG_4
Address	0000000013010447 (SCOM)
Description	This register contains masks A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: mska.
24:47	RW	MASKB: mskb.

Register Name	Trace Data Configuration Register 5
Mnemonic	TP.TCEP03.TPCL3.L3TRA0.TR1.TRACE_TRDATA_CONFIG_5
Address	0000000013010448 (SCOM)
Description	This register contains masks C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: mskc.
24:47	RW	MASKD: mskd.

Register Name	Trace Data Configuration Register 9
Mnemonic	TP.TCEP03.TPCL3.L3TRA0.TR1.TRACE_TRDATA_CONFIG_9
Address	0000000013010449 (SCOM)
Description	This register contains trace data configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disable trace data compression (store data every cycle).
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Take into account changes in the error bit for trace data compression (default = 0).
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.

Bits	SCOM	Field Mnemonic: Description
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.
10:13	RW	TRIG0_OR_MASK: The OR of all selected MATCHes is ORed with result of TRIG0_AND. 0b1xxx = Select MATCHA OR. 0bx1xx = Select MATCHB OR. 0bxx1x = Select MATCHC OR. 0bxxx1 = Select MATCHD OR. 0b0000 = Select to not OR any MATCHes.
14:17	RW	TRIG0_AND_MASK: The AND of following selected MATCHes is ORed with result of TRIG0_OR. 0b1xxx = Select MATCHA AND. 0bx1xx = Select MATCHB AND. 0bxx1x = Select MATCHC AND. 0bxxx1 = Select MATCHD AND. 0b0000 = Select to not AND any MATCHes together to form TRIG0.
18:21	RW	TRIG1_OR_MASK: The OR of all selected MATCHes is ORed with result of TRIG1_AND. 0b1xxx = Select MATCHA OR. 0bx1xx = Select MATCHB OR. 0bxx1x = Select MATCHC OR. 0bxxx1 = Select MATCHD OR. 0b0000 = Select to not OR any MATCHes to form TRIG1.
22:25	RW	TRIG1_AND_MASK: The AND of following selected MATCHes is ORed with result of TRIG1_OR. 0b1xxx = Select MATCHA AND. 0bx1xx = Select MATCHB AND. 0bxx1x = Select MATCHC AND. 0bxxx1 = Select MATCHD AND. 0b0000 = Select to not AND any MATCHes together to form TRIG1.
26	RW	TRIG0_NOT_MODE: Invert TRIG0 before using it.
27	RW	TRIG1_NOT_MODE: Invert TRIG1 before using it.
28:31	RW	MATCH_NOT_MODE: Invert the match polarity before using it to form a trigger. 0b1000 inverts MATCHA. 0b0100 inverts MATCHB. 0b0010 inverts MATCHC. 0b0001 inverts MATCHD.
32:35	RW	Reserved field.
36	RW	DD1_STRETCH_TRIGGER_PULSES: (DD1 workaround.) Stretch trigger output pulses to two clocks. Must be enabled for MCFAST and L2FAST traces.
37	RW	Reserved field.

Register Name	**Trace Array High Data Register**
Mnemonic	TP.TCEP03.TPCL3.L3TRA1.TR0.TRACE_HI_DATA_REG
Address	0000000013010480 (SCOM)
Description	This register provides the high trace array data.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace array data 0:63.

Register Name	Trace Array Low Data Register
Mnemonic	TP.TCEP03.TPCL3.L3TRA1.TR0.TRACE_LO_DATA_REG
Address	0000000013010481 (SCOM)
Description	This register provides the low trace array data.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace array data 64:95.
32:41	ROX	TRACE_ADDRESS: Trace address.
42:50	ROX	TRACE_LAST_BANK: Trace last bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace last bank valid.
52	ROX	TRACE_WRITE_ON_RUN: Trace write-on-run indicator.
53	ROX	TRACE_RUNNING: Trace run indicator.
54:63	ROX	TRACE_HOLD_ADDRESS: Trace hold address (pointing to last entry).

Register Name	Trace Control Configuration Register
Mnemonic	TP.TCEP03.TPCL3.L3TRA1.TR0.TRACE_TRCTRL_CONFIG
Address	0000000013010482 (SCOM)
Description	This register contains trace control configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	STORE_ON_TRIG_MODE: Enable store on trigger mode.
1	RW	WRITE_ON_RUN_MODE: Enable unconditional forced write when trace_run.
2:9	RW	EXTEND_TRIG_MODE: Counter value for extended trigger mode.
10	RW	BANK_MODE: Enable bank mode.
11	RW	ENH_TRACE_MODE: Enable enhanced trace mode.
12	RW	LOCAL_CLOCK_GATE_CONTROL: When this bit is set, internal clock gating is disabled. The trace control logic and the trace data pipeline are always clocked.
13	RW	UNUSED_13B: Unused.
14:17	RW	TRACE_SELCT_CONTROL: Selector for two sets of external trace bus multiplexers, tra_mux0_sel(0:1) and tra_mux1_sel(0:1).
18:21	RW	SPARE_CONTROL: Spare control bits.

Register Name	Trace Data Configuration Register 0
Mnemonic	TP.TCEP03.TPCL3.L3TRA1.TR0.TRACE_TRDATA_CONFIG_0
Address	0000000013010483 (SCOM)
Description	This register contains a trace data compare mask for bits 0 – 63.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: Trace data compare mask for bits 0 to 63.

Register Name	Trace Data Configuration Register 1
Mnemonic	TP.TCEP03.TPCL3.L3TRA1.TR0.TRACE_TRDATA_CONFIG_1
Address	0000000013010484 (SCOM)
Description	This register contains a trace data compare mask for bits 64 – 87.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: Trace data compare mask for bits 64 to 87.

Register Name	Trace Data Configuration Register 2
Mnemonic	TP.TCEP03.TPCL3.L3TRA1.TR0.TRACE_TRDATA_CONFIG_2
Address	0000000013010485 (SCOM)
Description	This register contains patterns A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: pattern_match_pata_0_to_23.
24:47	RW	PATTERNB: pattern_match_patb_0_to_23.

Register Name	Trace Data Configuration Register 3
Mnemonic	TP.TCEP03.TPCL3.L3TRA1.TR0.TRACE_TRDATA_CONFIG_3
Address	0000000013010486 (SCOM)
Description	This register contains patterns C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNC: pattern_match_patc_0_to_23.
24:47	RW	PATTERND: pattern_match_patd_0_to_23.

Register Name	Trace Data Configuration Register 4
Mnemonic	TP.TCEP03.TPCL3.L3TRA1.TR0.TRACE_TRDATA_CONFIG_4
Address	0000000013010487 (SCOM)
Description	This register contains masks A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: mska.
24:47	RW	MASKB: mskb.

Register Name	Trace Data Configuration Register 5
Mnemonic	TP.TCEP03.TPCL3.L3TRA1.TR0.TRACE_TRDATA_CONFIG_5
Address	0000000013010488 (SCOM)
Description	This register contains masks C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: mskc.
24:47	RW	MASKD: mskd.

Register Name	Trace Data Configuration Register 9
Mnemonic	TP.TCEP03.TPCL3.L3TRA1.TR0.TRACE_TRDATA_CONFIG_9
Address	0000000013010489 (SCOM)
Description	This register contains trace data configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disable trace data compression (store data every cycle).
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Take into account changes in the error bit for trace data compression (default = 0).
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.
10:13	RW	TRIG0_OR_MASK: The OR of all selected MATCHes is ORed with result of TRIG0_AND. 0b1xxx = Select MATCHA OR. 0bx1xx = Select MATCHB OR. 0bxx1x = Select MATCHC OR. 0bxxx1 = Select MATCHD OR. 0b0000 = Select to not OR any MATCHes.
14:17	RW	TRIG0_AND_MASK: The AND of following selected MATCHes is ORed with result of TRIG0_OR. 0b1xxx = Select MATCHA AND. 0bx1xx = Select MATCHB AND. 0bxx1x = Select MATCHC AND. 0bxxx1 = Select MATCHD AND. 0b0000 = Select to not AND any MATCHes together to form TRIG0.
18:21	RW	TRIG1_OR_MASK: The OR of all selected MATCHes is ORed with result of TRIG1_AND. 0b1xxx = Select MATCHA OR. 0bx1xx = Select MATCHB OR. 0bxx1x = Select MATCHC OR. 0bxxx1 = Select MATCHD OR. 0b0000 = Select to not OR any MATCHes to form TRIG1.

Bits	SCOM	Field Mnemonic: Description
22:25	RW	TRIG1_AND_MASK: The AND of following selected MATCHes is ORed with result of TRIG1_OR. 0b1xxx = Select MATCHA AND. 0bx1xx = Select MATCHB AND. 0bxx1x = Select MATCHC AND. 0bxxx1 = Select MATCHD AND. 0b0000 = Select to not AND any MATCHes together to form TRIG1.
26	RW	TRIG0_NOT_MODE: Invert TRIG0 before using it.
27	RW	TRIG1_NOT_MODE: Invert TRIG1 before using it.
28:31	RW	MATCH_NOT_MODE: Invert the match polarity before using it to form a trigger. 0b1000 inverts MATCHA. 0b0100 inverts MATCHB. 0b0010 inverts MATCHC. 0b0001 inverts MATCHD.
32:35	RW	Reserved field.
36	RW	DD1_STRETCH_TRIGGER_PULSES: (DD1 workaround.) Stretch trigger output pulses to two clocks. Must be enabled for MCFAST and L2FAST traces.
37	RW	Reserved field.

Register Name	Trace Array High Data Register
Mnemonic	TP.TCEP03.TPCL3.L3TRA1.TR1.TRACE_HI_DATA_REG
Address	00000000130104C0 (SCOM)
Description	This register provides the high trace array data.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace array data 0:63.

Register Name	Trace Array Low Data Register
Mnemonic	TP.TCEP03.TPCL3.L3TRA1.TR1.TRACE_LO_DATA_REG
Address	00000000130104C1 (SCOM)
Description	This register provides the low trace array data.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace array data 64:95.
32:41	ROX	TRACE_ADDRESS: Trace address.
42:50	ROX	TRACE_LAST_BANK: Trace last bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace last bank valid.
52	ROX	TRACE_WRITE_ON_RUN: Trace write-on-run indicator.
53	ROX	TRACE_RUNNING: Trace run indicator.
54:63	ROX	TRACE_HOLD_ADDRESS: Trace hold address (pointing to last entry).

Register Name	Trace Control Configuration Register
Mnemonic	TP.TCEP03.TPCL3.L3TRA1.TR1.TRACE_TRCTRL_CONFIG
Address	00000000130104C2 (SCOM)
Description	This register contains trace control configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	STORE_ON_TRIG_MODE: Enable store on trigger mode.
1	RW	WRITE_ON_RUN_MODE: Enable unconditional forced write when trace_run.
2:9	RW	EXTEND_TRIG_MODE: Counter value for extended trigger mode.
10	RW	BANK_MODE: Enable bank mode.
11	RW	ENH_TRACE_MODE: Enable enhanced trace mode.
12	RW	LOCAL_CLOCK_GATE_CONTROL: When this bit is set, internal clock gating is disabled. The trace control logic and the trace data pipeline are always clocked.
13	RW	UNUSED_13B: Unused.
14:17	RW	TRACE_SELCT_CONTROL: Selector for two sets of external trace bus multiplexers, tra_mux0_sel(0:1) and tra_mux1_sel(0:1).
18:21	RW	SPARE_CONTROL: Spare control bits.

Register Name	Trace Data Configuration Register 0
Mnemonic	TP.TCEP03.TPCL3.L3TRA1.TR1.TRACE_TRDATA_CONFIG_0
Address	00000000130104C3 (SCOM)
Description	This register contains a trace data compare mask for bits 0 – 63.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: Trace data compare mask for bits 0 to 63.

Register Name	Trace Data Configuration Register 1
Mnemonic	TP.TCEP03.TPCL3.L3TRA1.TR1.TRACE_TRDATA_CONFIG_1
Address	00000000130104C4 (SCOM)
Description	This register contains a trace data compare mask for bits 64 – 87.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: Trace data compare mask for bits 64 to 87.

Register Name	Trace Data Configuration Register 2
Mnemonic	TP.TCEP03.TPCL3.L3TRA1.TR1.TRACE_TRDATA_CONFIG_2
Address	00000000130104C5 (SCOM)
Description	This register contains patterns A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: pattern_match_pata_0_to_23.

Bits	SCOM	Field Mnemonic: Description
24:47	RW	PATTERNB: pattern_match_patb_0_to_23.

Register Name	Trace Data Configuration Register 3
Mnemonic	TP.TCEP03.TPCL3.L3TRA1.TR1.TRACE_TRDATA_CONFIG_3
Address	00000000130104C6 (SCOM)
Description	This register contains patterns C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNC: pattern_match_patc_0_to_23.
24:47	RW	PATTERND: pattern_match_patd_0_to_23.

Register Name	Trace Data Configuration Register 4
Mnemonic	TP.TCEP03.TPCL3.L3TRA1.TR1.TRACE_TRDATA_CONFIG_4
Address	00000000130104C7 (SCOM)
Description	This register contains masks A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: mska.
24:47	RW	MASKB: mskb.

Register Name	Trace Data Configuration Register 5
Mnemonic	TP.TCEP03.TPCL3.L3TRA1.TR1.TRACE_TRDATA_CONFIG_5
Address	00000000130104C8 (SCOM)
Description	This register contains masks C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: mskc.
24:47	RW	MASKD: mskd.

Register Name	Trace Data Configuration Register 9
Mnemonic	TP.TCEP03.TPCL3.L3TRA1.TR1.TRACE_TRDATA_CONFIG_9
Address	00000000130104C9 (SCOM)
Description	This register contains trace data configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disable trace data compression (store data every cycle).
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Take into account changes in the error bit for trace data compression (default = 0).

Bits	SCOM	Field Mnemonic: Description
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.
10:13	RW	TRIG0_OR_MASK: The OR of all selected MATCHes is ORed with result of TRIG0_AND. 0b1xxx = Select MATCHA OR. 0bx1xx = Select MATCHB OR. 0bxx1x = Select MATCHC OR. 0bxxx1 = Select MATCHD OR. 0b0000 = Select to not OR any MATCHes.
14:17	RW	TRIG0_AND_MASK: The AND of following selected MATCHes is ORed with result of TRIG0_OR. 0b1xxx = Select MATCHA AND. 0bx1xx = Select MATCHB AND. 0bxx1x = Select MATCHC AND. 0bxxx1 = Select MATCHD AND. 0b0000 = Select to not AND any MATCHes together to form TRIG0.
18:21	RW	TRIG1_OR_MASK: NOTE: the OR of all selected MATCHes is ORed with result of TRIG1_AND. 0b1xxx = Select MATCHA OR 0bx1xx = Select MATCHB OR 0bxx1x = Select MATCHC OR 0bxxx1 = Select MATCHD OR 0b0000 = Select to not OR any MATCHes to form TRIG1.
22:25	RW	TRIG1_AND_MASK: The AND of following selected MATCHes is ORed with result of TRIG1_OR. 0b1xxx = Select MATCHA AND. 0bx1xx = Select MATCHB AND. 0bxx1x = Select MATCHC AND. 0bxxx1 = Select MATCHD AND. 0b0000 = Select to not AND any MATCHes together to form TRIG1.
26	RW	TRIG0_NOT_MODE: Invert TRIG0 before using it.
27	RW	TRIG1_NOT_MODE: Invert TRIG1 before using it.
28:31	RW	MATCH_NOT_MODE: Invert the match polarity before using it to form a trigger. 0b1000 inverts MATCHA. 0b0100 inverts MATCHB. 0b0010 inverts MATCHC. 0b0001 inverts MATCHD.
32:35	RW	Reserved field.
36	RW	DD1_STRETCH_TRIGGER_PULSES: (DD1 workaround.) Stretch trigger output pulses to two clocks. Must be enabled for MCFAST and L2FAST traces.

Bits	SCOM	Field Mnemonic: Description
37	RW	Reserved field.

Register Name	Debug Mode Register
Mnemonic	TP.TCEP03.TPCL3.EPS.DBG.DBG_MODE_REG
Address	00000000130107C0 (SCOM)
Description	This is debug macro configuration register 0 for the configuration component.

Bits	SCOM	Field Mnemonic: Description
0:2	RW	GLB_BRCST_MODE: global_broadcast_mode (0 to 2): 100 = dbg_trace_run and dbg_trace_freeze. 101 = pc_tcdbg_trace_run_fncd and dbg_trace_freeze. 110 = dbg_triggers_out(0 to 1). 111 = pc_tcdbg_triggers(0 to 1) (from core).
3:5	RW	TRACE_SEL_MODE: Select source for trace_run and bank. 001 = Core trace run and bank. 010 = TP broadcast run and 0. 011 = tc_dbg_inter_brcst latched. 100 = tc_dbg_dbg_sync_brcst_rcv. else = dbg_trace_run and dbg_trace_bank.
6:7	RW	TRIG_SEL_MODE: Select source for tcdbg_trigger(0). 10 = Global broadcast. 11 = pc_tcdbg_trigger (from core). else = dbg_triggers_out(0:1).
8	RW	STOP_ON_XSTOP_SELECTION: Enable trace stop on checkstop.
9	RW	STOP_ON_RECOV_ERR_SELECTION: Enable trace stop on recoverable error.
10	RW	STOP_ON_SPATTN_SELECTION: Enable trace stop on special attention.
11	RW	FREEZE_SEL_MODE: Select freeze source: 0 = Local debug freeze. 1 = Via broadcast: tp_tcdbg_glb_brcst(1).
12:13	RW	SYNC_BRCST_MODE: Originally used for synchronous broadcast mode; currently unused because it is obsolete. See trace_sel_mode.
14	RO	constant = 0b0
15	RO	constant = 0b0
16:31	ROX	dbg_status.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	Debug Instance 1 Condition 1 Register
Mnemonic	TP.TCEP03.TPCL3.EPS.DBG.DBG_INST1_COND_REG_1
Address	00000000130107C1 (SCOM)
Description	This is debug macro configuration register 1 for front-end component 1.

Bits	SCOM	Field Mnemonic: Description
0:7	RW	INST1_COND1_SEL_A: Multiplexer for cond1_trig_in(0). 000 = Select constant 0 001 = Select constant 1 -- CONDITION FEEDBACK --

Bits	SCOM	Field Mnemonic: Description
		002 = Select inst1_dbg_cond1. 003 = Select inst1_dbg_cond2. 004 = Select inst1_dbg_cond3. 005 = Select inst1_dbg_cond2timeout. 006 = Select inst2_dbg_cond1. 007 = Select inst2_dbg_cond2. 008 = Select inst2_dbg_cond3. 009 = Select inst2_dbg_cond2timeout. 010 = Select inst3_dbg_cond1 - unused, tied down. 011 = Select inst3_dbg_cond2 - unused, tied down. 012 = Select inst3_dbg_cond3 - unused, tied down. 013 = Select inst3_dbg_cond2timeout - unused, tied down. 014 = Select inst4_dbg_cond1 - unused, tied down. 015 = Select inst4_dbg_cond2 - unused, tied down. 016 = Select inst4_dbg_cond3 - unused, tied down. 017 = Select inst4_dbg_cond2timeout - unused, tied down. 018 = Select inst1_dbg_trig_sp. 019 = Select inst2_dbg_trig_sp. 020 = Select inst3_dbg_trig_sp - unused, tied down. 021 = Select inst4_dbg_trig_sp - unused, tied down. 022 = Select tctrc_tcdbg_trigger_a(0). 023 = Select tctrc_tcdbg_trigger_b(0). 024 = Select tctrc_tcdbg_trigger_a(0) and tctrc_tcdbg_trigger_b(0). 025 = Select tctrc_tcdbg_trigger_a(1). 026 = Select tctrc_tcdbg_trigger_b(1). 027 = Select tctrc_tcdbg_trigger_a(1) and tctrc_tcdbg_trigger_b(1). 028 = Select tctrc_tcdbg_trigger_a(2). 029 = Select tctrc_tcdbg_trigger_b(2). 030 = Select tctrc_tcdbg_trigger_a(2) and tctrc_tcdbg_trigger_b(2). 031 = Select tctrc_tcdbg_trigger_a(3). 032 = Select tctrc_tcdbg_trigger_b(3). 033 = Select tctrc_tcdbg_trigger_a(3) and tctrc_tcdbg_trigger_b(3). 034 = Select tctrc_tcdbg_trigger_a(4). 035 = Select tctrc_tcdbg_trigger_b(4). 036 = Select tctrc_tcdbg_trigger_a(4) and tctrc_tcdbg_trigger_b(4). 037 = Select tctrc_tcdbg_trigger_a(5). 038 = Select tctrc_tcdbg_trigger_b(5). 039 = Select tctrc_tcdbg_trigger_a(5) and tctrc_tcdbg_trigger_b(5). 040 = Select tctrc_tcdbg_trigger_a(6). 041 = Select tctrc_tcdbg_trigger_b(6). 042 = Select tctrc_tcdbg_trigger_a(6) and tctrc_tcdbg_trigger_b(6). 043 = Select tctrc_tcdbg_trigger_a(7). 044 = Select tctrc_tcdbg_trigger_b(7). 045 = Select tctrc_tcdbg_trigger_a(7) and tctrc_tcdbg_trigger_b(7). 046 = Select tctrc_tcdbg_trigger_a(8). 047 = Select tctrc_tcdbg_trigger_b(8). 048 = Select tctrc_tcdbg_trigger_a(8) and tctrc_tcdbg_trigger_b(8). 049 = Select tctrc_tcdbg_trigger_a(9). 050 = Select tctrc_tcdbg_trigger_b(9). 051 = Select tctrc_tcdbg_trigger_a(9) and tctrc_tcdbg_trigger_b(9). 052 = Select tctrc_tcdbg_trigger_a(10). 053 = Select tctrc_tcdbg_trigger_b(10). 054 = Select tctrc_tcdbg_trigger_a(10) and tctrc_tcdbg_trigger_b(10). 055 = Select tctrc_tcdbg_trigger_a(11). 056 = Select tctrc_tcdbg_trigger_b(11). 057 = Select tctrc_tcdbg_trigger_a(11) and tctrc_tcdbg_trigger_b(11). 058 = Select tctrc_tcdbg_trigger_a(12). 059 = Select tctrc_tcdbg_trigger_b(12). 060 = Select tctrc_tcdbg_trigger_a(12) and tctrc_tcdbg_trigger_b(12). 061 = Select tctrc_tcdbg_trigger_a(13). 062 = Select tctrc_tcdbg_trigger_b(13).

Bits	SCOM	Field Mnemonic: Description
		063 = Select tctrc_tcdbg_trigger_a(13) and tctrc_tcdbg_trigger_b(13). 064 = Select tctrc_tcdbg_trigger_a(14). 065 = Select tctrc_tcdbg_trigger_b(14). 066 = Select tctrc_tcdbg_trigger_a(14) and tctrc_tcdbg_trigger_b(14). 067 = Select tctrc_tcdbg_trigger_a(15). 068 = Select tctrc_tcdbg_trigger_b(15). 069 = Select tctrc_tcdbg_trigger_a(15) and tctrc_tcdbg_trigger_b(15). 070 = Select tctrc_tcdbg_trigger_a(16). 071 = Select tctrc_tcdbg_trigger_b(16). 072 = Select tctrc_tcdbg_trigger_a(16) and tctrc_tcdbg_trigger_b(16). 073 = Select tctrc_tcdbg_trigger_a(17). 074 = Select tctrc_tcdbg_trigger_b(17). 075 = Select tctrc_tcdbg_trigger_a(17) and tctrc_tcdbg_trigger_b(17). -- LOGIC (UNIT) TRIGGERS -- EP: 0:3 L3C0, 4:7 L3C1, 8:9 GX, 10 TP (hang), 11 spare, 12:13 MCA, 14:15 spare. ES: 0:4 L4C, 5:6 L4F, 7:8 TPTOD, 9 TP (hang), 10:15 spare. 076 = Select logic_trigger_in(0). 077 = Select logic_trigger_in(1). 078 = Select logic_trigger_in(2). 079 = Select logic_trigger_in(3). 080 = Select logic_trigger_in(4). 081 = Select logic_trigger_in(5). 082 = Select logic_trigger_in(6). 083 = Select logic_trigger_in(7). 084 = Select logic_trigger_in(8). 085 = Select logic_trigger_in(9). 086 = Select logic_trigger_in(10). 087 = Select logic_trigger_in(11). 088 = Select logic_trigger_in(12). 089 = Select logic_trigger_in(13). 090 = Select logic_trigger_in(14). 091 = Select logic_trigger_in(15). 092 = Select pc_tcdbg_trigger(0). 093 = Select pc_tcdbg_trigger(1). 094 = Select tctrc_tcdbg_glb_brcst(0). 095 = Select tctrc_tcdbg_glb_brcst(1). 096 = Select xstop_err. 097 = Select recov_err. 098 = Select spattn. 099 = Select fir_dbg_local_xstop_err. 100 = Select tc_dbg_inter_brcst(0). 101 = Select tc_dbg_inter_brcst(1). -- CORE TRIGGERS (EP chip only) -- **Note:** Set core_slave_mode to honor ec[0:5]_tc_trace_run. 102 = Select core trigger 0: any rising edge of ec[0:5]_tc_trace_run(0). 103 = Select core trigger 1: any rising edge of ec[0:5]_tc_trace_run(1). 104 = Select core trigger 2: any falling edge of ec[0:5]_tc_trace_run(0). 105 = Select core trigger 3: any falling edge of ec[0:5]_tc_trace_run(1). 106 = Select glb_trig_or_trace_in(0). 107 = Select glb_trig_or_trace_in(1). 108 = Select core_local_brcst_trc(0). 109 = Select core_local_brcst_trc(1). 110 = Select glb_freeze_brcst_rec(0). 111 = Select trig_2_extern_in(0). 112 = Select trig_2_extern_in(1). 113 = Select dbg_triggers_out(2). 114 = Select dbg_triggers_out(3). 115 = Select dbg_triggers_out(4). 116 = Select dbg_triggers_out(5). 117 = Select dbg_triggers_out(6). 118 = Select tcdbg_trigger_in(0).

Bits	SCOM	Field Mnemonic: Description
		119 = Select tcdbg_trigger_in(1).
8:15	RW	INST1_COND1_SEL_B: Multiplexer for cond1_trig_in(1). Selection as cond1_trig_in(0).
16:23	RW	INST1_COND2_SEL_A: Multiplexer for cond2_trig_in(0). Selection as cond1_trig_in(0).
24:31	RW	INST1_COND2_SEL_B: Multiplexer for cond2_trig_in(1). Selection as cond1_trig_in(0).
32	RW	INST1_C1_INAROW_MODE: Front end instance 1 c1_inarow_mode.
33	RW	INST1_AND_TRIGGER_MODE1: Front end instance 1 and trigger mode condition1.
34	RW	INST1_NOT_TRIGGER_MODE1: Front end instance 1 inverted trigger mode condition1.
35	RW	INST1_EDGE_TRIGGER_MODE1: Front end instance 1 edge trigger mode condition1.
36:38	RWX	INST1_UNUSED_1: Unused.
39	RW	INST1_C2_INAROW_MODE: Front end instance 1 counter 2 in-a-row mode.
40	RW	INST1_AND_TRIGGER_MODE2: Front end instance 1 and trigger mode2.
41	RW	INST1_NOT_TRIGGER_MODE2: Front end instance 1 inverted (not) trigger.
42	RW	INST1_EDGE_TRIGGER_MODE2: Front end instance 1edge trigger.
43:45	RWX	INST1_UNUSED_2: Unused.
46	RW	INST1_COND3_ENABLE_RESET: Front end instance 1 condition3 enable.
47	RW	INST1_EXACT_TO_MODE: Front end instance 1 exact timeout mode.
48	RW	INST1_RESET_C2TIMER_ON_C1: Front end instance 1 reset condition2 timer on condition1.
49	RW	INST1_RESET_C3_ON_C0: Front end instance 1 reset condition3 on condition0.
50	RW	INST1_SLOW_TO_MODE: Front end instance 1 slow timeout mode.
51	RW	INST1_EXACT_RESET_C3_ON_TO: Front end instance 1 exact reset condition3 on timeout.
52:55	RW	INST1_C1_COUNT_LT: inst1 condition1 counter compare value.
56:59	RW	INST1_C2_COUNT_LT: inst1 condition2 counter compare value.
60:62	RW	INST1_RESET_C3_SELECT: Front end instance 1: reset condition3 for reset_c3_on_c0. 0B100 = dbg_cross_couple_triggers(4). 0b101 = dbg_cross_couple_triggers(12). 0b110 = dbg_cross_couple_triggers(20). 0b111 = dbg_cross_couple_triggers(28).

Register Name	**Debug Instance 1 Condition 2 Register**
Mnemonic	TP.TCEP03.TPCL3.EPS.DBG.DBG_INST1_COND_REG_2
Address	00000000130107C2 (SCOM)
Description	This is debug macro configuration register 2 for front-end component 1.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	INST1_CROSS_COUPLE_SELECT_1_A: Cross coupling is the same for all selectors: 00000 = Select inst1_cond1_trig_a. 00001 = Select inst1_cond1_trig_b. 00010 = Select inst1_cond2_trig_a. 00011 = Select inst1_cond2_trig_b. 00100 = Select inst1_condition1. 00101 = Select inst1_condition2. 00110 = Select inst1_condition3. 00111 = Select inst1_cond2_timeout. 01000 = Select inst2_cond1_trig_a. 01001 = Select inst2_cond1_trig_b. 01010 = Select inst2_cond2_trig_a. 01011 = Select inst2_cond2_trig_b. 01100 = Select inst2_condition1. 01101 = Select inst2_condition2. 01110 = Select inst2_condition3. 01111 = Select inst2_cond2_timeout. 10000 = Select inst3_cond1_trig_a. 10001 = Select inst3_cond1_trig_b. 10010 = Select inst3_cond2_trig_a. 10011 = Select inst3_cond2_trig_b. 10100 = Select inst3_condition1. 10101 = Select inst3_condition2. 10110 = Select inst3_condition3. 10111 = Select inst3_cond2_timeout. 11000 = Select inst4_cond1_trig_a. 11001 = Select inst4_cond1_trig_b. 11010 = Select inst4_cond2_trig_a. 11011 = Select inst4_cond2_trig_b. 11100 = Select inst4_condition1. 11101 = Select inst4_condition2. 11110 = Select inst4_condition3. 11111 = Select inst4_cond2_timeout.
5:9	RW	INST1_CROSS_COUPLE_SELECT_1_B: inst1_cross_couple_select_1_b.
10:14	RW	INST1_CROSS_COUPLE_SELECT_2_A: inst1_cross_couple_select_2_a.
15:19	RW	INST1_CROSS_COUPLE_SELECT_2_B: inst1_cross_couple_select_2_b.
20:43	RW	INST1_TO_CMP_LT: Compare value for special counter sp_cnt_lt in debug component 1.
44	RW	INST1_FORCE_TEST_MODE: Force test mode to indicate compare without actual compare.

Register Name	Debug Instance 1 Condition 3 Register
Mnemonic	TP.TCEP03.TPCL3.EPS.DBG.DBG_INST1_COND_REG_3
Address	00000000130107C3 (SCOM)
Description	This is debug macro configuration register 2 for the front-end 1 component.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	INST1_SP_COUNT_LT: Timeout counter to_cmp compare value for dbg_cond_comp_1.

Register Name	Debug Instance 2 Condition 1 Register
Mnemonic	TP.TCEP03.TPCL3.EPS.DBG.DBG_INST2_COND_REG_1
Address	00000000130107C4 (SCOM)
Description	This is debug macro configuration register 1 for the front-end 1 component.

Bits	SCOM	Field Mnemonic: Description
0:7	RW	INST2_COND1_SEL_A: Multiplexer for cond1_trig_in(0). 000 = Select constant 0 001 = Select constant 1 -- CONDITION FEEDBACK -- 002 = Select inst2_dbg_cond1. 003 = Select inst2_dbg_cond2. 004 = Select inst2_dbg_cond3. 005 = Select inst2_dbg_cond2timeout. 006 = Select inst2_dbg_cond1. 007 = Select inst2_dbg_cond2. 008 = Select inst2_dbg_cond3. 009 = Select inst2_dbg_cond2timeout. 010 = Select inst3_dbg_cond1 - unused, tied down. 011 = Select inst3_dbg_cond2 - unused, tied down. 012 = Select inst3_dbg_cond3 - unused, tied down. 013 = Select inst3_dbg_cond2timeout - unused, tied down. 014 = Select inst4_dbg_cond1 - unused, tied down. 015 = Select inst4_dbg_cond2 - unused, tied down. 016 = Select inst4_dbg_cond3 - unused, tied down. 017 = Select inst4_dbg_cond2timeout - unused, tied down. 018 = Select inst2_dbg_trig_sp. 019 = Select inst2_dbg_trig_sp. 020 = Select inst3_dbg_trig_sp - unused, tied down. 021 = Select inst4_dbg_trig_sp - unused, tied down. 022 = Select tctrc_tcdbg_trigger_a(0). 023 = Select tctrc_tcdbg_trigger_b(0). 024 = Select tctrc_tcdbg_trigger_a(0) and tctrc_tcdbg_trigger_b(0). 025 = Select tctrc_tcdbg_trigger_a(1). 026 = Select tctrc_tcdbg_trigger_b(1). 027 = Select tctrc_tcdbg_trigger_a(1) and tctrc_tcdbg_trigger_b(1). 028 = Select tctrc_tcdbg_trigger_a(2). 029 = Select tctrc_tcdbg_trigger_b(2). 030 = Select tctrc_tcdbg_trigger_a(2) and tctrc_tcdbg_trigger_b(2). 031 = Select tctrc_tcdbg_trigger_a(3). 032 = Select tctrc_tcdbg_trigger_b(3). 033 = Select tctrc_tcdbg_trigger_a(3) and tctrc_tcdbg_trigger_b(3). 034 = Select tctrc_tcdbg_trigger_a(4). 035 = Select tctrc_tcdbg_trigger_b(4). 026 = Select tctrc_tcdbg_trigger_a(4) and tctrc_tcdbg_trigger_b(4). 027 = Select tctrc_tcdbg_trigger_a(5). 028 = Select tctrc_tcdbg_trigger_b(5). 029 = Select tctrc_tcdbg_trigger_a(5) and tctrc_tcdbg_trigger_b(5). 030 = Select tctrc_tcdbg_trigger_a(6). 031 = Select tctrc_tcdbg_trigger_b(6). 032 = Select tctrc_tcdbg_trigger_a(6) and tctrc_tcdbg_trigger_b(6). 033 = Select tctrc_tcdbg_trigger_a(7). 034 = Select tctrc_tcdbg_trigger_b(7). 035 = Select tctrc_tcdbg_trigger_a(7) and tctrc_tcdbg_trigger_b(7). 036 = Select tctrc_tcdbg_trigger_a(8). 037 = Select tctrc_tcdbg_trigger_b(8). 038 = Select tctrc_tcdbg_trigger_a(8) and tctrc_tcdbg_trigger_b(8). 039 = Select tctrc_tcdbg_trigger_a(9). 040 = Select tctrc_tcdbg_trigger_b(9).

Bits	SCOM	Field Mnemonic: Description
		041 = Select tctrc_tcdbg_trigger_a(9) and tctrc_tcdbg_trigger_b(9). 042 = Select xstop_err. 043 = Select recov_err. 044 = Select spattn. 045 = Select fir_dbg_local_xstop_err. 046 = Select tc_dbg_inter_brcst(0). 047 = Select tc_dbg_inter_brcst(1). -- LOGIC (UNIT) TRIGGERS -- EP: 0:3 L3C0, 4:7 L3C1, 8:9 GX, 10 TP (hang), 11 spare, 12:13 MCA, 14:15 spare. ES: 0:4 L4C, 5:6 L4F, 7:8 TPTOD, 9 TP (hang), 10:15 spare. 102 = Select logic_trigger_in(0). 103 = Select logic_trigger_in(1). 104 = Select logic_trigger_in(2). 105 = Select logic_trigger_in(3). 106 = Select logic_trigger_in(4). 107 = Select logic_trigger_in(5). 108 = Select logic_trigger_in(6). 109 = Select logic_trigger_in(7). 110 = Select logic_trigger_in(8). 111 = Select logic_trigger_in(9). 112 = Select logic_trigger_in(10). 113 = Select logic_trigger_in(11). 114 = Select logic_trigger_in(12). 115 = Select logic_trigger_in(13). 116 = Select logic_trigger_in(14). 117 = Select logic_trigger_in(15). -- CORE TRIGGERS (EP chip only) -- **Note:** Set core_slave_mode to honor ec[0:5]_tc_trace_run. 118 = Select core trigger 0: any rising edge of ec[0:5]_tc_trace_run(0). 119 = Select core trigger 1: any rising edge of ec[0:5]_tc_trace_run(1). 120 = Select core trigger 2: any falling edge of ec[0:5]_tc_trace_run(0). 121 = Select core trigger 3: any falling edge of ec[0:5]_tc_trace_run(1). -- BROADCAST / ERRORS. 122 = Select glb_trc_bdcst_recv (received global broadcast). 123 = Select edge detected fir_dbg_xstop_err. 124 = Select edge detected fir_dbg_recov_err. 125 = Select edge detected fir_dbg_spatn. 126 ... 127 = Select constant 0 (unused).
8:15	RW	INST2_COND1_SEL_B: Multiplexer for cond1_trig_in(1). Selection as cond1_trig_in(0).
16:23	RW	INST2_COND2_SEL_A: Multiplexer for cond2_trig_in(0). Selection as cond1_trig_in(0).
24:31	RW	INST2_COND2_SEL_B: Multiplexer for cond2_trig_in(1). Selection as cond1_trig_in(0).
32	RW	INST2_C1_INAROW_MODE: Front end instance 1 c1_inarow_mode.
33	RW	INST2_AND_TRIGGER_MODE1: Front end instance 1 and trigger mode condition1.
34	RW	INST2_NOT_TRIGGER_MODE1: Front end instance 1 inverted trigger mode condition1.
35	RW	INST2_EDGE_TRIGGER_MODE1: Front end instance 1 edge trigger mode condition1.
36:38	RWX	INST2_UNUSED_1: Unused.
39	RW	INST2_C2_INAROW_MODE: Front end instance 1 counter 2 in-a-row mode.
40	RW	INST2_AND_TRIGGER_MODE2: Front end instance 1 and trigger mode2.
41	RW	INST2_NOT_TRIGGER_MODE2: Front end instance 1 inverted (not) trigger.
42	RW	INST2_EDGE_TRIGGER_MODE2: Front end instance 1edge trigger.

Bits	SCOM	Field Mnemonic: Description
43:45	RWX	INST2_UNUSED_2: Unused.
46	RW	INST2_COND3_ENABLE_RESET: Front end instance 1 condition3 enable.
47	RW	INST2_EXACT_TO_MODE: Front end instance 1 exact timeout mode.
48	RW	INST2_RESET_C2TIMER_ON_C1: Front end instance 1 reset condition2 timer on condition1.
49	RW	INST2_RESET_C3_ON_C0: Front end instance 1 reset condition3 on condition0.
50	RW	INST2_SLOW_TO_MODE: Front end instance 1 slow timeout mode.
51	RW	INST2_EXACT_RESET_C3_ON_TO: Front end instance 1 exact reset condition3 on timeout.
52:55	RW	INST2_C1_COUNT_LT: inst2 condition1 counter compare value.
56:59	RW	INST2_C2_COUNT_LT: inst2 condition2 counter compare value.
60:62	RW	INST2_RESET_C3_SELECT: Front end instance 1: reset condition3 for reset_c3_on_c0. 0b100 = dbg_cross_couple_triggers(4). 0b101 = dbg_cross_couple_triggers(12). 0b110 = dbg_cross_couple_triggers(20). 0b111 = dbg_cross_couple_triggers(28).

Register Name	Debug Macro Configuration 2 Register
Mnemonic	TP.TCEP03.TPCL3.EPS.DBG.DBG_INST2_COND_REG_2
Address	00000000130107C5 (SCOM)
Description	Debug macro configuration register 2 for front end 1 component

Bits	SCOM	Field Mnemonic: Description
0:4	RW	INST2_CROSS_COUPLE_SELECT_1_A: Cross coupling is the same for all selectors: 00000 = Select inst2_cond1_trig_a. 00001 = Select inst2_cond1_trig_b. 00010 = Select inst2_cond2_trig_a. 00011 = Select inst2_cond2_trig_b. 00100 = Select inst2_condition1. 00101 = Select inst2_condition2. 00110 = Select inst2_condition3. 00111 = Select inst2_cond2_timeout. 01000 = Select inst2_cond1_trig_a. 01001 = Select inst2_cond1_trig_b. 01010 = Select inst2_cond2_trig_a. 01011 = Select inst2_cond2_trig_b. 01100 = Select inst2_condition1. 01101 = Select inst2_condition2. 01110 = Select inst2_condition3. 01111 = Select inst2_cond2_timeout. 10000 = Select inst3_cond1_trig_a. 10001 = Select inst3_cond1_trig_b. 10010 = Select inst3_cond2_trig_a. 10011 = Select inst3_cond2_trig_b. 10100 = Select inst3_condition1. 10101 = Select inst3_condition2. 10110 = Select inst3_condition3. 10111 = Select inst3_cond2_timeout. 11000 = Select inst4_cond1_trig_a. 11001 = Select inst4_cond1_trig_b. 11010 = Select inst4_cond2_trig_a. 11011 = Select inst4_cond2_trig_b. 11100 = Select inst4_condition1. 11101 = Select inst4_condition2. 11110 = Select inst4_condition3. 11111 = Select inst4_cond2_timeout.
5:9	RW	INST2_CROSS_COUPLE_SELECT_1_B: inst2 cross couple select 1b.
10:14	RW	INST2_CROSS_COUPLE_SELECT_2_A: inst2 cross couple select 2a.
15:19	RW	INST2_CROSS_COUPLE_SELECT_2_B: inst2 cross couple select 2b.
20:43	RW	INST2_TO_CMP_LT: Compare value for special counter sp_cnt_lt in debug component 2.
44	RW	INST2_FORCE_TEST_MODE: Force test mode to indicate compare without actual compare.

Register Name	Debug Instance 2 Condition 3 Register
Mnemonic	TP.TCEP03.TPCL3.EPS.DBG.DBG_INST2_COND_REG_3
Address	00000000130107C6 (SCOM)
Description	This is debug macro configuration register 2 for the front-end 1 component.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	INST2_SP_COUNT_LT: Timeout counter to_cmp compare value for dbg_cond_comp_1.

Register Name	Debug Trace 0 Register
Mnemonic	TP.TCEP03.TPCL3.EPS.DBG.DBG_TRACE_REG_0
Address	00000000130107CD (SCOM)
Description	This is debug macro configuration register 0 for the debug back-end component.

Bits	SCOM	Field Mnemonic: Description
0	RW	INST1_COND3_ENABLE: Enable of instance 1 condition 3.
1	RW	INST2_COND3_ENABLE: Enable of instance 2 condition 3.
2	RW	INST3_COND3_ENABLE: Unused.
3	RW	INST4_COND3_ENABLE: Unused.
4	RW	INST1_SLOW_LFSR_MODE: Enable slow LFSR mode of front end instance 1.
5	RW	INST2_SLOW_LFSR_MODE: Enable slow LFSR mode of front end instance 2.
6	RW	INST3_SLOW_LFSR_MODE: Unused.
7	RW	INST4_SLOW_LFSR_MODE: Unused.
8:9	RW	INST1_CONDITION1_TRIG_SEL: Select inst1 condition1 for output (external) triggers. 00 = Do nothing. 01 = trigger_out(0). 10 = trigger_out(1). 11 = trigger_out(2).
10:11	RW	INST1_CONDITION2_TRIG_SEL: Select inst1 condition2 for output (external) triggers. 00 = Do nothing. 01 = trigger_out(0). 10 = trigger_out(1). 11 = trigger_out(2).
12:13	RW	INST1_C2_TIMEOUT_TRIG_SEL: Select inst1 c2 time-out counter for output (external) triggers. 00 = Do nothing. 01 = trigger_out(0). 10 = trigger_out(1). 11 = trigger_out(2).
14:15	RW	INST2_CONDITION1_TRIG_SEL: Select inst2 condition1 for output (external) triggers. 00 = Do nothing. 01 = trigger_out(0). 10 = trigger_out(1). 11 = trigger_out(2).
16:17	RW	INST2_CONDITION2_TRIG_SEL: Select inst2 condition2 trigger for output (external) triggers. 00 = Do nothing. 01 = trigger_out(0). 10 = trigger_out(1). 11 = trigger_out(2).
18:19	RW	INST2_C2_TIMEOUT_TRIG_SEL: Select inst2 c2 time-out counter for output (external) triggers. 00 = Do nothing. 01 = trigger_out(0). 10 = trigger_out(1). 11 = trigger_out(2).
20:31	RO	constant = 0b000000000000
32	RW	EXT_TRIG_ON_STOP: Enable trigger on stop.
33	RW	EXT_TRIG_ON_FREEZE: Enable trigger on freeze.
34:38	RW	CORE_RAS0_TRIG_SEL:
39:43	RW	CORE_RAS1_TRIG_SEL:

Bits	SCOM	Field Mnemonic: Description
44:45	RW	PC_TP_TRIG_SEL:
46:49	RW	DBG_ARM_SEL:
50:53	RW	TRIG0_LEVEL_SEL: Select additional conditions for output (external) trigger signal trigger_out(0). **Note:** Some are N/A (inst3/4 conditions are tied to zero). 0001 = inst1_cond3_state_int(1). 0010 = inst1_cond3_state_int(0). 0011 = inst2_cond3_state_int(1). 0100 = inst2_cond3_state_int(0). 0101 = inst3_cond3_state_int(1). 0110 = inst3_cond3_state_int(0). 0111 = inst4_cond3_state_int(1). 1000 = inst4_cond3_state_int(0). 1001 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1). 1010 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1). 1011 = inst3_cond3_state_int(1) or inst4_cond3_state_int(1). 1100 = inst3_cond3_state_int(1) and inst4_cond3_state_int(1). 1101 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1). 1110 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1) and inst3_cond3_state_int(1). 1111 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1) or inst4_cond3_state_int(1).
54:57	RW	TRIG1_LEVEL_SEL: Select additional conditions for output (external) trigger signal trigger_out(1). **Note:** Some are N/A (inst3/4 conditions are tied to zero). 0001 = inst1_cond3_state_int(1). 0010 = inst1_cond3_state_int(0). 0011 = inst2_cond3_state_int(1). 0100 = inst2_cond3_state_int(0). 0101 = inst3_cond3_state_int(1). 0110 = inst3_cond3_state_int(0). 0111 = inst4_cond3_state_int(1). 1000 = inst4_cond3_state_int(0). 1001 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1). 1010 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1). 1011 = inst3_cond3_state_int(1) or inst4_cond3_state_int(1). 1100 = inst3_cond3_state_int(1) and inst4_cond3_state_int(1). 1101 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1). 1110 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1) and inst3_cond3_state_int(1). 1111 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1) or inst4_cond3_state_int(1).
58:63	RO	constant = 0b000000

Register Name	**Debug Trace 1 Register**
Mnemonic	TP.TCEP03.TPCL3.EPS.DBG.DBG_TRACE_REG_1
Address	00000000130107CE (SCOM)
Description	This is debug macro configuration register 1 for the back-end component.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	INST1_CONDITION1_ACTION_DO: Inst1 action selection, condition1: 00 = No action. 01 = Start. 10 = Stop. 11 = RUNN: Start now, stop after n cycles.

Bits	SCOM	Field Mnemonic: Description
2:3	RW	INST1_CONDITION2_ACTION_DO: Inst1 action selection, condition2: 00 = No action. 01 = Start. 10 = Stop. 11 = RUNN: Start now, stop after n cycles.
4:5	RW	INST1_C2_TIMEOUT_ACTION_DO: Inst1 action selection, c2_timeout: 00 = No action. 01 = Start. 10 = Stop. 11 = RUNN: Start now, stop after n cycles.
6:7	RW	INST2_CONDITION1_ACTION_DO: inst2 action selection, condition1: 00 = No action. 01 = Start. 10 = Stop. 11 = RUNN: Start now, stop after n cycles.
8:9	RW	INST2_CONDITION2_ACTION_DO: Inst2 action selection, condition2: 00 = No action. 01 = Start. 10 = Stop. 11 = RUNN: Start now, stop after n cycles.
10:11	RW	INST2_C2_TIMEOUT_ACTION_DO: Inst2 action selection, c2_timeout: 00 = No action. 01 = Start. 10 = Stop. 11 = RUNN: Start now, stop after n cycles.
12:23	RO	constant = 0b000000000000
24	RW	INST1_CONDITION1_ACTION_WAITN: For wait-N.
25	RW	INST1_CONDITION2_ACTION_WAITN: For wait-N.
26	RW	INST1_C2_TIMEOUT_ACTION_WAITN: For wait-N.
27	RW	INST2_CONDITION1_ACTION_WAITN: For wait-N.
28	RW	INST2_CONDITION2_ACTION_WAITN: For wait-N.
29	RW	INST2_C2_TIMEOUT_ACTION_WAITN: For wait-N.
30:35	RO	constant = 0b000000
36	RW	INST1_CONDITION1_ACTION_BANK: Trace bank switch (inst1, condition1).
37	RW	INST1_CONDITION2_ACTION_BANK: Trace bank switch (inst1, condition2).
38	RW	INST1_C2_TIMEOUT_ACTION_BANK: Trace bank switch (inst1, c2_timeout).
39	RW	INST2_CONDITION1_ACTION_BANK: Trace bank switch (inst2, condition1).
40	RW	INST2_CONDITION2_ACTION_BANK: Trace bank switch (inst2, condition2).
41	RW	INST2_C2_TIMEOUT_ACTION_BANK: Trace bank switch (inst2, c2_timeout).
42:47	RO	constant = 0b000000
48:50	RW	INST1_CHECKSTOP_MODE_LT: Select additional condition with fir_error_lt for dbg_fir_xstop_on_trig output: 000 = inst1_condition1_lt. 001 = inst1_condition2_lt. 010 = inst1_condition3_lt. 011 = inst1_cond2_timeout_lt. 1xx = Disable checkstop_mode.

Bits	SCOM	Field Mnemonic: Description
51	RW	INST1_CHECKSTOP_MODE_SELECTOR: enable_fir_trig_xstop. Enable checkstop on debug trigger: 0 = Disable checkstop on debug trigger. 1 = Enable checkstop on debug trigger.
52:54	RW	INST2_CHECKSTOP_MODE_LT: Select additional condition with fir_error_lt for dbg_fir_xstop_on_trig output: 000 = inst2_condition1_lt. 001 = inst2_condition2_lt. 010 = inst2_condition3_lt. 011 = inst2_cond2_timeout_lt. 1xx = Disable checkstop_mode.
55	RW	INST2_CHECKSTOP_MODE_SELECTOR: Enable checkstop on FIR error: 0 = Disable checkstop on FIR error. 1 = Enable checkstop on FIR error.
56:63	RO	constant = 0b00000000

Register Name	Debug Trace Mode 2 Register
Mnemonic	TP.TCEP03.TPCL3.EPS.DBG.DBG_TRACE_MODE_REG_2
Address	00000000130107CF (SCOM)
Description	This is debug macro configuration register 2 for the back-end component.

Bits	SCOM	Field Mnemonic: Description
0:15	RW	RUNN_COUNT_COMPARE_VALUE: Compare value for the RUNN counter used in trace modes RUNN and wait-N.
16	RW	IMM_FREEZE_MODE: Immediate freeze mode.
17	RW	STOP_ON_ERR: Stop and freeze on checkstop.
18	RW	BANK_ON_RUNN_MATCH: Bank switch on RUNN match.
19	RW	FORCE_TEST_MODE: Force RUNN condition to be true.
20	RW	ACCUM_HIST_MODE: Accumulate history mode, do not clear history mode when trace_run active.
21	RW	FRZ_COUNT_ON_FRZ: Freeze condition counters on trace freeze.

Register Name	Debug Trace Control Register
Mnemonic	TP.TCEP03.TPCL3.EPS.DBG.DEBUG_TRACE_CONTROL
Address	00000000130107D0 (SCOM)
Description	This is the trace start/stop/rest using SCOM command register. Use write data(0/1/2) = 1. This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0	WOX	Reserved field.
1	WOX	Reserved field.
2	WOX	Reserved field.

Register Name	Extra Trace Mode Register
Mnemonic	TP.TCEP03.TPCL3.EPS.DBG.XTRA_TRACE_MODE
Address	00000000130107D1 (SCOM)
Description	This register provides an extra or dedicated trace mode register for core triggers.

Bits	SCOM	Field Mnemonic: Description
0:37	RW	XTRA_TRACE_MODE_DATA: Extra / dedicated trace mode register for core triggers.

Register Name	L2 FIR Register
Mnemonic	EX07.L2.L2MISC.L2CERRS.FIR_REG
Address	0000000013010C00 (SCOM) 0000000013010C01 (SCOM1) 0000000013010C02 (SCOM2)
Description	L2 FIR register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	CACHE_RD_CE: Hardware trigger mechanism at point cache read occurs that detects a CE by ECCCK on RC/CO/SN read. **Note:** PRD counts the number of these and then triggers line delete.
1	RWX	WOX_AND	WOX_OR	CACHE_RD_UE: Hardware trigger mechanism at point cache read occurs that detects a UE (non-SUE) by ECCCK on RC/CO/SN read.
2	RWX	WOX_AND	WOX_OR	CACHE_RD_SUE: Hardware trigger mechanism at point cache read occurs that detects a SUE by ECCCK on RC/CO/SN read.
3	RWX	WOX_AND	WOX_OR	HW_DIR_INTIATED_LINE_DELETE_OCCURRED: Hardware-initiated line delete occurred (ID state injected into the DIR) by RC or SN machine.
4	RWX	WOX_AND	WOX_OR	CACHE_UE_SUE_DETECTED_ON_MODIFIED_LINE_BY_CO: L2 cast-out where a L2 cache read detected UE/SUE and line is M,Mu,T,Tn.
5	RWX	WOX_AND	WOX_OR	CACHE_UE_SUE_DETECTED_ON_NON_MODIFIED_LINE_BY_CO: L2 cast-out where a L2 cache read detected UE/SUE and line is Me,Te,Ten,Sl,S.
6	RWX	WOX_AND	WOX_OR	DIR_CE_DETECTED: L2 corrected a CE in the L2 directory.
7	RWX	WOX_AND	WOX_OR	DIR_UE_DETECTED: L2 detected a UE in the L2 directory.
8	RWX	WOX_AND	WOX_OR	DIR_STUCK_BIT_CE: L2 detected an SBCE in the L2 directory.
9	RWX	WOX_AND	WOX_OR	DIR_SBCE_REPAIR_FAILED: PEC attempted to repair and cast-out a SBCE condition but failed. The cache line was lost.
10	RWX	WOX_AND	WOX_OR	MULTIPLE_DIR_ERRORS_DETECTED: **Depricated:** *This FIR bit should always be masked.* Multiple CE/UE detected between two hang (early hang) pulse time windows.
11	RWX	WOX_AND	WOX_OR	LRU_READ_ERROR_DETECTED: LRU array has illegal value in it (due to a flipped bit).
12	RWX	WOX_AND	WOX_OR	RC_POWERBUS_DATA_TIMEOUT: RC timed out waiting for processor bus to return data.
13	RWX	WOX_AND	WOX_OR	NCU_POWERBUS_DATA_TIMEOUT: NCU timed out waiting for processor bus to return data.
14	RWX	WOX_AND	WOX_OR	HW_CONTROL_ERROR: Internal hardware control error.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
15	RWX	WOX_AND	WOX_OR	LRU_ALL_MEMBERS_IN_CGC_ARE_LINE_DELETED: All members in a single congruence class have been deleted.
16	RWX	WOX_AND	WOX_OR	CACHE_INHIBITED_HIT_CACHEABLE_ERROR: Cache inhibited LD/ST hit a line in the L2 cache. Software error.
17	RWX	WOX_AND	WOX_OR	RC_LOAD_RECEIVED_PB_CRESP_ADR_ERR: RC was doing a fabric operation on behalf of a load and received a CRESP=addr_err.
18	RWX	WOX_AND	WOX_OR	RC_STORE_RECEIVED_PB_CRESP_ADR_ERR: RC was doing a fabric operation on behalf of a store and received a CRESP=addr_err.
19	RWX	WOX_AND	WOX_OR	RC_POWBUS_DATA_CE_ERR_FROM_F2CHK: RC incoming power bus data had a CE error.
20	RWX	WOX_AND	WOX_OR	RC_POWBUS_DATA_UE_ERR_FROM_F2CHK: RC incoming power bus data had a UE error.
21	RWX	WOX_AND	WOX_OR	RC_POWBUS_DATA_SUE_ERR_FROM_F2CHK: RC incoming power bus data had a SUE error.
22	RWX	WOX_AND	WOX_OR	TGT_NODAL_REQ_DINC_ERR: Foreign CPS request got retry DINC.
23	RWX	WOX_AND	WOX_OR	RC_LOAD_RECEIVED_PB_CRESP_ADR_ERR_FOR_HYP: RC was doing a fabric operation on behalf of a load and received a CRESP=addr_err for HYP memory.
24	RWX	WOX_AND	WOX_OR	RCDAT_RD_PARITY_ERR: RCDAT read parity error.
25	RWX	WOX_AND	WOX_OR	CO_PSH_RECEIVED_PB_CRESP_ADR_ERR: CO or SNP was doing a fabric operation on behalf of a store and received a CRESP=addr_err.
26	RWX	WOX_AND	WOX_OR	LVDIR_PERR: LVDIR took a parity error.
27	RWX	WOX_AND	WOX_OR	RC_LOAD_RECEIVED_PB_ACK_DEAD_FROM_ALINKRECOV: RC load received pb_ack_dead from alinkrecov.
28	RWX	WOX_AND	WOX_OR	DARN_DATA_TIMEOUT: Darn timed out waiting for data.
29	RWX	WOX_AND	WOX_OR	RC_STORE_RECEIVED_PB_ACK_DEAD_FROM_ALINKRECOV:
30:35	RWX	WOX_AND	WOX_OR	Reserved field.
36	RWX	WOX_AND	WOX_OR	CACHE_RD_CE_AND_UE: Cache read CE and UE popped within a short hang pulse. Could be a triple bit error.
37:39	RWX	WOX_AND	WOX_OR	Reserved field.
40	RWX	WOX_AND	WOX_OR	SCOM_ERR1: SCOM error.
41	RWX	WOX_AND	WOX_OR	SCOM_ERR2: SCOM error.
42:63	RO	RO	RO	constant = 0b0000000000000000000000

Register Name	**L2 FIR Mask Register**
Mnemonic	EX07.L2.L2MISC.L2CERRS.FIR_MASK_REG
Address	0000000013010C03 (SCOM) 0000000013010C04 (SCOM1) 0000000013010C05 (SCOM2)
Description	L2 FIR mask register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:41	RW	WO_AND	WO_OR	L2_FIR_MASK: L2 FIR mask register.
42:63	RO	RO	RO	constant = 0b0000000000000000000000

Register Name	**L2 FIR Action0 Register**
Mnemonic	EX07.L2.L2MISC.L2CERRS.FIR_ACTION0_REG
Address	0000000013010C06 (SCOM)
Description	L2 FIR action0 register

Bits	SCOM	Field Mnemonic: Description
0:41	RW	FIR_ACTION0: Action0 select for corresponding bit in FIR. (Action0,Action1) = Action select. (0,0) = Checkstop error. (0,1) = Recoverable error. (1,0) = Reserved. (1,1) = Local core checkstop.
42:63	RO	constant = 0b0000000000000000000000

Register Name	**L2 FIR Action1 Register**
Mnemonic	EX07.L2.L2MISC.L2CERRS.FIR_ACTION1_REG
Address	0000000013010C07 (SCOM)
Description	L2 FIR action1 register

Bits	SCOM	Field Mnemonic: Description
0:41	RW	FIR_ACTION1: Action1 select for corresponding bit in FIR. (Action0,Action1) = Action select. (0,0) = Checkstop error. (0,1) = Recoverable error. (1,0) = Reserved. (1,1) = Local core checkstop.
42:63	RO	constant = 0b0000000000000000000000

Register Name	**L2 Mode 0 Register**
Mnemonic	EX07.L2.L2MISC.L2CERRS.MODE_REG0
Address	0000000013010C0A (SCOM)
Description	L2 mode register 0

Bits	SCOM	Field Mnemonic: Description
0	RW	CFG_LRU_DIRECT_MAP: Enables direct mapped LRU mode.
1	RW	CFG_RANDOM_EN: Enables random LRU mode.
2	RW	CFG_SINGLE_MEM_EN: Enables only one member per congruence class to be used.
3:10	RW	CFG_SINGLE_MEM: One-hot member to use in single member mode.
11	RW	CFG_L3_DIS: Indicates that the L3 below the L2 is disabled.
12	RW	CFG_CO_SOFT_PURGE_ME_SX_EN: Enables CO soft purge on shared. All Me and Sx cache lines are dropped when they are cast out of the L2.

Bits	SCOM	Field Mnemonic: Description
13	RW	CFG_CO_SOFT_PURGE_ALL_LINES_EN: Enables CO soft purge on modified. All Mx and Tx cache lines are dropped when they are cast out of the L2. This mode is *only* intended for use at boot up where software ID destroys the boot-code preloaded into the L2 by flushing the L2. **Note:** While this bit is set, if ICSWs or Part64B lines are attempted, the COFSM will discard these operations.
14	RW	CFG_DCBZ_TRASHMODE_EN: Enable RC, for L2 trash mode, to treat 128-byte-marked stores or DCBZs such that RC will not go to the processor bus but instead pretend like it received a CRESP=go_m. **Software restriction:** ICSW and ICSWcr instructions should NOT be issued while in this mode (reproducible trash mode) since this will cause the COFSM to go to the processor bus. If trash is being run as non-reproducible (that is, PB active), then ICSW/ICSWcr can be sent and the COFSM will attempt them on the power bus.
15	RW	CFG_CAC_ERR_REPAIR_EN: Enable cache error repair. Enables RC and SN to trigger a purge action (of the line they are working on) if they detect a CE/UE/SUE on a cache read.
16	RW	CFG_LINEDEL_ON_CAC_UE_EN: Enable line delete on cache UE (or a software trig_det CE). L2 RC/SN, upon detecting a UE (or a software trig_det CE) on a cache read, will trigger a purge of the line and write the dir=Id. The Ioad will cause the L2 to never allocate into this physical location (that is, the L2 assumes these cache line cells are damaged). **Note:** If this bit is set to Disable, then software trig_det ce should not be activated. If software trig_det is activated, the RC will purge the line on CE, but the software trig_det ce masking will never reset since it is waiting for the RC to indicate it wrote an ID on behalf of the CE (which this bit prevented).
17	RW	CFG_HW_TRIG_LINEDEL_LDDISP_CE_EN: **Note:** This is for lab debug *only*. Enables line delete on detection of any RC dispatch of a load that is an L2 hit that results in a cache CE or UE (SUE will not trigger the line delete). Upon detecting a CE/UE on a cache read, will trigger a purge of the line and write the dir=Id. The Ioad will cause the L2 to never allocate into this physical location (that is, the L2 assumes these cache line cells are damaged). **Warning:** This aggressive line delete policy could cause soft CEs to quickly form a large number of line delete locations in the cache (that is, to the point where a CGC in the L2 has been completely line deleted away, causing a hang). This lab-only mode is intended for early-bring-up parts.
18:20	RWX	CFG_C0_L2_PB_ARB_RATE_SEL: Selects how fast the L2 requests to the PB.
21	RW	CFG_HASH_L3_ADDR_EN:
22	RW	CFG_RC_FRC_DISP_EQ_NTM_INIG_SI_TO_RCR_EN: Enables TM trash mode where IN or IG goes to L3 instead of PB.
23	RW	CFG_SYSMAP_SM_NOT_LG_SEL: Selects single chip groups.
24:31	RWX	CFG_Q_BIT_TID_MASK: QOS bits help PB and MC arbitrate.
32	RW	CFG_STQ_PF_EN: Enables store spawned prefetching.
33	RW	CFG_DCACHE_CAPP_LPC_MODE_EN: Enables store spawned prefetching.
34	RW	CFG_PERFMON_INFO_SRC_ED_SEL: Selects ED DCACHE information to include Sl interventions.
35:37	RWX	CFG_C1_L2_PB_ARB_RATE_SEL: Selects how fast the L2 requests to the PB.
38	RW	CFG_SKIP_GRP_SCOPE_EN: Forces RCs to skip group scope when upgrading from LN scope, used for chip = group PB settings.
39	RW	Reserved field.
40:63	RO	constant = 0b000000000000000000000000

Register Name	L2 Mode 1 Register
Mnemonic	EX07.L2.L2MISC.L2CERRS.MODE_REG1
Address	0000000013010C0B (SCOM)
Description	L2 mode register 1

Bits	SCOM	Field Mnemonic: Description
0	RW	CFG_ECCCK_CE_UE_SUE_ERR_DET_DIS: When set to 1, this field causes ECCCK CE, UE, SUE to all be gated off from being seen by RC/CO/SN and FIR logic (that is, RCDSP masks ECCCK signals). This bit is meant as a fail-safe mode. All errors will be ignored by RC/CO/SN. FIR bits will not get set. SUE data that is brought in or forms due to misses will *lose* is-SUE stamp on the next L2 load request LD(S) and load request LD(E) hit (that is, RC ignores all errors and assumes data should be used as is).
1	RW	CFG_ECCCK_UE_SUE_DET_DIS: When 1, causes ECCCK UE, SUE to all be gated off from being seen by RC/CO/SN and FIR logic (that is, RCDSP masks ECCCK signals. This bit should *not* be activated, as it can result in hang conditions if SUE/UE form when SUE/UE causes DERR to be sent to the core and RC ignores this and fails to resend data.
2:3	RW	Reserved field.
4:7	RW	HANG_POLL_PULSE_DIV: Hang pulse divider.
8:11	RW	DATA_POLL_PULSE_DIV: Data hang pulse divider.
12:15	RW	Reserved field.
16	RW	PM03_SMT_MODE_ROTATION_DIS: When 1, disables PERFMON thread information rotation.
17	RW	PM47_SMT_MODE_ROTATION_DIS: When 1, disables PERFMON thread information rotation.
18:19	RW	Reserved field.
20:22	RW	PM07_TID_ROTATE_PLSS_RATE: Time period the L2 will stay on a given thread before switching to the next thread.
23:24	RW	Reserved field.
25	RW	PM03_L23_EVENT_TID_SEL_EN: When 1, enables thread selection for PERFMON information.
26:27	RW	PM03_L23_EVENT_TID_SEL_NUM: Specifies the thread.
28	RO	constant = 0b0
29	RW	PM47_L23_EVENT_TID_SEL_EN: When 1, enables thread selection for PERFMON information.
30:31	RW	PM47_L23_EVENT_TID_SEL_NUM: Specifies the thread.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	Line Delete on Trigger Register
Mnemonic	EX07.L2.L2MISC.L2CERRS.LINEDEL_TRIG_REG
Address	0000000013010C0D (SCOM)
Description	L2 one shot line delete on next CE trigger register

Bits	SCOM	Field Mnemonic: Description
0	RW	LINEDEL_TRIG: When this register is written and triggers the L2 to do a line delete on the next RC load hit CE (or UE, if the CE migrated to an UE) it detects, only one RC should be triggered to do so if multiple dispatches occur with their own CE. Once this bit is set, the L2 must mask future settings of FIR Bit0 (l2rcdsp_fir_rccosn_cr_ce_err) until after the l2f2ctl_scom_ldel_on_cr_ce_or_ue_done field is set (that is, the CE line delete is purged). PRD firmware will go through the following sequence: 1) PRD detects FIR Bit0(l2rcdsp_fir_rccosn_cr_ce_err) for x times in a given time period. 2a) PRD triggers line delete on CE by setting LineDel_CE_Trig Reg(bit0). This *must* now gate future setting of FIR Bit0 (l2rcdsp_fir_rccosn_cr_ce_err) until hardware sets LineDel_CE_Trig Reg(bit1) in step 3. 2b) PRD writes FIR Bit0 (l2rcdsp_fir_rccosn_cr_ce_err) to 0. 3) Hardware watches for next CE (or UE since CE might have mutated to UE) to do a line delete on a CR of a CE/UE. Hardware will set LineDel_CE_Trig Reg(bit1). 4) Optional software step: PRD detects is LineDel_CE_Trig Reg(bit1) set and then writes LineDel_CE_Trig Reg (bit0:1) = 00 (that is, clears trigger and status). 5) Increments total number of line deletes installed in the L2 cache. If PRD:LineDelCntr > 6, then put this process in _guarded_ status. Else, PRD return to step 1 (to wait for next FIR bit0 setting).
1	RWX	LINEDEL_DONE: Line delete done status bit. Must be written back to 0 before the next line delete trigger.
2:3	RW	LINEDEL_SPARE: Spare bits.
4:63	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000

Register Name	PRD Purge Engine Command Register
Mnemonic	EX07.L2.L2MISC.L2CERRS.PRD_PURGE_CMD_REG
Address	0000000013010C0E (SCOM)
Description	PRD purge engine command register

Bits	SCOM	Field Mnemonic: Description
0	RW	PRD_PURGE_CMD_TRIGGER: When this register is written and this trigger bit is loaded with a 1, the purge engine mechanism starts. **Note:** The reg_busy must be 0 (that is, completion bit set) before the state of any of the purge_cmd register is changed.
1:4	RW	PRD_PURGE_CMD_TYPE: 0000 = L2 Cache_Flush. mem(0:2), addr(48:55), bank (ra56), must all be set to 0. 0010 = L2 Dir Line_Delete. mem(0:2), addr(48:55), bank (ra56), must be set to the directory entry being deleted. The RC will victimize entry and write directory to ID. 0011 = L2 Cache_mini_flush. mem(0:2) and bank must be set to 0. addr(48:55) can be set to any CGC. L2 will flush all eight members in the next 32 CGC.
5:8	RO	constant = 0b0000
9	RWX	PRD_PURGE_CMD_REG_BUSY: Command register is waiting to be serviced by the purge state machine.
10	ROX	PRD_PURGE_CMD_PRGSM_BUSY_ON_THIS: The purge machine has taken this register's command.
11	ROX	PRD_PURGE_CMD_PRGSM_BUSY: The purge machine is currently busy.
12:16	RO	constant = 0b00000
17:19	RW	PRD_PURGE_CMD_MEM: The member associated with L2 line delete commands. For an L2 Cache_Flush command, member(0:2) must be set to 0b000.
20:27	RW	PRD_PURGE_CMD_CGC: CGC address for L2 line delete commands. For an L2 cache flush command, cgc(0:7) must be set to 0x00.
28	RW	PRD_PURGE_CMD_BANK: Bank for L2 line delete commands. For an L2 cache flush command, bank must be set to 0.
29	RWX	PRD_PURGE_CMD_ERR: Attempted write to command register while cmd_reg_busy = 1, or illegal TTYPE.

Bits	SCOM	Field Mnemonic: Description
30:63	RO	constant = 0b0000000000000000000000000000000000

Register Name	PHYP Purge Engine Command Register
Mnemonic	EX07.L2.L2MISC.L2CERRS.PHYP_PURGE_CMD_REG
Address	0000000013010C0F (SCOM)
Description	Hypervisor purge engine command register

Bits	SCOM	Field Mnemonic: Description
0	RW	PHYP_PURGE_CMD_TRIGGER: When this register is written and this trigger bit is loaded with a 1, the purge engine mechanism to starts. **Note:** The reg_busy field must be 0 (that is, completion bit set) before the state of any of the purge_cmd register is changed.
1:4	RW	PHYP_PURGE_CMD_TYPE: 0000 = L2 Cache_Flush. mem(0:2), addr(48:55), bank (ra56), must all be set to 0. 0010 = L2 Dir Line_Delete. mem(0:2), addr(48:55), bank (ra56), must be set to the directory entry being deleted. The RC will victimize entry and write directory to ID. 0011 = L2 Cache_mini_flush. mem(0:2) and bank must be set to 0. addr(48:55) can be set to any CGC. L2 will flush all eight members in the next 32 CGC.
5:8	RO	constant = 0b0000
9	RWX	PHYP_PURGE_CMD_REG_BUSY: Command register is waiting to be serviced by purge state machine.
10	ROX	PHYP_PURGE_CMD_PRGSM_BUSY_ON_THIS: Purge machine has taken this register's command.
11	ROX	PHYP_PURGE_CMD_PRGSM_BUSY: Purge machine is currently busy.
12:16	RO	constant = 0b00000
17:19	RW	PHYP_PURGE_CMD_MEM: The member associated with L2 line delete commands. For an L2 cache flush command, member(0:2) must be set to 0b000.
20:27	RW	PHYP_PURGE_CMD_CGC: The CGC address for L2 line delete commands. For an L2 cache flush command, cgc(0:7) must be set to 0x00.
28	RW	PHYP_PURGE_CMD_BANK: Bank for L2 line delete commands. For an L2 cache flush command, bank must be set to 0.
29	RWX	PHYP_PURGE_CMD_ERR: Attempted to write cmd_reg while cmd_reg_busy = 1 or illegal TTYPE.
30:63	RO	constant = 0b0000000000000000000000000000000000

Register Name	Read Epsilon Register
Mnemonic	EX07.L2.L2MISC.L2CERRS.RD_EPS_REG
Address	0000000013010C10 (SCOM)
Description	Read Epsilon register

Bits	SCOM	Field Mnemonic: Description
0:11	RW	TIER0_RD_EPS_VALUE: tier0 read Epsilon.
12:23	RW	TIER1_RD_EPS_VALUE: tier1 read Epsilon.
24:35	RW	TIER2_RD_EPS_VALUE: tier2 read Epsilon.
36:63	RO	constant = 0b0000000000000000000000000000

Register Name	Write Epsilon Register
Mnemonic	EX07.L2.L2MISC.L2CERRS.WR_EPS_REG
Address	0000000013010C11 (SCOM)
Description	Write Epsilon register

Bits	SCOM	Field Mnemonic: Description
0:11	RW	TIER1_WR_EPS_VALUE: Write Epsilon.
12:23	RW	TIER2_WR_EPS_VALUE: Write Epsilon.
24:27	RW	EPS_DIVIDER_MODE: Epsilon count divider 0 => 16, non-zero => itself.
28	RW	EPS_MODE_SEL: Sets how long each CRESP case should wait.
29	RW	EPS_CNT_USE_L2_DIVIDER_EN: Use L2 clocks instead of PB step.
30:33	RW	L2_EPS_STEP_MODE: L2 Epsilon step count, only if eps_cnt_use_l2_divider_en = 1.
34:63	RO	constant = 0b000000000000000000000000000000

Register Name	Error Report 0 Register
Mnemonic	EX07.L2.L2MISC.L2CERRS.ERR_RPT0
Address	0000000013010C12 (SCOM)
Description	Error report register 0

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	FIR14_NCCTL_RLD_BARRIER_ERR: Error report hold.
2	ROX	FIR14_NCCTL_SNP_ERR: Error report hold.
3	ROX	FIR14_NCCTL_TLBIE_ACK_ERR: Error report hold.
4	ROX	FIR14_NCCTL_SYNC_ERR: Error report hold.
5	ROX	FIR14_NCCTL_VSYNC_ERR: Error report hold.
6	ROX	FIR14_TMCTL_TIDX_TEND_LDST_SEQ_ERR: Error report hold.
7	ROX	FIR14_RVCTL_ERR: Error report hold.
8	ROX	FIR14_SRCTL0_BAD_HPC_ERR: Error report hold.
9	ROX	FIR14_SRCTL1_BAD_HPC_ERR: Error report hold.
10	ROX	FIR14_SRCTL2_BAD_HPC_ERR: Error report hold.
11	ROX	FIR14_SRCTL3_BAD_HPC_ERR: Error report hold.
12	ROX	FIR14_PBARB_FSM_REQ_OVERFLOW_ERR: Error report hold.
13	ROX	FIR14_PBARB_TRASHMODE_PB_REQ_ERR: Error report hold.
14	ROX	FIR14_L3PF_MACH_DONE_ERR: Error report hold.
15	ROX	FIR14_RCMD0_TTAG_PERR: Error report hold.
16	ROX	FIR14_RCMD1_TTAG_PERR: Error report hold.
17	ROX	FIR14_RCMD2_TTAG_PERR: Error report hold.
18	ROX	FIR14_RCMD3_TTAG_PERR: Error report hold.
19	ROX	FIR14_CR0_TTAG_PERR: Error report hold.

Bits	SCOM	Field Mnemonic: Description
20	ROX	FIR14_CR0_ATAG_PERR: Error report hold.
21	ROX	FIR14_CR1_TTAG_PERR: Error report hold.
22	ROX	FIR14_CR1_ATAG_PERR: Error report hold.
23	ROX	FIR14_CR2_TTAG_PERR: Error report hold.
24	ROX	FIR14_CR2_ATAG_PERR: Error report hold.
25	ROX	FIR14_CR3_TTAG_PERR: Error report hold.
26	ROX	FIR14_CR3_ATAG_PERR: Error report hold.
27	ROX	FIR14_RCMD0_ADDR_PERR: Error report hold.
28	ROX	FIR14_RCMD1_ADDR_PERR: Error report hold.
29	ROX	FIR14_RCMD2_ADDR_PERR: Error report hold.
30	ROX	FIR14_RCMD3_ADDR_PERR: Error report hold.
31	ROX	FIR9_PEC_PHASE3_TIMEOUT: Error report hold.
32	ROX	FIR9_PEC_PHASE4_SAME_ERR: Error report hold.
33	ROX	FIR9_PEC_PHASE4_RCCO_DISP_FAIL: Error report hold.
34	ROX	FIR9_PEC_PHASE5_TIMEOUT: Error report hold.
35	ROX	FIR14_B01_BOTH_ACTIVE: Error report hold.
36	ROX	FIR14_PHANTOM_B01_REQ: Error report hold.
37	ROX	FIR14_RC_UNEXP_F2_DATA_ERR: Error report hold.
38	ROX	FIR14_RC_UNEXP_PURG_HIT_ERR: Error report hold.
39	ROX	FIR14_RCX_UNEXP_IDLE_PBL3_DATA_ERR: Error report hold.
40	ROX	FIR14_RCX_UNEXP_IDLE_PB_CRESP_ERR: Error report hold.
41	ROX	FIR14_COX_UNEXP_IDLE_PB_CRESP_ERR: Error report hold.
42:63	RO	constant = 0b0000000000000000000000

Register Name	Error Report 1 Register
Mnemonic	EX07.L2.L2MISC.L2CERRS.ERR_RPT1
Address	0000000013010C13 (SCOM)
Description	Error report register 1

Bits	SCOM	Field Mnemonic: Description
0	ROX	FIR14_RCX_UNEXP_IDLE_L3_CRESP_ERR: Error report hold.
1	ROX	FIR14_RCX_UNEXP_IDLE_L3_DWDONE_ERR: Error report hold.
2	ROX	FIR14_RCX_UNEXP_PB_RC_DTAG_PCHK_ERR: Error report hold.
3	ROX	FIR14_DW_SET_REF_WITH_FLAG_IDLE_ERR: Error report hold.
4	ROX	FIR14_KILL_REF_WITH_FLAG_IDLE_ERR: Error report hold.
5	ROX	Reserved field.
6	ROX	FIR14_DW_SET_SI_BY_MACH: Error report hold.
7	ROX	FIR14_PD_DIR_MULT_HIT: Error report hold.
8	ROX	FIR14_B0_SD_DIR_MULT_HIT: Error report hold.

Bits	SCOM	Field Mnemonic: Description
9	ROX	FIR14_B1_SD_DIR_MULT_HIT: Error report hold.
10	ROX	FIR14_B2_SD_DIR_MULT_HIT: Error report hold.
11	ROX	FIR14_B3_SD_DIR_MULT_HIT: Error report hold.
12	ROX	FIR14_INVALID_SNP_CPS_STATU_RTN: Error report hold.
13	ROX	FIR14_HANG_WAITING_FOR_FP_MATE: Error report hold.
14	ROX	FIR14_BAD_FP_MATE: Error report hold.
15	ROX	FIR14_LSU_TAG_REUSE_ERR: Error report hold.
16	ROX	FIR14_IFU_MULT_REQ_ERR: Error report hold.
17	ROX	FIR14_XPF_MULT_REQ_ERR: Error report hold.
18	ROX	FIR14_XLT_QUEUE_OVRFLW_ERR: Error report hold.
19	ROX	FIR14_L3PF_REQ_ERR: Error report hold.
20	ROX	FIR14_NCU_TID_DONE_ERR: Error report hold.
21	ROX	FIR11_LRU_MEM_INVALID_ABCD: Error report hold.
22	ROX	FIR11_LRU_MEM_INVALID_EFGH: Error report hold.
23	ROX	FIR14_STQ_COMING_ERR: Error report hold.
24	ROX	FIR14_STQ_OVERFLOW_ERR: Error report hold.
25	ROX	FIR14_RC_PBBUS_SFSTAT_ERR: Error report hold.
26	ROX	FIR14_TMA_LARXA_VS_FRCMISS_SV_ERR: Error report hold.
27	ROX	FIR37_RC_TGT_NODAL_REQ_CRESP_DINC_ERR: Error report hold.
28	ROX	FIR37_SN_TGT_NODAL_REQ_CRESP_DINC_ERR: Error report hold.
29	ROX	FIR14_RC_UNEXP_DIRSTAT_VS_DSECT_CHK_ERR: Error report hold.
30:63	RO	constant = 0b0000000000000000000000000000000000

Register Name	NCU FIR Register
Mnemonic	EX07.NC.NCMISC.NCSCOMS.FIR_REG
Address	0000000013011400 (SCOM) 0000000013011401 (SCOM1) 0000000013011402 (SCOM2)
Description	NCU FIR Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	CONTROL_ERR: Hardware control error.
1	RWX	WOX_AND	WOX_OR	TLBIE_CONTROL_ERR: TLBIE control error.
2	RWX	WOX_AND	WOX_OR	TLBIE_SLBIEG_SW_ERR: TLBIE or SLBIEG received illegal fields from core.
3	RWX	WOX_AND	WOX_OR	ST_ADDR_ERR: Store address machine or TLBIE/sync machine received addr_err CRESP.
4	RWX	WOX_AND	WOX_OR	LD_ADDR_ERR: Load address machine received addr_err CRESP.
5	RWX	WOX_AND	WOX_OR	ST_ACK_DEAD: Store received ack_dead.
6	RWX	WOX_AND	WOX_OR	LD_ACK_DEAD: Load received ack_dead.
7	RWX	WOX_AND	WOX_OR	MSG_ADDR_ERR: MSGSND received addr_err.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
8	RWX	WOX_AND	WOX_OR	STQ_DATA_PARITY_ERR: Store data parity error from register file detected.
9	RWX	WOX_AND	WOX_OR	STORE_TIMEOUT: Store timed out on PB.
10	RWX	WOX_AND	WOX_OR	TLBIE_MASTER_TIMEOUT: TLBIE master timed out on PB.
11	RWX	WOX_AND	WOX_OR	TLBIE_SNOOP_TIMEOUT: TLBIE snooper timed out waiting for core.
12	RWX	WOX_AND	WOX_OR	IMA_CRESP_ADDR_ERR: IMA received addr_err CRESP.
13	RWX	WOX_AND	WOX_OR	IMA_ACK_DEAD: IMA received ack_dead.
14	RWX	WOX_AND	WOX_OR	PMISC_CRESP_ADDR_ERR: PMISC received address error CRESP.
15	RWX	WOX_AND	WOX_OR	PPE_RD_CRESP_ADDR_ERR: PPE read CRESP address error.
16	RWX	WOX_AND	WOX_OR	PPE_WR_CRESP_ADDR_ERR: PPE write CRESP address error.
17	RWX	WOX_AND	WOX_OR	PPE_RD_ACK_DEAD: PPE read received ack_dead.
18	RWX	WOX_AND	WOX_OR	PPE_WR_ACK_DEAD: PPE write received ack_dead.
19	RWX	WOX_AND	WOX_OR	TGT_NODAL_DINC_ERR: PPE write received ack_dead.
20	RWX	WOX_AND	WOX_OR	DARN_EN_ERR: Darn TTYPE while darn not enabled.
21	RWX	WOX_AND	WOX_OR	DARN_ADDR_ERR: Darn TTYPE while darn not enabled.
22:28	RWX	WOX_AND	WOX_OR	SPARE_FIR: Spare FIR bits.
29	RWX	WOX_AND	WOX_OR	SCOM_ERR1: SCOM error.
30	RWX	WOX_AND	WOX_OR	SCOM_ERR2: SCOM error.
31:63	RO	RO	RO	constant = 0b000000000000000000000000000000000

Register Name	NCU FIR Mask Register
Mnemonic	EX07.NC.NCMISC.NCSCOMS.FIR_MASK_REG
Address	0000000013011403 (SCOM) 0000000013011404 (SCOM1) 0000000013011405 (SCOM2)
Description	NCU FIR mask register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:30	RW	WO_AND	WO_OR	FIR_MASK: FIR mask.
31:63	RO	RO	RO	constant = 0b000000000000000000000000000000000

Register Name	NCU FIR Action0 Register
Mnemonic	EX07.NC.NCMISC.NCSCOMS.FIR_ACTION0_REG
Address	0000000013011406 (SCOM)
Description	NCU FIR action0 register

Bits	SCOM	Field Mnemonic: Description
0:30	RW	FIR_ACTION0: Action0 select for corresponding bit in FIR. (Action0,Action1) = Action select. (0,0) = Checkstop error. (0,1) = Recoverable error. (1,0) = Reserved. (1,1) = Local core checkstop.
31:63	RO	constant = 0b000000000000000000000000000000000

Register Name	NCU FIR Action1 Register
Mnemonic	EX07.NC.NCMISC.NCSCOMS.FIR_ACTION1_REG
Address	0000000013011407 (SCOM)
Description	NCU FIR action1 register

Bits	SCOM	Field Mnemonic: Description
0:30	RW	FIR_ACTION1: Action1 select for corresponding bit in FIR. (Action0,Action1) = Action select. (0,0) = Checkstop error. (0,1) = Recoverable error. (1,0) = Reserved. (1,1) = Local core checkstop.
31:63	RO	constant = 0b000000000000000000000000000000000

Register Name	NCU Mode Register
Mnemonic	EX07.NC.NCMISC.NCSCOMS.NCU_MODE_REG
Address	000000001301140A (SCOM)
Description	NCU mode register

Bits	SCOM	Field Mnemonic: Description
0:1	RW	HTM_QUEUE_LIMIT: Determines how many HTM address tenures can be active at one time.
2	RW	TRASH_MODE_EN: Enables trash mode where the processor bus is disabled so the NCU will send TLBIE and PTESYNCS through the PB bypass logic.
3	RW	FENCE_TLBIE: SCOM TLBIE fence.
4:6	RW	DROP_PRIORITY_MASK: When to increase the drop priority after a rty_drp CRESP.
7	RW	TLBI_GROUP_PUMP_EN: Group pump TLBIE.
8	RW	SLBI_GROUP_PUMP_EN: Group pump SLBIEG.
9	RW	SYSMAP_SM_NOT_LG_SEL: Select small system map.
10	RW	TLBIE_PACING_CNT_EN: Enables TLBIE pacing logic.
11:18	RW	TLBIE_DEC_RATE: Snoop counter decrement rate.
19:26	RW	TLBIE_INC_RATE: Snoop counter increment rate.
27:34	RW	TLBIE_CNT_THRESH: Threshold at which to respond to tlbi_chk and tlbi_op1.
35	RW	TLBIE_CNT_WT4TX_CORE_EN: Allows TLBIEs waiting on previous TLBIEs to also count.
36:43	RW	TLB_CHK_WAIT_DEC: Wait tlbi_chk wait counter decrement rate.
44:63	RO	constant = 0b00000000000000000000

Register Name	NCU Mode 2 Register
Mnemonic	EX07.NC.NCMISC.NCSCOMS.NCU_MODE_REG2
Address	000000001301140B (SCOM)
Description	NCU mode register

Bits	SCOM	Field Mnemonic: Description
0:3	RW	HANG_POLL_PULSE_DIV: Hang pulse divider.
4:7	RW	MASTER_CP_DATA_POLL_PULSE_DIV: Store/load master data hang divider.
8:17	RW	TLB_SNOOP_DATA_POLL_PULSE_DIV: TLBIE Snooper data hang divider.
18:21	RW	TLB_STG1_HANG_POLL_PULSE_DIV: TLB master stg1 hang pulse divider.
22:25	RW	TLB_STG2_HANG_POLL_PULSE_DIV: TLB master stg2 hang pulse divider.
26:35	RW	MASTER_TLB_DATA_POLL_PULSE_DIV: TLBIE master data hang divider bits 0:9.
36:63	RO	constant = 0b0000000000000000000000000000

Register Name	NCU Mode 3 Register
Mnemonic	EX07.NC.NCMISC.NCSCOMS.NCU_MODE_REG3
Address	000000001301140C (SCOM)
Description	NCU mode register

Bits	SCOM	Field Mnemonic: Description
0	RW	TLBIE_STALL_EN: Enables NCU stalling the core if NCUs are overflowing with TLBIES.
1:3	RW	TLBIE_STALL_THRESHOLD: The number of TLBIEs pending that are needed before the NCU will start the stall count. Min is 1, Max is 7.
4:7	RW	TLBIE_STALL_CMPLT_CNT: The number of TLBIEs (from 1 to 8) to be completed before NCU stops stalling the core.
8:15	RW	TLBIE_STALL_DELAY_CNT: The number of cycles that will wait while over threshold before actually stalling the core. This count is in increments of 128 cycles, up to 32K.
16:63	RO	constant = 0b000000000000000000000000000000000000000000000000

Register Name	NCU Flush And Error Injection Register
Mnemonic	EX07.NC.NCMISC.NCSCOMS.INJ_REG
Address	000000001301140D (SCOM)
Description	NCU flush and error injection register

Bits	SCOM	Field Mnemonic: Description
0:1	RW	STQ_ERR_INJ: STQ error injection into STQ register file.
2:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	NCU Error Report Register
Mnemonic	EX07.NC.NCMISC.NCSCOMS.ERR_RPT_REG
Address	000000001301140E (SCOM)
Description	NCU error report register

Bits	SCOM	Field Mnemonic: Description
0	ROX	FIR0_OVERFLOW_ERR: Error report hold.
1	ROX	FIR0_ILLEGAL_STORE_SIZE: Error report hold.
2	ROX	FIR0_LD_AMO_SEQ_ERR: Error report hold.
3	ROX	FIR0_CR0_TTAG_PERR: Error report hold.
4	ROX	FIR0_CR0_ATAG_PERR: Error report hold.
5	ROX	FIR0_CR1_TTAG_PERR: Error report hold.
6	ROX	FIR0_CR1_ATAG_PERR: Error report hold.
7	ROX	FIR0_CR2_TTAG_PERR: Error report hold.
8	ROX	FIR0_CR2_ATAG_PERR: Error report hold.
9	ROX	FIR0_CR3_TTAG_PERR: Error report hold.
10	ROX	FIR0_CR3_ATAG_PERR: Error report hold.
11	ROX	FIR0_SNP0_ADDR_PERR: Error report hold.
12	ROX	FIR0_SNP0_TTAG_PERR: Error report hold.
13	ROX	FIR0_SNP1_ADDR_PERR: Error report hold.
14	ROX	FIR0_SNP1_TTAG_PERR: Error report hold.
15	ROX	FIR0_PBARB_TRASHMODE_ERR: Error report hold.
16	ROX	FIR1_TLBIE_BAD_OP_ERR: Error report hold.
17	ROX	FIR1_MASTER_SEQ_ID_PAR_ERR: Error report hold.
18	ROX	FIR1_SNOOP_TLBIE_SEQ_PARITY_ERR: Error report hold.
19	ROX	FIR0_PURGE_LVL_ERR1: Purge level falling before purge_done_lvl rise.
20	ROX	FIR0_PURGE_LVL_ERR2: Purge level rising before purge_done_lvl fall.
21	ROX	FIR0_PURGE_ABORT_LVL_ERR1: Purge_abort_lvl rising when purge_lvl = 0.
22	ROX	FIR0_PURGE_ABORT_LVL_ERR2: Purge_abort_lvl falling when purge_done_lvl = 1.
23	ROX	FIR0_PURGE_DONE_LVL_ERR1: Purge_done_lvl falling and purge_lvl or purge_abort_lvl = 1.
24	ROX	FIR0_IMA_FSM_TIMEOUT: IMA machine timeout.
25	ROX	FIR0_PPE_WR_FSM_TIMEOUT: IMA machine timeout.
26	ROX	FIR0_PPE_RD_FSM_TIMEOUT: IMA machine timeout.
27	ROX	FIR0_TLB_DATA_PAR_ERR: Data parity error on TLBIE/SLBIE request.
28	ROX	FIR19_LD_TGT_NODAL_DINC_ERR: CI-load targeted pump got rty_inc CRESP.
29	ROX	FIR19_ST_TGT_NODAL_DINC_ERR: CI-store targeted pump got rty_inc CRESP.
30:63	RO	constant = 0b0000000000000000000000000000000000

Register Name	NCU Mode Register
Mnemonic	EX07.NC.NCMISC.NCSCOMS.NCU_STATUS_REG
Address	000000001301140F (SCOM)
Description	NCU mode register

Bits	SCOM	Field Mnemonic: Description
0	ROX	NCU_CORE0_REQ_ACTIVE: NCU is busy on core0 requests (loads/stores).
1	ROX	NCU_CORE1_REQ_ACTIVE: NCU is busy on core1 requests (loads/stores).
2	ROX	NCU_CORE_OR_SNP_REQ_ACTIVE: NCU is busy on core requests and snoops (loads/stores/snooped TLBIEs/SLBIEGs).
3	ROX	NCU_ANY_REQ_ACTIVE: NCU is busy on anything, including IMA/PPE/HTM.
4:63	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000

Register Name	NCU Special BAR Register
Mnemonic	EX07.NC.NCMISC.NCSCOMS.NCU_SPEC_BAR_REG
Address	0000000013011410 (SCOM)
Description	Load BAR register

Bits	SCOM	Field Mnemonic: Description
0	RW	SPEC_BAR_EN: Enables NCU node pump only special CI-store/CI-load operations.
1	RW	SPEC_BAR_256K: Enables 256 KB size bar for special CI-store/CI-load operations.
2:7	RO	constant = 0b000000
8:49	RW	SPEC_BAR_ADDR: 16 KB BAR address of the special CI operations.
50:63	RO	constant = 0b00000000000000

Register Name	NCU Darn BAR Register
Mnemonic	EX07.NC.NCMISC.NCSCOMS.NCU_DARN_BAR_REG
Address	0000000013011411 (SCOM)
Description	NCU darn BAR register

Bits	SCOM	Field Mnemonic: Description
0	RW	DARN_BAR_EN: Enables NCU RNG BAR register.
1:7	RO	constant = 0b0000000
8:51	RW	DARN_BAR_ADDR: 4 KB BAR address of the darn CI operations.
52:63	RO	constant = 0b000000000000

Register Name	NCU Mode 0 Register
Mnemonic	EX07.NC.NCMISC.NCSCOMS.NCU_SLOW_LPAR_REG0
Address	0000000013011412 (SCOM)
Description	NCU mode register

Bits	SCOM	Field Mnemonic: Description
0	RWX	DELAY8_LPAR_VALID: LPARID is valid.
1:12	ROX	DELAY8_LPAR_ID: LPARID.
13	RWX	DELAY7_LPAR_VALID: LPARID is valid.
14:25	ROX	DELAY7_LPAR_ID: LPARID.
26	RWX	DELAY6_LPAR_VALID: LPARID is valid.
27:38	ROX	DELAY6_LPAR_ID: LPARID.
39	RWX	DELAY5_LPAR_VALID: LPARID is valid.
40:51	ROX	DELAY5_LPAR_ID: LPARID.
52:63	RO	constant = 0b000000000000

Register Name	NCU Mode 1 Register
Mnemonic	EX07.NC.NCMISC.NCSCOMS.NCU_SLOW_LPAR_REG1
Address	0000000013011413 (SCOM)
Description	NCU mode register

Bits	SCOM	Field Mnemonic: Description
0	RWX	DELAY4_LPAR_VALID: LPARID is valid.
1:12	ROX	DELAY4_LPAR_ID: LPARID.
13	RWX	DELAY3_LPAR_VALID: LPARID is valid.
14:25	ROX	DELAY3_LPAR_ID: LPARID.
26	RWX	DELAY2_LPAR_VALID: LPARID is valid.
27:38	ROX	DELAY2_LPAR_ID: LPARID.
39	RWX	DELAY1_LPAR_VALID: LPARID is valid.
40:51	ROX	DELAY1_LPAR_ID: LPARID.
52:63	RO	constant = 0b000000000000

Register Name	L3 FIR Register
Mnemonic	EX07.L3.L3_MISC.L3CERRS.FIR_REG
Address	0000000013011C00 (SCOM) 0000000013011C01 (SCOM1) 0000000013011C02 (SCOM2)
Description	L3 FIR Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	L3_RDDSP_SEGR_LCO_ALL_MEM_UNAVAIL_ERR: When this error occurs, no members are available for a particular CGC. This causes an infinite hang of a CI machine. There may be no members available due to a combination of line delete, column delete, eDRAM bank fail, and SEGR LCO mode.
1	RWX	WOX_AND	WOX_OR	L3_FIR_SPARE1: spare1.
2	RWX	WOX_AND	WOX_OR	L3_FIR_SPARE2: spare2.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
3	RWX	WOX_AND	WOX_OR	L3_DRAM_POS_WORDLINE_FAIL: This error indicates at least one CE and one UE have occurred within one fabric data hang pulse interval. This is an indication that a word line fail may be occurring.
4	RWX	WOX_AND	WOX_OR	L3_CAC_RD_CE_DET_NOT_LINDEL_REQ: CE detected on L3 cache read that is not a line delete request.
5	RWX	WOX_AND	WOX_OR	L3_CAC_RD_UE_DET: UE detected on L3 cache read.
6	RWX	WOX_AND	WOX_OR	L3_CAC_RD_SUE_DET: SUE detected on L3 cache read.
7	RWX	WOX_AND	WOX_OR	L3_CAC_WR_DATA_CE_FROM_PB: CE detected on processor bus write data for prefetch, LCO, or cache inject.
8	RWX	WOX_AND	WOX_OR	L3_CAC_WR_DATA_UE_FROM_PB: UE detected on processor bus write data for prefetch, LCO, or cache inject.
9	RWX	WOX_AND	WOX_OR	L3_CAC_WR_DATA_SUE_FROM_PB: SUE detected on processor bus write data for prefetch, LCO, or cache inject.
10	RWX	WOX_AND	WOX_OR	L3_CAC_WR_DATA_CE_FROM_L2: CE detected on write data from L2 CPI buffer.
11	RWX	WOX_AND	WOX_OR	L3_CAC_WR_DATA_UE_FROM_L2: UE detected on write data from L2 CPI buffer.
12	RWX	WOX_AND	WOX_OR	L3_CAC_WR_DATA_SUE_FROM_L2_OR_WIHPC: SUE detected on write data from L2 CPI buffer or WIHPC (on an L3HPC PWI).
13	RWX	WOX_AND	WOX_OR	L3_DIR_RD_CE_DET: Directory CE occurred.
14	RWX	WOX_AND	WOX_OR	L3_DIR_RD_UE_DET: Directory UE occurred.
15	RWX	WOX_AND	WOX_OR	L3_DIR_RD_PHANTOM_ERROR: Directory error occurred but not found during correction sequence.
16	RWX	WOX_AND	WOX_OR	L3_PB_MAST_WR_ADDR_ERR: Received addr_error CRESP on snoop machine or castout operation.
17	RWX	WOX_AND	WOX_OR	L3_PB_MAST_RD_ADDR_ERR: Received addr_error CRESP for prefetch operation.
18	RWX	WOX_AND	WOX_OR	L3_ADDR_HANG_DETECTED: Some L3 machine hung waiting for combined response or FLINK hang.
19	RWX	WOX_AND	WOX_OR	L3_LRU_INVAL_CNT: LRU invalid count error. Violation of requirement that, when not in DMAP or fixed-member mode, each group must have a member with lru_cnt = 0 for first class and a member with lru_cnt = 0 for second class if there is a second class member.
20	RWX	WOX_AND	WOX_OR	L3_PPE_RD_CE_DET: PPE CE occurred.
21	RWX	WOX_AND	WOX_OR	L3_PPE_RD_UE_DET: PPE UE occurred.
22	RWX	WOX_AND	WOX_OR	L3_PPE_RD_SUE_DET: PPE SUE occurred.
23	RWX	WOX_AND	WOX_OR	L3_MACH_HANG_DETECTED: Prefetch or write inject machine processor bus data hang check.
24	RWX	WOX_AND	WOX_OR	L3_HW_CONTROL_ERR: Hardware control error. See the Hardware Control Error Read0/1 SCOM Registers for details.
25	RWX	WOX_AND	WOX_OR	L3_SNP_CACHE_INHIBIT_ERR: Cache inhibited operation was hit in the L3 directory. This is usually a software bug.
26	RWX	WOX_AND	WOX_OR	L3_LINE_DEL_CE_DONE: Snoop machine or read machine has performed a line delete.
27	RWX	WOX_AND	WOX_OR	L3_DRAM_ERROR: DRAM command collision error.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
28	RWX	WOX_AND	WOX_OR	L3_LRU_ERROR: LRU array parity error. Parity is checked whenever the LRU array is read. The hardware automatically recovers from this error. On an RD request or snoop, the array is read, but parity errors are not corrected (no LRU array write). Thus, repeated read to the location with the parity error may cause this bit to repeated assert.
29	RWX	WOX_AND	WOX_OR	L3_ALL_MEMBERS_DELETED_ERROR: All members are either column or line deleted in some CGC class.
30	RWX	WOX_AND	WOX_OR	L3_REFRESH_TIMER_ERROR: Refresh timer pulse either was not configured to run properly or has stopped.
31	RWX	WOX_AND	WOX_OR	L3_PB_MAST_WR_ACK_DEAD: Received ack_dead or ed_ack_dead CRESP on CO, SN operation (PB write).
32	RWX	WOX_AND	WOX_OR	L3_PB_MAST_RD_ACK_DEAD: Received ack_dead or ed_ack_dead CRESP on PF operation (PB read).
33	RWX	WOX_AND	WOX_OR	SCOM_ERR1: SCOM error FIR 1.
34	RWX	WOX_AND	WOX_OR	SCOM_ERR2: SCOM error FIR 2.
35:63	RO	RO	RO	constant = 0b00000000000000000000000000000

Register Name	L3 FIR Mask Register
Mnemonic	EX07.L3.L3_MISC.L3CERRS.FIR_MASK_REG
Address	0000000013011C03 (SCOM) 0000000013011C04 (SCOM1) 0000000013011C05 (SCOM2)
Description	L3 FIR mask register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	Reserved field.
1	RW	WO_AND	WO_OR	Reserved field.
2	RW	WO_AND	WO_OR	Reserved field.
3	RW	WO_AND	WO_OR	Reserved field.
4	RW	WO_AND	WO_OR	Reserved field.
5	RW	WO_AND	WO_OR	Reserved field.
6	RW	WO_AND	WO_OR	Reserved field.
7	RW	WO_AND	WO_OR	Reserved field.
8	RW	WO_AND	WO_OR	Reserved field.
9	RW	WO_AND	WO_OR	Reserved field.
10	RW	WO_AND	WO_OR	Reserved field.
11	RW	WO_AND	WO_OR	Reserved field.
12	RW	WO_AND	WO_OR	Reserved field.
13	RW	WO_AND	WO_OR	Reserved field.
14	RW	WO_AND	WO_OR	Reserved field.
15	RW	WO_AND	WO_OR	Reserved field.
16	RW	WO_AND	WO_OR	Reserved field.
17	RW	WO_AND	WO_OR	Reserved field.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
18	RW	WO_AND	WO_OR	Reserved field.
19	RW	WO_AND	WO_OR	Reserved field.
20	RW	WO_AND	WO_OR	Reserved field.
21	RW	WO_AND	WO_OR	Reserved field.
22	RW	WO_AND	WO_OR	Reserved field.
23	RW	WO_AND	WO_OR	Reserved field.
24	RW	WO_AND	WO_OR	Reserved field.
25	RW	WO_AND	WO_OR	Reserved field.
26	RW	WO_AND	WO_OR	Reserved field.
27	RW	WO_AND	WO_OR	Reserved field.
28	RW	WO_AND	WO_OR	Reserved field.
29	RW	WO_AND	WO_OR	Reserved field.
30	RW	WO_AND	WO_OR	Reserved field.
31	RW	WO_AND	WO_OR	Reserved field.
32	RW	WO_AND	WO_OR	Reserved field.
33	RW	WO_AND	WO_OR	Reserved field.
34	RW	WO_AND	WO_OR	Reserved field.
35:63	RO	RO	RO	constant = 0b00000000000000000000000000000

Register Name	L3 FIR Action 0 Register
Mnemonic	EX07.L3.L3_MISC.L3CERRS.FIR_ACTION0_REG
Address	0000000013011C06 (SCOM)
Description	L3 FIR action0 register

Bits	SCOM	Field Mnemonic: Description
0:30	RW	FIR_ACTION0: Action0 select for corresponding bit in FIR. (Action0,Action1) = Action select. (0,0) = Checkstop error. (0,1) = Recoverable error. (1,0) = Reserved. (1,1) = Local core checkstop.
31:61	RO	constant = 0b0000000000000000000000000000000

Register Name	L3 FIR Action 1 Register
Mnemonic	EX07.L3.L3_MISC.L3CERRS.FIR_ACTION1_REG
Address	0000000013011C07 (SCOM)
Description	L3 FIR action1 register

Bits	SCOM	Field Mnemonic: Description
0:30	RW	FIR_ACTION1: Action1 select for corresponding bit in FIR. (Action0,Action1) = Action select. (0,0) = Checkstop error. (0,1) = Recoverable error. (1,0) = Reserved. (1,1) = Local core checkstop.
31:61	RO	constant = 0b0000000000000000000000000000000

Register Name	L3 Mode 1 Register
Mnemonic	EX07.L3.L3_MISC.L3CERRS.MODE_REG1
Address	0000000013011C0A (SCOM)
Description	L3 mode register 1

Bits	SCOM	Field Mnemonic: Description
0	RW	L3_LCO_ENABLE_CFG: When on, enables L3.1 lateral cast outs. If set, the user *must* configure group, ID, and victim fields in this register. Also, when modifying any of the target IDs or victim bits while the machine is running, you must SCOM-write this bit off, and then write it back on along with the other updates. A leading edge detect of 0 to 1 causes the logic to sample the other bits.
1	RW	L3_LCO_TARGET_GROUP: Set the target group/chip for this chiplet.
2:5	RW	L3_LCO_TARGET_ID: Set the target ID for this chiplet.
6:21	RW	L3_LCO_TARGET_VICTIMS: Set the allowable target victims for this chiplet. **Notes:** 1. If no targets are enabled in this register, l3_lco_enable_cfg should be set to zero. 2. If only one target is enabled (self does not count) in this register, the dial l3_lco_hash_mask_home_tgts_dis field should be turned on.
22	RW	L3_SCOM_CINJ_LCO_DIS: When on, disables acceptance of cache injects and LCOs. This field is only for back-up purposes.
23:62	RO	constant = 0b0000000000000000000000000000000000000000

Register Name	L3 eDRAM Bank Soft Disable Register
Mnemonic	EX07.L3.L3_MISC.L3CERRS.EDRAM_BANK_SOFT_DIS
Address	0000000013011C0B (SCOM)
Description	L3 eDRAM bank soft disable

Bits	SCOM	Field Mnemonic: Description
0:9	RW	L3_EDRAM_BANK_SOFT_DIS_CFG: eDRAM banks can be soft disabled using this register. eDRAM banks that are disabled in this way are refreshed and can be read, but are never written. Specifically, eDRAM banks that are disabled with this register, but not disabled with the eDRAM macro internal disable SLAT, are still refreshed and readable, though they are never selected for a cache line insertion. 0 = Bank is not disabled. 1 = Bank is disabled.
10:21	RO	constant = 0b000000000000

Register Name	L3 eDRAM and Charge Pump Register
Mnemonic	EX07.L3.L3_MISC.L3CERRS.EDRAM_REG
Address	0000000013011C0C (SCOM)
Description	L3 eDRAM and charge pump register

Bits	SCOM	Field Mnemonic: Description
0	RW	L3_CP_UTIL_EN_DC: When on, enables charge pump monitoring.
1:2	RW	L3_CP_UTIL_SEL_DC: Selects the internal reference source for charge pump monitoring.
3	RW	L3_EDRAM_REG_SPARE3: Spare.
4:6	RW	L3_CP_UTIL_EXT_SEL: Selects which charge pump to monitor. Values 0 to 5 are valid (there are six charge pumps).
7:12	RWX	L3_UTIL_MON_BITS: Charge pump monitor bits.
13:63	RO	constant = 0b000000000000000000000000000000000000000000000000000

Register Name	L3 Error Inject Register
Mnemonic	EX07.L3.L3_MISC.L3CERRS.ERR_INJ_REG
Address	0000000013011C0D (SCOM)
Description	L3 error inject register

Bits	SCOM	Field Mnemonic: Description
0	RWX_WOR	L3_SINGLE_CAC_ERR_INJ: When on, injects a single error into the cache. Cleared by hardware when injection has occurred.
1	RW	L3_SOLID_CAC_ERR_INJ: When on, injects a solid error into the cache.
2:3	RW	L3_CAC_ERR_INJ_TYPE: Define cache error inject type.
4	RWX_WOR	L3_SINGLE_DIR_ERR_INJ: When on, injects a single error into the directory. Cleared by hardware when injection has occurred.
5	RW	L3_SOLID_DIR_ERR_INJ: When on, injects a solid error into the directory unless the l3_rand_dir_err_enable bit is set, in which case the errors will be random about 25% of the time.
6	RW	L3_DIR_ERR_INJ_TYPE: Define directory error inject type. 0 = CE. 1 = UE. **Note:** This bit should not be altered while l3_single_dir_err_inj is set. If this restriction is not followed, it is unpredictable if a CE or UE will be injected.
7	RWX_WOR	L3_SINGLE_LRU_ERR_INJ: When on, injects a single error (parity) into the LRU array. Cleared by hardware when injection has occurred.
8	RW	L3_SOLID_LRU_ERR_INJ: When on, injects a solid error (parity) into the LRU array.
9:45	RO	constant = 0b0000000000000000000000000000000000000

Register Name	L3 PRD Purge Register
Mnemonic	EX07.L3.L3_MISC.L3CERRS.PRD_PURGE_REG
Address	0000000013011C0E (SCOM)
Description	L3 PRD Purge Register

Bits	SCOM	Field Mnemonic: Description
0	RWX_WOR	L3_PRD_PURGE_REQ: When set, will initiate a purge of the type specified by the TTYPE field beginning at the address specified in the address field. This bit will remain set until the purge is completed.
1:4	RW	L3_PRD_PURGE_TTYPE: This field specifies which kind of operation is to be done: full purge, single line purge, single line delete, full blind purge, or dynamic purge. **Note:** Dynamic purge is similar to a full purge, except that it starts without waiting for work pending in the L3 to complete. It is only used for lab stress purposes, as it increases the probability of a purge encountering a collision. Outside of the lab environment, software does not use dynamic purge and waits for internally pending transactions to complete before a purge runs.
5	RWX_WOR	L3_PRD_LINE_DEL_ON_NEXT_CE: When set, will cause RD and snoop machines to delete the line on the next occurrence of a CE. This bit will be reset by hardware when the line delete is done.
6	RW	L3_PRD_LINE_DEL_ON_ALL_CE: When set, will cause RD and snoop machines to delete the line on every occurrence of a CE.
7:8	RW	Reserved field.
9	ROX	L3_PRD_PURGE_BUSY_ERR: When set, indicates that a purge was requested when this register was still busy from a previous purge request. The request that caused this bit to be set will be dropped.
10:11	RW	Reserved field.
12:16	RW	L3_PRD_PURGE_MEMBER: Specifies the member for a purge. 0 - 19 = Members 0 to 19. 20 - 31 = Reserved. This field is used only for single line delete/purge. Full, blind, and dynamic always purge all 20 members of the cache.
17:28	RW	L3_PRD_PURGE_DIR_ADDR: Specifies the congruence class to begin the purge.
29:63	RO	constant = 0b00000000000000000000000000000000000

Register Name	**L3 Refresh Timer Control Register**
Mnemonic	EX07.L3.L3_CARB.L3CACTL.DRAM_REF_REG
Address	0000000013011C0F (SCOM)
Description	L3 refresh timer control register and init DRAM

Bits	SCOM	Field Mnemonic: Description
0:3	RW	L3_REF_TIMER_DIVIDE_MAJOR: Major divide value. In conjunction with minor divide value, controls the division of the refresh timer pulse before it is sent to eDRAMs. Refresh period (must be $\leq$ 40 μs) = period_of(tc_l3_edram_refresh) $\times$ (1 + major) $\times$ (10 + minor) $\times$ 524.
4	RWX	L3_SCOM_INIT_DRAM: When set will cause an initialization of the eDRAM. Cleared by the L3 when eDRAM is ready (eDRAM initialization is complete).
5	RW	L3_SCOM_QUIESCE_CACHE: When set will cause the cache arbiter to quiesce system commands to the cache. This is a SCOM-based backup to the tc_cc_l3_quiesce_lvl pin.
6	RW	L3_SCOM_QUIESCE_CACHE_LFSR: When set will cause the cache arbiter to quiesce system commands to the cache based off of an LFSR, toggling on and off every 2k or 1k cycles. This is for stress testing.
7	RWX	L3_SCOM_QUIESCE_REFRESH: When set will put the L3 into a refresh quiesced state. This must occur before reference clock domain is clock-stopped to ensure stop is not in the middle of a refresh. Refresh will begin again when a dram_init command is received from OHA.
8:11	RW	L3_REF_TIMER_DIVIDE_MINOR: Minor divide value. In conjunction with the major divide value, controls the division of the refresh timer pulse before it is sent to eDRAMs. Refresh period (must be $\leq$ 40 μs) = period_of(tc_l3_edram_refresh) $\times$ (1 + major) $\times$ (10 + minor) $\times$ 524.
12:23	RO	constant = 0b000000000000

Register Name	L3 Error Report 0 Register
Mnemonic	EX07.L3.L3_MISC.L3CERRS.L3_ERR_RPT0_REG
Address	0000000013011C10 (SCOM)
Description	L3 error report register 0

Bits	SCOM	Field Mnemonic: Description
0	RO	L3SDRTL0_BAD_HPC_ERR: l3sdrtl0_bad_hpc_err.
1	RO	L3SDRTL1_BAD_HPC_ERR: l3sdrtl1_bad_hpc_err.
2	RO	L3CORTR_NO_LCO_TGTS_ERR: l3cortr_no_lco_tgts_err.
3	RO	SN0_RCMD_TTAG_P_ERR: sn0 rcmd_ttag_p_err.
4	RO	SN1_RCMD_TTAG_P_ERR: sn1 rcmd_ttag_p_err.
5	RO	SN0_RCMD_ADDR_P_ERR: sn0 rcmd_addr_p_err.
6	RO	SN1_RCMD_ADDR_P_ERR: sn1 rcmd_addr_p_err.
7	RO	SN0_CRESP_TTAG_P_ERR: sn0 cresp_ttag_p_err.
8	RO	SN1_CRESP_TTAG_P_ERR: sn1 cresp_ttag_p_err.
9	RO	SN0_CRESP_ATAG_P_ERR: sn0 cresp_atag_p_err.
10	RO	SN1_CRESP_ATAG_P_ERR: sn1 cresp_atag_p_err.
11	RO	DATA_RTAG_P_ERR: Two conditions cause this field to assert. 1. An RTAG parity error occurred. 2. The system is in cache-contained mode and a SN/PF/CO is pending on the fabric.
12	RO	PF_UNSOLICITED_CRESP_ERR: pf_unsolicited_cresp_err.
13	RO	SN_UNSOLICITED_CRESP_ERR: sn_unsolicited_cresp_err.
14	RO	CO_UNSOLICITED_CRESP_ERR: co_unsolicited_cresp_err.
15	RO	SPARE_ERR_RPT0_15: spare_err_rpt0_15.
16	RO	SPARE_ERR_RPT0_16: spare_err_rpt0_16.
17	RO	SPARE_ERR_RPT0_17: spare_err_rpt0_17.
18	RO	WI_UNSOLICITED_DATA_ERR: wi_unsolicited_data_err.
19	RO	PF_UNSOLICITED_DATA_ERR: pf_unsolicited_data_err.
20:23	RO	TM_CAM_ERR: tm_cam_err.
24	RO	COFSM_ADDR_ERR: cofsm_addr_err.
25	RO	SNFSM_ADDR_ERR: snfsm_addr_err.
26	RO	L3SDRTL0_CACHE_INHIBIT_ERR: l3sdrtl0_cache_inhibit_err.
27	RO	L3SDRTL1_CACHE_INHIBIT_ERR: l3sdrtl1_cache_inhibit_err.
28	RO	L3SDRTL2_CACHE_INHIBIT_ERR: l3sdrtl2_cache_inhibit_err.
29	RO	L3SDRTL3_CACHE_INHIBIT_ERR: l3sdrtl3_cache_inhibit_err.
30	RO	L3SDRTL2_BAD_HPC_ERR: l3sdrtl2_bad_hpc_err.
31	RO	L3SDRTL3_BAD_HPC_ERR: l3sdrtl3_bad_hpc_err.
32	RO	SN_MACHINE_HANG_ERR: sn_machine_hang_err.
33	RO	RD_MACHINE_HANG_ERR: rd_machine_hang_err.
34	RO	CI_MACHINE_HANG_ERR: ci_machine_hang_err.
35	RO	CO_MACHINE_HANG_ERR: co_machine_hang_err.

Register Name	L3 LRU Segregated LCO Mode Configuration Register
Mnemonic	EX07.L3.L3_MISC.L3CERRS.LRU_VIC_ALLOC_REG
Address	0000000013011C11 (SCOM)
Description	L3 LRU segregated LCO mode configuration register

Bits	SCOM	Field Mnemonic: Description
0:19	RW	L3_COLUMN_SEGR_LCO_COLUMN_L2_CFG: Each bit corresponds to a directory member. This register is only used if l3_column_alloc_md_cfg = segregated_lco_mode. If set, that member can only be used for lines inserted by way of L2 cast-outs or L3 prefetch. If cleared, that member can only be used for lines inserted by way of incoming LCOs. When in segregated_lco_mode, there must be at least one enabled member per group (group A = members 0 to 9, group B = members 10 to 19) designated for L2 cast-out/L3 prefetch and one enabled member per group designated for incoming LCOs. Software must take into account any disabled eDRAM bank members and set this register appropriately. If no member is available for an operation, then the CI machine will hang in an infinite loop, continually failing dispatch and a FIR is set (dial: l3_all_members_deleted_error).
20:21	RW	L3_COLUMN_ALLOC_MD_CFG: When in normal mode, members can be used for either L2 cast-outs or incoming LCOs. When in segregated_lco_mode, the value of l3_segr_lco_column_l2_cfg determines which members can be used for L2 cast-outs versus incoming LCOs.
22:55	RO	constant = 0b0000000000000000000000000000000000

Register Name	L3 RTIM Pulse Period Monitor Register
Mnemonic	EX07.L3.L3_MISC.L3CERRS.L3_RTIM_PERIOD_MONITOR
Address	0000000013011C12 (SCOM)
Description	Indicates the period of the RTIM pulse from pervasive

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	L3_RTIM_PERIOD_MON: Indicates the number of cycles between the refresh timer pulse from pervasive. POR is 10 when running at 3.7 GHz, for example.
8:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	L3 PM Purge Register
Mnemonic	EX07.L3.L3_MISC.L3CERRS.PM_PURGE_REG
Address	0000000013011C13 (SCOM)
Description	L3 PM purge register

Bits	SCOM	Field Mnemonic: Description
0	RWX_WOR	L3_PM_PURGE_REQ: When set, initiates a purge. This bit will remain set until the purge is completed (or successfully aborted).
1	ROX	L3_PM_PURGE_BUSY_ERR: When set, indicates that a purge was requested after another PM purge had already been requested (and not yet completed). The second request (the one that caused this bit to be set) will be dropped. Once set, this bit will not reset until another purge request comes in (that is, setting (0) again).
2	RWX_WOR	L3_PM_PURGE_ABORT: When set, a purge is aborted. This bit will clear once the PM purge has been successfully aborted. When the abort is successfully complete, it will also cause (0) to clear. This bit will only set when there is a valid purge to abort (that is, it will not remain set if there was no PM purge to abort in the first place.

Bits	SCOM	Field Mnemonic: Description
3:5	RO	constant = 0b000

Register Name	L3 PHYP Purge Register
Mnemonic	EX07.L3.L3_MISC.L3CERRS.PHYP_PURGE_REG
Address	0000000013011C14 (SCOM)
Description	L3 PHYP purge register

Bits	SCOM	Field Mnemonic: Description
0	RWX_WOR	L3_PHYP_PURGE_REQ: When set, initiates a purge of the type specified by the TTYPE field beginning at the address specified in the address field. This bit will remain set until the purge is completed.
1:4	RW	L3_PHYP_PURGE_TTYPE: This field specifies which kind of operation is to be done: full purge, single line purge, single line delete, full blind purge, or dynamic purge. **Note:** Dynamic purge is similar to a full purge, except that it starts without waiting for work pending in the L3 to complete. It is only used for lab stress purposes, as it increases the probability of a purge encountering a collision. Outside of the lab environment, software does not use dynamic purge and waits for internally pending transactions to complete before a purge runs.
5	RWX_WOR	L3_PHYP_LINE_DEL_ON_NEXT_CE: When set, will cause RD and snoop machines to delete the line on the next occurrence of a CE. This bit will be reset by hardware when the line delete is done.
6	RW	L3_PHYP_LINE_DEL_ON_ALL_CE: When set, will cause RD and snoop machines to delete the line on every occurrence of a CE.
7:8	RW	Reserved field.
9	ROX	L3_PHYP_PURGE_BUSY_ERR: When set, indicates that a purge was requested when this register was still busy from a previous purge request. The request that caused this bit to be set will be dropped.
10:11	RW	Reserved field.
12:16	RW	L3_PHYP_PURGE_MEMBER: Specifies the member for a purge. 0 - 19 = Members 0 to 19. 20 - 31 = Reserved. This field is used only for single line delete/purge. Full, blind, and dynamic always purge all 20 members of the cache.
17:28	RW	L3_PHYP_PURGE_DIR_ADDR: Specifies the congruence class to begin the purge.
29:63	RO	constant = 0b00000000000000000000000000000000000

Register Name	L3 Line Deleted Members Count Register
Mnemonic	EX07.L3.L3_MISC.L3CERRS.LINE_DELETED_MEMBERS_REG
Address	0000000013011C15 (SCOM)
Description	L3 line deleted members count register

Bits	SCOM	Field Mnemonic: Description
0:4	RWX	L3_LINE_DELETED_MEMBERS: L3 line deleted member count. This register monitors the number of deleted members in any access congruence class. It can be cleared, and will simply continue monitoring.
5:60	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	L3 PM Fence LCO Register
Mnemonic	EX07.L3.L3_MISC.L3CERRS.PM_LCO_DIS_REG
Address	0000000013011C16 (SCOM)
Description	L3 PM fence LCO register

Bits	SCOM	Field Mnemonic: Description
0	RW	L3_PM_LCO_DIS_CFG: When set, L3 will not accept incoming LCO transactions. This is enabled before a purge to ensure that the purge results in a completely empty cache.

Register Name	L3 Error Report 1 Register
Mnemonic	EX07.L3.L3_MISC.L3CERRS.L3_ERR_RPT1_REG
Address	0000000013011C17 (SCOM)
Description	L3 error report register 1

Bits	SCOM	Field Mnemonic: Description
0	RO	PF_MACHINE_HANG_ERR: pf_machine_hang_err.
1	RO	WI_MACHINE_HANG_ERR: wi_machine_hang_err.
2	RO	L3L2CTL_RD_OVERRUN_CK_ERR: l3l2ctl_rd_overrun_ck_err.
3	RO	L3L2CTL_PF_OVERRUN_CK_ERR: l3l2ctl_pf_overrun_ck_err.
4	RO	L3CICTL_CI_OVERRUN_CK_ERR: l3l2ctl_ci_overrun_ck_err.
5	RO	L3XMEMA0_DW_DIR_HIT_ERR: l3xmema0_dw_dir_hit_err.
6	RO	L3XMEMA1_DW_DIR_HIT_ERR: l3xmema1_dw_dir_hit_err.
7	RO	L3XMEMA0_CRW_DIR_HIT_ERR: l3xmema0_crw_dir_hit_err.
8	RO	L3XMEMA1_CRW_DIR_HIT_ERR: l3xmema1_crw_dir_hit_err.
9	RO	PBEXCA0_CMD_REQ_ERR0: pbexca0_cmd_req_err0.
10	RO	PBEXCA0_CMD_REQ_ERR1: pbexca0_cmd_req_err1.
11	RO	PBEXCA0_CMD_REQ_ERR2: pbexca0_cmd_req_err2.
12	RO	PBEXCA1_CMD_REQ_ERR0: pbexca1_cmd_req_err0.
13	RO	PBEXCA1_CMD_REQ_ERR1: pbexca1_cmd_req_err1.
14	RO	PBEXCA1_CMD_REQ_ERR2: pbexca1_cmd_req_err2.
15	RO	MC_FP_MATE_CMD_ERR0: mc_fp_mate_cmd_err0.
16	RO	MC_FP_MATE_CMD_ERR1: mc_fp_mate_cmd_err1.
17	RO	L3PBEXCA0_OVERFLOW_ERR: l3pbexca0_overflow_err.
18	RO	L3PBEXCA1_OVERFLOW_ERR: l3pbexca1_overflow_err.
19	RO	L3PBEXCA0_UNDERFLOW_ERR: l3pbexca0_underflow_err.
20	RO	L3PBEXCA1_UNDERFLOW_ERR: l3pbexca1_underflow_err.
21	RO	PF_MACHINE_W4DT_HANG_ERR: pf_machine_w4dt_hang_err.
22	RO	WI_MACHINE_W4DT_HANG_ERR: wi_machine_w4dt_hang_err.
23	RO	CO_CRESP_ACK_DEAD_ERR: co_cresp_ack_dead_err.
24	RO	SN_CRESP_ACK_DEAD_ERR: sn_cresp_ack_dead_err.
25	RO	SN2_RCMD_TTAG_P_ERR: sn2 rcmd_ttag_p_err.

Bits	SCOM	Field Mnemonic: Description
26	RO	SN3_RCMD_TTAG_P_ERR: sn3 rcmd_ttag_p_err.
27	RO	SN2_RCMD_ADDR_P_ERR: sn2 rcmd_addr_p_err.
28	RO	SN3_RCMD_ADDR_P_ERR: sn3 rcmd_addr_p_err.
29	RO	SN2_CRESP_TTAG_P_ERR: sn2 cresp_ttag_p_err.
30	RO	SN3_CRESP_TTAG_P_ERR: sn3 cresp_ttag_p_err.
31	RO	SN2_CRESP_ATAG_P_ERR: sn2 cresp_atag_p_err.
32	RO	SN3_CRESP_ATAG_P_ERR: sn3 cresp_atag_p_err.

Register Name	Disable L2 RCMD Register
Mnemonic	EX07.L3.L3_MISC.L3CERRS.PM_L2_RCMD_DIS_REG
Address	0000000013011C18 (SCOM)
Description	Disable L2 RCMD register

Bits	SCOM	Field Mnemonic: Description
0	RW	L3_PM_L2_RCMD_DIS_CFG: When set, snoops from the fabric (RCMD) are not forwarded to the L2. This is asserted before the L2 is stop-clocked (but after L2 is idle) to ensure L2 is not stopped in the middle of a snoop.

Register Name	L3 eDRAM RD Error Status 0 Register
Mnemonic	EX07.L3.L3_MISC.L3CERRS.ED_RD_ERR_STAT_REG0
Address	0000000013011C19 (SCOM)
Description	L3 eDRAM RD error status register 0

Bits	SCOM	Field Mnemonic: Description
0	RWX_WAND	L3_ED_RD_ERR_STAT_VAL: When set, indicates that the syndrome, DW, RA, and bank have been captured for an eDRAM CE, UE, or SUE.
1	ROX	L3_ED_RD_ERR_STAT_1ST_BEAT_UE: Indicates the first beat had a UE. This is redundant since it can be determined from the syndrome, but it is useful for debugging.
2	ROX	L3_ED_RD_ERR_STAT_2ND_BEAT_UE: Indicates the second beat had a UE. This redundant since it can be determined from the syndrome, but it is useful for debugging.
3	ROX	L3_ED_RD_ERR_STAT_SPARE3: Spare bit 3.
4:11	ROX	L3_ED_RD_ERR_STAT_1ST_BEAT_SYNDROME: Captures the syndrome of the first beat when a CE, UE, or SUE occurs.
12:19	ROX	L3_ED_RD_ERR_STAT_2ND_BEAT_SYNDROME: Captures the syndrome of the second beat when a CE, UE, or SUE occurs.
20:22	ROX	L3_ED_RD_ERR_STAT_DW: Indicates which DW when a CE, UE, or SUE occurred. Will be the same DW captured over both beats.
23:47	RO	constant = 0b0000000000000000000000000

Register Name	L3 eDRAM RD Error Status 1 Register
Mnemonic	EX07.L3.L3_MISC.L3CERRS.ED_RD_ERR_STAT_REG1
Address	0000000013011C1A (SCOM)
Description	L3 eDRAM RD error status register 1

Bits	SCOM	Field Mnemonic: Description
0:13	ROX	L3_ED_RD_ERR_STAT_RA: Captures the RA when a CE, UE, or SUE occurred.
14:17	ROX	L3_ED_RD_ERR_STAT_BANK: Captures which eDRAM bank when a CE, UE, or SUE occurred.
18:38	RO	constant = 0b000000000000000000000

Register Name	L3 eDRAM Bank Fail SCOM Read Register
Mnemonic	EX07.L3.L3_MISC.L3CERRS.EDRAM_BANK_FAIL_SCOM_RD
Address	0000000013011C1B (SCOM)
Description	L3 eDRAM bank fail

Bits	SCOM	Field Mnemonic: Description
0:2	ROX	L3_EDRAM_BANK_FAIL_SCOM_RD: The L3 includes a set of SLATs on the refresh repair scan ring called edram_bank_fail. These latches are set by ABIST to indicate the associated eDRAM banks that must be disabled. While ABIST must set these latches, disabling the associated eDRAM macros via their internal disable SLATs is optional and only affects power consumption. The L3 internally functionally disables eDRAM banks that are indicated as "off" via these edram_bank_fail SLATs. The edram_bank_fail SLATs can be read through SCOM using this register. 0x0 = All eDRAM banks are on; banks 0-9 are all good. 0x1 = eDRAM banks 0-1 are off; eDRAM banks 2-9 are on. 0x2 = eDRAM banks 2-3 are off; eDRAM banks 0-1 and 4-9 are on. 0x3 = eDRAM banks 4-5 are off; eDRAM banks 0-3 and 6-9 are on. 0x4 = eDRAM banks 6-7 are off; eDRAM banks 0-5 and 8-9 are on. 0x5 = eDRAM banks 8-9 are off; eDRAM banks 0-7 are on. This is the read-only version (delayed by one clock) of the value from the SLATs referred to above.

Register Name	L3 Read Epsilon Configuration Register
Mnemonic	EX07.L3.L3_MISC.L3CERRS.L3_RD_EPSILON_CFG_REG
Address	0000000013011C29 (SCOM)
Description	L3 read Epsilon configuration register

Bits	SCOM	Field Mnemonic: Description
0:11	RW	L3_WT4CR_RD_TIER0_EPS_VAL: Epsilon for extend protection after CRESP for triangle protection. Read Epsilon is used when providing intervention data. The tier0 value is used for local-node scope commands. 1 maps to a count of one clock, 2 maps to a count of two clocks, and so on, but 0 (and 0xFFF) maps to the maximum value of 4095.
12:23	RW	L3_WT4CR_RD_TIER1_EPS_VAL: Epsilon for extend protection after CRESP for triangle protection. Read Epsilon is used when providing intervention data. The tier1 value is used for near-node and group scope commands. 1 maps to a count of one clock, 2 maps to a count of two clocks, and so on, but 0 (and 0xFFF) maps to the maximum value of 4095.
24:35	RW	L3_WT4CR_RD_TIER2_EPS_VAL: Epsilon for extend protection after CRESP for triangle protection. Read Epsilon is used when providing intervention data. The tier2 value is used for remote-node and vectored-group scope commands. 1 maps to a count of one clock, 2 maps to a count of two clocks, and so on, but 0 (and 0xFFF) maps to the maximum value of 4095.

Bits	SCOM	Field Mnemonic: Description
36	RW	L3_RD_EPS_MODE_SEL_CFG: Controls tier selection for different command scope: mode1 = Use scope as tier selection. mode2 = Use largest tier (tier2) for all protection.
37:63	RO	constant = 0b000000000000000000000000000

Register Name	L3 Write and Read/Write Epsilon Configuration Register
Mnemonic	EX07.L3.L3_MISC.L3CERRS.L3_WR_EPSILON_CFG_REG
Address	0000000013011C2A (SCOM)
Description	L3 write and read/write Epsilon configuration register

Bits	SCOM	Field Mnemonic: Description
0:11	RW	L3_WT4CR_WR_TIER1_EPS_VAL: Epsilon for extend protection after CRESP for triangle protection. Write Epsilon is used for cast-out, snoop push, and LCO. LCO use is mode-able. The tier1 value is used for near-node and group scope commands. 1 maps to a count of one clock, 2 maps to a count of two clocks, and so on, but 0 (and 0xFFF) maps to the maximum value of 4095.
12:23	RW	L3_WT4CR_WR_TIER2_EPS_VAL: Epsilon for extend protection after CRESP for triangle protection. write eps is used for cast-out, snoop push and LCO. LCO use is mode-able. The tier2 value is used for remote-node and vectored-group scope commands. 1 maps to a count of one clock, 2 maps to a count of two clocks, and so on, but 0 (and 0xFFF) maps to the maximum value of 4095.
24	RW	L3_EN_WT4CR_WR_EPS_ON_LCO: Enable the use of write Epsilon for LCO commands. Default is to *not* use extended protection for LCOs.
25	RW	L3_EN_WT4CR_WR_EXTENDED_MODE: Write extended mode: 0 = Select Epsilon tier based on scope. This is the default value. 1 = Always use the largest tier for all scopes.
26:29	RW	L3_EPS_STEP_MODE: Divider of L3 clocks to produce *L3 step*, which is used when the Epsilon counter is based on internal L3 clock rather than the pb_xx_epsilon_step input (dial l3_eps_cnt_use_l3_divider_en = ON). Note that 'L3 stop' (if used) goes through the eps_divider (l3_eps_divider_mode). This field is used for both read and write Epsilons. The +1 effect is due to the counter resetting to 0 and running off the L3 clock. Range: 0x0 = Step once every 16 cycles. 0x1:0xf = Divide by encoded value + 1.
30:33	RW	L3_EPS_DIVIDER_MODE: Divide down the PB step/L3 step: 0x0 = Maximum division; divide by 16 (1/ 16). 0x1 - 0xF = Divide by the encoded value. This field is used for both read and write Epsilons.
34	RW	EPS_CNT_USE_L3_DIVIDER_EN: This field is used for both read and write Epsilons. 0 = Epsilon step based on pb_step_transition. 1 = Epsilon step based on L3 clock.
35:63	RO	constant = 0b00000000000000000000000000000

Register Name	L3 Mode 0 Register
Mnemonic	EX07.L3.L3_MISC.L3CERRS.MODE_REG0
Address	0000000013011C2B (SCOM)
Description	L3 mode register 0

Bits	SCOM	Field Mnemonic: Description
0	RW	L3_DISABLED_CFG: When on, disables this L3.

Bits	SCOM	Field Mnemonic: Description
1	RW	L3_DMAP_CI_EN_CFG: When on, puts L3 into direct map mode. This only affects cache-insertions. Note that enabling hashing (l3_addr_hash_en_cfg) and enabling direct-map-mode results in a CGC mapping that may be unexpected. This bit must only be changed when the cache is empty (reset-with-ABIST-clear or purged).
2	RW	L3_RDSN_LINEDEL_UE_EN: When on, enables RD and SN machines to line delete when they see cache read UEs. This needs to be set in IPL process.
3	RW	L3_NO_ALLOCATE_MODE_EN: When on, enables the L3 to enter a non-allocation mode after a UE occurs.
4	RWX	L3_NO_ALLOCATE_MODE_ACTIVE: When on, indicates that L3 is currently in non-allocation mode.
5	RW	L3_MODE_REG0_SPARE5: Spare.
6	RW	L3_MODE_REG0_SPARE6: Spare.
7	RW	L3_MODE_REG0_SPARE7: Spare.
8	RW	L3_LCO_RTY_LIMIT_DISABLE: When set, will never use an LCO retry limit count to change to CO_memory. Retried LCOs will always be retried as another LCO.
9	RW	L3_DYN_LCO_BLK_DIS_CFG: When on, disables the block on LCO related behaviors (allows LCOs to occur).
10	RW	L3_LCO_ADDR_TGT_ENABLE: When on, will enable a special LCO mode whereby all L3 cast-outs will be LCOed to a set of four L3.1s based on address bits 39:40. The intention of this mode is for wafer test or other bring-up situations where memory is not installed but a footprint larger than one L3 is desired. In this configuration, there would only be one core running and the entire address space would have to fit in the four L3.1s. The code or test would have to be loaded into the L3 by some means other than fetching from memory. The four L3.1s will effectively become memory. This mode overrides the l3_lco_enable_cfg dial setting. If more than one core is enabled in this mode, the L3 cannot be used as backing store for transactional memory. This mode does not work with cast-throughs; thus, if enabled, L2 must have cast-throughs disabled.
11	RW	L3_ADDR_HASH_EN_CFG: When on, will enable hashing of the L3 address, aa44:53 == aa34:43 XOR aa44:53. When this is used there is a corresponding dial in L2 that must be set: cfg_hash_l3_addr_en. Note that enabling hashing (here) and enabling direct-map-mode (l3_dmap_ci_en_cfg) results in a CGC mapping that may be unexpected.
12	RW	L3CERRS_CFG_DCACHE_CAPP_MODE: When on, enables DCACHE CAPP mode.
13	RW	L3CERRS_LCO_RETRY_THROTL_DIS: When on, disables the throttling of incoming LCOs via retries, based on the heuristic mechanism.
14:17	RW	L3_HANG_POLL_PULSE_DIV: Poll hang pulse divider.
18:21	RW	L3_DATA_POLL_PULSE_DIV: Data hang pulse divider.
22	RW	L3_SYSMAP_SM_NOT_LG_SEL: When off (the default), the large address map is supported. When on, the small address map is supported.
23:46	RO	constant = 0b000000000000000000000000

Register Name	CME_SCOM CME LFIR Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_LFIR
Address	0000000013012000 (SCOM) 0000000013012001 (SCOM1) 0000000013012002 (SCOM2)
Description	CME_SCOM CME LFIR

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_PPE_INTERNAL_ERROR: PPE asserted an internally detected error condition that caused it to halt. This indication is intended to be reported to both Core PPM macros to be forwarded to the OCC complex as an error interrupt.
1	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_PPE_EXTERNAL_ERROR: PPE detected an error condition on an external interface to the memory bolt-on that caused it to halt. This indication is intended to be reported to both core PPM macros to be forwarded to the OCC complex as an error interrupt.
2	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_PPE_PROGRESS_ERROR: PPE detected a lack of forward progress that caused it to halt. This indication is intended to be reported to both core PPM macros to be forwarded to the OCC complex as an error interrupt.
3	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_PPE_BREAKPOINT_ERROR: PPE halted either upon a hardware debug or software-requested breakpoint event. This indication is intended to be reported to both core PPM macros to be forwarded to the OCC complex as an error interrupt.
4	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_PPE_WATCHDOG: PPE asserted a watchdog timeout condition. Will likely be masked; for debug information only.
5	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_PPE_HALTED: PPE asserted a halt condition. Will likely be masked since there are several sources of halt that may be valid.
6	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_PPE_DEBUG_TRIGGER: PPE asserted a debug trigger.
7	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_SRAM_UE: SRAM uncorrectable error. CME will get a MCHK. Should be marked as as a recoverable error for run-time diagnostics reporting.
8	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_SRAM_CE: SRAM correctable error. CME received corrected data, but SRAM content is bad until the next scrub to that line. (Should be masked in the product; unmasked and marked as a recoverable error in manufacturing test.)
9	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_SRAM_SCRUB_ERR: Scrub timer tick occurred when scrub is still pending.
10	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_BCE_ERROR: Block copy engine error. BCE received an error from L3 or NCU. This also causes an interrupt to the CME, if it is running.
11	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_SPARE11: Implemented but not used. Inputs tied to 0.
12	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_SPARE12: Implemented but not used. Inputs tied to 0.
13	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_C0_IVRM_DROPOUT: Dropout was detected on core0 chiplet iVRM. Note that if IDCR[DROPOUT_NOTIFY_ENABLE] = 1, the unmasked value of this bit is ORed with the two subsequent dropout indication events and sent to the QPPM as a level signal.
14	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_C1_IVRM_DROPOUT: Dropout was detected on core1 chiplet iVRM.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
15	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_CACHE_IVRM_DROPOUT: Dropout was detected on cache chiplet iVRM.
16	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_EXTREME_DROOP_ERR: Extreme droop (as reported to the DPLL) over time exceeded the threshold in VCTR. Note that if VCCR[DROOP_NOTIFY_ENABLE] = 1, the unmasked value of this bit is ORed with the three subsequent droop indication events and sent to the QPPM as a level signal (ORed with the dropout indications above).
17	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_LARGE_DROOP_ERR: Large droop (as reported to the DPLL) over time exceeded the threshold in VCTR.
18	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_SMALL_DROOP_ERR: Small droop (as reported to the DPLL) over time exceeded the threshold in VCTR.
19	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_UNEXPECTED_DROOP_ENCODE: Detected non-thermometer code that should not be caused by metastability (that is, b'0001', b'0011', b'0010', or b'0111'). For debug and characterization only.
20	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_FIR_PARITY_ERR_DUP: Internal FIR parity error duplicate (same as fir_parity_err).
21	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_FIR_PARITY_ERR: Internal FIR parity error.
22:63	RO	RO	RO	constant = 0b000000000000000000000000000000000000000000

Register Name	CME_SCOM CME LFIR Mask Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_LFIRMASK
Address	0000000013012003 (SCOM) 0000000013012004 (SCOM1) 0000000013012005 (SCOM2)
Description	CME_SCOM CME LFIR Mask

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:21	RW	WO_AND	WO_OR	CME_SCOM_LFIRMASK_FIR_MASK: PPE asserted an error condition.
22:63	RO	RO	RO	constant = 0b000000000000000000000000000000000000000000

Register Name	CME_SCOM CME LFIR Action0 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_LFIRACT0
Address	0000000013012006 (SCOM)
Description	CME_SCOM CME LFIR Action0

Bits	SCOM	Field Mnemonic: Description
0:21	RW	CME_SCOM_LFIRACT0_FIR_ACTION0: MSB of action select for corresponding bit in FIR.
22:63	RO	constant = 0b000000000000000000000000000000000000000000

Register Name	CME_SCOM CME LFIR Action1 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_LFIRACT1
Address	0000000013012007 (SCOM)
Description	CME_SCOM CME LFIR Action1

Bits	SCOM	Field Mnemonic: Description
0:21	RW	CME_SCOM_LFIRACT1_FIR_ACTION1: LSB of action select for corresponding bit in FIR.
22:63	RO	constant = 0b000000000000000000000000000000000000000000

Register Name	PPE Local SRAM Control Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CMEARB.CSCR
Address	000000001301200A (SCOM) 000000001301200B (SCOM1) 000000001301200C (SCOM2)
Description	PPE local SRAM control register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_CLEAR	WO_OR	CSCR_SRAM_ACCESS_MODE: SRAM access mode.
1	RWX	WOX_CLEAR	WOX_OR	CSCR_SRAM_SCRUB_ENABLE: Enable background scrub (atomic read-write) to periodically check, and if needed, correct the data in the SRAM for bit flips due to alpha particles. This bit is cleared by the hardware when a UE is detected to assist with fault analysis.
2	RW	WO_CLEAR	WO_OR	CSCR_ECC_CORRECT_DIS: Do not correct the data coming out of the array on ECC detected correctable errors. This will cause CEs to report an error back to the PPE in addition to the usual UEs.
3	RW	WO_CLEAR	WO_OR	CSCR_ECC_DETECT_DIS: Do not flag an error back to PPE for ECC miscompares. Data from the SRAM is always treated as good. Note that errors are always detected and reported to the FIR and must be masked there independently from this bit.
4	RW	WO_CLEAR	WO_OR	CSCR_ECC_INJECT_TYPE: Used only when ECC_INJECT_ERR is set. When set to 1, causes an ECC error to be reported on every SRAM read. When set to 0, causes a single ECC error to be indicated on the next SRAM read to occur, since it also clears ECC_INJECT_ERR when that happens.
5	RWX	WOX_CLEAR	WOX_OR	CSCR_ECC_INJECT_ERR: When set, the hardware will inject or cause a dummy uncorrectable error (UE) to be reported to both the PPE and the FIR on all SRAM reads. The SRAM contents are not modified. Type of error to inject is determined by the previous bit. If ECC_INJECT_TYPE = 1, then this bit clears when the first error is injected. Note this bit can also be set by the PPE local register CFMSR.
6:7	RW	WO_CLEAR	WO_OR	CSCR_SPARE_6_7: Implemented but unused.
8:46	RO	RO	RO	constant = 0b000000000000000000000000000000000000000
47:59	RWX	WOX_CLEAR	WOX_OR	CSCR_SRAM_SCRUB_INDEX: 32 KB scrub index. This field is auto-incremented by hardware for every scrub operation. Upon a UE detection, this field is over-written with the index of the double-word containing the error. **Note:** SRAM_SCRUB_ENABLE should be set to 0 when writing this field to prevent one cycle window from ignoring this write if a scrub update happens to occur concurrently.
60:63	RO	RO	RO	constant = 0b0000

Register Name	**PPE Local SRAM Address Register**
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CMEARB.CSAR
Address	000000001301200D (SCOM)
Description	PPE local SRAM address register

Bits	SCOM	Field Mnemonic: Description
0:15	RO	constant = 0b0000000000000000
16:28	RW	CSAR_SRAM_ADDRESS: Address of an 8-byte SRAM entry in the 32 KB SRAM array.
29:63	RO	constant = 0b00000000000000000000000000000000000

Register Name	**PPE Local SRAM Data Register**
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CMEARB.CSDR
Address	000000001301200E (SCOM)
Description	PPE Local SRAM Data Register

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	CSDR_SRAM_DATA: 8-byte SRAM data entry for the address given by the SRAM_ADDRESS. Reads cause this register to be written with data from the local SRAM. Writes cause the local SRAM to be written with the contents of this register.

Register Name	**CME SCOM CME Local BCE Control and Status Register**
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_BCECSR
Address	000000001301200F (SCOM)
Description	CME_SCOM CME local BCE control and status register (BCECSR)

Bits	SCOM	Field Mnemonic: Description
0	ROX	CME_SCOM_BCECSR_BUSY: This field reads as '1' whenever the BCE is busy processing a transfer. This status bit is also routed to the CME external interrupt controller. It is an error to attempt to issue another start command to a busy BCE. This bit is cleared if an error occurs during the transaction.
1	RW_WCLEAR	CME_SCOM_BCECSR_ERROR: This bit is set if an error occurs during the transaction and locks this register until cleared, by writing this bit to a '1'. All of the other fields of this register are ignored on a write when this bit is set.
2:3	RO	constant = 0b00
4	RW	CME_SCOM_BCECSR_RNW: Read, not write. 0 = The transfer is a write from SRAM into main memory 1 = The transfer is a read from main memory into SRAM.
5	RW	CME_SCOM_BCECSR_BARSEL: Specifies which BCEBAR[n] to use for main memory addressing. 0 = Use BCEBAR[0]. 1 = Use BCEBAR[1]. **Note:** It is an error to issue a start command specifying a disabled or improperly initialized BAR (IPL host boot code requirement).
6	RW	CME_SCOM_BCECSR_PRIORITY: Specifies whether the transfer will be given priority on the processor bus over other units. Set only when block copy latency is important. 0 = Transfer will not have priority. 1 = Transfer will have priority. **Note:** Causes a trusted processor bus operation.

Bits	SCOM	Field Mnemonic: Description
7	RW	CME_SCOM_BCECSR_INJECT_ERR: when on, causes the BCE to report a false error on the last block copy transaction.
8:12	RO	constant = 0b00000
13:15	RW	CME_SCOM_BCECSR_TYPE: Specifies the access mode (processor bus TTYPE) for writes from SRAM into main memory: 0 = Default mode (standard 8-byte coherent partial-DMA write). 1 = Atomic ADD. 2 = Atomic AND. 3 = Atomic OR. 4 = Atomic XOR. 5:7 = Illegal. This field is ignored for reads, but must specify a valid value for write transfers.
16	RO	constant = 0b0
17:27	RW	CME_SCOM_BCECSR_NUM_BLOCKS: The number of 8-byte blocks to transfer for writes, or the number of 32-byte blocks to transfer for reads. This field is decremented after each block is successfully transferred. While busy, this indicates which block is currently being copied and will always be 0 after a successfully completed transfer. After a stop or error, this can be read to determine how many blocks have not yet been successfully copied. **Note:** Using a value of 0 will complete instantly and not transfer any data (for testing code). Using a value greater than 0x400 is not advised because it will cause the BCE to transfer some blocks twice, potentially overwriting data.
28:39	RW	CME_SCOM_BCECSR_SBASE: Written with the SRAM block index of the first block of the transfer when the transfer is initiated, this field will be seen to increment (and possibly wrap) during the transfer. The SRAM address associated with SBASE is 0xFFFF8000 + ((SBASE × size) % 32KB) where size is 32 bytes for reads and 8 bytes for writes. When BUSY clears without an ERROR, (that is, on a STOP or when the block copy completes), this index points to the block after the one successfully written.
40:41	RO	constant = 0b00
42:63	RW	CME_SCOM_BCECSR_MBASE: Written with the main memory block index of the first block of the transfer when the transfer is initiated, this field will be seen to increment (and possibly wrap) during the transfer. The main memory address associated with MBASE is pbase + ((MBASE × size) % extent) where pbase is the processor bus base address implied by the BCEBAR[n] register selected for the transfer, size is 32 bytes for reads and 8 bytes for writes, and extent is the BCEBAR[n] aperture size.

Register Name	**PPE External Interface XCR Register**
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CMEPPE.PPE.PPE_XIXCR
Address	0000000013012010 (SCOM)
Description	PPE External Interface XCR

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:3	WOX	PPE_XIXCR_XCR: PPE external control register CMD command: 000 = Clear debug status. 001 = Halt. 010 = Resume. 011 = Single-step. 100 = Toggle XSR[TRH]. 101 = Soft reset. 110 = Hard reset. 111 = Force halt.
4:63	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000

Register Name	PPE External Interface RAMRA Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CMEPPE.PPE.PPE_XIRAMRA
Address	0000000013012011 (SCOM)
Description	PPE external interface RAMRA

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:3	WOX	PPE_XIXCR_XCR: PPE external control register CMD command: 000 = Clear debug status. 001 = Halt. 010 = Resume. 011 = Single-step. 100 = Toggle XSR[TRH]. 101 = Soft reset. 110 = Hard reset. 111 = Force halt.
4:31	RO	constant = 0b0000000000000000000000000000
32:63	WOX	PPE_XIRAMRA_SPRG0: SPRG0 register value, by convention, is used by PPE code to keep status. SPRG0 is a 32-bit scratch register. SPRG0 can only be written as an XIR when the processor is halted (XSR[HS] = '1').

Register Name	PPE External Interface RAMGA Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CMEPPE.PPE.PPE_XIRAMGA
Address	0000000013012012 (SCOM)
Description	PPE External Interface RAMGA

Bits	SCOM	Field Mnemonic: Description
0:31	WOX	PPE_XIRAMGA_IR: PPE instruction register. Writes cause a RAM operation. It can only be written when the processor is halted (XSR[HS] = '1'). Provides the requested PPE instruction to execute.
32:63	WOX	PPE_XIRAMRA_SPRG0: SPRG0 register value, by convention, is used by PPE code to keep status. SPRG0 is a 32-bit scratch register. SPRG0 can only be written as an XIR when the processor is halted (XSR[HS] = '1').

Register Name	PPE External Interface RAMDBG Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CMEPPE.PPE.PPE_XIRAMDBG
Address	0000000013012013 (SCOM)
Description	PPE external interface RAMDBG

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1:3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.
7	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
8	ROX	Reserved field.
9:11	ROX	NULL_MSR_SIBRC:
12	ROX	Reserved field.
13	ROX	Reserved field.
14	ROX	NULL_MSR_WE:
15	ROX	Reserved field.
16:19	ROX	Reserved field.
20	ROX	NULL_MSR_LP:
21	ROX	Reserved field.
22:23	RO	constant = 0b00
24	ROX	Reserved field.
25	ROX	Reserved field.
26:27	RO	constant = 0b00
28	ROX	Reserved field.
29:31	ROX	Reserved field.
32:63	RWX	PPE_XIRAMRA_SPRG0: SPRG0 register value, by convention, is used by PPE code to keep status. SPRG0 is a 32-bit scratch register. SPRG0 can only be written as an XIR when the processor is halted (XSR[HS] = '1').

Register Name	PPE External Interface RAMEDR Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CMEPPE.PPE.PPE_XIRAMEDR
Address	0000000013012014 (SCOM)
Description	PPE external interface RAMEDR

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	PPE_XIRAMGA_IR: PPE instruction register. Writes cause a RAM operation. It can only be written when the processor is halted (XSR[HS] = '1'). Provides the requested PPE instruction to execute.
32:63	ROX	PPE_XIRAMEDR_EDR: Error data register, set on PPE interrupts caused by an error.

Register Name	PPE External Interface DBGPRO Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CMEPPE.PPE.PPE_XIDBGPRO
Address	0000000013012015 (SCOM)
Description	PPE external interface DBGPRO

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1:3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
7	ROX	Reserved field.
8	ROX	Reserved field.
9:11	ROX	NULL_MSR_SIBRC:
12	ROX	Reserved field.
13	ROX	Reserved field.
14	ROX	NULL_MSR_WE:
15	ROX	Reserved field.
16:19	ROX	Reserved field.
20	ROX	NULL_MSR_LP:
21	ROX	Reserved field.
22:23	RO	constant = 0b00
24	ROX	Reserved field.
25	ROX	Reserved field.
26:27	RO	constant = 0b00
28	ROX	Reserved field.
29:31	ROX	Reserved field.
32:61	RWX	Reserved field.
62:63	RO	constant = 0b00

Register Name	**MIB External Interface MEM Register**
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CMEPPE.MIB.MIB_XIMEM
Address	0000000013012017 (SCOM)
Description	MIB external interface MEM information

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MIB_XIMEM_MEM_ADDR: MEM transaction buffer current or previous transaction byte address.
32	ROX	MIB_XIMEM_MEM_R_NW: MEM transaction buffer current or previous transaction type, read if '1' and write if '0'.
33	ROX	MIB_XIMEM_MEM_BUSY: Indicates if the transaction buffer is occupied with an ongoing transaction. Busy is cleared when the transaction is completed.
34	ROX	MIB_XIMEM_MEM_IMPRECISE_ERROR_PENDING: Indicates that the current or previous transaction had an imprecise error. Cleared when it is reported back to PPE. **Note:** The address of the erroneous transaction is copied into the SGB address latches such that the memory interface can continue to service I-fetches.
35:42	ROX	MIB_XIMEM_MEM_BYTE_ENABLE: MEM transaction buffer current or previous transaction byte enables.
43	ROX	MIB_XIMEM_MEM_LINE_MODE: MEM transaction buffer current or previous transaction line mode. Indicates a 32-byte read request when set to '1'.
44:48	RO	constant = 0b00000
49:51	ROX	MIB_XIMEM_MEM_ERROR: MEM transaction buffer error code. Current or previous transaction got an error on the memory interface when non-zero.
52:61	RO	constant = 0b0000000000

Bits	SCOM	Field Mnemonic: Description
62	ROX	MIB_XIMEM_MEM_IFETCH_PENDING: Indicates a instruction fetch is pending on the MEM interface when set to 1.
63	ROX	MIB_XIMEM_MEM_DATAOP_PENDING: When set to 1, indicates a data transaction is pending on the MEM interface.

Register Name	MIB External Interface Store Gather Buffer Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CMEPPE.MIB.MIB_XISGB
Address	0000000013012018 (SCOM)
Description	MIB external interface store gather buffer information

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MIB_XISGB_STORE_ADDRESS: Contains either the 4-byte SGB address tag or the address of an imprecise store error that occurred when performing a previous data transaction.
32:34	RO	constant = 0b000
35	ROX	MIB_XIMEM_MEM_IMPRECISE_ERROR_PENDING: Indicates that the current or previous transaction had an imprecise error. This field is cleared when it is reported back to PPE. **Note:** The address of the erroneous transaction is copied into the SGB address latches such that the memory interface can continue to service instruction fetches.
36:39	ROX	MIB_XISGB_SGB_BYTE_VALID: Byte valid bits within the 4B tag. Cleared when the SGB contents are committed, meaning either flushed to memory or copied into the transaction buffer. **Note:** These bits can never be set if a MEM_IMPRECISE_ERROR is pending.
40:62	RO	constant = 0b00000000000000000000000
63	ROX	MIB_XISGB_SGB_FLUSH_PENDING: When set to 1, indicates a store gather buffer flush to memory is pending on the MEM interface. Can only happen if MEM_BUSY in the MEM transaction buffer is set to 0.

Register Name	MIB External Interface ICACHE Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CMEPPE.MIB.MIB_XIICAC
Address	0000000013012019 (SCOM)
Description	MIB external interface ICACHE information

Bits	SCOM	Field Mnemonic: Description
0:26	ROX	Reserved field.
27:31	RO	constant = 0b00000
32	ROX	Reserved field.
33	RO	constant = 0b0
34	ROX	CME_SCOM_XISIB_PIB_IFETCH_PENDING: When set to 1, indicates an instruction fetch is pending on the PIB interface.
35	ROX	MIB_XIMEM_MEM_IFETCH_PENDING: When set to 1, indicates an instruction fetch is pending on the MEM interface.
36:39	ROX	Reserved field.
40:43	ROX	Reserved field.
44	RO	constant = 0b0
45	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
46	ROX	Reserved field.
47	ROX	Reserved field.
48:63	RO	constant = 0b0000000000000000

Register Name	CME_SCOM CME PCB Queue 0 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_XIPCBQ0
Address	000000001301201A (SCOM)
Description	CME_SCOM CME PCB Queue0 Info

Bits	SCOM	Field Mnemonic: Description
0:25	ROX	CME_SCOM_XIPCBQ0_PCBQ_N_INFO: CME PCBMUX queue [n] information register.
26:63	RO	constant = 0b00000000000000000000000000000000000000

Register Name	CME_SCOM CME PCB Queue 1 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_XIPCBQ1
Address	000000001301201B (SCOM)
Description	CME_SCOM CME PCB Queue1 Info

Bits	SCOM	Field Mnemonic: Description
0:25	ROX	CME_SCOM_XIPCBQ1_PCBQ_N_INFO: CME PCBMUX queue [n] information register.
26:63	RO	constant = 0b00000000000000000000000000000000000000

Register Name	CME_SCOM CME External Interface PCBMUX Data 0 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_XIPCBMD0
Address	000000001301201C (SCOM)
Description	CME_SCOM CME External Interface PCBMUX0 Data

Bits	SCOM	Field Mnemonic: Description
0:26	ROX	Reserved field.
27:63	RO	constant = 0b0000000000000000000000000000000000000

Register Name	CME_SCOM CME External Interface PCBMUX Data 1 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_XIPCBMD1
Address	000000001301201D (SCOM)
Description	CME_SCOM CME External Interface PCBMUX1 Data

Bits	SCOM	Field Mnemonic: Description
0:26	ROX	Reserved field.
27:63	RO	constant = 0b0000000000000000000000000000000000000

Register Name	CME_SCOM CME External Interface PCBMUX Information 0 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_XIPCBMI0
Address	000000001301201E (SCOM)
Description	CME_SCOM CME External Interface PCBMUX0 Info

Bits	SCOM	Field Mnemonic: Description
0:6	ROX	Reserved field.
7:63	RO	constant = 0b000000000000000000000000000000000000000000000000000000000

Register Name	CME_SCOM CME External Interface PCBMUX Information 1 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_XIPCBMI1
Address	000000001301201F (SCOM)
Description	CME_SCOM CME External Interface PCBMUX1 Info

Bits	SCOM	Field Mnemonic: Description
0:6	ROX	Reserved field.
7:63	RO	constant = 0b000000000000000000000000000000000000000000000000000000000

Register Name	CME_SCOM CME Flags Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_FLAGS
Address	0000000013012020 (SCOM) 0000000013012021 (SCOM1) 0000000013012022 (SCOM2)
Description	CME_SCOM CME Flags

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:31	RWX	WOX_CLEAR	WOX_OR	CME_SCOM_FLAGS_DATA: Flags that are defined by CME firmware.
32:63	RO	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	CME_SCOM CME Scratch 0 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_SRTCH0
Address	0000000013012023 (SCOM)
Description	CME_SCOM CME Scratch 0

Bits	SCOM	Field Mnemonic: Description
0:31	RW	CME_SCOM_SRTCH0_DATA: Scratch data.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	CME_SCOM CME Scratch 1 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_SRTCH1
Address	0000000013012024 (SCOM)
Description	CME_SCOM CME Scratch 1

Bits	SCOM	Field Mnemonic: Description
0:31	RW	CME_SCOM_SRTCH1_DATA: Scratch data.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	CME_LCL CME Local External Interrupt Source Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_LCL_EISR
Address	0000000013012025 (SCOM)
Description	CME_LCL CME local external interrupt source register

Bits	SCOM	Field Mnemonic: Description
0	ROX	CME_LCL_EISR_DEBUGGER: Debugger software uses this bit to produce an interrupt. The physical input is tied low. The respective EITR bit must be set to Edge so that a WOR to this register or pulse from the EIIR will produce an interrupt.
1	ROX	CME_LCL_EISR_DEBUG_TRIGGER: Asserted if the trace array logic analyzer logic has detected a trigger condition.
2	ROX	CME_LCL_EISR_QUAD_CHECKSTOP: QUAD checkstop present.
3	ROX	CME_LCL_EISR_PVREF_FAIL: The precision voltage reference circuit has failed and voltage regulation and VDM measurement is now in question.
4	ROX	CME_LCL_EISR_OCC_HEARTBEAT_LOST: OCC heartbeat lost indication from QPPM.
5	ROX	CME_LCL_EISR_CORE_CHECKSTOP: Core pair checkstop condition (recoverable).
6	ROX	CME_LCL_EISR_DROPOUT_DETECT: An iVRM dropout event occurred (pulse). May be used for characterization or tuning the iVRM deadzone where it is no longer able to regulate voltage.
7	ROX	CME_LCL_EISR_INTERCME_DIRECT_IN_0: Tied to INTERCME_DIRECT_IN Bit 0. Used for general communication from the sibling CME.
8	ROX	CME_LCL_EISR_BCE_BUSY_HIGH: High priority block copy engine busy indication. (Same source as bit 23, but as Low Priority; only one of these two bits should ever be unmasked). Falling edge indicates completion or error.
9	ROX	CME_LCL_EISR_BCE_TIMEOUT: Notification that BCE has not made forward progress in the time period corresponding to two scrub timer pulses (regardless of scrub enable). The BCE remains active but CME can use this notification to communicate a problem to the OCC.
10	ROX	CME_LCL_EISR_DOORBELL3_C0: Core 0 Doorbell 3 - a non-zero value is present in Core 0 PPM_CME_DOORBELL_REG3(0:7).
11	ROX	CME_LCL_EISR_DOORBELL3_C1: Core 1 Doorbell 3 - a non-zero value is present in Core 1 PPM_CME_DOORBELL_REG3(0:7).
12	ROX	CME_LCL_EISR_PC_INTR_PENDING_C0: Core 0 interrupt pending (Stop Exit Request) from PC. Mask when core is not in Stop state.
13	ROX	CME_LCL_EISR_PC_INTR_PENDING_C1: Core 1 interrupt pending (Stop Exit Request) from PC. Mask when core is not in Stop state.
14	ROX	CME_LCL_EISR_SPECIAL_WAKEUP_C0: Core 0 special wake-up present (input from Core0 PPM). **Note:** Code should mask this bit when core is not in Stop state.

Bits	SCOM	Field Mnemonic: Description
15	ROX	CME_LCL_EISR_SPECIAL_WAKEUP_C1: Core 1 special wake-up present (input from Core1 PPM). **Note:** Code should mask this bit when core is not in Stop state.
16	ROX	CME_LCL_EISR_REG_WAKEUP_C0: Core 0 external or malfunction alert interrupt wake-up source is present and enabled as a wake-up source. Code should mask this bit when core is not in Stop state. **Note:** When WSR[PC_FUSED_CORE_MODE] = '1', the hardware maps external interrupts for even threads to this bit; otherwise threads 0:3.
17	ROX	CME_LCL_EISR_REG_WAKEUP_C1: Core 1 external or malfunction alert interrupt wake-up is present and enabled as a wake-up source. Code should mask this bit when core is not in Stop state. **Note:** When WSR[PC_FUSED_CORE_MODE] = '1', the hardware maps external interrupts for odd threads to this bit; otherwise threads 4:7.
18	ROX	CME_LCL_EISR_DOORBELL2_C0: Core 0 Doorbell 2 - a non-zero value is present in Core 0 PPM_CME_DOORBELL_REG2(0:7).
19	ROX	CME_LCL_EISR_DOORBELL2_C1: Core 1 Doorbell 2 - a non-zero value is present in Core 1 PPM_CME_DOORBELL_REG2(0:7).
20	ROX	CME_LCL_EISR_PC_PM_STATE_ACTIVE_C0: Core 0 PM State Active, as controlled by FWMR. The direct signal will produce interrupts when the Core Chiplet enters ANY Stop state; the moded settings in FWMR allows for the entry into Stop 1 or all Stop Levels to be filtered to the CME.
21	ROX	CME_LCL_EISR_PC_PM_STATE_ACTIVE_C1: Core 1 PM State Active, as controlled by FWMR. The direct signal will produce interrupts when the Core Chiplet enters ANY Stop state; the moded settings in FWMR allows for the entry into Stop 1 or all Stop Levels to be filtered to the CME.
22	ROX	CME_LCL_EISR_L2_PURGE_DONE: L2 Purge Done (level) in response to the SICR L2 PURGE or ABORT request.
23	ROX	CME_LCL_EISR_NCU_PURGE_DONE: NCU Purge Done (level) in response to the SICR L2 PURGE or ABORT request.
24	ROX	CME_LCL_EISR_CHTM_PURGE_DONE_C0: Core 0 hardware trace macro purge done pulse indication.
25	ROX	CME_LCL_EISR_CHTM_PURGE_DONE_C1: Core 1 hardware trace macro purge done pulse indication.
26	ROX	CME_LCL_EISR_BCE_BUSY_LOW: Lower priority block copy engine busy indication (same source as bit 6, but as High Priority; only one of these two bits should ever be unmasked). Falling edge indicates completion or error.
27:28	ROX	CME_LCL_EISR_FINAL_VDM_DATA01: Final VDM Data bits 0:1.
29	ROX	CME_LCL_EISR_COMM_RECVD: CME Communication Received - Indicates that ICRR has been updated by the partner CME.
30	ROX	CME_LCL_EISR_COMM_SEND_ACK: CME Communication send acknowledgments. Indicates that the partner CME has affirmatively acknowledged the sent communication. Firmware must clear this bit (and cme_comm_send_nack) before writing to ICSR to ensure that acknowledgments are accurately recorded.
31	ROX	CME_LCL_EISR_COMM_SEND_NACK: CME Communication send negative acknowledgments. Indicates that the partner CME has negatively acknowledged the sent communication. Firmware must clear this bit (and cme_comm_send_ack) before writing to ICSR to ensure that acknowledgments are accurately recorded.
32:33	ROX	CME_LCL_EISR_SPARE_32_33: Implemented but unused. The physical inputs are tied low.
34	ROX	CME_LCL_EISR_PMCR_UPDATE_C0: PMCR update received from Core 0 (or via SCOM).
35	ROX	CME_LCL_EISR_PMCR_UPDATE_C1: PMCR update received from Core 1 (or via SCOM).
36	ROX	CME_LCL_EISR_DOORBELL0_C0: Core 0 Doorbell 0. A non-zero value is present in Core0 PPM_CME_DOORBELL_REG0(0:7).
37	ROX	CME_LCL_EISR_DOORBELL0_C1: Core 1 Doorbell 0. A non-zero value is present in Core1 PPM_CME_DOORBELL_REG0(0:7).
38:39	ROX	CME_LCL_EISR_INTERCME_DIRECT_IN_1_2: Tied to INTERCME_DIRECT_IN Bit(1:2). Used for general communication from the sibling CME.

Bits	SCOM	Field Mnemonic: Description
40	ROX	CME_LCL_EISR_DOORBELL1_C0: Core 0 Doorbell 1. A non-zero value is present in Core 0 PPM_CME_DOORBELL_REG1(0:7).
41	ROX	CME_LCL_EISR_DOORBELL1_C1: Core 1 Doorbell 1. A non-zero value is present in Core 1 PPM_CME_DOORBELL_REG1(0:7).
42:43	ROX	CME_LCL_EISR_RESERVED_42_43: Implemented but unused. The physical inputs are tied low.
44:63	RO	constant = 0b00000000000000000000

Register Name	CME_LCL CME Local External Interrupt Mask Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_LCL_EIMR
Address	0000000013012026 (SCOM)
Description	CME_LCL CME local external interrupt mask register

Bits	SCOM	Field Mnemonic: Description
0:43	RO	CME_LCL_EIMR_INTERRUPT_MASK: (See the CME External Interrupt Source Register for bit definitions.) Masks the respective event from producing an interrupt to the CME. The events are still captured in the EISR but are not reported via interrupt signals. 0 = Not masked (enabled). 1 = Masked.
44:63	RO	constant = 0b00000000000000000000

Register Name	CME_LCL CME Local External Interrupt Polarity Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_LCL_EIPR
Address	0000000013012027 (SCOM)
Description	CME_LCL CME local external interrupt polarity register

Bits	SCOM	Field Mnemonic: Description
0:43	RO	CME_LCL_EIPR_INTERRUPT_POLARITY: (See CME External Interrupt Source Register for bit definitions.) Establishes the edge or polarity of an interrupt. 0 = Falling low. If this bit is set to low, the respective EISR bit follows the inverted input to the OISR from the unit driving the signal. 1 = Rising high. If this bit is set to high, the respective EISR bit follows the direct input to the EISR from the unit driving the signal. When set, the respective bit in the OITR[n] is set to Edge, then the Falling and Rising meanings apply as follows: If this bit is set to Falling, a transition from 1 to 0 of the input signal to the EISR sets the respective EISR bit. If this bit is set to Rising, a transition from 0 to 1 of the input signal to the EISR sets the respective EISR bit.
44:63	RO	constant = 0b00000000000000000000

Register Name	CME_LCL CME Local External Interrupt Type Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_LCL_EITR
Address	0000000013012028 (SCOM)
Description	CME_LCL CME Local External Interrupt Type Register

Bits	SCOM	Field Mnemonic: Description
0:43	RO	CME_LCL_EITR_INTERRUPT_TYPE: See the CME External Interrupt Source for bit definitions. Establishes the type of interrupt that is monitored. 0 = Level. When set to Level, the respective EISR bit follows the input to the EISR from the unit driving the signal but with the polarity defined by the EIPR. Specifically, if the respective EIPR bit is set to High, this register retains the polarity of the incoming signal; if the respective EIPR bit is set to Low, this register captures the inverted polarity of the incoming signal. 1 = Edge. When set to Edge, the respective EISR bit is asserted upon the transition defined by the CME External Interrupt Source Register of the input from the unit driving the signal. Specifically, if the respective EIPR bit is set to Rising, a transition from 0 to 1 sets the bit; if the respective EIPR bit is set to Falling, a transition from 1 to 0 sets the bit. **Note:** When set to Level, attempts to override the signal setting via W1CLR or WOR to the CME External Interrupt Source Register will not stick as the signal input is the priority. Firmware must control the source of the Level signal to control the state of the EISR bit. When set to Edge, CLEAR and OR operations to the EISR will stick (clear or set respectively) in the EISR. **Engineering Note:** For firmware testing, a potential interrupt injection technique for Level interrupts is to override their definition to Edge and then use the OR register associated with the CME External Interrupt Source Register. This allows the injected transition to stick, as the logic will not follow the input interrupt signal. However, if the firmware is expecting to find status in the driving unit, this technique may not be appropriate.
44:63	RO	constant = 0b00000000000000000000

Register Name	CME_LCL CME Local External Interrupt Status Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_LCL_EISTR
Address	0000000013012029 (SCOM)
Description	CME_LCL CME local external interrupt status register

Bits	SCOM	Field Mnemonic: Description
0:43	RO	Reserved field.
44:63	RO	constant = 0b00000000000000000000

Register Name	CME_LCL CME Local External Interrupt Input Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_LCL_EINR
Address	000000001301202A (SCOM)
Description	CME_LCL CME local external interrupt input register

Bits	SCOM	Field Mnemonic: Description
0:43	ROX	CME_LCL_EINR_INTERRUPT_INPUT: Raw inputs to the interrupt controller.
44:63	RO	constant = 0b00000000000000000000

Register Name	CME_SCOM CME Local External Interrupt Injection Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_EIIR
Address	000000001301202B (SCOM)
Description	CME_SCOM CME local external interrupt injection register

Bits	SCOM	Field Mnemonic: Description
0	WO_4P	CME_SCOM_EIIR_DEBUGGER: Generates a pulse that is ORed with the same EISR bit position and name.
1	WO_4P	CME_SCOM_EIIR_DEBUG_TRIGGER: Generates a pulse that is ORed with the same EISR bit position and name.
2:8	RO	constant = 0b0000000
9	RW	CME_SCOM_EIIR_BCE_TIMEOUT: ORed with the same EISR bit position and name.
10:11	RO	constant = 0b00
12	RW	CME_SCOM_EIIR_PC_INTR_PENDING_C0: ORed with the same EISR bit position and name.
13	RW	CME_SCOM_EIIR_PC_INTR_PENDING_C1: ORed with the same EISR bit position and name.
14	RW	CME_SCOM_EIIR_SPECIAL_WAKEUP_C0: ORed with the same EISR bit position and name.
15	RW	CME_SCOM_EIIR_SPECIAL_WAKEUP_C1: ORed with the same EISR bit position and name.
16	RW	CME_SCOM_EIIR_REG_WAKEUP_C0: ORed with the same EISR bit position and name.
17	RW	CME_SCOM_EIIR_REG_WAKEUP_C1: ORed with the same EISR bit position and name.
18:19	RO	constant = 0b00
20	RW	CME_SCOM_EIIR_PC_PM_STATE_ACTIVE_C0: ORed with the same EISR bit position and name.
21	RW	CME_SCOM_EIIR_PC_PM_STATE_ACTIVE_C1: ORed with the same EISR bit position and name.

Bits	SCOM	Field Mnemonic: Description
22	RW	CME_SCOM_EIIR_L2_PURGE_DONE: ORed with the same EISR bit position and name.
23	RW	CME_SCOM_EIIR_NCU_PURGE_DONE: ORed with the same EISR bit position and name.
24	WO_4P	CME_SCOM_EIIR_CHTM_PURGE_DONE_C0: ORed with the same EISR bit position and name.
25	WO_4P	CME_SCOM_EIIR_CHTM_PURGE_DONE_C1: ORed with the same EISR bit position and name.
26:63	RO	constant = 0b00000000000000000000000000000000000000

Register Name	**CME_SCOM CME VDM Count Configuration Register**
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_VCCR
Address	000000001301202C (SCOM)
Description	CME_SCOM CME VDM count configuration register

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CME_SCOM_VCCR_SMALL_EVENT_THRESHOLD: Number of timer periods (or 4:1 cycle periods if DROOP_TIMER_MODE = 0) that a small droop event was seen. Used for event duration profiling (16b).
16:27	RW	CME_SCOM_VCCR_LARGE_EVENT_THRESHOLD: Number of timer periods (or 4:1 cycle periods if DROOP_TIMER_MODE = 0) that a large droop event was seen. Used for event duration profiling (12b).
28:35	RW	CME_SCOM_VCCR_EXTREME_EVENT_THRESHOLD: Number of timer periods (or 4:1 cycle periods if DROOP_TIMER_MODE = 0) that an extreme droop event was seen. Used for event duration profiling (8b).
36:37	RW	CME_SCOM_VCCR_DROOP_PROFILE_TYPE: Chooses profile type in the programmable VECR event fields: 00 = Total droop duration (of that level or deeper). 01 = Only that level droop duration (without going deeper). 10 = That level-in-a-row duration (despite going deeper, before or after). 11 = Only that level in-a-row duration (without ever going deeper). **Note:** Setting an above threshold = 0x0 makes the DROOP_PROFILE(1) a *don't care*.
38	RW	CME_SCOM_VCCR_DROOP_TIMER_MODE: 0 = The VDCR counters increment their 1:1 precounter every cycle that droop level is active, and this precounter increments the corresponding 4:1droop counter whenever it carries. 1 = The VDCR counters increment if its droop level input was ever active for one or more cache cycles between two timer input pulses (~31ns period) without a deeper droop in that same period.
39	RW	CME_SCOM_VCCR_DROOP_CHAR_MODE: Enables Droop characterization mode. When set, this changes the behavior of the VDM Sample counters (VDCR & VNCR, but not VECR) for lab characterization and disables runtime monitoring (threshold detects) from setting Droop errors in the FIR. Based on this mode, the fields in VDCR and VNCR: 0 = Count how many times a droop state has occurred so far during the configured droop sample window, and clear at the beginning of each sample period 1 = Count how many times a droop has occurred since the last read to that register, which clears it. In this mode, code must read the QMFR register simultaneously to compare against the delta in either CYCLES or TIMEBASE pulses (dependent on DROOP_TIMER_MODE).
40	RW	CME_SCOM_VCCR_DROOP_NOTIFY_ENABLE: Causes VDM droop indication to notify the QPPM macro by enabling the UNMASKED FIR bits for the three dropout errors to OR into the (now misnamed) QPPM_IVRM_DROPOUT signal.
41:43	RW	CME_SCOM_VCCR_SPARE41_43: Implemented but not used.
44:58	RO	constant = 0b000000000000000

Bits	SCOM	Field Mnemonic: Description
59:63	RW	CME_SCOM_VCCR_DROOP_SAMPLE_RATE: Sample rate used when DROOP_CHAR_MODE = 0, whose meaning is dependent on the value of DROOP_TIMER_MODE: 0 = This field specifies the rising edge of which bit of the QFMR[CYCLES] to use to start a new sample window 1 = Bits (1:4) of this field are used as a TSEL using the PPE timer to select which output bit is used to start a new sample window (bit 0 is unused). This delay is defined as $2^{(29 - select)}$/ Nest_Frequency. The default value for this register corresponds to 262 µs (assuming a 2 GHz processor bus). **Note:** When this register is written, the first sample window will be truncated (smaller) than the selected value depending on the relative value in the selected timer being used. An event threshold may still be reached despite the smaller window.

Register Name	CME_SCOM CME IVRM Dropout Configuration Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_IDCR
Address	000000001301202D (SCOM)
Description	CME_SCOM CME iVRM dropout configuration register

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CME_SCOM_IDCR_DROPOUT_EVENT_THRESHOLD: Number of sustained dropout periods that must be counted before setting a Dropout Event. Setting this field to zero disables dropout event notifications when this field is non-zero, DROPOUT_CHAR_MODE == 0, and any of the three *_DROPOUT_EVENT_COUNT == the value of this field, the corresponding *_IVRM_DROPOUT bit is set in the FIR register and is ORed as a pulse into the DROPOUT_DETECT bit in the EISR.
24:31	RW	CME_SCOM_IDCR_DROPOUT_INAROW_THRESHOLD: Dropout count value used to determine a sustained dropout period has occurred. How many 4:1 cache cycles (or timer periods if DROPOUT_TIMER_MODE = 1) in a row the dropout must be present before being counted in the *_DROPOUT_EVENT_COUNT. Note that a value of '1' causes every Dropout to be counted.
32	RW	CME_SCOM_IDCR_DROPOUT_TIMER_MODE: Dropout period timer select. Controls the Dropout Present condition used to increment the *_DROPOUT_INAROW_COUNT. 0 = Every 4:1 cache cycle counts towards the droop count. (Implementation note: Dropout Present is connected to the output of the 'dropout indication' latch, which follows the value of dropout input.) 1 = Dropout indication must be asserted for an entire CME input timer pulse period to be counted (~31 ns). (Implementation note: Set-dominant sticky 'dropout indication' latch running at 4:1 is set on every timer pulse and is reset whenever the dropout input = '0'. Dropout present is the AND of the indication latch output and the timer pulse.
33	RW	CME_SCOM_IDCR_DROPOUT_CHAR_MODE: Enables Dropout Characterization mode. Changes the behavior of the *_DROPOUT_EVENT_COUNT for run-time monitoring versus lab characterization of the iVRM dead zone. Based on this mode, the *_DROPOUT_EVENT_COUNT fields: 0 = Count how many times a sustained dropout period has been detected so far during the configured dropout sample window, and clear at the beginning of each sample window. 1 = Count how many time s a sustained dropout period has occurred since the last read to that register, which clears it. In this mode code must read the QFMR register simultaneously to compare against the delta in either CYCLES or TIMEBASE pulses (dependent on DROPOUT_TIMER_MODE).
34:35	RW	CME_SCOM_IDCR_SIBLING_CORE_DROPOUT_ENABLE: Connected to cme_dropout_enable_out(0:1). Used by the QUAD Manager hcode to control the dropout detection of the other pair of cores in the QUAD in the sibling CME. These bits must be set to '11' for the non-QUAD Manager CME.
36:37	RW	CME_SCOM_IDCR_CORE_DROPOUT_ENABLE: These are ANDed with cme_dropout_enable_in(0:1) from the sibling CME to enable the C[01]_IVRM_DROPOUT function. These bits must be set to '11' for the non-QUAD Manager CME.
38	RW	CME_SCOM_IDCR_CACHE_DROPOUT_ENABLE: Connected to cme_dropout_enable_out(2). This bit is also AND'd with cme_dropout_enable_in(2) to enable the CACHE_IVRM_DROPOUT function in this CME. This bit must also be set to '1' for the non-QUAD Manager CME.
39	RW	CME_SCOM_IDCR_SPARE: Implemented but not used.

Bits	SCOM	Field Mnemonic: Description
40	RW	CME_SCOM_IDCR_DROPOUT_NOTIFY_ENABLE: Causes Dropout indication to notify the QPPM macro by enabling the UNMASKED FIR bits for the three Dropout errors to OR into the QPPM_IVRM_DROPOUT signal.
41:43	RW	CME_SCOM_IDCR_SPARE41_43: Implemented but not used.
44:58	RO	constant = 0b000000000000000
59:63	RW	CME_SCOM_IDCR_DROPOUT_SAMPLE_RATE: Sample Rate used when DROPOUT_CHAR_MODE = 0, whose meaning is dependent on the value of DROPOUT_TIMER_MODE: 0 = This field specifies rising edge of which bit of the QFMR[CYCLES] to use to start a new sample window 1 = Bits (1:4) of this field are used as a TSEL using the PPE timer to select which output bit is used to start a new sample window (bit 0 unused). This delay is defined as $2^{(29 - \text{select})}$ / Nest_Frequency. The default value for this register corresponds to 262 µs (assuming a 2 GHz processor bus). Note that when this register is written, the first sample window will be truncated (smaller) than the selected value dependent on the relative value in the selected timer being used. An event threshold may still be reached despite the smaller window.

Register Name	CME_SCOM CME Core IVRM Dropout Sample Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_CIDSR
Address	000000001301202E (SCOM)
Description	CME_SCOM CME core iVRM dropout sample register

Bits	SCOM	Field Mnemonic: Description
0:23	ROX	CME_SCOM_CIDSR_C0_DROPOUT_EVENT_COUNT: Count of how many sustained dropouts have been detected for the core chiplet 0 iVRM. This counter always saturates at 0xFFFFFF and clears when the IDCR is written. Additionally, the behavior of this field depends on the value of IDCR[DROPOUT_CHAR_MODE].
24:31	ROX	CME_SCOM_CIDSR_C0_DROPOUT_INAROW_COUNT: Counter recording how many dropout indications for the core chiplet 0 iVRM have occurred in-a-row form a sustained dropout period. This field increments on each dropout present and resets when either: a) this field equals the DROPOUT_INAROW_THRESHOLD, b) the Dropout Present indicator = 0, or c) the IDCR register is written. **Notes:** 1. If a reset occurs on a cycle when dropout is present, the counter is set to a value of 1, else it resets to 0. 2. When in CHAR_MODE, starting a new sample window does not affect this counter.
32:55	ROX	CME_SCOM_CIDSR_C1_DROPOUT_EVENT_COUNT: Count of how many sustained dropouts have been detected for the core chiplet 1 iVRM. This field operates like the core chiplet 0 counter in the preceding fields.
56:63	ROX	CME_SCOM_CIDSR_C1_DROPOUT_INAROW_COUNT: Counter recording how many dropout indications for the core chiplet 1 iVRM have occurred in-a-row form a sustained dropout period. This field operates like the core chiplet 0 counter in the preceding fields.

Register Name	CME_SCOM CME QUAD/Cache iVRM Dropout Sample Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_QIDSR
Address	000000001301202F (SCOM)
Description	CME_SCOM CME QUAD/cache iVRM dropout sample register

Bits	SCOM	Field Mnemonic: Description
0:23	ROX	CME_SCOM_QIDSR_CACHE_DROPOUT_EVENT_COUNT: Count of how many sustained dropouts have been detected for the cache chiplet iVRM. This field operates like the core chiplet counters in the CME_SCOM CME Core iVRM Dropout Sample Register.

Bits	SCOM	Field Mnemonic: Description
24:31	ROX	CME_SCOM_QIDSR_CACHE_DROPOUT_INAROW_COUNT: Counter recording how many dropout indications for the Cache Chiplet iVRM have occurred in-a-row form a sustained dropout period. This field operates like the Core Chiplet counters in the preceding register.
32:34	ROX	CME_SCOM_QIDSR_DROPOUT_SAMPLE: Instantaneous values coming directly from the iVRM dropout signals. Bit0 = Core0 (Core2 for CME1). Bit1 = Core1 (Core3 for CME1). Bit2 = Cache.
35:61	RO	constant = 0b000000000000000000000000000

Register Name	CME_SCOM CME Block Copy Engine Base Address Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_BCEBAR0
Address	0000000013012030 (SCOM)
Description	CME_SCOM CME block copy engine base address register0

Bits	SCOM	Field Mnemonic: Description
0:7	RO	constant = 0b00000000
8:43	RW	CME_SCOM_BCEBAR0_BASE: Specifies bits 8:43 of the processor bus base address of the mapping. If this mapping is enabled (BCEBAR[SIZE] not 0), the base address is required to be aligned such that the BCEBAR[SIZE] - 1 low-order bits of the field are '0'.
44:56	RO	constant = 0b0000000000000
57:58	RW	CME_SCOM_BCEBAR0_RD_SCOPE: Scope for Read transaction broadcasts across the processor bus to the system Memory controllers, used to optimize processor bus traffic and latency. **Note:** Should be set intelligently based on known physical memory mapping based on CME Memory Location Affinity.
59	RW	CME_SCOM_BCEBAR0_WR_SCOPE: Scope for Write transaction broadcasts. See above for definition. **Note:** Local Node Scope is not allowed for writes through the NCU.
60	RW	CME_SCOM_BCEBAR0_VG_TARGET_SEL: Selects the 16-bit target for vectored group transactions to use. Note: this bit is ignored for read transactions when RD_SCOPE != 01 or for write transactions when WR_SCOPE != 1, in which case the target is always 0x0000. This bit should only be set as a workaround for power bus issues.
61:63	RW	CME_SCOM_BCEBAR0_SIZE: Specifies the size of the mapping: 0 = Mapping disabled 1 = 1 MB 2 = 2 MB 3 = 4 MB 4 = 8 MB 5 = 16 MB 6 = 32 MB 7 = 64 MB

Register Name	CME_SCOM CME Block Copy Engine Base Address 1 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_BCEBAR1
Address	0000000013012031 (SCOM)
Description	CME_SCOM CME block copy engine base address 1 register

Bits	SCOM	Field Mnemonic: Description
0:7	RO	constant = 0b00000000
8:43	RW	CME_SCOM_BCEBAR1_BASE: Specifies bits 8:43 of the processor bus base address of the mapping. If this mapping is enabled (BCEBAR[SIZE] not 0), the base address is required to be aligned such that the BCEBAR[SIZE] - 1 low-order bits of the field are '0'.
44:56	RO	constant = 0b0000000000000
57:58	RW	CME_SCOM_BCEBAR1_RD_SCOPE: Scope for Read transaction broadcasts across the processor bus to the system Memory controllers, used to optimize processor bus traffic and latency. **Note:** Should be set intelligently based on known physical memory mapping based on CME Memory Location Affinity.
59	RW	CME_SCOM_BCEBAR1_WR_SCOPE: Scope for Write transaction broadcasts. See above for definition. **Note:** Local Node Scope is not allowed for writes through the NCU.
60	RW	CME_SCOM_BCEBAR1_VG_TARGET_SEL: Selects the 16-bit Target for Vectored Group transactions to use. Note: this bit is ignored for read transactions when RD_SCOPE != 01 or for write transactions when WR_SCOPE != 1, in which case the target is always 0x0000. This bit should only be set as a workaround for power bus issues.
61:63	RW	CME_SCOM_BCEBAR1_SIZE: Specifies the size of the mapping: 0 = Mapping disabled 1 = 1 MB 2 = 2 MB 3 = 4 MB 4 = 8 MB 5 = 16 MB 6 = 32 MB 7 = 64 MB

Register Name	CME_SCOM CME QUAD Frequency Measurement Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_QFMR
Address	0000000013012032 (SCOM)
Description	CME_SCOM CME QUAD frequency measurement register

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	CME_SCOM_QFMR_TIMEBASE: CME Timebase free-running counter whose least significant bit increments every CME timer input pulse, which will be configured to run at nest (processor bus) clock64. (At 2 GHz, this will increment every 32 ns, and this counter will wrap every 137 seconds.) Firmware must perform all delta calculations (including accounting for the wrap condition) to perform elapsed time functions.
32:63	ROX	CME_SCOM_QFMR_CYCLES: Free-running cycle counter that accumulates number of QUAD cycles4. Delta of this field per unit time (using the TIMEBASE field in this register) allows for an accurate average frequency calculation: CoreFreqavg = (Freqnest 8) * delta(CYCLESA,CYCLESB) delta(TIMEBASEA,TIMEBASEB), where the delta(A,B) function includes counter wraproll-over correction as follows: delta(A,B) = (((D = B – A) < 0) ? D+=232 : D).

Register Name	CME_SCOM CME Average Frequency Sample Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_AFSR
Address	0000000013012033 (SCOM)
Description	CME_SCOM CME average frequency sample register

Bits	SCOM	Field Mnemonic: Description
0:19	ROX	CME_SCOM_AFSR_INST_CYCLE_SAMPLE: Instantaneous count of the number of cycles that elapsed during the last sample period. Allows firmware to perform an average frequency calculation over the most recent sample period. The sample rate is controlled by FWMR[AVG_FREQ_TSEL]. The average frequency can then be calculated by firmware as: (Nest_Frequency* INST_CYCLE_SAMPLE 2^(29-FWMR[AVG_FREQ_TSEL])).
20:31	RO	constant = 0b000000000000
32:51	ROX	CME_SCOM_AFSR_AVG_CYCLE_SAMPLE: Running average of sampled cycles collected since the last read to this register. Allows firmware to perform a slightly longer term average frequency calculation. **Note:** Reads reset this field to INST_CYCLE_SAMPLE. For every INST_CYCLE_SAMPLE sample, the hardware performs the following calculation: AVG_CYCLE_SAMPLE = (3*AVG_CYCLE_SAMPLE + INST_CYCLE_SAMPLE)4 This means that after four samples, this field will contain 32% previous avg + 11% three samples ago + 14% two samples ago + 19% the last sample + 25% INST_CYCLE_SAMPLE, which is approximately 13 *previous AVG_CYCLE_SAMPLE + 25 * average of last 3 samples + 14 INST_CYCLE_SAMPLE.
52:62	RO	constant = 0b00000000000
63	ROX_CLRPART	CME_SCOM_AFSR_SAMPLE_VALID: A sample has occurred and caused this register to be updated since the last time it was read.

Register Name	**CME_SCOM CME Average Frequency Threshold Register**
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_AFTR
Address	0000000013012034 (SCOM)
Description	CME_SCOM CME Average Frequency Threshold Register

Bits	SCOM	Field Mnemonic: Description
0:19	ROX	CME_SCOM_AFTR_MAX_CYCLE_SAMPLE: Largest INST_CYCLE_SAMPLE value that occurred since the last read to this register. **Note:** Reads reset this field to AFSR[INST_CYCLE_SAMPLE].
20:31	RO	constant = 0b000000000000
32:51	ROX	CME_SCOM_AFTR_MIN_CYCLE_SAMPLE: Smallest INST_CYCLE_SAMPLE value that occurred since the last read to this register. **Note:** Reads reset this field to AFSR[INST_CYCLE_SAMPLE].
52:63	RO	constant = 0b000000000000

Register Name	**CME_SCOM CME VDM Droop Count Register**
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_VDCR
Address	0000000013012035 (SCOM)
Description	CME_SCOM CME VDM droop count register

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	CME_SCOM_VDCR_VDM_EXTREME_DROOP_CTR: Extreme droop threshold counter (16b). This counter always saturates at 0xFFFF and clears when the VDSR is written. Otherwise the behavior of this field depends on the value of DROOP_CHAR_MODE. (Increments when b'0xxx'.)
16:39	ROX	CME_SCOM_VDCR_VDM_LARGE_DROOP_CTR: Large droop threshold counter (24b). This counter always saturates at 0xFFFFFF and clears when the VDSR is written. Otherwise the behavior of this field depends on the value of DROOP_CHAR_MODE. (Increments when b'10xx'.)

Bits	SCOM	Field Mnemonic: Description
40:63	ROX	CME_SCOM_VDCR_VDM_SMALL_DROOP_CTR: Small droop threshold counter (24b). This counter always saturates at 0xFFFFFF and clears when the VDSR is written. Otherwise the behavior of this field depends on the value of DROOP_CHAR_MODE. (Increments when b'110x'.)

Register Name	**CME_SCOM CME VDM No-Droop Count Register**
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_VNCR
Address	0000000013012036 (SCOM)
Description	No-droop count register

Bits	SCOM	Field Mnemonic: Description
0:15	RO	constant = 0b0000000000000000
16:39	ROX	CME_SCOM_VNCR_VDM_NO_DROOP_CTR: No droop threshold counter (24b). This counter always saturates at 0xFFFFFF and clears when the VDSR is written. Otherwise the behavior of this field depends on the value of DROOP_CHAR_MODE and DROOP_TIMER_MODE. (Increments when b'1110'.)
40:63	ROX	CME_SCOM_VNCR_VDM_OVERVOLT_CTR: Overvolt threshold counter (24b). This counter always saturates at 0xFFFFFF and clears when the VDSR is written. Otherwise the behavior of this field depends on the value of DROOP_CHAR_MODE and DROOP_TIMER_MODE. (Increments when b'1111'.)

Register Name	**CME_SCOM CME VDM Data Sample Register**
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_VDSR
Address	0000000013012037 (SCOM)
Description	CME_SCOM CME VDM data sample register

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	CME_SCOM_VDSR_INSTANT_VDM_CONTROL_SUMMARY: Instantaneous VDM summary to DPLL.
4:7	ROX	CME_SCOM_VDSR_INSTANT_CACHE_VDM_DATA: Instantaneous cache VDM output.
8:11	ROX	CME_SCOM_VDSR_INSTANT_CORE0_VDM_DATA: Instantaneous core chiplet 0 VDM output.
12:15	ROX	CME_SCOM_VDSR_INSTANT_CORE1_VDM_DATA: Instantaneous core chiplet 1 VDM output.
16:19	ROX	CME_SCOM_VDSR_INSTANT_CORE2_VDM_DATA: Instantaneous core chiplet 2 VDM output.
20:23	ROX	CME_SCOM_VDSR_INSTANT_CORE3_VDM_DATA: Instantaneous core chiplet 3 VDM output.
24:31	RO	constant = 0b00000000
32:35	ROX	CME_SCOM_VDSR_STICKY_VDM_CONTROL_SUMMARY: Worst case VDM summary to DPLL per-cycle sticky-AND operation. Resets to 1111 on read.
36:39	ROX	CME_SCOM_VDSR_STICKY_CACHE_VDM_DATA: Worst case cache VDM output per-cycle sticky-AND operation. Resets to 1111 on read.
40:43	ROX	CME_SCOM_VDSR_STICKY_CORE0_VDM_DATA: Worst case core chiplet 0 VDM output per-cycle sticky-AND operation. Resets to 1111 on read.
44:47	ROX	CME_SCOM_VDSR_STICKY_CORE1_VDM_DATA: Worst case core chiplet 1 VDM output per-cycle sticky-AND operation. Resets to 1111 on read.
48:51	ROX	CME_SCOM_VDSR_STICKY_CORE2_VDM_DATA: Worst case core chiplet 2 VDM output per-cycle sticky-AND operation. Resets to 1111 on read.
52:55	ROX	CME_SCOM_VDSR_STICKY_CORE3_VDM_DATA: Worst case (sticky) core chiplet 3 VDM output per-cycle sticky-AND operation. Resets to 1111 on read.

Bits	SCOM	Field Mnemonic: Description
56:63	RO	constant = 0b00000000

Register Name	CME_SCOM CME VDM Event Count Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_VECR
Address	0000000013012038 (SCOM)
Description	CME_SCOM CME VDM event count register

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	CME_SCOM_VECR_TOTAL_DROOP_EVENT_CTR: Total number of droop events detected (starting from over-volt or no-droop condition, regardless of depth).
16:31	ROX	CME_SCOM_VECR_SMALL_EVENT_PROFILE_CTR: Number of small droop profiled events, counts how often the small droop event > small threshold based on DROOP_PROFILE_TYPE. 00 = Total droop duration (small or deeper). 01 = Small-only droop duration (without ever going deeper). 10 = Small-in-a-row duration (despite going deeper, before or after). 11 = Small-only in-a-row duration (without ever going deeper).
32:43	ROX	CME_SCOM_VECR_LARGER_DROOP_EVENT_CTR: Number of large (or deeper) droop events detected (starting from over-volt or no-droop droop condition).
44:55	ROX	CME_SCOM_VECR_LARGE_EVENT_PROFILE_CTR: Number of large droop profiled events, counts how often the large droop event > large threshold based on DROOP_PROFILE_TYPE. 00 = Total droop duration (large or deeper). 01 = Large-only droop duration (without ever going deeper). 10 = Large-in-a-row duration (despite going deeper, before or after). 11 = Large-only in-a-row duration (without ever going deeper).
56:63	ROX	CME_SCOM_VECR_EXTREME_DROOP_EVENT_CTR: Number of extreme droop profiled events, droop event > extreme threshold based on DROOP_PROFILE_TYPE. 00 or 01 = Total extreme droop duration (deeper not possible). 10 or 11 = Extreme-in-a-row duration (deeper not possible).

Register Name	CME_SCOM CME VDM Count Threshold Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_VCTR
Address	0000000013012039 (SCOM)
Description	CME_SCOM CME VDM Count Threshold Register

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CME_SCOM_VCTR_VDM_EXTREME_DROOP_THRESHOLD: Extreme droop threshold. A value of all zeros disables this threshold. Otherwise, when DROOP_CHAR_MODE = '0', if this value matches the count value for this same field in VDCR, an LFIR[extreme_droop_err] is indicated.
16:39	RW	CME_SCOM_VCTR_VDM_LARGE_DROOP_THRESHOLD: Large droop threshold. A value of all zeros disables this threshold. Otherwise, when DROOP_CHAR_MODE = '0', if this value matches the count value for this same field in VDCR, an LFIR[large_droop_err] is indicated.
40:63	RW	CME_SCOM_VCTR_VDM_SMALL_DROOP_THRESHOLD: Small droop threshold. A value of all zeros disables this threshold. Otherwise, when DROOP_CHAR_MODE = '0', if this value matches the count value for this same field in VDCR, an LFIR[small_droop_err] is indicated.

Register Name	CME_SCOM CME Local Mode Control Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_LMCR
Address	000000001301203A (SCOM) 000000001301203B (SCOM1) 000000001301203C (SCOM2)
Description	CME_SCOM CME local mode control register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_PMCR_OVERRIDE_EN: Enables SCOM writes to both PMCRS registers for manual testing access. Disables core chiplet updates from the PMCR serial interface from PC. 0 = Core shifter updates are accepted; SCOM updates are blocked and return Invalid Access return code. 1 = SCOM updates are accepted; core shifter updates are ignored. Note: This bit is intended to only be changed during IPL, not during run time.
1	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_PSCR_OVERRIDE_EN: Enables SCOM write to the PSCRS registers for manual testing access. Disables core chiplet updates from the PSCR serial interface from PC. Same behavior as the previous bit.
2	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_PMSR_OVERRIDE_EN: Enable SCOM control for the stop-GPE or manual testing to serially shift values into the processor cores. 0 = CME writes are accepted; SCOM updates are ignored and return invalid access return code. 1 = SCOM writes are accepted; CME writes are blocked and timeout (PPE MCHK) will occur. **Note:** This bit is intended to only be changed during IPL, not during run time.
3	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_BCECSR_OVERRIDE_EN: Disables local register writes to the BCECSR to allow SCOM to perform block copy operations to the CME SRAM instead. Same behavior as the previous bit.
4	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_IDR_LCL_SAMPLE_EN: Allow the CME local interface to control the iVRM Dropout Data and Configuration Registers. If this bit is set to one and SCOM attempts to read the CIDSR and QIDSR or to write the IDCR, an invalid access error code is returned on the SCOM interface. If this bit is zero, CME attempts to read the CIDSR and QIDSR or to write the IDCR local registers are ignored (will cause a timeout) and do not clear the sample registers.
5	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_VDM_LCL_SAMPLE_EN: Allow the CME local interface to sample the VDM Sample Registers. If this bit is set to one and SCOM attempts to read the VCSR or VDSR, an invalid access error code is returned on the SCOM interface. If this bit is zero, CME attempts to read the VCSR and VDSR local registers are ignored (will cause a timeout) and do not clear the registers.
6	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_FREQ_LCL_SAMPLE_EN: Allow the CME local interface to sample the frequency sample registers. If this bit is set to one and SCOM attempts to read the AFSR or AFTR, an invalid access error code is returned on the SCOM interface. If this bit is zero, CME attempts to read the AFSR and AFTR local registers are ignored (will cause a timeout) and do not clear the registers.
7	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_LOCK_PCB_ON_ERR: When set, unmasked PCB errors will cause the PCB queue logic to lock or stop accepting new PCB requests from the memory bolt-on, in order to preserve debug data in the interface registers.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
8	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_QUEUED_WR_EN: Enable CME to perform queued PCB write operations. If not set, attempts to store to queued PCB address encodes will return a DSI error to PPE.
9	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_QUEUED_RD_EN: Enable CME to perform queued PCB read operations. If not set, attempts to load from queued PCB address encodes will return a DSI error to PPE.
10	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_MASK_PURGE_INTERFACE: Suppress CME from sending and receiving purge request to the L2, NCU, and CHTM. When this bit is set: the PURGE and PURGE_ABORT bits in the SICR should be gated off to always output zero from the CME to those units, and mask off the PURGE_DONE inputs from those units into the EISR (but does not mask off the corresponding EIIR bits).
11	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_SPARE_11: Implemented but unused.
12	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_C0_AUTO_SPECIAL_WAKEUP_DISABLE: When set, specifies to not automatically force PM_EXIT = 1 and PM_ENTRY_ACK = 0 to core 0 in response to a special wake-up request, and to not automatically assert done back to the Core PPM (using instead the values in the SICR). **Notes:** 1. This bit should be set by CME Hcode when the core chiplet is in a STOP state > 1 or transitioning in or out of the STOP state. 2. When this mode is set, special wake-up interrupts in the EIMR must never be masked by code during run time (but otherwise in auto mode, special wake-ups should only be unmasked when the core is in stop state). This bit should be cleared by hcode when the core is in a stop state such that special wake-up transitions intersecting with regular wake-ups do not create blips on PM_EXIT and confuse the PC logic.
13	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_C1_AUTO_SPECIAL_WAKEUP_DISABLE: Same as previous bit, but for core chiplet 1.
14	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_C0_HALTED_STOP_OVERRIDE_DISABLE: By default, the POWER9 core chiplets should be allowed to automatically go in and out of STOP state when the PPE is halted and not available to service its STOP entry and exit requests (in effect converting all stop requests to a Level1). This allows the system to continue running when the CME is being halted for lab debug, or in the unlikely event that a CME error happens. This bit should be set by CME Hcode when either core chiplet is in a STOP state > 1 or transitioning in or out of STOP state. 1 = PPE halted has no effect on the PC STOP interface signals to core chiplet 0. 0 = PPE halted indication is ORed with the CME_SCOM_FWMR[STOP_OVERRIDE_MODE] functionality for core chiplet 0.
15	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_C1_HALTED_STOP_OVERRIDE_DISABLE: Same as previous bit, but for core chiplet 1.
16	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_STOP_OVERRIDE_MODE: Override to disable CME being involved in Stop sequencing, in effect converting all new stop requests into stop level 1. Setting this mode will prevent the core chiplets from hanging on STOP instructions if the CME does not respond. Available to software or simulation as a workaround. (Equivalent to setting both treat_sleep_as nap and treat_winkle_as_sleep in POWER8). **Note:** The user is responsible to first special wake-up the core chiplets corresponding to this CME before changing this bit. **Implementation note:** When set, always assert PM_ENTRY_ACK, PM_WAKE_UP, and deassert BLOCK_INTERRUPTS to both core chiplets, regardless of the values of these controls in SICR.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
17	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_STOP_ACTIVE_MASK: This mode will gate off PC_PM_STATE_ACTIVE from both core chiplets from setting the EISR (using the interrupt bolt-on fence such that it is still visible in the EINR), allowing the EIMR to remain unchanged. **Note:** Must only be set if STOP_OVERRIDE_MODE = 1; otherwise PC (and therefore the core chiplet) will hang.
18	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_AUTO_STOP1_DISABLE: Disables instant entry and exit nap mode for stop 1 without CME code involvement. This bit must be set to enable auto-promote or CME hardware workarounds for the stop 1 state. When this bit is set, the CME is responsible for controlling the stop interface to PC via the SICR for stop level 1 transitions. **Note:** The user is responsible to first special wake-up the core chiplets corresponding to this CME before changing this bit. When this bit is set, STOP1_ACTIVE_ENABLE must also be set. **Implementation note:** When a Core Chiplet asserts PC_PM_STATE_ACTIVE with PC_PM_STATE = 1 (or = 0, although it should never occur), the hardware by default automatically asserts the stop interface control signals to that core chiplet as described in STOP_OVERRIDE MODE without CME involvement. Setting this bit disables that hardware functionality.
19	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_STOP1_ACTIVE_ENABLE: This mode will enable PC_PM_STATE_ACTIVE from a core chiplet to set the EISR when a core chiplet asserts PC_PM_STATE_ACTIVE with PC_PM_STATE = 1 (or = 0, although it should never occur), allowing the EIMR to remain unchanged. Otherwise, the EISR for that core chiplet (using the interrupt bolt-on fence such that it is still visible in the EINR) is not set for this condition.
20	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_FENCE_EISR: Fence off all interrupt inputs from causing EISR bits to be set. May be used for workarounds to keep from having to clean up the EISR afterwards. **Note:** Implemented in hardware by asserting all fence inputs to the ICB.
21	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_PC_DISABLE_DROOP: Assert disable droop signal to both cores. Used to temporarily disable instruction throttling for workarounds or reconfiguration. ORed with CME_LCL_LMCR to feed a single output of CME.
22:23	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_SPARE_22_23: Implemented but unused.
24:27	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_AVG_FREQ_TSEL: Sample rate used by the AFSR[INST_CYCLE_SAMPLE] calculation, using the PPE timer, defined as $2^{(29\text{-select})}$ / Nest_Frequency. This field selects which timer output bit is used to sample the sample cycle counter. Note: The user must ensure that the value chosen never exceeds the equivalent of 2^{31} processor cycles; otherwise the sample will wrap and the calculation will be invalid. The default value for this register corresponds to 262 µs (assuming a 2 GHz processor bus).
28:31	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_SPARE_28_31: Implemented but unused.
32	WO_4P	NCX	WO_4P	CME_SCOM_LMCR_RESET_IMPRECISE_QERR: Reset the PCB queue imprecise error, to unlock the CME core SIB interface after an error occurs on a queued transaction.
33	WO_4P	NCX	WO_4P	CME_SCOM_LMCR_SET_ECC_INJECT_ERR: Write 1 to this bit causes an SRAM error to be injected by setting ECC_INJECT_ERR in the CME_SCOM_FWMR. **Note:** The ECC_INJECT_TYPE of error injected is only controllable by firmware in the CMEFWM.
34:62	RO	RO	RO	constant = 0b00000000000000000000000000000

Register Name	CME_SCOM CME Local Core Stop Interface Control Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_SICR
Address	000000001301203D (SCOM) 000000001301203E (SCOM1) 000000001301203F (SCOM2)
Description	CME_SCOM CME Local Core Stop Interface Control Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_PM_ENTRY_ACK_C0: Core 0 STOP entry acknowledgment to PC. **Note:** Output may also be asserted automatically for STOP level 1 or if the CME is halted as per LMCR bit 34.
1	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_PM_ENTRY_ACK_C1: Core 1 STOP entry acknowledgment to PC. **Note:** Output may also be asserted automatically for STOP level 1 or if the CME is halted as per LMCR bit 35.
2	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_PM_BLOCK_INTERRUPTS_C0: Core 0 block interrupts from allowing PC to start instructions in STOP state. **Note:** Output may also be asserted automatically for STOP level1 or if the CME is Halted as per LMCR bit 34.
3	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_PM_BLOCK_INTERRUPTS_C1: Core 1 block interrupts from allowing PC to start instructions in STOP state. **Note:** Output may also be asserted automatically for STOP level1 or if the CME is Halted as per LMCR bit 35.
4	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_PM_EXIT_C0: Core 0 request for PC to exit STOP state. **Note:** Output may also be asserted automatically for STOP level1 or if the CME is Halted as per LMCR bit 34.
5	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_PM_EXIT_C1: Core 1 request for PC to exit STOP state. **Note:** Output may also be asserted automatically for STOP level 1 or if the CME is Halted as per LMCR bit 35.
6	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_PCC_CORE_INTF_QUIESCE_C0: Core 0 processor common core logical fence.
7	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_PCC_CORE_INTF_QUIESCE_C1: Core 1 processor common core logical fence.
8	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_L2_CORE_INTF_QUIESCE_C0: Core 0 logical fence to the L2.
9	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_L2_CORE_INTF_QUIESCE_C1: Core 1 logical fence to the L2.
10	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_PCBMUX_REQ_C0: Core 0 PCB multiplexer request. See SISR for grant.
11	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_PCBMUX_REQ_C1: Core 1 PCB multiplexer request. See SISR for grant.
12:15	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_RESERVED_12_15: Implemented but unused.
16	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_SPECIAL_WKUP_DONE_C0: Connected to special wake-up done output to Core 0 PPM only when LMCR[SPECIAL_WAKEUP_DONE_OVERRIDE] = 1.
17	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_SPECIAL_WKUP_DONE_C1: Connected to special wake-up done output to Core 1 PPM only when LMCR[SPECIAL_WAKEUP_DONE_OVERRIDE] = 1.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
18	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_L2_PURGE: L2 purge request.
19	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_L2_PURGE_ABORT: L2 purge abort.
20	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_PC_THROTTLE_REQ: Requests PC to engage instruction throttling to both core chiplets.
21	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_NCU_TLBIE_QUIESCE: Request NCU to start ignoring new incoming TLBIEs.
22	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_NCU_PURGE: NCU purge request (needed for QUAD STOP states).
23	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_NCU_PURGE_ABORT: NCU purge abort (needed for QUAD STOP states).
24	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_CHTM_PURGE_C0: Core 0 CHTM purge request (needed for for QUAD STOP states).
25	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_CHTM_PURGE_C1: Core 1 CHTM purge request (needed for QUAD STOP states).
26	WO_4P	NC	WO_4P	CME_SCOM_SICR_HMI_REQUEST_C0: Pulse that sets a bit in core 0 HMER register to send an interrupt to the hypervisor. Intended for debug or workarounds.
27	WO_4P	NC	WO_4P	CME_SCOM_SICR_HMI_REQUEST_C1: Pulse that sets a bit in core 1 HMER register to send an interrupt to the hypervisor. Intended for debug or workarounds.
28	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_PPM_SPARE_OUT_C0: Spare output signal to Core 0 PPM.
29	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_PPM_SPARE_OUT_C1: Spare output signal to Core 1 PPM.
30:31	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_RESERVED_30_31: Implemented but unused.
32:63	RO	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	CME_SCOM Power Management Status Shadow Core0 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_PMSRS0
Address	0000000013012040 (SCOM)
Description	CME_SCOM Power Management Status Register Shadow Core0

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	CME_SCOM_PMSRS0_DATA: Meaning is defined by firmware usage. Intended to communicate information like actual Pstate, chip and system limits, and other power management state data back to the hypervisor.

Register Name	CME_SCOM Power Management Status Shadow Core1 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_PMSRS1
Address	0000000013012041 (SCOM)
Description	CME_SCOM Power Management Status Register Shadow Core1

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	CME_SCOM_PMSRS1_DATA: Meaning is defined by firmware usage. Intended to communicate information like actual Pstate, chip and system limits, and other power management state data back to the hypervisor.

Register Name	CME_SCOM Power Management Control Shadow Core0 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_PMCRS0
Address	0000000013012042 (SCOM)
Description	CME_SCOM Power Management Control Register Shadow Core0

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	CME_SCOM_PMCRS0_DATA: Meaning is defined by firmware usage. Intended to communicate Pstate requests and hints to power management firmware.

Register Name	CME_SCOM Power Management Control Shadow Core1 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_PMCRS1
Address	0000000013012043 (SCOM)
Description	CME_SCOM Power Management Control Register Shadow Core1

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	CME_SCOM_PMCRS1_DATA: Meaning is defined by firmware usage. Intended to communicate Pstate requests and hints to power management firmware.

Register Name	Processor Stop Control Core 0 Shadow Thread 0 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_PSCRS00
Address	0000000013012044 (SCOM)
Description	Processor Stop Control Register Core 0 Shadow Thread 0

Bits	SCOM	Field Mnemonic: Description
0	RWX	CME_SCOM_PSCRS00_SPARE0: Implemented but unused.
1	RWX	CME_SCOM_PSCRS00_OS_STATUS_DISABLE_A_N: OS status disable. Corresponds to PSSCR[41]. When '1' causes status field to return all zeros when read by OS.
2	RWX	CME_SCOM_PSCRS00_STATE_LOSS_ENABLE_A_N: Stop state loss enable. Corresponds to PSSCR[42]. When set, allows hardware to lose state, for example, allocate core resource to the remaining threads.
3	RWX	CME_SCOM_PSCRS00_EXIT_CRITERION_A_N: Stop exit criterion. Corresponds to PSSCR[43]. 0 = Exit power-saving mode on any interrupt without any state loss. 1 = Exit power-saving mode only on LPCR PECE conditions and take system reset interrupt with HV = 1; state loss is allowed and implementation-dependent.
4:7	RWX	CME_SCOM_PSCRS00_POWER_SAVING_LIMIT_A_N: Power-saving level limit. Corresponds to PSSCR[44:47]. Causes an OS stop request greater than or equal to this value to take an interrupt to the hypervisor instead.
8	RWX	CME_SCOM_PSCRS00_HYP_VIRT_EXIT_ENABLE: Hypervisor virtualization exit enable. Corresponds to PECE[17] and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.

Bits	SCOM	Field Mnemonic: Description
9	RWX	CME_SCOM_PSCRS00_EXT_EBB_EXIT_ENABLE: External event-based branch exit enable. Corresponds to PECE[18] and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
10	RWX	CME_SCOM_PSCRS00_EXT_RESUME_EXIT_ENABLE: External resume exit enable. Corresponds to PECE[19] and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
11	RWX	CME_SCOM_PSCRS00_EXT_EXIT_ENABLE: External OS exit enable. Corresponds to PECE[49] and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
12	RWX	CME_SCOM_PSCRS00_DEC_EXIT_ENABLE: Decrementer exit enable. Corresponds to PECE[50]. Unused by CME since this exit event is handled inside the core directly. Available to CME only for potential workarounds or sampling.
13	RWX	CME_SCOM_PSCRS00_HMI_EXIT_ENABLE: Hypervisor maintenance interrupt exit enable. Corresponds to PECE[51] and enables the malfunction alert interrupt source in WSR[32] to cause an exit from STOP state.
14:15	RWX	CME_SCOM_PSCRS00_LEVEL_TRANSITION_RATE_A_N: Stop level transition rate field. Corresponds to PSSCR[54:55]. The requested rate of progression from initial to maximum power-saving level if stop promote is implemented. Rate of progression increases with the value of level transition rate field actual rates corresponding to each value are defined by firmware and are TBD.
16:19	RWX	CME_SCOM_PSCRS00_MAX_PROMOTE_LEVEL_A_N: Maximum stop request level. Corresponds to PSSCR[56:59]. Allows hardware to auto-promote to deeper levels as the power-saved core ages (without waking up). Setting this field ≤ initial request level disables promotion. Setting this field to zero always disables auto-promotion. See STOP_REQUEST_LEVEL encoding in the following field.
20:23	RWX	CME_SCOM_PSCRS00_STOP_REQUEST_LEVEL_A_N: Stop request level. Corresponds to PSSCR[60:63]. 0x0 = Stop 0 (Quiesce thread only). 0x1 = Stop 1 (legacy nap). 0x2 = Stop 2 (legacy fast sleep). 0x3 = Stop 3 (if supported, legacy fast sleep @V_{min} using iVRMs). 0x4 = Stop 4 (instant-on; legacy deep sleep without HV loss). 0x5 - 0x7 = Reserved. 0x8 = Stop 8 (legacy deep sleep plus shared L2 clock off). 0x9 = Stop 9 (legacy fast winkle, for lab and simulation only). 0xA = Reserved. 0xB = Stop 11 (legacy deep winkle). 0xC - 0xF = Reserved.
24:63	RO	constant = 0b0000000000000000000000000000000000000000

Register Name	Processor Stop Control Core 0 Shadow Thread 1 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_PSCRS01
Address	0000000013012045 (SCOM)
Description	Processor Stop Control Register Core 0 Shadow Thread 1

Bits	SCOM	Field Mnemonic: Description
0	RWX	CME_SCOM_PSCRS01_SPARE0: Implemented but unused.
1	RWX	CME_SCOM_PSCRS01_OS_STATUS_DISABLE_A_N: OS status disable. Corresponds to PSSCR[41]. When '1' causes status field to return all 0's when read by OS.
2	RWX	CME_SCOM_PSCRS01_STATE_LOSS_ENABLE_A_N: Stop state loss enable. Corresponds to PSSCR[42]. When set, allows hardware to lose state, for example, allocate core resource to the remaining threads.

Bits	SCOM	Field Mnemonic: Description
3	RWX	CME_SCOM_PSCRS01_EXIT_CRITERION_A_N: Stop exit criterion. Corresponds to PSSCR[43]. 0 = Exit power-saving mode on any interrupt without any state loss. 1 = Exit power-saving mode only on LPCR PECE conditions and take system reset interrupt with HV = 1; state loss is allowed and implementation-dependent.
4:7	RWX	CME_SCOM_PSCRS01_POWER_SAVING_LIMIT_A_N: Power-saving level limit. Corresponds to PSSCR[44:47]. Causes an OS stop request greater than or equal to this value to take an interrupt to the hypervisor instead.
8	RWX	CME_SCOM_PSCRS01_HYP_VIRT_EXIT_ENABLE: Hypervisor virtualization exit enable. Corresponds to PECE[17] and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
9	RWX	CME_SCOM_PSCRS01_EXT_EBB_EXIT_ENABLE: External event-based branch exit enable. Corresponds to PECE[18] and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
10	RWX	CME_SCOM_PSCRS01_EXT_RESUME_EXIT_ENABLE: External resume exit enable. Corresponds to PECE[19] and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
11	RWX	CME_SCOM_PSCRS01_EXT_EXIT_ENABLE: External OS exit enable. Corresponds to PECE[49] and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
12	RWX	CME_SCOM_PSCRS01_DEC_EXIT_ENABLE: Decrementer exit enable. Corresponds to PECE[50]. Unused by CME since this exit event is handled inside the core directly. Available to CME only for potential workarounds or sampling.
13	RWX	CME_SCOM_PSCRS01_HMI_EXIT_ENABLE: Hypervisor maintenance interrupt exit enable. Corresponds to PECE[51] and enables the malfunction alert interrupt source in WSR[32] to cause an exit from STOP state.
14:15	RWX	CME_SCOM_PSCRS01_LEVEL_TRANSITION_RATE_A_N: Stop level transition rate field. Corresponds to PSSCR[54:55]. The requested rate of progression from initial to maximum power-saving level if stop promote is implemented. Rate of progression increases with the value of level transition rate field actual rates corresponding to each value are defined by firmware and are TBD.
16:19	RWX	CME_SCOM_PSCRS01_MAX_PROMOTE_LEVEL_A_N: Maximum stop request level. Corresponds to PSSCR[56:59]. Allows hardware to auto-promote to deeper levels as the power-saved core ages (without waking up). Setting this field ≤ initial request level disables promotion. Setting this field to zero always disables auto-promotion. See STOP_REQUEST_LEVEL encoding in the following field.
20:23	RWX	CME_SCOM_PSCRS01_STOP_REQUEST_LEVEL_A_N: Stop Request Level. Corresponds to PSSCR[60:63]. 0x0 = Stop 0 (Quiesce thread only). 0x1 = Stop 1 (legacy nap). 0x2 = Stop 2 (legacy fast sleep). 0x3 = Stop 3 (if supported, legacy fast sleep @V_{min} using iVRMs). 0x4 = Stop 4 (instant-on; legacy deep sleep without HV loss). 0x5 - 0x7 = Reserved. 0x8 = Stop 8 (legacy deep sleep plus shared L2 clock off). 0x9 = Stop 9 (legacy fast winkle, for lab and simulation only). 0xA = Reserved. 0xB = Stop 11 (legacy deep winkle). 0xC - 0xF = Reserved.
24:63	RO	constant = 0b0000000000000000000000000000000000000000

Register Name	Processor Stop Control Core 0 Shadow Thread 2 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_PSCRS02
Address	0000000013012046 (SCOM)
Description	Processor Stop Control Register Core 0 Shadow Thread 2

Bits	SCOM	Field Mnemonic: Description
0	RWX	CME_SCOM_PSCRS02_SPARE0: Implemented but unused.
1	RWX	CME_SCOM_PSCRS02_OS_STATUS_DISABLE_A_N: OS status disable. Corresponds to PSSCR[41]. When '1' causes status field to return all 0's when read by OS.
2	RWX	CME_SCOM_PSCRS02_STATE_LOSS_ENABLE_A_N: Stop state loss enable. Corresponds to PSSCR[42]. When set, allows hardware to lose state, for example, allocate core resource to the remaining threads.
3	RWX	CME_SCOM_PSCRS02_EXIT_CRITERION_A_N: Stop exit criterion. Corresponds to PSSCR[43]. 0 = Exit power-saving mode on any interrupt without any state loss. 1 = Exit power-saving mode only on LPCR PECE conditions and take system reset interrupt with HV = 1; state loss is allowed and implementation-dependent.
4:7	RWX	CME_SCOM_PSCRS02_POWER_SAVING_LIMIT_A_N: Power-saving level limit. Corresponds to PSSCR[44:47]. Causes an OS stop request greater than or equal to this value to take an interrupt to the hypervisor instead.
8	RWX	CME_SCOM_PSCRS02_HYP_VIRT_EXIT_ENABLE: Hypervisor virtualization exit enable. Corresponds to PECE[17] and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
9	RWX	CME_SCOM_PSCRS02_EXT_EBB_EXIT_ENABLE: External event-based branch exit enable. Corresponds to PECE[18] and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
10	RWX	CME_SCOM_PSCRS02_EXT_RESUME_EXIT_ENABLE: External resume exit enable. Corresponds to PECE[19] and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
11	RWX	CME_SCOM_PSCRS02_EXT_EXIT_ENABLE: External OS exit enable. Corresponds to PECE[49] and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
12	RWX	CME_SCOM_PSCRS02_DEC_EXIT_ENABLE: Decrementer exit enable. Corresponds to PECE[50]. Unused by CME since this exit event is handled inside the core directly. Available to CME only for potential workarounds or sampling.
13	RWX	CME_SCOM_PSCRS02_HMI_EXIT_ENABLE: Hypervisor maintenance interrupt exit enable. Corresponds to PECE[51] and enables the malfunction alert interrupt source in WSR[32] to cause an exit from STOP state.
14:15	RWX	CME_SCOM_PSCRS02_LEVEL_TRANSITION_RATE_A_N: Stop level transition rate field. Corresponds to PSSCR[54:55]. The requested rate of progression from initial to maximum power-saving level if stop promote is implemented. Rate of progression increases with the value of level transition rate field actual rates corresponding to each value are defined by firmware and are TBD.
16:19	RWX	CME_SCOM_PSCRS02_MAX_PROMOTE_LEVEL_A_N: Maximum stop request level. Corresponds to PSSCR[56:59]. Allows hardware to auto-promote to deeper levels as the power-saved core ages (without waking up). Setting this field ≤ initial request level disables promotion. Setting this field to zero always disables auto-promotion. See STOP_REQUEST_LEVEL encoding in the following field.
20:23	RWX	CME_SCOM_PSCRS02_STOP_REQUEST_LEVEL_A_N: Stop Request Level. Corresponds to PSSCR[60:63]. 0x0 = Stop 0 (Quiesce thread only). 0x1 = Stop 1 (legacy nap). 0x2 = Stop 2 (legacy fast sleep). 0x3 = Stop 3 (if supported, legacy fast sleep @V_{min} using iVRMs). 0x4 = Stop 4 (instant-on; legacy deep sleep without HV loss). 0x5 - 0x7 = Reserved. 0x8 = Stop 8 (legacy deep sleep plus shared L2 clock off). 0x9 = Stop 9 (legacy fast winkle, for lab and simulation only). 0xA = Reserved. 0xB = Stop 11 (legacy deep winkle). 0xC - 0xF = Reserved.

Bits	SCOM	Field Mnemonic: Description
24:63	RO	constant = 0b0000000000000000000000000000000000000000

Register Name	Processor Stop Control Core 0 Shadow Thread 3 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_PSCRS03
Address	0000000013012047 (SCOM)
Description	Processor Stop Control Register Core 0 Shadow Thread 3

Bits	SCOM	Field Mnemonic: Description
0	RWX	CME_SCOM_PSCRS03_SPARE0: Implemented but unused.
1	RWX	CME_SCOM_PSCRS03_OS_STATUS_DISABLE_A_N: OS status disable. Corresponds to PSSCR[41]. When '1' causes status field to return all 0's when read by OS.
2	RWX	CME_SCOM_PSCRS03_STATE_LOSS_ENABLE_A_N: Stop state loss enable. Corresponds to PSSCR[42]. When set, allows hardware to lose state, for example, allocate core resource to the remaining threads.
3	RWX	CME_SCOM_PSCRS03_EXIT_CRITERION_A_N: Stop exit criterion. Corresponds to PSSCR[43]. 0 = Exit power-saving mode on any interrupt without any state loss. 1 = Exit power-saving mode only on LPCR PECE conditions and take system reset interrupt with HV = 1; state loss is allowed and implementation-dependent.
4:7	RWX	CME_SCOM_PSCRS03_POWER_SAVING_LIMIT_A_N: Power-saving level limit. Corresponds to PSSCR[44:47]. Causes an OS stop request greater than or equal to this value to take an interrupt to the hypervisor instead.
8	RWX	CME_SCOM_PSCRS03_HYP_VIRT_EXIT_ENABLE: Hypervisor virtualization exit enable. Corresponds to PECE[17] and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
9	RWX	CME_SCOM_PSCRS03_EXT_EBB_EXIT_ENABLE: External event-based branch exit enable. Corresponds to PECE[18] and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
10	RWX	CME_SCOM_PSCRS03_EXT_RESUME_EXIT_ENABLE: External resume exit enable. Corresponds to PECE[19] and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
11	RWX	CME_SCOM_PSCRS03_EXT_EXIT_ENABLE: External OS exit enable. Corresponds to PECE[49] and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
12	RWX	CME_SCOM_PSCRS03_DEC_EXIT_ENABLE: Decrementer exit enable. Corresponds to PECE[50]. Unused by CME since this exit event is handled inside the core directly. Available to CME only for potential workarounds or sampling.
13	RWX	CME_SCOM_PSCRS03_HMI_EXIT_ENABLE: Hypervisor maintenance interrupt exit enable. Corresponds to PECE[51] and enables the malfunction alert interrupt source in WSR[32] to cause an exit from STOP state.
14:15	RWX	CME_SCOM_PSCRS03_LEVEL_TRANSITION_RATE_A_N: Stop level transition rate field. Corresponds to PSSCR[54:55]. The requested rate of progression from initial to maximum power-saving level if stop promote is implemented. Rate of progression increases with the value of level transition rate field actual rates corresponding to each value are defined by firmware and are TBD.
16:19	RWX	CME_SCOM_PSCRS03_MAX_PROMOTE_LEVEL_A_N: Maximum stop request level. Corresponds to PSSCR[56:59]. Allows hardware to auto-promote to deeper levels as the power-saved core ages (without waking up). Setting this field ≤ initial request level disables promotion. Setting this field to zero always disables auto-promotion. See STOP_REQUEST_LEVEL encoding in the following field.

Bits	SCOM	Field Mnemonic: Description
20:23	RWX	CME_SCOM_PSCRS03_STOP_REQUEST_LEVEL_A_N: Stop Request Level. Corresponds to PSSCR[60:63]. 0x0 = Stop 0 (Quiesce thread only). 0x1 = Stop 1 (legacy nap). 0x2 = Stop 2 (legacy fast sleep). 0x3 = Stop 3 (if supported, legacy fast sleep @V_{min} using iVRMs). 0x4 = Stop 4 (instant-on; legacy deep sleep without HV loss). 0x5 - 0x7 = Reserved. 0x8 = Stop 8 (legacy deep sleep plus shared L2 clock off). 0x9 = Stop 9 (legacy fast winkle, for lab and simulation only). 0xA = Reserved. 0xB = Stop 11 (legacy deep winkle). 0xC - 0xF = Reserved.
24:63	RO	constant = 0b0000000000000000000000000000000000000000

Register Name	Processor Stop Control Core 1 Shadow Thread 0 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_PSCRS10
Address	0000000013012048 (SCOM)
Description	Processor Stop Control Register Core 1 Shadow Thread 0

Bits	SCOM	Field Mnemonic: Description
0	RWX	CME_SCOM_PSCRS10_SPARE0: Implemented but unused.
1	RWX	CME_SCOM_PSCRS10_OS_STATUS_DISABLE_A_N: OS status disable. Corresponds to PSSCR[41]. When '1' causes status field to return all 0's when read by OS.
2	RWX	CME_SCOM_PSCRS10_STATE_LOSS_ENABLE_A_N: Stop state loss enable. Corresponds to PSSCR[42]. When set, allows hardware to lose state, for example, allocate core resource to the remaining threads.
3	RWX	CME_SCOM_PSCRS10_EXIT_CRITERION_A_N: Stop Exit Criterion. Corresponds to PSSCR[43]. 0 = Exit power-saving mode on any interrupt without any state loss. 1 = Exit power-saving mode only on LPCR PECE conditions and take system reset interrupt with HV = 1; state loss is allowed and implementation-dependent.
4:7	RWX	CME_SCOM_PSCRS10_POWER_SAVING_LIMIT_A_N: Power-saving level limit. Corresponds to PSSCR[44:47]. Causes an OS stop request greater than or equal to this value to take an interrupt to the hypervisor instead.
8	RWX	CME_SCOM_PSCRS10_HYP_VIRT_EXIT_ENABLE: Hypervisor virtualization exit enable. Corresponds to PECE[17] and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
9	RWX	CME_SCOM_PSCRS10_EXT_EBB_EXIT_ENABLE: External event-based branch exit enable. Corresponds to PECE[18] and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
10	RWX	CME_SCOM_PSCRS10_EXT_RESUME_EXIT_ENABLE: External resume exit enable. Corresponds to PECE[19] and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
11	RWX	CME_SCOM_PSCRS10_EXT_EXIT_ENABLE: External OS exit enable. Corresponds to PECE[49] and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
12	RWX	CME_SCOM_PSCRS10_DEC_EXIT_ENABLE: Decrementer exit enable. Corresponds to PECE[50]. Unused by CME since this exit event is handled inside the core directly. Available to CME only for potential workarounds or sampling.
13	RWX	CME_SCOM_PSCRS10_HMI_EXIT_ENABLE: Hypervisor maintenance interrupt exit enable. Corresponds to PECE[51] and enables the malfunction alert interrupt source in WSR[32] to cause an exit from STOP state.

Bits	SCOM	Field Mnemonic: Description
14:15	RWX	CME_SCOM_PSCRS10_LEVEL_TRANSITION_RATE_A_N: Stop level transition rate field. Corresponds to PSSCR[54:55]. The requested rate of progression from initial to maximum power-saving level if stop promote is implemented. Rate of progression increases with the value of level transition rate field actual rates corresponding to each value are defined by firmware and are TBD.
16:19	RWX	CME_SCOM_PSCRS10_MAX_PROMOTE_LEVEL_A_N: Maximum stop request level. Corresponds to PSSCR[56:59]. Allows hardware to auto-promote to deeper levels as the power-saved core ages (without waking up). Setting this field ≤ initial request level disables promotion. Setting this field to zero always disables auto-promotion. See STOP_REQUEST_LEVEL encoding in the following field.
20:23	RWX	CME_SCOM_PSCRS10_STOP_REQUEST_LEVEL_A_N: Stop Request Level. Corresponds to PSSCR[60:63]. 0x0 = Stop 0 (Quiesce thread only). 0x1 = Stop 1 (legacy nap). 0x2 = Stop 2 (legacy fast sleep). 0x3 = Stop 3 (if supported, legacy fast sleep @V_{min} using iVRMs). 0x4 = Stop 4 (instant-on; legacy deep sleep without HV loss). 0x5 - 0x7 = Reserved. 0x8 = Stop 8 (legacy deep sleep plus shared L2 clock off). 0x9 = Stop 9 (legacy fast winkle, for lab and simulation only). 0xA = Reserved. 0xB = Stop 11 (legacy deep winkle). 0xC - 0xF = Reserved.
24:63	RO	constant = 0b0000000000000000000000000000000000000000

Register Name	Processor Stop Control Core 1 Shadow Thread 1 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_PSCRS11
Address	0000000013012049 (SCOM)
Description	Processor Stop Control Register Core 1 Shadow Thread 1

Bits	SCOM	Field Mnemonic: Description
0	RWX	CME_SCOM_PSCRS11_SPARE0: Implemented but unused.
1	RWX	CME_SCOM_PSCRS11_OS_STATUS_DISABLE_A_N: OS status disable. Corresponds to PSSCR[41]. When '1' causes status field to return all 0's when read by OS.
2	RWX	CME_SCOM_PSCRS11_STATE_LOSS_ENABLE_A_N: Stop state loss enable. Corresponds to PSSCR[42]. When set, allows hardware to lose state, for example, allocate core resource to the remaining threads.
3	RWX	CME_SCOM_PSCRS11_EXIT_CRITERION_A_N: Stop exit criterion. Corresponds to PSSCR[43]. 0 = Exit power-saving mode on any interrupt without any state loss. 1 = Exit power-saving mode only on LPCR PECE conditions and take system reset interrupt with HV = 1; state loss is allowed and implementation-dependent.
4:7	RWX	CME_SCOM_PSCRS11_POWER_SAVING_LIMIT_A_N: Power-saving level limit. Corresponds to PSSCR[44:47]. Causes an OS stop request greater than or equal to this value to take an interrupt to the hypervisor instead.
8	RWX	CME_SCOM_PSCRS11_HYP_VIRT_EXIT_ENABLE: Hypervisor virtualization exit enable. Corresponds to PECE[17] and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
9	RWX	CME_SCOM_PSCRS11_EXT_EBB_EXIT_ENABLE: External event-based branch exit enable. Corresponds to PECE[18] and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
10	RWX	CME_SCOM_PSCRS11_EXT_RESUME_EXIT_ENABLE: External resume exit enable. Corresponds to PECE[19] and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.

Bits	SCOM	Field Mnemonic: Description
11	RWX	CME_SCOM_PSCRS11_EXT_EXIT_ENABLE: External OS exit enable. Corresponds to PECE[49] and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
12	RWX	CME_SCOM_PSCRS11_DEC_EXIT_ENABLE: Decrementer exit enable. Corresponds to PECE[50]. Unused by CME since this exit event is handled inside the core directly. Available to CME only for potential workarounds or sampling.
13	RWX	CME_SCOM_PSCRS11_HMI_EXIT_ENABLE: Hypervisor maintenance interrupt exit enable. Corresponds to PECE[51] and enables the malfunction alert interrupt source in WSR[32] to cause an exit from STOP state.
14:15	RWX	CME_SCOM_PSCRS11_LEVEL_TRANSITION_RATE_A_N: Stop level transition rate field. Corresponds to PSSCR[54:55]. The requested rate of progression from initial to maximum power-saving level if stop promote is implemented. Rate of progression increases with the value of level transition rate field actual rates corresponding to each value are defined by firmware and are TBD.
16:19	RWX	CME_SCOM_PSCRS11_MAX_PROMOTE_LEVEL_A_N: Maximum stop request level. Corresponds to PSSCR[56:59]. Allows hardware to auto-promote to deeper levels as the power-saved core ages (without waking up). Setting this field ≤ initial request level disables promotion. Setting this field to zero always disables auto-promotion. See STOP_REQUEST_LEVEL encoding in the following field.
20:23	RWX	CME_SCOM_PSCRS11_STOP_REQUEST_LEVEL_A_N: Stop Request Level. Corresponds to PSSCR[60:63]. 0x0 = Stop 0 (Quiesce thread only). 0x1 = Stop 1 (legacy nap). 0x2 = Stop 2 (legacy fast sleep). 0x3 = Stop 3 (if supported, legacy fast sleep @V_{min} using iVRMs). 0x4 = Stop 4 (instant-on; legacy deep sleep without HV loss). 0x5 - 0x7 = Reserved. 0x8 = Stop 8 (legacy deep sleep plus shared L2 clock off). 0x9 = Stop 9 (legacy fast winkle, for lab and simulation only). 0xA = Reserved. 0xB = Stop 11 (legacy deep winkle). 0xC - 0xF = Reserved.
24:63	RO	constant = 0b0000000000000000000000000000000000000000

Register Name	Processor Stop Control Core 1 Shadow Thread 2 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_PSCRS12
Address	000000001301204A (SCOM)
Description	Processor Stop Control Register Core 1 Shadow Thread 2

Bits	SCOM	Field Mnemonic: Description
0	RWX	CME_SCOM_PSCRS12_SPARE0: Implemented but unused.
1	RWX	CME_SCOM_PSCRS12_OS_STATUS_DISABLE_A_N: OS status disable. Corresponds to PSSCR[41]. When '1' causes status field to return all 0's when read by OS.
2	RWX	CME_SCOM_PSCRS12_STATE_LOSS_ENABLE_A_N: Stop state loss enable. Corresponds to PSSCR[42]. When set, allows hardware to lose state, for example, allocate core resource to the remaining threads.
3	RWX	CME_SCOM_PSCRS12_EXIT_CRITERION_A_N: Stop exit criterion. Corresponds to PSSCR[43]. 0 = Exit power-saving mode on any interrupt without any state loss. 1 = Exit power-saving mode only on LPCR PECE conditions and take system reset interrupt with HV = 1; state loss is allowed and implementation-dependent.
4:7	RWX	CME_SCOM_PSCRS12_POWER_SAVING_LIMIT_A_N: Power-saving level limit. Corresponds to PSSCR[44:47]. Causes an OS stop request greater than or equal to this value to take an interrupt to the hypervisor instead.

Bits	SCOM	Field Mnemonic: Description
8	RWX	CME_SCOM_PSCRS12_HYP_VIRT_EXIT_ENABLE: Hypervisor virtualization exit enable. Corresponds to PECE[17] and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
9	RWX	CME_SCOM_PSCRS12_EXT_EBB_EXIT_ENABLE: External event-based branch exit enable. Corresponds to PECE[18] and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
10	RWX	CME_SCOM_PSCRS12_EXT_RESUME_EXIT_ENABLE: External resume exit enable. Corresponds to PECE[19] and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
11	RWX	CME_SCOM_PSCRS12_EXT_EXIT_ENABLE: External OS exit enable. Corresponds to PECE[49] and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
12	RWX	CME_SCOM_PSCRS12_DEC_EXIT_ENABLE: Decrementer exit enable. Corresponds to PECE[50]. Unused by CME since this exit event is handled inside the core directly. Available to CME only for potential workarounds or sampling.
13	RWX	CME_SCOM_PSCRS12_HMI_EXIT_ENABLE: Hypervisor maintenance interrupt exit enable. Corresponds to PECE[51] and enables the malfunction alert interrupt source in WSR[32] to cause an exit from STOP state.
14:15	RWX	CME_SCOM_PSCRS12_LEVEL_TRANSITION_RATE_A_N: Stop level transition rate field. Corresponds to PSSCR[54:55]. The requested rate of progression from initial to maximum power-saving level if stop promote is implemented. Rate of progression increases with the value of level transition rate field actual rates corresponding to each value are defined by firmware and are TBD.
16:19	RWX	CME_SCOM_PSCRS12_MAX_PROMOTE_LEVEL_A_N: Maximum stop request level. Corresponds to PSSCR[56:59]. Allows hardware to auto-promote to deeper levels as the power-saved core ages (without waking up). Setting this field ≤ initial request level disables promotion. Setting this field to zero always disables auto-promotion. See STOP_REQUEST_LEVEL encoding in the following field.
20:23	RWX	CME_SCOM_PSCRS12_STOP_REQUEST_LEVEL_A_N: Stop Request Level. Corresponds to PSSCR[60:63]. 0x0 = Stop 0 (Quiesce thread only). 0x1 = Stop 1 (legacy nap). 0x2 = Stop 2 (legacy fast sleep). 0x3 = Stop 3 (if supported, legacy fast sleep @V_{min} using iVRMs). 0x4 = Stop 4 (instant-on; legacy deep sleep without HV loss). 0x5 - 0x7 = Reserved. 0x8 = Stop 8 (legacy deep sleep plus shared L2 clock off). 0x9 = Stop 9 (legacy fast winkle, for lab and simulation only). 0xA = Reserved. 0xB = Stop 11 (legacy deep winkle). 0xC - 0xF = Reserved.
24:63	RO	constant = 0b0000000000000000000000000000000000000000

Register Name	Processor Stop Control Core 1 Shadow Thread 3 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_SCOM_PSCRS13
Address	000000001301204B (SCOM)
Description	Processor Stop Control Register Core 1 Shadow Thread 3

Bits	SCOM	Field Mnemonic: Description
0	RWX	CME_SCOM_PSCRS13_SPARE0: Implemented but unused.
1	RWX	CME_SCOM_PSCRS13_OS_STATUS_DISABLE_A_N: OS status disable. Corresponds to PSSCR[41]. When '1' causes status field to return all 0's when read by OS.
2	RWX	CME_SCOM_PSCRS13_STATE_LOSS_ENABLE_A_N: Stop state loss enable. Corresponds to PSSCR[42]. When set, allows hardware to lose state, for example, allocate core resource to the remaining threads.

Bits	SCOM	Field Mnemonic: Description
3	RWX	CME_SCOM_PSCRS13_EXIT_CRITERION_A_N: Stop Exit Criterion. Corresponds to PSSCR[43]. 0 = Exit power-saving mode on any interrupt without any state loss. 1 = Exit power-saving mode only on LPCR PECE conditions and take system reset interrupt with HV = 1; state loss is allowed and implementation-dependent.
4:7	RWX	CME_SCOM_PSCRS13_POWER_SAVING_LIMIT_A_N: Power-saving level limit. Corresponds to PSSCR[44:47]. Causes an OS stop request greater than or equal to this value to take an interrupt to the hypervisor instead.
8	RWX	CME_SCOM_PSCRS13_HYP_VIRT_EXIT_ENABLE: Hypervisor virtualization exit enable. Corresponds to PECE[17] and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
9	RWX	CME_SCOM_PSCRS13_EXT_EBB_EXIT_ENABLE: External event-based branch exit enable. Corresponds to PECE[18] and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
10	RWX	CME_SCOM_PSCRS13_EXT_RESUME_EXIT_ENABLE: External resume exit enable. Corresponds to PECE[19] and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
11	RWX	CME_SCOM_PSCRS13_EXT_EXIT_ENABLE: External OS exit enable. Corresponds to PECE[49] and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
12	RWX	CME_SCOM_PSCRS13_DEC_EXIT_ENABLE: Decrementer exit enable. Corresponds to PECE[50]. Unused by CME since this exit event is handled inside the core directly. Available to CME only for potential workarounds or sampling.
13	RWX	CME_SCOM_PSCRS13_HMI_EXIT_ENABLE: Hypervisor maintenance interrupt exit enable. Corresponds to PECE[51] and enables the malfunction alert interrupt source in WSR[32] to cause an exit from STOP state.
14:15	RWX	CME_SCOM_PSCRS13_LEVEL_TRANSITION_RATE_A_N: Stop level transition rate field. Corresponds to PSSCR[54:55]. The requested rate of progression from initial to maximum power-saving level if stop promote is implemented. Rate of progression increases with the value of level transition rate field actual rates corresponding to each value are defined by firmware and are TBD.
16:19	RWX	CME_SCOM_PSCRS13_MAX_PROMOTE_LEVEL_A_N: Maximum stop request level. Corresponds to PSSCR[56:59]. Allows hardware to auto-promote to deeper levels as the power-saved core ages (without waking up). Setting this field ≤ initial request level disables promotion. Setting this field to zero always disables auto-promotion. See STOP_REQUEST_LEVEL encoding in the following field.
20:23	RWX	CME_SCOM_PSCRS13_STOP_REQUEST_LEVEL_A_N: Stop Request Level. Corresponds to PSSCR[60:63]. 0x0 = Stop 0 (Quiesce thread only). 0x1 = Stop 1 (legacy nap). 0x2 = Stop 2 (legacy fast sleep). 0x3 = Stop 3 (if supported, legacy fast sleep @V_{min} using iVRMs). 0x4 = Stop 4 (instant-on; legacy deep sleep without HV loss). 0x5 - 0x7 = Reserved. 0x8 = Stop 8 (legacy deep sleep plus shared L2 clock off). 0x9 = Stop 9 (legacy fast winkle, for lab and simulation only). 0xA = Reserved. 0xB = Stop 11 (legacy deep winkle). 0xC - 0xF = Reserved.
24:63	RO	constant = 0b0000000000000000000000000000000000000000

Register Name	CME_LCL CME Local Stop Interface Status Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_LCL_SISR
Address	000000001301204C (SCOM)
Description	CME_LCL CME Local Stop Interface Status Register

Bits	SCOM	Field Mnemonic: Description
0	ROX	CME_LCL_SISR_PM_ENTRY_ACK_C0_ACTUAL: Actual value being driven on the CME output to Core 0 PC after all overrides have been applied.
1	ROX	CME_LCL_SISR_PM_ENTRY_ACK_C1_ACTUAL: Actual value being driven on the CME output to Core 1 PC after all overrides have been applied.
2	ROX	CME_LCL_SISR_PM_BLOCK_INTERRUPTS_C0_ACTUAL: Actual value being driven on the CME output to Core 0 PC after all overrides have been applied.
3	ROX	CME_LCL_SISR_PM_BLOCK_INTERRUPTS_C1_ACTUAL: Actual value being driven on the CME output to Core 1 PC after all overrides have been applied.
4	ROX	CME_LCL_SISR_PM_EXIT_C0_ACTUAL: Actual value being driven on the CME output to Core 0 PC after all overrides have been applied.
5	ROX	CME_LCL_SISR_PM_EXIT_C1_ACTUAL: Actual value being driven on the CME output to Core 1 PC after all overrides have been applied.
6:8	ROX	CME_LCL_SISR_RESERVED_6_8: Not implemented.
9	ROX	CME_LCL_SISR_PC_FUSED_CORE_MODE: Input signal indicating the system is in fused core mode. **Note:** This bit is not valid (will be zero) when the L2 domain (which includes PC common core) is fenced.
10	ROX	CME_LCL_SISR_PCBMUX_GRANT_C0: Core 0 PCB multiplexer grant. See SICR for request.
11	ROX	CME_LCL_SISR_PCBMUX_GRANT_C1: Core 1 PCB multiplexer grant. See SICR for request.
12:15	ROX	CME_LCL_SISR_RESERVED_12_15: Not implemented.
16	ROX	CME_LCL_SISR_SPECIAL_WAKEUP_DONE_C0_ACTUAL: Actual value being driven on the CME output to C0PPM after all overrides have been applied.
17	ROX	CME_LCL_SISR_SPECIAL_WAKEUP_DONE_C1_ACTUAL: Actual value being driven on the CME output to C1PPM after all overrides have been applied.
18:29	ROX	CME_LCL_SISR_RESERVED_18_29: Not implemented.

Bits	SCOM	Field Mnemonic: Description
30:31	ROX	CME_LCL_SISR_L2_INTF_QUIESCE_DONE_LVL_0_1: Indicates the L2 interface is quiesced per core.
32	ROX	CME_LCL_SISR_PC_UNMASKED_ATTN_C0: Core 0 Unmasked special attention indication.
33	ROX	CME_LCL_SISR_PC_UNMASKED_ATTN_C1: Core 1 Unmasked special attention indication.
34	ROX	CME_LCL_SISR_PM_STATE_ACTIVE_C0: Core 0 PM state active (raw value from PC). **Note:** May also conditionally cause an external interrupt.
35	ROX	CME_LCL_SISR_PM_STATE_ACTIVE_C1: Core 1 PM state active (raw value from PC). **Note:** May also conditionally cause an external interrupt.
36:39	ROX	CME_LCL_SISR_PM_STATE_C0: Core 0 PM state (stop level).
40:43	ROX	CME_LCL_SISR_PM_STATE_C1: Core 1 PM state (stop level).
44	ROX	CME_LCL_SISR_PM_STATE_ALL_HV_C0: Core 0 all threads in HV state.
45	ROX	CME_LCL_SISR_PM_STATE_ALL_HV_C1: Core 1 all threads in HV state.
46	ROX	CME_LCL_SISR_PC_INSTR_RUNNING_C0: Core 0 instructions running on at least one thread.
47	ROX	CME_LCL_SISR_PC_INSTR_RUNNING_C1: Core 1 instructions running on at least one thread.
48:51	ROX	CME_LCL_SISR_PC_NON_HV_RUNNING_C0: Core 0 per thread 0..3 indication if it is running in non-HV mode (used only for instant-on latency measurement).
52:55	ROX	CME_LCL_SISR_PC_NON_HV_RUNNING_C1: Core 1 per thread 0..3 indication if it is running in non-HV mode.
56	ROX	CME_LCL_SISR_ALLOW_REG_WAKEUP_C0: Core 0 PPM allow regular wake-up (control for OCC power shifting).
57	ROX	CME_LCL_SISR_ALLOW_REG_WAKEUP_C1: Core 1 PPM allow regular wake-up (control for OCC power shifting).
58:63	RO	constant = 0b000000

Register Name	CME_LCL Inter-CME Local Communication Receive Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CME.CME_LCL_ICRR
Address	000000001301204D (SCOM)
Description	CME local communication receive register

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	CME_LCL_ICRR_CME_COMM_RECV: Data received from partner CME.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	HTM Collection Mode Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CHTMLBS0.CHTM.SC.HTM_MODE
Address	0000000013012200 (SCOM)
Description	HTM collection mode register

Bits	SCOM	Field Mnemonic: Description
0	RW	HTMSC_MODE_HTM_ENABLE: HTM enable. Set by software to start HTM trace.
1:2	RW	HTMSC_MODE_CONTENT_SEL: HTM content selection mode: Core instruction trace, LLAT trace, PPE trace, or Direct Memory Write.
3	RW	HTMSC_MODE_SPARE0: Unused bit.

Bits	SCOM	Field Mnemonic: Description
4:9	RW	HTMSC_MODE_CAPTURE: HTM capture mode(0:5) has different meanings based on the value of the content selection mode: When htm_mode_q(1 TO 2) == 00, that is, Core Instruction Trace. 00xxxx = tc_pc_trace_active asserted when HTM_STAT[Tracing] = 1 to purge the ERAT when entering and exiting trace. 01xxxx = tc_pc_trace_active asserted when HTM_MODE[HTM_Trace_enable] = 1 to purge the ERAT only at the beginning. When htm_mode_q(1 TO 2) == 01, that is, LLAT Trace. 0xxxxx = capture on assertion of l2_htm_llat_disp_req, that is, any dispatch request. 1xxxxx = capture on assertion of l2_htm_llat_disp_req AND l2_llat_htm_rcdisp_occurred, that is, only on passed dispatch. x0xxxx = capture on assertion of l2_htm_llat_disp_req, that is, loads or stores. x1xxxx = capture on assertion of l2_htm_llat_disp_req AND l2_llat_htm_rcdisp_ld_not_st, that is, only loads. xx0xxx = capture on assertion of l2_llat_htm_pbl3hit_dval. xx1xxx = no capture on assertion of l2_llat_htm_pbl3hit_dval - enable embedded time stamp. When htm_mode_q(1 TO 2) == 11, that is, Direct Memory Write. 1xxxxx = Enable HPMC-IMA Mode.
10	RW	HTMSC_MODE_DD1EQUIV: POWER8 processor with NVLink technology DD1equiv for purge done not asserted bug HW238754.
11:12	RW	HTMSC_MODE_SPARE_1TO2: Spare bits.
13	RW	HTMSC_MODE_WRAP: 0 = Stop trace when it reaches the top of trace memory. 1 = Continue trace until a stop trigger is received. Trace wraps to the beginning of trace memory when the top has been reached.
14	RW	HTMSC_MODE_DIS_TSTAMP: 0 = Writing of time stamps is enabled. 1 = Writing of time stamps is disabled.
15	RW	HTMSC_MODE_SINGLE_TSTAMP: 0 = Additional time stamp written on timer overflow. 1 = Time stamp only before new record (if enabled).
16	RW	HTMSC_MODE_DIS_STALL: 0 = Core execution stalls when buffer full, Core Trace only. 1 = Core instruction trace stall disabled.
17	RW	HTMSC_MODE_MARKERS_ONLY: 0 = Normal trace. 1 = Ave only markers and enabled stamps.
18	RW	HTMSC_MODE_DIS_GROUP: 0 = Send cmd as programmed. Convert nodal to group scope. 1 = If programmed to group or nodal, send as VGs.
19:23	RW	HTMSC_MODE_SPARES: Spares.
24:39	RW	HTMSC_MODE_VGTARGET: VG target bits used in VGs mode.
40:63	RO	constant = 0b000000000000000000000000

Register Name	HTM Trace Memory Configuration Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CHTMLBS0.CHTM.SC.HTM_MEM
Address	0000000013012201 (SCOM)
Description	HTM Trace Memory Configuration Register

Bits	SCOM	Field Mnemonic: Description
0	RW	HTMSC_MEM_ALLOC: 0 = Memory based address not configured. 1 = Memory address configured. This bit must be written to zero before setting since the HTM looks for the 0->1 transition to indicate the memory address has been updated.
1:3	RW	HTMSC_MEM_SCOPE: Configure the scope used when writing the HTM trace memory. If the scope is not large enough, the HTM will get an address error. If the scope is too large, HTM will experience excessive delay. Set scope to system if CHTM memory is on foreign link.
4	RW	HTMSC_MEM_PRIORITY: Configure the starting priority used when writing the HTM trace memory.
5	RW	HTMSC_MEM_SIZE_SMALL: 0 = Trace memory size from 512 MB to 256 GB. 1 = Trace memory size from 16 MB to 8 GB.
6:7	RW	HTMSC_MEM_SPARE: Spare bits.
8:39	RW	HTMSC_MEM_BASE: Trace memory base address (8:39). The trace memory base address must be aligned on a Trace Memory Size boundary.

Bits	SCOM	Field Mnemonic: Description
40:48	RW	HTMSC_MEM_SIZE: When htmsc_mem_size_small = 0, these bits define the mask to bits (26:35) of the trace memory base address and define the size of the trace memory between 512 MB and 256 GB. When htmsc_mem_size_small = 1, these bits define the mask to bits (31:39) of the trace memory base address and define the size of the trace memory between 16 MB and 8 GB.
49:56	RO	constant = 0b00000000

Register Name	HTM Trace Status Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CHTMLBS0.CHTM.SC.HTM_STAT
Address	0000000013012202 (SCOM)
Description	HTM Trace Status Register

Bits	SCOM	Field Mnemonic: Description
0	ROX	HTMCO_STATUS_PURGE_IN_PROG: Purge in progress.
1	ROX	HTMCO_STATUS_PURGE_DONE: Purge done.
2	ROX	HTMCO_STATUS_CRESP_OV: Not set in CHTM.
3	ROX	HTMCO_STATUS_REPAIR: Address repair. Asserted on occurrence of address error to indicate the need of software to clear and update HTM_MEM. Will stay high until HTM_MEM updated.
4	ROX	HTMCO_STATUS_BUF_WAIT: Buffer waiting. Asserted on condition of data buffers full in tracing state. Any markers, stamps, and trace data will be lost.
5	ROX	STATUS_TRIG_DROPPED_Q: Buffer Overrun Trigger. Asserted on buffer overrun due to trigger lost. Cleared on the writing of 1 to the reset trigger bit, htmsc_trig_reset.
6	ROX	HTMCO_STATUS_ADDR_ERROR: Address error. Asserted on address error when write buffer was allocated. Need to set new address range.
7	ROX	STATUS_REC_DROPPED_Q: Buffer Overrun data. Asserted on buffer overrun due to trace data lost. Cleared on the writing of 1 to the reset trigger bit, htmsc_trig_reset.
8	ROX	HTMCO_STATUS_INIT: Asserted when htm_cofsm is in Init state.
9	ROX	HTMCO_STATUS_PREREQ: Asserted when htm_cofsm is in Pre-req state.
10	ROX	HTMCO_STATUS_READY: Asserted when htm_cofsm is in Ready state.
11	ROX	HTMCO_STATUS_TRACING: Asserted when htm_cofsm is in Tracing state.
12	ROX	HTMCO_STATUS_PAUSED: Asserted when htm_cofsm is in Paused state.
13	ROX	HTMCO_STATUS_FLUSH: Asserted when htm_cofsm is in Flush state.
14	ROX	HTMCO_STATUS_COMPLETE: Asserted when htm_cofsm is in Complete state.
15	ROX	HTMCO_STATUS_ENABLE: Asserted when htm_cofsm is in Enable state.
16	ROX	HTMCO_STATUS_STAMP: Asserted when htm_cofsm is in Stamp state.
17	ROX	STATUS_SCOM_ERROR: SCOM ERROR: Asserted to indicate to the HTM that a SCOM error indication was received from the SCOM satellite. Cleared on the writing of 1 to the reset trigger bit, htmsc_trig_reset.
18:19	ROX	STATUS_UNUSED: NHTM only. Unused in CHTM.
20:63	RO	constant = 0b00000000000000000000000000000000000000000000

Register Name	**HTM Last Address Register**
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CHTMLBS0.CHTM.SC.HTM_LAST
Address	0000000013012203 (SCOM)
Description	HTM Last Address Register

Bits	**SCOM**	**Field Mnemonic: Description**
0:7	RO	constant = 0b00000000
8:56	ROX	HTM_LAST_ADDRESS: The last cache line address of the memory trace. Valid only when HTM is in the complete state.
57:63	RO	constant = 0b0000000

Register Name	**HTM SCOM Trigger Register**
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CHTMLBS0.CHTM.SC.HTM_TRIG
Address	0000000013012204 (SCOM)
Description	HTM SCOM Trigger Register

Bits	**SCOM**	**Field Mnemonic: Description**
0	RW	HTMSC_TRIG_START: Start trigger.
1	RW	HTMSC_TRIG_STOP: Stop trigger.
2	RW	HTMSC_TRIG_PAUSE: Pause trigger.
3	RW	HTMSC_TRIG_STOP_ALT: Stop trigger 2. Legacy bit that used to be the freeze trigger in POWER6 implementation.
4	RW	HTMSC_TRIG_RESET: Reset trigger.
5	RW	HTMSC_TRIG_MARK_VALID: Mark type valid.
6:15	RW	HTMSC_TRIG_MARK_TYPE: Mark type is put into mark record when bit 5 is set.
16:63	RO	constant = 0b000000000000000000000000000000000000000000000000

Register Name	**HTM Trigger Control Register**
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CHTMLBS0.CHTM.SC.HTM_CTRL
Address	0000000013012205 (SCOM)
Description	HTM Trigger Control Register

Bits	**SCOM**	**Field Mnemonic: Description**
0:1	RW	HTMSC_CTRL_TRIG: Local trigger forwarding. 00 = Local triggers are not forwarded to the processor bus; they are inserted into the trace when tracing. Both local and global triggers control the HTM. 01 = Local triggers are not forwarded to the processor bus; they are inserted into the trace when tracing. Only local triggers control the HTM. 1x = Local triggers are forwarded to the processor bus; they are not inserted into the trace when tracing. Only global triggers control the HTM.
2	RW	HTMSC_CTRL_MTSPR_TRIG: MTSPR trigger control. 0 = Ignore MTSPR trace triggers. 1 = Treat MTSPR trace triggers as local triggers.

Bits	SCOM	Field Mnemonic: Description
3	RW	HTMSC_CTRL_MTSPR_MARK: MTSPR marker control. 0 = Ignore MTSPR trace markers. 1 = Treat MTSPR trace markers as local markers.
4:5	RW	HTMSC_CTRL_MARK: MTSPR marker forwarding/insertion. 00 = Local markers are not forwarded to the processor bus. Both local and global markers are inserted into the trace. 01 = Local markers are not forwarded to the processor bus. Only local markers are inserted into the trace. 10 = Local markers are forwarded to the processor bus. Only global markers are inserted into the trace. 11 = Local markers are forwarded to the processor bus. Markers are not inserted into the trace.
6	RW	HTMSC_CTRL_DBG0_STOP: Stop on local DBG_Trigger0 to PC. 1 = Stop on local trace debug trigger 0. 0 = Ignore debug trigger 0.
7	RW	HTMSC_CTRL_DBG1_STOP: Stop on local DBG_Trigger1 to PC. 1 = Stop on local trace debug trigger 1. 0 = Ignore debug trigger 1.
8	RW	HTMSC_CTRL_RUN_STOP: Stop on trace run falling. 1 = Stop trace on falling edge of tcdgb_tchtm_trace_run. 0 = Ignore signal tcdgb_tchtm_trace_run.
9	RW	HTMSC_CTRL_CHIP0_STOP: Stop on PC_TC_DBG_Trigger0. 1 = Stop trigger core debug trigger 0. 0 = Ignore core debug trigger 0.
10	RW	HTMSC_CTRL_CHIP1_STOP: Stop on PC_TC_DBG_Trigger1. 1 = Stop trigger on core debug trigger 1. 0 = Ignore core debug trigger 1.
11:12	RW	HTMSC_CTRL_SPARE1112: Spare bits.
13	RW	HTMSC_CTRL_XSTOP_STOP: Stop on checkstop. 1 = Stop trigger on chiplet checkstop. 0 = Ignore chiplet checkstop.
14:15	RW	HTMSC_CTRL_SPARE1415: Spare bits.
16:63	RO	constant = 0b000000000000000000000000000000000000000000000000

Register Name	HTM IMA Status Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CHTMLBS0.CHTM.SC.HTM_IMA_STATUS
Address	000000001301220A (SCOM)
Description	HTM IMA status

Bits	SCOM	Field Mnemonic: Description
0	ROX	HTMSC_IMA_ERROR: IMA ERROR: NCU transfer error. Deasserted after performing the CHTM HPMC-IMA reset sequence.
1	ROX	HTMSC_IMA_TRACE_ACTIVE: IMA idle indicator.
2	ROX	HTMSC_PDBAR_ERROR: PDBAR parity error. Deasserted after performing the CHTM HPMC-IMA reset sequence.
3:4	ROX	HTMSC_IMA_RESERVED: Reserved.

Bits	SCOM	Field Mnemonic: Description
5:11	ROX	HTMSC_IMA_FSM: Display current IMA FSM state. 01 Disabled. 02 Idle. 04 Clear. 08 Capture. 10 Write LDBAR. 20 Write PDBAR. 40 Error.
12:15	ROX	HTMSC_IMA_COUNT: Number of writes completed to LDBAR or PDBAR address. Counts 0 to 7.
16:55	RO	constant = 0b0000000000000000000000000000000000000000

Register Name	HTM IMA PDBAR Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME0.CHTMLBS0.CHTM.SC.HTM_IMA_PDBAR
Address	000000001301220B (SCOM)
Description	HTM IMA PDBAR

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1	RW	HTMSC_IMA_ENABLE_SPLIT_CORE: This bit controls the indexing of the PDBAR address for the starting address of the write to the PDBAR space. 0 = Big core mode. 1 = Split core mode.
2:4	RW	HTMSC_IMA_PDBAR_SPARE2TO4:
5:7	RW	HTMSC_IMA_PDBAR_SCOPE: Configure the scope used for direct memory write. The scope will be forced to a group minimum unless HTM_MODE(dis_force_group) = 1. Foreign scope is not supported.
8:50	RW	HTMSC_IMA_PDBAR: IMA Write physical base address PDBAR spare bit 2 to 4.
51:63	RO	constant = 0b0000000000000

Register Name	CME_SCOM CME LFIR Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_LFIR
Address	0000000013012400 (SCOM) 0000000013012401 (SCOM1) 0000000013012402 (SCOM2)
Description	CME_SCOM CME LFIR

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_PPE_INTERNAL_ERROR: PPE asserted an internally detected error condition that caused it to halt. This indication is intended to be reported to both core PPM macros to be forwarded to the OCC complex as an error interrupt.
1	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_PPE_EXTERNAL_ERROR: PPE detected an error condition on an external interface to the memory bolt-on that caused it to halt. This indication is intended to be reported to both core PPM macros to be forwarded to the OCC complex as an error interrupt.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
2	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_PPE_PROGRESS_ERROR: PPE detected a lack of forward progress that caused it to halt. This indication is intended to be reported to both core PPM macros to be forwarded to the OCC complex as an error interrupt.
3	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_PPE_BREAKPOINT_ERROR: PPE halted either upon a hardware debug or software-requested breakpoint event. This indication is intended to be reported to both core PPM macros to be forwarded to the OCC complex as an error interrupt.
4	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_PPE_WATCHDOG: PPE asserted a watchdog timeout condition. Will likely be masked. For debug information only.
5	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_PPE_HALTED: PPE asserted a halt condition. Will likely be masked since there are several sources of halt that may be valid.
6	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_PPE_DEBUG_TRIGGER: PPE asserted a debug trigger.
7	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_SRAM_UE: SRAM uncorrectable error. CME will get a MCHK. Should be marked as as a recoverable error for runtime diagnostics reporting.
8	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_SRAM_CE: SRAM correctable error. CME received corrected data, but SRAM content is bad until the next scrub to that line. (Should be masked in the product; unmasked and marked as a recoverable error in manufacturing test.)
9	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_SRAM_SCRUB_ERR: Scrub timer tick occurred when scrub is still pending.
10	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_BCE_ERROR: Block copy engine error. BCE received an error from L3 or NCU. This also causes an interrupt to the CME, if it is running.
11	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_SPARE11: Implemented but not used. Inputs tied to 0.
12	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_SPARE12: Implemented but not used. Inputs tied to 0.
13	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_C0_IVRM_DROPOUT: Dropout was detected on core 0 chiplet iVRM. Note that if IDCR[DROPOUT_NOTIFY_ENABLE] = 1, the UNMASKED value of this bit is ORed with the two subsequent dropout indication events and sent to the QPPM as a level signal.
14	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_C1_IVRM_DROPOUT: Dropout was detected on core 1 chiplet iVRM.
15	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_CACHE_IVRM_DROPOUT: Dropout was detected on cache chiplet iVRM.
16	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_EXTREME_DROOP_ERR: Extreme droop (as reported to the DPLL) over time exceeded the threshold in VCTR. Note that if VCCR[DROOP_NOTIFY_ENABLE] = 1, the UNMASKED value of this bit is ORed with the three subsequent droop indication events and sent to the QPPM as a level signal (ORed with the DROPOUT indications above).
17	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_LARGE_DROOP_ERR: Large droop (as reported to the DPLL) over time exceeded the threshold in VCTR.
18	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_SMALL_DROOP_ERR: Small droop (as reported to the DPLL) over time exceeded the threshold in VCTR.
19	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_UNEXPECTED_DROOP_ENCODE: Detected non-thermometer code that should not be caused by metastability (that is, b'0001', b'0011', b'0010', or b'0111'). For debug and characterization only.
20	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_FIR_PARITY_ERR_DUP: Internal FIR parity error duplicate (same as fir_parity_err).

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
21	RWX	WOX_AND	WOX_OR	CME_SCOM_LFIR_FIR_PARITY_ERR: Internal FIR parity error.
22:63	RO	RO	RO	constant = 0b000000000000000000000000000000000000000000

Register Name	CME_SCOM CME LFIR Mask Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_LFIRMASK
Address	0000000013012403 (SCOM) 0000000013012404 (SCOM1) 0000000013012405 (SCOM2)
Description	CME_SCOM CME LFIR mask

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:21	RW	WO_AND	WO_OR	CME_SCOM_LFIRMASK_FIR_MASK: PPE asserted an error condition.
22:63	RO	RO	RO	constant = 0b000000000000000000000000000000000000000000

Register Name	CME_SCOM CME LFIR Action 0 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_LFIRACT0
Address	0000000013012406 (SCOM)
Description	CME_SCOM CME LFIR action0

Bits	SCOM	Field Mnemonic: Description
0:21	RW	CME_SCOM_LFIRACT0_FIR_ACTION0: MSB of action select for corresponding bit in FIR.
22:63	RO	constant = 0b000000000000000000000000000000000000000000

Register Name	CME_SCOM CME LFIR Action 1 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_LFIRACT1
Address	0000000013012407 (SCOM)
Description	CME_SCOM CME LFIR action1

Bits	SCOM	Field Mnemonic: Description
0:21	RW	CME_SCOM_LFIRACT1_FIR_ACTION1: LSB of action select for corresponding bit in FIR.
22:63	RO	constant = 0b000000000000000000000000000000000000000000

Register Name	PPE Local SRAM Control Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CMEARB.CSCR
Address	000000001301240A (SCOM) 000000001301240B (SCOM1) 000000001301240C (SCOM2)
Description	PPE local SRAM control register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_CLEAR	WO_OR	CSCR_SRAM_ACCESS_MODE: SRAM access mode.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
1	RWX	WOX_CLEAR	WOX_OR	CSCR_SRAM_SCRUB_ENABLE: Enable background scrub (atomic read-write) to periodically check, and if needed correct, the data in the SRAM for bit flips due to alpha particles. This bit is cleared by the hardware when a UE is detected to assist with fault analysis.
2	RW	WO_CLEAR	WO_OR	CSCR_ECC_CORRECT_DIS: Do not correct the data coming out of the array on ECC detected correctable errors. This will cause CEs to report an error back to the PPE in addition to the usual UEs.
3	RW	WO_CLEAR	WO_OR	CSCR_ECC_DETECT_DIS: Do not flag an error back to PPE for ECC miscompares. Data from the SRAM is always treated as good. Note that errors are always detected and reported to the FIR and must be masked there independently from this bit.
4	RW	WO_CLEAR	WO_OR	CSCR_ECC_INJECT_TYPE: Used only when ECC_INJECT_ERR is set. When set to 1, causes an ECC error to be reported on every SRAM read. When 0, causes a single ECC error to be indicated on the next SRAM read to occur, since it also clears ECC_INJECT_ERR when that happens.
5	RWX	WOX_CLEAR	WOX_OR	CSCR_ECC_INJECT_ERR: When set, the hardware will inject or cause a dummy uncorrectable error (UE) to be reported to both the PPE and the FIR on all SRAM reads. The SRAM contents are not modified. Type of error to inject is determined by the previous bit. If ECC_INJECT_TYPE = 1, then this bit clears when the first error is injected. Note that this bit can also be set by the PPE local register CFMSR.
6:7	RW	WO_CLEAR	WO_OR	CSCR_SPARE_6_7: Implemented but unused.
8:46	RO	RO	RO	constant = 0b000000000000000000000000000000000000000
47:59	RWX	WOX_CLEAR	WOX_OR	CSCR_SRAM_SCRUB_INDEX: 32 KB scrub index. This field is auto-incremented by hardware for every scrub operation. Upon a UE detection, this field is over-written with the index of the double word containing the error. **Note:** SRAM_SCRUB_ENABLE should be set to 0 when writing this field to prevent one cycle window from ignoring this write if a scrub update happens to occur concurrently.
60:63	RO	RO	RO	constant = 0b0000

Register Name	PPE Local SRAM Address Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CMEARB.CSAR
Address	000000001301240D (SCOM)
Description	PPE local SRAM address register

Bits	SCOM	Field Mnemonic: Description
0:15	RO	constant = 0b0000000000000000
16:28	RW	CSAR_SRAM_ADDRESS: Address of an 8-byte SRAM entry in the 32 KB SRAM array.
29:63	RO	constant = 0b00000000000000000000000000000000000

Register Name	PPE Local SRAM Data Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CMEARB.CSDR
Address	000000001301240E (SCOM)
Description	PPE local SRAM data register

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	CSDR_SRAM_DATA: 8-byte SRAM data entry for the address given by the SRAM_ADDRESS. Reads cause this register to be written with data from the local SRAM. Writes cause the local SRAM to be written with the contents of this register.

Register Name	CME_SCOM CME Local BCE Control and Status Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_BCECSR
Address	000000001301240F (SCOM)
Description	CME_SCOM CME local BCE control and status register (BCECSR)

Bits	SCOM	Field Mnemonic: Description
0	ROX	CME_SCOM_BCECSR_BUSY: This field reads as '1' whenever the BCE is busy processing a transfer. This status bit is also routed to the CME external interrupt controller. It is an error to attempt to issue another start command to a busy BCE. This bit is cleared if an error occurs during the transaction.
1	RW_WCLEAR	CME_SCOM_BCECSR_ERROR: This bit is set if an error occurs during the transaction and locks this register until cleared, by writing this bit to a 1. All of the other fields of this register are ignored on a write when this bit is set.
2:3	RO	constant = 0b00
4	RW	CME_SCOM_BCECSR_RNW: Read, not write. 0 = The transfer is a write from SRAM into main memory. 1 = The transfer is a read from main memory into SRAM.
5	RW	CME_SCOM_BCECSR_BARSEL: Specifies which BCEBAR[n] to use for main memory addressing. 0 = Use BCEBAR[0] 1 = Use BCEBAR[1] **Note:** It is an error to issue a start command specifying a disabled or improperly initialized BAR (IPL host boot code requirement).
6	RW	CME_SCOM_BCECSR_PRIORITY: Specifies whether the transfer will be given priority on the processor bus over other units. Set only when block copy latency is important. 0 = Transfer will not have priority. 1 = Transfer will have priority. **Note:** Causes a trusted processor bus operation.
7	RW	CME_SCOM_BCECSR_INJECT_ERR: When set, causes the BCE to report a false error on the last block copy transaction.
8:12	RO	constant = 0b00000
13:15	RW	CME_SCOM_BCECSR_TYPE: Specifies the access mode (processor bus TTYPE) for writes from SRAM into main memory. 0 = Default mode (standard 8-byte coherent partial-DMA write). 1 = Atomic ADD. 2 = Atomic AND. 3 = Atomic OR. 4 = Atomic XOR. 5:7 = Illegal. This field is ignored for reads, but must specify a valid value for write transfers.
16	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
17:27	RW	CME_SCOM_BCECSR_NUM_BLOCKS: The number of 8-byte blocks to transfer for writes, or the number of 32-byte blocks to transfer for reads. This field is decremented after each block is successfully transferred. While BUSY this indicates which block is currently being copied and will always be 0 after a successfully completed transfer. After a STOP or ERROR this can be read to determine how many blocks have not yet been successfully copied. **Notes:** 1. Using a value of 0 will complete instantly and not transfer any data (for testing code). 2. Using a value greater than 0x400 is not advised because it will cause the BCE to transfer some blocks twice, potentially overwriting data.
28:39	RW	CME_SCOM_BCECSR_SBASE: Written with the SRAM block index of the first block of the transfer when the transfer is initiated, this field will be seen to increment (and possibly wrap) during the transfer. The SRAM address associated with SBASE is 0xFFFF8000 + ((SBASE * size) % 32 KB) where size is 32 bytes for reads and 8 bytes for writes. When BUSY clears without an ERROR, (that is, on a STOP or when the block copy completes), this index points to the block after the one successfully written.
40:41	RO	constant = 0b00
42:63	RW	CME_SCOM_BCECSR_MBASE: Written with the main memory block index of the first block of the transfer when the transfer is initiated, this field will be seen to increment (and possibly wrap) during the transfer. The main memory address associated with MBASE is pbase + ((MBASE * size) % extent) where pbase is the processor bus base address implied by the BCEBAR[n] register selected for the transfer, size is 32 bytes for reads and 8 bytes for writes, and extent is the BCEBAR[n] aperture size.

Register Name	PPE External Interface External Control Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CMEPPE.PPE.PPE_XIXCR
Address	0000000013012410 (SCOM)
Description	PPE External Interface external control

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:3	WOX	PPE_XIXCR_XCR: PPE external control register CMD command. 000 = Clear debug status. 001 = Halt. 010 = Resume. 011 = Single-step. 100 = Toggle XSR[TRH]. 101 = Soft reset. 110 = Hard reset. 111 = Force halt.
4:63	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000

Register Name	PPE External Interface RAMRA Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CMEPPE.PPE.PPE_XIRAMRA
Address	0000000013012411 (SCOM)
Description	PPE external interface RAMRA

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0

Bits	SCOM	Field Mnemonic: Description
1:3	WOX	PPE_XIXCR_XCR: PPE external control register CMD command. 000 = Clear debug status. 001 = Halt. 010 = Resume. 011 = Single-step. 100 = Toggle XSR[TRH]. 101 = Soft reset. 110 = Hard reset. 111 = Force halt.
4:31	RO	constant = 0b0000000000000000000000000000
32:63	WOX	PPE_XIRAMRA_SPRG0: The SPRG0 register value, by convention, is used by PPE code to keep status. SPRG0 is a 32-bit scratch register. SPRG0 can only be written as an XIR when the processor is halted (XSR[HS] = '1').

Register Name	PPE External Interface RAMGA Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CMEPPE.PPE.PPE_XIRAMGA
Address	0000000013012412 (SCOM)
Description	PPE external interface RAMGA

Bits	SCOM	Field Mnemonic: Description
0:31	WOX	PPE_XIRAMGA_IR: PPE instruction register. Writes cause a RAM operation. It can only be written when the processor is halted (XSR[HS] = '1'). Provides the requested PPE instruction to execute.
32:63	WOX	PPE_XIRAMRA_SPRG0: The SPRG0 register value, by convention, is used by PPE code to keep status. SPRG0 is a 32-bit scratch register. SPRG0 can only be written as an XIR when the processor is halted (XSR[HS] = '1').

Register Name	PPE External Interface RAMDBG Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CMEPPE.PPE.PPE_XIRAMDBG
Address	0000000013012413 (SCOM)
Description	PPE external interface RAMDBG

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1:3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.
7	ROX	Reserved field.
8	ROX	Reserved field.
9:11	ROX	NULL_MSR_SIBRC:
12	ROX	Reserved field.
13	ROX	Reserved field.
14	ROX	NULL_MSR_WE:
15	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
16:19	ROX	Reserved field.
20	ROX	NULL_MSR_LP:
21	ROX	Reserved field.
22:23	RO	constant = 0b00
24	ROX	Reserved field.
25	ROX	Reserved field.
26:27	RO	constant = 0b00
28	ROX	Reserved field.
29:31	ROX	Reserved field.
32:63	RWX	PPE_XIRAMRA_SPRG0: The SPRG0 register value, by convention, is used by PPE code to keep status. SPRG0 is a 32-bit scratch register. SPRG0 can only be written as an XIR when the processor is halted (XSR[HS] = '1').

Register Name	PPE External Interface RAM Error Data Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CMEPPE.PPE.PPE_XIRAMEDR
Address	0000000013012414 (SCOM)
Description	PPE external interface RAM error data

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	PPE_XIRAMGA_IR: PPE instruction register. Writes cause a RAM operation. It can only be written when the processor is halted (XSR[HS] = '1'). Provides the requested PPE instruction to execute.
32:63	ROX	PPE_XIRAMEDR_EDR: Error data register, set on PPE interrupts caused by an error.

Register Name	PPE External Interface DBGPRO Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CMEPPE.PPE.PPE_XIDBGPRO
Address	0000000013012415 (SCOM)
Description	PPE external interface DBGPRO

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1:3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.
7	ROX	Reserved field.
8	ROX	Reserved field.
9:11	ROX	NULL_MSR_SIBRC:
12	ROX	Reserved field.
13	ROX	Reserved field.
14	ROX	NULL_MSR_WE:

Bits	SCOM	Field Mnemonic: Description
15	ROX	Reserved field.
16:19	ROX	Reserved field.
20	ROX	NULL_MSR_LP:
21	ROX	Reserved field.
22:23	RO	constant = 0b00
24	ROX	Reserved field.
25	ROX	Reserved field.
26:27	RO	constant = 0b00
28	ROX	Reserved field.
29:31	ROX	Reserved field.
32:61	RWX	Reserved field.
62:63	RO	constant = 0b00

Register Name	**MIB External Interface MEM Register**
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CMEPPE.MIB.MIB_XIMEM
Address	0000000013012417 (SCOM)
Description	MIB external interface MEM info

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MIB_XIMEM_MEM_ADDR: MEM transaction buffer current or previous transaction byte address.
32	ROX	MIB_XIMEM_MEM_R_NW: MEM transaction buffer current or previous transaction type, read if '1' and write if '0'.
33	ROX	MIB_XIMEM_MEM_BUSY: Indicates if the transaction buffer is occupied with an ongoing transaction. Busy is cleared when the transaction is completed.
34	ROX	MIB_XIMEM_MEM_IMPRECISE_ERROR_PENDING: Indicates that the current or previous transaction had an imprecise error. Cleared when it is reported back to PPE. **Note:** The address of the erroneous transaction is copied into the SGB address latches such that the memory interface can continue to service instruction fetches.
35:42	ROX	MIB_XIMEM_MEM_BYTE_ENABLE: MEM transaction buffer current or previous transaction byte enables.
43	ROX	MIB_XIMEM_MEM_LINE_MODE: MEM transaction buffer current or previous transaction line mode. Indicates a 32-byte read request when set to '1'.
44:48	RO	constant = 0b00000
49:51	ROX	MIB_XIMEM_MEM_ERROR: MEM transaction buffer error code. Current or previous transaction got an error on the memory interface when non-zero.
52:61	RO	constant = 0b0000000000
62	ROX	MIB_XIMEM_MEM_IFETCH_PENDING: Indicates a instruction fetch is pending on the MEM interface when set to '1'.
63	ROX	MIB_XIMEM_MEM_DATAOP_PENDING: Indicates a data transaction is pending on the MEM interface when set to '1'.

Register Name	MIB External Interface Store Gather Buffer Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CMEPPE.MIB.MIB_XISGB
Address	0000000013012418 (SCOM)
Description	MIB external interface store gather buffer information

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MIB_XISGB_STORE_ADDRESS: Contains either the SGB address 4-byte tag *or* the address of an imprecise store error that occurred when performing a previous data transaction.
32:34	RO	constant = 0b000
35	ROX	MIB_XIMEM_MEM_IMPRECISE_ERROR_PENDING: Indicates that the current or previous transaction had an imprecise error. Cleared when it is reported back to PPE. **Note:** The address of the erroneous transaction is copied into the SGB address latches such that the memory interface can continue to service instruction fetches.
36:39	ROX	MIB_XISGB_SGB_BYTE_VALID: Byte valid bits within the 4B tag. Cleared when the SGB contents are committed, meaning either flushed to memory *or* copied into the transaction buffer. **Note:** These bits can never be set if a MEM imprecise error is pending.
40:62	RO	constant = 0b00000000000000000000000
63	ROX	MIB_XISGB_SGB_FLUSH_PENDING: Indicates a store gather buffer flush to memory is pending on the MEM interface when set to '1'. This can happen only if MEM_BUSY in the MEM transaction buffer is '0'.

Register Name	MIB External Interface ICACHE Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CMEPPE.MIB.MIB_XIICAC
Address	0000000013012419 (SCOM)
Description	MIB external interface ICACHE information

Bits	SCOM	Field Mnemonic: Description
0:26	ROX	Reserved field.
27:31	RO	constant = 0b00000
32	ROX	Reserved field.
33	RO	constant = 0b0
34	ROX	CME_SCOM_XISIB_PIB_IFETCH_PENDING: Indicates an instruction fetch is pending on the PIB interface when set to '1'.
35	ROX	MIB_XIMEM_MEM_IFETCH_PENDING: Indicates an instruction fetch is pending on the MEM interface when set to '1'.
36:39	ROX	Reserved field.
40:43	ROX	Reserved field.
44	RO	constant = 0b0
45	ROX	Reserved field.
46	ROX	Reserved field.
47	ROX	Reserved field.
48:63	RO	constant = 0b0000000000000000

Register Name	CME_SCOM CME PCB Queue 0 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_XIPCBQ0
Address	000000001301241A (SCOM)
Description	CME_SCOM CME PCB queue0 information

Bits	SCOM	Field Mnemonic: Description
0:25	ROX	CME_SCOM_XIPCBQ0_PCBQ_N_INFO: CME PCBMUX queue [n] information register.
26:63	RO	constant = 0b00000000000000000000000000000000000000

Register Name	CME_SCOM CME PCB Queue 1 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_XIPCBQ1
Address	000000001301241B (SCOM)
Description	CME_SCOM CME PCB queue1 information

Bits	SCOM	Field Mnemonic: Description
0:25	ROX	CME_SCOM_XIPCBQ1_PCBQ_N_INFO: CME PCBMUX queue [n] information register.
26:63	RO	constant = 0b00000000000000000000000000000000000000

Register Name	CME_SCOM CME External Interface PCBMUX0 Data Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_XIPCBMD0
Address	000000001301241C (SCOM)
Description	CME_SCOM CME external interface PCBMUX0 data

Bits	SCOM	Field Mnemonic: Description
0:26	ROX	Reserved field.
27:63	RO	constant = 0b0000000000000000000000000000000000000

Register Name	CME_SCOM CME External Interface PCBMUX1 Data Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_XIPCBMD1
Address	000000001301241D (SCOM)
Description	CME_SCOM CME external interface PCBMUX1 data

Bits	SCOM	Field Mnemonic: Description
0:26	ROX	Reserved field.
27:63	RO	constant = 0b0000000000000000000000000000000000000

Register Name	CME_SCOM CME External Interface PCBMUX0 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_XIPCBMI0
Address	000000001301241E (SCOM)
Description	CME_SCOM CME external interface PCBMUX0 information

Bits	SCOM	Field Mnemonic: Description
0:6	ROX	Reserved field.
7:63	RO	constant = 0b000000000000000000000000000000000000000000000000000000000

Register Name	CME_SCOM CME External Interface PCBMUX1 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_XIPCBMI1
Address	000000001301241F (SCOM)
Description	CME_SCOM CME external interface PCBMUX1 information

Bits	SCOM	Field Mnemonic: Description
0:6	ROX	Reserved field.
7:63	RO	constant = 0b000000000000000000000000000000000000000000000000000000000

Register Name	CME_SCOM CME Flags Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_FLAGS
Address	0000000013012420 (SCOM) 0000000013012421 (SCOM1) 0000000013012422 (SCOM2)
Description	CME_SCOM CME flags

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:31	RWX	WOX_CLEAR	WOX_OR	CME_SCOM_FLAGS_DATA: Flags that are defined by CME firmware.
32:63	RO	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	CME_SCOM CME Scratch 0 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_SRTCH0
Address	0000000013012423 (SCOM)
Description	CME_SCOM CME scratch 0

Bits	SCOM	Field Mnemonic: Description
0:31	RW	CME_SCOM_SRTCH0_DATA: Scratch data.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	CME_SCOM CME Scratch 1 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_SRTCH1
Address	0000000013012424 (SCOM)
Description	CME_SCOM CME scratch 1

Bits	SCOM	Field Mnemonic: Description
0:31	RW	CME_SCOM_SRTCH1_DATA: Scratch data.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	CME_LCL CME Local External Interrupt Source Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_LCL_EISR
Address	0000000013012425 (SCOM)
Description	CME_LCL CME local external interrupt source register

Bits	SCOM	Field Mnemonic: Description
0	ROX	CME_LCL_EISR_DEBUGGER: Debugger software uses this bit to produce an interrupt. The physical input is tied low. The respective EITR bit must be set to edge so that a WOR to this register or pulse from the EIIR will produce an interrupt.
1	ROX	CME_LCL_EISR_DEBUG_TRIGGER: Asserted if the trace array logic analyzer logic has detected a trigger condition.
2	ROX	CME_LCL_EISR_QUAD_CHECKSTOP: QUAD checkstop present.
3	ROX	CME_LCL_EISR_PVREF_FAIL: The precision voltage reference circuit has failed and voltage regulation and VDM measurement is now in question.
4	ROX	CME_LCL_EISR_OCC_HEARTBEAT_LOST: OCC heartbeat lost indication from QPPM.
5	ROX	CME_LCL_EISR_CORE_CHECKSTOP: Core pair checkstop condition (recoverable).
6	ROX	CME_LCL_EISR_DROPOUT_DETECT: An iVRM dropout event occurred (pulse). May be used for characterization or tuning the iVRM dead zone where it is no longer able to regulate voltage.
7	ROX	CME_LCL_EISR_INTERCME_DIRECT_IN_0: Tied to INTERCME_DIRECT_IN bit 0. Used for general communication from the sibling CME.
8	ROX	CME_LCL_EISR_BCE_BUSY_HIGH: High priority block copy engine busy indication. (It has the same source as bit 23, but as low priority; only one of these two bits should ever be unmasked). Falling edge indicates completion or error.
9	ROX	CME_LCL_EISR_BCE_TIMEOUT: Notification that BCE has not made forward progress in the time period corresponding to two scrub timer pulses (regardless of scrub enable). The BCE remains active but CME can use this notification to communicate a problem to the OCC.
10	ROX	CME_LCL_EISR_DOORBELL3_C0: Core 0 doorbell 3. A non-zero value is present in core 0 PPM_CME_DOORBELL_REG3(0:7).
11	ROX	CME_LCL_EISR_DOORBELL3_C1: Core 1 doorbell 3. A non-zero value is present in core 1 PPM_CME_DOORBELL_REG3(0:7).
12	ROX	CME_LCL_EISR_PC_INTR_PENDING_C0: Core 0 interrupt pending (stop exit request) from PC. Mask when core is not in stop state.
13	ROX	CME_LCL_EISR_PC_INTR_PENDING_C1: Core 1 interrupt pending (stop exit request) from PC. Mask when core is not in stop state.
14	ROX	CME_LCL_EISR_SPECIAL_WAKEUP_C0: Core 0 special wake-up present (input from Core0 PPM). **Note:** Code should mask this bit when core is not in stop state.
15	ROX	CME_LCL_EISR_SPECIAL_WAKEUP_C1: Core 1 special wake-up present (input from Core1 PPM). **Note:** Code should mask this bit when core is not in stop state.
16	ROX	CME_LCL_EISR_REG_WAKEUP_C0: Core 0 external or malfunction alert interrupt wake-up source is present and enabled as a wake-up source. Code should mask this bit when core is not in stop state. **Note:** When WSR[PC_FUSED_CORE_MODE] = '1', the hardware maps external interrupts for even threads to this bit; otherwise threads 0:3.
17	ROX	CME_LCL_EISR_REG_WAKEUP_C1: Core 1 external or malfunction alert interrupt wake-up is present and enabled as a wake-up source. Code should mask this bit when core is not in stop state. **Note:** When WSR[PC_FUSED_CORE_MODE] = '1', the hardware maps external interrupts for odd threads to this bit; otherwise threads 4:7.

Bits	SCOM	Field Mnemonic: Description
18	ROX	CME_LCL_EISR_DOORBELL2_C0: Core 0 doorbell 2. A non-zero value is present in core 0 PPM_CME_DOORBELL_REG2(0:7).
19	ROX	CME_LCL_EISR_DOORBELL2_C1: Core 1 doorbell 2. A non-zero value is present in core 1 PPM_CME_DOORBELL_REG2(0:7).
20	ROX	CME_LCL_EISR_PC_PM_STATE_ACTIVE_C0: Core 0 PM state active, as controlled by FWMR. The direct signal will produce interrupts when the core chiplet enters *any* Stop state; the mode settings in FWMR allows for the entry into Stop 1 or all Stop Levels to be filtered to the CME.
21	ROX	CME_LCL_EISR_PC_PM_STATE_ACTIVE_C1: Core 1 PM state active, as controlled by FWMR. The direct signal will produce interrupts when the Core Chiplet enters *any* Stop state; the mode settings in FWMR allows for the entry into Stop 1 or all Stop Levels to be filtered to the CME.
22	ROX	CME_LCL_EISR_L2_PURGE_DONE: L2 purge done (level) in response to the SICR L2 PURGE or ABORT request.
23	ROX	CME_LCL_EISR_NCU_PURGE_DONE: NCU purge done (level) in response to the SICR L2 PURGE or ABORT request.
24	ROX	CME_LCL_EISR_CHTM_PURGE_DONE_C0: Core 0 hardware trace macro purge done pulse indication.
25	ROX	CME_LCL_EISR_CHTM_PURGE_DONE_C1: Core 1 hardware trace macro purge done pulse indication.
26	ROX	CME_LCL_EISR_BCE_BUSY_LOW: Lower priority block copy engine busy indication. (Same source as bit 6, but as high priority; only one of these two bits should ever be unmasked). Falling edge indicates completion or error.
27:28	ROX	CME_LCL_EISR_FINAL_VDM_DATA01: Final VDM data bits 0:1.
29	ROX	CME_LCL_EISR_COMM_RECVD: CME communication received. Indicates that ICRR has been updated by the partner CME.
30	ROX	CME_LCL_EISR_COMM_SEND_ACK: Indicates that the partner CME has affirmatively acknowledged the sent communication. Firmware must clear this bit (and cme_comm_send_nack) before writing to ICSR to ensure that acknowledgments are accurately recorded.
31	ROX	CME_LCL_EISR_COMM_SEND_NACK: Indicates that the partner CME has negatively acknowledged the sent communication. Firmware must clear this bit (and cme_comm_send_ack) before writing to ICSR to ensure that acknowledgments are accurately recorded.
32:33	ROX	CME_LCL_EISR_SPARE_32_33: Implemented but unused. The physical inputs are tied low.
34	ROX	CME_LCL_EISR_PMCR_UPDATE_C0: PMCR update received from core 0 (or via SCOM).
35	ROX	CME_LCL_EISR_PMCR_UPDATE_C1: PMCR update received from core 1 (or via SCOM).
36	ROX	CME_LCL_EISR_DOORBELL0_C0: Core 0 doorbell 0. A non-zero value is present in core 0 PPM_CME_DOORBELL_REG0(0:7).
37	ROX	CME_LCL_EISR_DOORBELL0_C1: Core 1 doorbell 0. A non-zero value is present in core 1 PPM_CME_DOORBELL_REG0(0:7).
38:39	ROX	CME_LCL_EISR_INTERCME_DIRECT_IN_1_2: Tied to INTERCME_DIRECT_IN(1:2). Used for general communication from the sibling CME.
40	ROX	CME_LCL_EISR_DOORBELL1_C0: Core 0 doorbell 1. A non-zero value is present in core 0 PPM_CME_DOORBELL_REG1(0:7).
41	ROX	CME_LCL_EISR_DOORBELL1_C1: Core 1 doorbell 1. A non-zero value is present in core 1 PPM_CME_DOORBELL_REG1(0:7).
42:43	ROX	CME_LCL_EISR_RESERVED_42_43: Implemented but unused. The physical inputs are tied low.
44:63	RO	constant = 0b00000000000000000000

Register Name	CME_LCL CME Local External Interrupt Mask Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_LCL_EIMR
Address	0000000013012426 (SCOM)
Description	CME_LCL CME local external interrupt mask register

Bits	SCOM	Field Mnemonic: Description
0:43	RO	CME_LCL_EIMR_INTERRUPT_MASK: (See the CME External Interrupt Source Register for bit definitions.) Masks the respective event from producing an interrupt to the CME. The events are still captured in the EISR but are not reported via interrupt signals. 0 = Not masked (Enabled). 1 = Masked.
44:63	RO	constant = 0b00000000000000000000

Register Name	CME_LCL CME Local External Interrupt Polarity Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_LCL_EIPR
Address	0000000013012427 (SCOM)
Description	CME_LCL CME local external interrupt polarity register

Bits	SCOM	Field Mnemonic: Description
0:43	RO	CME_LCL_EIPR_INTERRUPT_POLARITY: (See the CME External Interrupt Source Register for bit definitions.) Establishes the edge or polarity of an interrupt. 0 = Falling low. 1 = Rising high. When set the respective bit in the EITR is set to Level, then the Low and High meanings apply as follows: If this bit is set to Low, the respective EISR bit follows the inverted input to the OISR from the unit driving the signal. If this bit is set to High, the respective EISR bit follows the direct input to the EISR from the unit driving the signal. When the respective bit in the OITR[n] is set to Edge, then the Falling and Rising meanings apply as follows: If this bit is set to Falling, a transition from 1 to 0 of the input signal to the EISR sets the respective EISR bit. If this bit is set to Rising, a transition from 0 to 1 of the input signal to the EISR sets the respective EISR bit.
44:63	RO	constant = 0b00000000000000000000

Register Name	CME_LCL CME Local External Interrupt Type Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_LCL_EITR
Address	0000000013012428 (SCOM)
Description	CME_LCL CME Local External Interrupt Type Register

Bits	SCOM	Field Mnemonic: Description
0:43	RO	CME_LCL_EITR_INTERRUPT_TYPE: (See the CME External Interrupt Source Register for bit definitions.) Establishes the type of interrupt that is monitored. 0 = Level 1 = Edge When set to Level, the respective EISR bit follows the input to the EISR from the unit driving the signal but with the polarity defined by the EIPR. Specifically, if the respective EIPR bit is set to High, this register retains the polarity of the incoming signal; if the respective EIPR bit is set to Low, this register captures the inverted polarity of the incoming signal. When set to Edge, the respective EISR bit is asserted upon the transition defined by the EIPR of the input from the unit driving the signal. Specifically, if the respective EIPR bit is set to Rising, a transition from 0 to 1 sets the bit; if the respective EIPR bit is set to Falling, a transition from 1 to 0 sets the bit. Note: When set to Level, attempts to override the signal setting via W1CLR or WOR to the EISR will not stick as the signal input is the priority. Firmware must control the source of the Level signal to control the state of the EISR bit. When set to Edge, CLEAR and OR operations to the EISR will stick (clear or set respectively) in the EISR. **Engineering Note:** For firmware testing, a potential interrupt injection technique for Level interrupts is to override their definition to Edge and then use the OR register associated with the EISR. This will allow the injected transition to stick as the logic will not follow the input interrupt signal. However, if the firmware is expecting to find status in the driving unit, this technique may not be appropriate.
44:63	RO	constant = 0b00000000000000000000

Register Name	CME_LCL CME Local External Interrupt Status Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_LCL_EISTR
Address	0000000013012429 (SCOM)
Description	CME_LCL CME local external interrupt status register

Bits	SCOM	Field Mnemonic: Description
0:43	RO	Reserved field.
44:63	RO	constant = 0b00000000000000000000

Register Name	CME_LCL CME Local External Interrupt Input Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_LCL_EINR
Address	000000001301242A (SCOM)
Description	CME_LCL CME local external interrupt input register

Bits	SCOM	Field Mnemonic: Description
0:43	ROX	CME_LCL_EINR_INTERRUPT_INPUT: Raw inputs to the interrupt controller.
44:63	RO	constant = 0b00000000000000000000

Register Name	CME_SCOM CME Local External Interrupt Injection Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_EIIR
Address	000000001301242B (SCOM)
Description	CME_SCOM CME local external interrupt injection register

Bits	SCOM	Field Mnemonic: Description
0	WO_4P	CME_SCOM_EIIR_DEBUGGER: Generates a pulse that is ORed with the same EISR bit position and name.

Bits	SCOM	Field Mnemonic: Description
1	WO_4P	CME_SCOM_EIIR_DEBUG_TRIGGER: Generates a pulse that is ORed with the same EISR bit position and name.
2:8	RO	constant = 0b0000000
9	RW	CME_SCOM_EIIR_BCE_TIMEOUT: ORed with the same EISR bit position and name.
10:11	RO	constant = 0b00
12	RW	CME_SCOM_EIIR_PC_INTR_PENDING_C0: ORed with the same EISR bit position and name.
13	RW	CME_SCOM_EIIR_PC_INTR_PENDING_C1: ORed with the same EISR bit position and name.
14	RW	CME_SCOM_EIIR_SPECIAL_WAKEUP_C0: ORed with the same EISR bit position and name.
15	RW	CME_SCOM_EIIR_SPECIAL_WAKEUP_C1: ORed with the same EISR bit position and name.
16	RW	CME_SCOM_EIIR_REG_WAKEUP_C0: ORed with the same EISR bit position and name.
17	RW	CME_SCOM_EIIR_REG_WAKEUP_C1: ORed with the same EISR bit position and name.
18:19	RO	constant = 0b00
20	RW	CME_SCOM_EIIR_PC_PM_STATE_ACTIVE_C0: ORed with the same EISR bit position and name.
21	RW	CME_SCOM_EIIR_PC_PM_STATE_ACTIVE_C1: ORed with the same EISR bit position and name.
22	RW	CME_SCOM_EIIR_L2_PURGE_DONE: ORed with the same EISR bit position and name.
23	RW	CME_SCOM_EIIR_NCU_PURGE_DONE: ORed with the same EISR bit position and name.
24	WO_4P	CME_SCOM_EIIR_CHTM_PURGE_DONE_C0: ORed with the same EISR bit position and name.
25	WO_4P	CME_SCOM_EIIR_CHTM_PURGE_DONE_C1: ORed with the same EISR bit position and name.
26:63	RO	constant = 0b00000000000000000000000000000000000000

Register Name	CME_SCOM CME VDM Count Configuration Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_VCCR
Address	000000001301242C (SCOM)
Description	CME_SCOM CME VDM count configuration register

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CME_SCOM_VCCR_SMALL_EVENT_THRESHOLD: Number of timer periods (or 4:1 cycle periods if DROOP_TIMER_MODE = 0) that a small droop event was seen. Used for event duration profiling (16b).
16:27	RW	CME_SCOM_VCCR_LARGE_EVENT_THRESHOLD: Number of timer periods (or 4:1 cycle periods if DROOP_TIMER_MODE = 0) that a large droop event was seen. Used for event duration profiling (12b).
28:35	RW	CME_SCOM_VCCR_EXTREME_EVENT_THRESHOLD: Number of timer periods (or 4:1 cycle periods if DROOP_TIMER_MODE = 0) that an extreme droop event was seen. Used for event duration profiling (8b).
36:37	RW	CME_SCOM_VCCR_DROOP_PROFILE_TYPE: Chooses profile type in the programmable VECR Event fields: 00 = Total droop duration (of that level or deeper) 01 = Only that level droop duration (without ever going deeper) 10 = That level-in-a-row duration (despite going deeper, before or after) 11 = Only that level in-a-row duration (without ever going deeper) **Note:** Setting an above threshold = 0x0 makes the DROOP_PROFILE(1) a *don't care*.
38	RW	CME_SCOM_VCCR_DROOP_TIMER_MODE: When '0', the VDCR counters increment their 1:1 precounter every cycle that droop level is active, and this precounter increments the corresponding 4:1 droop counter whenever it carries. When '1', the VDCR counters increment if its droop level input was ever active for one or more cache cycles between two timer input pulses (~31ns period) without a deeper droop in that same period.

Bits	SCOM	Field Mnemonic: Description
39	RW	CME_SCOM_VCCR_DROOP_CHAR_MODE: Enables Droop characterization mode. When set, this changes the behavior of the VDM sample counters (VDCR and VNCR, but not VECR) for lab characterization and disables run-time monitoring (threshold detects) from setting droop errors in the FIR. Based on this mode, the fields in VDCR and VNCR: 0 = Count how many times a droop state happened so far during the configured droop sample window, and clear at the beginning of each sample period 1 = Count how many times a droop has occurred since the last read to that register, which clears it. In this mode, code must read the QMFR register simultaneously to compare against the delta in either CYCLES or TIMEBASE pulses (dependent on DROOP_TIMER_MODE).
40	RW	CME_SCOM_VCCR_DROOP_NOTIFY_ENABLE: Causes VDM droop indication to notify the QPPM macro by enabling the UNMASKED FIR bits for the three dropout errors to OR with the (now misnamed) QPPM_IVRM_DROPOUT signal.
41:43	RW	CME_SCOM_VCCR_SPARE41_43: Implemented but not used.
44:58	RO	constant = 0b000000000000000
59:63	RW	CME_SCOM_VCCR_DROOP_SAMPLE_RATE: Sample rate used when DROOP_CHAR_MODE = 0, whose meaning is dependent on the value of DROOP_TIMER_MODE: 0 = This field specifies the rising edge of which bit of the QFMR[CYCLES] to use to start a new sample window. 1 = Bits (1:4) of this field are used as a TSEL using the PPE timer to select which output bit is used to start a new sample window (bit 0 unused). This delay is defined as $2^{(29 - \text{select})}$ / Nest_Frequency. The default value for this register corresponds to 262 µs (assuming a 2 GHz processor bus). Note that when this register is written, the first sample window will be truncated (smaller) than the selected value dependent on the relative value in the selected timer being used. An event threshold may still be reached despite the smaller window.

Register Name	**CME_SCOM CME iVRM Dropout Configuration Register**
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_IDCR
Address	000000001301242D (SCOM)
Description	CME_SCOM CME iVRM dropout configuration register

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CME_SCOM_IDCR_DROPOUT_EVENT_THRESHOLD: Number of sustained dropout periods that must be counted before setting a dropout event. Setting this field to zero disables dropout event notifications when this field is non-zero, DROPOUT_CHAR_MODE == 0, and any of the three *_DROPOUT_EVENT_COUNT == the value of this field, the corresponding *_IVRM_DROPOUT bit is set in the FIR register and is ORed as a pulse with the DROPOUT_DETECT bit in the EISR.
24:31	RW	CME_SCOM_IDCR_DROPOUT_INAROW_THRESHOLD: Dropout count value used to determine a sustained dropout period has occurred. How many 4:1 cache cycles (or timer periods if DROPOUT_TIMER_MODE = 1) in a row the dropout must be present before being counted in the *_DROPOUT_EVENT_COUNT. Note that a value of '1' causes every dropout to be counted.
32	RW	CME_SCOM_IDCR_DROPOUT_TIMER_MODE: Dropout period timer select. Controls the dropout present condition used to increment the *_DROPOUT_INAROW_COUNT. When this field is: 0 = Every 4:1 cache cycle counts towards the droop count. (Implementation note: Dropout present is connected to the output of the dropout indication latch, which follows the value of dropout input.) 1 = Dropout indication must be asserted for an entire CME input timer pulse period to be counted (~31 ns). (Implementation note: Set-dominant sticky dropout indication latch running at 4:1 is set on every timer pulse and is reset whenever the dropout input = 0. Dropout present is the AND of the indication latch output and the timer pulse.)

Bits	SCOM	Field Mnemonic: Description
33	RW	CME_SCOM_IDCR_DROPOUT_CHAR_MODE: Enables dropout characterization mode. Changes the behavior of the *_DROPOUT_EVENT_COUNT for run time monitoring versus lab characterization of the iVRM dead zone. Based on this mode, the *_DROPOUT_EVENT_COUNT fields: 0 = Count how many times a sustained dropout period has been detected so far during the configured dropout sample window, and clear at the beginning of each sample window. 1 = Count how many times a sustained dropout period has occurred since the last read to that register, which clears it. In this mode, code must read the QFMR register simultaneously to compare against the delta in either CYCLES or TIMEBASE pulses (dependent on DROPOUT_TIMER_MODE).
34:35	RW	CME_SCOM_IDCR_SIBLING_CORE_DROPOUT_ENABLE: Connected to cme_dropout_enable_out(0:1). Used by the QUAD manager Hcode to control the dropout detection of the other pair of cores in the QUAD in the sibling CME. These bits must be set to '11' for the non-QUAD manager CME.
36:37	RW	CME_SCOM_IDCR_CORE_DROPOUT_ENABLE: These are ANDed with cme_dropout_enable_in(0:1) from the sibling CME to enable the C[01]_IVRM_DROPOUT function. These bits must be set to '11' for the non-QUAD manager CME.
38	RW	CME_SCOM_IDCR_CACHE_DROPOUT_ENABLE: Connected to cme_dropout_enable_out(2). This bit is also ANDed with cme_dropout_enable_in(2) to enable the CACHE_IVRM_DROPOUT function in this CME. This bit must also be set to '1' for the non-QUAD manager CME.
39	RW	CME_SCOM_IDCR_SPARE: Implemented but not used.
40	RW	CME_SCOM_IDCR_DROPOUT_NOTIFY_ENABLE: Causes dropout indication to notify the QPPM macro by enabling the UNMASKED FIR bits for the three Dropout errors to OR with the QPPM_IVRM_DROPOUT signal.
41:43	RW	CME_SCOM_IDCR_SPARE41_43: Implemented but not used.
44:58	RO	constant = 0b000000000000000
59:63	RW	CME_SCOM_IDCR_DROPOUT_SAMPLE_RATE: Sample rate used when DROOP_CHAR_MODE = 0, whose meaning is dependent on the value of DROOP_TIMER_MODE: 0 = This field specifies the rising edge of which bit of the QFMR[CYCLES] to use to start a new sample window. 1 = Bits (1:4) of this field are used as a TSEL using the PPE timer to select which output bit is used to start a new sample window (bit 0 unused). This delay is defined as $2^{(29 - \text{select})}$ / Nest_Frequency. The default value for this register corresponds to 262 µs (assuming a 2 GHz processor bus). Note that when this register is written, the first sample window will be truncated (smaller) than the selected value dependent on the relative value in the selected timer being used. An event threshold may still be reached despite the smaller window.

Register Name	**CME_SCOM CME Core iVRM Dropout Sample Register**
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_CIDSR
Address	000000001301242E (SCOM)
Description	CME_SCOM CME Core IVRM Dropout Sample Register

Bits	SCOM	Field Mnemonic: Description
0:23	ROX	CME_SCOM_CIDSR_C0_DROPOUT_EVENT_COUNT: Count of how many sustained dropouts have been detected for the core chiplet 0 iVRM. This counter always saturates at 0xFFFFFF and clears when the IDCR is written. Additionally, the behavior of this field depends on the value of IDCR[DROPOUT_CHAR_MODE].
24:31	ROX	CME_SCOM_CIDSR_C0_DROPOUT_INAROW_COUNT: Counter recording how many dropout indications for the core chiplet 0 iVRM have occurred in a row form a sustained dropout period. This field increments on each dropout present and resets when either: a) this field equals the DROPOUT_INAROW_THRESHOLD, b) the dropout present indicator = 0, or c) the IDCR register is written. Note that if a reset occurs on a cycle when dropout is present, the counter is set to a value of '1' else it resets to '0'. Also note when in CHAR_MODE, starting a new sample window does not affect this counter.

Bits	SCOM	Field Mnemonic: Description
32:55	ROX	CME_SCOM_CIDSR_C1_DROPOUT_EVENT_COUNT: Count of how many sustained dropouts have been detected for the core chiplet 1 iVRM. This field operates like the core chiplet 0 counter in the preceding fields.
56:63	ROX	CME_SCOM_CIDSR_C1_DROPOUT_INAROW_COUNT: Counter recording how many dropout indications for the core chiplet 1 iVRM have occurred in a row form a sustained dropout period. This field operates like the core chiplet 0 counter in the preceding fields.

Register Name	CME_SCOM CME QUAD/Cache iVRM Dropout Sample Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_QIDSR
Address	000000001301242F (SCOM)
Description	CME_SCOM CME QUAD/Cache iVRM dropout sample register

Bits	SCOM	Field Mnemonic: Description
0:23	ROX	CME_SCOM_QIDSR_CACHE_DROPOUT_EVENT_COUNT: Count of how many sustained dropouts have been detected for the cache chiplet iVRM. This field operates like the core chiplet counters in the preceding register.
24:31	ROX	CME_SCOM_QIDSR_CACHE_DROPOUT_INAROW_COUNT: Counter recording how many dropout indications for the cache chiplet iVRM have occurred in a row form a sustained dropout period. This field operates like the core chiplet counters in the preceding register.
32:34	ROX	CME_SCOM_QIDSR_DROPOUT_SAMPLE: Instantaneous values coming directly from the iVRM dropout signals. Bit0 = Core0 (Core2 for CME1). Bit1 = Core1 (Core3 for CME1). Bit2 = Cache.
35:61	RO	constant = 0b000000000000000000000000000

Register Name	CME_SCOM CME Block Copy Engine Base Address 0 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_BCEBAR0
Address	0000000013012430 (SCOM)
Description	CME_SCOM CME block copy engine base address register0

Bits	SCOM	Field Mnemonic: Description
0:7	RO	constant = 0b00000000
8:43	RW	CME_SCOM_BCEBAR0_BASE: Specifies bits 8:43 of the processor bus base address of the mapping. If this mapping is enabled (BCEBAR[SIZE] is not 0), the base address is required to be aligned such that the BCEBAR[SIZE] - 1 low-order bits of the field are '0'.
44:56	RO	constant = 0b0000000000000
57:58	RW	CME_SCOM_BCEBAR0_RD_SCOPE: Scope for read transaction broadcasts across the processor bus to the system memory controllers. Used to optimize processor bus traffic and latency. **Note:** Should be set intelligently based on known physical memory mapping based on CME memory location affinity.
59	RW	CME_SCOM_BCEBAR0_WR_SCOPE: Scope for write transaction broadcasts. See above for definition. **Note:** Local node scope is not allowed for writes through the NCU.
60	RW	CME_SCOM_BCEBAR0_VG_TARGET_SEL: Selects the 16-bit target for vectored group transactions to use. **Note:** This bit is ignored for read transactions when RD_SCOPE != 01 or for write transactions when WR_SCOPE != 1, in which case the target is always 0x0000. This bit should only be set as a workaround for power bus issues.

Bits	SCOM	Field Mnemonic: Description
61:63	RW	CME_SCOM_BCEBAR0_SIZE: Specifies the size of the mapping: 0 = Mapping disabled 1 = 1 MB 2 = 2 MB 3 = 4 MB 4 = 8 MB 5 = 16 MB 6 = 32 MB 7 = 64 MB

Register Name	CME_SCOM CME Block Copy Engine Base Address 1 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_BCEBAR1
Address	0000000013012431 (SCOM)
Description	CME_SCOM CME block copy engine base address register 1

Bits	SCOM	Field Mnemonic: Description
0:7	RO	constant = 0b00000000
8:43	RW	CME_SCOM_BCEBAR1_BASE: Specifies bits 8:43 of the processor bus base address of the mapping. If this mapping is enabled (BCEBAR[SIZE] not 0), the base address is required to be aligned such that the BCEBAR[SIZE] - 1 low-order bits of the field are '0'.
44:56	RO	constant = 0b0000000000000
57:58	RW	CME_SCOM_BCEBAR1_RD_SCOPE: Scope for read transaction broadcasts across the processor bus to the system memory controllers. Used to optimize processor bus traffic and latency. **Note:** Should be set intelligently based on known physical memory mapping based on CME memory location affinity.
59	RW	CME_SCOM_BCEBAR1_WR_SCOPE: Scope for write transaction broadcasts. See above for definition. **Note:** Local node scope is not allowed for writes through the NCU.
60	RW	CME_SCOM_BCEBAR1_VG_TARGET_SEL: Selects the 16-bit target for vectored group transactions to use. **Note:** This bit is ignored for read transactions when RD_SCOPE != 01 or for write transactions when WR_SCOPE != 1, in which case the target is always 0x0000. This bit should only be set as a workaround for power bus issues.
61:63	RW	CME_SCOM_BCEBAR1_SIZE: Specifies the size of the mapping: 0 = Mapping disabled 1 = 1 MB 2 = 2 MB 3 = 4 MB 4 = 8 MB 5 = 16 MB 6 = 32 MB 7 = 64 MB

Register Name	CME_SCOM CME QUAD Frequency Measurement Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_QFMR
Address	0000000013012432 (SCOM)
Description	CME_SCOM CME QUAD frequency measurement register

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	CME_SCOM_QFMR_TIMEBASE: CME Timebase free-running counter whose least significant bit increments every CME timer input pulse, which will be configured to run at nest (processor bus) clock64. (At 2 GHz, this will increment every 32 ns, and this counter will wrap every 137 seconds.) Firmware must perform all delta calculations (including accounting for the wrap condition) to perform elapsed time functions.
32:63	ROX	CME_SCOM_QFMR_CYCLES: Free-running cycle counter, that accumulates number of QUAD cycles4. Delta of this field per unit time (using the TIMEBASE field in this register) allows for an accurate average frequency calculation. The calculation is made as follows: CoreFreqavg = (Freqnest 8) * delta(CYCLESA,CYCLESB) delta(TIMEBASEA,TIMEBASEB) where the delta(A,B) function includes counter wraproll-over correction as follows: delta(A,B) = (((D=B-A)<0) ? D+=232 : D).

Register Name	CME_SCOM CME Average Frequency Sample Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_AFSR
Address	0000000013012433 (SCOM)
Description	CME_SCOM CME average frequency sample register

Bits	SCOM	Field Mnemonic: Description
0:19	ROX	CME_SCOM_AFSR_INST_CYCLE_SAMPLE: Instantaneous count of the number of cycles that elapsed during the last sample period. Allows firmware to perform an average frequency calculation over the most recent sample period. The sample rate is controlled by FWMR[AVG_FREQ_TSEL]. The average frequency can then be calculated by firmware as: (Nest_Frequency* INST_CYCLE_SAMPLE 2^(29-FWMR[AVG_FREQ_TSEL])).
20:31	RO	constant = 0b000000000000
32:51	ROX	CME_SCOM_AFSR_AVG_CYCLE_SAMPLE: Running average of sampled cycles collected since the last read to this register. Allows firmware to perform a slightly longer term average frequency calculation. **Note:** Reads reset this field to INST_CYCLE_SAMPLE. For every INST_CYCLE_SAMPLE sample, the hardware performs the following calculation: AVG_CYCLE_SAMPLE = (3*AVG_CYCLE_SAMPLE + INST_CYCLE_SAMPLE)4. This means that after four samples this field will contain: 32% previous avg + 11% three samples ago + 14% two samples ago + 19% the last sample + 25% INST_CYCLE_SAMPLE, which is approximately: 13 *previous AVG_CYCLE_SAMPLE + 25 * average of last 3 samples + 14 INST_CYCLE_SAMPLE.
52:62	RO	constant = 0b00000000000
63	ROX_CLRPART	CME_SCOM_AFSR_SAMPLE_VALID: A sample has occurred and caused this register to be updated since the last time it was read.

Register Name	CME_SCOM CME Average Frequency Threshold Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_AFTR
Address	0000000013012434 (SCOM)
Description	CME_SCOM CME average frequency threshold register

Bits	SCOM	Field Mnemonic: Description
0:19	ROX	CME_SCOM_AFTR_MAX_CYCLE_SAMPLE: Largest INST_CYCLE_SAMPLE value that occurred since the last read to this register. **Note:** Reads reset this field to AFSR[INST_CYCLE_SAMPLE].

Bits	SCOM	Field Mnemonic: Description
20:31	RO	constant = 0b000000000000
32:51	ROX	CME_SCOM_AFTR_MIN_CYCLE_SAMPLE: Smallest INST_CYCLE_SAMPLE value that occurred since the last read to this register. **Note:** Reads reset this field to AFSR[INST_CYCLE_SAMPLE].
52:63	RO	constant = 0b000000000000

Register Name	**CME_SCOM CME VDM Droop Count Register**
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_VDCR
Address	0000000013012435 (SCOM)
Description	CME_SCOM CME VDM Droop Count Register

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	CME_SCOM_VDCR_VDM_EXTREME_DROOP_CTR: Extreme droop threshold counter (16b). This counter always saturates at 0xFFFF and clears when the VDSR is written. Otherwise the behavior of this field depends on the value of DROOP_CHAR_MODE. (Increments when b'0xxx'.)
16:39	ROX	CME_SCOM_VDCR_VDM_LARGE_DROOP_CTR: Large droop threshold counter (24b). This counter always saturates at 0xFFFFFF and clears when the VDSR is written. Otherwise the behavior of this field depends on the value of DROOP_CHAR_MODE. (Increments when b'10xx'.)
40:63	ROX	CME_SCOM_VDCR_VDM_SMALL_DROOP_CTR: Small droop threshold counter (24b). This counter always saturates at 0xFFFFFF and clears when the VDSR is written. Otherwise the behavior of this field depends on the value of DROOP_CHAR_MODE. (Increments when b'110x'.)

Register Name	**CME_SCOM CME VDM No-Droop Count Register**
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_VNCR
Address	0000000013012436 (SCOM)
Description	No-droop count register

Bits	SCOM	Field Mnemonic: Description
0:15	RO	constant = 0b0000000000000000
16:39	ROX	CME_SCOM_VNCR_VDM_NO_DROOP_CTR: No droop threshold counter (24b). This counter always saturates at 0xFFFFFF and clears when the VDSR is written. Otherwise the behavior of this field depends on the value of DROOP_CHAR_MODE and DROOP_TIMER_MODE. (Increments when b'1110'.)
40:63	ROX	CME_SCOM_VNCR_VDM_OVERVOLT_CTR: Over-volt threshold counter (24b). This counter always saturates at 0xFFFFFF and clears when the VDSR is written. Otherwise the behavior of this field depends on the value of DROOP_CHAR_MODE and DROOP_TIMER_MODE. (Increments when b'1111'.)

Register Name	**CME_SCOM CME VDM Data Sample Register**
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_VDSR
Address	0000000013012437 (SCOM)
Description	CME_SCOM CME VDM data sample register

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	CME_SCOM_VDSR_INSTANT_VDM_CONTROL_SUMMARY: Instantaneous VDM summary to DPLL.

Bits	SCOM	Field Mnemonic: Description
4:7	ROX	CME_SCOM_VDSR_INSTANT_CACHE_VDM_DATA: Instantaneous cache VDM output.
8:11	ROX	CME_SCOM_VDSR_INSTANT_CORE0_VDM_DATA: Instantaneous core chiplet 0 VDM output.
12:15	ROX	CME_SCOM_VDSR_INSTANT_CORE1_VDM_DATA: Instantaneous core chiplet 1 VDM output.
16:19	ROX	CME_SCOM_VDSR_INSTANT_CORE2_VDM_DATA: Instantaneous core chiplet 2 VDM output.
20:23	ROX	CME_SCOM_VDSR_INSTANT_CORE3_VDM_DATA: Instantaneous core chiplet 3 VDM output.
24:31	RO	constant = 0b00000000
32:35	ROX	CME_SCOM_VDSR_STICKY_VDM_CONTROL_SUMMARY: Worst case VDM summary to DPLL per-cycle sticky-AND operation. Resets to 1111 on read.
36:39	ROX	CME_SCOM_VDSR_STICKY_CACHE_VDM_DATA: Worst case cache VDM output per-cycle sticky-AND operation. Resets to 1111 on read.
40:43	ROX	CME_SCOM_VDSR_STICKY_CORE0_VDM_DATA: Worst case core chiplet 0 VDM output per-cycle sticky-AND operation. Resets to 1111 on read.
44:47	ROX	CME_SCOM_VDSR_STICKY_CORE1_VDM_DATA: Worst case core chiplet 1 VDM output per-cycle sticky-AND operation. Resets to 1111 on read.
48:51	ROX	CME_SCOM_VDSR_STICKY_CORE2_VDM_DATA: Worst case core chiplet 2 VDM output per-cycle sticky-AND operation. Resets to 1111 on read.
52:55	ROX	CME_SCOM_VDSR_STICKY_CORE3_VDM_DATA: Worst case (sticky) core chiplet 3 VDM output per-cycle sticky-AND operation. Resets to 1111 on read.
56:63	RO	constant = 0b00000000

Register Name	**CME_SCOM CME VDM Event Count Register**
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_VECR
Address	0000000013012438 (SCOM)
Description	CME_SCOM CME VDM Event Count Register

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	CME_SCOM_VECR_TOTAL_DROOP_EVENT_CTR: Total number of droop events detected (starting from Overvolt or No-Droop condition, regardless of depth).
16:31	ROX	CME_SCOM_VECR_SMALL_EVENT_PROFILE_CTR: Number of small droop profiled events. Counts how often the small droop event > small threshold based on DROOP_PROFILE_TYPE. 00 = Total droop duration (small or deeper). 01 = Small-only droop duration (without ever going deeper). 10 = Small-in-a-row duration (despite going deeper, before or after). 11 = Small-only in-a-row duration (without ever going deeper).
32:43	ROX	CME_SCOM_VECR_LARGER_DROOP_EVENT_CTR: Number of large (or deeper) droop events detected (starting from over-volt or no-droop droop condition).
44:55	ROX	CME_SCOM_VECR_LARGE_EVENT_PROFILE_CTR: Number of large droop profiled events. Counts how often the large droop event > large threshold based on DROOP_PROFILE_TYPE. 00 = Total droop duration (large or deeper). 01 = Large-only droop duration (without ever going deeper). 10 = Large-in-a-row duration (despite going deeper, before or after). 11 = Large-only in-a-row duration (without ever going deeper).
56:63	ROX	CME_SCOM_VECR_EXTREME_DROOP_EVENT_CTR: Number of extreme droop profiled events, droop event > extreme threshold based on DROOP_PROFILE_TYPE. 00 or 01 = Total extreme droop duration (deeper not possible). 10 or 11 = Extreme-in-a-row duration (deeper not possible).

Register Name	CME_SCOM CME VDM Count Threshold Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_VCTR
Address	0000000013012439 (SCOM)
Description	CME_SCOM CME VDM count threshold register

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CME_SCOM_VCTR_VDM_EXTREME_DROOP_THRESHOLD: Extreme droop threshold. A value of all zeros disables this threshold. Otherwise, when DROOP_CHAR_MODE = '0', if this value matches the count value for this same field in VDCR, an LFIR[extreme_droop_err] is indicated.
16:39	RW	CME_SCOM_VCTR_VDM_LARGE_DROOP_THRESHOLD: Large droop threshold. A value of all zeros disables this threshold. Otherwise, when DROOP_CHAR_MODE = '0', if this value matches the count value for this same field in VDCR, an LFIR[large_droop_err] is indicated.
40:63	RW	CME_SCOM_VCTR_VDM_SMALL_DROOP_THRESHOLD: Small droop threshold. A value of all zeros disables this threshold. Otherwise, when DROOP_CHAR_MODE = '0', if this value matches the count value for this same field in VDCR, an LFIR[small_droop_err] is indicated.

Register Name	CME_SCOM CME Local Mode Control Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_LMCR
Address	000000001301243A (SCOM) 000000001301243B (SCOM1) 000000001301243C (SCOM2)
Description	CME_SCOM CME local mode control register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_PMCR_OVERRIDE_EN: Enables SCOM writes to both PMCRS registers for manual testing access. Disables core chiplet updates from the PMCR serial interface from PC. 0 = Core shifter updates are accepted; SCOM updates are blocked and return an invalid access return code. 1 = SCOM updates are accepted; core shifter updates are ignored. **Note:** This bit is intended to only be changed during IPL, not during run time.
1	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_PSCR_OVERRIDE_EN: Enables SCOM write to the PSCRS registers for manual testing access. Disables core chiplet updates from the PSCR serial interface from PC. Same behavior as the previous bit.
2	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_PMSR_OVERRIDE_EN: Enable SCOM control for the stop-GPE or manual testing to serially shift values into the processor cores. 0 = CME writes are accepted; SCOM updates are ignored and return an invalid access return code. 1 = SCOM writes are accepted; CME writes are blocked and timeout (PPE MCHK) will occur. **Note:** This bit is intended to only be changed during IPL, not during run time.
3	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_BCECSR_OVERRIDE_EN: Disables local register writes to the BCECSR to allow SCOM to perform block copy operations to the CME SRAM instead. Same behavior as the previous bit.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
4	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_IDR_LCL_SAMPLE_EN: Allow the CME local interface to control the iVRM Dropout Data and Configuration Registers. If this bit is set to 1 and SCOM attempts to read the CIDSR and QIDSR or to write the IDCR, an invalid access error code is returned on the SCOM interface. If this bit is 0, CME attempts to read the CIDSR and QIDSR or to write the IDCR local registers are ignored (will cause a timeout) and do not clear the sample registers.
5	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_VDM_LCL_SAMPLE_EN: Allow the CME local interface to sample the VDM sample registers. If this bit is set to 1 and SCOM attempts to read the VCSR or VDSR, an invalid access error code is returned on the SCOM interface. If this bit is 0, CME attempts to read the VCSR, and VDSR local registers are ignored (will cause a timeout) and do not clear the registers.
6	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_FREQ_LCL_SAMPLE_EN: Allow the CME local interface to sample the Frequency Sample Registers. If this bit is set to 1 and SCOM attempts to read the AFSR or AFTR, an invalid access error code is returned on the SCOM interface. If this bit is 0, CME attempts to read the AFSR, and AFTR local registers are ignored (will cause a timeout) and do not clear the registers.
7	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_LOCK_PCB_ON_ERR: When set, unmasked PCB errors will cause the PCB queue logic to lock or stop accepting new PCB requests from the memory bolt-on, in order to preserve debug data in the interface registers.
8	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_QUEUED_WR_EN: Enable CME to perform queued PCB write operations. If not set, attempts to store to queued PCB address encodes will return a DSI error to PPE.
9	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_QUEUED_RD_EN: Enable CME to perform queued PCB read operations. If not set, attempts to load from queued PCB address encodes will return a DSI error to PPE.
10	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_MASK_PURGE_INTERFACE: Suppress CME from sending and receiving purge request to the L2, NCU, and CHTM. When this bit is set, the PURGE and PURGE_ABORT bits in the SICR should be gated off to always output zero from the CME to those units, and mask off the PURGE_DONE inputs from those units into the EISR (but does not mask off the corresponding EIIR bits).
11	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_SPARE_11: Implemented but unused.
12	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_C0_AUTO_SPECIAL_WAKEUP_DISABLE: When set, do not automatically force PM_EXIT = 1 and PM_ENTRY_ACK = 0 to core 0 in response to special wake-up request, and do not automatically assert done back to the core PPM (instead use the values in the SICR). **Notes:** 1. This bit should be set by CME Hcode when core chiplet is in a STOP state > 1 or transitioning in or out of the STOP state. 2. When this mode is set, special wake-up interrupts in the EIMR must never be masked by code during run time (but otherwise, in auto mode, special wake-ups should only be unmasked when the core is in Stop state). This bit should be cleared by Hcode when the core is in a Stop state such that special wake-up transitions intersecting with regular wake-ups do not create blips on PM_EXIT and confuse the PC logic.
13	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_C1_AUTO_SPECIAL_WAKEUP_DISABLE: Same as previous bit, but for core chiplet 1.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
14	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_C0_HALTED_STOP_OVERRIDE_DISABLE: By default the POWER9 core chiplets should be allowed to automatically go in and out of STOP state when the PPE is halted and not available to service its STOP entry and exit requests (in effect converting all Stop requests to a Level 1). This allows the system to continue running when the CME is being halted for lab debug, or in the unlikely event that a CME error happens. This bit should be set by CME Hcode when either core chiplet is in a STOP state > 1 or transitioning in or out of STOP state. 1 = PPE halted has no effect on the PC STOP interface signals to core chiplet 0. 0 = PPE halted indication is ORed with the CME_SCOM_FWMR[STOP_OVERRIDE_MODE] functionality for core chiplet 0.
15	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_C1_HALTED_STOP_OVERRIDE_DISABLE: Same as previous bit, but for core chiplet 1.
16	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_STOP_OVERRIDE_MODE: Override to disable CME being involved in Stop sequencing, in effect converting all new stop requests into Stop Level 1. Setting this mode will prevent the core chiplets from hanging on STOP instructions if the CME doesn't respond. Available to software or simulation as a workaround. (Equivalent to setting both treat_sleep_as nap and treat_winkle_as_sleep in POWER8). **Note:** The user is responsible to first special wake-up the core chiplets corresponding to this CME before changing this bit. **Implementation note:** When set, always assert PM_ENTRY_ACK, PM_WAKE_UP, and deassert BLOCK_INTERRUPTS to both core chiplets, regardless of the values of these controls in SICR.
17	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_STOP_ACTIVE_MASK: This mode will gate off PC_PM_STATE_ACTIVE from both core chiplets from setting the EISR (using the interrupt bolt-on fence such that it is still visible in the EINR), allowing the EIMR to remain unchanged. **Note:** Must only be set if STOP_OVERRIDE_MODE = 1, otherwise PC (and therefore the core chiplet) will hang.
18	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_AUTO_STOP1_DISABLE: Disables instant entry and exit Nap mode for Stop 1 without CME code involvement. This bit must be set to enable auto-promote or CME hardware workarounds for the Stop 1 state. When this bit is set, the CME is responsible for controlling the Stop interface to PC via the SICR for Stop Level 1 transitions. **Note:** The user is responsible to first special wake-up the core chiplets corresponding to this CME before changing this bit. When this bit is set, STOP1_ACTIVE_ENABLE must also be set. **Implementation note:** When a Core Chiplet asserts PC_PM_STATE_ACTIVE with PC_PM_STATE = 1 (or = 0 although it should never occur), the hardware by default automatically asserts the Stop interface control signals to that core chiplet as described in STOP_OVERRIDE MODE without CME involvement. Setting this bit disables that hardware functionality.
19	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_STOP1_ACTIVE_ENABLE: This mode will enable PC_PM_STATE_ACTIVE from a core chiplet to set the EISR when a core chiplet asserts PC_PM_STATE_ACTIVE with PC_PM_STATE = 1 (or = 0 although it should never occur), allowing the EIMR to remain unchanged. Otherwise, the EISR for that core chiplet (using the interrupt bolt-on fence such that it is still visible in the EINR) is not set for this condition.
20	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_FENCE_EISR: Fence off all interrupt inputs from causing EISR bits to be set. May be used for workarounds to keep from having to clean up the EISR afterwards. **Note:** Implemented in hardware by asserting all fence inputs to the ICB.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
21	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_PC_DISABLE_DROOP: Assert disable droop signal to both cores. Used to temporarily disable instruction throttling for workarounds or reconfiguration. ORed with CME_LCL_LMCR to feed a single output of CME.
22:23	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_SPARE_22_23: Implemented but unused.
24:27	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_AVG_FREQ_TSEL: Sample rate used by the AFSR[INST_CYCLE_SAMPLE] calculation, using the PPE timer, defined as $2^{(29 - select)}$ / Nest_Frequency. This field selects which timer output bit is used to sample the sample cycle counter. **Note:** It is the user's responsibility to ensure that the value chosen never exceeds the equivalent of 2^{31} processor cycles, otherwise the sample will wrap and the calculation will be invalid. The default value for this register corresponds to 262 µs (assuming a 2 GHz processor bus).
28:31	RW	WO_CLEAR	WO_OR	CME_SCOM_LMCR_SPARE_28_31: Implemented but unused.
32	WO_4P	NCX	WO_4P	CME_SCOM_LMCR_RESET_IMPRECISE_QERR: Reset the PCB queue imprecise error, to unlock the CME core SIB interface after an error occurs on a queued transaction.
33	WO_4P	NCX	WO_4P	CME_SCOM_LMCR_SET_ECC_INJECT_ERR: Write 1 to this bit causes an SRAM error to be injected by setting ECC_INJECT_ERR in the CME_SCOM_FWMR. **Note:** The ECC_INJECT_TYPE of error injected is only controllable by firmware in the CMEFWM.
34:62	RO	RO	RO	constant = 0b00000000000000000000000000000

Register Name	CME_SCOM CME Local Core Stop Interface Control Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_SICR
Address	000000001301243D (SCOM) 000000001301243E (SCOM1) 000000001301243F (SCOM2)
Description	CME_SCOM CME local core stop interface control register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_PM_ENTRY_ACK_C0: Core 0 STOP entry acknowledgment to PC. **Note:** Output may also be asserted automatically for STOP level1 or if the CME is halted as per LMCR bit 34.
1	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_PM_ENTRY_ACK_C1: Core 1 STOP entry acknowledgment to PC. **Note:** Output may also be asserted automatically for STOP level1 or if the CME is halted as per LMCR bit 35.
2	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_PM_BLOCK_INTERRUPTS_C0: Core 0 block interrupts from allowing PC to start instructions in STOP state. **Note:** Output may also be asserted automatically for STOP level1 or if the CME is halted as per LMCR bit 34.
3	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_PM_BLOCK_INTERRUPTS_C1: Core 1 block interrupts from allowing PC to start instructions in STOP state. **Note:** Output may also be asserted automatically for STOP level1 or if the CME is halted as per LMCR bit 35.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
4	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_PM_EXIT_C0: Core 0 request for PC to exit STOP state. **Note:** Output may also be asserted automatically for STOP level1 or if the CME is halted as per LMCR bit 34.
5	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_PM_EXIT_C1: Core 1request for PC to exit STOP state. **Note:** Output may also be asserted automatically for STOP level1 or if the CME is halted as per LMCR bit 35.
6	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_PCC_CORE_INTF_QUIESCE_C0: Core 0 processor common core logical fence.
7	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_PCC_CORE_INTF_QUIESCE_C1: Core 1 processor common core logical fence.
8	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_L2_CORE_INTF_QUIESCE_C0: Core 0 logical fence to the L2.
9	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_L2_CORE_INTF_QUIESCE_C1: Core 1 logical fence to the L2.
10	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_PCBMUX_REQ_C0: Core 0 PCB multiplexer request. See SISR for Grant.
11	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_PCBMUX_REQ_C1: Core 1 PCB multiplexer request. See SISR for grant.
12:15	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_RESERVED_12_15: Implemented but unused.
16	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_SPECIAL_WKUP_DONE_C0: Connected to special wake-up done output to core 0 PPM only when LMCR[SPECIAL_WAKEUP_DONE_OVERRIDE] = 1.
17	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_SPECIAL_WKUP_DONE_C1: Connected to special wake-up done output to core1 PPM only when LMCR[SPECIAL_WAKEUP_DONE_OVERRIDE] = 1.
18	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_L2_PURGE: L2 purge request.
19	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_L2_PURGE_ABORT: L2 purge abort.
20	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_PC_THROTTLE_REQ: Requests PC to engage instruction throttling to both core chiplets.
21	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_NCU_TLBIE_QUIESCE: Request NCU to start ignoring new incoming TLBIEs.
22	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_NCU_PURGE: NCU purge request (needed for QUAD STOP states).
23	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_NCU_PURGE_ABORT: NCU purge abort (needed for QUAD STOP states).
24	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_CHTM_PURGE_C0: Core 0 CHTM purge request (needed for for QUAD STOP states).
25	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_CHTM_PURGE_C1: Core 1 CHTM purge request (needed for QUAD STOP states).
26	WO_4P	NC	WO_4P	CME_SCOM_SICR_HMI_REQUEST_C0: Pulse that sets a bit in Core0 HMER register to send an interrupt to the hypervisor. Intended for debug or workarounds.
27	WO_4P	NC	WO_4P	CME_SCOM_SICR_HMI_REQUEST_C1: Pulse that sets a bit in Core1 HMER register to send an interrupt to the hypervisor. Intended for debug or workarounds.
28	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_PPM_SPARE_OUT_C0: Spare output signal to Core 0 PPM.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
29	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_PPM_SPARE_OUT_C1: Spare output signal to Core 1 PPM.
30:31	RW	WO_CLEAR	WO_OR	CME_SCOM_SICR_RESERVED_30_31: Implemented but unused.
32:63	RO	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	CME_SCOM Power Management Status Shadow Core 0 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_PMSRS0
Address	0000000013012440 (SCOM)
Description	CME_SCOM power management status register shadow core0

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	CME_SCOM_PMSRS0_DATA: Meaning is defined by firmware usage. Intended to communicate information such as the actual Pstate, chip and system limits, and other power management state data back to the hypervisor.

Register Name	CME_SCOM Power Management Status Shadow Core 1 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_PMSRS1
Address	0000000013012441 (SCOM)
Description	CME_SCOM power management status register shadow core1

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	CME_SCOM_PMSRS1_DATA: Meaning is defined by firmware usage. Intended to communicate information such as the actual Pstate, chip and system limits, and other power management state data back to the hypervisor.

Register Name	CME_SCOM Power Management Control Shadow Core 0 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_PMCRS0
Address	0000000013012442 (SCOM)
Description	CME_SCOM power management control register shadow core0

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	CME_SCOM_PMCRS0_DATA: Meaning is defined by firmware usage. Intended to communicate Pstate requests and hints to power management firmware.

Register Name	CME_SCOM Power Management Control Shadow Core 1 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_PMCRS1
Address	0000000013012443 (SCOM)
Description	CME_SCOM power management control register shadow core1

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	CME_SCOM_PMCRS1_DATA: Meaning is defined by firmware usage. Intended to communicate Pstate requests and hints to power management firmware.

Register Name	Processor Stop Control Core 0 Shadow Thread 0 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_PSCRS00
Address	0000000013012444 (SCOM)
Description	Processor stop control register core 0 shadow thread 0

Bits	SCOM	Field Mnemonic: Description
0	RWX	CME_SCOM_PSCRS00_SPARE0: Implemented but unused.
1	RWX	CME_SCOM_PSCRS00_OS_STATUS_DISABLE_A_N: OS status disable. Corresponds to PSSCR[41]. When set to 1, causes the status field to return all 0's when read by OS.
2	RWX	CME_SCOM_PSCRS00_STATE_LOSS_ENABLE_A_N: Stop state loss enable. Corresponds to PSSCR[42]. When set, allows hardware to lose state, for example, to allocate core resource to the remaining threads.
3	RWX	CME_SCOM_PSCRS00_EXIT_CRITERION_A_N: Stop exit criterion. Corresponds to PSSCR[43]. 0 = Exit power-saving mode on any interrupt without any state loss. 1 = Exit power-saving mode only on LPCR PECE conditions and take system reset interrupt with HV = 1; state loss is allowed and implementation-dependent.
4:7	RWX	CME_SCOM_PSCRS00_POWER_SAVING_LIMIT_A_N: Power-saving level limit. Corresponds to PSSCR[44:47]. Causes an OS stop request greater than or equal to this value to take an interrupt to the hypervisor instead.
8	RWX	CME_SCOM_PSCRS00_HYP_VIRT_EXIT_ENABLE: Hypervisor virtualization exit enable. Corresponds to PECE[17], and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
9	RWX	CME_SCOM_PSCRS00_EXT_EBB_EXIT_ENABLE: External event-based branch exit enable. Corresponds to PECE[18], and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
10	RWX	CME_SCOM_PSCRS00_EXT_RESUME_EXIT_ENABLE: External resume exit enable. Corresponds to PECE[19], and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
11	RWX	CME_SCOM_PSCRS00_EXT_EXIT_ENABLE: External OS exit enable. Corresponds to PECE[49], and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
12	RWX	CME_SCOM_PSCRS00_DEC_EXIT_ENABLE: Decrementer exit enable. Corresponds to PECE[50]. Unused by CME since this exit event is handled inside the core directly. Available to CME only for potential workarounds or sampling.
13	RWX	CME_SCOM_PSCRS00_HMI_EXIT_ENABLE: Hypervisor maintenance interrupt exit enable. Corresponds to PECE[51] and enables the malfunction alert interrupt source in WSR[32] to cause an exit from STOP state.
14:15	RWX	CME_SCOM_PSCRS00_LEVEL_TRANSITION_RATE_A_N: Stop level transition rate field. Corresponds to PSSCR[54:55]. The requested rate of progression from initial to maximum power-saving level if stop promote is implemented. The rate of progression increases with the value of the level transition rate field. Actual rates corresponding to each value are defined by firmware and are TBD.
16:19	RWX	CME_SCOM_PSCRS00_MAX_PROMOTE_LEVEL_A_N: Maximum stop request level. Corresponds to PSSCR[56:59]. Allows hardware to auto-promote to deeper levels as the power-saved core ages (without waking up). Setting this field ≤ initial request level disables promotion. Setting this field to zero always disables auto-promotion. See STOP_REQUEST_LEVEL encoding in the following field.

Bits	SCOM	Field Mnemonic: Description
20:23	RWX	CME_SCOM_PSCRS00_STOP_REQUEST_LEVEL_A_N: Stop request level. Corresponds to PSSCR[60:63]. 0x0 = Stop 0 (Quiesce thread only). 0x1 = Stop 1 (legacy nap). 0x2 = Stop 2 (legacy fast sleep). 0x3 = Stop 3 (if supported, legacy fast sleep @V_{min} using iVRMs). 0x4 = Stop 4 (instant-on; legacy deep sleep without HV loss). 0x5 - 0x7 = Reserved. 0x8 = Stop 8 (legacy deep sleep plus shared L2 clock off). 0x9 = Stop 9 (legacy fast winkle, for lab and simulation only). 0xA = Reserved. 0xB = Stop 11 (legacy deep winkle). 0xC - 0xF = Reserved.
24:63	RO	constant = 0b0000000000000000000000000000000000000000

Register Name	Processor Stop Control Core 0 Shadow Thread 1 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_PSCRS01
Address	0000000013012445 (SCOM)
Description	Processor stop control register core 0 shadow thread 1

Bits	SCOM	Field Mnemonic: Description
0	RWX	CME_SCOM_PSCRS01_SPARE0: Implemented but unused.
1	RWX	CME_SCOM_PSCRS01_OS_STATUS_DISABLE_A_N: OS status disable. Corresponds to PSSCR[41]. When set to 1, causes the status field to return all 0's when read by OS.
2	RWX	CME_SCOM_PSCRS01_STATE_LOSS_ENABLE_A_N: Stop state loss enable. Corresponds to PSSCR[42]. When set, allows hardware to lose state, for example, to allocate core resource to the remaining threads.
3	RWX	CME_SCOM_PSCRS01_EXIT_CRITERION_A_N: Stop exit criterion. Corresponds to PSSCR[43]. 0 = Exit power-saving mode on any interrupt without any state loss. 1 = Exit power-saving mode only on LPCR PECE conditions and take system reset interrupt with HV = 1; state loss is allowed and implementation-dependent.
4:7	RWX	CME_SCOM_PSCRS01_POWER_SAVING_LIMIT_A_N: Power-saving level limit. Corresponds to PSSCR[44:47]. Causes an OS stop request greater than or equal to this value to take an interrupt to the hypervisor instead.
8	RWX	CME_SCOM_PSCRS01_HYP_VIRT_EXIT_ENABLE: Hypervisor virtualization exit enable. Corresponds to PECE[17], and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
9	RWX	CME_SCOM_PSCRS01_EXT_EBB_EXIT_ENABLE: External event-based branch exit enable. Corresponds to PECE[18], and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
10	RWX	CME_SCOM_PSCRS01_EXT_RESUME_EXIT_ENABLE: External resume exit enable. Corresponds to PECE[19], and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
11	RWX	CME_SCOM_PSCRS01_EXT_EXIT_ENABLE: External OS exit enable. Corresponds to PECE[49], and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
12	RWX	CME_SCOM_PSCRS01_DEC_EXIT_ENABLE: Decrementer exit enable. Corresponds to PECE[50]. Unused by CME since this exit event is handled inside the core directly. Available to CME only for potential workarounds or sampling.
13	RWX	CME_SCOM_PSCRS01_HMI_EXIT_ENABLE: Hypervisor maintenance interrupt exit enable. Corresponds to PECE[51] and enables the malfunction alert interrupt source in WSR[32] to cause an exit from STOP state.

Bits	SCOM	Field Mnemonic: Description
14:15	RWX	CME_SCOM_PSCRS01_LEVEL_TRANSITION_RATE_A_N: Stop level transition rate field. Corresponds to PSSCR[54:55]. The requested rate of progression from initial to maximum power-saving level if stop promote is implemented. The rate of progression increases with the value of the level transition rate field. Actual rates corresponding to each value are defined by firmware and are TBD.
16:19	RWX	CME_SCOM_PSCRS01_MAX_PROMOTE_LEVEL_A_N: Maximum stop request level. Corresponds to PSSCR[56:59]. Allows hardware to auto-promote to deeper levels as the power-saved core ages (without waking up). Setting this field ≤ initial request level disables promotion. Setting this field to zero always disables auto-promotion. See STOP_REQUEST_LEVEL encoding in the following field.
20:23	RWX	CME_SCOM_PSCRS01_STOP_REQUEST_LEVEL_A_N: Stop request level. Corresponds to PSSCR[60:63]. 0x0 = Stop 0 (Quiesce thread only). 0x1 = Stop 1 (legacy nap). 0x2 = Stop 2 (legacy fast sleep). 0x3 = Stop 3 (if supported, legacy fast sleep @V_{min} using iVRMs). 0x4 = Stop 4 (instant-on; legacy deep sleep without HV loss). 0x5 - 0x7 = Reserved. 0x8 = Stop 8 (legacy deep sleep plus shared L2 clock off). 0x9 = Stop 9 (legacy fast winkle, for lab and simulation only). 0xA = Reserved. 0xB = Stop 11 (legacy deep winkle). 0xC - 0xF = Reserved.
24:63	RO	constant = 0b0000000000000000000000000000000000000000

Register Name	Processor Stop Control Core 0 Shadow Thread 2 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_PSCRS02
Address	0000000013012446 (SCOM)
Description	Processor stop control register core 0 shadow thread 2

Bits	SCOM	Field Mnemonic: Description
0	RWX	CME_SCOM_PSCRS02_SPARE0: Implemented but unused.
1	RWX	CME_SCOM_PSCRS02_OS_STATUS_DISABLE_A_N: OS status disable. Corresponds to PSSCR[41]. When set to 1, causes the status field to return all 0's when read by OS.
2	RWX	CME_SCOM_PSCRS02_STATE_LOSS_ENABLE_A_N: Stop state loss enable. Corresponds to PSSCR[42]. When set, allows hardware to lose state, for example, to allocate core resource to the remaining threads.
3	RWX	CME_SCOM_PSCRS02_EXIT_CRITERION_A_N: Stop exit criterion. Corresponds to PSSCR[43]. 0 = Exit power-saving mode on any interrupt without any state loss. 1 = Exit power-saving mode only on LPCR PECE conditions and take system reset interrupt with HV = 1; state loss is allowed and implementation-dependent.
4:7	RWX	CME_SCOM_PSCRS02_POWER_SAVING_LIMIT_A_N: Power-saving level limit. Corresponds to PSSCR[44:47]. Causes an OS stop request greater than or equal to this value to take an interrupt to the hypervisor instead.
8	RWX	CME_SCOM_PSCRS02_HYP_VIRT_EXIT_ENABLE: Hypervisor virtualization exit enable. Corresponds to PECE[17], and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
9	RWX	CME_SCOM_PSCRS02_EXT_EBB_EXIT_ENABLE: External event-based branch exit enable. Corresponds to PECE[18], and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
10	RWX	CME_SCOM_PSCRS02_EXT_RESUME_EXIT_ENABLE: External resume exit enable. Corresponds to PECE[19], and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.

Bits	SCOM	Field Mnemonic: Description
11	RWX	CME_SCOM_PSCRS02_EXT_EXIT_ENABLE: External OS exit enable. Corresponds to PECE[49], and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
12	RWX	CME_SCOM_PSCRS02_DEC_EXIT_ENABLE: Decrementer exit enable. Corresponds to PECE[50]. Unused by CME since this exit event is handled inside the core directly. Available to CME only for potential workarounds or sampling.
13	RWX	CME_SCOM_PSCRS02_HMI_EXIT_ENABLE: Hypervisor maintenance interrupt exit enable. Corresponds to PECE[51] and enables the malfunction alert interrupt source in WSR[32] to cause an exit from STOP state.
14:15	RWX	CME_SCOM_PSCRS02_LEVEL_TRANSITION_RATE_A_N: Stop level transition rate field. Corresponds to PSSCR[54:55]. The requested rate of progression from initial to maximum power-saving level if stop promote is implemented. The rate of progression increases with the value of the level transition rate field. Actual rates corresponding to each value are defined by firmware and are TBD.
16:19	RWX	CME_SCOM_PSCRS02_MAX_PROMOTE_LEVEL_A_N: Maximum stop request level. Corresponds to PSSCR[56:59]. Allows hardware to auto-promote to deeper levels as the power-saved core ages (without waking up). Setting this field ≤ initial request level disables promotion. Setting this field to zero always disables auto-promotion. See STOP_REQUEST_LEVEL encoding in the following field.
20:23	RWX	CME_SCOM_PSCRS02_STOP_REQUEST_LEVEL_A_N: Stop request level. Corresponds to PSSCR[60:63]. 0x0 = Stop 0 (Quiesce thread only). 0x1 = Stop 1 (legacy nap). 0x2 = Stop 2 (legacy fast sleep). 0x3 = Stop 3 (if supported, legacy fast sleep @V_{min} using iVRMs). 0x4 = Stop 4 (instant-on; legacy deep sleep without HV loss). 0x5 - 0x7 = Reserved. 0x8 = Stop 8 (legacy deep sleep plus shared L2 clock off). 0x9 = Stop 9 (legacy fast winkle, for lab and simulation only). 0xA = Reserved. 0xB = Stop 11 (legacy deep winkle). 0xC - 0xF = Reserved.
24:63	RO	constant = 0b0000000000000000000000000000000000000000

Register Name	Processor Stop Control Core 0 Shadow Thread 3 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_PSCRS03
Address	0000000013012447 (SCOM)
Description	Processor stop control register core 0 shadow thread 3

Bits	SCOM	Field Mnemonic: Description
0	RWX	CME_SCOM_PSCRS03_SPARE0: Implemented but unused.
1	RWX	CME_SCOM_PSCRS03_OS_STATUS_DISABLE_A_N: OS status disable. Corresponds to PSSCR[41]. When set to 1, causes the status field to return all 0's when read by OS.
2	RWX	CME_SCOM_PSCRS03_STATE_LOSS_ENABLE_A_N: Stop state loss enable. Corresponds to PSSCR[42]. When set, allows hardware to lose state, for example, to allocate core resource to the remaining threads.
3	RWX	CME_SCOM_PSCRS03_EXIT_CRITERION_A_N: Stop exit criterion. Corresponds to PSSCR[43]. 0 = Exit power-saving mode on any interrupt without any state loss. 1 = Exit power-saving mode only on LPCR PECE conditions and take system reset interrupt with HV = 1; state loss is allowed and implementation-dependent.
4:7	RWX	CME_SCOM_PSCRS03_POWER_SAVING_LIMIT_A_N: Power-saving level limit. Corresponds to PSSCR[44:47]. Causes an OS stop request greater than or equal to this value to take an interrupt to the hypervisor instead.

Bits	SCOM	Field Mnemonic: Description
8	RWX	CME_SCOM_PSCRS03_HYP_VIRT_EXIT_ENABLE: Hypervisor virtualization exit enable. Corresponds to PECE[17], and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
9	RWX	CME_SCOM_PSCRS03_EXT_EBB_EXIT_ENABLE: External event-based branch exit enable. Corresponds to PECE[18], and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
10	RWX	CME_SCOM_PSCRS03_EXT_RESUME_EXIT_ENABLE: External resume exit enable. Corresponds to PECE[19], and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
11	RWX	CME_SCOM_PSCRS03_EXT_EXIT_ENABLE: External OS exit enable. Corresponds to PECE[49], and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
12	RWX	CME_SCOM_PSCRS03_DEC_EXIT_ENABLE: Decrementer exit enable. Corresponds to PECE[50]. Unused by CME since this exit event is handled inside the core directly. Available to CME only for potential workarounds or sampling.
13	RWX	CME_SCOM_PSCRS03_HMI_EXIT_ENABLE: Hypervisor maintenance interrupt exit enable. Corresponds to PECE[51] and enables the malfunction alert interrupt source in WSR[32] to cause an exit from STOP state.
14:15	RWX	CME_SCOM_PSCRS03_LEVEL_TRANSITION_RATE_A_N: Stop level transition rate field. Corresponds to PSSCR[54:55]. The requested rate of progression from initial to maximum power-saving level if stop promote is implemented. The rate of progression increases with the value of the level transition rate field. Actual rates corresponding to each value are defined by firmware and are TBD.
16:19	RWX	CME_SCOM_PSCRS03_MAX_PROMOTE_LEVEL_A_N: Maximum stop request level. Corresponds to PSSCR[56:59]. Allows hardware to auto-promote to deeper levels as the power-saved core ages (without waking up). Setting this field ≤ initial request level disables promotion. Setting this field to zero always disables auto-promotion. See STOP_REQUEST_LEVEL encoding in the following field.
20:23	RWX	CME_SCOM_PSCRS03_STOP_REQUEST_LEVEL_A_N: Stop request level. Corresponds to PSSCR[60:63]. 0x0 = Stop 0 (Quiesce thread only). 0x1 = Stop 1 (legacy nap). 0x2 = Stop 2 (legacy fast sleep). 0x3 = Stop 3 (if supported, legacy fast sleep @V_{min} using iVRMs). 0x4 = Stop 4 (instant-on; legacy deep sleep without HV loss). 0x5 - 0x7 = Reserved. 0x8 = Stop 8 (legacy deep sleep plus shared L2 clock off). 0x9 = Stop 9 (legacy fast winkle, for lab and simulation only). 0xA = Reserved. 0xB = Stop 11 (legacy deep winkle). 0xC - 0xF = Reserved.
24:63	RO	constant = 0b0000000000000000000000000000000000000000

Register Name	Processor Stop Control Core 1 Shadow Thread 0 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_PSCRS10
Address	0000000013012448 (SCOM)
Description	Processor stop control register core 1 shadow thread 0

Bits	SCOM	Field Mnemonic: Description
0	RWX	CME_SCOM_PSCRS10_SPARE0: Implemented but unused.
1	RWX	CME_SCOM_PSCRS10_OS_STATUS_DISABLE_A_N: OS status disable. Corresponds to PSSCR[41]. When set to 1, causes the status field to return all 0's when read by OS.
2	RWX	CME_SCOM_PSCRS10_STATE_LOSS_ENABLE_A_N: Stop state loss enable. Corresponds to PSSCR[42]. When set, allows hardware to lose state, for example, to allocate core resource to the remaining threads.

Bits	SCOM	Field Mnemonic: Description
3	RWX	CME_SCOM_PSCRS10_EXIT_CRITERION_A_N: Stop exit criterion. Corresponds to PSSCR[43]. 0 = Exit power-saving mode on any interrupt without any state loss 1 = Exit power-saving mode only on LPCR PECE conditions and take system reset interrupt with HV = 1; state loss is allowed and implementation-dependent.
4:7	RWX	CME_SCOM_PSCRS10_POWER_SAVING_LIMIT_A_N: Power-saving level limit. Corresponds to PSSCR[44:47]. Causes an OS stop request greater than or equal to this value to take an interrupt to the hypervisor instead.
8	RWX	CME_SCOM_PSCRS10_HYP_VIRT_EXIT_ENABLE: Hypervisor virtualization exit enable. Corresponds to PECE[17], and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
9	RWX	CME_SCOM_PSCRS10_EXT_EBB_EXIT_ENABLE: External event-based branch exit enable. Corresponds to PECE[18], and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
10	RWX	CME_SCOM_PSCRS10_EXT_RESUME_EXIT_ENABLE: External resume exit enable. Corresponds to PECE[19], and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
11	RWX	CME_SCOM_PSCRS10_EXT_EXIT_ENABLE: External OS exit enable. Corresponds to PECE[49], and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
12	RWX	CME_SCOM_PSCRS10_DEC_EXIT_ENABLE: Decrementer exit enable. Corresponds to PECE[50]. Unused by CME since this exit event is handled inside the core directly. Available to CME only for potential workarounds or sampling.
13	RWX	CME_SCOM_PSCRS10_HMI_EXIT_ENABLE: Hypervisor maintenance interrupt exit enable. Corresponds to PECE[51] and enables the malfunction alert interrupt source in WSR[32] to cause an exit from STOP state.
14:15	RWX	CME_SCOM_PSCRS10_LEVEL_TRANSITION_RATE_A_N: Stop level transition rate field. Corresponds to PSSCR[54:55]. The requested rate of progression from initial to maximum power-saving level if stop promote is implemented. The rate of progression increases with the value of the level transition rate field. Actual rates corresponding to each value are defined by firmware and are TBD.
16:19	RWX	CME_SCOM_PSCRS10_MAX_PROMOTE_LEVEL_A_N: Maximum stop request level. Corresponds to PSSCR[56:59]. Allows hardware to auto-promote to deeper levels as the power-saved core ages (without waking up). Setting this field ≤ initial request level disables promotion. Setting this field to zero always disables auto-promotion. See STOP_REQUEST_LEVEL encoding in the following field.
20:23	RWX	CME_SCOM_PSCRS10_STOP_REQUEST_LEVEL_A_N: Stop request level. Corresponds to PSSCR[60:63]. 0x0 = Stop 0 (Quiesce thread only). 0x1 = Stop 1 (legacy nap). 0x2 = Stop 2 (legacy fast sleep). 0x3 = Stop 3 (if supported, legacy fast sleep @V_{min} using iVRMs). 0x4 = Stop 4 (instant-on; legacy deep sleep without HV loss). 0x5 - 0x7 = Reserved. 0x8 = Stop 8 (legacy deep sleep plus shared L2 clock off). 0x9 = Stop 9 (legacy fast winkle, for lab and simulation only). 0xA = Reserved. 0xB = Stop 11 (legacy deep winkle). 0xC - 0xF = Reserved.
24:63	RO	constant = 0b0000000000000000000000000000000000000000

Register Name	Processor Stop Control Core 1 Shadow Thread 1 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_PSCRS11
Address	0000000013012449 (SCOM)
Description	Processor stop control register core 1 shadow thread 1

Bits	SCOM	Field Mnemonic: Description
0	RWX	CME_SCOM_PSCRS11_SPARE0: Implemented but unused.
1	RWX	CME_SCOM_PSCRS11_OS_STATUS_DISABLE_A_N: OS status disable. Corresponds to PSSCR[41]. When set to 1, causes the status field to return all 0's when read by OS.
2	RWX	CME_SCOM_PSCRS11_STATE_LOSS_ENABLE_A_N: Stop state loss enable. Corresponds to PSSCR[42]. When set, allows hardware to lose state, for example, to allocate core resource to the remaining threads.
3	RWX	CME_SCOM_PSCRS11_EXIT_CRITERION_A_N: Stop exit criterion. Corresponds to PSSCR[43]. 0 = Exit power-saving mode on any interrupt without any state loss. 1 = Exit power-saving mode only on LPCR PECE conditions and take system reset interrupt with HV = 1; state loss is allowed and implementation-dependent.
4:7	RWX	CME_SCOM_PSCRS11_POWER_SAVING_LIMIT_A_N: Power-saving level limit. Corresponds to PSSCR[44:47]. Causes an OS stop request greater than or equal to this value to take an interrupt to the hypervisor instead.
8	RWX	CME_SCOM_PSCRS11_HYP_VIRT_EXIT_ENABLE: Hypervisor virtualization exit enable. Corresponds to PECE[17], and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
9	RWX	CME_SCOM_PSCRS11_EXT_EBB_EXIT_ENABLE: External event-based branch exit enable. Corresponds to PECE[18], and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
10	RWX	CME_SCOM_PSCRS11_EXT_RESUME_EXIT_ENABLE: External resume exit enable. Corresponds to PECE[19], and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
11	RWX	CME_SCOM_PSCRS11_EXT_EXIT_ENABLE: External OS exit enable. Corresponds to PECE[49], and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
12	RWX	CME_SCOM_PSCRS11_DEC_EXIT_ENABLE: Decrementer exit enable. Corresponds to PECE[50]. Unused by CME since this exit event is handled inside the core directly. Available to CME only for potential workarounds or sampling.
13	RWX	CME_SCOM_PSCRS11_HMI_EXIT_ENABLE: Hypervisor maintenance interrupt exit enable. Corresponds to PECE[51] and enables the malfunction alert interrupt source in WSR[32] to cause an exit from STOP state.
14:15	RWX	CME_SCOM_PSCRS11_LEVEL_TRANSITION_RATE_A_N: Stop level transition rate field. Corresponds to PSSCR[54:55]. The requested rate of progression from initial to maximum power-saving level if stop promote is implemented. The rate of progression increases with the value of the level transition rate field. Actual rates corresponding to each value are defined by firmware and are TBD.
16:19	RWX	CME_SCOM_PSCRS11_MAX_PROMOTE_LEVEL_A_N: Maximum stop request level. Corresponds to PSSCR[56:59]. Allows hardware to auto-promote to deeper levels as the power-saved core ages (without waking up). Setting this field ≤ initial request level disables promotion. Setting this field to zero always disables auto-promotion. See STOP_REQUEST_LEVEL encoding in the following field.
20:23	RWX	CME_SCOM_PSCRS11_STOP_REQUEST_LEVEL_A_N: Stop request level. Corresponds to PSSCR[60:63]. 0x0 = Stop 0 (Quiesce thread only). 0x1 = Stop 1 (legacy nap). 0x2 = Stop 2 (legacy fast sleep). 0x3 = Stop 3 (if supported, legacy fast sleep @V_{min} using iVRMs). 0x4 = Stop 4 (instant-on; legacy deep sleep without HV loss). 0x5 - 0x7 = Reserved. 0x8 = Stop 8 (legacy deep sleep plus shared L2 clock off). 0x9 = Stop 9 (legacy fast winkle, for lab and simulation only). 0xA = Reserved. 0xB = Stop 11 (legacy deep winkle). 0xC - 0xF = Reserved.

Bits	SCOM	Field Mnemonic: Description
24:63	RO	constant = 0b0000000000000000000000000000000000000000

Register Name	Processor Stop Control Core 1 Shadow Thread 2 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_PSCRS12
Address	000000001301244A (SCOM)
Description	Processor stop control register core 1 shadow thread 2

Bits	SCOM	Field Mnemonic: Description
0	RWX	CME_SCOM_PSCRS12_SPARE0: Implemented but unused.
1	RWX	CME_SCOM_PSCRS12_OS_STATUS_DISABLE_A_N: OS status disable. Corresponds to PSSCR[41]. When set to 1, causes the status field to return all 0's when read by OS.
2	RWX	CME_SCOM_PSCRS12_STATE_LOSS_ENABLE_A_N: Stop state loss enable. Corresponds to PSSCR[42]. When set, allows hardware to lose state, for example, to allocate core resource to the remaining threads.
3	RWX	CME_SCOM_PSCRS12_EXIT_CRITERION_A_N: Stop exit criterion. Corresponds to PSSCR[43]. 0 = Exit power-saving mode on any interrupt without any state loss 1 = Exit power-saving mode only on LPCR PECE conditions and take system reset interrupt with HV = 1; state loss is allowed and implementation-dependent.
4:7	RWX	CME_SCOM_PSCRS12_POWER_SAVING_LIMIT_A_N: Power-saving level limit. Corresponds to PSSCR[44:47]. Causes an OS stop request greater than or equal to this value to take an interrupt to the hypervisor instead.
8	RWX	CME_SCOM_PSCRS12_HYP_VIRT_EXIT_ENABLE: Hypervisor virtualization exit enable. Corresponds to PECE[17], and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
9	RWX	CME_SCOM_PSCRS12_EXT_EBB_EXIT_ENABLE: External event-based branch exit enable. Corresponds to PECE[18], and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
10	RWX	CME_SCOM_PSCRS12_EXT_RESUME_EXIT_ENABLE: External resume exit enable. Corresponds to PECE[19], and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
11	RWX	CME_SCOM_PSCRS12_EXT_EXIT_ENABLE: External OS exit enable. Corresponds to PECE[49], and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
12	RWX	CME_SCOM_PSCRS12_DEC_EXIT_ENABLE: Decrementer exit enable. Corresponds to PECE[50]. Unused by CME since this exit event is handled inside the core directly. Available to CME only for potential workarounds or sampling.
13	RWX	CME_SCOM_PSCRS12_HMI_EXIT_ENABLE: Hypervisor maintenance interrupt exit enable. Corresponds to PECE[51] and enables the malfunction alert interrupt source in WSR[32] to cause an exit from STOP state.
14:15	RWX	CME_SCOM_PSCRS12_LEVEL_TRANSITION_RATE_A_N: Stop level transition rate field. Corresponds to PSSCR[54:55]. The requested rate of progression from initial to maximum power-saving level if stop promote is implemented. The rate of progression increases with the value of the level transition rate field. Actual rates corresponding to each value are defined by firmware and are TBD.
16:19	RWX	CME_SCOM_PSCRS12_MAX_PROMOTE_LEVEL_A_N: Maximum stop request level. Corresponds to PSSCR[56:59]. Allows hardware to auto-promote to deeper levels as the power-saved core ages (without waking up). Setting this field ≤ initial request level disables promotion. Setting this field to zero always disables auto-promotion. See STOP_REQUEST_LEVEL encoding in the following field.

Bits	SCOM	Field Mnemonic: Description
20:23	RWX	CME_SCOM_PSCRS12_STOP_REQUEST_LEVEL_A_N: Stop request level. Corresponds to PSSCR[60:63]. 0x0 = Stop 0 (Quiesce thread only). 0x1 = Stop 1 (legacy nap). 0x2 = Stop 2 (legacy fast sleep). 0x3 = Stop 3 (if supported, legacy fast sleep @V_{min} using iVRMs). 0x4 = Stop 4 (instant-on; legacy deep sleep without HV loss). 0x5 - 0x7 = Reserved. 0x8 = Stop 8 (legacy deep sleep plus shared L2 clock off). 0x9 = Stop 9 (legacy fast winkle, for lab and simulation only). 0xA = Reserved. 0xB = Stop 11 (legacy deep winkle). 0xC - 0xF = Reserved.
24:63	RO	constant = 0b0000000000000000000000000000000000000000

Register Name	Processor Stop Control Core 1 Shadow Thread 3 Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_SCOM_PSCRS13
Address	000000001301244B (SCOM)
Description	Processor stop control register core 1 shadow thread 3

Bits	SCOM	Field Mnemonic: Description
0	RWX	CME_SCOM_PSCRS13_SPARE0: Implemented but unused.
1	RWX	CME_SCOM_PSCRS13_OS_STATUS_DISABLE_A_N: OS status disable. Corresponds to PSSCR[41]. When set to 1, causes the status field to return all 0's when read by OS.
2	RWX	CME_SCOM_PSCRS13_STATE_LOSS_ENABLE_A_N: Stop state loss enable. Corresponds to PSSCR[42]. When set, allows hardware to lose state, for example, to allocate core resource to the remaining threads.
3	RWX	CME_SCOM_PSCRS13_EXIT_CRITERION_A_N: Stop exit criterion. Corresponds to PSSCR[43]. 0 = Exit power-saving mode on any interrupt without any state loss 1 = Exit power-saving mode only on LPCR PECE conditions and take system reset interrupt with HV = 1; state loss is allowed and implementation-dependent.
4:7	RWX	CME_SCOM_PSCRS13_POWER_SAVING_LIMIT_A_N: Power-saving level limit. Corresponds to PSSCR[44:47]. Causes an OS stop request greater than or equal to this value to take an interrupt to the hypervisor instead.
8	RWX	CME_SCOM_PSCRS13_HYP_VIRT_EXIT_ENABLE: Hypervisor virtualization exit enable. Corresponds to PECE[17], and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
9	RWX	CME_SCOM_PSCRS13_EXT_EBB_EXIT_ENABLE: External event-based branch exit enable. Corresponds to PECE[18], and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
10	RWX	CME_SCOM_PSCRS13_EXT_RESUME_EXIT_ENABLE: External resume exit enable. Corresponds to PECE[19], and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
11	RWX	CME_SCOM_PSCRS13_EXT_EXIT_ENABLE: External OS exit enable. Corresponds to PECE[49], and enables the corresponding interrupt source in WSR[0:31] to cause an exit from STOP state.
12	RWX	CME_SCOM_PSCRS13_DEC_EXIT_ENABLE: Decrementer exit enable. Corresponds to PECE[50]. Unused by CME since this exit event is handled inside the core directly. Available to CME only for potential workarounds or sampling.
13	RWX	CME_SCOM_PSCRS13_HMI_EXIT_ENABLE: Hypervisor maintenance interrupt exit enable. Corresponds to PECE[51] and enables the malfunction alert interrupt source in WSR[32] to cause an exit from STOP state.

Bits	SCOM	Field Mnemonic: Description
14:15	RWX	CME_SCOM_PSCRS13_LEVEL_TRANSITION_RATE_A_N: Stop level transition rate field. Corresponds to PSSCR[54:55]. The requested rate of progression from initial to maximum power-saving level if stop promote is implemented. The rate of progression increases with the value of the level transition rate field. Actual rates corresponding to each value are defined by firmware and are TBD.
16:19	RWX	CME_SCOM_PSCRS13_MAX_PROMOTE_LEVEL_A_N: Maximum stop request level. Corresponds to PSSCR[56:59]. Allows hardware to auto-promote to deeper levels as the power-saved core ages (without waking up). Setting this field ≤ initial request level disables promotion. Setting this field to zero always disables auto-promotion. See STOP_REQUEST_LEVEL encoding in the following field.
20:23	RWX	CME_SCOM_PSCRS13_STOP_REQUEST_LEVEL_A_N: Stop request level. Corresponds to PSSCR[60:63]. 0x0 = Stop 0 (Quiesce thread only). 0x1 = Stop 1 (legacy nap). 0x2 = Stop 2 (legacy fast sleep). 0x3 = Stop 3 (if supported, legacy fast sleep @V_{min} using iVRMs). 0x4 = Stop 4 (instant-on; legacy deep sleep without HV loss). 0x5 - 0x7 = Reserved. 0x8 = Stop 8 (legacy deep sleep plus shared L2 clock off). 0x9 = Stop 9 (legacy fast winkle, for lab and simulation only). 0xA = Reserved. 0xB = Stop 11 (legacy deep winkle). 0xC - 0xF = Reserved.
24:63	RO	constant = 0b0000000000000000000000000000000000000000

Register Name	CME_LCL CME Local Stop Interface Status Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_LCL_SISR
Address	000000001301244C (SCOM)
Description	CME_LCL CME local stop interface status register

Bits	SCOM	Field Mnemonic: Description
0	ROX	CME_LCL_SISR_PM_ENTRY_ACK_C0_ACTUAL: Actual value being driven on the CME output to core 0 PC after all overrides have been applied.
1	ROX	CME_LCL_SISR_PM_ENTRY_ACK_C1_ACTUAL: Actual value being driven on the CME output to core 1 PC after all overrides have been applied.
2	ROX	CME_LCL_SISR_PM_BLOCK_INTERRUPTS_C0_ACTUAL: Actual value being driven on the CME output to core 0 PC after all overrides have been applied.
3	ROX	CME_LCL_SISR_PM_BLOCK_INTERRUPTS_C1_ACTUAL: Actual value being driven on the CME output to core 1 PC after all overrides have been applied.
4	ROX	CME_LCL_SISR_PM_EXIT_C0_ACTUAL: Actual value being driven on the CME output to core 0 PC after all overrides have been applied.
5	ROX	CME_LCL_SISR_PM_EXIT_C1_ACTUAL: Actual value being driven on the CME output to core 1 PC after all overrides have been applied.
6:8	ROX	CME_LCL_SISR_RESERVED_6_8: Not implemented.
9	ROX	CME_LCL_SISR_PC_FUSED_CORE_MODE: Input signal indicating that the fused core mode is on. **Note:** This bit is not valid (will be zero) when the L2 domain (which includes PC common core) is fenced.
10	ROX	CME_LCL_SISR_PCBMUX_GRANT_C0: Core 0 PCB multiplexer grant. See SICR for request.
11	ROX	CME_LCL_SISR_PCBMUX_GRANT_C1: Core 1 PCB multiplexer grant. See SICR for request.
12:15	ROX	CME_LCL_SISR_RESERVED_12_15: Not Implemented.

Bits	SCOM	Field Mnemonic: Description
16	ROX	CME_LCL_SISR_SPECIAL_WAKEUP_DONE_C0_ACTUAL: Actual value being driven on the CME output to C0PPM after all overrides have been applied.
17	ROX	CME_LCL_SISR_SPECIAL_WAKEUP_DONE_C1_ACTUAL: Actual value being driven on the CME output to C1PPM after all overrides have been applied.
18:29	ROX	CME_LCL_SISR_RESERVED_18_29: Not implemented.
30:31	ROX	CME_LCL_SISR_L2_INTF_QUIESCE_DONE_LVL_0_1: Indicates the L2 interface is quiesced per core.
32	ROX	CME_LCL_SISR_PC_UNMASKED_ATTN_C0: Core 0 unmasked special attention indication.
33	ROX	CME_LCL_SISR_PC_UNMASKED_ATTN_C1: Core 1 unmasked special attention indication.
34	ROX	CME_LCL_SISR_PM_STATE_ACTIVE_C0: Core 0 PM state active (raw value from PC). **Note:** May also conditionally cause an external interrupt.
35	ROX	CME_LCL_SISR_PM_STATE_ACTIVE_C1: Core 1 PM state active (raw value from PC). **Note:** May also conditionally cause an external interrupt.
36:39	ROX	CME_LCL_SISR_PM_STATE_C0: Core 0 PM state (stop level).
40:43	ROX	CME_LCL_SISR_PM_STATE_C1: Core 1 PM state (stop level).
44	ROX	CME_LCL_SISR_PM_STATE_ALL_HV_C0: Core 0 all threads in HV state.
45	ROX	CME_LCL_SISR_PM_STATE_ALL_HV_C1: Core 1 all threads in HV state.
46	ROX	CME_LCL_SISR_PC_INSTR_RUNNING_C0: Core 0 Instructions running on at least one thread.
47	ROX	CME_LCL_SISR_PC_INSTR_RUNNING_C1: Core 1 instructions running on at least one thread.
48:51	ROX	CME_LCL_SISR_PC_NON_HV_RUNNING_C0: Core 0 per thread 0..3 indication if it is running in non-HV mode (used only for instant-on latency measurement).
52:55	ROX	CME_LCL_SISR_PC_NON_HV_RUNNING_C1: Core 1 per thread 0..3 indication if it is running in non-HV mode.
56	ROX	CME_LCL_SISR_ALLOW_REG_WAKEUP_C0: Core 0 PPM allow regular wake-up (control for OCC power shifting).
57	ROX	CME_LCL_SISR_ALLOW_REG_WAKEUP_C1: Core 1 PPM allow regular wake-up (control for OCC power shifting).
58:63	RO	constant = 0b000000

Register Name	CME_LCL Inter-CME Local Communication Receive Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CME.CME_LCL_ICRR
Address	000000001301244D (SCOM)
Description	CME local communication receive register

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	CME_LCL_ICRR_CME_COMM_RECV: Data received from partner CME.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	HTM Collection Mode Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CHTMLBS0.CHTM.SC.HTM_MODE
Address	0000000013012600 (SCOM)
Description	HTM collection mode register

Bits	SCOM	Field Mnemonic: Description
0	RW	HTMSC_MODE_HTM_ENABLE: HTM enable, set by software to start HTM trace.
1:2	RW	HTMSC_MODE_CONTENT_SEL: HTM MODE: Core instruction trace, LLAT trace, PPE trace, or Direct Memory Write.
3	RW	HTMSC_MODE_SPARE0: Unused bit.
4:9	RW	HTMSC_MODE_CAPTURE: HTM capture mode(0:5) has different meanings according to the Content Select: When htm_mode_q(1 TO 2) == 00, that is, Core Instruction Trace. 00xxxx : tc_pc_trace_active asserted when HTM_STAT[Tracing] = 1 to purge the ERAT when entering and exitting trace. 01xxxx : tc_pc_trace_active asserted when HTM_MODE[HTM_Trace_enable] = 1 to purge the ERAT only at the beginning. When htm_mode_q(1 TO 2) == 01, that is, LLAT Trace. 0xxxxx : capture on assertion of l2_htm_llat_disp_req, that is, any dispatch request. 1xxxxx : capture on assertion of l2_htm_llat_disp_req AND l2_llat_htm_rcdisp_occurred, that is, only on passed dispatch. x0xxxx : capture on assertion of l2_htm_llat_disp_req, that is, loads or stores. x1xxxx : capture on assertion of l2_htm_llat_disp_req AND l2_llat_htm_rcdisp_ld_not_st, that is, only loads. xx0xxx : capture on assertion of l2_llat_htm_pbl3hit_dval. xx1xxx : no capture on assertion of l2_llat_htm_pbl3hit_dval - enable embedded time stamp. When htm_mode_q(1 TO 2) == 11, that is, Direct Memory Write. 1xxxxx : Enable HPMC-IMA Mode.
10	RW	HTMSC_MODE_DD1EQUIV: POWER8 processor with NVLink technology DD1equiv for purge done not asserted bug HW238754.
11:12	RW	HTMSC_MODE_SPARE_1TO2: Spare bits.
13	RW	HTMSC_MODE_WRAP: 0 = Stop trace when reach top of trace memory. 1 = Trace will continue until a stop trigger is received. Wrap to beginning of trace memory when the top has been reached.
14	RW	HTMSC_MODE_DIS_TSTAMP: 0 = Write of time stamps enabled. 1 = Disable writing of time stamps.
15	RW	HTMSC_MODE_SINGLE_TSTAMP: 0 = Additional time stamp written on timer overflow. 1 = Time stamp only before new record (if enabled).
16	RW	HTMSC_MODE_DIS_STALL: 0 = Core execution stalls when buffer full, Core Trace only. 1 = Core instruction trace stall disabled.
17	RW	HTMSC_MODE_MARKERS_ONLY: 0 = Normal trace. 1 = Ave only markers and enabled stamps.
18	RW	HTMSC_MODE_DIS_GROUP: 0 = Send command as programmed. Convert nodal to group scope. 1 = If programmed to group or nodal, send as VGs.
19:23	RW	HTMSC_MODE_SPARES: Spares.
24:39	RW	HTMSC_MODE_VGTARGET: VG target bits used in VGs mode.
40:63	RO	constant = 0b000000000000000000000000

Register Name	HTM Trace Memory Configuration Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CHTMLBS0.CHTM.SC.HTM_MEM
Address	0000000013012601 (SCOM)
Description	HTM trace memory configuration register

Bits	SCOM	Field Mnemonic: Description
0	RW	HTMSC_MEM_ALLOC: 0 = Memory based address not configured. 1 = Memory address configured. This bit must be written to zero before setting because the HTM looks for the 0 => 1 transition to indicate the memory address has been updated.
1:3	RW	HTMSC_MEM_SCOPE: Configure the scope used when writing the HTM trace memory. If the scope is not large enough, the HTM will get an address error. If the scope is too large, HTM will experience excessive delay. Set scope to system if CHTM memory is on foreign link.
4	RW	HTMSC_MEM_PRIORITY: Configure the starting priority used when writing the HTM trace memory.
5	RW	HTMSC_MEM_SIZE_SMALL: 0 = Trace memory size from 512 MB to 256 GB. 1 = Trace memory size from 16 MB to 8 GB.
6:7	RW	HTMSC_MEM_SPARE: Spare bits.
8:39	RW	HTMSC_MEM_BASE: Trace memory base address (8:39). The trace memory base address must be aligned on a trace memory size boundary.
40:48	RW	HTMSC_MEM_SIZE: When htmsc_mem_size_small = 0, these bits define the mask to bits (26:35) of the trace memory base address and define the size of the trace memory between 512 MB and 256 GB. When htmsc_mem_size_small = 1, these bits define the mask to bits (31:39) of the trace memory base address and define the size of the trace memory between 16 MB and 8 GB.
49:56	RO	constant = 0b00000000

Register Name	HTM Trace Status Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CHTMLBS0.CHTM.SC.HTM_STAT
Address	0000000013012602 (SCOM)
Description	HTM trace status register

Bits	SCOM	Field Mnemonic: Description
0	ROX	HTMCO_STATUS_PURGE_IN_PROG: Purge in progress.
1	ROX	HTMCO_STATUS_PURGE_DONE: Purge completed.
2	ROX	HTMCO_STATUS_CRESP_OV: Not set in CHTM.
3	ROX	HTMCO_STATUS_REPAIR: Address repair. Asserted on the occurrence of an address error to indicate the need of software to clear and update HTM_MEM. Will stay high until HTM_MEM is updated.
4	ROX	HTMCO_STATUS_BUF_WAIT: Buffer waiting. Asserted on condition of data buffers full in tracing state. Any markers, stamps, and trace data will be lost.
5	ROX	STATUS_TRIG_DROPPED_Q: Buffer overrun trigger. Asserted on buffer overrun due to trigger lost. Cleared on the writing of 1 to the reset trigger bit, htmsc_trig_reset.
6	ROX	HTMCO_STATUS_ADDR_ERROR: Address error. Asserted on address error when write buffer was allocated. Need to set new address range.
7	ROX	STATUS_REC_DROPPED_Q: Buffer overrun data. Asserted on buffer overrun due to trace data lost. Cleared on the writing of 1 to the reset trigger bit, htmsc_trig_reset.

Bits	SCOM	Field Mnemonic: Description
8	ROX	HTMCO_STATUS_INIT: Asserted when htm_cofsm is in Init state.
9	ROX	HTMCO_STATUS_PREREQ: Asserted when htm_cofsm is in Pre-req state.
10	ROX	HTMCO_STATUS_READY: Asserted when htm_cofsm is in Ready state.
11	ROX	HTMCO_STATUS_TRACING: Asserted when htm_cofsm is in Tracing state.
12	ROX	HTMCO_STATUS_PAUSED: Asserted when htm_cofsm is in Paused state.
13	ROX	HTMCO_STATUS_FLUSH: Asserted when htm_cofsm is in Flush state.
14	ROX	HTMCO_STATUS_COMPLETE: Asserted when htm_cofsm is in Complete state.
15	ROX	HTMCO_STATUS_ENABLE: Asserted when htm_cofsm is in Enable state.
16	ROX	HTMCO_STATUS_STAMP: Asserted when htm_cofsm is in Stamp state.
17	ROX	STATUS_SCOM_ERROR: Asserted to indicate to the HTM that a SCOM error indication was received from the SCOM satellite. Cleared on the writing of 1 to the reset trigger bit, htmsc_trig_reset.
18:19	ROX	STATUS_UNUSED: NHTM only. Unused in CHTM.
20:63	RO	constant = 0b00000000000000000000000000000000000000000000

Register Name	HTM Last Address Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CHTMLBS0.CHTM.SC.HTM_LAST
Address	0000000013012603 (SCOM)
Description	HTM last address register

Bits	SCOM	Field Mnemonic: Description
0:7	RO	constant = 0b00000000
8:56	ROX	HTM_LAST_ADDRESS: The last cache line address of the memory trace. Valid only when HTM is in the Complete state.
57:63	RO	constant = 0b0000000

Register Name	HTM SCOM Trigger Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CHTMLBS0.CHTM.SC.HTM_TRIG
Address	0000000013012604 (SCOM)
Description	HTM SCOM trigger register

Bits	SCOM	Field Mnemonic: Description
0	RW	HTMSC_TRIG_START: Start trigger.
1	RW	HTMSC_TRIG_STOP: Stop trigger.
2	RW	HTMSC_TRIG_PAUSE: Pause trigger.
3	RW	HTMSC_TRIG_STOP_ALT: Stop trigger 2. This is a legacy bit that used to be the freeze trigger in POWER6 implementation.
4	RW	HTMSC_TRIG_RESET: Reset trigger.
5	RW	HTMSC_TRIG_MARK_VALID: Mark type valid.
6:15	RW	HTMSC_TRIG_MARK_TYPE: Mark type is put into the mark record when bit 5 is set.
16:63	RO	constant = 0b000000000000000000000000000000000000000000000000

Register Name	HTM Trigger Control Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CHTMLBS0.CHTM.SC.HTM_CTRL
Address	0000000013012605 (SCOM)
Description	HTM trigger control register

Bits	SCOM	Field Mnemonic: Description
0:1	RW	HTMSC_CTRL_TRIG: Local trigger forwarding. 00 = Local triggers are not forwarded to the processor bus; they are inserted into the trace when tracing. Both local and global triggers control the HTM. 01 = Local triggers are not forwarded to the processor bus; they are inserted into the trace when tracing. Only local triggers control the HTM. 1x = Local triggers are forwarded to the processor bus; they are not inserted into the trace when tracing. Only global triggers control the HTM.
2	RW	HTMSC_CTRL_MTSPR_TRIG: MTSPR Trigger Control. 0 = Ignore MTSPR trace triggers. 1 = Treat MTSPR trace triggers as local triggers.
3	RW	HTMSC_CTRL_MTSPR_MARK: MTSPR marker control. 0 = Ignore MTSPR trace markers. 1 = Treat MTSPR trace markers as local markers.
4:5	RW	HTMSC_CTRL_MARK: MTSPR marker forwarding/insertion. 00 = Local markers are not forwarded to the processor bus. Both local and global markers are inserted into the trace. 01 = Local markers are not forwarded to the processor bus. Only local markers are inserted into the trace. 10 = Local markers are forwarded to the processor bus. Only global markers are inserted into the trace. 11 = Local markers are forwarded to the processor bus. Markers are not inserted into the trace.
6	RW	HTMSC_CTRL_DBG0_STOP: Stop on local DBG trigger0 to PC. 1 = Stop on local trace debug trigger 0. 0 = Ignore debug trigger 0.
7	RW	HTMSC_CTRL_DBG1_STOP: Stop on local DBG trigger1 to PC. 1 = Stop on local trace debug trigger 1. 0 = Ignore debug trigger 1.
8	RW	HTMSC_CTRL_RUN_STOP: Stop on trace run falling. 1 = Stop trace on falling edge of tcdgb_tchtm_trace_run. 0 = Ignore signal tcdgb_tchtm_trace_run.
9	RW	HTMSC_CTRL_CHIP0_STOP: Stop on PC_TC_DBG_Trigger0. 1 = Stop trigger Core Debug Trigger 0. 0 = Ignore Core Debug Trigger 0.
10	RW	HTMSC_CTRL_CHIP1_STOP: Stop on PC_TC_DBG_Trigger1. 1 = Stop trigger on Core Debug trigger 1. 0 = Ignore Core debug Trigger 1.
11:12	RW	HTMSC_CTRL_SPARE1112: Spare bits.
13	RW	HTMSC_CTRL_XSTOP_STOP: Stop on checkstop. 1 = Stop trigger on chiplet checkstop. 0 = Ignore chiplet checkstop.
14:15	RW	HTMSC_CTRL_SPARE1415: Spare bits.
16:63	RO	constant = 0b000000000000000000000000000000000000000000000000

Register Name	HTM IMA Status Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CHTMLBS0.CHTM.SC.HTM_IMA_STATUS
Address	000000001301260A (SCOM)
Description	HTM IMA status

Bits	SCOM	Field Mnemonic: Description
0	ROX	HTMSC_IMA_ERROR: NCU transfer error. Deasserted after performing the CHTM HPMC-IMA reset sequence.
1	ROX	HTMSC_IMA_TRACE_ACTIVE: IMA idle indicator.
2	ROX	HTMSC_PDBAR_ERROR: PDBAR parity error. Deasserted after performing the CHTM HPMC-IMA reset sequence.
3:4	ROX	HTMSC_IMA_RESERVED: Reserved.
5:11	ROX	HTMSC_IMA_FSM: Display the current IMA FSM state. 01 = Disabled. 02 = Idle. 04 = Clear. 08 = Capture. 10 = Write LDBAR. 20 = Write PDBAR. 40 = Error.
12:15	ROX	HTMSC_IMA_COUNT: Number of writes completed to LDBAR or PDBAR address. Counts 0 to 7.
16:55	RO	constant = 0b0000000000000000000000000000000000000000

Register Name	HTM IMA PDBAR Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CHTMLBS0.CHTM.SC.HTM_IMA_PDBAR
Address	000000001301260B (SCOM)
Description	HTM IMA PDBAR

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1	RW	HTMSC_IMA_ENABLE_SPLIT_CORE: This bit controls the indexing of the PDBAR address for the starting address of the write to the PDBAR space. 0 = Big core mode. 1 = Split core mode.
2:4	RW	HTMSC_IMA_PDBAR_SPARE2TO4:
5:7	RW	HTMSC_IMA_PDBAR_SCOPE: Configure the scope used for direct memory writes. The scope is forced to a group minimum unless HTM_MODE(dis_force_group) = 1. Foreign scope is not supported.
8:50	RW	HTMSC_IMA_PDBAR: IMA Write Physical Base Address PDBAR spare bit 2 to 4.
51:63	RO	constant = 0b0000000000000

Register Name	HTM Collection Mode Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CHTMLBS1.CHTM.SC.HTM_MODE
Address	0000000013012700 (SCOM)
Description	HTM collection mode register

Bits	SCOM	Field Mnemonic: Description
0	RW	HTMSC_MODE_HTM_ENABLE: HTM enable, set by software to start HTM trace.
1:2	RW	HTMSC_MODE_CONTENT_SEL: HTM MODE: Core instruction trace, LLAT trace, PPE trace, or direct memory write.
3	RW	HTMSC_MODE_SPARE0: Unused bit.
4:9	RW	HTMSC_MODE_CAPTURE: HTM capture mode(0:5) has different meanings according to the Content Select field: When htm_mode_q(1 TO 2) == 00, that is, Core Instruction Trace: 00xxxx = tc_pc_trace_active asserted when HTM_STAT[Tracing] = 1 to purge the ERAT when entering and exitting trace. 01xxxx : tc_pc_trace_active asserted when HTM_MODE[HTM_Trace_enable] = 1 to purge the ERAT only at the beginning. When htm_mode_q(1 TO 2) == 01, that is, LLAT Trace. 0xxxxx : capture on assertion of l2_htm_llat_disp_req, that is, any dispatch request. 1xxxxx : capture on assertion of l2_htm_llat_disp_req AND l2_llat_htm_rcdisp_occurred, that is, only on passed dispatch. x0xxxx : capture on assertion of l2_htm_llat_disp_req, that is, loads or stores. x1xxxx : capture on assertion of l2_htm_llat_disp_req AND l2_llat_htm_rcdisp_ld_not_st, that is, only loads. xx0xxx : capture on assertion of l2_llat_htm_pbl3hit_dval. xx1xxx : no capture on assertion of l2_llat_htm_pbl3hit_dval - enable embedded time stamp. When htm_mode_q(1 TO 2) == 11, that is, Direct Memory Write. 1xxxxx : Enable HPMC-IMA Mode.
10	RW	HTMSC_MODE_DD1EQUIV: POWER8 processor with NVLink technology DD1equiv for purge done not asserted bug HW238754.
11:12	RW	HTMSC_MODE_SPARE_1TO2: Spare bits.
13	RW	HTMSC_MODE_WRAP: 0 = Stop trace when reach top of trace memory. 1 = Trace will continue until a stop trigger is received. Wrap to beginning of trace memory when the top has been reached.
14	RW	HTMSC_MODE_DIS_TSTAMP: 0 = Write of time stamps enabled. 1 = Disable writing of time stamps.
15	RW	HTMSC_MODE_SINGLE_TSTAMP: 0 = Additional time stamp written on timer overflow. 1 = Time stamp only before new record (if enabled).
16	RW	HTMSC_MODE_DIS_STALL: 0 = Core execution stalls when buffer full, Core Trace only. 1 = Core instruction trace stall disabled.
17	RW	HTMSC_MODE_MARKERS_ONLY: 0 = Normal trace. 1 = Ave only markers and enabled stamps.
18	RW	HTMSC_MODE_DIS_GROUP: 0 = Send the command as programmed. Convert nodal to group scope. 1 = If programmed to group or nodal, send as VGs.
19:23	RW	HTMSC_MODE_SPARES: Spares.
24:39	RW	HTMSC_MODE_VGTARGET: VG target bits used in VGs mode.
40:63	RO	constant = 0b000000000000000000000000

Register Name	HTM Trace Memory Configuration Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CHTMLBS1.CHTM.SC.HTM_MEM
Address	0000000013012701 (SCOM)
Description	HTM trace memory configuration register

Bits	SCOM	Field Mnemonic: Description
0	RW	HTMSC_MEM_ALLOC: This bit must be written to zero before setting since the HTM looks for the 0->1 transition to indicate the memory address has been updated. 0 = Memory based address not configured. 1 = Memory address configured.
1:3	RW	HTMSC_MEM_SCOPE: Configure the scope used when writing the HTM trace memory. If the scope is not large enough, the HTM receives an address error. If the scope is too large, HTM experiences excessive delay. Set the scope to system if CHTM memory is on a foreign link.
4	RW	HTMSC_MEM_PRIORITY: Configure the starting priority used when writing the HTM trace memory.
5	RW	HTMSC_MEM_SIZE_SMALL: 0 = Trace memory size from 512 MB to 256 GB. 1 = Trace memory size from 16 MB to 8 GB.
6:7	RW	HTMSC_MEM_SPARE: Spare bits.
8:39	RW	HTMSC_MEM_BASE: Trace memory base address (8:39). The trace memory base address must be aligned on a trace memory size boundary.
40:48	RW	HTMSC_MEM_SIZE: When htmsc_mem_size_small = 0, these bits define the mask to bits (26:35) of the trace memory base address and define the size of the trace memory between 512 MB and 256 GB. When htmsc_mem_size_small = 1, these bits define the mask to bits (31:39) of the trace memory base address and define the size of the trace memory between 16 MB and 8 GB.
49:56	RO	constant = 0b00000000

Register Name	HTM Trace Status Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CHTMLBS1.CHTM.SC.HTM_STAT
Address	0000000013012702 (SCOM)
Description	HTM trace status register

Bits	SCOM	Field Mnemonic: Description
0	ROX	HTMCO_STATUS_PURGE_IN_PROG: Purge in progress.
1	ROX	HTMCO_STATUS_PURGE_DONE: Purge completed.
2	ROX	HTMCO_STATUS_CRESP_OV: Not set in CHTM.
3	ROX	HTMCO_STATUS_REPAIR: Address repair. Asserted on the occurrence of an address error to indicate the need for software to clear and update HTM_MEM. Remains high until HTM_MEM is updated.
4	ROX	HTMCO_STATUS_BUF_WAIT: Buffer waiting. Asserted when data buffers are full in tracing state. Any markers, stamps, and trace data will be lost.
5	ROX	STATUS_TRIG_DROPPED_Q: Buffer overrun trigger. Asserted on a buffer overrun because of a lost trigger. Cleared on the writing of 1 to the reset trigger bit, htmsc_trig_reset.
6	ROX	HTMCO_STATUS_ADDR_ERROR: Address error. Asserted on address error when the write buffer was allocated. Need to set a new address range.
7	ROX	STATUS_REC_DROPPED_Q: Buffer overrun data. Asserted on buffer overrun due to trace data lost. Cleared on the writing of 1 to the reset trigger bit, htmsc_trig_reset.

Bits	SCOM	Field Mnemonic: Description
8	ROX	HTMCO_STATUS_INIT: Asserted when htm_cofsm is in Init state.
9	ROX	HTMCO_STATUS_PREREQ: Asserted when htm_cofsm is in Pre-req state.
10	ROX	HTMCO_STATUS_READY: Asserted when htm_cofsm is in Ready state.
11	ROX	HTMCO_STATUS_TRACING: Asserted when htm_cofsm is in Tracing state.
12	ROX	HTMCO_STATUS_PAUSED: Asserted when htm_cofsm is in Paused state.
13	ROX	HTMCO_STATUS_FLUSH: Asserted when htm_cofsm is in Flush state.
14	ROX	HTMCO_STATUS_COMPLETE: Asserted when htm_cofsm is in Complete state.
15	ROX	HTMCO_STATUS_ENABLE: Asserted when htm_cofsm is in Enable state.
16	ROX	HTMCO_STATUS_STAMP: Asserted when htm_cofsm is in Stamp state.
17	ROX	STATUS_SCOM_ERROR: Asserted to indicate to the HTM that a SCOM error indication was received from the SCOM satellite. Cleared on the writing of 1 to the reset trigger bit, htmsc_trig_reset.
18:19	ROX	STATUS_UNUSED: NHTM only. Unused in CHTM.
20:63	RO	constant = 0b00000000000000000000000000000000000000000000

Register Name	HTM Last Address Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CHTMLBS1.CHTM.SC.HTM_LAST
Address	0000000013012703 (SCOM)
Description	HTM last address register

Bits	SCOM	Field Mnemonic: Description
0:7	RO	constant = 0b00000000
8:56	ROX	HTM_LAST_ADDRESS: The last cache line address of the memory trace. Valid only when HTM is in the complete state.
57:63	RO	constant = 0b0000000

Register Name	HTM SCOM Trigger Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CHTMLBS1.CHTM.SC.HTM_TRIG
Address	0000000013012704 (SCOM)
Description	HTM SCOM trigger register

Bits	SCOM	Field Mnemonic: Description
0	RW	HTMSC_TRIG_START: Start trigger.
1	RW	HTMSC_TRIG_STOP: Stop trigger.
2	RW	HTMSC_TRIG_PAUSE: Pause trigger.
3	RW	HTMSC_TRIG_STOP_ALT: Stop trigger 2. This is a legacy bit that used to be the freeze trigger in POWER6 implementation.
4	RW	HTMSC_TRIG_RESET: Reset trigger.
5	RW	HTMSC_TRIG_MARK_VALID: Mark type valid.
6:15	RW	HTMSC_TRIG_MARK_TYPE: Mark type is put into the mark record when bit 5 is set.
16:63	RO	constant = 0b000000000000000000000000000000000000000000000000

Register Name	HTM Trigger Control Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CHTMLBS1.CHTM.SC.HTM_CTRL
Address	0000000013012705 (SCOM)
Description	HTM trigger control register

Bits	SCOM	Field Mnemonic: Description
0:1	RW	HTMSC_CTRL_TRIG: Local trigger forwarding. 00 = Local triggers are not forwarded to the processor bus; they are inserted into the trace when tracing. Both local and global triggers control the HTM. 01 = Local triggers are not forwarded to the processor bus; they are inserted into the trace when tracing. Only local triggers control the HTM. 1x = Local triggers are forwarded to the processor bus; they are not inserted into the trace when tracing. Only global triggers control the HTM.
2	RW	HTMSC_CTRL_MTSPR_TRIG: MTSPR trigger control. 0 = Ignore MTSPR trace triggers. 1 = Treat MTSPR trace triggers as local triggers.
3	RW	HTMSC_CTRL_MTSPR_MARK: MTSPR marker control. 0 = Ignore MTSPR trace markers. 1 = Treat MTSPR trace markers as local markers.
4:5	RW	HTMSC_CTRL_MARK: MTSPR marker forwarding and insertion. 00 = Local markers are not forwarded to the processor bus. Both local and global markers are inserted into the trace. 01 = Local markers are not forwarded to the processor bus. Only local markers are inserted into the trace. 10 = Local markers are forwarded to the processor bus. Only global markers are inserted into the trace. 11 = Local markers are forwarded to the processor bus. Markers are not inserted into the trace.
6	RW	HTMSC_CTRL_DBG0_STOP: Stop on local DBG_Trigger0 to PC. 1 = Stop on local trace debug trigger 0. 0 = Ignore debug trigger 0.
7	RW	HTMSC_CTRL_DBG1_STOP: Stop on local DBG_Trigger1 to PC. 1 = Stop on local trace debug trigger 1. 0 = Ignore debug trigger 1.
8	RW	HTMSC_CTRL_RUN_STOP: Stop on trace run falling. 1 = Stop trace on falling edge of tcdgb_tchtm_trace_run. 0 = Ignore signal tcdgb_tchtm_trace_run.
9	RW	HTMSC_CTRL_CHIP0_STOP: Stop on PC_TC_DBG_Trigger0. 1 = Stop trigger core debug trigger 0. 0 = Ignore core debug trigger 0.
10	RW	HTMSC_CTRL_CHIP1_STOP: Stop on PC_TC_DBG_Trigger1. 1 = Stop trigger on core debug trigger 1. 0 = Ignore core debug trigger 1.
11:12	RW	HTMSC_CTRL_SPARE1112: Spare bits.
13	RW	HTMSC_CTRL_XSTOP_STOP: Stop on checkstop. 1 = Stop trigger on chiplet checkstop. 0 = Ignore chiplet checkstop.
14:15	RW	HTMSC_CTRL_SPARE1415: Spare bits.
16:63	RO	constant = 0b000000000000000000000000000000000000000000000000

Register Name	HTM IMA Status Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CHTMLBS1.CHTM.SC.HTM_IMA_STATUS
Address	000000001301270A (SCOM)
Description	HTM IMA status

Bits	SCOM	Field Mnemonic: Description
0	ROX	HTMSC_IMA_ERROR: IMA ERROR : NCU transfer error. Deasserted after performing the CHTM HPMC-IMA reset sequence.
1	ROX	HTMSC_IMA_TRACE_ACTIVE: IMA trace active. IMA idle indicator.
2	ROX	HTMSC_PDBAR_ERROR: PDBAR parity error. Deasserted after performing the CHTM HPMC-IMA reset sequence.
3:4	ROX	HTMSC_IMA_RESERVED: Reserved.
5:11	ROX	HTMSC_IMA_FSM: Display the current IMA FSM state. 01 = Disabled. 02 = Idle. 04 = Clear. 08 = Capture. 10 = Write LDBAR. 20 = Write PDBAR. 40 = Error.
12:15	ROX	HTMSC_IMA_COUNT: Number of writes completed to LDBAR or PDBAR address. Counts 0 to 7.
16:55	RO	constant = 0b0000000000000000000000000000000000000000

Register Name	HTM IMA PDBAR Register
Mnemonic	TP.TCEP03.TPCL3.PPE.CME1.CHTMLBS1.CHTM.SC.HTM_IMA_PDBAR
Address	000000001301270B (SCOM)
Description	HTM IMA PDBAR

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1	RW	HTMSC_IMA_ENABLE_SPLIT_CORE: This bit controls the indexing of the PDBAR address for the starting address of the write to the PDBAR space. 0 = Big core mode. 1 = Split core mode.
2:4	RW	HTMSC_IMA_PDBAR_SPARE2TO4:
5:7	RW	HTMSC_IMA_PDBAR_SCOPE: Configure the scope used for direct memory write. The scope is forced to a group minimum unless HTM_MODE(dis_force_group) = 1. Foreign scope is not supported.
8:50	RW	HTMSC_IMA_PDBAR: IMA write physical base address PDBAR spare bit 2 to 4.
51:63	RO	constant = 0b0000000000000

14. CORE Chiplet

The POWER9 processor registers are listed alphabetically by mnemonic in the following address table.

Mnemonic	Address	Page
EX07.EC.C0.IFU.IFRE.IFCER0.ERR_INJ_REG	0x000000002E010C04	2296
EX07.EC.C0.IFU.IFRE.IFCER0.IFU_HOLD_OUT_0	0x000000002E010C00	2294
EX07.EC.C0.IFU.IFRE.IFCER0.IFU_HOLD_OUT_1	0x000000002E010C01	2294
EX07.EC.C0.IFU.IFRE.IFCER0.IFU_HOLD_OUT_2	0x000000002E010C02	2295
EX07.EC.C0.IFU.IFRE.IFCER0.IFU_HOLD_OUT_3	0x000000002E010C03	2295
EX07.EC.C0.LS.ERR_INJ_REG	0x000000002E010CBF	2303
EX07.EC.C0.LS.LSU_HOLD_OUT_REG0	0x000000002E010C80	2301
EX07.EC.C0.LS.LSU_HOLD_OUT_REG1	0x000000002E010C81	2301
EX07.EC.C0.LS.LSU_HOLD_OUT_REG2	0x000000002E010C82	2302
EX07.EC.C0.LS.LSU_HOLD_OUT_REG3	0x000000002E010C83	2303
EX07.EC.C0.PC.FIR.CORE_ACTION0	0x000000002E010A46	2264
EX07.EC.C0.PC.FIR.CORE_ACTION1	0x000000002E010A47	2266
EX07.EC.C0.PC.FIR.CORE_FIR	0x000000002E010A40	2260
EX07.EC.C0.PC.FIR.CORE_FIRMASK	0x000000002E010A43	2262
EX07.EC.C0.PC.FIR.CORE_WOF	0x000000002E010A48	2268
EX07.EC.C0.PC.FIR.FIR_ERR_INJ	0x000000002E010A4D	2270
EX07.EC.C0.PC.FIR.FIR_HOLD_OUT	0x000000002E010A51	2272
EX07.EC.C0.PC.FIR.RAM_CTRL	0x000000002E010A4F	2271
EX07.EC.C0.PC.FIR.RAM_MODEREG	0x000000002E010A4E	2271
EX07.EC.C0.PC.FIR.RAM_STATUS	0x000000002E010A50	2272
EX07.EC.C0.PC.FIR.RECOV_FWD_PROG_CTRL	0x000000002E010A4B	2270
EX07.EC.C0.PC.FIR.RECOV_THOLD	0x000000002E010A4C	2270
EX07.EC.C0.PC.FIR.RESET_KEEPER	0x000000002E010A4A	2269
EX07.EC.C0.PC.IMA.IMA_EVENT_MASK	0x000000002E010AA8	2288
EX07.EC.C0.PC.IMA.IMA_TRACE	0x000000002E010AA9	2289
EX07.EC.C0.PC.PMU.PMUC.SIER_MASK	0x000000002E010AAE	2291
EX07.EC.C0.PC.PMU.PMUC.SRC_MASK	0x000000002E010AAF	2291
EX07.EC.C0.PC.PMU.SPR_CORE.CORE_FUSES	0x000000002E010AA7	2288
EX07.EC.C0.PC.PMU.SPR_CORE.HV_STATE	0x000000002E010AA6	2287
EX07.EC.C0.PC.PMU.SPR_CORE.INV_ERATE	0x000000002E010AB4	2292
EX07.EC.C0.PC.PMU.SPR_CORE.PMU_HOLD_OUT	0x000000002E010AB6	2293
EX07.EC.C0.PC.PMU.SPR_CORE.PMU_SCOMC	0x000000002E010AB0	2291
EX07.EC.C0.PC.PMU.SPR_CORE.PMU_SCOMC_EN	0x000000002E010AB2	2292
EX07.EC.C0.PC.PMU.SPR_CORE.RAS_MODEREG	0x000000002E010A9D	2282
EX07.EC.C0.PC.PMU.SPR_CORE.SHID0	0x000000002E010AA5	2287
EX07.EC.C0.PC.PMU.SPR_CORE.SPR_CORE_HOLD_OUT	0x000000002E010AB5	2293
EX07.EC.C0.PC.T0_PMU_SCOM	0x000000002E010AAA	2289
EX07.EC.C0.PC.T1_PMU_SCOM	0x000000002E010AAB	2290
EX07.EC.C0.PC.T2_PMU_SCOM	0x000000002E010AAC	2290
EX07.EC.C0.PC.T3_PMU_SCOM	0x000000002E010AAD	2290
EX07.EC.C0.PC.THRCTL.TCTLCOM.HANG_CONTROL	0x000000002E010A00	2258
EX07.EC.C0.PC.THRCTL.TCTLCOM.HID	0x000000002E010A01	2258

Mnemonic	Address	Page
EX07.EC.C0.PC.THRCTL.TCTLCOM.RAS_STATUS	0x000000002E010A02	2259
EX07.EC.C0.PC.THRCTL.TCTLCOM.THRCTL_HOLD_OUT	0x000000002E010A03	2260
EX07.EC.C0.PC.TRACE1.TR.TR0.TRACE_HI_DATA_REG	0x000000002E011440	2304
EX07.EC.C0.PC.TRACE1.TR.TR0.TRACE_LO_DATA_REG	0x000000002E011441	2304
EX07.EC.C0.PC.TRACE1.TR.TR0.TRACE_TRCTRL_CONFIG	0x000000002E011442	2304
EX07.EC.C0.PC.TRACE1.TR.TR0.TRACE_TRDATA_CONFIG_0	0x000000002E011443	2305
EX07.EC.C0.PC.TRACE1.TR.TR0.TRACE_TRDATA_CONFIG_1	0x000000002E011444	2305
EX07.EC.C0.PC.TRACE1.TR.TR0.TRACE_TRDATA_CONFIG_2	0x000000002E011445	2305
EX07.EC.C0.PC.TRACE1.TR.TR0.TRACE_TRDATA_CONFIG_3	0x000000002E011446	2305
EX07.EC.C0.PC.TRACE1.TR.TR0.TRACE_TRDATA_CONFIG_4	0x000000002E011447	2306
EX07.EC.C0.PC.TRACE1.TR.TR0.TRACE_TRDATA_CONFIG_5	0x000000002E011448	2306
EX07.EC.C0.PC.TRACE1.TR.TR0.TRACE_TRDATA_CONFIG_9	0x000000002E011449	2306
EX07.EC.C0.PC.TRACE2.TR.TR0.TRACE_HI_DATA_REG	0x000000002E011480	2307
EX07.EC.C0.PC.TRACE2.TR.TR0.TRACE_LO_DATA_REG	0x000000002E011481	2308
EX07.EC.C0.PC.TRACE2.TR.TR0.TRACE_TRCTRL_CONFIG	0x000000002E011482	2308
EX07.EC.C0.PC.TRACE2.TR.TR0.TRACE_TRDATA_CONFIG_0	0x000000002E011483	2308
EX07.EC.C0.PC.TRACE2.TR.TR0.TRACE_TRDATA_CONFIG_1	0x000000002E011484	2309
EX07.EC.C0.PC.TRACE2.TR.TR0.TRACE_TRDATA_CONFIG_2	0x000000002E011485	2309
EX07.EC.C0.PC.TRACE2.TR.TR0.TRACE_TRDATA_CONFIG_3	0x000000002E011486	2309
EX07.EC.C0.PC.TRACE2.TR.TR0.TRACE_TRDATA_CONFIG_4	0x000000002E011487	2309
EX07.EC.C0.PC.TRACE2.TR.TR0.TRACE_TRDATA_CONFIG_5	0x000000002E011488	2309
EX07.EC.C0.PC.TRACE2.TR.TR0.TRACE_TRDATA_CONFIG_9	0x000000002E011489	2310
EX07.EC.C0.SD.ISU_DEBUG_CTRL	0x000000002E010C46	2301
EX07.EC.C0.SD.ISU_REG0_HOLD_OUT	0x000000002E010C40	2297
EX07.EC.C0.SD.ISU_REG1_HOLD_OUT	0x000000002E010C41	2298
EX07.EC.C0.SD.ISU_REG2_HOLD_OUT	0x000000002E010C42	2298
EX07.EC.C0.SD.ISU_REG3_HOLD_OUT	0x000000002E010C43	2299
EX07.EC.C0.SD.ISU_REG4_HOLD_OUT	0x000000002E010C44	2300
EX07.EC.C0.SD.ISU_REG5_HOLD_OUT	0x000000002E010C45	2300
EX07.EC.C0.SD.TRA_01.TR.TR0.TRACE_HI_DATA_REG	0x000000002E011C00	2311
EX07.EC.C0.SD.TRA_01.TR.TR0.TRACE_LO_DATA_REG	0x000000002E011C01	2311
EX07.EC.C0.SD.TRA_01.TR.TR0.TRACE_TRCTRL_CONFIG	0x000000002E011C02	2311
EX07.EC.C0.SD.TRA_01.TR.TR0.TRACE_TRDATA_CONFIG_0	0x000000002E011C03	2312
EX07.EC.C0.SD.TRA_01.TR.TR0.TRACE_TRDATA_CONFIG_1	0x000000002E011C04	2312
EX07.EC.C0.SD.TRA_01.TR.TR0.TRACE_TRDATA_CONFIG_2	0x000000002E011C05	2312
EX07.EC.C0.SD.TRA_01.TR.TR0.TRACE_TRDATA_CONFIG_3	0x000000002E011C06	2312
EX07.EC.C0.SD.TRA_01.TR.TR0.TRACE_TRDATA_CONFIG_4	0x000000002E011C07	2313
EX07.EC.C0.SD.TRA_01.TR.TR0.TRACE_TRDATA_CONFIG_5	0x000000002E011C08	2313
EX07.EC.C0.SD.TRA_01.TR.TR0.TRACE_TRDATA_CONFIG_9	0x000000002E011C09	2313
EX07.EC.CC.PCC0.COMMON.POW.THROTTLE_CONTROL	0x000000002E010A9E	2283
EX07.EC.CC.PCC0.COMMON.SPR_COMMON.CTRL	0x000000002E010A85	2274
EX07.EC.CC.PCC0.COMMON.SPR_COMMON.HMEER	0x000000002E010A96	2279
EX07.EC.CC.PCC0.COMMON.SPR_COMMON.OCC_SCOMC	0x000000002E010A82	2273
EX07.EC.CC.PCC0.COMMON.SPR_COMMON.SCOMC	0x000000002E010A80	2272
EX07.EC.CC.PCC0.COMMON.SPR_COMMON.SCR0	0x000000002E010A86	2274
EX07.EC.CC.PCC0.COMMON.SPR_COMMON.SCR1	0x000000002E010A87	2274
EX07.EC.CC.PCC0.COMMON.SPR_COMMON.SCR2	0x000000002E010A88	2274
EX07.EC.CC.PCC0.COMMON.SPR_COMMON.SCR3	0x000000002E010A89	2275

Mnemonic	Address	Page
EX07.EC.CC.PCC0.COMMON.SPR_COMMON.SPATTN	0x000000002E010A97	2279
EX07.EC.CC.PCC0.COMMON.SPR_COMMON.SPATTN_MASK	0x000000002E010A9A	2280
EX07.EC.CC.PCC0.COMMON.SPR_COMMON.SPR_COMMON_HOLD_OUT	0x000000002E010AB8	2293
EX07.EC.CC.PCC0.COMMON.SPR_COMMON.SPR_MODE	0x000000002E010A84	2273
EX07.EC.CC.PCC0.COMMON.SPR_COMMON.TFAC_HOLD_OUT	0x000000002E010AB7	2293
EX07.EC.CC.PCC0.COMMON.SPR_COMMON.V0_HMER	0x000000002E010A8E	2275
EX07.EC.CC.PCC0.COMMON.SPR_COMMON.V1_HMER	0x000000002E010A8F	2276
EX07.EC.CC.PCC0.COMMON.SPR_COMMON.V2_HMER	0x000000002E010A90	2277
EX07.EC.CC.PCC0.COMMON.SPR_COMMON.V3_HMER	0x000000002E010A91	2278
EX07.EC.CC.PCC0.COMMON.TFC.TOD_STEP_CHECK	0x000000002E010AA4	2287
EX07.EC.CC.PCC0.PMC.CORE_THREAD_STATE	0x000000002E010AB3	2292
EX07.EC.CC.PCC0.PMC.DIRECT_CONTROLS	0x000000002E010A9C	2281
EX07.EC.CC.PCC0.PMC.THREAD_INFO	0x000000002E010A9B	2281
EX07.EC.CC.PCC0.TFDP.TFP.PWM_EVENTS	0x000000002E010AA2	2284
EX07.EC.CC.PCC0.TFDP.TFP.SPURR_FREQ_DETECT_CYC_CNT	0x000000002E010A9F	2283
EX07.EC.CC.PCC0.TFDP.TFP.SPURR_FREQ_REF	0x000000002E010AA1	2284
EX07.EC.CC.PCC0.TFDP.TFP.SPURR_FREQ_SCALE	0x000000002E010AA0	2283
EX07.EC.CC.PCC0.TOD_READ	0x000000002E010AA3	2284
EX07.EC.CC.PCC0.TOD_SYNC000	0x000000002E010AA3	2285
EX07.EC.CC.PCC0.TOD_SYNC001	0x000000002E010AA3	2285
EX07.EC.CC.PCC0.TOD_SYNC010	0x000000002E010AA3	2285
EX07.EC.CC.PCC0.TOD_SYNC011	0x000000002E010AA3	2286
EX07.EC.CC.PCC0.TOD_SYNC100	0x000000002E010AA3	2286
EX07.EC.CC.PCC0.TOD_SYNC101	0x000000002E010AA3	2286
EX07.EC.CC.PCC0.TOD_SYNC110	0x000000002E010AA3	2286
EX07.EC.CC.PCC0.TOD_SYNC111	0x000000002E010AA3	2287
TP.TCEC14.CORE.BIST	0x000000002E03000B	2324
TP.TCEC14.CORE.CC_ATOMIC_LOCK_REG	0x000000002E0303FF	2332
TP.TCEC14.CORE.CC_PROTECT_MODE_REG	0x000000002E0303FE	2332
TP.TCEC14.CORE.CLK_REGION	0x000000002E030006	2320
TP.TCEC14.CORE.CLOCK_STAT_ARY	0x000000002E03000A	2322
TP.TCEC14.CORE.CLOCK_STAT_NSL	0x000000002E030009	2322
TP.TCEC14.CORE.CLOCK_STAT_SL	0x000000002E030008	2321
TP.TCEC14.CORE.CPLT_CONF0	0x000000002E000008	2238
TP.TCEC14.CORE.CPLT_CONF1	0x000000002E000009	2239
TP.TCEC14.CORE.CPLT_CTRL0	0x000000002E000000	2235
TP.TCEC14.CORE.CPLT_CTRL1	0x000000002E000001	2237
TP.TCEC14.CORE.CPLT_MASK0	0x000000002E000101	2241
TP.TCEC14.CORE.CPLT_STAT0	0x000000002E000100	2240
TP.TCEC14.CORE.CTRL_ATOMIC_LOCK_REG	0x000000002E0003FF	2241
TP.TCEC14.CORE.CTRL_PROTECT_MODE_REG	0x000000002E0003FE	2241
TP.TCEC14.CORE.DBG_CBS_CC	0x000000002E030013	2331
TP.TCEC14.CORE.EPS.DBG.DBG_INST1_COND_REG_1	0x000000002E0107C1	2246
TP.TCEC14.CORE.EPS.DBG.DBG_INST1_COND_REG_2	0x000000002E0107C2	2248
TP.TCEC14.CORE.EPS.DBG.DBG_INST1_COND_REG_3	0x000000002E0107C3	2249
TP.TCEC14.CORE.EPS.DBG.DBG_INST2_COND_REG_1	0x000000002E0107C4	2250
TP.TCEC14.CORE.EPS.DBG.DBG_INST2_COND_REG_2	0x000000002E0107C5	2252
TP.TCEC14.CORE.EPS.DBG.DBG_INST2_COND_REG_3	0x000000002E0107C6	2253

Mnemonic	Address	Page
TP.TCEC14.CORE.EPS.DBG.DBG_MODE_REG	0x000000002E0107C0	2245
TP.TCEC14.CORE.EPS.DBG.DBG_TRACE_MODE_REG_2	0x000000002E0107CF	2257
TP.TCEC14.CORE.EPS.DBG.DBG_TRACE_REG_0	0x000000002E0107CD	2254
TP.TCEC14.CORE.EPS.DBG.DBG_TRACE_REG_1	0x000000002E0107CE	2255
TP.TCEC14.CORE.EPS.DBG.DEBUG_TRACE_CONTROL	0x000000002E0107D0	2257
TP.TCEC14.CORE.EPS.DBG.XTRA_TRACE_MODE	0x000000002E0107D1	2258
TP.TCEC14.CORE.EPS.FIR.GXSTOP0_MASK_REG	0x000000002E040014	2338
TP.TCEC14.CORE.EPS.FIR.GXSTOP1_MASK_REG	0x000000002E040015	2339
TP.TCEC14.CORE.EPS.FIR.GXSTOP2_MASK_REG	0x000000002E040016	2339
TP.TCEC14.CORE.EPS.FIR.GXSTOP_TRIG_REG	0x000000002E040013	2338
TP.TCEC14.CORE.EPS.FIR.LOCAL_FIR_ACTION0	0x000000002E040010	2337
TP.TCEC14.CORE.EPS.FIR.LOCAL_FIR_ACTION1	0x000000002E040011	2337
TP.TCEC14.CORE.EPS.FIR.LOCAL_FIR_MASK	0x000000002E04000D	2337
TP.TCEC14.CORE.EPS.FIR.MODE_REG	0x000000002E040008	2334
TP.TCEC14.CORE.EPS.FIR.SUM_MASK_REG	0x000000002E040017	2340
TP.TCEC14.CORE.EPS.PSC.PSC.ADDR_TRAP_REG	0x000000002E010003	2244
TP.TCEC14.CORE.EPS.PSC.PSC.ATOMIC_LOCK_MASK_LATCH_REG	0x000000002E010007	2245
TP.TCEC14.CORE.EPS.PSC.PSC.PSCOM_ERROR_MASK	0x000000002E010002	2243
TP.TCEC14.CORE.EPS.PSC.PSC.PSCOM_MODE_REG	0x000000002E010000	2242
TP.TCEC14.CORE.EPS.PSC.PSC.PSCOM_STATUS_ERROR_REG	0x000000002E010001	2242
TP.TCEC14.CORE.EPS.PSC.PSC.RING_FENCE_MASK_LATCH_REG	0x000000002E010008	2245
TP.TCEC14.CORE.EPS.PSC.PSC.WRITE_PROTECT_ENABLE_REG	0x000000002E010005	2245
TP.TCEC14.CORE.EPS.PSC.PSC.WRITE_PROTECT_RINGS_REG	0x000000002E010006	2245
TP.TCEC14.CORE.EPS.THERM.CONTROL_REG	0x000000002E050012	2344
TP.TCEC14.CORE.EPS.THERM.DTS_RESULT0	0x000000002E050000	2341
TP.TCEC14.CORE.EPS.THERM.DTS_TRC_RESULT	0x000000002E050003	2341
TP.TCEC14.CORE.EPS.THERM.ERR_STATUS_REG	0x000000002E050013	2344
TP.TCEC14.CORE.EPS.THERM.INJECT_REG	0x000000002E050011	2343
TP.TCEC14.CORE.EPS.THERM.SKITTER_CLKSRC_REG	0x000000002E050016	2346
TP.TCEC14.CORE.EPS.THERM.SKITTER_DATA0	0x000000002E050019	2346
TP.TCEC14.CORE.EPS.THERM.SKITTER_DATA1	0x000000002E05001A	2346
TP.TCEC14.CORE.EPS.THERM.SKITTER_DATA2	0x000000002E05001B	2347
TP.TCEC14.CORE.EPS.THERM.SKITTER_FORCE_REG	0x000000002E050014	2346
TP.TCEC14.CORE.EPS.THERM.SKITTER_MODE_REG	0x000000002E050010	2343
TP.TCEC14.CORE.EPS.THERM.THERM_MODE_REG	0x000000002E05000F	2342
TP.TCEC14.CORE.EPS.THERM.TIMESTAMP_COUNTER_READ	0x000000002E05001C	2347
TP.TCEC14.CORE.ERROR_STATUS	0x000000002E03000F	2328
TP.TCEC14.CORE.FIR_MASK	0x000000002E040002	2333
TP.TCEC14.CORE.HOSTATTN	0x000000002E040009	2335
TP.TCEC14.CORE.HOSTATTN_MASK	0x000000002E04001A	2341
TP.TCEC14.CORE.LOCAL_FIR	0x000000002E04000A	2336
TP.TCEC14.CORE.LOCAL_XSTOP_ERR	0x000000002E040018	2340
TP.TCEC14.CORE.LOCAL_XSTOP_MASK	0x000000002E040019	2341
TP.TCEC14.CORE.OPCG_ALIGN	0x000000002E030001	2316
TP.TCEC14.CORE.OPCG_CAPT1	0x000000002E030010	2329
TP.TCEC14.CORE.OPCG_CAPT2	0x000000002E030011	2330
TP.TCEC14.CORE.OPCG_CAPT3	0x000000002E030012	2331
TP.TCEC14.CORE.OPCG_REG0	0x000000002E030002	2317

Mnemonic	Address	Page
TP.TCEC14.CORE.OPCG_REG1	0x000000002E030003	2318
TP.TCEC14.CORE.OPCG_REG2	0x000000002E030004	2319
TP.TCEC14.CORE.RFIR	0x000000002E040001	2333
TP.TCEC14.CORE.SCAN_REGION_TYPE	0x000000002E030005	2319
TP.TCEC14.CORE.SPATTN	0x000000002E040004	2334
TP.TCEC14.CORE.SPA_MASK	0x000000002E040007	2334
TP.TCEC14.CORE.SYNC_CONFIG	0x000000002E030000	2314
TP.TCEC14.CORE.XFIR	0x000000002E040000	2333
TP.TCEC14.CORE.XSTOP1	0x000000002E03000C	2325
TP.TCEC14.CORE.XSTOP2	0x000000002E03000D	2326
TP.TCEC14.CORE.XSTOP3	0x000000002E03000E	2327

The POWER9 processor registers are listed in the following tables.

Register Name	Chiplet Control Register 0
Mnemonic	TP.TCEC14.CORE.CPLT_CTRL0
Address	000000002E000000 (SCOM) 000000002E000010 (SCOM1) 000000002E000020 (SCOM2)
Description	This register contains the first set of vital chiplet controls.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_OR	WO_CLEAR	CTRL_CC_ABSTCLK_MUXSEL_DC: Select the ABIST clock source for arrays on a chiplet boundary. When set to 1, clocks are used from a chiplet with ABIST.
1	RW	WO_OR	WO_CLEAR	TC_UNIT_SYNCCLK_MUXSEL_DC: Select the synchronous clock for asynchronous latches. (The initial value is 1.)
2	RW	WO_OR	WO_CLEAR	CTRL_CC_FLUSHMODE_INH_DC: Prevent pipeline latches from going into flush mode. (The initial value is 1.)
3	RW	WO_OR	WO_CLEAR	CTRL_CC_FORCE_ALIGN_DC: Force an alignment signal to be sent. (The initial value is 1. Drop before dropping flushmode_inh.)
4	RW	WO_OR	WO_CLEAR	TC_UNIT_ARY_WRT_THRU_DC: Set the array into write-through mode. Used for LBIST.
5	RW	WO_OR	WO_CLEAR	TC_UNIT_AVP_MODE: AVP mode. Switches from refresh pulse to phase counter.
6	RW	WO_OR	WO_CLEAR	FREE_USAGE_6A: Free usage.
7	RW	WO_OR	WO_CLEAR	FREE_USAGE_7A: Free usage.
8	RW	WO_OR	WO_CLEAR	CTRL_CC_ABIST_RECOV_DISABLE_DC: New signal to disable recovery.
9	RW	WO_OR	WO_CLEAR	FREE_USAGE_9A: Free usage.
10	RW	WO_OR	WO_CLEAR	TC_UNIT_IOBIST_TX_WRAP_ENABLE_DC:
11	RW	WO_OR	WO_CLEAR	RESERVED_11A: Reserved.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
12	RW	WO_OR	WO_CLEAR	TC_SKIT_MODE_BIST_DC:
13	RW	WO_OR	WO_CLEAR	TC_UNIT_DETERMINISTIC_TEST_ENABLE_DC: Forces login into deterministic test mode. For example, for LBIST.
14	RW	WO_OR	WO_CLEAR	TC_UNIT_CONSTRAIN_SAFESCAN_DC: Safe scan of N1L latches. Prevent lock when switching SE.
15	RW	WO_OR	WO_CLEAR	TC_UNIT_RRFA_TEST_ENABLE_DC:
16	RW	WO_OR	WO_CLEAR	TC_NBTI_HDR_ENABLE_OVR_DC: NBTI.
17	RW	WO_OR	WO_CLEAR	TC_NBTI_PROBE_GATE_DC: NBTI.
18	RW	WO_OR	WO_CLEAR	RESERVED_18A: Reserved.
19	RW	WO_OR	WO_CLEAR	RESERVED_19A: Reserved.
20:27	RW	WO_OR	WO_CLEAR	TC_PSRO_SEL_DC: PSRO select.
28	RW	WO_OR	WO_CLEAR	TC_BSC_WRAPSEL_DC: Wrap select for BSC.
29	RW	WO_OR	WO_CLEAR	TC_BSC_INTMODE_DC: INT mode for BSC.
30	RW	WO_OR	WO_CLEAR	TC_BSC_INV_DC: INV for BSC mode.
31	RW	WO_OR	WO_CLEAR	TC_BSC_EXTMODE_DC: EXT mode for BSC.
32	RW	WO_OR	WO_CLEAR	TC_REFCLK_DRVR_EN_DC: Reference clock driver enable.
33	RW	WO_OR	WO_CLEAR	RESERVED_33A: Reserved.
34	RW	WO_OR	WO_CLEAR	RESERVED_34A: Reserved.
35	RW	WO_OR	WO_CLEAR	RESERVED_35A: Reserved.
36	RW	WO_OR	WO_CLEAR	TC_OELCC_EDGE_DELAYED_DC: Allows to delay the alignment by one fast cycle. Only used in dual mesh chiplets.
37	RW	WO_OR	WO_CLEAR	TC_OELCC_ALIGN_FLUSH_DC: Forces the alignment and odd/even toggling latch into a flush state. For DFT only.
38	RW	WO_OR	WO_CLEAR	RESERVED_38A: Reserved.
39	RW	WO_OR	WO_CLEAR	RESERVED_39A: Reserved.
40:41	RW	WO_OR	WO_CLEAR	CTRL_MISC_CLKDIV_SEL_DC: Clock divider select. 00 = 1024:1 01 = 64:1 10 = 16:1 11 = 4:1
42	RW	WO_OR	WO_CLEAR	RESERVED_42A: Reserved.
43	RW	WO_OR	WO_CLEAR	RESERVED_43A: Reserved.
44	RW	WO_OR	WO_CLEAR	CTRL_CC_DCTEST_DC: TE = 1 only. Enable DCTEST.
45	RW	WO_OR	WO_CLEAR	CTRL_CC_OTP_PRGMODE_DC: TE = 1 only. OTP ROM program mode.
46	RW	WO_OR	WO_CLEAR	CTRL_CC_SSS_CALIBRATE_DC: TE = 1 only. Sensors calibration.
47	RW	WO_OR	WO_CLEAR	CTRL_CC_PIN_LBIST_DC: TE = 1 only. PIN LBIST mode. The LBIST is controlled by the pin, not by the OPCG.
48	RW	WO_OR	WO_CLEAR	FREE_USAGE_48A: Free usage.
49	RW	WO_OR	WO_CLEAR	FREE_USAGE_49A: Free usage.
50	RW	WO_OR	WO_CLEAR	FREE_USAGE_50A: Free usage.
51	RW	WO_OR	WO_CLEAR	FREE_USAGE_51A: Free usage.
52	RW	WO_OR	WO_CLEAR	FREE_USAGE_52A: Free usage.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
53	RW	WO_OR	WO_CLEAR	FREE_USAGE_53A: Free usage.
54	RW	WO_OR	WO_CLEAR	FREE_USAGE_54A: Free usage.
55	RW	WO_OR	WO_CLEAR	FREE_USAGE_55A: Free usage.
56	RW	WO_OR	WO_CLEAR	FREE_USAGE_56A: Free usage.
57	RW	WO_OR	WO_CLEAR	FREE_USAGE_57A: Free usage.
58	RW	WO_OR	WO_CLEAR	FREE_USAGE_58A: Free usage.
59	RW	WO_OR	WO_CLEAR	FREE_USAGE_59A: Free usage.
60	RW	WO_OR	WO_CLEAR	FREE_USAGE_60A: Free usage.
61	RW	WO_OR	WO_CLEAR	FREE_USAGE_61A: Free usage.
62	RW	WO_OR	WO_CLEAR	FREE_USAGE_62A: Free usage.
63	RW	WO_OR	WO_CLEAR	FREE_USAGE_63A: Free usage.

Register Name	**Chiplet Control Register 1**
Mnemonic	TP.TCEC14.CORE.CPLT_CTRL1
Address	000000002E000001 (SCOM) 000000002E000011 (SCOM1) 000000002E000021 (SCOM2)
Description	This register contains the second set of vital chiplet controls.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_OR	WO_CLEAR	UNUSED_0B: Unused.
1	RW	WO_OR	WO_CLEAR	UNUSED_1B: Unused.
2	RW	WO_OR	WO_CLEAR	UNUSED_2B: Unused.
3	RW	WO_OR	WO_CLEAR	TC_VITL_REGION_FENCE: VITL fence. VITL fence. Protect the VITL region logic from pollution by other regions during LBIST, or when the chiplet is not initialized and running yet.
4	RW	WO_OR	WO_CLEAR	TC_PERV_REGION_FENCE: Fence for the pervasive region.
5	RW	WO_OR	WO_CLEAR	TC_REGION1_FENCE: Fence for region c00 (LSU, IFU, PC).
6	RW	WO_OR	WO_CLEAR	TC_REGION2_FENCE: Fence for region c01 (ISU, VSU).
7	RW	WO_OR	WO_CLEAR	UNUSED_7B: Unused.
8	RW	WO_OR	WO_CLEAR	UNUSED_8B: Unused.
9	RW	WO_OR	WO_CLEAR	UNUSED_9B: Unused.
10	RW	WO_OR	WO_CLEAR	UNUSED_10B: Unused.
11	RW	WO_OR	WO_CLEAR	UNUSED_11B: Unused.
12	RW	WO_OR	WO_CLEAR	UNUSED_12B: Unused.
13	RW	WO_OR	WO_CLEAR	UNUSED_13B: Unused.
14	RW	WO_OR	WO_CLEAR	UNUSED_14B: Unused.
15	RW	WO_OR	WO_CLEAR	RESERVED: Reserved.
16	RW	WO_OR	WO_CLEAR	TC_UNIT_MULTICYCLE_TEST_FENCE:
17	RW	WO_OR	WO_CLEAR	UNUSED_17B: Unused.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
18	RW	WO_OR	WO_CLEAR	UNUSED_18B: Unused.
19	RW	WO_OR	WO_CLEAR	UNUSED_19B: Unused.
20	RW	WO_OR	WO_CLEAR	UNUSED_20B: Unused.
21	RW	WO_OR	WO_CLEAR	UNUSED_21B: Unused.
22	RW	WO_OR	WO_CLEAR	UNUSED_22B: Unused.
23	RW	WO_OR	WO_CLEAR	UNUSED_23B: Unused.
24	RW	WO_OR	WO_CLEAR	UNUSED_24B: Unused.
25	RW	WO_OR	WO_CLEAR	UNUSED_25B: Unused.
26	RW	WO_OR	WO_CLEAR	UNUSED_26B: Unused.
27	RW	WO_OR	WO_CLEAR	UNUSED_27B: Unused.
28	RW	WO_OR	WO_CLEAR	UNUSED_28B: Unused.
29	RW	WO_OR	WO_CLEAR	UNUSED_29B: Unused.
30	RW	WO_OR	WO_CLEAR	UNUSED_30B: Unused.
31	RW	WO_OR	WO_CLEAR	UNUSED_31B: Unused.

Register Name	Chiplet Configuration Register 0
Mnemonic	TP.TCEC14.CORE.CPLT_CONF0
Address	000000002E000008 (SCOM) 000000002E000018 (SCOM1) 000000002E000028 (SCOM2)
Description	This register contains the first set of vital chiplet configuration functions.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:5	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE0_SEL_DC: Probe 0 select.
6	RW	WO_OR	WO_CLEAR	RESERVED_6C: Reserved.
7	RW	WO_OR	WO_CLEAR	RESERVED_7C: Reserved.
8:13	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE1_SEL_DC: Probe 1 select.
14	RW	WO_OR	WO_CLEAR	RESERVED_14C: Reserved.
15	RW	WO_OR	WO_CLEAR	RESERVED_15C: Reserved.
16:21	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE2_SEL_DC: Probe 2 select.
22	RW	WO_OR	WO_CLEAR	RESERVED_22C: Reserved.
23	RW	WO_OR	WO_CLEAR	RESERVED_23C: Reserved.
24:29	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE3_SEL_DC: Probe 3 select.
30	RW	WO_OR	WO_CLEAR	RESERVED_30C: Reserved.
31	RW	WO_OR	WO_CLEAR	RESERVED_31C: Reserved.
32	RW	WO_OR	WO_CLEAR	CTRL_CC_OFLOW_FEH_SEL_DC: Enables ABIST overflow or failure indication.
33	RW	WO_OR	WO_CLEAR	CTRL_CC_SCAN_PROTECT_DC: Enables scan protection and the scan collision error mechanism.
34	RW	WO_OR	WO_CLEAR	CTRL_CC_SDIS_DC_N: Disables the scan diagnostic scan path.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
35	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_35C: Reserved for test control.
36	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_36C: Reserved for test control.
37	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_37C: Reserved for test control.
38	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_38C: Reserved for test control.
39	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_39C: Reserved for test control.
40	RW	WO_OR	WO_CLEAR	CTRL_EPS_MASK_VITL_PCB_ERR_DC: Mask VITL PCB errors from CC or CPLT_CTRL.
41	RW	WO_OR	WO_CLEAR	CTRL_CC_MASK_VITL_SCAN_OPCG_ERR_DC: Mask VITL errors in CC, which are not PCB related.
42	RW	WO_OR	WO_CLEAR	RESERVED_42C: Reserved.
43	RW	WO_OR	WO_CLEAR	RESERVED_43C: Reserved.
44	RW	WO_OR	WO_CLEAR	FREE_USAGE_44C: Free usage.
45	RW	WO_OR	WO_CLEAR	FREE_USAGE_45C: Free usage.
46	RW	WO_OR	WO_CLEAR	FREE_USAGE_46C: Free usage.
47	RW	WO_OR	WO_CLEAR	FREE_USAGE_47C: Free usage.
48:51	RW	WO_OR	WO_CLEAR	TC_UNIT_GROUP_ID_DC: Group ID.
52:54	RW	WO_OR	WO_CLEAR	TC_UNIT_CHIP_ID_DC: Chip ID.
55	RW	WO_OR	WO_CLEAR	RESERVED_ID_55C: Reserved ID.
56:60	RW	WO_OR	WO_CLEAR	TC_UNIT_SYS_ID_DC: System ID.
61	RW	WO_OR	WO_CLEAR	RESERVED_ID_61C: Reserved ID.
62	RW	WO_OR	WO_CLEAR	RESERVED_ID_62C: Reserved ID.
63	RW	WO_OR	WO_CLEAR	RESERVED_ID_63C: Reserved ID.

Register Name	**Chiplet Configuration Register 1**
Mnemonic	TP.TCEC14.CORE.CPLT_CONF1
Address	000000002E000009 (SCOM) 000000002E000019 (SCOM1) 000000002E000029 (SCOM2)
Description	This register contains the second set of vital chiplet configuration functions.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_OR	WO_CLEAR	UNUSED_0D: Unused.
1	RW	WO_OR	WO_CLEAR	UNUSED_1D: Unused.
2	RW	WO_OR	WO_CLEAR	UNUSED_2D: Unused.
3	RW	WO_OR	WO_CLEAR	UNUSED_3D: Unused.
4	RW	WO_OR	WO_CLEAR	IOVALID_4D:
5	RW	WO_OR	WO_CLEAR	IOVALID_5D:
6	RW	WO_OR	WO_CLEAR	IOVALID_6D:
7	RW	WO_OR	WO_CLEAR	IOVALID_7D:
8	RW	WO_OR	WO_CLEAR	IOVALID_8D:
9	RW	WO_OR	WO_CLEAR	IOVALID_9D:

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
10	RW	WO_OR	WO_CLEAR	IOVALID_10D:
11	RW	WO_OR	WO_CLEAR	IOVALID_11D:
12	RW	WO_OR	WO_CLEAR	FREE_USAGE_12D: Free usage.
13	RW	WO_OR	WO_CLEAR	FREE_USAGE_13D: Free usage.
14	RW	WO_OR	WO_CLEAR	FREE_USAGE_14D: Free usage.
15	RW	WO_OR	WO_CLEAR	FREE_USAGE_15D: Free usage.
16	RW	WO_OR	WO_CLEAR	FREE_USAGE_16D: Free usage.
17	RW	WO_OR	WO_CLEAR	FREE_USAGE_17D: Free usage.
18	RW	WO_OR	WO_CLEAR	FREE_USAGE_18D: Free usage.
19	RW	WO_OR	WO_CLEAR	FREE_USAGE_19D: Free usage.
20	RW	WO_OR	WO_CLEAR	FREE_USAGE_20D: Free usage.
21	RW	WO_OR	WO_CLEAR	FREE_USAGE_21D: Free usage.
22	RW	WO_OR	WO_CLEAR	FREE_USAGE_22D: Free usage.
23	RW	WO_OR	WO_CLEAR	FREE_USAGE_23D: Free usage.
24	RW	WO_OR	WO_CLEAR	FREE_USAGE_24D: Free usage.
25	RW	WO_OR	WO_CLEAR	FREE_USAGE_25D: Free usage.
26	RW	WO_OR	WO_CLEAR	FREE_USAGE_26D: Free usage.
27	RW	WO_OR	WO_CLEAR	FREE_USAGE_27D: Free usage.
28	RW	WO_OR	WO_CLEAR	FREE_USAGE_28D: Free usage.
29	RW	WO_OR	WO_CLEAR	FREE_USAGE_29D: Free usage.
30	RW	WO_OR	WO_CLEAR	FREE_USAGE_30D: Free usage.
31	RW	WO_OR	WO_CLEAR	FREE_USAGE_31D: Free usage.

Register Name	Chiplet Status Register
Mnemonic	TP.TCEC14.CORE.CPLT_STAT0
Address	000000002E000100 (SCOM)
Description	An interrupt is sent out on a bit change if not masked by the Chiplet Mask Register. A mask only masks the interrupt, not the status register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	SRAM_ABIST_DONE_DC: SRAM and eDRAM ABIST done.
1	ROX	DRAM_ABIST_DONE_DC: Unused in POWER9 DD1.
2	ROX	RESERVED_2E: Reserved.
3	ROX	RESERVED_3E: Reserved.
4	ROX	TC_DIAG_PORT0_OUT: Diagnostic output port.
5	ROX	TC_DIAG_PORT1_OUT: Diagnostic output port.
6	ROX	RESERVED_6E: Reserved.
7	ROX	PLL_DESTOUT: Reserved.
8	ROX	CC_CTRL_OPCG_DONE_DC: OPCG done. For LBIST, ABIST, or other OPCG runs.
9	ROX	CC_CTRL_CHIPLET_IS_ALIGNED_DC: Indicates that a chiplet is aligned.

Bits	SCOM	Field Mnemonic: Description
10	ROX	PC_TC_VALID_NOT_HV_MODE: Chiplet specific.
11	ROX	PC_TC_AVP_OUT: Chiplet specific.
12	ROX	FREE_USAGE_12E: Free usage.
13	ROX	FREE_USAGE_13E: Free usage.
14	ROX	FREE_USAGE_14E: Free usage.
15	ROX	FREE_USAGE_15E: Free usage.
16	ROX	FREE_USAGE_16E: Free usage.
17	ROX	FREE_USAGE_17E: Free usage.
18	ROX	FREE_USAGE_18E: Free usage.
19	ROX	FREE_USAGE_19E: Free usage.
20	ROX	FREE_USAGE_20E: Free usage.
21	ROX	FREE_USAGE_21E: Free usage.
22	ROX	FREE_USAGE_22E: Free usage.
23	ROX	FREE_USAGE_23E: Free usage.

Register Name	Chiplet Mask Register
Mnemonic	TP.TCEC14.CORE.CPLT_MASK0
Address	000000002E000101 (SCOM)
Description	This register masks an interrupt when a bit changes in the Chiplet Status Register. It does not mask the status itself.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CPLTMASK0: Bitwise masking of the Chiplet Status Register.

Register Name	Control Protect Mode Register
Mnemonic	TP.TCEC14.CORE.CTRL_PROTECT_MODE_REG
Address	000000002E0003FE (SCOM)
Description	This register enables read and write protection.

Bits	SCOM	Field Mnemonic: Description
0	RW	CTRL_READ_PROTECT_ENABLE: Enable read protection.
1	RW	CTRL_WRITE_PROTECT_ENABLE: Enable write protection.

Register Name	Atomic Lock Register
Mnemonic	TP.TCEC14.CORE.CTRL_ATOMIC_LOCK_REG
Address	000000002E0003FF (SCOM)
Description	This register enables an atomic lock and an atomic lock counter.

Bits	SCOM	Field Mnemonic: Description
0	RW	CTRL_ATOMIC_LOCK_ENABLE: Enable atomic lock.

Bits	SCOM	Field Mnemonic: Description
1:4	ROX	CTRL_ATOMIC_ID: Atomic ID.
5:7	RO	constant = 0b000
8:15	ROX	CTRL_ATOMIC_ACTIVITY: Atomic lock counter.

Register Name	PSCOMLE Mode Register
Mnemonic	TP.TCEC14.CORE.EPS.PSC.PSC.PSCOM_MODE_REG
Address	000000002E010000 (SCOM)
Description	This is the parallel-to-serial communication light edition (PSCOMLE) mode register.

Bits	SCOM	Field Mnemonic: Description
0	RW	ABORT_ON_PCB_ADDR_PARITY_ERROR: Abort on PCB address parity error.
1	RW	ABORT_ON_PCB_WDATA_PARITY_ERROR: Abort on PCB write data parity error.
2	RW	ABORT_ON_DL_RETURN_P0_ERROR: Unused.
3	RW	ABORT_ON_DL_RETURN_WDATA_PARITY_ERROR: Abort on DL return write data parity error.
4	RW	WATCHDOG_ENABLE: Enable watchdog.
5:6	RW	SCOM_HANG_LIMIT: 0b11 = 256 0b10 = 512 0b01 = 768 0b00 = 1023
7	RW	FORCE_ALL_RINGS: Set to a logical 1 if all rings should be enabled independent of the ring address.
8	RW	FSM_SELFRESET_ON_STATEVEC_PARITYERROR_ENABLE: FSM self reset on statevec parity error enable.
9:11	RW	RESERVED_PSCOM_MODE_LT: Reserved.

Register Name	PSCOMLE Error Register
Mnemonic	TP.TCEC14.CORE.EPS.PSC.PSC.PSCOM_STATUS_ERROR_REG
Address	000000002E010001 (SCOM)
Description	This is the parallel-to-serial communication light edition (PSCOMLE) error register.

Bits	SCOM	Field Mnemonic: Description
0	RWX	ACCUMULATED_PCB_WDATA_PARITY_ERROR: Accumulated PCB write data parity error.
1	RWX	ACCUMULATED_PCB_ADDRESS_PARITY_ERROR: Accumulated PCB address parity error.
2	RWX	ACCUMULATED_DL_RETURN_WDATA_PARITY_ERROR: Accumulated DL return write data parity error.
3	RWX	ACCUMULATED_DL_RETURN_P0_ERROR: Accumulated DL return P0 error.
4	RWX	ACCUMULATED_UL_RDATA_PARITY_ERROR: Accumulated UL read data parity error.
5	RWX	ACCUMULATED_UL_P0_ERROR: Accumulated UL P0 error.
6	RWX	ACCUMULATED_PARITY_ERROR_ON_INTERFACE_MACHINE: Accumulated parity error on interface machine.
7	RWX	ACCUMULATED_PARITY_ERROR_ON_P2S_MACHINE: Accumulated parity error on p2s machine.
8	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_ULCCH: Accumulated timeout while waiting for ULCCH.

Bits	SCOM	Field Mnemonic: Description
9	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: Accumulated timeout while waiting for DLDCH return.
10	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_ULDCH: Accumulated timeout while waiting for ULDCH.
11	RWX	ACCUMULATED_PSCOM_PARALLEL_WRITE_NVLD: Accumulated PSCOM parallel write NVLD.
12	RWX	ACCUMULATED_PSCOM_PARALLEL_READ_NVLD: Accumulated PSCOM parallel read NVLD.
13	RWX	ACCUMULATED_PSCOM_PARALLEL_ADDR_INVALID: Accumulated PSCOM parallel address invalid.
14	RWX	ACCUMULATED_PCB_COMMAND_PARITY_ERROR: Accumulated PCB command parity error.
15	RWX	ACCUMULATED_GENERAL_TIMEOUT: Accumulated general timeout.
16	RWX	ACCUMULATED_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: Accumulated satellite acknowledge access violation.
17	RWX	ACCUMULATED_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: Accumulated satellite acknowledge invalid register.
18	RWX	TRAPPED_PCB_WDATA_PARITY_ERROR: Trapped PCB write data parity error.
19	RWX	TRAPPED_PCB_ADDRESS_PARITY_ERROR: Trapped PCB address parity error.
20	RWX	TRAPPED_DL_RETURN_WDATA_PARITY_ERROR: Trapped DL return write data parity error.
21	RWX	TRAPPED_DL_RETURN_P0_ERROR: Trapped DL return P0 error.
22	RWX	TRAPPED_UL_RDATA_PARITY_ERROR: Trapped UL read data parity error.
23	RWX	TRAPPED_UL_P0_ERROR: Trapped UL P0 error.
24	RWX	TRAPPED_PARITY_ERROR_ON_INTERFACE_MACHINE: Trapped parity error on interface machine.
25	RWX	TRAPPED_PARITY_ERROR_ON_P2S_MACHINE: Trapped parity error on p2s machine.
26	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_ULCCH: Trapped timeout while waiting for ULCCH.
27	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: Trapped timeout while waiting for DLDCH return.
28	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_ULDCH: Trapped timeout while waiting for ULDCH.
29	RWX	TRAPPED_PSCOM_PARALLEL_WRITE_NVLD: Trapped PSCOM parallel write NVLD.
30	RWX	TRAPPED_PSCOM_PARALLEL_READ_NVLD: Trapped PSCOM parallel read NVLD.
31	RWX	TRAPPED_PSCOM_PARALLEL_ADDR_INVALID: Trapped PSCOM parallel address invalid.
32	RWX	TRAPPED_PCB_COMMAND_PARITY_ERROR: Trapped PCB command parity error.
33	RWX	TRAPPED_GENERAL_TIMEOUT: Trapped general timeout.
34	RWX	TRAPPED_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: Trapped satellite acknowledge access violation.
35	RWX	TRAPPED_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: Trapped satellite acknowledge invalid register.

Register Name	PSCOMLE Error Mask Register
Mnemonic	TP.TCEC14.CORE.EPS.PSC.PSC.PSCOM_ERROR_MASK
Address	000000002E010002 (SCOM)
Description	This is the parallel-to-serial communication light edition (PSCOMLE) error mask register.

Bits	SCOM	Field Mnemonic: Description
0	RW	MASK_PCB_WDATA_PARITY_ERROR: Mask PCB write data parity error.

Bits	SCOM	Field Mnemonic: Description
1	RW	MASK_PCB_ADDRESS_PARITY_ERROR: Mask PCB address parity error.
2	RW	MASK_DL_RETURN_WDATA_PARITY_ERROR: Mask DL return write data parity error.
3	RW	MASK_DL_RETURN_P0_ERROR: Mask DL return P0 error.
4	RW	MASK_UL_RDATA_PARITY_ERROR: Mask UL read data parity error.
5	RW	MASK_UL_P0_ERROR: Mask UL P0 error.
6	RW	MASK_PARITY_ERROR_ON_INTERFACE_MACHINE: Mask parity error on interface machine.
7	RW	MASK_PARITY_ERROR_ON_P2S_MACHINE: Mask parity error on p2s machine.
8	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_ULCCH: Mask timeout while waiting for ULCCH.
9	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: Mask timeout while waiting for DLDCH return.
10	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_ULDCH: Mask timeout while waiting for ULDCH.
11	RW	MASK_PSCOM_PARALLEL_WRITE_NVLD: Mask PSCOM parallel write NVLD.
12	RW	MASK_PSCOM_PARALLEL_READ_NVLD: Mask PSCOM parallel read NVLD.
13	RW	MASK_PSCOM_PARALLEL_ADDR_INVALID: Mask PSCOM parallel address invalid.
14	RW	MASK_PCB_COMMAND_PARITY_ERROR: Mask PCB command parity error.
15	RW	MASK_GENERAL_TIMEOUT: Mask general timeout.
16	RW	MASK_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: Mask satellite acknowledge access violation.
17	RW	MASK_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: Mask satellite acknowledge invalid register.

Register Name	PSCOMLE Address Trap Register
Mnemonic	TP.TCEC14.CORE.EPS.PSC.PSC.ADDR_TRAP_REG
Address	000000002E010003 (SCOM)
Description	This is the parallel-to-serial communication light edition (PSCOMLE) address trap register.

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	PCB_ADDRESS_OF_LAST_TRANSACTION_WITH_ERROR: PCB address of the last transaction with an error.
16	ROX	PCB_READ_NOTWRITE_OF_LAST_TRANSACTION_WITH_ERROR: PCB read, not write, of the last transaction with an error.
17	ROX	RESERVED_ADDR_LAST_TRAP_LT: Reserved_0.
18:30	ROX	SERIAL2PARALLEL_STATE_MACHINE_AT_TIME_OF_ERROR: Serial2 parallel state machine at the time of the error.
31	ROX	SATELLITE_ACKNOWLEDGE_BIT_RETURN_PARITY: This bit is set to 1 if no parity error is detected in the satellite number or acknowledgment bits.
32	ROX	SATELLITE_ACKNOWLEDGE_BIT_WRITE_PARITY_ERROR: Set if a write parity error is detected by the satellite.
33	ROX	SATELLITE_ACKNOWLEDGE_BIT_ACCESS_VIOLATION: Set if an invalid read or write access is detected by the satellite.
34	ROX	SATELLITE_ACKNOWLEDGE_BIT_INVALID_REGISTER: Set if an invalid register address is detected by the satellite.

Register Name	Ring Lock Enable Register
Mnemonic	TP.TCEC14.CORE.EPS.PSC.PSC.WRITE_PROTECT_ENABLE_REG
Address	000000002E010005 (SCOM)
Description	This register enables the ring lock.

Bits	SCOM	Field Mnemonic: Description
0	RW	ENABLE_RING_LOCKING: General enable of ring locking upon a write to a specific ring.
1	RW	RESERVED_RING_LOCKING: Reserved.

Register Name	Write Protect Rings Register
Mnemonic	TP.TCEC14.CORE.EPS.PSC.PSC.WRITE_PROTECT_RINGS_REG
Address	000000002E010006 (SCOM)
Description	This register writes ring protect bit maps.

Bits	SCOM	Field Mnemonic: Description
0:15	RW	WRITE_PROTECT_RINGS: Write a protect bit map for each ring.

Register Name	Atomic Lock Mask Register
Mnemonic	TP.TCEC14.CORE.EPS.PSC.PSC.ATOMIC_LOCK_MASK_LATCH_REG
Address	000000002E010007 (SCOM)
Description	This register provides a bit mask for atomic locking.

Bits	SCOM	Field Mnemonic: Description
0:15	RW	ATOMIC_LOCK_MASK: A bit mask for atomic locking on a ring-by-ring basis.

Register Name	Ring Fence Enable Mask Register
Mnemonic	TP.TCEC14.CORE.EPS.PSC.PSC.RING_FENCE_MASK_LATCH_REG
Address	000000002E010008 (SCOM)
Description	This register provides a bit mask for ring fencing.

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b0
1:15	RW	RING_FENCE_ENABLE_MASK: Enable bit mask for ring fencing on a ring-by-ring basis.

Register Name	Debug Mode Register
Mnemonic	TP.TCEC14.CORE.EPS.DBG.DBG_MODE_REG
Address	000000002E0107C0 (SCOM)
Description	This is debug macro configuration register 0 for the configuration component.

Bits	SCOM	Field Mnemonic: Description
0:2	RW	GLB_BRCST_MODE: Global broadcast mode (0 to 2): 100 = dbg_trace_run and dbg_trace_freeze. 101 = pc_tcdbg_trace_run_fncd and dbg_trace_freeze. 110 = dbg_triggers_out (0 to 1). 111 = pc_tcdbg_triggers (0 to 1) (from core).
3:5	RW	TRACE_SEL_MODE: Select source for trace run and bank. 001 = Core trace run and bank. 010 = tp broadcast run and 0. 011 = tc_dbg_inter_brcst latched. 100 = tc_dbg_dbg_sync_brcst_rcv. else = dbg_trace_run and dbg_trace_bank.
6:7	RW	TRIG_SEL_MODE: Select source for tcdbg trigger (0). 10 = Global broadcast. 11 = pc_tcdbg_trigger (from core). else = dbg_triggers_out (0:1).
8	RW	STOP_ON_XSTOP_SELECTION: Enable trace stop on checkstop.
9	RW	STOP_ON_RECOV_ERR_SELECTION: Enable trace stop on recoverable error.
10	RW	STOP_ON_SPATTN_SELECTION: Enable trace stop on special attention.
11	RW	FREEZE_SEL_MODE: Select freeze source: 0 = Local debug freeze. 1 = Via broadcast: tp_tcdbg_glb_brcst(1).
12:13	RW	SYNC_BRCST_MODE: Originally used for synchronous broadcast mode. Currently obsolete. See trace_sel_mode.
14	RO	constant = 0b0 sync_brcst_mode.
15	RO	constant = 0b0.
16:31	ROX	dbg_status.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	Debug Instance 1 Condition 1 Register
Mnemonic	TP.TCEC14.CORE.EPS.DBG.DBG_INST1_COND_REG_1
Address	000000002E0107C1 (SCOM)
Description	This is debug macro configuration register 1 for front-end component 1.

Bits	SCOM	Field Mnemonic: Description
0:7	RW	INST1_COND1_SEL_A: Multiplexer for cond1_trig_in(0). 000 = Select constant 0 001 = Select constant 1 -- CONDITION FEEDBACK -- 002 = Select inst1_dbg_cond1. 003 = Select inst1_dbg_cond2. 004 = Select inst1_dbg_cond3. 005 = Select inst1_dbg_cond2timeout. 006 = Select inst2_dbg_cond1. 007 = Select inst2_dbg_cond2. 008 = Select inst2_dbg_cond3. 009 = Select inst2_dbg_cond2timeout. 010 = Select inst3_dbg_cond1. Unused, tied down. 011 = Select inst3_dbg_cond2. Unused, tied down. 012 = Select inst3_dbg_cond3. Unused, tied down. 013 = Select inst3_dbg_cond2timeout. Unused, tied down. 014 = Select inst4_dbg_cond1. Unused, tied down. 015 = Select inst4_dbg_cond2. Unused, tied down. 016 = Select inst4_dbg_cond3. Unused, tied down. 017 = Select inst4_dbg_cond2timeout. Unused, tied down. 018 = Select inst1_dbg_trig_sp. 019 = Select inst2_dbg_trig_sp. 020 = Select inst3_dbg_trig_sp. Unused, tied down. 021 = Select inst4_dbg_trig_sp. Unused, tied down. 022 = Select tctrc_tcdbg_trigger_a(0). 023 = Select tctrc_tcdbg_trigger_b(0). 024 = Select tctrc_tcdbg_trigger_a(0) and tctrc_tcdbg_trigger_b(0). 025 = Select tctrc_tcdbg_trigger_a(1). 026 = Select tctrc_tcdbg_trigger_b(1). 027 = Select tctrc_tcdbg_trigger_a(1) and tctrc_tcdbg_trigger_b(1). 028 = Select tctrc_tcdbg_trigger_a(2). 029 = Select tctrc_tcdbg_trigger_b(2). 030 = Select tctrc_tcdbg_trigger_a(2) and tctrc_tcdbg_trigger_b(2). 031 = Select tctrc_tcdbg_trigger_a(3). 032 = Select tctrc_tcdbg_trigger_b(3). 033 = Select tctrc_tcdbg_trigger_a(3) and tctrc_tcdbg_trigger_b(3). 034 = Select tctrc_tcdbg_trigger_a(4). 035 = Select tctrc_tcdbg_trigger_b(4). 036 = Select tctrc_tcdbg_trigger_a(4) and tctrc_tcdbg_trigger_b(4). 037 = Select tctrc_tcdbg_trigger_a(5). 038 = Select tctrc_tcdbg_trigger_b(5). 039 = Select tctrc_tcdbg_trigger_a(5) and tctrc_tcdbg_trigger_b(5). 040 = Select tctrc_tcdbg_trigger_a(6). 041 = Select tctrc_tcdbg_trigger_b(6). 042 = Select tctrc_tcdbg_trigger_a(6) and tctrc_tcdbg_trigger_b(6). 043 = Select tctrc_tcdbg_trigger_a(7). 044 = Select tctrc_tcdbg_trigger_b(7). 045 = Select tctrc_tcdbg_trigger_a(7) and tctrc_tcdbg_trigger_b(7). 046 = Select tctrc_tcdbg_trigger_a(8). 047 = Select tctrc_tcdbg_trigger_b(8). 048 = Select tctrc_tcdbg_trigger_a(8) and tctrc_tcdbg_trigger_b(8). 049 = Select tctrc_tcdbg_trigger_a(9). 050 = Select tctrc_tcdbg_trigger_b(9). 051 = Select tctrc_tcdbg_trigger_a(9) and tctrc_tcdbg_trigger_b(9). 052 = Select tctrc_tcdbg_trigger_a(10). 053 = Select tctrc_tcdbg_trigger_b(10). 054 = Select tctrc_tcdbg_trigger_a(10) and tctrc_tcdbg_trigger_b(10). 055 = Select tctrc_tcdbg_trigger_a(11). 056 = Select tctrc_tcdbg_trigger_b(11). 057 = Select tctrc_tcdbg_trigger_a(11) and tctrc_tcdbg_trigger_b(11). 058 = Select tctrc_tcdbg_trigger_a(12). 059 = Select tctrc_tcdbg_trigger_b(12).

Bits	SCOM	Field Mnemonic: Description
8:15	RW	INST1_COND1_SEL_B: Multiplexer for cond1_trig_in(1). Selection as cond1_trig_in(0).
16:23	RW	INST1_COND2_SEL_A: Multiplexer for cond2_trig_in(0). Selection as cond1_trig_in(0).
24:31	RW	INST1_COND2_SEL_B: Multiplexer for cond2_trig_in(1). Selection as cond1_trig_in(0).
32	RW	INST1_C1_INAROW_MODE: Front-end instance 1, counter 1 in-a-row mode.
33	RW	INST1_AND_TRIGGER_MODE1: Front-end instance 1 and trigger mode condition 1.
34	RW	INST1_NOT_TRIGGER_MODE1: Front-end instance 1 inverted trigger mode condition 1.
35	RW	INST1_EDGE_TRIGGER_MODE1: Front-end instance 1 edge trigger mode condition 1.
36:38	RWX	INST1_UNUSED_1: Unused.
39	RW	INST1_C2_INAROW_MODE: Front-end instance 1, counter 2 in-a-row mode.
40	RW	INST1_AND_TRIGGER_MODE2: Front-end instance 1 and trigger mode 2.
41	RW	INST1_NOT_TRIGGER_MODE2: Front-end instance 1 inverted (not) trigger.
42	RW	INST1_EDGE_TRIGGER_MODE2: Front-end instance 1 edge trigger.
43:45	RWX	INST1_UNUSED_2: Unused.
46	RW	INST1_COND3_ENABLE_RESET: Front-end instance 1 condition 3 enable.
47	RW	INST1_EXACT_TO_MODE: Front-end instance 1 exact timeout mode.
48	RW	INST1_RESET_C2TIMER_ON_C1: Front-end instance 1 reset condition 2 timer on condition 1.
49	RW	INST1_RESET_C3_ON_C0: Front-end instance 1 reset condition 3 on condition 0.
50	RW	INST1_SLOW_TO_MODE: Front-end instance 1 slow timeout mode.
51	RW	INST1_EXACT_RESET_C3_ON_TO: Front-end instance 1 exact reset condition 3 on timeout.
52:55	RW	INST1_C1_COUNT_LT: Instance 1 condition 1 counter compare value.
56:59	RW	INST1_C2_COUNT_LT: Instance 1 condition 2 counter compare value.
60:62	RW	INST1_RESET_C3_SELECT: Front-end instance 1, reset condition 3 for reset_c3_on_c0. 0b100 = dbg_cross_couple_triggers(4). 0b101 = dbg_cross_couple_triggers(12). 0b110 = dbg_cross_couple_triggers(20). 0b111 = dbg_cross_couple_triggers(28).

Register Name	Debug Instance 1 Condition 2 Register
Mnemonic	TP.TCEC14.CORE.EPS.DBG.DBG_INST1_COND_REG_2
Address	000000002E0107C2 (SCOM)
Description	This is debug macro configuration register 2 for front-end component 1.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	INST1_CROSS_COUPLE_SELECT_1_A: Cross coupling is the same for all selectors: 00000 = Selects inst1_cond1_trig_a. 00001 = Selects inst1_cond1_trig_b. 00010 = Selects inst1_cond2_trig_a. 00011 = Selects inst1_cond2_trig_b. 00100 = Selects inst1_condition1. 00101 = Selects inst1_condition2. 00110 = Selects inst1_condition3. 00111 = Selects inst1_cond2_timeout. 01000 = Selects inst2_cond1_trig_a. 01001 = Selects inst2_cond1_trig_b. 01010 = Selects inst2_cond2_trig_a. 01011 = Selects inst2_cond2_trig_b. 01100 = Selects inst2_condition1. 01101 = Selects inst2_condition2. 01110 = Selects inst2_condition3. 01111 = Selects inst2_cond2_timeout. 10000 = Selects inst3_cond1_trig_a. 10001 = Selects inst3_cond1_trig_b. 10010 = Selects inst3_cond2_trig_a. 10011 = Selects inst3_cond2_trig_b. 10100 = Selects inst3_condition1. 10101 = Selects inst3_condition2. 10110 = Selects inst3_condition3. 10111 = Selects inst3_cond2_timeout. 11000 = Selects inst4_cond1_trig_a. 11001 = Selects inst4_cond1_trig_b. 11010 = Selects inst4_cond2_trig_a. 11011 = Selects inst4_cond2_trig_b. 11100 = Selects inst4_condition1. 11101 = Selects inst4_condition2. 11110 = Selects inst4_condition3. 11111 = Selects inst4_cond2_timeout.
5:9	RW	INST1_CROSS_COUPLE_SELECT_1_B: Instance 1 cross couple select 1_b.
10:14	RW	INST1_CROSS_COUPLE_SELECT_2_A: Instance 1 cross couple select 2_a.
15:19	RW	INST1_CROSS_COUPLE_SELECT_2_B: Instance 1 cross couple select 2_b.
20:43	RW	INST1_TO_CMP_LT: Compare value for special counter sp_cnt_lt in debug component 1.
44	RW	INST1_FORCE_TEST_MODE: Force test mode to indicate compare without actual compare.

Register Name	Debug Instance 1 Condition 3 Register
Mnemonic	TP.TCEC14.CORE.EPS.DBG.DBG_INST1_COND_REG_3
Address	000000002E0107C3 (SCOM)
Description	This is debug macro configuration register 2 for the front-end 1 component.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	INST1_SP_COUNT_LT: Timeout counter to_cmp compare value for dbg_cond_comp_1.

Register Name	**Debug Instance 2 Condition 1 Register**
Mnemonic	TP.TCEC14.CORE.EPS.DBG.DBG_INST2_COND_REG_1
Address	000000002E0107C4 (SCOM)
Description	This is debug macro configuration register 1 for the front-end 1 component.

Bits	SCOM	Field Mnemonic: Description
0:7	RW	INST2_COND1_SEL_A: Multiplexer for cond1_trig_in(0). 000 = Select constant 0 001 = Select constant 1 -- CONDITION FEEDBACK -- 002 = Select inst2_dbg_cond1. 003 = Select inst2_dbg_cond2. 004 = Select inst2_dbg_cond3. 005 = Select inst2_dbg_cond2timeout. 006 = Select inst2_dbg_cond1. 007 = Select inst2_dbg_cond2. 008 = Select inst2_dbg_cond3. 009 = Select inst2_dbg_cond2timeout. 010 = Select inst3_dbg_cond1. Unused, tied down. 011 = Select inst3_dbg_cond2. Unused, tied down. 012 = Select inst3_dbg_cond3. Unused, tied down. 013 = Select inst3_dbg_cond2timeout. Unused, tied down. 014 = Select inst4_dbg_cond1. Unused, tied down. 015 = Select inst4_dbg_cond2. Unused, tied down. 016 = Select inst4_dbg_cond3. Unused, tied down. 017 = Select inst4_dbg_cond2timeout. Unused, tied down. 018 = Select inst2_dbg_trig_sp. 019 = Select inst2_dbg_trig_sp. 020 = Select inst3_dbg_trig_sp. Unused, tied down. 021 = Select inst4_dbg_trig_sp. Unused, tied down. 022 = Select tctrc_tcdbg_trigger_a(0). 023 = Select tctrc_tcdbg_trigger_b(0). 024 = Select tctrc_tcdbg_trigger_a(0) and tctrc_tcdbg_trigger_b(0). 025 = Select tctrc_tcdbg_trigger_a(1). 026 = Select tctrc_tcdbg_trigger_b(1). 027 = Select tctrc_tcdbg_trigger_a(1) and tctrc_tcdbg_trigger_b(1). 028 = Select tctrc_tcdbg_trigger_a(2). 029 = Select tctrc_tcdbg_trigger_b(2). 030 = Select tctrc_tcdbg_trigger_a(2) and tctrc_tcdbg_trigger_b(2). 031 = Select tctrc_tcdbg_trigger_a(3). 032 = Select tctrc_tcdbg_trigger_b(3). 033 = Select tctrc_tcdbg_trigger_a(3) and tctrc_tcdbg_trigger_b(3). 034 = Select tctrc_tcdbg_trigger_a(4). 035 = Select tctrc_tcdbg_trigger_b(4). 026 = Select tctrc_tcdbg_trigger_a(4) and tctrc_tcdbg_trigger_b(4). 027 = Select tctrc_tcdbg_trigger_a(5). 028 = Select tctrc_tcdbg_trigger_b(5). 029 = Select tctrc_tcdbg_trigger_a(5) and tctrc_tcdbg_trigger_b(5). 030 = Select tctrc_tcdbg_trigger_a(6). 031 = Select tctrc_tcdbg_trigger_b(6). 032 = Select tctrc_tcdbg_trigger_a(6) and tctrc_tcdbg_trigger_b(6). 033 = Select tctrc_tcdbg_trigger_a(7). 034 = Select tctrc_tcdbg_trigger_b(7). 035 = Select tctrc_tcdbg_trigger_a(7) and tctrc_tcdbg_trigger_b(7). 036 = Select tctrc_tcdbg_trigger_a(8). 037 = Select tctrc_tcdbg_trigger_b(8). 038 = Select tctrc_tcdbg_trigger_a(8) and tctrc_tcdbg_trigger_b(8). 039 = Select tctrc_tcdbg_trigger_a(9). 040 = Select tctrc_tcdbg_trigger_b(9). 041 = Select tctrc_tcdbg_trigger_a(9) and tctrc_tcdbg_trigger_b(9). 042 = Select xstop_err. 043 = Select recov_err. 044 = Select spattn. 045 = Select fir_dbg_local_xstop_err. 046 = Select tc_dbg_inter_brcst(0). 047 = Select tc_dbg_inter_brcst(1). -- LOGIC (UNIT) TRIGGERS -- EP: 0:3 L3C0, 4:7 L3C1, 8:9 GX, 10 TP (hang), 11 spare, 12:13 MCA, 14:15 spare.

Bits	SCOM	Field Mnemonic: Description
8:15	RW	INST2_COND1_SEL_B: Multiplexer for cond1_trig_in(1). Selection as cond1_trig_in(0).
16:23	RW	INST2_COND2_SEL_A: Multiplexer for cond2_trig_in(0). Selection as cond1_trig_in(0).
24:31	RW	INST2_COND2_SEL_B: Multiplexer for cond2_trig_in(1). Selection as cond1_trig_in(0).
32	RW	INST2_C1_INAROW_MODE: Front-end instance 1 counter 1 in-a-row mode.
33	RW	INST2_AND_TRIGGER_MODE1: Front-end instance 1 and trigger mode condition 1.
34	RW	INST2_NOT_TRIGGER_MODE1: Front-end instance 1 inverted trigger mode condition 1.
35	RW	INST2_EDGE_TRIGGER_MODE1: Front-end instance 1 edge trigger mode condition 1.
36:38	RWX	INST2_UNUSED_1: Unused.
39	RW	INST2_C2_INAROW_MODE: Front-end instance 1 counter 2 in-a-row mode.
40	RW	INST2_AND_TRIGGER_MODE2: Front-end instance 1 and trigger mode 2.
41	RW	INST2_NOT_TRIGGER_MODE2: Front-end instance 1 inverted (not) trigger.
42	RW	INST2_EDGE_TRIGGER_MODE2: Front-end instance 1 edge trigger.
43:45	RWX	INST2_UNUSED_2: Unused.
46	RW	INST2_COND3_ENABLE_RESET: Front-end instance 1 condition 3 enable.
47	RW	INST2_EXACT_TO_MODE: Front-end instance 1 exact timeout mode.
48	RW	INST2_RESET_C2TIMER_ON_C1: Front-end instance 1 reset condition 2 timer on condition 1.
49	RW	INST2_RESET_C3_ON_C0: Front-end instance 1 reset condition 3 on condition 0.
50	RW	INST2_SLOW_TO_MODE: Front-end instance 1 slow timeout mode.
51	RW	INST2_EXACT_RESET_C3_ON_TO: Front-end instance 1 exact reset condition 3 on timeout.
52:55	RW	INST2_C1_COUNT_LT: Instance 2 condition 1 counter compare value.
56:59	RW	INST2_C2_COUNT_LT: Instance 2 condition 2 counter compare value.
60:62	RW	INST2_RESET_C3_SELECT: Front-end instance 1: reset condition 3 for reset_c3_on_c0. 0b100 = dbg_cross_couple_triggers(4). 0b101 = dbg_cross_couple_triggers(12). 0b110 = dbg_cross_couple_triggers(20). 0b111 = dbg_cross_couple_triggers(28).

Register Name	Debug Instance 2 Condition 2 Register
Mnemonic	TP.TCEC14.CORE.EPS.DBG.DBG_INST2_COND_REG_2
Address	000000002E0107C5 (SCOM)
Description	This is debug macro configuration register 2 for the front-end 1 component.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	INST2_CROSS_COUPLE_SELECT_1_A: Cross coupling is the same for all selectors: 00000 = Selects inst2_cond1_trig_a. 00001 = Selects inst2_cond1_trig_b. 00010 = Selects inst2_cond2_trig_a. 00011 = Selects inst2_cond2_trig_b. 00100 = Selects inst2_condition1. 00101 = Selects inst2_condition2. 00110 = Selects inst2_condition3. 00111 = Selects inst2_cond2_timeout. 01000 = Selects inst2_cond1_trig_a. 01001 = Selects inst2_cond1_trig_b. 01010 = Selects inst2_cond2_trig_a. 01011 = Selects inst2_cond2_trig_b. 01100 = Selects inst2_condition1. 01101 = Selects inst2_condition2. 01110 = Selects inst2_condition3. 01111 = Selects inst2_cond2_timeout. 10000 = Selects inst3_cond1_trig_a. 10001 = Selects inst3_cond1_trig_b. 10010 = Selects inst3_cond2_trig_a. 10011 = Selects inst3_cond2_trig_b. 10100 = Selects inst3_condition1. 10101 = Selects inst3_condition2. 10110 = Selects inst3_condition3. 10111 = Selects inst3_cond2_timeout. 11000 = Selects inst4_cond1_trig_a. 11001 = Selects inst4_cond1_trig_b. 11010 = Selects inst4_cond2_trig_a. 11011 = Selects inst4_cond2_trig_b. 11100 = Selects inst4_condition1. 11101 = Selects inst4_condition2. 11110 = Selects inst4_condition3. 11111 = Selects inst4_cond2_timeout.
5:9	RW	INST2_CROSS_COUPLE_SELECT_1_B: Instance 2 cross couple select 1_b.
10:14	RW	INST2_CROSS_COUPLE_SELECT_2_A: Instance 2 cross couple select 2_a.
15:19	RW	INST2_CROSS_COUPLE_SELECT_2_B: Instance 2 cross couple select 2_b.
20:43	RW	INST2_TO_CMP_LT: Compare value for special counter sp_cnt_lt in debug component 2.
44	RW	INST2_FORCE_TEST_MODE: Force test mode to indicate compare without actual compare.

Register Name	Debug Instance 2 Condition 3 Register
Mnemonic	TP.TCEC14.CORE.EPS.DBG.DBG_INST2_COND_REG_3
Address	000000002E0107C6 (SCOM)
Description	This is debug macro configuration register 2 for the front-end 1 component.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	INST2_SP_COUNT_LT: Timeout counter to_cmp compare value for dbg_cond_comp_1.

Register Name	Debug Trace 0 Register
Mnemonic	TP.TCEC14.CORE.EPS.DBG.DBG_TRACE_REG_0
Address	000000002E0107CD (SCOM)
Description	This is debug macro configuration register 0 for the debug back-end component.

Bits	SCOM	Field Mnemonic: Description
0	RW	INST1_COND3_ENABLE: Enable instance 1 condition 3.
1	RW	INST2_COND3_ENABLE: Enable instance 2 condition 3.
2	RW	INST3_COND3_ENABLE: Unused.
3	RW	INST4_COND3_ENABLE: Unused.
4	RW	INST1_SLOW_LFSR_MODE: Enable slow LFSR mode of front-end instance 1.
5	RW	INST2_SLOW_LFSR_MODE: Enable slow LFSR mode of front-end instance 2.
6	RW	INST3_SLOW_LFSR_MODE: Unused.
7	RW	INST4_SLOW_LFSR_MODE: Unused.
8:9	RW	INST1_CONDITION1_TRIG_SEL: Select instance 1 condition 1 for output (external) triggers. 00 = Do nothing. 01 = trigger_out(0). 10 = trigger_out(1). 11 = trigger_out(2).
10:11	RW	INST1_CONDITION2_TRIG_SEL: Select instance 1 condition 2 for output (external) triggers. 00 = Do nothing. 01 = trigger_out(0). 10 = trigger_out(1). 11 = trigger_out(2).
12:13	RW	INST1_C2_TIMEOUT_TRIG_SEL: Select instance 1 condition 2 time-out counter for output (external) triggers. 00 = Do nothing. 01 = trigger_out(0). 10 = trigger_out(1). 11 = trigger_out(2).
14:15	RW	INST2_CONDITION1_TRIG_SEL: Select instance 2 condition 1 for output (external) triggers. 00 = Do nothing. 01 = trigger_out(0). 10 = trigger_out(1). 11 = trigger_out(2).
16:17	RW	INST2_CONDITION2_TRIG_SEL: Select instance 2 condition 2 trigger for output (external) triggers. 00 = Do nothing. 01 = trigger_out(0). 10 = trigger_out(1). 11 = trigger_out(2).
18:19	RW	INST2_C2_TIMEOUT_TRIG_SEL: Select instance 2 condition 2 time-out counter for output (external) triggers. 00 = Do nothing. 01 = trigger_out(0). 10 = trigger_out(1). 11 = trigger_out(2).
20:31	RO	constant = 0b000000000000
32	RW	EXT_TRIG_ON_STOP: Enable trigger on stop.
33	RW	EXT_TRIG_ON_FREEZE: Enable trigger on freeze.
34:38	RW	CORE_RAS0_TRIG_SEL:

Bits	SCOM	Field Mnemonic: Description
39:43	RW	CORE_RAS1_TRIG_SEL:
44:45	RW	PC_TP_TRIG_SEL:
46:49	RW	DBG_ARM_SEL:
50:53	RW	TRIG0_LEVEL_SEL: Select additional conditions for output (external) trigger signal trigger_out(0). Note: Some are N/A (inst3/4 conditions are tied to zero). 0001 = inst1_cond3_state_int(1). 0010 = inst1_cond3_state_int(0). 0011 = inst2_cond3_state_int(1). 0100 = inst2_cond3_state_int(0). 0101 = inst3_cond3_state_int(1). 0110 = inst3_cond3_state_int(0). 0111 = inst4_cond3_state_int(1). 1000 = inst4_cond3_state_int(0). 1001 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1). 1010 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1). 1011 = inst3_cond3_state_int(1) or inst4_cond3_state_int(1). 1100 = inst3_cond3_state_int(1) and inst4_cond3_state_int(1). 1101 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1). 1110 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1) and inst3_cond3_state_int(1). 1111 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1) or inst4_cond3_state_int(1).
54:57	RW	TRIG1_LEVEL_SEL: Select additional conditions for output (external) trigger signal trigger_out(1). Note: Some are N/A (inst3/4 conditions are tied to zero). 0001 = inst1_cond3_state_int(1). 0010 = inst1_cond3_state_int(0). 0011 = inst2_cond3_state_int(1). 0100 = inst2_cond3_state_int(0). 0101 = inst3_cond3_state_int(1). 0110 = inst3_cond3_state_int(0). 0111 = inst4_cond3_state_int(1). 1000 = inst4_cond3_state_int(0). 1001 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1). 1010 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1). 1011 = inst3_cond3_state_int(1) or inst4_cond3_state_int(1). 1100 = inst3_cond3_state_int(1) and inst4_cond3_state_int(1). 1101 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1). 1110 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1) and inst3_cond3_state_int(1). 1111 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1) or inst4_cond3_state_int(1).
58:63	RO	constant = 0b000000

Register Name	Debug Trace 1 Register
Mnemonic	TP.TCEC14.CORE.EPS.DBG.DBG_TRACE_REG_1
Address	000000002E0107CE (SCOM)
Description	This is debug macro configuration register 1 for the back-end component.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	INST1_CONDITION1_ACTION_DO: Instance 1 action selection, condition 1: 00 = Nothing 01 = Start 10 = Stop 11 = RUNN. Start now, and stop after n cycles.

Bits	SCOM	Field Mnemonic: Description
2:3	RW	INST1_CONDITION2_ACTION_DO: Instance 1 action selection, condition 2: 00 = Nothing 01 = Start 10 = Stop 11 = RUNN. Start now, and stop after n cycles.
4:5	RW	INST1_C2_TIMEOUT_ACTION_DO: Instance 1 action selection, c2_timeout: 00 = Nothing 01 = Start 10 = Stop 11 = RUNN. Start now, and stop after n cycles.
6:7	RW	INST2_CONDITION1_ACTION_DO: Instance 2 action selection, condition 1: 00 = Nothing 01 = Start 10 = Stop 11 = RUNN. Start now, and stop after n cycles.
8:9	RW	INST2_CONDITION2_ACTION_DO: Instance 2 action selection, condition 2: 00 = Nothing 01 = Start 10 = Stop 11 = RUNN. Start now, and stop after n cycles.
10:11	RW	INST2_C2_TIMEOUT_ACTION_DO: Instance 2 action selection, c2_timeout: 00 = Nothing 01 = Start 10 = Stop 11 = RUNN. Start now, and stop after n cycles.
12:23	RO	constant = 0b000000000000
24	RW	INST1_CONDITION1_ACTION_WAITN: For WAITN.
25	RW	INST1_CONDITION2_ACTION_WAITN: For WAITN.
26	RW	INST1_C2_TIMEOUT_ACTION_WAITN: For WAITN.
27	RW	INST2_CONDITION1_ACTION_WAITN: For WAITN.
28	RW	INST2_CONDITION2_ACTION_WAITN: For WAITN.
29	RW	INST2_C2_TIMEOUT_ACTION_WAITN: For WAITN.
30:35	RO	constant = 0b000000
36	RW	INST1_CONDITION1_ACTION_BANK: Trace bank switch (inst1, condition1).
37	RW	INST1_CONDITION2_ACTION_BANK: Trace bank switch (inst1, condition2).
38	RW	INST1_C2_TIMEOUT_ACTION_BANK: Trace bank switch (inst1, c2_timeout).
39	RW	INST2_CONDITION1_ACTION_BANK: Trace bank switch (inst2, condition1).
40	RW	INST2_CONDITION2_ACTION_BANK: Trace bank switch (inst2, condition2).
41	RW	INST2_C2_TIMEOUT_ACTION_BANK: Trace bank switch (inst2, c2_timeout).
42:47	RO	constant = 0b000000
48:50	RW	INST1_CHECKSTOP_MODE_LT: Select additional condition with fir_error_lt for dbg_fir_xstop_on_trig output: 000 = inst1_condition1_lt. 001 = inst1_condition2_lt. 010 = inst1_condition3_lt. 011 = inst1_cond2_timeout_lt. 1XX = Disable checkstop_mode.

Bits	SCOM	Field Mnemonic: Description
51	RW	INST1_CHECKSTOP_MODE_SELECTOR: Enable_fir_trig_xstop; enable checkstop on debug trigger: 0 = Disable checkstop on debug trigger. 1 = Enable checkstop on debug trigger.
52:54	RW	INST2_CHECKSTOP_MODE_LT: Select additional condition with fir_error_lt for dbg_fir_xstop_on_trig output: 000 = inst2_condition1_lt. 001 = inst2_condition2_lt. 010 = inst2_condition3_lt. 011 = inst2_cond2_timeout_lt. 1XX = Disable checkstop mode.
55	RW	INST2_CHECKSTOP_MODE_SELECTOR: enable_fir_error_xstop; enable checkstop on FIR error: 0 = Disable checkstop on FIR error. 1 = Enable checkstop on FIR error.
56:63	RO	constant = 0b00000000

Register Name	Debug Trace Mode 2 Register
Mnemonic	TP.TCEC14.CORE.EPS.DBG.DBG_TRACE_MODE_REG_2
Address	000000002E0107CF (SCOM)
Description	This is debug macro configuration register 2 for the back-end component.

Bits	SCOM	Field Mnemonic: Description
0:15	RW	RUNN_COUNT_COMPARE_VALUE: Compare value for the RUNN counter used in trace modes RUNN and WAITN.
16	RW	IMM_FREEZE_MODE: Immediate freeze mode.
17	RW	STOP_ON_ERR: Stop and freeze on checkstop.
18	RW	BANK_ON_RUNN_MATCH: Bank switch on run match.
19	RW	FORCE_TEST_MODE: Force RUNN condition to be true.
20	RW	ACCUM_HIST_MODE: Accumulate history mode; do not clear history mode when trace_run active.
21	RW	FRZ_COUNT_ON_FRZ: Freeze condition counters on trace freeze.

Register Name	Debug Trace Control Register
Mnemonic	TP.TCEC14.CORE.EPS.DBG.DEBUG_TRACE_CONTROL
Address	000000002E0107D0 (SCOM)
Description	This is the trace start/stop/rest using SCOM command register. Use write data(0/1/2) = 1. This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0	WOX	Reserved field.
1	WOX	Reserved field.
2	WOX	Reserved field.

Register Name	Extra Trace Mode Register
Mnemonic	TP.TCEC14.CORE.EPS.DBG.XTRA_TRACE_MODE
Address	000000002E0107D1 (SCOM)
Description	This register provides an extra or dedicated trace mode register for core triggers.

Bits	SCOM	Field Mnemonic: Description
0:37	RW	XTRA_TRACE_MODE_DATA: Contents of the extra or dedicated trace mode register for core triggers.

Register Name	Hang Control Register
Mnemonic	EX07.EC.C0.PC.THRCTL.TCTLCOM.HANG_CONTROL
Address	000000002E010A00 (SCOM)
Description	Hang control register

Bits	SCOM	Field Mnemonic: Description
0:7	RW	CORE_HANG_LIMIT: Core hang limit. 3_hang_pulses => 0x9F (default). 5_hang_pulses => 0x27. 10_hang_pulses => 0xA1. 50_hang_pulsed => 0x99. 100_hang_pulses => 0x2D. 150_hang_pulses => 0xF6. 200_hang_pulses => 0x64.
8:15	RW	NEST_HANG_LIMIT: Nest hang limit. 20_hang_pulses => 0x5F. 50_hang_pulses => 0x99. 100_hang_pulses => 0x2D (default). 150_hang_pulses => 0xF6. 200_hang_pulses => 0x64.
16	RW	RETURN_GOOD_ON_COMP: Return good on completion without waiting for a hang_pulse.
17:24	RW	COMP_CNT_LIMIT: Completion count mode.
25:27	RW	HANG_REC_LIMIT: Hang record limit.
28	RW	USE_HANG_REC_LIMIT: Use hang record limit.
29:33	RW	ACTIVE_MASK: Active mask latch for hang condition enable/disable.
34:41	RW	Reserved field.
42:63	RO	constant = 0b0000000000000000000000

Register Name	HID Register
Mnemonic	EX07.EC.C0.PC.THRCTL.TCTLCOM.HID
Address	000000002E010A01 (SCOM)
Description	HID register

Bits	SCOM	Field Mnemonic: Description
0	RW	ONE_PPC: One PowerPC instruction is sent out of the iBUFFERs and decoded at a time.
1	RW	EN_INSTRUC_TRACE: Enable enhanced tracing (hardware instruction trace).
2	RW	FLUSH_IC: Flush the ICACHE directory and the IEADIR on a transition from 0 to 1.

Bits	SCOM	Field Mnemonic: Description
3	RW	EN_ATTN: Enable the support processor attention instruction.
4	RW	HILE: The contents of this bit are copied into the MSR[LE] by interrupts that set MSR[HV] = '1'.
5	RW	DIS_RECOVERY: Disable the processor recovery mechanism.
6	RW	MEGAMOUTH: Store ordering for adapters.
7	RW	PREFETCH_RESET: Reset the prefetch queues.
8	RW	LSU_SPARE: LSU spare.
9:63	RO	constant = 0b0000000000000000000000000000000000000000000000000000000

Register Name	RAS Status Register
Mnemonic	EX07.EC.C0.PC.THRCTL.TCTLCOM.RAS_STATUS
Address	000000002E010A02 (SCOM)
Description	RAS status register

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	Reserved field.
2	ROX	Reserved field.
3	ROX	Reserved field.
4	ROX	Reserved field.
5:7	RO	constant = 0b000
8	ROX	Reserved field.
9	ROX	Reserved field.
10	ROX	Reserved field.
11	ROX	Reserved field.
12	ROX	Reserved field.
13:15	RO	constant = 0b000
16	ROX	Reserved field.
17	ROX	Reserved field.
18	ROX	Reserved field.
19	ROX	Reserved field.
20	ROX	Reserved field.
21:23	RO	constant = 0b000
24	ROX	Reserved field.
25	ROX	Reserved field.
26	ROX	Reserved field.
27	ROX	Reserved field.
28	ROX	Reserved field.
29:63	RO	constant = 0b00000000000000000000000000000000000

Register Name	Thread Control Hold Out Register
Mnemonic	EX07.EC.C0.PC.THRCTL.TCTLCOM.THRCTL_HOLD_OUT
Address	000000002E010A03 (SCOM)
Description	Thread control error report hold out register

Bits	SCOM	Field Mnemonic: Description
0:49	ROX	Reserved.
50:63	RO	constant = 0b00000000000000

Register Name	Core Fault Isolation Register
Mnemonic	EX07.EC.C0.PC.FIR.CORE_FIR
Address	000000002E010A40 (SCOM) 000000002E010A41 (SCOM1) 000000002E010A42 (SCOM2)
Description	Core fault isolation register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	Reserved field.
1	RWX	WOX_AND	WOX_OR	Reserved field.
2	RWX	WOX_AND	WOX_OR	Reserved field.
3	RWX	WOX_AND	WOX_OR	Reserved field.
4	RWX	WOX_AND	WOX_OR	Reserved field.
5	RWX	WOX_AND	WOX_OR	Reserved field.
6	RWX	WOX_AND	WOX_OR	Reserved field.
7	RWX	WOX_AND	WOX_OR	Reserved field.
8	RWX	WOX_AND	WOX_OR	Reserved field.
9	RWX	WOX_AND	WOX_OR	Reserved field.
10	RWX	WOX_AND	WOX_OR	Reserved field.
11	RWX	WOX_AND	WOX_OR	Reserved field.
12	RWX	WOX_AND	WOX_OR	Reserved field.
13	RWX	WOX_AND	WOX_OR	Reserved field.
14	RWX	WOX_AND	WOX_OR	Reserved field.
15	RWX	WOX_AND	WOX_OR	Reserved field.
16	RWX	WOX_AND	WOX_OR	Reserved field.
17	RWX	WOX_AND	WOX_OR	Reserved field.
18	RWX	WOX_AND	WOX_OR	Reserved field.
19	RWX	WOX_AND	WOX_OR	Reserved field.
20	RWX	WOX_AND	WOX_OR	Reserved field.
21	RWX	WOX_AND	WOX_OR	Reserved field.
22	RWX	WOX_AND	WOX_OR	Reserved field.
23	RWX	WOX_AND	WOX_OR	Reserved field.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
24	RWX	WOX_AND	WOX_OR	Reserved field.
25	RWX	WOX_AND	WOX_OR	Reserved field.
26	RWX	WOX_AND	WOX_OR	Reserved field.
27	RWX	WOX_AND	WOX_OR	Reserved field.
28	RWX	WOX_AND	WOX_OR	Reserved field.
29	RWX	WOX_AND	WOX_OR	Reserved field.
30	RWX	WOX_AND	WOX_OR	Reserved field.
31	RWX	WOX_AND	WOX_OR	Reserved field.
32	RWX	WOX_AND	WOX_OR	Reserved field.
33	RWX	WOX_AND	WOX_OR	Reserved field.
34	RWX	WOX_AND	WOX_OR	Reserved field.
35	RWX	WOX_AND	WOX_OR	Reserved field.
36	RWX	WOX_AND	WOX_OR	Reserved field.
37	RWX	WOX_AND	WOX_OR	Reserved field.
38	RWX	WOX_AND	WOX_OR	Reserved field.
39	RWX	WOX_AND	WOX_OR	Reserved field.
40	RWX	WOX_AND	WOX_OR	Reserved field.
41	RWX	WOX_AND	WOX_OR	Reserved field.
42	RWX	WOX_AND	WOX_OR	Reserved field.
43	RWX	WOX_AND	WOX_OR	Reserved field.
44	RWX	WOX_AND	WOX_OR	Reserved field.
45	RWX	WOX_AND	WOX_OR	Reserved field.
46	RWX	WOX_AND	WOX_OR	Reserved field.
47	RWX	WOX_AND	WOX_OR	Reserved field.
48	RWX	WOX_AND	WOX_OR	Reserved field.
49	RWX	WOX_AND	WOX_OR	Reserved field.
50	RWX	WOX_AND	WOX_OR	Reserved field.
51	RWX	WOX_AND	WOX_OR	Reserved field.
52	RWX	WOX_AND	WOX_OR	Reserved field.
53	RWX	WOX_AND	WOX_OR	Reserved field.
54	RWX	WOX_AND	WOX_OR	Reserved field.
55	RWX	WOX_AND	WOX_OR	Reserved field.
56	RWX	WOX_AND	WOX_OR	Reserved field.
57	RWX	WOX_AND	WOX_OR	Reserved field.
58	RWX	WOX_AND	WOX_OR	Reserved field.
59	RWX	WOX_AND	WOX_OR	Reserved field.
60	RWX	WOX_AND	WOX_OR	Reserved field.
61	RWX	WOX_AND	WOX_OR	Reserved field.
62	RWX	WOX_AND	WOX_OR	Reserved field.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
63	RWX	WOX_AND	WOX_OR	Reserved field.

Register Name	Core FIR Mask Register
Mnemonic	EX07.EC.C0.PC.FIR.CORE_FIRMASK
Address	000000002E010A43 (SCOM) 000000002E010A44 (SCOM1) 000000002E010A45 (SCOM2)
Description	Core FIR mask register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	MASK_IF_SRAM_REC_ERROR: IFU SRAM recoverable error (ICACHE parity error, and so on).
1	RW	WO_AND	WO_OR	MASK_TC_FIR_XSTOP_ERROR: TC checkstop.
2	RW	WO_AND	WO_OR	MASK_IF_RFILE_REC_ERROR: IFU register file recoverable error.
3	RW	WO_AND	WO_OR	MASK_IF_RFILE_XSTOP_ERROR: IFU register file core checkstop.
4	RW	WO_AND	WO_OR	MASK_IF_LOG_REC_ERROR: IFU logic recoverable error.
5	RW	WO_AND	WO_OR	MASK_IF_LOG_XSTOP_ERROR: IFU logic core checkstop.
6	RW	WO_AND	WO_OR	MASK_UNUSED_6: Reserved.
7	RW	WO_AND	WO_OR	MASK_UNUSED_7: Reserved.
8	RW	WO_AND	WO_OR	MASK_PC_RECOV_XSTOP_ERROR: Recovery core checkstop.
9	RW	WO_AND	WO_OR	MASK_SD_RFILE_REC_ERROR: ISU register file recoverable error (GPR/VRF).
10	RW	WO_AND	WO_OR	MASK_SD_RFILE_XSTOP_ERROR: ISU register file core checkstop (mapper error).
11	RW	WO_AND	WO_OR	MASK_SD_LOG_REC_ERROR: ISU logic recoverable error.
12	RW	WO_AND	WO_OR	MASK_SD_LOG_XSTOP_ERROR: ISU logic core checkstop.
13	RW	WO_AND	WO_OR	MASK_SD_NOT_MT_CI_REC_ERROR: ISU recoverable if not in an MT window.
14	RW	WO_AND	WO_OR	MASK_SD_MCHK_AND_ME_EQ_0_ERROR: MCHK received while ME = 0; not recoverable.
15	RW	WO_AND	WO_OR	MASK_SD_L2_UE_ERROR: UE from L2.
16	RW	WO_AND	WO_OR	MASK_SD_L2_UE_OVER_THRES_ERROR: Number of UEs from L2 above the threshold.
17	RW	WO_AND	WO_OR	MASK_SD_CI_UE_ERROR: UE on CI load.
18	RW	WO_AND	WO_OR	MASK_UNUSED_18: Reserved.
19	RW	WO_AND	WO_OR	MASK_UNUSED_19: Reserved.
20	RW	WO_AND	WO_OR	MASK_SD_SYS_XSTOP_ERROR: ISU system checkstop (MSR corrupted).
21	RW	WO_AND	WO_OR	MASK_UNUSED_21: Reserved.
22	RW	WO_AND	WO_OR	MASK_UNUSED_22: Reserved.
23	RW	WO_AND	WO_OR	MASK_UNUSED_23: Reserved.
24	RW	WO_AND	WO_OR	MASK_VS_LOG_REC_ERROR: VSU logic recoverable error.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
25	RW	WO_AND	WO_OR	MASK_VS_LOG_XSTOP_ERROR: VSU logic core checkstop.
26	RW	WO_AND	WO_OR	MASK_PC_RECOV_IN_MAINT_ERROR: Thread in maintenance mode and receives recovery request.
27	RW	WO_AND	WO_OR	MASK_VS_DU_LOG_REC_ERROR: VSU DFU logic recoverable error.
28	RW	WO_AND	WO_OR	MASK_PC_SYS_XSTOP_ERROR: PC system checkstop; recoverable error received when recovery is disabled.
29	RW	WO_AND	WO_OR	MASK_LS_SRAM_PARITY_ERROR: LSU SRAM recoverable error (DCACHE parity error, ERAT parity error, TLB parity error, SLB parity error, and so on).
30	RW	WO_AND	WO_OR	MASK_LS_SETDELETE_ERROR: LSU set deleted.
31	RW	WO_AND	WO_OR	MASK_LS_RFILE_REC_ERROR: LSU register file recoverable error.
32	RW	WO_AND	WO_OR	MASK_LS_RFILE_XSTOP_ERROR: LSU register file core checkstop.
33	RW	WO_AND	WO_OR	MASK_LS_TLB_MULTIHIT_ERROR: LSU TLB multiple hit error occurred.
34	RW	WO_AND	WO_OR	MASK_LS_SLB_MULTIHIT_ERROR: LSU SLB multiple hit error occurred.
35	RW	WO_AND	WO_OR	MASK_LS_DERAT_MULTIHIT_ERROR: LSU ERAT multiple hit error occurred.
36	RW	WO_AND	WO_OR	MASK_PC_FWD_PROGRESS_ERROR: PC forward progress error.
37	RW	WO_AND	WO_OR	MASK_LS_LOG_REC_ERROR: LSU logic recoverable error.
38	RW	WO_AND	WO_OR	MASK_LS_LOG_XSTOP_ERROR: LSU logic core checkstop.
39	RW	WO_AND	WO_OR	MASK_LS_NOT_MT_REC_ERROR: LSU recoverable if not in an MT window.
40	RW	WO_AND	WO_OR	MASK_UNUSED_40: Reserved.
41	RW	WO_AND	WO_OR	MASK_LS_SYS_XSTOP_ERROR: LSU system checkstop.
42	RW	WO_AND	WO_OR	MASK_UNUSED_42: Reserved.
43	RW	WO_AND	WO_OR	MASK_PC_THREAD_HANG_REC_ERROR: PC thread hang recoverable error.
44	RW	WO_AND	WO_OR	MASK_UNUSED_44: Reserved.
45	RW	WO_AND	WO_OR	MASK_PC_LOG_XSTOP_ERROR: PC logic checkstop.
46	RW	WO_AND	WO_OR	MASK_UNUSED_46: Reserved.
47	RW	WO_AND	WO_OR	MASK_PC_TFAC_XSTOP_ERROR: PC Timebase facility checkstop.
48	RW	WO_AND	WO_OR	MASK_PC_HYP_RES_ERROR: Hypervisor resource error.
49	RW	WO_AND	WO_OR	MASK_UNUSED_49: Reserved.
50	RW	WO_AND	WO_OR	MASK_UNUSED_50: Reserved.
51	RW	WO_AND	WO_OR	MASK_UNUSED_51: Reserved.
52	RW	WO_AND	WO_OR	MASK_PC_HANG_RECOVERY_FAILED: Hang recovery failed.
53	RW	WO_AND	WO_OR	MASK_PC_CORE_HANG_DETECT_ERROR: Core hang detected.
54	RW	WO_AND	WO_OR	MASK_UNUSED_54: Reserved.
55	RW	WO_AND	WO_OR	MASK_PC_NEST_HANG_DETECT_ERROR: Nest hang detected.
56	RW	WO_AND	WO_OR	MASK_PC_OTHER_CORE_CHIPLET_REC_ERROR: Other core chiplet recoverable error.
57	RW	WO_AND	WO_OR	MASK_PC_OTHER_CORE_CHIPLET_XSTOP_ERROR: Other core chiplet core checkstop.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
58	RW	WO_AND	WO_OR	MASK_PC_OTHER_CORE_CHIPLET_SYS_XSTOP_ERROR: Other core chiplet system checkstop.
59	RW	WO_AND	WO_OR	MASK_PC_SCOM_ERROR: SCOM satellite error detected.
60	RW	WO_AND	WO_OR	MASK_PC_XSTOP_ON_DBG_TRIGGER_ERROR: Debug trigger error inject.
61	RW	WO_AND	WO_OR	MASK_PC_FW_INJ_REC_ERROR: SCOM or firmware recoverable error inject.
62	RW	WO_AND	WO_OR	MASK_PC_FW_INJ_XSTOP_ERROR: Firmware checkstop error inject.
63	RW	WO_AND	WO_OR	MASK_PC_PHYP_XSTOP_ERROR: Hypervisor checkstop via SPRC/SPRD.

Register Name	Core FIR Action 0 Register
Mnemonic	EX07.EC.C0.PC.FIR.CORE_ACTION0
Address	000000002E010A46 (SCOM)
Description	Core FIR Action 0 Register

Bits	SCOM	Field Mnemonic: Description
0	RW	ACTION_IF_SRAM_REC_ERROR: IFU SRAM recoverable error (ICACHE parity error, and so on).
1	RW	ACTION_TC_FIR_XSTOP_ERROR: TC checkstop.
2	RW	ACTION_IF_RFILE_REC_ERROR: IFU register file recoverable error.
3	RW	ACTION_IF_RFILE_XSTOP_ERROR: IFU register file core checkstop.
4	RW	ACTION_IF_LOG_REC_ERROR: IFU logic recoverable error.
5	RW	ACTION_IF_LOG_XSTOP_ERROR: IFU logic core checkstop.
6	RW	ACTION_UNUSED_6: Reserved.
7	RW	ACTION_UNUSED_7: Reserved.
8	RW	ACTION_PC_RECOV_XSTOP_ERROR: Recovery core checkstop.
9	RW	ACTION_SD_RFILE_REC_ERROR: ISU register file recoverable error (GPR/VRF).
10	RW	ACTION_SD_RFILE_XSTOP_ERROR: ISU register file core checkstop (mapper error).
11	RW	ACTION_SD_LOG_REC_ERROR: ISU logic recoverable error.
12	RW	ACTION_SD_LOG_XSTOP_ERROR: ISU logic core checkstop.
13	RW	ACTION_SD_NOT_MT_CI_REC_ERROR: ISU recoverable if not in MT window.
14	RW	ACTION_SD_MCHK_AND_ME_EQ_0_ERROR: MCHK received while ME = 0, nonrecoverable.
15	RW	ACTION_SD_L2_UE_ERROR: UE from L2.
16	RW	ACTION_SD_L2_UE_OVER_THRES_ERROR: Number of UEs from L2 above the threshold.
17	RW	ACTION_SD_CI_UE_ERROR: UE on CI load.
18	RW	ACTION_UNUSED_18: Reserved.
19	RW	ACTION_UNUSED_19: Reserved.
20	RW	ACTION_SD_SYS_XSTOP_ERROR: ISU system checkstop (MSR corrupted).
21	RW	ACTION_UNUSED_21: Reserved.
22	RW	ACTION_UNUSED_22: Reserved.
23	RW	ACTION_UNUSED_23: Reserved.

Bits	SCOM	Field Mnemonic: Description
24	RW	ACTION_VS_LOG_REC_ERROR: VSU logic recoverable error.
25	RW	ACTION_VS_LOG_XSTOP_ERROR: VSU logic core checkstop.
26	RW	ACTION_PC_RECOV_IN_MAINT_ERROR: Thread in maintenance mode and receives recovery request.
27	RW	ACTION_VS_DU_LOG_REC_ERROR: VSU DFU logic recoverable error.
28	RW	ACTION_PC_SYS_XSTOP_ERROR: PC system checkstop. Recoverable error received when recovery was disabled.
29	RW	ACTION_LS_SRAM_PARITY_ERROR: LSU SRAM recoverable error (DCACHE parity error, ERAT parity error, TLB parity error, SLB parity error, and so on).
30	RW	ACTION_LS_SETDELETE_ERROR: LSU set deleted.
31	RW	ACTION_LS_RFILE_REC_ERROR: LSU register file recoverable error.
32	RW	ACTION_LS_RFILE_XSTOP_ERROR: LSU register file core checkstop.
33	RW	ACTION_LS_TLB_MULTIHIT_ERROR: LSU TLB multiple-hit error occurred.
34	RW	ACTION_LS_SLB_MULTIHIT_ERROR: LSU SLB multiple-hit error occurred.
35	RW	ACTION_LS_DERAT_MULTIHIT_ERROR: LSU ERAT multiple-hit error occurred.
36	RW	ACTION_PC_FWD_PROGRESS_ERROR: PC forward progress error.
37	RW	ACTION_LS_LOG_REC_ERROR: LSU logic recoverable error.
38	RW	ACTION_LS_LOG_XSTOP_ERROR: LSU logic core checkstop.
39	RW	ACTION_LS_NOT_MT_REC_ERROR: LSU recoverable if not in MT window.
40	RW	ACTION_UNUSED_40: Reserved.
41	RW	ACTION_LS_SYS_XSTOP_ERROR: LSU system checkstop.
42	RW	ACTION_UNUSED_42: Reserved.
43	RW	ACTION_PC_THREAD_HANG_REC_ERROR: PC thread hang recoverable error.
44	RW	ACTION_UNUSED_44: Reserved.
45	RW	ACTION_PC_LOG_XSTOP_ERROR: PC logic checkstop.
46	RW	ACTION_UNUSED_46: Reserved.
47	RW	ACTION_PC_TFAC_XSTOP_ERROR: PC Timebase facility checkstop.
48	RW	ACTION_PC_HYP_RES_ERROR: Hypervisor resource error.
49	RW	ACTION_UNUSED_49: Reserved.
50	RW	ACTION_UNUSED_50: Reserved.
51	RW	ACTION_UNUSED_51: Reserved.
52	RW	ACTION_PC_HANG_RECOVERY_FAILED: Hang recovery failed.
53	RW	ACTION_PC_CORE_HANG_DETECT_ERROR: Core hang detected.
54	RW	ACTION_UNUSED_54: Reserved.
55	RW	ACTION_PC_NEST_HANG_DETECT_ERROR: Nest hang detected.
56	RW	ACTION_PC_OTHER_CORE_CHIPLET_REC_ERROR: Other core chiplet recoverable error.
57	RW	ACTION_PC_OTHER_CORE_CHIPLET_XSTOP_ERROR: Other core chiplet core checkstop.
58	RW	ACTION_PC_OTHER_CORE_CHIPLET_SYS_XSTOP_ERROR: Other core chiplet system checkstop.
59	RW	ACTION_PC_SCOM_ERROR: SCOM satellite error detected.
60	RW	ACTION_PC_XSTOP_ON_DBG_TRIGGER_ERROR: Debug trigger error inject.
61	RW	ACTION_PC_FW_INJ_REC_ERROR: SCOM or firmware recoverable error inject.

Bits	SCOM	Field Mnemonic: Description
62	RW	ACTION_PC_FW_INJ_XSTOP_ERROR: Firmware checkstop error inject.
63	RW	ACTION_PC_PHYP_XSTOP_ERROR: Hypervisor checkstop via SPRC/SPRD.

Register Name	Core FIR Action 1 Register
Mnemonic	EX07.EC.C0.PC.FIR.CORE_ACTION1
Address	000000002E010A47 (SCOM)
Description	Core FIR Action 1 Register

Bits	SCOM	Field Mnemonic: Description
0	RW	ACTION_IF_SRAM_REC_ERROR: IFU SRAM recoverable error (ICACHE parity error, and so on).
1	RW	ACTION_TC_FIR_XSTOP_ERROR: TC checkstop.
2	RW	ACTION_IF_RFILE_REC_ERROR: IFU register file recoverable error.
3	RW	ACTION_IF_RFILE_XSTOP_ERROR: IFU register file core checkstop.
4	RW	ACTION_IF_LOG_REC_ERROR: IFU logic recoverable error.
5	RW	ACTION_IF_LOG_XSTOP_ERROR: IFU logic core checkstop.
6	RW	ACTION_UNUSED_6: Reserved.
7	RW	ACTION_UNUSED_7: Reserved.
8	RW	ACTION_PC_RECOV_XSTOP_ERROR: Recovery core checkstop.
9	RW	ACTION_SD_RFILE_REC_ERROR: ISU register file recoverable error (GPR/VRF).
10	RW	ACTION_SD_RFILE_XSTOP_ERROR: ISU register file core checkstop (mapper error).
11	RW	ACTION_SD_LOG_REC_ERROR: ISU logic recoverable error.
12	RW	ACTION_SD_LOG_XSTOP_ERROR: ISU logic core checkstop.
13	RW	ACTION_SD_NOT_MT_CI_REC_ERROR: ISU recoverable if not in an MT window.
14	RW	ACTION_SD_MCHK_AND_ME_EQ_0_ERROR: MCHK received while ME = 0, nonrecoverable.
15	RW	ACTION_SD_L2_UE_ERROR: UE from L2.
16	RW	ACTION_SD_L2_UE_OVER_THRES_ERROR: Number of UEs from L2 above the threshold.
17	RW	ACTION_SD_CI_UE_ERROR: UE on CI load.
18	RW	ACTION_UNUSED_18: Reserved.
19	RW	ACTION_UNUSED_19: Reserved.
20	RW	ACTION_SD_SYS_XSTOP_ERROR: ISU system checkstop (MSR corrupted).
21	RW	ACTION_UNUSED_21: Reserved.
22	RW	ACTION_UNUSED_22: Reserved.
23	RW	ACTION_UNUSED_23: Reserved.
24	RW	ACTION_VS_LOG_REC_ERROR: VSU logic recoverable error.
25	RW	ACTION_VS_LOG_XSTOP_ERROR: VSU logic core checkstop.
26	RW	ACTION_PC_RECOV_IN_MAINT_ERROR: Thread in maintenance mode receives recovery request.
27	RW	ACTION_VS_DU_LOG_REC_ERROR: VSU DFU logic recoverable error.
28	RW	ACTION_PC_SYS_XSTOP_ERROR: PC system checkstop. Recoverable error received when recovery was disabled.

Bits	SCOM	Field Mnemonic: Description
29	RW	ACTION_LS_SRAM_PARITY_ERROR: LSU SRAM recoverable error (DCACHE parity error, ERAT parity error, TLB parity error, SLB parity error, and so on).
30	RW	ACTION_LS_SETDELETE_ERROR: LSU set deleted.
31	RW	ACTION_LS_RFILE_REC_ERROR: LSU register file recoverable error.
32	RW	ACTION_LS_RFILE_XSTOP_ERROR: LSU register file core checkstop.
33	RW	ACTION_LS_TLB_MULTIHIT_ERROR: LSU TLB multiple-hit error occurred.
34	RW	ACTION_LS_SLB_MULTIHIT_ERROR: LSU SLB multiple-hit error occurred.
35	RW	ACTION_LS_DERAT_MULTIHIT_ERROR: LSU ERAT multiple-hit error occurred.
36	RW	ACTION_PC_FWD_PROGRESS_ERROR: PC forward progress error.
37	RW	ACTION_LS_LOG_REC_ERROR: LSU logic recoverable error.
38	RW	ACTION_LS_LOG_XSTOP_ERROR: LSU logic core checkstop.
39	RW	ACTION_LS_NOT_MT_REC_ERROR: LSU recoverable if not in MT window.
40	RW	ACTION_UNUSED_40: Reserved.
41	RW	ACTION_LS_SYS_XSTOP_ERROR: LSU system checkstop.
42	RW	ACTION_UNUSED_42: Reserved.
43	RW	ACTION_PC_THREAD_HANG_REC_ERROR: PC thread hang recoverable error.
44	RW	ACTION_UNUSED_44: Reserved.
45	RW	ACTION_PC_LOG_XSTOP_ERROR: PC logic checkstop.
46	RW	ACTION_UNUSED_46: Reserved.
47	RW	ACTION_PC_TFAC_XSTOP_ERROR: PC Timebase facility checkstop.
48	RW	ACTION_PC_HYP_RES_ERROR: Hypervisor resource error.
49	RW	ACTION_UNUSED_49: Reserved.
50	RW	ACTION_UNUSED_50: Reserved.
51	RW	ACTION_UNUSED_51: Reserved.
52	RW	ACTION_PC_HANG_RECOVERY_FAILED: Hang recovery failed.
53	RW	ACTION_PC_CORE_HANG_DETECT_ERROR: Core hang detected.
54	RW	ACTION_UNUSED_54: Reserved.
55	RW	ACTION_PC_NEST_HANG_DETECT_ERROR: Nest hang detected.
56	RW	ACTION_PC_OTHER_CORE_CHIPLET_REC_ERROR: Other core chiplet recoverable error.
57	RW	ACTION_PC_OTHER_CORE_CHIPLET_XSTOP_ERROR: Other core chiplet core checkstop.
58	RW	ACTION_PC_OTHER_CORE_CHIPLET_SYS_XSTOP_ERROR: Other core chiplet system checkstop.
59	RW	ACTION_PC_SCOM_ERROR: SCOM satellite error detected.
60	RW	ACTION_PC_XSTOP_ON_DBG_TRIGGER_ERROR: Debug trigger error inject.
61	RW	ACTION_PC_FW_INJ_REC_ERROR: SCOM or firmware recoverable error inject.
62	RW	ACTION_PC_FW_INJ_XSTOP_ERROR: Firmware checkstop error inject.
63	RW	ACTION_PC_PHYP_XSTOP_ERROR: Hypervisor checkstop via SPRC/SPRD.

Register Name	Core Who's on First Register
Mnemonic	EX07.EC.C0.PC.FIR.CORE_WOF
Address	000000002E010A48 (SCOM)
Description	Who's-on-first register

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	Reserved field.
1	RWX_WCLRREG	Reserved field.
2	RWX_WCLRREG	Reserved field.
3	RWX_WCLRREG	Reserved field.
4	RWX_WCLRREG	Reserved field.
5	RWX_WCLRREG	Reserved field.
6	RWX_WCLRREG	Reserved field.
7	RWX_WCLRREG	Reserved field.
8	RWX_WCLRREG	Reserved field.
9	RWX_WCLRREG	Reserved field.
10	RWX_WCLRREG	Reserved field.
11	RWX_WCLRREG	Reserved field.
12	RWX_WCLRREG	Reserved field.
13	RWX_WCLRREG	Reserved field.
14	RWX_WCLRREG	Reserved field.
15	RWX_WCLRREG	Reserved field.
16	RWX_WCLRREG	Reserved field.
17	RWX_WCLRREG	Reserved field.
18	RWX_WCLRREG	Reserved field.
19	RWX_WCLRREG	Reserved field.
20	RWX_WCLRREG	Reserved field.
21	RWX_WCLRREG	Reserved field.
22	RWX_WCLRREG	Reserved field.
23	RWX_WCLRREG	Reserved field.
24	RWX_WCLRREG	Reserved field.
25	RWX_WCLRREG	Reserved field.
26	RWX_WCLRREG	Reserved field.
27	RWX_WCLRREG	Reserved field.
28	RWX_WCLRREG	Reserved field.
29	RWX_WCLRREG	Reserved field.
30	RWX_WCLRREG	Reserved field.
31	RWX_WCLRREG	Reserved field.
32	RWX_WCLRREG	Reserved field.
33	RWX_WCLRREG	Reserved field.

Bits	SCOM	Field Mnemonic: Description
34	RWX_WCLRREG	Reserved field.
35	RWX_WCLRREG	Reserved field.
36	RWX_WCLRREG	Reserved field.
37	RWX_WCLRREG	Reserved field.
38	RWX_WCLRREG	Reserved field.
39	RWX_WCLRREG	Reserved field.
40	RWX_WCLRREG	Reserved field.
41	RWX_WCLRREG	Reserved field.
42	RWX_WCLRREG	Reserved field.
43	RWX_WCLRREG	Reserved field.
44	RWX_WCLRREG	Reserved field.
45	RWX_WCLRREG	Reserved field.
46	RWX_WCLRREG	Reserved field.
47	RWX_WCLRREG	Reserved field.
48	RWX_WCLRREG	Reserved field.
49	RWX_WCLRREG	Reserved field.
50	RWX_WCLRREG	Reserved field.
51	RWX_WCLRREG	Reserved field.
52	RWX_WCLRREG	Reserved field.
53	RWX_WCLRREG	Reserved field.
54	RWX_WCLRREG	Reserved field.
55	RWX_WCLRREG	Reserved field.
56	RWX_WCLRREG	Reserved field.
57	RWX_WCLRREG	Reserved field.
58	RWX_WCLRREG	Reserved field.
59	RWX_WCLRREG	Reserved field.
60	RWX_WCLRREG	Reserved field.
61	RWX_WCLRREG	Reserved field.
62	RWX_WCLRREG	Reserved field.
63	RWX_WCLRREG	Reserved field.

Register Name	Reset Keeper Register
Mnemonic	EX07.EC.C0.PC.FIR.RESET_KEEPER
Address	000000002E010A4A (SCOM)
Description	Resets the error hold latches on the error report macros.

Bits	SCOM	Field Mnemonic: Description
0	WOX_1P	Reserved field.
1:63	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000000

Register Name	Recovery Forward Progress Control Register
Mnemonic	EX07.EC.C0.PC.FIR.RECOV_FWD_PROG_CTRL
Address	000000002E010A4B (SCOM)
Description	Recovery forward progress control

Bits	SCOM	Field Mnemonic: Description
0	RW	Reserved field.
1:3	RW	Reserved field.
4:63	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000

Register Name	Recovery Threshold Register
Mnemonic	EX07.EC.C0.PC.FIR.RECOV_THOLD
Address	000000002E010A4C (SCOM)
Description	Recovery threshold

Bits	SCOM	Field Mnemonic: Description
0:7	RW	Reserved field.
8:9	RW	THRESHOLD_RESET: 00 = Disable 01 = Reset after one hang pulse 10 = Reset after two hang pulses
10:63	RO	constant = 0b000000000000000000000000000000000000000000000000000000

Register Name	FIR Error Injection Register
Mnemonic	EX07.EC.C0.PC.FIR.FIR_ERR_INJ
Address	000000002E010A4D (SCOM)
Description	Error injection control register

Bits	SCOM	Field Mnemonic: Description
0	RW	ERR_INJ_TO_LSU: Error injection to the LSU.
1	RW	ERR_INJ_TO_IFU: Error injection to the IFU.
2	RW	ERR_INJ_TO_ISU: Error injection to the ISU.
3	RW	ERR_INJ_TO_VSU: Error injection to the VSU.
4	RW	ERR_INJ_TO_PC: Error injection to the PC.
5	RW	Reserved field.
6	RW	ERROR_PULSE_OR_LEVEL: 0 = Injections is a pulse. 1 = Injection is a level.
7	RW	CLEAR_STICKY_LEVEL: Clear sticky latch used for level.
8	RW	ERR_INJ_SCOM_WRITE: SCOM write.
9	RW	ERR_INJ_TRIGGER: Trigger 0.

Bits	SCOM	Field Mnemonic: Description
10	RW	ERR_INJ_TRIGGER1: Trigger 1.
11	RW	ERR_INJ_TOD_TAP: TOD-tap.
12:13	RW	ERR_INJ_BLOCK: Block select 00 = Disable block by HV mode. 01 = Block if any thread is in HV mode. 10 = Block if all threads are in HV mode.
14	RW	ERR_INJ_DELAY_AFTER_BLOCK: Injection is delayed for 32 cycles after a block.
15	RW	ERR_INJ_RECOVERY_BLK: Injection is blocked while recovery is active.
16	RW	ERR_INJ_RECOVERY_BLK_EXTEND: Extend recovery block until there is forward progress.
17:20	RW	ERR_INJ_TAP_SEL: Tap select: 0000 => .5 ms. 0001 => 1.0 ms. 0010 => 2.0 ms. 0011 => 4.1 ms. 0100 => 8.2 ms. 0101 => 16.4 ms. 0110 => 32.8 ms. 0111 => 65.5 ms. 1000 => 131.0 ms. 1001 => 262.1 ms. 1010 => 524.3 ms. 1011 => 1.0 s. 1100 => 2.0 s. 1101 => 4.2 s. 1110 => 8.4 s. 1111 => 16.8 s.
21:23	RW	ERR_INJ_HYP_BLOCK: 0xx => Ignore HV and PR bits. 1HP => Block inject if MSR(HV) = H and MSR(PR) = P for any active thread.
24:63	RO	constant = 0b0000000000000000000000000000000000000000

Register Name	RAM Mode Register
Mnemonic	EX07.EC.C0.PC.FIR.RAM_MODEREG
Address	000000002E010A4E (SCOM)
Description	RAM instruction mode register

Bits	SCOM	Field Mnemonic: Description
0	RWX	RAM_MODE_ENABLE: RAM mode enable.
1:63	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000000

Register Name	FIR RAM Control Register
Mnemonic	EX07.EC.C0.PC.FIR.RAM_CTRL
Address	000000002E010A4F (SCOM)
Description	RAM instruction control register

Bits	SCOM	Field Mnemonic: Description
0:1	RWX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
2:5	RWX	Reserved field.
6:7	RWX	Reserved field.
8:39	RWX	Reserved field.
40:63	RO	constant = 0b000000000000000000000000

Register Name	**RAM Status Register**
Mnemonic	EX07.EC.C0.PC.FIR.RAM_STATUS
Address	000000002E010A50 (SCOM)
Description	RAM instruction status register

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	Reserved field.
2	ROX	Reserved field.
3	ROX	Reserved field.
4:63	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000

Register Name	**FIR Hold Out Register**
Mnemonic	EX07.EC.C0.PC.FIR.FIR_HOLD_OUT
Address	000000002E010A51 (SCOM)
Description	FIR/RECOV error report hold out register

Bits	SCOM	Field Mnemonic: Description
0:21	ROX	Reserved.
22:63	RO	constant = 0b000000000000000000000000000000000000000000

Register Name	**SCOM Control Register**
Mnemonic	EX07.EC.CC.PCC0.COMMON.SPR_COMMON.SCOMC
Address	000000002E010A80 (SCOM)
Description	SCOM control register

Bits	SCOM	Field Mnemonic: Description
0:53	RO	constant = 0b000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
54:60	RW	MODE_CX_SCOMC: 0000xxx = SCRATCH xx SPR. 0001xxx = TFMR xx SPR. 0010xxx = PURR xx SPR. 0011xxx = SPURR xx SPR. 0100xxx = DEC xx SPR. 0111000 = SPR_MODE. 0111001 = AVP output pin. 0111010 = Core checkstop request. 0111011 = SPATTN SPR. 0111100 = Core thread state. 1xxxxxx = Emmpath counters.
61:63	RO	constant = 0b000

Register Name	**OCC SCOM Control Register**
Mnemonic	EX07.EC.CC.PCC0.COMMON.SPR_COMMON.OCC_SCOMC
Address	000000002E010A82 (SCOM)
Description	OCC SCOM Control Register

Bits	SCOM	Field Mnemonic: Description
0:53	RO	constant = 0b000000000000000000000000000000000000000000000000000000
54:60	RW	MODE_CX_OCC_SCOMC: 1xxxxxx = Emmpath counters.
61:63	RO	constant = 0b000

Register Name	**SPR Mode Register**
Mnemonic	EX07.EC.CC.PCC0.COMMON.SPR_COMMON.SPR_MODE
Address	000000002E010A84 (SCOM)
Description	SPR_MODE register

Bits	SCOM	Field Mnemonic: Description
0:9	RO	constant = 0b0000000000
10:15	WO_1P	SPR_MODEREG_TFAC_ERR_INJ: Timebase facility error inject.
16:19	RO	constant = 0b0000
20	RW	SPR_MODEREG_SPRC_LT0_SEL: Allows SCOMC write of bits 54:60 of logical T0 SPRC.
21	RW	SPR_MODEREG_SPRC_LT1_SEL: Allows SCOMC write of bits 54:60 of logical T1 SPRC.
22	RW	SPR_MODEREG_SPRC_LT2_SEL: Allows SCOMC write of bits 54:60 of logical T2 SPRC.
23	RW	SPR_MODEREG_SPRC_LT3_SEL: Allows SCOMC write of bits 54:60 of logical T3 SPRC.
24	RW	SPR_MODEREG_SPRC_LT4_SEL: Allows SCOMC write of bits 54:60 of logical T4 SPRC.
25	RW	SPR_MODEREG_SPRC_LT5_SEL: Allows SCOMC write of bits 54:60 of logical T5 SPRC.
26	RW	SPR_MODEREG_SPRC_LT6_SEL: Allows SCOMC write of bits 54:60 of logical T6 SPRC.
27	RW	SPR_MODEREG_SPRC_LT7_SEL: Allows SCOMC write of bits 54:60 of logical T7 SPRC.
28:63	RO	constant = 0b000000000000000000000000000000000000

Register Name	Control Register	
Mnemonic	EX07.EC.CC.PCC0.COMMON.SPR_COMMON.CTRL	
Address	000000002E010A85 (SCOM)	
Description	Control register	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b000000000000000000000000000000000000000000000000
48	ROX	CTRL_T0_RUN_Q: Logical thread 0 run latch.
49	ROX	CTRL_T1_RUN_Q: Logical thread 1 run latch.
50	ROX	CTRL_T2_RUN_Q: Logical thread 2 run latch.
51	ROX	CTRL_T3_RUN_Q: Logical thread 3 run latch.
52	ROX	CTRL_T4_RUN_Q: Logical thread 4 run latch.
53	ROX	CTRL_T5_RUN_Q: Logical thread 5 run latch.
54	ROX	CTRL_T6_RUN_Q: Logical thread 6 run latch.
55	ROX	CTRL_T7_RUN_Q: Logical thread 7 run latch.
56:62	RO	constant = 0b0000000
63	NCX	Reserved field.

Register Name	Scratch 0 Register
Mnemonic	EX07.EC.CC.PCC0.COMMON.SPR_COMMON.SCR0
Address	000000002E010A86 (SCOM)
Description	Scratch register 0

Bits	SCOM	Field Mnemonic: Description
0:63	RW	Reserved.

Register Name	Scratch 1 Register
Mnemonic	EX07.EC.CC.PCC0.COMMON.SPR_COMMON.SCR1
Address	000000002E010A87 (SCOM)
Description	Scratch Register 1

Bits	SCOM	Field Mnemonic: Description
0:63	RW	Reserved.

Register Name	Scratch 2 Register
Mnemonic	EX07.EC.CC.PCC0.COMMON.SPR_COMMON.SCR2
Address	000000002E010A88 (SCOM)
Description	Scratch Register 2

Bits	SCOM	Field Mnemonic: Description
0:63	RW	Reserved.

Register Name	Scratch 3 Register
Mnemonic	EX07.EC.CC.PCC0.COMMON.SPR_COMMON.SCR3
Address	000000002E010A89 (SCOM)
Description	Scratch Register 3

Bits	SCOM	Field Mnemonic: Description
0:63	RW	Reserved.

Register Name	Virtual Thread 0 HMER Register
Mnemonic	EX07.EC.CC.PCC0.COMMON.SPR_COMMON.V0_HMER
Address	000000002E010A8E (SCOM2) 000000002E010A92 (SCOM1)
Description	Virtual thread 0 HMER register

Bits	SCOM2	SCOM1	Field Mnemonic: Description
0	WOX_OR	RWX_WAND	V0_HMER_MALFUNCTION_ALERT: A processor core in the system has encountered a checkstop error (broadcast signal).
1	WOX_OR	RWX_WAND	V0_HMER_CME_REQUEST: CME requested a hypervisor interrupt.
2	WOX_OR	RWX_WAND	V0_HMER_PROC_RCVY_DONE: A recovery has occurred for error bits that are not masked.
3	WOX_OR	RWX_WAND	Reserved field.
4	WOX_OR	RWX_WAND	V0_HMER_TFAC_ERR: Error for other registers in Timebase facility details in the TFMR.
5	WOX_OR	RWX_WAND	V0_HMER_TFMR_PARITY_ERR: Parity error for the TFMR register in the Timebase facility.
6	WOX_OR	RWX_WAND	Reserved field.
7	WOX_OR	RWX_WAND	Reserved field.
8	WOX_OR	RWX_WAND	V0_HMER_XSCOM_FAIL: An XSCOM operation ended with bad status.
9	WOX_OR	RWX_WAND	V0_HMER_XSCOM_DONE: An XSOM operation ended.
10	WOX_OR	RWX_WAND	Reserved field.
11	WOX_OR	RWX_WAND	V0_HMER_PROC_RCVY_AGAIN: Recovery occurred while bit 2 is still set.
12	WOX_OR	RWX_WAND	Reserved field.
13	WOX_OR	RWX_WAND	Reserved field.
14	WOX_OR	RWX_WAND	Reserved field.
15	WOX_OR	RWX_WAND	Reserved field.
16	WOX_OR	RWX_WAND	V0_HMER_SCOM_FIR_HMI: SCOM set FIR bit to cause recovery.
17	WOX_OR	RWX_WAND	V0_HMER_TRIG_FIR_HMI: Debug trigger set FIR bit to cause recovery.
18	WOX_OR	RWX_WAND	Reserved field.
19	WOX_OR	RWX_WAND	Reserved field.

Bits	SCOM2	SCOM1	Field Mnemonic: Description
20	WOX_OR	RWX_WAND	V0_HMER_HYP_RECOURCE_ERR: Parity error on a hypervisor resource register.
21:23	WOX_OR	RWX_WAND	V0_HMER_XSCOM_STATUS: 000 = No error. 001 = XSCOM blocked due to pending error. 010 = Chiplet offline. 011 = Partial good. 100 = Invalid address / address error. 101 = Clock error. 110 = Parity error. 111 = Time out.
24:63	RO	RO	constant = 0b0000000000000000000000000000000000000000

Register Name	Virtual Thread 1 HMER Register
Mnemonic	EX07.EC.CC.PCC0.COMMON.SPR_COMMON.V1_HMER
Address	000000002E010A8F (SCOM2) 000000002E010A93 (SCOM1)
Description	Virtual thread 1 HMER register

Bits	SCOM2	SCOM1	Field Mnemonic: Description
0	WOX_OR	RWX_WAND	V1_HMER_MALFUNCTION_ALERT: A processor core in the system has encountered a checkstop error (broadcast signal).
1	WOX_OR	RWX_WAND	V1_HMER_CME_REQUEST: The CME requested a hypervisor interrupt.
2	WOX_OR	RWX_WAND	V1_HMER_PROC_RCVY_DONE: A recovery has occurred for error bits that are not masked.
3	WOX_OR	RWX_WAND	Reserved field.
4	WOX_OR	RWX_WAND	V1_HMER_TFAC_ERR: Error for other registers in the Timebase facility.
5	WOX_OR	RWX_WAND	V1_HMER_TFMR_PARITY_ERR: Parity error for the TFMR register in the Timebase facility.
6	WOX_OR	RWX_WAND	Reserved field.
7	WOX_OR	RWX_WAND	Reserved field.
8	WOX_OR	RWX_WAND	V1_HMER_XSCOM_FAIL: An XSCOM operation ended with bad status.
9	WOX_OR	RWX_WAND	V1_HMER_XSCOM_DONE: An XSOM operation ended.
10	WOX_OR	RWX_WAND	Reserved field.
11	WOX_OR	RWX_WAND	V1_HMER_PROC_RCVY_AGAIN: Recovery occurred while bit 2 is still set.
12	WOX_OR	RWX_WAND	Reserved field.
13	WOX_OR	RWX_WAND	Reserved field.
14	WOX_OR	RWX_WAND	Reserved field.
15	WOX_OR	RWX_WAND	Reserved field.
16	WOX_OR	RWX_WAND	V1_HMER_SCOM_FIR_HMI: SCOM set the FIR bit to cause recovery.
17	WOX_OR	RWX_WAND	V1_HMER_TRIG_FIR_HMI: Debug trigger set the FIR bit to cause recovery.
18	WOX_OR	RWX_WAND	Reserved field.
19	WOX_OR	RWX_WAND	Reserved field.

Bits	SCOM2	SCOM1	Field Mnemonic: Description
20	WOX_OR	RWX_WAND	V1_HMER_HYP_RECOURCE_ERR: Parity error on a hypervisor resource register.
21:23	WOX_OR	RWX_WAND	V1_HMER_XSCOM_STATUS: 000 = No error. 001 = XSCOM blocked due to pending error. 010 = Chiplet is offline. 011 = Partial good. 100 = Invalid address / address error. 101 = Clock error. 110 = Parity error. 111 = Time out.
24:63	RO	RO	constant = 0b0000000000000000000000000000000000000000

Register Name	Virtual Thread 2 HMER Register
Mnemonic	EX07.EC.CC.PCC0.COMMON.SPR_COMMON.V2_HMER
Address	000000002E010A90 (SCOM2) 000000002E010A94 (SCOM1)
Description	Virtual thread 2 HMER register

Bits	SCOM2	SCOM1	Field Mnemonic: Description
0	WOX_OR	RWX_WAND	V2_HMER_MALFUNCTION_ALERT: A processor core in the system has encountered a checkstop error (broadcast signal).
1	WOX_OR	RWX_WAND	V2_HMER_CME_REQUEST: The CME requested a hypervisor interrupt.
2	WOX_OR	RWX_WAND	V2_HMER_PROC_RCVY_DONE: A recovery has occurred for error bits that are not masked.
3	WOX_OR	RWX_WAND	Reserved field.
4	WOX_OR	RWX_WAND	V2_HMER_TFAC_ERR: Error for other registers in Timebase facility details in TFMR.
5	WOX_OR	RWX_WAND	V2_HMER_TFMR_PARITY_ERR: Parity error for the TFMR register in Timebase facility.
6	WOX_OR	RWX_WAND	Reserved field.
7	WOX_OR	RWX_WAND	Reserved field.
8	WOX_OR	RWX_WAND	V2_HMER_XSCOM_FAIL: An XSCOM operation ended with bad status.
9	WOX_OR	RWX_WAND	V2_HMER_XSCOM_DONE: An XSOM operation ended.
10	WOX_OR	RWX_WAND	Reserved field.
11	WOX_OR	RWX_WAND	V2_HMER_PROC_RCVY_AGAIN: Recovery occurred while bit 2 is still set.
12	WOX_OR	RWX_WAND	Reserved field.
13	WOX_OR	RWX_WAND	Reserved field.
14	WOX_OR	RWX_WAND	Reserved field.
15	WOX_OR	RWX_WAND	Reserved field.
16	WOX_OR	RWX_WAND	V2_HMER_SCOM_FIR_HMI: SCOM set the FIR bit to cause recovery.
17	WOX_OR	RWX_WAND	V2_HMER_TRIG_FIR_HMI: Debug trigger set the FIR bit to cause recovery.
18	WOX_OR	RWX_WAND	Reserved field.
19	WOX_OR	RWX_WAND	Reserved field.

Bits	SCOM2	SCOM1	Field Mnemonic: Description
20	WOX_OR	RWX_WAND	V2_HMER_HYP_RECOURCE_ERR: Parity error on a hypervisor resource register.
21:23	WOX_OR	RWX_WAND	V2_HMER_XSCOM_STATUS: 000 = No error. 001 = XSCOM blocked due to pending error. 010 = Chiplet offline. 011 = Partial good. 100 = Invalid address / address error. 101 = Clock error. 110 = Parity error. 111 = Time out.
24:63	RO	RO	constant = 0b0000000000000000000000000000000000000000

Register Name	Virtual Thread 3 HMER Register
Mnemonic	EX07.EC.CC.PCC0.COMMON.SPR_COMMON.V3_HMER
Address	000000002E010A91 (SCOM2) 000000002E010A95 (SCOM1)
Description	Virtual Thread 3 HMER register

Bits	SCOM2	SCOM1	Field Mnemonic: Description
0	WOX_OR	RWX_WAND	V3_HMER_MALFUNCTION_ALERT: A processor core in the system has encountered a checkstop error (broadcast signal).
1	WOX_OR	RWX_WAND	V3_HMER_CME_REQUEST: The CME requested a hypervisor interrupt.
2	WOX_OR	RWX_WAND	V3_HMER_PROC_RCVY_DONE: A recovery has occurred for error bits that are not masked.
3	WOX_OR	RWX_WAND	Reserved field.
4	WOX_OR	RWX_WAND	V3_HMER_TFAC_ERR: Error for other registers in the Timebase facility.
5	WOX_OR	RWX_WAND	V3_HMER_TFMR_PARITY_ERR: Parity error for the TFMR register in Timebase facility.
6	WOX_OR	RWX_WAND	Reserved field.
7	WOX_OR	RWX_WAND	Reserved field.
8	WOX_OR	RWX_WAND	V3_HMER_XSCOM_FAIL: An XSCOM operation ended with bad status.
9	WOX_OR	RWX_WAND	V3_HMER_XSCOM_DONE: An XSOM operation ended.
10	WOX_OR	RWX_WAND	Reserved field.
11	WOX_OR	RWX_WAND	V3_HMER_PROC_RCVY_AGAIN: Recovery occurred while bit 2 is still set.
12	WOX_OR	RWX_WAND	Reserved field.
13	WOX_OR	RWX_WAND	Reserved field.
14	WOX_OR	RWX_WAND	Reserved field.
15	WOX_OR	RWX_WAND	Reserved field.
16	WOX_OR	RWX_WAND	V3_HMER_SCOM_FIR_HMI: SCOM set the FIR bit to cause recovery.
17	WOX_OR	RWX_WAND	V3_HMER_TRIG_FIR_HMI: Debug trigger set the FIR bit to cause recovery.
18	WOX_OR	RWX_WAND	Reserved field.
19	WOX_OR	RWX_WAND	Reserved field.

Bits	SCOM2	SCOM1	Field Mnemonic: Description
20	WOX_OR	RWX_WAND	V3_HMER_HYP_RECOURCE_ERR: Parity error on a hypervisor resource register.
21:23	WOX_OR	RWX_WAND	V3_HMER_XSCOM_STATUS: 000 = No error. 001 = XSCOM blocked due to pending error. 010 = Chiplet offline. 011 = Partial good. 100 = Invalid address / address error. 101 = Clock error. 110 = Parity error. 111 = Time out.
24:63	RO	RO	constant = 0b0000000000000000000000000000000000000000

Register Name	HMER Enable Register
Mnemonic	EX07.EC.CC.PCC0.COMMON.SPR_COMMON.HMEER
Address	000000002E010A96 (SCOM)
Description	HMER enable register

Bits	SCOM	Field Mnemonic: Description
0:23	RW	Reserved field.
24:63	RO	constant = 0b0000000000000000000000000000000000000000

Register Name	Special Attention Register
Mnemonic	EX07.EC.CC.PCC0.COMMON.SPR_COMMON.SPATTN
Address	000000002E010A97 (SCOM2) 000000002E010A98 (SCOM1) 000000002E010A99 (SCOM)
Description	Special attention register

Bits	SCOM2	SCOM1	SCOM	Field Mnemonic: Description
0	WOX_OR	WOX_AND	RWX	Reserved field.
1	WOX_OR	WOX_AND	RWX	Reserved field.
2	WOX_OR	WOX_AND	RWX	Reserved field.
3	WOX_OR	WOX_AND	RWX	Reserved field.
4	WOX_OR	WOX_AND	RWX	Reserved field.
5	WOX_OR	WOX_AND	RWX	Reserved field.
6	WOX_OR	WOX_AND	RWX	Reserved field.
7	WOX_OR	WOX_AND	RWX	Reserved field.
8	WOX_OR	WOX_AND	RWX	Reserved field.
9	WOX_OR	WOX_AND	RWX	Reserved field.
10	WOX_OR	WOX_AND	RWX	Reserved field.
11	WOX_OR	WOX_AND	RWX	Reserved field.
12	WOX_OR	WOX_AND	RWX	Reserved field.

Bits	SCOM2	SCOM1	SCOM	Field Mnemonic: Description
13	WOX_OR	WOX_AND	RWX	Reserved field.
14	WOX_OR	WOX_AND	RWX	Reserved field.
15	WOX_OR	WOX_AND	RWX	Reserved field.
16	WOX_OR	WOX_AND	RWX	Reserved field.
17	WOX_OR	WOX_AND	RWX	Reserved field.
18	WOX_OR	WOX_AND	RWX	Reserved field.
19	WOX_OR	WOX_AND	RWX	Reserved field.
20	WOX_OR	WOX_AND	RWX	Reserved field.
21	WOX_OR	WOX_AND	RWX	Reserved field.
22	WOX_OR	WOX_AND	RWX	Reserved field.
23	WOX_OR	WOX_AND	RWX	Reserved field.
24	WOX_OR	WOX_AND	RWX	Reserved field.
25	WOX_OR	WOX_AND	RWX	Reserved field.
26	WOX_OR	WOX_AND	RWX	Reserved field.
27	WOX_OR	WOX_AND	RWX	Reserved field.
28	WOX_OR	WOX_AND	RWX	Reserved field.
29	WOX_OR	WOX_AND	RWX	Reserved field.
30	WOX_OR	WOX_AND	RWX	Reserved field.
31	WOX_OR	WOX_AND	RWX	Reserved field.
32:63	RO	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	Special Attention Mask Register
Mnemonic	EX07.EC.CC.PCC0.COMMON.SPR_COMMON.SPATTN_MASK
Address	000000002E010A9A (SCOM)
Description	Special attention mask register

Bits	SCOM	Field Mnemonic: Description
0:3	RW	Reserved field.
4:7	RW	Reserved field.
8:11	RW	Reserved field.
12:15	RW	Reserved field.
16:19	RW	Reserved field.
20:23	RW	Reserved field.
24:27	RW	Reserved field.
28:31	RW	Reserved field.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	Thread Information Register
Mnemonic	EX07.EC.CC.PCC0.PMC.THREAD_INFO
Address	000000002E010A9B (SCOM)
Description	Thread Information Register

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	Reserved field.
2	ROX	Reserved field.
3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.
7	ROX	Reserved field.
8:9	ROX	Reserved field.
10:11	ROX	Reserved field.
12:13	ROX	Reserved field.
14:15	ROX	Reserved field.
16:17	ROX	Reserved field.
18:21	RW	Reserved field.
22	RWX	Reserved field.
23:63	RO	constant = 0b00000000000000000000000000000000000000000

Register Name	Direct Controls Register
Mnemonic	EX07.EC.CC.PCC0.PMC.DIRECT_CONTROLS
Address	000000002E010A9C (SCOM)
Description	Directs injects into logic.

Bits	SCOM	Field Mnemonic: Description
0:2	RO	constant = 0b000
3	WOX_1P	Reserved field.
4	WOX_1P	Reserved field.
5	WOX_1P	Reserved field.
6	WOX_1P	Reserved field.
7	WOX_1P	Reserved field.
8:10	RO	constant = 0b000
11	WOX_1P	Reserved field.
12	WOX_1P	Reserved field.
13	WOX_1P	Reserved field.
14	WOX_1P	Reserved field.

Bits	SCOM	Field Mnemonic: Description
15	WOX_1P	Reserved field.
16:18	RO	constant = 0b000
19	WOX_1P	Reserved field.
20	WOX_1P	Reserved field.
21	WOX_1P	Reserved field.
22	WOX_1P	Reserved field.
23	WOX_1P	Reserved field.
24:26	RO	constant = 0b000
27	WOX_1P	Reserved field.
28	WOX_1P	Reserved field.
29	WOX_1P	Reserved field.
30	WOX_1P	Reserved field.
31	WOX_1P	Reserved field.
32	WOX_1P	Reserved field.
33:36	WOX_1P	Reserved field.
37:39	WOX_1P	Reserved field.
40	WOX_1P	Reserved field.
41:44	WOX_1P	Reserved field.
45:47	WOX_1P	Reserved field.
48	WOX_1P	Reserved field.
49:52	WOX_1P	Reserved field.
53:55	WOX_1P	Reserved field.
56	WOX_1P	Reserved field.
57:60	WOX_1P	Reserved field.
61:63	WOX_1P	Reserved field.

Register Name	**RAS Mode Register**
Mnemonic	EX07.EC.C0.PC.PMU.SPR_CORE.RAS_MODEREG
Address	000000002E010A9D (SCOM)
Description	RAS mode register

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	RW	Reserved field.
57	RW	Reserved field.
58:61	RO	constant = 0b0000
62	RW	Reserved field.
63	RW	Reserved field.

Register Name	Throttle Control Register
Mnemonic	EX07.EC.CC.PCC0.COMMON.POW.THROTTLE_CONTROL
Address	000000002E010A9E (SCOM)
Description	Throttle Control Register

Bits	SCOM	Field Mnemonic: Description
0:1	RW	Reserved field.
2	RW	Reserved field.
3	RW	Reserved field.
4	RW	Reserved field.
5	RW	Reserved field.
6:8	RW	Reserved field.
9:10	RW	Reserved field.
11:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000

Register Name	SPURR Frequency Detection Cycle Count Register
Mnemonic	EX07.EC.CC.PCC0.TFDP.TFP.SPURR_FREQ_DETECT_CYC_CNT
Address	000000002E010A9F (SCOM)
Description	Scale detect cycle count SCOM

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	CYCLE_COUNT: The cycle count used by the automatic frequency scale detector represents the upper eight bits of a 13-bit cycle counter that counts the number of core clock cycles in the last interval of 16 TOD steps.
8:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	SPURR Frequency Scale Register
Mnemonic	EX07.EC.CC.PCC0.TFDP.TFP.SPURR_FREQ_SCALE
Address	000000002E010AA0 (SCOM)
Description	SPURR frequency scale SCOM

Bits	SCOM	Field Mnemonic: Description
0	RW	SCALE_OVERRIDE_EN: Frequency scale override enable (default=0b1). Reading this bit returns the value that was written.
1:7	RW	SCALE_FACTOR: Frequency scale factor in 64ths (default=0b1000000). Reading these bits returns the value that was written.
8:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	SPURR Frequency Reference Register
Mnemonic	EX07.EC.CC.PCC0.TFDP.TFP.SPURR_FREQ_REF
Address	000000002E010AA1 (SCOM)
Description	SPURR frequency reference SCOM

Bits	SCOM	Field Mnemonic: Description
0:7	RW	FREQUENCY_REFERENCE: The frequency reference override. Represents the reference cycle count in twos complement form for 16 TOD step intervals, dropping the five LSBs before forming the complement. Reading these bits returns the value that was written.
8:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	POWER Management Events Register
Mnemonic	EX07.EC.CC.PCC0.TFDP.TFP.PWM_EVENTS
Address	000000002E010AA2 (SCOM)
Description	POWER management event selects

Bits	SCOM	Field Mnemonic: Description
0:31	RO	constant = 0b00000000000000000000000000000000
32	RW	PWM_EVENTS_RESERVED_32: Reserved.
33:39	RW	FREQ_SCALE_A_THRESHOLD: Frequency scale lower threshold A (default = 0b1000000).
40	RW	PWM_EVENTS_RESERVED_40: Reserved.
41:47	RW	FREQ_SCALE_B_THRESHOLD: Frequency scale upper threshold B (default = 0b1000000).
48	RW	PWM_EVENTS_RESERVED_48: Reserved.
49:51	RW	PSTATE_A_THRESHOLD: P-state lower threshold A.
52	RW	PWM_EVENTS_RESERVED_52: Reserved.
53:55	RW	PSTATE_B_THRESHOLD: P-state upper threshold B.
56	RW	PWM_EVENTS_RESERVED_56: Reserved.
57	RW	PWM_EVENTS_RESERVED_57: Reserved.
58:59	RW	EVENT_MUX_SELECTS: Event multiplexer select 00 = Frequency threshold compares A and B (against scale used by SPURR before PMCR fraction) 01 = P-state threshold compares A and B (against value in PMCR) 10 = PMCM threshold compare (from PMCR) || Max PSAV Mode (from PMCR) 11 = PMCM threshold compare (from PMCR) || PMCM compare (actual).
60	RW	PWM_EVENTS_RESERVED_60: Reserved.
61	RW	PWM_EVENTS_RESERVED_61: Reserved.
62:63	RW	PMCM_THRESHOLD: PMCM threshold.

Register Name	Timebase Read from Chip TOD Register
Mnemonic	EX07.EC.CC.PCC0.TOD_READ
Address	000000002E010AA3 (SCOM)
Description	Timebase read from chip TOD

Bits	SCOM	Field Mnemonic: Description
0:59	ROX	TIMEBASE: Timebase register.
60:63	RO	constant = 0b0000

Register Name	Time Of Day Synchronization 0 Register
Mnemonic	EX07.EC.CC.PCC0.TOD_SYNC000
Address	000000002E010AA3 (SCOM1)
Description	Time of day (mttod) for sync_bit_sel = 000. Note: The TOD_SYNCxxx registers cannot be tested together by register check in one run.

Bits	SCOM1	Field Mnemonic: Description
0:54	WOX	TIMEBASE: Timebase register.
55:59	RO	Not implemented.
60:63	WOX	CHIP_TOD_STATUS: Chip time of day status.

Register Name	Time Of Day Synchronization 1 Register
Mnemonic	EX07.EC.CC.PCC0.TOD_SYNC001
Address	000000002E010AA3 (SCOM1)
Description	Time of day (mttod) for sync_bit_sel = 001. Note: The TOD_SYNCxxx registers cannot be tested together by register check in one run.

Bits	SCOM1	Field Mnemonic: Description
0:53	WOX	TIMEBASE: Timebase register.
54:59	RO	Not implemented.
60:63	WOX	CHIP_TOD_STATUS: Chip time of day status.

Register Name	Time Of Day Synchronization 2 Register
Mnemonic	EX07.EC.CC.PCC0.TOD_SYNC010
Address	000000002E010AA3 (SCOM1)
Description	Time of day (mttod) for sync_bit_sel = 010. Note: The TOD_SYNCxxx registers cannot be tested together by register check in one run.

Bits	SCOM1	Field Mnemonic: Description
0:52	WOX	TIMEBASE: Timebase register.
53:59	RO	Not implemented.
60:63	WOX	CHIP_TOD_STATUS: Chip time of day status.

Register Name	Time Of Day Synchronization 3 Register
Mnemonic	EX07.EC.CC.PCC0.TOD_SYNC011
Address	000000002E010AA3 (SCOM1)
Description	Time of day (mttod) for sync_bit_sel=011. Note: The TOD_SYNCxxx registers cannot be tested together by register check in one run.

Bits	SCOM1	Field Mnemonic: Description
0:51	WOX	TIMEBASE: Timebase register.
52:59	RO	Not implemented.
60:63	WOX	CHIP_TOD_STATUS: Chip time of day status.

Register Name	Time Of Day Synchronization 4 Register
Mnemonic	EX07.EC.CC.PCC0.TOD_SYNC100
Address	000000002E010AA3 (SCOM1)
Description	Time of day (mttod) for sync_bit_sel = 100. Note: The TOD_SYNCxxx registers cannot be tested together by register check in one run.

Bits	SCOM1	Field Mnemonic: Description
0:50	WOX	TIMEBASE: Timebase register.
51:59	RO	Not implemented.
60:63	WOX	CHIP_TOD_STATUS: Chip time of day status.

Register Name	Time Of Day Synchronization 5 Register
Mnemonic	EX07.EC.CC.PCC0.TOD_SYNC101
Address	000000002E010AA3 (SCOM1)
Description	Time of day (mttod) for sync_bit_sel = 101. Note: The TOD_SYNCxxx registers cannot be tested together by register check in one run.

Bits	SCOM1	Field Mnemonic: Description
0:49	WOX	TIMEBASE: Timebase register.
50:59	RO	Not implemented.
60:63	WOX	CHIP_TOD_STATUS: Chip time of day status.

Register Name	Time Of Day Synchronization 6 Register
Mnemonic	EX07.EC.CC.PCC0.TOD_SYNC110
Address	000000002E010AA3 (SCOM1)
Description	Time of day (mttod) for sync_bit_sel=110. Note: The TOD_SYNCxxx registers cannot be tested together by register check in one run.

Bits	SCOM1	Field Mnemonic: Description
0:48	WOX	TIMEBASE: Timebase register.
49:59	RO	Not implemented.

Bits	SCOM1	Field Mnemonic: Description
60:63	WOX	CHIP_TOD_STATUS: Chip time of day status.

Register Name	Time Of Day Synchronization 7 Register
Mnemonic	EX07.EC.CC.PCC0.TOD_SYNC111
Address	000000002E010AA3 (SCOM1)
Description	Time of day (mttod) for sync_bit_sel = 111. Note: The TOD_SYNCxxx registers cannot be tested together by register check in one run.

Bits	SCOM1	Field Mnemonic: Description
0:47	WOX	TIMEBASE: Timebase register.
48:59	RO	Not implemented.
60:63	WOX	CHIP_TOD_STATUS: Chip time of day status.

Register Name	Time of Day Step Check Register
Mnemonic	EX07.EC.CC.PCC0.COMMON.TFC.TOD_STEP_CHECK
Address	000000002E010AA4 (SCOM)
Description	Time of day step check register

Bits	SCOM	Field Mnemonic: Description
0:14	RW	Reserved.
15:63	RO	constant = 0b0000000000000000000000000000000000000000000000000

Register Name	SCOM Hardware Implementation Detail 0 Register
Mnemonic	EX07.EC.C0.PC.PMU.SPR_CORE.SHID0
Address	000000002E010AA5 (SCOM)
Description	SCOM hardware implementation detail register 0

Bits	SCOM	Field Mnemonic: Description
0	RW	Reserved field.
1	RW	Reserved field.
2:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	Hypervisor Current State Register
Mnemonic	EX07.EC.C0.PC.PMU.SPR_CORE.HV_STATE
Address	000000002E010AA6 (SCOM)
Description	Hypervisor current state

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
56	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60	ROX	Reserved field.
61	ROX	Reserved field.
62	ROX	Reserved field.
63	ROX	Reserved field.

Register Name	Core Fuses Register
Mnemonic	EX07.EC.C0.PC.PMU.SPR_CORE.CORE_FUSES
Address	000000002E010AA7 (SCOM)
Description	Core fuses

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	Reserved field.
2:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	IMA Event Mask Register
Mnemonic	EX07.EC.C0.PC.IMA.IMA_EVENT_MASK
Address	000000002E010AA8 (SCOM)
Description	IMA event mask register

Bits	SCOM	Field Mnemonic: Description
0	RWX	Reserved field.
1	RWX	Reserved field.
2	RWX	Reserved field.
3	RWX	Reserved field.
4	RWX	Reserved field.
5	RWX	Reserved field.
6	RWX	Reserved field.
7	RWX	Reserved field.
8	RWX	Reserved field.
9	RWX	Reserved field.
10	RWX	Reserved field.
11	RWX	Reserved field.
12	RWX	Reserved field.
13	RWX	Reserved field.
14	RWX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
15	RWX	Reserved field.
16	RWX	Reserved field.
17	RWX	Reserved field.
18	RWX	Reserved field.
19	RWX	Reserved field.
20	RWX	Reserved field.
21	RWX	Reserved field.
22	RWX	Reserved field.
23	RWX	Reserved field.
24	RWX	Reserved field.
25	RWX	Reserved field.
26	RWX	Reserved field.
27	RWX	Reserved field.
28	RWX	Reserved field.
29	RWX	Reserved field.
30:32	RWX	Reserved field.
33	RWX	Reserved field.
34	RWX	Reserved field.
35:63	RO	constant = 0b00000000000000000000000000000

Register Name	IMA Trace Register
Mnemonic	EX07.EC.C0.PC.IMA.IMA_TRACE
Address	000000002E010AA9 (SCOM)
Description	IMA trace register

Bits	SCOM	Field Mnemonic: Description
0:1	RWX	Reserved field.
2:33	RWX	Reserved field.
34:40	RWX	Reserved field.
41:47	RWX	Reserved field.
48:63	RO	constant = 0b0000000000000000

Register Name	SCOM PMU 0 Register
Mnemonic	EX07.EC.C0.PC.T0_PMU_SCOM
Address	000000002E010AAA (SCOM)
Description	Writable PMU control register

Bits	SCOM	Field Mnemonic: Description
0:8	RW	Reserved field.

Bits	SCOM	Field Mnemonic: Description
9:17	RW	Reserved field.
18	RW	Reserved field.
19:23	RW	Reserved field.

Register Name	SCOM PMU 1 Register
Mnemonic	EX07.EC.C0.PC.T1_PMU_SCOM
Address	000000002E010AAB (SCOM)
Description	Writable PMU control register

Bits	SCOM	Field Mnemonic: Description
0:8	RW	Reserved field.
9:17	RW	Reserved field.
18	RW	Reserved field.
19:23	RW	Reserved field.

Register Name	SCOM PMU 2 Register
Mnemonic	EX07.EC.C0.PC.T2_PMU_SCOM
Address	000000002E010AAC (SCOM)
Description	Writable PMU control register

Bits	SCOM	Field Mnemonic: Description
0:8	RW	Reserved field.
9:17	RW	Reserved field.
18	RW	Reserved field.
19:23	RW	Reserved field.

Register Name	SCOM PMU 3 Register
Mnemonic	EX07.EC.C0.PC.T3_PMU_SCOM
Address	000000002E010AAD (SCOM)
Description	Writable PMU control register

Bits	SCOM	Field Mnemonic: Description
0:8	RW	Reserved field.
9:17	RW	Reserved field.
18	RW	Reserved field.
19:23	RW	Reserved field.

Register Name	Sier Mask Register
Mnemonic	EX07.EC.C0.PC.PMU.PMUC.SIER_MASK
Address	000000002E010AAE (SCOM)
Description	Sier Mask SCOM Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	Reserved field.

Register Name	SRC Mask Register
Mnemonic	EX07.EC.C0.PC.PMU.PMUC.SRC_MASK
Address	000000002E010AAF (SCOM)
Description	SRC mask SCOM register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	Reserved field.

Register Name	SCOMC for PMU Register
Mnemonic	EX07.EC.C0.PC.PMU.SPR_CORE.PMU_SCOMC
Address	000000002E010AB0 (SCOM)
Description	SCOMC for PMU indirect SCOM access

Bits	SCOM	Field Mnemonic: Description
0	RWX	Reserved field.
1	RWX	Reserved field.
2	RWX	Reserved field.
3	RWX	Reserved field.
4	RWX	Reserved field.
5	RWX	Reserved field.
6	RWX	Reserved field.
7	RWX	Reserved field.
8	RWX	Reserved field.
9	RWX	Reserved field.
10	RWX	Reserved field.
11	RWX	Reserved field.
12:13	RWX	Reserved field.
14:63	RO	constant = 0b00000000000000000000000000000000000000000000000000

Register Name	Enable SCOMC for PMU Register
Mnemonic	EX07.EC.C0.PC.PMU.SPR_CORE.PMU_SCOMC_EN
Address	000000002E010AB2 (SCOM)
Description	Enable for PMU indirect SCOM access

Bits	SCOM	Field Mnemonic: Description
0	RWX	Reserved field.
1:63	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000000

Register Name	Core Thread State Register
Mnemonic	EX07.EC.CC.PCC0.PMC.CORE_THREAD_STATE
Address	000000002E010AB3 (SCOM)
Description	Restore

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	Reserved.
32:35	ROX	Reserved field.
36:39	ROX	Reserved field.
40:43	ROX	Reserved field.
44:47	ROX	Reserved field.
48:55	ROX	Reserved.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60:62	ROX	Reserved.
63	ROX	Reserved field.

Register Name	Invalidate ERAT Register
Mnemonic	EX07.EC.C0.PC.PMU.SPR_CORE.INV_ERATE
Address	000000002E010AB4 (SCOM)
Description	Invalidate ERATs

Bits	SCOM	Field Mnemonic: Description
0:62	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000000
63	WOX_1P	Reserved field.

Register Name	SPR Core Hold Out Register
Mnemonic	EX07.EC.C0.PC.PMU.SPR_CORE.SPR_CORE_HOLD_OUT
Address	000000002E010AB5 (SCOM)
Description	SPR core error report hold out register

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	Reserved field.
2:7	ROX	Reserved field.
8	ROX	Reserved field.
9	ROX	Reserved field.
10	ROX	Reserved field.
11	ROX	Reserved field.
12:63	RO	constant = 0b0000000000000000000000000000000000000000000000000000

Register Name	PMU Hold Out Register
Mnemonic	EX07.EC.C0.PC.PMU.SPR_CORE.PMU_HOLD_OUT
Address	000000002E010AB6 (SCOM)
Description	PMU error report hold out register

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	Reserved field.
4:7	ROX	Reserved field.
8:11	ROX	Reserved field.
12:15	ROX	Reserved field.
16:63	RO	constant = 0b000000000000000000000000000000000000000000000000

Register Name	TFAC Hold Out Register
Mnemonic	EX07.EC.CC.PCC0.COMMON.SPR_COMMON.TFAC_HOLD_OUT
Address	000000002E010AB7 (SCOM)
Description	TFAC error report hold out register

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved.

Register Name	SPR Common Hold Out Register
Mnemonic	EX07.EC.CC.PCC0.COMMON.SPR_COMMON.SPR_COMMON_HOLD_OUT
Address	000000002E010AB8 (SCOM)
Description	SPR common error report hold out register

Bits	SCOM	Field Mnemonic: Description
0:20	ROX	Reserved.
21:63	RO	constant = 0b0000000000000000000000000000000000000000000

Register Name	IFU Hold Out 0 Register
Mnemonic	EX07.EC.C0.IFU.IFRE.IFCER0.IFU_HOLD_OUT_0
Address	000000002E010C00 (SCOM)
Description	IFU error report hold out 0 register

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.
7	ROX	Reserved field.
8	ROX	Reserved field.
9	ROX	Reserved field.
10	ROX	Reserved field.
11	ROX	Reserved field.
12	ROX	Reserved field.
13	ROX	Reserved field.
14	ROX	Reserved field.
15	ROX	Reserved field.
16:31	RO	constant = 0b0000000000000000

Register Name	IFU Hold Out 1 Register
Mnemonic	EX07.EC.C0.IFU.IFRE.IFCER0.IFU_HOLD_OUT_1
Address	000000002E010C01 (SCOM)
Description	IFU error report hold out 1 register

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	Reserved field.
2	ROX	Reserved field.
3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.
7	ROX	Reserved field.
8	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
9	ROX	Reserved field.
10	ROX	Reserved field.
11	ROX	Reserved field.
12	ROX	Reserved field.
13	ROX	Reserved field.
14	ROX	Reserved field.
15	ROX	Reserved field.
16:31	RO	constant = 0b0000000000000000

Register Name	IFU Hold Out 2 Register
Mnemonic	EX07.EC.C0.IFU.IFRE.IFCER0.IFU_HOLD_OUT_2
Address	000000002E010C02 (SCOM)
Description	IFU error report hold out 2 register

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	Reserved field.
2	ROX	Reserved field.
3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.
7	ROX	Reserved field.
8	ROX	Reserved field.
9	ROX	Reserved field.
10	ROX	Reserved field.
11	ROX	Reserved field.
12	ROX	Reserved field.
13	ROX	Reserved field.
14	ROX	Reserved field.
15	ROX	Reserved field.
16:31	RO	constant = 0b0000000000000000

Register Name	IFU Hold Out 3 Register
Mnemonic	EX07.EC.C0.IFU.IFRE.IFCER0.IFU_HOLD_OUT_3
Address	000000002E010C03 (SCOM)
Description	IFU error report hold out 3 register

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	Reserved field.
2	ROX	Reserved field.
3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.
7	ROX	Reserved field.
8	ROX	Reserved field.
9	ROX	Reserved field.
10	ROX	Reserved field.
11	ROX	Reserved field.
12	ROX	Reserved field.
13	ROX	Reserved field.
14	ROX	Reserved field.
15	ROX	Reserved field.
16:31	RO	constant = 0b0000000000000000

Register Name	**Parity Error Injection Register**
Mnemonic	EX07.EC.C0.IFU.IFRE.IFCER0.ERR_INJ_REG
Address	000000002E010C04 (SCOM)
Description	Parity error injection

Bits	SCOM	Field Mnemonic: Description
0	RW	ICACHE_PARITY_ERROR_INJECT: ICACHE parity error inject. Bit0 = Each time pc_if_err_inj turns on, IFU injects on ICACHE parity error on the next demand ICACHE miss Bit1 = Each time pc_if_err_inj turns on, IFU will inject on ICACHE directory parity error on the next demand ICACHE miss Bit2 = Each time pc_if_err_inj turns on, IFU will inject on ERAT ram parity error on the real address for the next ERAT miss Bit3 = Each time pc_if_err_inj turns on, IFU will inject on ERAT cam parity error on the EA for next ERAT miss Bit4 = When set to 1, the bandwidth beyond the L3 cache is reduced.
1	RW	IDIR_ERROR_INJECT: ICACHE directory parity error inject. Bit0 = Each time pc_if_err_inj turns on, IFU will inject on ICACHE parity error on the next demand ICACHE miss Bit1 = Each time pc_if_err_inj turns on, IFU will inject on ICACHE directory parity error on the next demand ICACHE miss Bit2 = Each time pc_if_err_inj turns on, IFU will inject on ERAT ram parity error on the real address for the next ERAT miss Bit3 = Each time pc_if_err_inj turns on, IFU will inject on ERAT cam parity error on the EA for next ERAT miss Bit4 = When set to 1, the bandwidth beyond the L3 cache is reduced.

Bits	SCOM	Field Mnemonic: Description
2	RW	IERAT_RA_INJECT: iERAT real address ram error inject. Bit0 = Each time pc_if_err_inj turns on, IFU will inject on ICACHE parity error on the next demand ICACHE miss Bit1 = Each time pc_if_err_inj turns on, IFU will inject on ICACHE directory parity error on the next demand ICACHE miss Bit2 = Each time pc_if_err_inj turns on, IFU will inject on ERAT ram parity error on the real address for the next ERAT miss Bit3 = Each time pc_if_err_inj turns on, IFU will inject on ERAT cam parity error on the EA for next ERAT miss Bit4 = When set to 1, the bandwidth beyond the L3 cache is reduced.
3	RW	IERAT_EA_INJECT: iERAT effective address cam error inject. Bit0 = Each time pc_if_err_inj turns on, IFU will inject on ICACHE parity error on the next demand ICACHE miss Bit1 = Each time pc_if_err_inj turns on, IFU will inject on ICACHE directory parity error on the next demand ICACHE miss Bit2 = Each time pc_if_err_inj turns on, IFU will inject on ERAT ram parity error on the real address for the next ERAT miss Bit3 = Each time pc_if_err_inj turns on, IFU will inject on ERAT cam parity error on the EA for next ERAT miss Bit4 = When set to 1, the bandwidth beyond the L3 cache is reduced.
4	RW	ENABLE_REDUCE_SPEC: When set at 1, reduces the bandwidth beyond the L3 cache. Bit0 = Each time pc_if_err_inj turns on, IFU will inject on ICACHE parity error on the next demand ICACHE miss Bit1 = Each time pc_if_err_inj turns on, IFU will inject on ICACHE directory parity error on the next demand ICACHE miss Bit2 = Each time pc_if_err_inj turns on, IFU will inject on ERAT ram parity error on the real address for the next ERAT miss Bit3 = Each time pc_if_err_inj turns on, IFU will inject on ERAT cam parity error on the EA for next ERAT miss Bit4 = When set to 1, the bandwidth beyond the L3 cache is reduced.
5:9	RO	constant = 0b00000

Register Name	ISU Hold Out 0 Register
Mnemonic	EX07.EC.C0.SD.ISU_REG0_HOLD_OUT
Address	000000002E010C40 (SCOM)
Description	ISU error report hold out register 0

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	Reserved field.
2	ROX	Reserved field.
3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.
7	ROX	Reserved field.
8	ROX	Reserved field.
9	ROX	Reserved field.
10:11	RO	constant = 0b00
12	ROX	Reserved field.
13	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
14	ROX	Reserved field.
15	ROX	Reserved field.
16	ROX	Reserved field.
17	ROX	Reserved field.

Register Name	ISU Hold Out 1 Register
Mnemonic	EX07.EC.C0.SD.ISU_REG1_HOLD_OUT
Address	000000002E010C41 (SCOM)
Description	ISU error report hold out register 1

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	Reserved field.
2	ROX	Reserved field.
3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.
7	ROX	Reserved field.
8	ROX	Reserved field.
9	ROX	Reserved field.
10:11	RO	constant = 0b00
12	ROX	Reserved field.
13	ROX	Reserved field.
14	ROX	Reserved field.
15	ROX	Reserved field.
16	ROX	Reserved field.
17	ROX	Reserved field.

Register Name	ISU Hold Out 2 Register
Mnemonic	EX07.EC.C0.SD.ISU_REG2_HOLD_OUT
Address	000000002E010C42 (SCOM)
Description	ISU error report hold out register 2

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	Reserved field.
2	ROX	Reserved field.
3	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.
7	ROX	Reserved field.
8	ROX	Reserved field.
9	ROX	Reserved field.
10:11	RO	constant = 0b00
12	ROX	Reserved field.
13	ROX	Reserved field.
14	ROX	Reserved field.
15	ROX	Reserved field.
16	ROX	Reserved field.
17	ROX	Reserved field.

Register Name	ISU Hold Out 3 Register
Mnemonic	EX07.EC.C0.SD.ISU_REG3_HOLD_OUT
Address	000000002E010C43 (SCOM)
Description	ISU error report hold out register 3

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	Reserved field.
2	ROX	Reserved field.
3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.
7	ROX	Reserved field.
8	ROX	Reserved field.
9	ROX	Reserved field.
10:11	RO	constant = 0b00
12	ROX	Reserved field.
13	ROX	Reserved field.
14	ROX	Reserved field.
15	ROX	Reserved field.
16	ROX	Reserved field.
17	ROX	Reserved field.

Register Name	ISU Hold Out 4 Register
Mnemonic	EX07.EC.C0.SD.ISU_REG4_HOLD_OUT
Address	000000002E010C44 (SCOM)
Description	ISU error report hold out register 4

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	Reserved field.
2	ROX	Reserved field.
3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.
7	ROX	Reserved field.
8	ROX	Reserved field.
9	ROX	Reserved field.
10	ROX	Reserved field.
11	ROX	Reserved field.
12	ROX	Reserved field.
13	ROX	Reserved field.
14	ROX	Reserved field.
15	ROX	Reserved field.
16	ROX	Reserved field.
17	ROX	Reserved field.

Register Name	ISU Hold Out 5 Register
Mnemonic	EX07.EC.C0.SD.ISU_REG5_HOLD_OUT
Address	000000002E010C45 (SCOM)
Description	ISU error report hold out register 5

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	Reserved field.
2	ROX	Reserved field.
3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.
7	ROX	Reserved field.
8	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
9	ROX	Reserved field.
10:17	ROX	Reserved field.

Register Name	ISU Debug Control Register
Mnemonic	EX07.EC.C0.SD.ISU_DEBUG_CTRL
Address	000000002E010C46 (SCOM)
Description	ISU debug bus controls

Bits	SCOM	Field Mnemonic: Description
0:17	RW	Reserved field.

Register Name	LSU Hold Out 0 Register
Mnemonic	EX07.EC.C0.LS.LSU_HOLD_OUT_REG0
Address	000000002E010C80 (SCOM)
Description	LSU error report hold out register 0

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	Reserved field.
2	ROX	Reserved field.
3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.
7	ROX	Reserved field.
8	ROX	Reserved field.
9	ROX	Reserved field.
10	ROX	Reserved field.
11	ROX	Reserved field.
12	ROX	Reserved field.
13	ROX	Reserved field.
14	ROX	Reserved field.
15	ROX	Reserved field.

Register Name	LSU Hold Out 1 Register
Mnemonic	EX07.EC.C0.LS.LSU_HOLD_OUT_REG1
Address	000000002E010C81 (SCOM)
Description	LSU error report hold out register 1

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	Reserved field.
2	ROX	Reserved field.
3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.
7	ROX	Reserved field.
8	ROX	Reserved field.
9	ROX	Reserved field.
10	ROX	Reserved field.
11	ROX	Reserved field.
12	ROX	Reserved field.
13	ROX	Reserved field.
14	ROX	Reserved field.
15	ROX	Reserved field.

Register Name	LSU Hold Out 2 Register
Mnemonic	EX07.EC.C0.LS.LSU_HOLD_OUT_REG2
Address	000000002E010C82 (SCOM)
Description	LSU error report hold out register 2

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	Reserved field.
2	ROX	Reserved field.
3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.
7	ROX	Reserved field.
8	ROX	Reserved field.
9	ROX	Reserved field.
10	ROX	Reserved field.
11	ROX	Reserved field.
12	ROX	Reserved field.
13	ROX	Reserved field.
14	ROX	Reserved field.
15	ROX	Reserved field.

Register Name	LSU Hold Out 3 Register
Mnemonic	EX07.EC.C0.LS.LSU_HOLD_OUT_REG3
Address	000000002E010C83 (SCOM)
Description	LSU error report hold out register 3

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	Reserved field.
2	ROX	Reserved field.
3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.
7	ROX	Reserved field.
8	ROX	Reserved field.
9	ROX	Reserved field.
10	ROX	Reserved field.
11	ROX	Reserved field.
12	ROX	Reserved field.
13	ROX	Reserved field.
14	ROX	Reserved field.
15	ROX	Reserved field.

Register Name	Error Injections Register
Mnemonic	EX07.EC.C0.LS.ERR_INJ_REG
Address	000000002E010CBF (SCOM)
Description	Error injections on LSU checkers

Bits	SCOM	Field Mnemonic: Description
0	RW	Reserved field.
1	RW	Reserved field.
2	RW	Reserved field.
3	RW	Reserved field.
4	RW	Reserved field.
5	RW	Reserved field.
6	RW	Reserved field.
7	RW	Reserved field.
8	RW	Reserved field.
9	RW	Reserved field.

Bits	SCOM	Field Mnemonic: Description
10	RW	Reserved field.
11	RW	Reserved field.
12	RW	Reserved field.
13	RW	Reserved field.
14	RW	Reserved field.
15	RW	Reserved field.

Register Name	Trace Array High Data Register
Mnemonic	EX07.EC.C0.PC.TRACE1.TR.TR0.TRACE_HI_DATA_REG
Address	000000002E011440 (SCOM)
Description	This register provides the high trace array data.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace array data 0:63.

Register Name	Trace Array Low Data Register
Mnemonic	EX07.EC.C0.PC.TRACE1.TR.TR0.TRACE_LO_DATA_REG
Address	000000002E011441 (SCOM)
Description	This register provides the low trace array data.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace array data 64:95.
32:41	ROX	TRACE_ADDRESS: Trace address.
42:50	ROX	TRACE_LAST_BANK: Trace last bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace last bank valid.
52	ROX	TRACE_WRITE_ON_RUN: Trace write-on-run indicator.
53	ROX	TRACE_RUNNING: Trace run indicator.
54:63	ROX	TRACE_HOLD_ADDRESS: Trace hold address (pointing to last entry).

Register Name	Trace Control Configuration Register
Mnemonic	EX07.EC.C0.PC.TRACE1.TR.TR0.TRACE_TRCTRL_CONFIG
Address	000000002E011442 (SCOM)
Description	This register contains trace control configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	Reserved field.
1	RW	WRITE_ON_RUN_MODE: Write on run mode.
2:9	RW	EXTENDED_STORE_ON_TRIG_MODE: Extended trigger mode.
10	RW	BANK_MODE: Bank mode.

Bits	SCOM	Field Mnemonic: Description
11	RW	ENH_TRACE_MODE: Enhanced trace mode.
12	RW	LOCAL_CLOCK_GATE_CONTROL: When this bit is set, internal clock gating is disabled. The trace control logic and the trace data pipeline are always clocked.
13	RW	UNUSED_13B: Unused.
14:21	RW	Reserved field.

Register Name	Trace Data Configuration Register 0
Mnemonic	EX07.EC.C0.PC.TRACE1.TR.TR0.TRACE_TRDATA_CONFIG_0
Address	000000002E011443 (SCOM)
Description	This register contains a trace data compare mask for bits 0 – 63.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: Trace data compare mask for bits 0 to 63.

Register Name	Trace Data Configuration Register 1
Mnemonic	EX07.EC.C0.PC.TRACE1.TR.TR0.TRACE_TRDATA_CONFIG_1
Address	000000002E011444 (SCOM)
Description	This register contains a trace data compare mask for bits 64 – 87.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: Trace data compare mask for bits 64 to 87.

Register Name	Trace Data Configuration Register 2
Mnemonic	EX07.EC.C0.PC.TRACE1.TR.TR0.TRACE_TRDATA_CONFIG_2
Address	000000002E011445 (SCOM)
Description	This register contains patterns A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: pattern_match_pata_0_to_23.
24:47	RW	PATTERNB: pattern_match_patb_0_to_23.

Register Name	Trace Data Configuration Register 3
Mnemonic	EX07.EC.C0.PC.TRACE1.TR.TR0.TRACE_TRDATA_CONFIG_3
Address	000000002E011446 (SCOM)
Description	This register contains patterns C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNC: pattern_match_patc_0_to_23.
24:47	RW	PATTERND: pattern_match_patd_0_to_23.

Register Name	Trace Data Configuration Register 4
Mnemonic	EX07.EC.C0.PC.TRACE1.TR.TR0.TRACE_TRDATA_CONFIG_4
Address	000000002E011447 (SCOM)
Description	This register contains masks A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: mska.
24:47	RW	MASKB: mskb.

Register Name	Trace Data Configuration Register 5
Mnemonic	EX07.EC.C0.PC.TRACE1.TR.TR0.TRACE_TRDATA_CONFIG_5
Address	000000002E011448 (SCOM)
Description	This register contains masks C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: mskc.
24:47	RW	MASKD: mskd.

Register Name	Trace Data Configuration Register 9
Mnemonic	EX07.EC.C0.PC.TRACE1.TR.TR0.TRACE_TRDATA_CONFIG_9
Address	000000002E011449 (SCOM)
Description	This register contains trace data configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disable trace data compression (store data on every cycle).
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Take into account changes in the error bit for trace data compression (default = 0).
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.

Bits	SCOM	Field Mnemonic: Description
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.
10:13	RW	TRIG0_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG0_AND. 0b1XXX = Selects MATCHA OR 0bX1XX = Selects MATCHB OR 0bXX1X = Selects MATCHC OR 0bXXX1 = Selects MATCHD OR 0b0000 = Selects to not OR any MATCHes.
14:17	RW	TRIG0_AND_MASK: The AND of following selected MATCHes is ORed with the result of TRIG0_OR. 0b1XXX = Selects MATCHA AND 0bX1XX = Selects MATCHB AND 0bXX1X = Selects MATCHC AND 0bXXX1 = Selects MATCHD AND 0b0000 = Selects to not AND any MATCHes together to form TRIG0.
18:21	RW	TRIG1_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG1_AND. 0b1XXX = Selects MATCHA OR 0bX1XX = Selects MATCHB OR 0bXX1X = Selects MATCHC OR 0bXXX1 = Selects MATCHD OR 0b0000 = Selects to not OR any MATCHes to form TRIG1.
22:25	RW	TRIG1_AND_MASK: The AND of following selected MATCHes is ORed with the result of TRIG1_OR. 0b1XXX = Selects MATCHA AND 0bX1XX = Selects MATCHB AND 0bXX1X = Selects MATCHC AND 0bXXX1 = Selects MATCHD AND 0b0000 = Selects to not AND any MATCHes together to form TRIG1.
26	RW	TRIG0_NOT_MODE: Invert TRIG0 before using it.
27	RW	TRIG1_NOT_MODE: Invert TRIG1 before using it.
28:31	RW	MATCH_NOT_MODE: Invert the match polarity before using it to form a trigger. 0b1000 = Inverts MATCHA. 0b0100 = Inverts MATCHB. 0b0010 = Inverts MATCHC. 0b0001 = Inverts MATCHD.
32:35	RW	Reserved field.
36:39	RW	Reserved field.

Register Name	Trace Array High Data Register
Mnemonic	EX07.EC.C0.PC.TRACE2.TR.TR0.TRACE_HI_DATA_REG
Address	000000002E011480 (SCOM)
Description	This register provides the high trace array data.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace array data 0:63.

Register Name	Trace Array Low Data Register
Mnemonic	EX07.EC.C0.PC.TRACE2.TR.TR0.TRACE_LO_DATA_REG
Address	000000002E011481 (SCOM)
Description	This register provides the low trace array data.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace array data 64:95.
32:41	ROX	TRACE_ADDRESS: Trace address.
42:50	ROX	TRACE_LAST_BANK: Trace last bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace last bank valid.
52	ROX	TRACE_WRITE_ON_RUN: Trace write-on-run indicator.
53	ROX	TRACE_RUNNING: Trace run indicator.
54:63	ROX	TRACE_HOLD_ADDRESS: Trace hold address (pointing to last entry).

Register Name	Trace Control Configuration Register
Mnemonic	EX07.EC.C0.PC.TRACE2.TR.TR0.TRACE_TRCTRL_CONFIG
Address	000000002E011482 (SCOM)
Description	This register contains trace control configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	Reserved field.
1	RW	WRITE_ON_RUN_MODE: Write-on-run mode.
2:9	RW	EXTENDED_STORE_ON_TRIG_MODE: Extended trigger mode.
10	RW	BANK_MODE: Bank mode.
11	RW	ENH_TRACE_MODE: Enhanced trace mode.
12:13	RW	LCL_CLK_GATE_CTRL: Application note: Do not set lcl_clk_gate_ctrl to '00'; always keep at '11' as a workaround for incorrect clock gating.
14:21	RW	Reserved field.

Register Name	Trace Data Configuration Register 0
Mnemonic	EX07.EC.C0.PC.TRACE2.TR.TR0.TRACE_TRDATA_CONFIG_0
Address	000000002E011483 (SCOM)
Description	This register contains a trace data compare mask for bits 0 – 63.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: Trace data compare mask for bits 0 to 63.

Register Name	Trace Data Configuration Register 1
Mnemonic	EX07.EC.C0.PC.TRACE2.TR.TR0.TRACE_TRDATA_CONFIG_1
Address	000000002E011484 (SCOM)
Description	This register contains a trace data compare mask for bits 64 – 87.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: Trace data compare mask for bits 64 to 87.

Register Name	Trace Data Configuration Register 2
Mnemonic	EX07.EC.C0.PC.TRACE2.TR.TR0.TRACE_TRDATA_CONFIG_2
Address	000000002E011485 (SCOM)
Description	This register contains patterns A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: pattern_match_pata_0_to_23.
24:47	RW	PATTERNB: pattern_match_patb_0_to_23.

Register Name	Trace Data Configuration Register 3
Mnemonic	EX07.EC.C0.PC.TRACE2.TR.TR0.TRACE_TRDATA_CONFIG_3
Address	000000002E011486 (SCOM)
Description	This register contains patterns C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNC: pattern_match_patc_0_to_23.
24:47	RW	PATTERND: pattern_match_patd_0_to_23.

Register Name	Trace Data Configuration Register 4
Mnemonic	EX07.EC.C0.PC.TRACE2.TR.TR0.TRACE_TRDATA_CONFIG_4
Address	000000002E011487 (SCOM)
Description	This register contains masks A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: mska.
24:47	RW	MASKB: mskb.

Register Name	Trace Data Configuration Register 5
Mnemonic	EX07.EC.C0.PC.TRACE2.TR.TR0.TRACE_TRDATA_CONFIG_5
Address	000000002E011488 (SCOM)
Description	This register contains masks C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: mskc.
24:47	RW	MASKD: mskd.

Register Name	Trace Data Configuration Register 9
Mnemonic	EX07.EC.C0.PC.TRACE2.TR.TR0.TRACE_TRDATA_CONFIG_9
Address	000000002E011489 (SCOM)
Description	This register contains trace data configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disable trace data compression (store data on every cycle).
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Take into account changes in the error bit for trace data compression (default = 0).
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.
10:13	RW	TRIG0_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG0_AND. 0b1XXX = Selects MATCHA OR 0bX1XX = Selects MATCHB OR 0bXX1X = Selects MATCHC OR 0bXXX1 = Selects MATCHD OR 0b0000 = Selects to not OR any MATCHes.
14:17	RW	TRIG0_AND_MASK: The AND of following selected MATCHes is ORed with the result of TRIG0_OR. 0b1XXX = Selects MATCHA AND 0bX1XX = Selects MATCHB AND 0bXX1X = Selects MATCHC AND 0bXXX1 = Selects MATCHD AND 0b0000 = Selects to not AND any MATCHes together to form TRIG0.
18:21	RW	TRIG1_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG1_AND. 0b1XXX = Selects MATCHA OR 0bX1XX = Selects MATCHB OR 0bXX1X = Selects MATCHC OR 0bXXX1 = Selects MATCHD OR 0b0000 = Selects to not OR any MATCHes to form TRIG1.

Bits	SCOM	Field Mnemonic: Description
22:25	RW	TRIG1_AND_MASK: The AND of following selected MATCHes is ORed with the result of TRIG1_OR. 0b1XXX = Selects MATCHA AND 0bX1XX = Selects MATCHB AND 0bXX1X = Selects MATCHC AND 0bXXX1 = Selects MATCHD AND 0b0000 = Selects to not AND any MATCHes together to form TRIG1.
26	RW	TRIG0_NOT_MODE: Invert TRIG0 before using it.
27	RW	TRIG1_NOT_MODE: Invert TRIG1 before using it.
28:31	RW	MATCH_NOT_MODE: Invert the match polarity before using it to form a trigger. 0B1000 = Inverts MATCHA. 0b0100 = Inverts MATCHB. 0b0010 = Inverts MATCHC. 0b0001 = Inverts MATCHD.
32:35	RW	Reserved field.
36:39	RW	Reserved field.

Register Name	Trace Array High Data Register
Mnemonic	EX07.EC.C0.SD.TRA_01.TR.TR0.TRACE_HI_DATA_REG
Address	000000002E011C00 (SCOM)
Description	This register provides the high trace array data.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace array data 0:63.

Register Name	Trace Array Low Data Register
Mnemonic	EX07.EC.C0.SD.TRA_01.TR.TR0.TRACE_LO_DATA_REG
Address	000000002E011C01 (SCOM)
Description	This register provides the low trace array data.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace array data 64:95.
32:41	ROX	TRACE_ADDRESS: Trace address.
42:50	ROX	TRACE_LAST_BANK: Trace the last bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace the last valid bank.
52	ROX	TRACE_WRITE_ON_RUN: Trace the write-on-run indicator.
53	ROX	TRACE_RUNNING: Trace the run indicator.
54:63	ROX	TRACE_HOLD_ADDRESS: Trace the hold address (pointing to last entry).

Register Name	Trace Control Configuration Register
Mnemonic	EX07.EC.C0.SD.TRA_01.TR.TR0.TRACE_TRCTRL_CONFIG
Address	000000002E011C02 (SCOM)
Description	This register contains trace control configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	Reserved field.
1	RW	WRITE_ON_RUN_MODE: Write-on-run mode.
2:9	RW	EXTENDED_STORE_ON_TRIG_MODE: Extended trigger mode.
10	RW	BANK_MODE: Bank mode.
11	RW	ENH_TRACE_MODE: Enhanced trace mode.
12:13	RW	LCL_CLK_GATE_CTRL: Application note: Do not set lcl_clk_gate_ctrl to '00'; always keep at '11' as a workaround for incorrect clock gating.
14:21	RW	Reserved field.

Register Name	Trace Data Configuration Register 0
Mnemonic	EX07.EC.C0.SD.TRA_01.TR.TR0.TRACE_TRDATA_CONFIG_0
Address	000000002E011C03 (SCOM)
Description	This register contains a trace data compare mask for bits 0 – 63.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: Trace data compare mask for bits 0 to 63.

Register Name	Trace Data Configuration Register 1
Mnemonic	EX07.EC.C0.SD.TRA_01.TR.TR0.TRACE_TRDATA_CONFIG_1
Address	000000002E011C04 (SCOM)
Description	This register contains a trace data compare mask for bits 64 – 87.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: Trace data compare mask for bits 64 to 87.

Register Name	Trace Data Configuration Register 2
Mnemonic	EX07.EC.C0.SD.TRA_01.TR.TR0.TRACE_TRDATA_CONFIG_2
Address	000000002E011C05 (SCOM)
Description	This register contains patterns A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: pattern_match_pata_0_to_23.
24:47	RW	PATTERNB: pattern_match_patb_0_to_23.

Register Name	Trace Data Configuration Register 3
Mnemonic	EX07.EC.C0.SD.TRA_01.TR.TR0.TRACE_TRDATA_CONFIG_3
Address	000000002E011C06 (SCOM)
Description	This register contains patterns C and D.

Bits	SCOM	Field Mnemonic: Description

Bits	SCOM	Field Mnemonic: Description
24:47	RW	PATTERND: pattern_match_patd_0_to_23.

Register Name	Trace Data Configuration Register 4
Mnemonic	EX07.EC.C0.SD.TRA_01.TR.TR0.TRACE_TRDATA_CONFIG_4
Address	000000002E011C07 (SCOM)
Description	This register contains masks A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: mska.
24:47	RW	MASKB: mskb.

Register Name	Trace Data Configuration Register 5
Mnemonic	EX07.EC.C0.SD.TRA_01.TR.TR0.TRACE_TRDATA_CONFIG_5
Address	000000002E011C08 (SCOM)
Description	This register contains masks C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: mskc.
24:47	RW	MASKD: mskd.

Register Name	Trace Data Configuration Register 9
Mnemonic	EX07.EC.C0.SD.TRA_01.TR.TR0.TRACE_TRDATA_CONFIG_9
Address	000000002E011C09 (SCOM)
Description	This register contains trace data configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disable trace data compression (store data on every cycle).
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Take into account changes in the error bit for trace data compression (default = 0).
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.

Bits	SCOM	Field Mnemonic: Description
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 0b00 = Debug bus bits(00:23). 0b01 = Debug bus bits(24:47). 0b10 = Debug bus bits(48:71). 0b11 = Debug bus bits(72:87) | 8 zeroes.
10:13	RW	TRIG0_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG0_AND. 0b1XXX = Selects MATCHA OR 0bX1XX = Selects MATCHB OR 0bXX1X = Selects MATCHC OR 0bXXX1 = Selects MATCHD OR 0b0000 = Selects to not OR any MATCHes.
14:17	RW	TRIG0_AND_MASK: The AND of following selected MATCHes is ORed with the result of TRIG0_OR. 0b1XXX = Selects MATCHA AND 0bX1XX = Selects MATCHB AND 0bXX1X = Selects MATCHC AND 0bXXX1 = Selects MATCHD AND 0b0000 = Selects to not AND any MATCHes together to form TRIG0.
18:21	RW	TRIG1_OR_MASK: The OR of all selected MATCHes is ORed with the result of TRIG1_AND. 0b1XXX = Selects MATCHA OR 0bX1XX = Selects MATCHB OR 0bXX1X = Selects MATCHC OR 0bXXX1 = Selects MATCHD OR 0b0000 = Selects to not OR any MATCHes to form TRIG1.
22:25	RW	TRIG1_AND_MASK: The AND of following selected MATCHes is ORed with the result of TRIG1_OR. 0b1XXX = Selects MATCHA AND 0bX1XX = Selects MATCHB AND 0bXX1X = Selects MATCHC AND 0bXXX1 = Selects MATCHD AND 0b0000 = Selects to not AND any MATCHes together to form TRIG1.
26	RW	TRIG0_NOT_MODE: Invert TRIG0 before using it.
27	RW	TRIG1_NOT_MODE: Invert TRIG1 before using it.
28:31	RW	MATCH_NOT_MODE: Invert the match polarity before using it to form a trigger. 0b1000 = Inverts MATCHA. 0b0100 = Inverts MATCHB. 0b0010 = Inverts MATCHC. 0b0001 = Inverts MATCHD.
32:35	RW	Reserved field.
36:39	RW	Reserved field.

Register Name	Synchronous Configuration Register
Mnemonic	TP.TCEC14.CORE.SYNC_CONFIG
Address	000000002E030000 (SCOM)
Description	Configuration of CC counters.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	SYNC_PULSE_DELAY: Delay the incoming synchronous pulse. The default is 8 latches including asynchronous. 0000 = Delay by 8 latches (default). 0001 = Delay by 2 latches. 0010 = Delay by 3 latches. 0011 = Delay by 4 latches. 0100 = Delay by 5 latches. 0101 = Delay by 6 latches. 0110 = Delay by 7 latches. 0111 = Delay by 8 latches. 1000 = Delay by 9 latches. 1001 = Delay by 10 latches. 1010 = Delay by 11 latches. 1011 = Delay by 12 latches. 1100 = Delay by 13 latches. 1101 = Delay by 14 latches. 1110 = Delay by 15 latches. 1111 = Delay by 16 latches.
4	RW	LISTEN_TO_SYNC_PULSE_DIS: Disable phase counter synchronization by sync_pulse signal (default is enabled). Note: When listen_to_sync is enabled, the chiplet becomes corrupted for 200 cycles.
5	RW	SYNC_PULSE_INPUT_SEL: The default is 0. When set to 1, the alternative input of the sync_pulse will be used. Note: When toggling the input select, the chiplet becomes corrupted for 200 cycles.
6	RW	USE_SYNC_FOR_SCAN: When set, use OPCG initial alignment for scan requests.
7	RW	CLEAR_CHIPLET_IS_ALIGNED: This bit clears the chiplet_is_aligned bit. See the Chiplet Status Register.
8	RW	UNIT_REGION_CLKCMD_ENABLE: Enable the unit interface to start or stop one dedicated region. Used for POWER9 cache/core.

Bits	SCOM	Field Mnemonic: Description
9	RW	DISABLE_PCB_ITR: Disable interrupt generation within CC. Interrupt sent on each HLD event.
10	RW	ENABLE_VITL_ALIGN_CHECK: Enable the VITL align check to compare alignment of incoming synchronous pulse with 2:1 VITL LCB.
11	RW	SYNC_PULSE_OUT_DIS: Disables sync_pulse output when set to 1. The master chiplet will no longer send synchronous pulses to slave chiplets.
12:19	RW	UNUSED1219: Unused.

Register Name	OPCG Alignment Register
Mnemonic	TP.TCEC14.CORE.OPCG_ALIGN
Address	000000002E030001 (SCOM)
Description	OPCG align

Bits	SCOM	Field Mnemonic: Description
0:3	RW	INOP_ALIGN: INOP phase alignment: 0 = None 1 = 2:1 2 = 3:1 3 = 4:1 4 = 6:1 5 = 8:1 6 = 12:1 7 = 16:1 8 = 24:1 9-15 = 48:1
4:7	RW	SNOP_ALIGN: SNOP phase alignment: 0 = None 1 = 2:1 2 = 3:1 3 = 4:1 4 = 6:1 5 = 8:1 6 = 12:1 7 = 16:1 8 = 24:1 9-15 = 48:1
8:11	RW	ENOP_ALIGN: ENOP phase alignment: 0 = None 1 = 2:1 2 = 3:1 3 = 4:1 4 = 6:1 5 = 8:1 6 = 12:1 7 = 16:1 8 = 24:1 9-15 = 48:1
12:19	RW	INOP_WAIT: INOP cycle delay (0-255).
20:31	RW	SNOP_WAIT: SNOP cycle delay (0-4095).
32:39	RW	ENOP_WAIT: ENOP cycle delay (0-255).
40	RW	INOP_FORCE_SG: Set SG high during INOP.
41	RW	SNOP_FORCE_SG: Set SG high during SNOP.

Bits	SCOM	Field Mnemonic: Description
42	RW	ENOP_FORCE_SG: Set SG high during ENOP (including LOOP phase).
43	RW	NO_WAIT_ON_CLK_CMD: 0 = A clock change request will first wait the OPCG_WAIT cycles. 1 = A clock change request will not wait, when not in flush.
44:45	RW	ALIGN_SOURCE_SELECT: 0 = Use inopa setting from opcg_reg0. 1 = Use rising edge of synchronous pulse. 2 = Use unit0_sync_lvl to align (for AVP: refresh0). 3 = Use unit1_sync_lvl to align (for AVP: refresh1).
46	RW	UNUSED46: Unused.
47:51	RW	SCAN_RATIO: Scan ratio. The default is 4:1 = 00011. 0 to 15 = (n+1):1 16 = 24:1 17 = 32:1 18 = 48:1 19 = 64:1 20 = 128:1
52:63	RW	OPCG_WAIT_CYCLES: Old PAD value; delay at the beginning and end of the OPCG run, to allow DC signals to be there at the right time (0-4095). The default is 0x020. Note: Must be higher than plat depth.

Register Name	OPCG Control 0 Register
Mnemonic	TP.TCEC14.CORE.OPCG_REG0
Address	000000002E030002 (SCOM)
Description	OPCG control register 0

Bits	SCOM	Field Mnemonic: Description
0	RW	RUNN_MODE: 0 = BIST-mode; used for LBIST. 1 = RUNN-mode; used for ABIST/IOBIST.
1	RWX	OPCG_GO: Start OPCG. The bit is cleared when OPCG completes. Poll for opcg_done in the Chiplet Status Register.
2	RWX	RUN_SCAN0: Run scan0 (overrides all BIST mode settings but the scan_ratio). Starts a scan0 run, and the bit is cleared when OPCG is done. Poll for opcg_done in the Chiplet Status Register.
3	RW	SCAN0_MODE: Sets PRPGs in scan0_mode but does not run the automatic scan0 sequence.
4	RWX	OPCG_IN_SLAVE_MODE: When selected, OPCG waits for the master chiplet to get started. When Keep_MS_Mode is 0, SLAVE_MODE is cleared after the incoming trigger.
5	RWX	OPCG_IN_MASTER_MODE: When selected, OPCG sends out a trigger to all slave chiplets. When Keep_MS_Mode is 0, MASTER_MODE is cleared after sending out one master trigger.
6	RW	KEEP_MS_MODE: When set to 1, OPCG in master and slave mode bits are not cleared after one incoming OPCG trigger. The default is to clear master and slave mode bits.
7	RW	TRIGGER_OPCG_ON_UNIT0_SYNC_LVL: Unit pin used for AVP can trigger OPCG (unit0_sync_lvl).
8	RW	TRIGGER_OPCG_ON_UNIT1_SYNC_LVL: Unit pin used for AVP can trigger OPCG (unit1_sync_lvl).
9	RWX	RUN_CHIPLET_SCAN0: Run scan0 on all regions and types; clears the chiplet at all regions and types.
10	RWX	RUN_CHIPLET_SCAN0_NO_PLL: Run scan0 on all regions and types; clears the chiplet at all exclude-PLL regions. PLL can continue to run.

Bits	SCOM	Field Mnemonic: Description
11	RW	RUN_OPCG_ON_UPDATE_DR: Start the OPCG engine when scan update (update_dr) is received (set pulse) Cronus requires this bit to be set at 1 for a set pulse WRITE.
12	RW	RUN_OPCG_ON_CAPTURE_DR: Start the OPCG engine when scan update (capture_dr) is received (set pulse). Cronus requires this bit to be set at 1 for a set pulse READ.
13	RW	STOP_RUNN_ON_XSTOP: RUNN mode. Stops RUNN on checkstop.
14	RW	OPCG_STARTS_BIST: RUNN mode. The OPCG engine controls start_bist for ABIST or IOBIST (see the BIST Register).
15:20	RW	UNUSED1520: Unused.
21:63	RWX	LOOP_COUNT: Loop counter for LBIST and RUNN. write = Target value. read = Current counter value. Counts from 0 to the target value.

Register Name	**OPCG Control 1 Register**
Mnemonic	TP.TCEC14.CORE.OPCG_REG1
Address	000000002E030003 (SCOM)
Description	OPCG control register 1

Bits	SCOM	Field Mnemonic: Description
0:11	RW	SCAN_COUNT: BIST mode: Channel scan count (s = 0-4095) RUNN-mode: start_bist match value (0:11)
12:23	RW	MISR_A_VAL: BIST mode: a value for MISR aperture RUNN-mode: start_bist match value (12:23)
24:35	RW	MISR_B_VAL: BIST mode: b value for MISR aperture RUNN-mode: start_bist match value (24:35)
36:47	RW	MISR_INIT_WAIT: BIST mode: delay MISR aperture; MISRs become active after this number of loops.
48	RW	OPCG_SUPPRESS_EVEN_CLK: OPCG creates only even, and not odd, clocks. Used for RUNN to create only one clock in fast domain. The default is 0.
49	RW	SCAN_CLK_USE_EVEN: Generate scan clock in even cycle instead of odd cycle. The default is 0 (odd cycle).
50:51	RW	UNUSED2: Unused.
52	RW	RTIM_THOLD_FORCE: Force rtim_thold low when not in test_dc mode (must be 0 at all times).
53	RW	DISABLE_ARY_CLK_DURING_FILL: LBIST and SCAN0. Prevent the firing of the ARY HLD bit during NSL fill.
54	RW	SG_HIGH_DURING_FILL: LBIST and SCAN0: Hold SG high during NSL fill.
55:56	RW	LBIST_SKITTER_CTL: BIST mode: 00 = Enable skitter during lbist_ip 01 = Enable skitter when misr_active; see misr_init_wait 10 = Skitter OPCG_GO mode; falling edge = start, rising edge = stop 11 = Unused
57	RW	MISR_MODE: BIST mode. MISR aperture mode (0: a-1 to b-1, 1: start to a and b to end).
58	RW	INFINITE_MODE: Infinite mode. RUNN and LBIST will run indefinitely and ignore the loop count.
59:63	RW	NSL_FILL_COUNT: BIST mode. NSL-fill count (0-31).

Register Name	OPCG Control 2 Register
Mnemonic	TP.TCEC14.CORE.OPCG_REG2
Address	000000002E030004 (SCOM)
Description	OPCG control register 2

Bits	SCOM	Field Mnemonic: Description
0	RWX	OPCG_GO2: Start OPCG for broadcast sequences (start sequence).
1:3	RW	PRPG_WEIGHTING: prpg_activate: 1/2, 1/4, 1/8, 1/16, 1/2, 3/4, 7/8, 15/16.
4:15	RWX	PRPG_VALUE: Set to 0 to keep PRPG always on, else seed.
16:27	RW	PRPG_A_VAL: a value for PRPG aperture.
28:39	RW	PRPG_B_VAL: b value for PRPG aperture.
40	RW	PRPG_MODE: PRPG aperture mode (0: a-1 to b-1, 1: start to a and b to end).
41:63	RW	UNUSED41_63: Unused.

Register Name	Scan Region and Type Register
Mnemonic	TP.TCEC14.CORE.SCAN_REGION_TYPE
Address	000000002E030005 (SCOM)
Description	Sets the scan region and type.

Bits	SCOM	Field Mnemonic: Description
0	RWX	SYSTEM_FAST_INIT: Default is 0. When set to 1, the MASK bits in the CMSK chain govern which part will be scanned or scan0. MASK = 1: scan0. MASK = 0: Partial or scan chain.
1:2	RO	constant = 0b00
3	NCX	SCAN_REGION_VITL: Scan clock region VITL (vital = clock).
4	RWX	SCAN_REGION_PERV: Scan clock region perv (pervasive).
5	RWX	SCAN_REGION_UNIT1: Scan clock region c00 (LSU, IFU, PC).
6	RWX	SCAN_REGION_UNIT2: Scan clock region c01 (ISU, VSU).
7	RWX	SCAN_REGION_UNIT3: Scan clock region unused.
8	RWX	SCAN_REGION_UNIT4: Scan clock region unused.
9	RWX	SCAN_REGION_UNIT5: Scan clock region unused.
10	RWX	SCAN_REGION_UNIT6: Scan clock region unused.
11	RWX	SCAN_REGION_UNIT7: Scan clock region unused.
12	RWX	SCAN_REGION_UNIT8: Scan clock region unused.
13	RWX	SCAN_REGION_UNIT9: Scan clock region unused.
14	RWX	SCAN_REGION_UNIT10: Scan clock region unused.
15:47	RO	constant = 0b000000000000000000000000000000000
48	RW	SCAN_TYPE_FUNC: Scan chain is functional.
49	RW	SCAN_TYPE_CFG: Scan chain mode (boot configuration and debug configuration).
50	RW	SCAN_TYPE_CCFG_GPTR: Scan chain ccfg / gptr (pervasive: CC configuration; others: GPTR).

Bits	SCOM	Field Mnemonic: Description
51	RW	SCAN_TYPE_REGF: Scan chain regf (register files).
52	RW	SCAN_TYPE_LBIST: Scan chain lbst (LBIST).
53	RW	SCAN_TYPE_ABIST: Scan chain abst (ABIST).
54	RW	SCAN_TYPE_REPR: Scan chain repr (array repair).
55	RW	SCAN_TYPE_TIME: Scan chain time (array timing).
56	RW	SCAN_TYPE_BNDY: Scan chain bndy (boundary IOs).
57	RW	SCAN_TYPE_FARR: Scan chain farr (fast array unload).
58	RW	SCAN_TYPE_CMSK: Scan chain cmsk (LBIST channel mask).
59	RW	SCAN_TYPE_INEX: Scan chain idex (c14 ASIC).
60:63	RO	constant = 0b0000

Register Name	Clock Region Register
Mnemonic	TP.TCEC14.CORE.CLK_REGION
Address	000000002E030006 (SCOM)
Description	Start and stop clocks.

Bits	SCOM	Field Mnemonic: Description
0:1	RWX	CLOCK_CMD: Command for clock control: 00 = NOP 01 = Start 10 = Stop 11 = Pulse (one pulse)
2	RWX	SLAVE_MODE: When selected, the clock command waits for the master chiplet to start. The bit is cleared after the incoming slave trigger and Keep_MS_Mode_after_trigger is set to 0.
3	RWX	MASTER_MODE: When selected, the clock command sends out a trigger to all slave chiplets. The bit is cleared after sending out one master trigger and Keep_MS_Mode_after_trigger is set to 0.
4	RWX	CLOCK_REGION_PERV: For clock region perv (pervasive).
5	RWX	CLOCK_REGION_UNIT1: For clock region c00 (LSU, IFU, PC).
6	RWX	CLOCK_REGION_UNIT2: For clock region c01 (ISU, VSU).
7	RWX	CLOCK_REGION_UNIT3: For clock region unused.
8	RWX	CLOCK_REGION_UNIT4: For clock region unused.
9	RWX	CLOCK_REGION_UNIT5: For clock region unused.
10	RWX	CLOCK_REGION_UNIT6: For clock region unused.
11	RWX	CLOCK_REGION_UNIT7: For clock region unused.
12	RWX	CLOCK_REGION_UNIT8: For clock region unused.
13	RWX	CLOCK_REGION_UNIT9: For clock region unused.
14	RWX	CLOCK_REGION_UNIT10: For clock region unused.
15:47	RO	constant = 0b000000000000000000000000000000000
48	RWX	SEL_THOLD_SL: Select SL tholds.
49	RWX	SEL_THOLD_NSL: Select NSL tholds.
50	RWX	SEL_THOLD_ARY: Select array thold.

Bits	SCOM	Field Mnemonic: Description
51	RO	constant = 0b0
52	RW	CLOCK_PULSE_USE_EVEN: For dual mesh support. The default for pulse is ODD phase. When this bit is set, pulse is applied on EVEN phase.
53:63	RO	constant = 0b00000000000

Register Name	Clock Status SL Register
Mnemonic	TP.TCEC14.CORE.CLOCK_STAT_SL
Address	000000002E030008 (SCOM)
Description	Clocks running SL.

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b1111
4	ROX	CLOCK_STATUS_PERV_SL: Status of pervasive SL HLD. 0 = Run. 1 = Stop.
5	ROX	CLOCK_STATUS_UNIT1_SL: Status of c00 (LSU, IFU, PC SL HLD). 0 = Run. 1 = Stop.
6	ROX	CLOCK_STATUS_UNIT2_SL: Status of c01 (ISU, VSU SL HLD). 0 = Run. 1 = Stop.
7	ROX	CLOCK_STATUS_UNIT3_SL: Status of unused SL HLD. 0 = Run. 1 = Stop.
8	ROX	CLOCK_STATUS_UNIT4_SL: Status of unused SL HLD. 0 = Run. 1 = Stop.
9	ROX	CLOCK_STATUS_UNIT5_SL: Status of unused SL HLD. 0 = Run. 1 = Stop.
10	ROX	CLOCK_STATUS_UNIT6_SL: Status of unused SL HLD. 0 = Run. 1 = Stop.
11	ROX	CLOCK_STATUS_UNIT7_SL: Status of unused SL HLD. 0 = Run. 1 = Stop.
12	ROX	CLOCK_STATUS_UNIT8_SL: Status of unused SL HLD. 0 = Run. 1 = Stop.
13	ROX	CLOCK_STATUS_UNIT9_SL: Status of unused SL HLD. 0 = Run. 1 = Stop.
14	ROX	CLOCK_STATUS_UNIT10_SL: Status of unused SL HLD. 0 = Run. 1 = Stop.
15:63	RO	constant = 0b1111111111111111111111111111111111111111111111111

Register Name	Clock Status NSL Register
Mnemonic	TP.TCEC14.CORE.CLOCK_STAT_NSL
Address	000000002E030009 (SCOM)
Description	Clocks running NSL.

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b1111
4	ROX	CLOCK_STATUS_PERV_NSL: Status of pervasive NSL HLD. 0 = Run. 1 = Stop.
5	ROX	CLOCK_STATUS_UNIT1_NSL: Status of c00 (LSU, IFU, PC NSL HLD). 0 = Run. 1 = Stop.
6	ROX	CLOCK_STATUS_UNIT2_NSL: Status of c01 (ISU, VSU NSL HLD). 0 = Run. 1 = Stop.
7	ROX	CLOCK_STATUS_UNIT3_NSL: Status of unused NSL HLD. 0 = Run. 1 = Stop.
8	ROX	CLOCK_STATUS_UNIT4_NSL: Status of unused NSL HLD. 0 = Run. 1 = Stop.
9	ROX	CLOCK_STATUS_UNIT5_NSL: Status of unused NSL HLD. 0 = Run. 1 = Stop.
10	ROX	CLOCK_STATUS_UNIT6_NSL: Status of unused NSL HLD. 0 = Run. 1 = Stop.
11	ROX	CLOCK_STATUS_UNIT7_NSL: Status of unused NSL HLD. 0 = Run. 1 = Stop.
12	ROX	CLOCK_STATUS_UNIT8_NSL: Status of unused NSL HLD. 0 = Run. 1 = Stop.
13	ROX	CLOCK_STATUS_UNIT9_NSL: Status of unused NSL HLD. 0 = Run. 1 = Stop.
14	ROX	CLOCK_STATUS_UNIT10_NSL: Status of unused NSL HLD. 0 = Run. 1 = Stop.
15:63	RO	constant = 0b1111111111111111111111111111111111111111111111111

Register Name	Clock Status Array Register
Mnemonic	TP.TCEC14.CORE.CLOCK_STAT_ARY
Address	000000002E03000A (SCOM)
Description	Clocks running ARY.

Bits	SCOM	Field Mnemonic: Description
0:3	RO	constant = 0b1111
4	ROX	CLOCK_STATUS_PERV_ARY: Status of pervasive ARY HLD. 0 = Run. 1 = Stop.
5	ROX	CLOCK_STATUS_UNIT1_ARY: Status of c00 (LSU, IFU, PC ARY HLD). 0 = Run. 1 = Stop.
6	ROX	CLOCK_STATUS_UNIT2_ARY: Status of c01 (ISU, VSU ARY HLD). 0 = Run. 1 = Stop.

Bits	SCOM	Field Mnemonic: Description
7	ROX	CLOCK_STATUS_UNIT3_ARY: Status of unused ARY HLD. 0 = Run. 1 = Stop.
8	ROX	CLOCK_STATUS_UNIT4_ARY: Status of unused ARY HLD. 0 = Run. 1 = Stop.
9	ROX	CLOCK_STATUS_UNIT5_ARY: Status of unused ARY HLD. 0 = Run. 1 = Stop.
10	ROX	CLOCK_STATUS_UNIT6_ARY: Status of unused ARY HLD. 0 = Run. 1 = Stop.
11	ROX	CLOCK_STATUS_UNIT7_ARY: Status of unused ARY HLD. 0 = Run. 1 = Stop.
12	ROX	CLOCK_STATUS_UNIT8_ARY: Status of unused ARY HLD. 0 = Run. 1 = Stop.
13	ROX	CLOCK_STATUS_UNIT9_ARY: Status of unused ARY HLD. 0 = Run. 1 = Stop.
14	ROX	CLOCK_STATUS_UNIT10_ARY: Status of unused ARY HLD. 0 = Run. 1 = Stop.
15:63	RO	constant = 0b1111111111111111111111111111111111111111111111111

Register Name	ABIST and IOBIST Register
Mnemonic	TP.TCEC14.CORE.BIST
Address	000000002E03000B (SCOM)
Description	ABIST and IOBIST per region

Bits	SCOM	Field Mnemonic: Description
0	RW	TC_BIST_START_TEST_DC: Keep this at 0 during ABIST/IOBIST. It can be used to bypass the RUNN start. When this bit is set, the BIST_START_TEST goes high immediately without waiting for RUNN. BIST starts with the first HLD clock cycle.
1	RW	TC_SRAM_ABIST_MODE_DC: Select the ABIST engines for SRAMs.
2	RW	TC_EDRAM_ABIST_MODE_DC: Select the ABIST engines for EDRAMs.
3	RW	TC_IOBIST_MODE_DC: Select the IOBIST engines.
4	RW	BIST_PERV: Region pervasive: 1 = BIST_START_TEST for this region is triggered. 0 = The region is not part of the ABIST/IOBIST run.
5	RW	BIST_UNIT1: Region c00 (LSU, IFU, PC): 1 = BIST_START_TEST for this region is triggered. 0 = The region is not part of the ABIST/IOBIST run.
6	RW	BIST_UNIT2: Region c01 (ISU, VSU): 1 = BIST_START_TEST for this region is triggered. 0 = The region is not part of the ABIST/IOBIST run.

Bits	SCOM	Field Mnemonic: Description
7	RW	BIST_UNIT3: Region unused: 1 = BIST_START_TEST for this region is triggered. 0 = The region is not part of the ABIST/IOBIST run.
8	RW	BIST_UNIT4: Region unused: 1 = BIST_START_TEST for this region is triggered. 0 = The region is not part of the ABIST/IOBIST run.
9	RW	BIST_UNIT5: Region unused: 1 = BIST_START_TEST for this region is triggered. 0 = The region is not part of the ABIST/IOBIST run.
10	RW	BIST_UNIT6: Region unused: 1 = BIST_START_TEST for this region is triggered. 0 = The region is not part of the ABIST/IOBIST run.
11	RW	BIST_UNIT7: Region unused: 1 = BIST_START_TEST for this region is triggered. 0 = The region is not part of the ABIST/IOBIST run.
12	RW	BIST_UNIT8: Region unused: 1 = BIST_START_TEST for this region is triggered. 0 = The region is not part of the ABIST/IOBIST run.
13	RW	BIST_UNIT9: Region unused: 1 = BIST_START_TEST for this region is triggered. 0 = The region is not part of the ABIST/IOBIST run.
14	RW	BIST_UNIT10: Region unused: 1 = BIST_START_TEST for this region will be triggered. 0 = The region is not part of the ABIST/IOBIST run.
15:47	RO	constant = 0b000000000000000000000000000000000
48	RW	BIST_STROBE_WINDOW_EN: Enable strobe window only in TE = 1 mode. The OPCGGO tester pin enables the ABIST compare, once ABIST has been started. Special setup in the ABIST engine is required. The default is 0. System mode cannot enable this feature.
49:63	RO	constant = 0b000000000000000

Register Name	Checkstop 1 Register
Mnemonic	TP.TCEC14.CORE.XSTOP1
Address	000000002E03000C (SCOM)
Description	Checkstop per region

Bits	SCOM	Field Mnemonic: Description
0	RW	XSTOP1_MASK_B: Mask for checkstop to clockstop of select regions. (See xstop_perv, xstop_unit0..n.) 0 = Ignore checkstop. 1 = Stop on checkstop.
1	RW	XSTOP1_UNUSED: Unused.
2	RW	TRIGGER_OPCG_ON_XSTOP1: Trigger OPCG on checkstop instead of performing clockstop.
3	RW	XSTOP1_WAIT_ALLWAYS: When set to 1, checkstop waits independently of flush. The default is to not wait when flush is not set.
4	RW	XSTOP1_PERV: Region perv: 1 = The region is stopped. 0 = The region continues to run on checkstop.

Bits	SCOM	Field Mnemonic: Description
5	RW	XSTOP1_UNIT1: Region c00 (LSU, IFU, PC): 1 = The region is stopped. 0 = The region continues to run on checkstop.
6	RW	XSTOP1_UNIT2: Region c01 (ISU, VSU): 1 = The region is stopped. 0 = The region continues to run on checkstop.
7	RW	XSTOP1_UNIT3: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
8	RW	XSTOP1_UNIT4: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
9	RW	XSTOP1_UNIT5: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
10	RW	XSTOP1_UNIT6: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
11	RW	XSTOP1_UNIT7: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
12	RW	XSTOP1_UNIT8: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
13	RW	XSTOP1_UNIT9: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
14	RW	XSTOP1_UNIT10: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
15:47	RO	constant = 0b000000000000000000000000000000000
48:59	RW	XSTOP1_WAIT_CYCLES: Specifies how many cycles checkstop waits (0 - 4095) after dropping flush before tholds are dropped.
60:63	RO	constant = 0b0000

Register Name	**Checkstop 2 Register**
Mnemonic	TP.TCEC14.CORE.XSTOP2
Address	000000002E03000D (SCOM)
Description	Checkstop per region

Bits	SCOM	Field Mnemonic: Description
0	RW	XSTOP2_MASK_B: Mask for checkstop to clockstop of select regions (see xstop_perv, xstop_unit0..n). 0 = Ignore checkstop 1 = Stop on checkstop
1	RW	XSTOP2_UNUSED: Unused.
2	RW	TRIGGER_OPCG_ON_XSTOP2: Trigger OPCG on checkstop instead of performing clockstop.
3	RW	XSTOP2_WAIT_ALLWAYS: When set to 1, checkstop waits independently of flush. The default is to not wait when flush is not set.

Bits	SCOM	Field Mnemonic: Description
4	RW	XSTOP2_PERV: Region perv: 1 = The region is stopped. 0 = The region continues to run on checkstop.
5	RW	XSTOP2_UNIT1: Region c00 (LSU, IFU, PC): 1 = The region is stopped. 0 = The region continues to run on checkstop.
6	RW	XSTOP2_UNIT2: Region c01 (ISU, VSU): 1 = The region is stopped. 0 = The region continues to run on checkstop.
7	RW	XSTOP2_UNIT3: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
8	RW	XSTOP2_UNIT4: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
9	RW	XSTOP2_UNIT5: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
10	RW	XSTOP2_UNIT6: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
11	RW	XSTOP2_UNIT7: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
12	RW	XSTOP2_UNIT8: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
13	RW	XSTOP2_UNIT9: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
14	RW	XSTOP2_UNIT10: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
15:47	RO	constant = 0b000000000000000000000000000000000
48:59	RW	XSTOP2_WAIT_CYCLES: Specifies how many cycles checkstop waits (0 - 4095) after dropping flush before tholds are dropped.
60:63	RO	constant = 0b0000

Register Name	Checkstop 3 Register
Mnemonic	TP.TCEC14.CORE.XSTOP3
Address	000000002E03000E (SCOM)
Description	Checkstop per region

Bits	SCOM	Field Mnemonic: Description
0	RW	XSTOP3_MASK_B: Mask for checkstop to clockstop of select regions. (See xstop_perv, xstop_unit0..n). 0 = Ignore checkstop. 1 = Stop on checkstop.
1	RW	XSTOP3_UNUSED: Unused.

Bits	SCOM	Field Mnemonic: Description
2	RW	TRIGGER_OPCG_ON_XSTOP3: Trigger OPCG on checkstop instead of performing clockstop.
3	RW	XSTOP3_WAIT_ALLWAYS: When set to 1, checkstop waits independently of flush. The default is to not wait when flush is not set.
4	RW	XSTOP3_PERV: Region perv: 1 = The region is stopped. 0 = The region continues to run on checkstop.
5	RW	XSTOP3_UNIT1: Region c00 (LSU, IFU, PC): 1 = The region is stopped. 0 = The region continues to run on checkstop.
6	RW	XSTOP3_UNIT2: Region c01 (ISU, VSU): 1 = The region is stopped. 0 = The region continues to run on checkstop.
7	RW	XSTOP3_UNIT3: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
8	RW	XSTOP3_UNIT4: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
9	RW	XSTOP3_UNIT5: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
10	RW	XSTOP3_UNIT6: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
11	RW	XSTOP3_UNIT7: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
12	RW	XSTOP3_UNIT8: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
13	RW	XSTOP3_UNIT9: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
14	RW	XSTOP3_UNIT10: Region unused: 1 = The region is stopped. 0 = The region continues to run on checkstop.
15:47	RO	constant = 0b000000000000000000000000000000000
48:59	RW	XSTOP3_WAIT_CYCLES: Specifies how many cycles checkstop waits (0 - 4095) after dropping flush before tholds are dropped.
60:63	RO	constant = 0b0000

Register Name	**Error Status Register**
Mnemonic	TP.TCEC14.CORE.ERROR_STATUS
Address	000000002E03000F (SCOM)
Description	Error status of the CC.

Bits	SCOM	Field Mnemonic: Description
0	RWX	PCB_WRITE_NOT_ALLOWED_ERR: A write was attempted on a read only register.

Bits	SCOM	Field Mnemonic: Description
1	RWX	PCB_READ_NOT_ALLOWED_ERR: A read is not allowed; the register might be write only.
2	RWX	PCB_PARITY_ON_CMD_ERR: A parity error on the command.
3	RWX	PCB_ADDRESS_NOT_VALID_ERR: Invalid address.
4	RWX	PCB_PARITY_ON_ADDR_ERR: Parity error on the address.
5	RWX	PCB_PARITY_ON_DATA_ERR: Parity error on data.
6	RWX	PCB_PROTECTED_ACCESS_INVALID_ERR: Protection violation.
7	RWX	PCB_PARITY_ON_SPCIF_ERR: Parity error on SPCIF.
8	RWX	PCB_WRITE_AND_OPCG_IP_ERR: A PCB write was attempted while OPCG is running.
9	RWX	SCAN_READ_AND_OPCG_IP_ERR: A scan read was attempted while OPCG is running.
10	RWX	CLOCK_CMD_CONFLICT_ERR: A clock command is in progress.
11	RWX	SCAN_COLLISION_ERR: Scan region was selected on a running region.
12	RWX	PREVENTED_SCAN_COLLISION_ERR: PCB request to set a scan region that is running.
13	RWX	OPCG_TRIGGER_ERR: OPCG was triggered while OPCG is running.
14	RWX	PHASE_CNT_CORRUPTION_ERR: The phase counters inside the chiplet are out of sync.
15	RWX	CLOCK_CMD_PREVENTED_ERR: Security or scan collision prevented a clock start.
16	RWX	PARITY_ON_OPCG_SM_ERR: Parity error on the OPCG state machine.
17	RWX	PARITY_ON_CLOCK_MUX_REG_ERR: Parity error on scan/clock region/type or clock status register.
18	RWX	PARITY_ON_OPCG_REG_ERR: Parity error on OPCG registers.
19	RWX	PARITY_ON_SYNC_CONFIG_REG_ERR: Parity error on sync configuration register.
20	RWX	PARITY_ON_XSTOP_REG_ERR: Parity error on checkstop register.
21	RWX	PARITY_ON_GPIO_REG_ERR: Parity error on GP0,4,5,6 registers.
22	RWX	CLKCMD_REQUEST_ERR: Region clkcmd has one request pending but received a second one.
23	RWX	CBS_PROTOCOL_ERR: CBS protocol error. The REQ / ACK sequence is wrong.
24	RWX	VITL_ALIGN_ERR: VITL alignment is out of sync to the sync pulse.
25	RWX	UNIT_SYNC_LVL_ERR: Unit0 and Unit1 sync lvl pulse are not in sync. AVP is broken.
26	RWX	PARITY_ON_SELFBOOT_CMD_STATE_ERR: Parity error on SELFBOOT command state.
27	RWX	UNUSED_ERROR27: Unused.
28	RWX	UNUSED_ERROR28: Unused.
29	RWX	UNUSED_ERROR29: Unused.
30	RWX	UNUSED_ERROR30: Unused.
31	RWX	UNUSED_ERROR31: Unused.

Register Name	OPCG Capture 1 Register
Mnemonic	TP.TCEC14.CORE.OPCG_CAPT1
Address	000000002E030010 (SCOM)
Description	OPCG capture 1 control.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	COUNT: 0000 = 12 cycles 0001 – 1100 = Cycles 1-12 1101-1111 = 24 cycles for normal, slow regions
4:8	RW	SEQ_01: Sequence cycle 1 for normal/slow region (SL, NSL, ARY, SE, FCE).
9:13	RW	SEQ_02: Sequence cycle 2 for normal/slow region (SL, NSL, ARY, SE, FCE).
14:18	RW	SEQ_03: Sequence cycle 3 for normal/slow region (SL, NSL, ARY, SE, FCE).
19:23	RW	SEQ_04: Sequence cycle 4 for normal/slow region (SL, NSL, ARY, SE, FCE).
24:28	RW	SEQ_05: Sequence cycle 5 for normal/slow region (SL, NSL, ARY, SE, FCE).
29:33	RW	SEQ_06: Sequence cycle 6 for normal/slow region (SL, NSL, ARY, SE, FCE).
34:38	RW	SEQ_07: Sequence cycle 7 for normal/slow region (SL, NSL, ARY, SE, FCE).
39:43	RW	SEQ_08: Sequence cycle 8 for normal/slow region (SL, NSL, ARY, SE, FCE).
44:48	RW	SEQ_09: Sequence cycle 9 for normal/slow region (SL, NSL, ARY, SE, FCE).
49:53	RW	SEQ_10: Sequence cycle 10 for normal/slow region (SL, NSL, ARY, SE, FCE).
54:58	RW	SEQ_11: Sequence cycle 11 for normal/slow region (SL, NSL, ARY, SE, FCE).
59:63	RW	SEQ_12: Sequence cycle 12 for normal/slow region (SL, NSL, ARY, SE, FCE).

Register Name	OPCG Capture 2 Register
Mnemonic	TP.TCEC14.CORE.OPCG_CAPT2
Address	000000002E030011 (SCOM)
Description	OPCG control capture 2.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	UNUSED_CAPT2:
4:8	RW	SEQ_13_01EVEN: Sequence cycle 1 is even for fast region or cycle 13 for normal region (SL, NSL, ARY, SE, FCE).
9:13	RW	SEQ_14_01ODD: Sequence cycle 1 is odd for fast region or cycle 14 for normal region (SL, NSL, ARY, SE, FCE).
14:18	RW	SEQ_15_02EVEN: Sequence cycle 2 is even for fast region or cycle 15 for normal region (SL, NSL, ARY, SE, FCE).
19:23	RW	SEQ_16_02ODD: Sequence cycle 2 is odd for fast region or cycle 16 for normal region (SL, NSL, ARY, SE, FCE).
24:28	RW	SEQ_17_03EVEN: Sequence cycle 3 is even for fast region or cycle 17 for normal region (SL, NSL, ARY, SE, FCE).
29:33	RW	SEQ_18_03ODD: Sequence cycle 3 is odd for fast region or cycle 18 for normal region (SL, NSL, ARY, SE, FCE).
34:38	RW	SEQ_19_04EVEN: Sequence cycle 4 is even for fast region or cycle 19 for normal region (SL, NSL, ARY, SE, FCE).
39:43	RW	SEQ_20_04ODD: Sequence cycle 4 is odd for fast region or cycle 20 for normal region (SL, NSL, ARY, SE, FCE).
44:48	RW	SEQ_21_05EVEN: Sequence cycle 5 is even for fast region or cycle 21 for normal region (SL, NSL, ARY, SE, FCE).
49:53	RW	SEQ_22_05ODD: Sequence cycle 5 is odd for fast region or cycle 22 for normal region (SL, NSL, ARY, SE, FCE).

Bits	SCOM	Field Mnemonic: Description
54:58	RW	SEQ_23_06EVEN: Sequence cycle 6 is even for fast region or cycle 23 for normal region (SL, NSL, ARY, SE, FCE).
59:63	RW	SEQ_24_06ODD: Sequence cycle 6 is odd for fast region or cycle 24 for normal region (SL, NSL, ARY, SE, FCE).

Register Name	OPCG Capture 3 Register
Mnemonic	TP.TCEC14.CORE.OPCG_CAPT3
Address	000000002E030012 (SCOM)
Description	OPCG control capture 3.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	UNUSED_CAPT3:
4:8	RW	SEQ_07EVEN: Sequence cycle 7 is even for fast region (SL, NSL, ARY, SE, FCE).
9:13	RW	SEQ_07ODD: Sequence cycle 7 is odd for fast region (SL, NSL, ARY, SE, FCE).
14:18	RW	SEQ_08EVEN: Sequence cycle 8 is even for fast region (SL, NSL, ARY, SE, FCE).
19:23	RW	SEQ_08ODD: Sequence cycle 8 is odd for fast region (SL, NSL, ARY, SE, FCE).
24:28	RW	SEQ_09EVEN: Sequence cycle 9 is even for fast region (SL, NSL, ARY, SE, FCE).
29:33	RW	SEQ_09ODD: Sequence cycle 9 is odd for fast region (SL, NSL, ARY, SE, FCE).
34:38	RW	SEQ_10EVEN: Sequence cycle 10 is even for fast region (SL, NSL, ARY, SE, FCE).
39:43	RW	SEQ_10ODD: Sequence cycle 10 is odd for fast region (SL, NSL, ARY, SE, FCE).
44:48	RW	SEQ_11EVEN: Sequence cycle 11 is even for fast region (SL, NSL, ARY, SE, FCE).
49:53	RW	SEQ_11ODD: Sequence cycle 11 is odd for fast region (SL, NSL, ARY, SE, FCE).
54:58	RW	SEQ_12EVEN: Sequence cycle 12 is even for fast region (SL, NSL, ARY, SE, FCE).
59:63	RW	SEQ_12ODD: Sequence cycle 12 is odd for fast region (SL, NSL, ARY, SE, FCE).

Register Name	Debug CBS CC Register
Mnemonic	TP.TCEC14.CORE.DBG_CBS_CC
Address	000000002E030013 (SCOM)
Description	Debug CBS CC Register

Bits	SCOM	Field Mnemonic: Description
0	ROX	DBG_RESET_EP: Reset endpoint.
1	ROX	DBG_OPCG_IP: OPCG in progress, not in idle state.
2	ROX	DBG_VITL_CLKOFF: VITL HLD stopped. When enabled, plat-depth cycles are needed to switch this latch.
3	ROX	DBG_TEST_ENABLE: Test enable.
4	ROX	DBG_CBS_REQ: CBS Interface. Request (latched).
5:7	ROX	DBG_CBS_CMD: CBS Interface. Command (latched).
8:12	ROX	DBG_CBS_STATE: CBS Command State Machine; 00000 = Idle.
13	ROX	DBG_SECURITY_DEBUG_MODE: Status of the security mode bit.

Bits	SCOM	Field Mnemonic: Description
14	ROX	DBG_CBS_PROTOCOL_ERROR: CBS protocol error. Request raised, although state machine is not in idle state. Need reset_ep to clear this bit. No impact on IPL.
15	ROX	DBG_PCB_IDLE: PCB Interface in idle state.
16:19	ROX	DBG_CURRENT_OPCG_MODE: The current (latest) OPCG mode: 0 = NOP 1 = LBIST 2 = ABIST 3 = RUNN 4 = SCAN0 5 = SCAN 6 = SCAN rotate 7 = SCAN with UpdateDR 8 = SCAN with CaptureDR 9 = CLK Change Request 10-15 = Unused
20:23	ROX	DBG_LAST_OPCG_MODE: Previous OPCG mode.
24	ROX	DBG_PCB_ERROR: PCB interface error. Read the CC error register or set CBS_CMD = 001 to switch the FSI CBS debug information to the CC error register.
25	ROX	DBG_PARITY_ERROR: Any parity error, non-PCB parity. Read the CC error register or set CBS_CMD = 001 to switch the FSI CBS debug information to the CC error register.
26	ROX	DBG_CC_ERROR: Any other CC error. Read the CC error register or set CBS_CMD = 001 to switch the FSI CBS debug information to the CC error register.
27	ROX	DBG_CHIPLET_IS_ALIGNED: Set to 1 when a valid align pulse was sent out.
28	ROX	DBG_PCB_REQUEST_SINCE_RESET: Reset clears this bit, and the first PCB request sets it.
29	ROX	DBG_PARANOIA_TEST_ENABLE_CHANGE: Rising or falling edge on test enable, after reset. Need reset_ep to clear. No impact on IPL.
30	ROX	DBG_PARANOIA_VITL_CLKOFF_CHANGE: Rising or falling edge on vitl_clkoff, after reset. Need reset_ep to clear. No impact on IPL.
31	ROX	TP_TPFSI_CBS_ACK: This is the only representation of the CC acknowledge signal that is sent to FSI.

Register Name	CC Protect Mode Register
Mnemonic	TP.TCEC14.CORE.CC_PROTECT_MODE_REG
Address	000000002E0303FE (SCOM)
Description	Enables read and write protection.

Bits	SCOM	Field Mnemonic: Description
0	RW	CC_READ_PROTECT_ENABLE: Enables read protection.
1	RW	CC_WRITE_PROTECT_ENABLE: Enables write protection.

Register Name	Atomic Lock Register
Mnemonic	TP.TCEC14.CORE.CC_ATOMIC_LOCK_REG
Address	000000002E0303FF (SCOM)
Description	Enables an atomic lock and an atomic lock counter.

Bits	SCOM	Field Mnemonic: Description
0	RW	CC_ATOMIC_LOCK_ENABLE: Enables atomic lock.
1:4	ROX	CC_ATOMIC_ID: Atomic ID.
5:7	RO	constant = 0b000
8:15	ROX	CC_ATOMIC_ACTIVITY: Atomic lock counter.

Register Name	Global Checkstop FIR Register
Mnemonic	TP.TCEC14.CORE.XFIR
Address	000000002E040000 (SCOM)
Description	Global checkstop FIR

Bits	SCOM	Field Mnemonic: Description
0	RWX	XFIR_IN0: Summary bit (any checkstop).
1	RWX	XFIR_IN1: Checkstop broadcast via OOB.
2	RWX	XFIR_IN2: Unused.
3	RWX	XFIR_IN3: Checkstop from pervasive unit.
4	RWX	XFIR_IN4: Checkstop from CX.
5:25	RWX	XFIR_IN5: Unused.
26	RWX	XFIR_IN26: Checkstop on debug trigger.

Register Name	Global Recoverable FIR Register
Mnemonic	TP.TCEC14.CORE.RFIR
Address	000000002E040001 (SCOM)
Description	Global recoverable FIR

Bits	SCOM	Field Mnemonic: Description
0	ROX	RFIR_IN0: Local checkstop from NX and CXA0.
1	ROX	LFIR_RECOV_ERR: Recoverable error from pervasive unit.
2	ROX	RFIR_IN4: Recovery from CX.
3:23	ROX	RFIR_IN5: Unused.

Register Name	FIR Mask Register
Mnemonic	TP.TCEC14.CORE.FIR_MASK
Address	000000002E040002 (SCOM)
Description	FIR mask

Bits	SCOM	Field Mnemonic: Description
0	RW	FIR_MASK_IN0: Mask for XFIR/RFIR summary bit.
1	RW	FIR_MASK_IN1: Mask for XFIR broadcast via OOB.
2	RW	FIR_MASK_IN2: Unused.

Bits	SCOM	Field Mnemonic: Description
3	RW	FIR_MASK_IN3: Mask for XFIR/RFIR from pervasive unit.
4	RW	FIR_MASK_IN4: Mask for CX, XFIR, and RFIR.
5:25	RW	FIR_MASK_IN5: Unused.
26	RW	FIR_MASK_IN26: Mask for debug trigger and local checkstop to recoverable error.

Register Name	Special Attention Register
Mnemonic	TP.TCEC14.CORE.SPATTN
Address	000000002E040004 (SCOM) 000000002E040005 (SCOM1) 000000002E040006 (SCOM2)
Description	Special attention

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	ROX	NCX	NCX	SPATTN_IN0: Special attention in 0.
1	ROX	NCX	NCX	SPATTN_IN1: Special attention in 1.
2	ROX	NCX	NCX	SPATTN_IN2: Special attention in 2.
3	ROX	NCX	NCX	SPATTN_IN3: Special attention in 3.
4	ROX	NCX	NCX	SPATTN_IN4: Unused special attentions.
5	ROX	NCX	NCX	SPATTN_IN5: Unused special attentions.
6	ROX	NCX	NCX	SPATTN_IN6: Unused special attentions.
7	ROX	NCX	NCX	SPATTN_IN7: Unused special attentions.
8	ROX	NCX	NCX	SPATTN_IN8: Unused special attentions.
9	ROX	NCX	NCX	SPATTN_IN9: Unused special attentions.

Register Name	Special Attention Mask Register
Mnemonic	TP.TCEC14.CORE.SPA_MASK
Address	000000002E040007 (SCOM)
Description	Special attention mask

Bits	SCOM	Field Mnemonic: Description
0:9	RW	SPA_MASK_IN: Special attention mask.

Register Name	Mode Register
Mnemonic	TP.TCEC14.CORE.EPS.FIR.MODE_REG
Address	000000002E040008 (SCOM)
Description	FIR mode register.

Bits	SCOM	Field Mnemonic: Description
0	RW	MODE_IN0: Unused.
1	RW	MODE_IN1: Unused.

Bits	SCOM	Field Mnemonic: Description
2	RW	MODE_IN2: Unused.
3	RW	MODE_IN3: Unused.
4	RW	MODE_IN4: Stop chip TOD on checkstop. (Unused in POWER9.)
5	RW	MODE_IN5: Stop chip TOD on recoverable. (Unused in POWER9.)
6	RW	MODE_IN6: Disable propagation of checkstop to other chips.
7	RW	MODE_IN7: Unused.
8	RW	MODE_IN8: Enable checkstop on special attention.
9	RW	MODE_IN9: mask_direct / local_error.
10	RW	MODE_IN10: Unused.
11	RW	MODE_IN11: Unused.
12:15	RW	MODE_IN: Unused.

Register Name	Host Attention Register
Mnemonic	TP.TCEC14.CORE.HOSTATTN
Address	000000002E040009 (SCOM)
Description	Host attention summary.

Bits	SCOM	Field Mnemonic: Description
0	ROX	HOSTATTN_IN0: Host attention summary bit.
1	ROX	HOSTATTN_IN1: Unused.
2	ROX	HOSTATTN_IN2: Unused.
3	ROX	HOSTATTN_IN3: Unused.
4	ROX	HOSTATTN_IN4: Unused.
5	ROX	HOSTATTN_IN5: Unused.
6	ROX	HOSTATTN_IN6: Unused.
7	ROX	HOSTATTN_IN7: Unused.
8	ROX	HOSTATTN_IN8: Unused.
9	ROX	HOSTATTN_IN9: Unused.
10	ROX	HOSTATTN_IN10: Unused.
11	ROX	HOSTATTN_IN11: Unused.
12	ROX	HOSTATTN_IN12: Unused.
13	ROX	HOSTATTN_IN13: Unused.
14	ROX	HOSTATTN_IN14: Unused.
15	ROX	HOSTATTN_IN15: Unused.
16	ROX	HOSTATTN_IN16: Unused.
17	ROX	HOSTATTN_IN17: Unused.
18	ROX	HOSTATTN_IN18: Unused.
19	ROX	HOSTATTN_IN19: Unused.
20	ROX	HOSTATTN_IN20: Unused.

Bits	SCOM	Field Mnemonic: Description
21	ROX	HOSTATTN_IN21: Unused.
22	ROX	HOSTATTN_IN22: Unused.

Register Name	Local FIR Register
Mnemonic	TP.TCEC14.CORE.LOCAL_FIR
Address	000000002E04000A (SCOM) 000000002E04000B (SCOM1) 000000002E04000C (SCOM2)
Description	Local FIR

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_IN0: CFIR internal parity error.
1	RWX	WOX_AND	WOX_OR	FIR_IN1: Errors from Control.
2	RWX	WOX_AND	WOX_OR	FIR_IN2: Local errors from CC (PCB error).
3	RWX	WOX_AND	WOX_OR	FIR_IN3: Local errors from CC (OPCG, parity, scan collision, and so on).
4	RWX	WOX_AND	WOX_OR	FIR_IN4: Local errors from PSC (PCB error).
5	RWX	WOX_AND	WOX_OR	FIR_IN5: Local errors from PSC (parity error).
6	RWX	WOX_AND	WOX_OR	FIR_IN6: Local errors from Thermal (parity error).
7	RWX	WOX_AND	WOX_OR	FIR_IN7: Local errors from Thermal (PCB error).
8	RWX	WOX_AND	WOX_OR	FIR_IN8: Local errors from Thermal (Trip error critical).
9	RWX	WOX_AND	WOX_OR	FIR_IN9: Local errors from Thermal (Trip error fatal).
10	RWX	WOX_AND	WOX_OR	FIR_IN10: Therm volttrip error.
11	RWX	WOX_AND	WOX_OR	FIR_IN11: Local errors from Debug (error).
12	RWX	WOX_AND	WOX_OR	FIR_IN12: Unused.
13	RWX	WOX_AND	WOX_OR	FIR_IN13: Unused.
14	RWX	WOX_AND	WOX_OR	FIR_IN14: Unused.
15	RWX	WOX_AND	WOX_OR	FIR_IN15: Unused.
16	RWX	WOX_AND	WOX_OR	FIR_IN16: Unused.
17	RWX	WOX_AND	WOX_OR	FIR_IN17: Unused.
18	RWX	WOX_AND	WOX_OR	FIR_IN18: Unused.
19	RWX	WOX_AND	WOX_OR	FIR_IN19: Unused.
20	RWX	WOX_AND	WOX_OR	FIR_IN20: Unused.
21	RWX	WOX_AND	WOX_OR	FIR_IN21: Unused.
22	RWX	WOX_AND	WOX_OR	FIR_IN22: Unused.
23	RWX	WOX_AND	WOX_OR	FIR_IN23: Unused.
24	RWX	WOX_AND	WOX_OR	FIR_IN24: Unused.
25	RWX	WOX_AND	WOX_OR	FIR_IN25: Unused.
26	RWX	WOX_AND	WOX_OR	FIR_IN26: Unused.
27	RWX	WOX_AND	WOX_OR	FIR_IN27: Unused.
28	RWX	WOX_AND	WOX_OR	FIR_IN28: Unused.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
29	RWX	WOX_AND	WOX_OR	FIR_IN29: Unused.
30	RWX	WOX_AND	WOX_OR	FIR_IN30: Unused.
31	RWX	WOX_AND	WOX_OR	FIR_IN31: Unused.
32	RWX	WOX_AND	WOX_OR	FIR_IN32: Unused.
33	RWX	WOX_AND	WOX_OR	FIR_IN33: Unused.
34	RWX	WOX_AND	WOX_OR	FIR_IN34: Unused.
35	RWX	WOX_AND	WOX_OR	FIR_IN35: Unused.
36	RWX	WOX_AND	WOX_OR	FIR_IN36: Unused.
37	RWX	WOX_AND	WOX_OR	FIR_IN37: Unused.
38	RWX	WOX_AND	WOX_OR	FIR_IN38: Unused.
39	RWX	WOX_AND	WOX_OR	FIR_IN39: Unused.
40	RWX	WOX_AND	WOX_OR	FIR_IN40: Unused.
41	RWX	WOX_AND	WOX_OR	FIR_IN41: Malfunction alert broadcast via OOB.

Register Name	Local FIR Mask Register
Mnemonic	TP.TCEC14.CORE.EPS.FIR.LOCAL_FIR_MASK
Address	000000002E04000D (SCOM) 000000002E04000E (SCOM1) 000000002E04000F (SCOM2)
Description	Local FIR mask

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:41	RW	WO_AND	WO_OR	LFIR_MASK_IN: Mask for LEM error collection vector.

Register Name	Local FIR Action 0 Register
Mnemonic	TP.TCEC14.CORE.EPS.FIR.LOCAL_FIR_ACTION0
Address	000000002E040010 (SCOM)
Description	Local FIR action 0

Bits	SCOM	Field Mnemonic: Description
0:41	RW	FIR_ACTION0_IN: action0 mask.

Register Name	Local FIR Action 1 Register
Mnemonic	TP.TCEC14.CORE.EPS.FIR.LOCAL_FIR_ACTION1
Address	000000002E040011 (SCOM)
Description	Local FIR action 1

Bits	SCOM	Field Mnemonic: Description
0:41	RW	FIR_ACTION1_IN: action1 mask.

Register Name	Group Checkstop Trigger Register
Mnemonic	TP.TCEC14.CORE.EPS.FIR.GXSTOP_TRIG_REG
Address	000000002E040013 (SCOM)
Description	Group checkstop mask

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP_TRIG_IN0: Mask bit for system checkstop.
1	RW	GXSTP_TRIG_IN1: Mask bit for recoverable error.
2	RW	GXSTP_TRIG_IN2: Mask bit for special attention.
3	RW	GXSTP_TRIG_IN3: Mask bit for local checkstop.
4	RW	GXSTP_TRIG_IN4: Mask bit for type 4 error (host attention).
5	RW	GXSTP_TRIG_IN5: Mask bit for OOB sys_checkstop input (0).
6	RW	GXSTP_TRIG_IN6: Mask bit for OOB sys_checkstop input (1).
7	RW	GXSTP_TRIG_IN7: Mask bit for group checkstop input (0).
8	RW	GXSTP_TRIG_IN8: Mask bit for group checkstop input (1).
9	RW	GXSTP_TRIG_IN9: Mask bit for debug checkstop on trigger.
10	RW	GXSTP_TRIG_IN10: Unused.
11	RW	GXSTP_TRIG_IN11: Unused.

Register Name	Group 0 Checkstop Mask Register
Mnemonic	TP.TCEC14.CORE.EPS.FIR.GXSTOP0_MASK_REG
Address	000000002E040014 (SCOM)
Description	Group 0 checkstop mask

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP0_TRIG_IN0: Mask bit for system checkstop.
1	RW	GXSTP0_TRIG_IN1: Mask bit for recoverable error.
2	RW	GXSTP0_TRIG_IN2: Mask bit for special attention.
3	RW	GXSTP0_TRIG_IN3: Mask bit for local checkstop.
4	RW	GXSTP0_TRIG_IN4: Mask bit for type 4 error (host attention).
5	RW	GXSTP0_TRIG_IN5: Mask bit for OOB sys_checkstop Input (0).
6	RW	GXSTP0_TRIG_IN6: Mask bit for OOB sys_checkstop Input (1).
7	RW	GXSTP0_TRIG_IN7: Mask bit for group checkstop input (0).
8	RW	GXSTP0_TRIG_IN8: Mask bit for group checkstop input (1).
9	RW	GXSTP0_TRIG_IN9: Mask bit for debug checkstop on trigger.
10	RW	GXSTP0_TRIG_IN10: Unused.
11	RW	GXSTP0_TRIG_IN11: Unused.

Register Name	Group 1 Checkstop Mask Register
Mnemonic	TP.TCEC14.CORE.EPS.FIR.GXSTOP1_MASK_REG
Address	000000002E040015 (SCOM)
Description	Group 1 checkstop mask

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP1_TRIG_IN0: Mask bit for system checkstop.
1	RW	GXSTP1_TRIG_IN1: Mask bit for recoverable error.
2	RW	GXSTP1_TRIG_IN2: Mask bit for special attention.
3	RW	GXSTP1_TRIG_IN3: Mask bit for local checkstop.
4	RW	GXSTP1_TRIG_IN4: Mask bit for type 4 error (host attention).
5	RW	GXSTP1_TRIG_IN5: Mask bit for OOB sys_checkstop Input (0).
6	RW	GXSTP1_TRIG_IN6: Mask bit for OOB sys_checkstop Input (1).
7	RW	GXSTP1_TRIG_IN7: Mask bit for group checkstop input (0).
8	RW	GXSTP1_TRIG_IN8: Mask bit for group checkstop input (1).
9	RW	GXSTP1_TRIG_IN9: Mask bit for debug checkstop on trigger.
10	RW	GXSTP1_TRIG_IN10: Unused.
11	RW	GXSTP1_TRIG_IN11: Unused.

Register Name	Group 2 Checkstop Mask Register
Mnemonic	TP.TCEC14.CORE.EPS.FIR.GXSTOP2_MASK_REG
Address	000000002E040016 (SCOM)
Description	Group 2 checkstop mask

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP2_TRIG_IN0: Mask bit for system checkstop.
1	RW	GXSTP2_TRIG_IN1: Mask bit for recoverable error.
2	RW	GXSTP2_TRIG_IN2: Mask bit for special attention.
3	RW	GXSTP2_TRIG_IN3: Mask bit for local checkstop.
4	RW	GXSTP2_TRIG_IN4: Mask bit for type 4 error (host attention).
5	RW	GXSTP2_TRIG_IN5: Mask bit for OOB sys_checkstop Input (0).
6	RW	GXSTP2_TRIG_IN6: Mask bit for OOB sys_checkstop Input (1).
7	RW	GXSTP2_TRIG_IN7: Mask bit for group checkstop input (0).
8	RW	GXSTP2_TRIG_IN8: Mask bit for group checkstop input (1).
9	RW	GXSTP2_TRIG_IN9: Mask bit for debug checkstop on trigger.
10	RW	GXSTP2_TRIG_IN10: Unused.
11	RW	GXSTP2_TRIG_IN11: Unused.

Register Name	Summary Mask Register
Mnemonic	TP.TCEC14.CORE.EPS.FIR.SUM_MASK_REG
Address	000000002E040017 (SCOM)
Description	FIR summary mask register

Bits	SCOM	Field Mnemonic: Description
0	RW	SMASK_IN0: System checkstop summary bit.
1	RW	SMASK_IN1: Recoverable summary bit.
2	RW	SMASK_IN2: Special attention summary bit.
3	RW	SMASK_IN3: Local checkstop summary bit.
4	RW	SMASK_IN4: Type4 (host attention) summary bit.

Register Name	Local Checkstop Error Register
Mnemonic	TP.TCEC14.CORE.LOCAL_XSTOP_ERR
Address	000000002E040018 (SCOM)
Description	Local checkstop error

Bits	SCOM	Field Mnemonic: Description
0	ROX	LOCAL_XSTOP_IN0: Local checkstop summary bit.
1	ROX	LOCAL_XSTOP_IN1: Local checkstop from core.
2	ROX	LOCAL_XSTOP_IN2: Unused.
3	ROX	LOCAL_XSTOP_IN3: Unused.
4	ROX	LOCAL_XSTOP_IN4: Unused.
5	ROX	LOCAL_XSTOP_IN5: Unused.
6	ROX	LOCAL_XSTOP_IN6: Unused.
7	ROX	LOCAL_XSTOP_IN7: Unused.
8	ROX	LOCAL_XSTOP_IN8: Unused.
9	ROX	LOCAL_XSTOP_IN9: Unused.
10	ROX	LOCAL_XSTOP_IN10: Unused.
11	ROX	LOCAL_XSTOP_IN11: Unused.
12	ROX	LOCAL_XSTOP_IN12: Unused.
13	ROX	LOCAL_XSTOP_IN13: Unused.
14	ROX	LOCAL_XSTOP_IN14: Unused.
15	ROX	LOCAL_XSTOP_IN15: Unused.
16	ROX	LOCAL_XSTOP_IN16: Unused.
17	ROX	LOCAL_XSTOP_IN17: Unused.
18	ROX	LOCAL_XSTOP_IN18: Unused.
19	ROX	LOCAL_XSTOP_IN19: Unused.
20	ROX	LOCAL_XSTOP_IN20: Unused.
21	ROX	LOCAL_XSTOP_IN21: Unused.

Bits	SCOM	Field Mnemonic: Description
22	ROX	LOCAL_XSTOP_IN22: Unused.

Register Name	Local Checkstop Mask Register
Mnemonic	TP.TCEC14.CORE.LOCAL_XSTOP_MASK
Address	000000002E040019 (SCOM)
Description	Local checkstop mask

Bits	SCOM	Field Mnemonic: Description
0:21	RW	LOCAL_XSTOP_MASK_IN: Local checkstop mask.

Register Name	Host Attention Mask Register
Mnemonic	TP.TCEC14.CORE.HOSTATTN_MASK
Address	000000002E04001A (SCOM)
Description	Host attention mask.

Bits	SCOM	Field Mnemonic: Description
0:21	RW	HOSTATTN_MASK_IN: Host attention mask.

Register Name	DTS Thermal Sensor Results 0 Register
Mnemonic	TP.TCEC14.CORE.EPS.THERM.DTS_RESULT0
Address	000000002E050000 (SCOM)
Description	DTS thermal sensor loop1 results.

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	DTS_0_RESULT: Calibrated DTS result of sensor with ID 0.
16:31	ROX	DTS_1_RESULT: Calibrated DTS result of sensor with ID 1.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	DTS Trace Results Register
Mnemonic	TP.TCEC14.CORE.EPS.THERM.DTS_TRC_RESULT
Address	000000002E050003 (SCOM)
Description	DTS trace results

Bits	SCOM	Field Mnemonic: Description
0:43	ROX	TIMESTAMP_COUNTER_VALUE: Time stamp counter value during DTS trace mode.
44	ROX	TIMESTAMP_COUNTER_OVERFLOW_ERR: Overflow error bit of the time stamp counter value during DTS trace mode.
45:47	RO	constant = 0b000
48:63	ROX	DTS_1_RESULT: Calibrated DTS result of sensor with ID 1.

Register Name	Thermal Mode Register
Mnemonic	TP.TCEC14.CORE.EPS.THERM.THERM_MODE_REG
Address	000000002E05000F (SCOM)
Description	Enables and controls CPM and DTS.

Bits	SCOM	Field Mnemonic: Description
0	RW	THERM_DIS_CPM_BUBBLE_CORR: Critical path result bubble correction active.
1	RW	THERM_FORCE_THRES_ACT: Forces tpc_therm_thres_mac clock gating off and activates clocks.
2:4	RW	THERM_THRES_TRIP_ENA: Enables therm_thres_trip compare. 1xx = trip0, warning. x1x = trip1, critical. xx1 = trip2, fatal.
5	RW	THERM_DTS_SAMPLE_ENA: 0 = No DTS sampling. 1 = DTS sampling is enabled and a below-counter compare match can occur.
6:9	RW	THERM_SAMPLE_PULSE_CNT: A 16 MHz sample pulse is fed into an 18-bit counter. therm_sample_pulse_cnt enables the selection of a high order bit of the counter to enable resolution of sampling DTSs between 2.5 ms and 80 ms. An edge detection circuit detects the rising edge of the selected counter bit and this triggers a DTS sample. 0000 = 16 ms. 0001 = 8 ms. 0010 = 4 ms. 0011 = 2 ms. 0100 = 1 ms. 0101 = 0.5 ms. 0110 = 250 ms. 0111 = 125 ms. 1000 = 62 .5 ms. 1001 = 31.3 ms. 1010 = 15.6 ms. 1011 = 7.8 ms. 1100 = 3.9 ms. 1101 = 2 ms. 1110 = 1 ms. 1111 = 0.5 ms.
10:11	RW	THERM_THRES_MODE_ENA: Forces maximum or minimum mode in the threshold unit: 00 = Off. 11 = Illegal. 10 = Maximum mode. 01 = Minimum mode.
12	RW	DTS_TRIGGER_MODE: Unused.
13	RW	DTS_TRIGGER_SEL: Unused.
14	RW	THERM_THRES_OVERFLOW_MASK: 0 = therm_overflow_err is enabled. 1 = therm_overflow_err is disabled.
15	RW	THERM_MODE_UNUSED: Unused.
16:19	RW	THERM_DTS_READ_SEL: Selects which DTS result will be provided with PCB read addr_v(4): 0000 = DTS 0. 0001 = DTS 1. 0010 = DTS 2. 0100 = DTS 4. 1111 = Worst case sensor.

Bits	SCOM	Field Mnemonic: Description
20:21	RW	THERM_DTS_ENABLE_L1: Loop1 DTS enables: 1x = DTS 0 available. x1 = DTS 1 available.
22:34	RO	constant = 0b0000000000000
35:36	RW	Reserved field.

Register Name	Skitter Mode Register
Mnemonic	TP.TCEC14.CORE.EPS.THERM.SKITTER_MODE_REG
Address	000000002E050010 (SCOM)
Description	Skitter control register

Bits	SCOM	Field Mnemonic: Description
0	RW	SKITTER_HOLD_SAMPLE: Forces skitter to hold the current sample.
1	RW	DISABLE_SKITTER_STICKINESS: A value of '0' specifies accumulation mode. A value of '1' samples a new value on each cycle and resets the sticky value.
2:3	RW	SKITTER_MODE_UNUSED1: Unused.
4:5	RW	SKITTER_HOLD_DBGTRIG_SEL: bit0 = hold_on_trigger0 bit1 = hold_on_trigger1
6:7	RW	SKITTER_RESET_TRIG_SEL: bit0 = reset_sticky_on_trigger0 bit1 = reset_sticky_on_trigger1
8:9	RW	SKITTER_SAMPLE_GUTS: Selects which guts to measure: 00 = guts1. 01 = guts2. 10 = guts3. 11 = guts4.
10:43	RO	constant = 0b0000000000000000000000000000000000
44	ROX	SKITTER_HOLD_SAMPLE_WITH_TRIGGER: Forces skitter to hold the current sample on debug trigger; this has highest priority.
45	ROX	SKITTER_DATA_V_LT: If set to '1', the data requested by a skitter force read register has finished and data is present in the skitter data register in the collector macro. The data be read by any combination of V25/V26/V27 PCB reads.

Register Name	Error Injection Control Register
Mnemonic	TP.TCEC14.CORE.EPS.THERM.INJECT_REG
Address	000000002E050011 (SCOM)
Description	Error injection control register

Bits	SCOM	Field Mnemonic: Description
0:1	RW	THERM_INJECT_TRIP: 00 = No injection. 01 = Warning trip level injection. 10 = Critical trip level injection. 11 = Fatal trip level injection.

Bits	SCOM	Field Mnemonic: Description
2:3	RW	THERM_INJECT_MODE: 00 = No injection. 01 = Injection on the next DTS sample. 10 = Solid injection for the next DTS samples until bit setting changes. 11 = Not used.

Register Name	Thermal Control Register
Mnemonic	TP.TCEC14.CORE.EPS.THERM.CONTROL_REG
Address	000000002E050012 (SCOM)
Description	Control / force reset register

Bits	SCOM	Field Mnemonic: Description
0	WO_1P	Reserved field.
1	WO_1P	Reserved field.
2	WO_1P	Reserved field.
3	WO_1P	Reserved field.
4	WO_1P	Reserved field.
5	WO_1P	Reserved field.
6	WO_1P	Reserved field.
7	WO_1P	Reserved field.
8	WO_1P	Reserved field.
9	WO_1P	Reserved field.
10	WO_1P	Reserved field.
11	WO_1P	Reserved field.
12	WO_1P	Reserved field.

Register Name	Thermal Error Status Register
Mnemonic	TP.TCEC14.CORE.EPS.THERM.ERR_STATUS_REG
Address	000000002E050013 (SCOM)
Description	Thermal error status register

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	Reserved field.
2	ROX	Reserved field.
3	ROX	Reserved field.
4	ROX	Reserved field.
5	ROX	Reserved field.
6	ROX	Reserved field.
7	ROX	Reserved field.
8	ROX	Reserved field.

Bits	SCOM	Field Mnemonic: Description
9	ROX	Reserved field.
10	ROX	Reserved field.
11	ROX	Reserved field.
12	ROX	Reserved field.
13	ROX	Reserved field.
14	ROX	Reserved field.
15	ROX	Reserved field.
16	ROX	SERIAL_SHIFTCNT_MODEREG_PARITY_ERR_MASK: Serial shift count parity error mask.
17	ROX	THERM_MODEREG_PARITY_ERR_MASK: Thermal Mode Register parity error mask.
18	ROX	SKITTER_MODEREG_PARITY_ERR_MASK: Skitter Mode Register parity error mask.
19	ROX	SKITTER_FORCEREG_PARITY_ERR_MASK: Skitter Force Register parity error mask.
20	ROX	SCAN_INIT_VERSION_REG_PARITY_ERR_MASK: Scan Initial Version Register parity error mask.
21	ROX	VOLT_MODEREG_PARITY_ERR_MASK: Volt Mode Register parity error mask.
22	RO	constant = 0b0
23	ROX	COUNT_STATE_ERR_MASK: Count state machine error mask.
24	ROX	RUN_STATE_ERR_MASK: Run state machine error mask.
25	ROX	THRES_STATE_ERR_MASK: Threshold state machine error mask.
26	ROX	OVERFLOW_ERR_MASK: DTS calibration calculation overflow error mask.
27	ROX	SHIFTER_PARITY_ERR_MASK: Shifter parity error mask.
28	ROX	SHIFTER_VALID_ERR_MASK: Shifter valid error mask.
29	ROX	TIMEOUT_ERR_MASK: Timeout error mask.
30	ROX	F_SKITTER_READ_ERR_MASK: Force skitter read error mask.
31	ROX	PCB_ERR_MASK: Pervasive control bus error mask.
32:39	RO	constant = 0b00000000
40:43	ROX	Reserved field.
44:46	ROX	Reserved field.
47	ROX	Reserved field.
48	ROX	Reserved field.
49:50	ROX	Reserved field.
51:54	ROX	Reserved field.
55	ROX	Reserved field.
56	ROX	Reserved field.
57	ROX	Reserved field.
58	ROX	Reserved field.
59	ROX	Reserved field.
60:63	RO	constant = 0b0000

Register Name	Skitter Force Read Register
Mnemonic	TP.TCEC14.CORE.EPS.THERM.SKITTER_FORCE_REG
Address	000000002E050014 (SCOM)
Description	Skitter force read register

Bits	SCOM	Field Mnemonic: Description
0	RW	F_SKITTER_READ: Forces the read of a particular skitter.

Register Name	Skitter Clock Source Control Register
Mnemonic	TP.TCEC14.CORE.EPS.THERM.SKITTER_CLKSRC_REG
Address	000000002E050016 (SCOM)
Description	Skitter clock source control register

Bits	SCOM	Field Mnemonic: Description
0:2	RW	SKITTER0_CLKSRC: Selects the clock to measure: 000 = Local mesh clock. 001 = External pin skitter_c1_1_in. 010 = Local d1clk only if d_mode = 1. 011 = External pin skitter_c1_2_in. 100 = Local lclk only if d_mode = 1. 101 = External pin skitter_c1_3_in. 110 = Unused. 111 = External pin skitter_c1_4_in.
3:35	RO	constant = 0b000000000000000000000000000000000
36:37	RW	SKITTER0_DELAY_SELECT: Selects the delay to be added between the skitter0 clock source multiplexer and the inverter chain. The base line delay is 12.2 psec. 00 = No delay. 01 = 0.6 psec. 10 = 1.8 psec. 11 = 5 psec.

Register Name	Skitter Data 0 Register
Mnemonic	TP.TCEC14.CORE.EPS.THERM.SKITTER_DATA0
Address	000000002E050019 (SCOM)
Description	Skitter data register read bit0:63.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved.

Register Name	Skitter Data 1 Register
Mnemonic	TP.TCEC14.CORE.EPS.THERM.SKITTER_DATA1
Address	000000002E05001A (SCOM)
Description	Skitter data 1 register read bit32:95.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved.

Register Name	Skitter Data 2 Register
Mnemonic	TP.TCEC14.CORE.EPS.THERM.SKITTER_DATA2
Address	000000002E05001B (SCOM)
Description	Skitter data 2 register read bit64:127.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved.

Register Name	Timestamp Counter Read Register
Mnemonic	TP.TCEC14.CORE.EPS.THERM.TIMESTAMP_COUNTER_READ
Address	000000002E05001C (SCOM)
Description	Timestamp counter read

Bits	SCOM	Field Mnemonic: Description
0:43	ROX	TIMESTAMP_COUNTER_VALUE: Time stamp counter value during DTS trace mode.
44	ROX	TIMESTAMP_COUNTER_OVERFLOW_ERR: Overflow error bit of the time stamp counter value during DTS trace mode.

15. CORE Chiplet PCB Slave

The POWER9 processor registers are listed alphabetically by mnemonic in the following address table.

Mnemonic	Address	Page
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_CGCR	0x000000002E0F0164	2370
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_GPMMR	0x000000002E0F0100	2358
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_IVRMAVR	0x000000002E0F01B5	2377
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_IVRMCR	0x000000002E0F01B0	2376
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_IVRMDVR	0x000000002E0F01B4	2377
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_IVRMST	0x000000002E0F01B3	2377
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_PFCS	0x000000002E0F0118	2364
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_PFDLY	0x000000002E0F011B	2366
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_PFOFF	0x000000002E0F011D	2367
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_PFSNS	0x000000002E0F011C	2366
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_PIG	0x000000002E0F0180	2371
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_SCRATCH0	0x000000002E0F011E	2367
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_SCRATCH1	0x000000002E0F011F	2367
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_SPWKUP_FSP	0x000000002E0F010B	2361
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_SPWKUP_HYP	0x000000002E0F010D	2361
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_SPWKUP_OCC	0x000000002E0F010C	2361
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_SPWKUP_OTR	0x000000002E0F010A	2360
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_SSHFSP	0x000000002E0F0111	2362
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_SSHHYP	0x000000002E0F0114	2363
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_SSHOCC	0x000000002E0F0112	2362
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_SSHOTR	0x000000002E0F0113	2363
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_SSHSRC	0x000000002E0F0110	2361
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_VDMCR	0x000000002E0F01B8	2378
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_CACCR	0x000000002E0F0168	2370
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_CACSR	0x000000002E0F016B	2371
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_CIIR	0x000000002E0F01AD	2374
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_CISR	0x000000002E0F01AE	2375
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_CIVRMLCR	0x000000002E0F01B7	2378
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_CMEDATA	0x000000002E0F01A8	2374
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_CMEDB0	0x000000002E0F0190	2372
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_CMEDB1	0x000000002E0F0194	2373
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_CMEDB2	0x000000002E0F0198	2373
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_CMEDB3	0x000000002E0F019C	2374
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_CMEMSG	0x000000002E0F01AB	2374
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_CPMMR	0x000000002E0F0106	2358
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_CSAR	0x000000002E0F0138	2369
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_ERR	0x000000002E0F0121	2368
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_ERRMSK	0x000000002E0F0122	2368
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_IPPMCMD	0x000000002E0F01C0	2379
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_IPPMRDATA	0x000000002E0F01C3	2380
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_IPPMSTAT	0x000000002E0F01C1	2379
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_IPPMWDATA	0x000000002E0F01C2	2379

Mnemonic	Address	Page
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_NC0INDIR	0x000000002E0F0130	2369
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_NC1INDIR	0x000000002E0F0133	2369
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_PECES	0x000000002E0F01AF	2375
TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_PERRSUM	0x000000002E0F0120	2367
TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.ASSIST_INTERRUPT_REG	0x000000002E0F0011	2351
TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.ATOMIC_LOCK_REG	0x000000002E0F03FF	2380
TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.ATTN_INTERRUPT_REG	0x000000002E0F001A	2352
TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.EDRAM_STATUS	0x000000002E0F0029	2356
TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.ERROR_REG	0x000000002E0F001F	2353
TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.HANG_PULSE_0_REG	0x000000002E0F0020	2354
TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.HANG_PULSE_1_REG	0x000000002E0F0021	2354
TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.HANG_PULSE_2_REG	0x000000002E0F0022	2354
TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.HANG_PULSE_3_REG	0x000000002E0F0023	2354
TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.HANG_PULSE_4_REG	0x000000002E0F0024	2355
TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.HANG_PULSE_5_REG	0x000000002E0F0025	2355
TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.HANG_PULSE_6_REG	0x000000002E0F0026	2355
TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.HEARTBEAT_REG	0x000000002E0F0018	2351
TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.MULTICAST_GROUP_1	0x000000002E0F0001	2350
TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.MULTICAST_GROUP_2	0x000000002E0F0002	2350
TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.MULTICAST_GROUP_3	0x000000002E0F0003	2350
TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.MULTICAST_GROUP_4	0x000000002E0F0004	2350
TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.NET_CTRL0	0x000000002E0F0040	2356
TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.NET_CTRL1	0x000000002E0F0044	2357
TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.PLL_LOCK_REG	0x000000002E0F0019	2351
TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.PRE_COUNTER_REG	0x000000002E0F0028	2355
TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.PRIMARY_ADDRESS_REG	0x000000002E0F0000	2349
TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.PROTECT_MODE_REG	0x000000002E0F03FE	2380
TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.RECOV_INTERRUPT_REG	0x000000002E0F001B	2352
TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.SLAVE_CONFIG_REG	0x000000002E0F001E	2352
TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.TIMEOUT_REG	0x000000002E0F0010	2351
TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.VITAL_SCAN_OUT	0x000000002E0F0017	2351
TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.XSTOP_INTERRUPT_REG	0x000000002E0F001C	2352

The POWER9 processor registers are listed in the following tables.

Register Name	**Primary Address Register**
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.PRIMARY_ADDRESS_REG
Address	000000002E0F0000 (SCOM)
Description	This register contains the primary address of a slave.

Bits	SCOM	Field Mnemonic: Description
0:5	RO	Reserved field.

Register Name	Multicast Group 1 Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.MULTICAST_GROUP_1
Address	000000002E0F0001 (SCOM)
Description	Multicast group 1

Bits	SCOM	Field Mnemonic: Description
0:2	RO	constant = 0b111
3:5	RW	MULTICAST1_GROUP: Multicast group1 setting.

Register Name	Multicast Group 2 Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.MULTICAST_GROUP_2
Address	000000002E0F0002 (SCOM)
Description	Multicast group 2

Bits	SCOM	Field Mnemonic: Description
0:2	RO	constant = 0b111
3:5	RW	MULTICAST2_GROUP: Multicast group2 setting.

Register Name	Multicast Group 3 Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.MULTICAST_GROUP_3
Address	000000002E0F0003 (SCOM)
Description	Multicast group 3

Bits	SCOM	Field Mnemonic: Description
0:2	RO	constant = 0b111
3:5	RW	MULTICAST3_GROUP: Multicast group3 setting.

Register Name	Multicast Group 4 Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.MULTICAST_GROUP_4
Address	000000002E0F0004 (SCOM)
Description	Multicast group 4

Bits	SCOM	Field Mnemonic: Description
0:2	RO	constant = 0b111
3:5	RW	MULTICAST4_GROUP: Multicast group4 setting.

Register Name	Timeout Select Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.TIMEOUT_REG
Address	000000002E0F0010 (SCOM)
Description	Timeout select register

Bits	SCOM	Field Mnemonic: Description
0:1	RW	Reserved field.

Register Name	Assist Interrupt Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.ASSIST_INTERRUPT_REG
Address	000000002E0F0011 (SCOM)
Description	Assist interrupt register

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	Reserved field.
2	ROX	Reserved field.

Register Name	Vital Scan Out Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.VITAL_SCAN_OUT
Address	000000002E0F0017 (SCOM)
Description	Vital scan out

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved.

Register Name	Chiplet Heartbeat Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.HEARTBEAT_REG
Address	000000002E0F0018 (SCOM)
Description	Chiplet heartbeat register

Bits	SCOM	Field Mnemonic: Description
0	ROX	HEARTBEAT_DEAD: The chiplet heartbeat is not detected.

Register Name	PLL Lock Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.PLL_LOCK_REG
Address	000000002E0F0019 (SCOM)
Description	Lock indications from PLLs.

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	Reserved field.

Register Name	Attention Interrupt Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.ATTN_INTERRUPT_REG
Address	000000002E0F001A (SCOM)
Description	Attention interrupt

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.

Register Name	Recovery Interrupt Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.RECOV_INTERRUPT_REG
Address	000000002E0F001B (SCOM)
Description	Recovery interrupt

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.

Register Name	Checkstop Interrupt Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.XSTOP_INTERRUPT_REG
Address	000000002E0F001C (SCOM)
Description	Checkstop interrupt

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.

Register Name	Slave Configuration Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.SLAVE_CONFIG_REG
Address	000000002E0F001E (SCOM)
Description	Slave configuration register

Bits	SCOM	Field Mnemonic: Description
0	RW	CFG_DISABLE_PERV_THOLD_CHECK: Disables the pervasive thold check.
1	RW	CFG_DISABLE_MALF_PULSE_GEN: Disables pulse generation for malfunction alert. Switches back to level.
2	RW	CFG_STOP_HANG_CNT_SYS_XSTP: Disables the hang counter stop for system checkstop.
3	RW	CFG_DISABLE_CL_ATOMIC_LOCK: Disables the atomic lock for chiplet accesses.
4	RW	CFG_DISABLE_HEARTBEAT: Disables a check for voltage and grid clock in the chiplet.
5	RW	CFG_DISABLE_FORCE_TO_ZERO: Disables force to zero for error cases.

Bits	SCOM	Field Mnemonic: Description
6	RW	CFG_PM_DISABLE: Disables the power management set/reset interface for the NET CNTRLx Registers.
7	RW	CFG_PM_MUX_DISABLE: Disables the power management multiplexer request signal.
8:13	RW	ERROR_MASK: Mask bits for slave error reporting.
14:15	RW	Reserved.

Register Name	Error Capture Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.ERROR_REG
Address	000000002E0F001F (SCOM)
Description	Error capture register

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	CE_ERROR: Correctable error on the PCB bus.
1:3	RWX_WCLEAR	CHIPLET_ERRORS: Errors reported by chiplet. This register is for debug purposes only. It holds meaningful data only if it is cleared after each error. 000 = No error. 001 = XSCOM command blocked due to pending errors. 010 = Chiplet offline. 011 = Partial good. 100 = Invalid address / address error / bad access type. 101 = Clock error. 110 = Parity error / received unexpected packet / wrong packet number. 111 = Timeout.
4	RWX_WCLEAR	PARITY_ERROR: Parity error on the PCB interface.
5	RWX_WCLEAR	DATA_BUFFER_ERROR: Parity error in the data buffer.
6	RWX_WCLEAR	ADDR_BUFFER_ERROR: Parity error in the address buffer.
7	RWX_WCLEAR	PCB_FSM_ERROR: Invalid state error in the PCB FSM.
8	RWX_WCLEAR	CL_FSM_ERROR: Invalid state error in the chiplet FSM.
9	RWX_WCLEAR	INT_RX_FSM_ERROR: Invalid state error in the interrupt RX FSM.
10	RWX_WCLEAR	INT_TX_FSM_ERROR: Invalid state error in the interrupt TX FSM.
11	RWX_WCLEAR	INT_TYPE_ERROR: Invalid interrupt type.
12	RWX_WCLEAR	CL_DATA_ERROR: Parity error on the chiplet interface.
13	RWX_WCLEAR	INFO_ERROR: Parity error on the chiplet information lines.
14	RWX_WCLEAR	UNUSED_0:
15	RWX_WCLEAR	CHIPLET_ATOMIC_LOCK_ERROR: Chiplet atomic lock error.
16	RWX_WCLEAR	PCB_INTERFACE_ERROR: Error of the PCB interface component for the internal endpoint.
17	RWX_WCLEAR	CHIPLET_OFFLINE: Heartbeat check indicated that the chiplet is offline.
18	RWX_WCLEAR	EDRAM_SEQUENCE_ERR: Error in the eDRAM power up sequence.
19	RWX_WCLEAR	CTRL_REG_PARITY_ERROR: Control register parity is bad.
20	RWX_WCLEAR	ADDRESS_REG_PARITY_ERROR: Address register parity is bad.
21	RWX_WCLEAR	TIMEOUT_REG_PARITY_ERROR: Timeout select register parity is bad.
22	RWX_WCLEAR	CONFIG_REG_PARITY_ERROR: Slave configuration register parity is bad.
23	RWX_WCLEAR	UNUSED_1:

Bits	SCOM	Field Mnemonic: Description
24	RWX_WCLEAR	DIV_REG_PARITY_ERROR: Register parity is bad.
25:28	RWX_WCLEAR	PLL_UNLOCK_ERROR: Unlock error from a chiplet PLL.

Register Name	Hang Pulse Generation 0 Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.HANG_PULSE_0_REG
Address	000000002E0F0020 (SCOM)
Description	Hang pulse generation register 0

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_0: Value of hang pulse 0. Time period = 2value x (precounter_reg + 1) / pcb_freq, where 34 ³ value > 0.
6	RW	SUPPRESS_HANG_0: If set to 1, hang pulses are suppressed in case of a checkstop.

Register Name	Hang Pulse Generation 1 Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.HANG_PULSE_1_REG
Address	000000002E0F0021 (SCOM)
Description	Hang pulse generation register 1

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_1: Value of hang pulse 1. Time period = 2value x (precounter_reg + 1) / pcb_freq, where 34 ³ value > 0.
6	RW	SUPPRESS_HANG_1: If set to 1, hang pulses are suppressed in case of a checkstop.

Register Name	Hang Pulse Generation 2 Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.HANG_PULSE_2_REG
Address	000000002E0F0022 (SCOM)
Description	Hang pulse generation register 2

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_2: Value of hang pulse 2. Time period = 2value x (precounter_reg + 1) / pcb_freq, where 34 ³ value > 0.
6	RW	SUPPRESS_HANG_2: If set to 1, hang pulses are suppressed in case of a checkstop.

Register Name	Hang Pulse Generation 3 Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.HANG_PULSE_3_REG
Address	000000002E0F0023 (SCOM)
Description	Hang pulse generation register 3

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_3: Value of hang pulse 3. Time period = 2value x (precounter_reg + 1) / pcb_freq, where 34 ³ value > 0.

Bits	SCOM	Field Mnemonic: Description
6	RW	SUPPRESS_HANG_3: If set to 1, hang pulses are suppressed in case of a checkstop.

Register Name	Hang Pulse Generation 4 Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.HANG_PULSE_4_REG
Address	000000002E0F0024 (SCOM)
Description	Hang pulse generation register 4

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_4: Value of hang pulse 4. Time period = 2value x (precounter_reg + 1) / pcb_freq, where 34 ³ value > 0.
6	RW	SUPPRESS_HANG_4: If set to 1, hang pulses are suppressed in case of a checkstop.

Register Name	Hang Pulse Generation 5 Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.HANG_PULSE_5_REG
Address	000000002E0F0025 (SCOM)
Description	Hang pulse generation register 5. This hang counter is used exclusively to generate the malfunction alert pulse.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_5: Value of hang pulse 5. Time period = 2value x (precounter_reg + 1) / pcb_freq, where 34 ³ value > 0.
6	RW	SUPPRESS_HANG_5: If set to 1, hang pulses are suppressed in case of a checkstop.

Register Name	Hang Pulse Generation 6 Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.HANG_PULSE_6_REG
Address	000000002E0F0026 (SCOM)
Description	Hang pulse generation register 6. This hang counter is used exclusively for heartbeat generation.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_6: Value of hang pulse 6. Time period = 2value x (precounter_reg + 1) / pcb_freq, where 34 ³ value > 0.
6	RW	SUPPRESS_HANG_6: If set to 1, hang pulses are suppressed in case of a checkstop.

Register Name	Pre-Counter Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.PRE_COUNTER_REG
Address	000000002E0F0028 (SCOM)
Description	Divider for hang counter clock

Bits	SCOM	Field Mnemonic: Description
0:7	RW	PRE_COUNTER: Divider for hang counter clock. Divides clock by n + 1. The default value for n = 0.

Register Name	eDRAM Status Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.EDRAM_STATUS
Address	000000002E0F0029 (SCOM)
Description	eDRAM control status register

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	EDRAM_STAT: eDRAM control status.

Register Name	NET CTRL0 Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.NET_CTRL0
Address	000000002E0F0040 (SCOM) 000000002E0F0041 (SCOM1) 000000002E0F0042 (SCOM2)
Description	NET CTRL0 register. (N/A in pervasive chiplet.)

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	CHIPLET_ENABLE: Set if chiplet is good.
1	RWX	RWX_WAND	RWX_WOR	PCB_EP_RESET: Output is ORed to the global EP reset.
2	RWX	RWX_WAND	RWX_WOR	CLK_ASYNC_RESET: For a POWER9 cache chiplet, the EQ skew adjustment is reset. For a POWER9 core chiplet, the core duty cycle adjustment is reset. For a POWER9 memory chiplet, the memory asynchronous glitchless multiplexer is reset.
3	RWX	RWX_WAND	RWX_WOR	PLL_TEST_EN: Test enable for chiplet PLL.
4	RWX	RWX_WAND	RWX_WOR	PLL_RESET: Reset for chiplet PLL.
5	RWX	RWX_WAND	RWX_WOR	PLL_BYPASS: Enable bypass for chiplet PLL.
6	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN: Scan control for chiplet vital domain.
7	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN_IN: Scan in for the chiplet vital domain.
8	RWX	RWX_WAND	RWX_WOR	VITAL_PHASE: Phase for vital domain.
9	RWX	RWX_WAND	RWX_WOR	FLUSH_ALIGN_OVR: Override flush, flush_nto1, align in chiplet to 1.
10	RWX	RWX_WAND	RWX_WOR	VITAL_AL: Align for vital domain.
11	RWX	RWX_WAND	RWX_WOR	ACT_DIS: LCB control signal for vital logic.
12	RWX	RWX_WAND	RWX_WOR	MPW1: LCB control signal for vital logic.
13	RWX	RWX_WAND	RWX_WOR	MPW2: LCB control signal for vital logic.
14	RWX	RWX_WAND	RWX_WOR	MPW3: LCB control signal for vital logic.
15	RWX	RWX_WAND	RWX_WOR	DELAY_LCLKR: LCB control signal for vital logic.
16	RWX	RWX_WAND	RWX_WOR	VITAL_THOLD: Thold for the chiplet vital domain.
17	RWX	RWX_WAND	RWX_WOR	FLUSH_SCAN_N: Flush scan control.
18	RWX	RWX_WAND	RWX_WOR	FENCE_EN: Fencing signal for chiplet.
19	RWX	RWX_WAND	RWX_WOR	CPLT_RCTRL: Chiplet receiver enable.
20	RWX	RWX_WAND	RWX_WOR	CPLT_DCTRL: Chiplet driver enable.
21	RWX	RWX_WAND	RWX_WOR	Reserved field.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
22	RWX	RWX_WAND	RWX_WOR	ADJ_FUNC_CLKSEL: POWER9 cache chiplet: Clock select for skew adjustment/duty cycle adjustment logic. POWER9 core chiplet: Skew sense to skew adjustment fencing.
23:24	RWX	RWX_WAND	RWX_WOR	Reserved field.
25	RWX	RWX_WAND	RWX_WOR	TP_FENCE_PCB: Fence the chiplet from the PCB bus. If set, PCB slave reports Chiplet Offline.
26	RWX	RWX_WAND	RWX_WOR	LVLTRANS_FENCE: Fence control for level translators.
27	RWX	RWX_WAND	RWX_WOR	ARRAY_WRITE_ASSIST_EN: Array write assist.
28	RWX	RWX_WAND	RWX_WOR	HTB_INTEST: HTB in test mode.
29	RWX	RWX_WAND	RWX_WOR	HTB_EXTEST: HTB in test mode.
30	RWX	RWX_WAND	RWX_WOR	Reserved field.
31	RWX	RWX_WAND	RWX_WOR	PLLFORCE_OUT_EN: PLL force out enable.

Register Name	**NET CTRL1 Register**
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.NET_CTRL1
Address	000000002E0F0044 (SCOM) 000000002E0F0045 (SCOM1) 000000002E0F0046 (SCOM2)
Description	NET CTRL1 Register. (N/A in pervasive chiplet.)

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	PLL_CLKIN_SEL: PLL clkin select.
1	RWX	RWX_WAND	RWX_WOR	CLK_DCC_BYPASS_EN: POWER9 cache chiplet: L2-0, L2-1, L3 duty cycle control bypass. POWER9 core chiplet: Core duty cycle control bypass. POWER9 memory chiplet: Memory duty cycle control bypass.
2	RWX	RWX_WAND	RWX_WOR	CLK_PDLY_BYPASS_EN: POWER9 cache chiplet: L2-0, L2-1, L3 progdly bypass. POWER9 core chiplet: Core progdly bypass. POWER9 memory chiplet: Memory progdly bypass.
3	RWX	RWX_WAND	RWX_WOR	CLK_DIV_BYPASS_EN: Enables clock divider bypass.
4	RWX	RWX_WAND	RWX_WOR	REFCLK_CLKMUX0_SEL: Select for reference clock mux0.
5	RWX	RWX_WAND	RWX_WOR	REFCLK_CLKMUX1_SEL: Select for reference clock mux1.
6	RWX	RWX_WAND	RWX_WOR	PLL_BNDY_BYPASS_EN: Bypass for IOP PLL.
7	RWX	RWX_WAND	RWX_WOR	Reserved field.
8:15	RWX	RWX_WAND	RWX_WOR	DPLL_TEST_SEL: DPLL testout multiplexing.
16:19	RWX	RWX_WAND	RWX_WOR	SB_STRENGTH: Sector buffer driver strength.
20	RWX	RWX_WAND	RWX_WOR	ASYNC_TYPE:
21	RWX	RWX_WAND	RWX_WOR	ASYNC_OBS:
22	RWX	RWX_WAND	RWX_WOR	CPM_CAL_SET: CPM calibrate.
23	RWX	RWX_WAND	RWX_WOR	SENSEADJ_RESET0: POWER9 cache chiplet: L2-0 duty cycle adjustment reset.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
24	RWX	RWX_WAND	RWX_WOR	SENSEADJ_RESET1: POWER9 cache chiplet: L2-1 duty cycle adjustment reset.
25	RWX	RWX_WAND	RWX_WOR	CLK_PULSE_EN: Clock pulse mode enable.
26:27	RWX	RWX_WAND	RWX_WOR	CLK_PULSE_MODE: Clock pulse mode setting.
28:31	RWX	RWX_WAND	RWX_WOR	Reserved field.

Register Name	**PPM General Power Management Mode Register**
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_GPMMR
Address	000000002E0F0100 (SCOM) 000000002E0F0101 (SCOM1) 000000002E0F0102 (SCOM2)
Description	PPM general power management mode register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_CLEAR	WOX_OR	Reserved field.
1	ROX	NCX	NCX	Reserved field.
2	ROX	NCX	NCX	Reserved field.
3	ROX	NCX	NCX	Reserved field.
4	ROX	NCX	NCX	Reserved field.
5	ROX	NCX	NCX	Reserved field.
6	RW	WO_CLEAR	WO_OR	Reserved field.
7	RW	WO_CLEAR	WO_OR	Reserved field.
8	RW	WO_CLEAR	WO_OR	Reserved field.
9	RW	WO_CLEAR	WO_OR	Reserved field.
10	RW	WO_CLEAR	WO_OR	Reserved field.
11	RO	NC	NC	Reserved field.
12:14	RW	WO_CLEAR	WO_OR	Reserved field.
15	RW	WO_CLEAR	WO_OR	Reserved field.
16:63	RO	RO	RO	constant = 0b000000000000000000000000000000000000000000000000

Register Name	**CPPM Core Power Management Mode Register**
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_CPMMR
Address	000000002E0F0106 (SCOM) 000000002E0F0107 (SCOM1) 000000002E0F0108 (SCOM2)
Description	CPPM core power management mode register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_CLEAR	WO_OR	CPPM_CPMMR_PPM_WRITE_DISABLE: Power management macro write access control. If set, PIB-sourced PCB writes to all core PPM registers except this register will return the resource-occupied PCB response code 0x1. Only CME PCB writes are allowed to the other core PMM registers. If clear, all core PPM register writes are permitted. Reads are not affected by the setting of this bit. Engineering Note: This bit blocks non-CME firmware from interfering with CME control of the PPM.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
1	RW	WO_CLEAR	WO_OR	CPPM_CPMMR_PPM_WRITE_OVERRIDE: Power management macro write override. If set, core PPM accesses are allowed from the PCB network even if PPM_WRITE_DISABLE is set. If clear, PPM_WRITE_DISABLE functionality is honored. Engineering Note: This bit is intended for lab use only as a means to handle potential CME hardware or firmware issues. If this bit is set, you must ensure that CME functionality is not compromised by writes from the PCB that disrupt CME operation.
2:8	RW	WO_CLEAR	WO_OR	CPPM_CPMMR_RESERVED_2_9: Implemented but not used.
9	RW	WO_CLEAR	WO_OR	CPPM_CPMMR_FUSED_CORE_MODE: A fused core mode input signal from the core pervasive unit. (Note that this bit also exists in the CPPM CME PECE Shadow Register.) Modifies interrupt mapping to physical core chiplets. This remapping is done by PPM hardware before applying the PECE bits in this register to them, such that the core PPM corresponding to the actual physical core chiplet being interrupted signals an interrupt to the CME or Stop GPE. 0 = The logic to physical core mapping is sequential (that is, Thread[0,1,2,3] is routed to Core0; and Thread[4,5,6,7] is routed to Core1). 1 = Even threads are routed to Core0 and odd threads are routed to Core1. The interrupts are routed as follows: Thread[0,2,4,6] to Core0; Thread[1,3,5,7] to Core1.
10	RW	WO_CLEAR	WO_OR	CPPM_CPMMR_STOP_EXIT_TYPE_SEL: Use type 3 instead of type 2 interrupts for stop exit interrupt generation (reference to the PIG register).
11	RW	WO_CLEAR	WO_OR	CPPM_CPMMR_BLOCK_INTR_INPUTS: When set, this bit blocks incoming interrupts from causing interrupts from being REQUESTED as wake-up sources but allows them to be sampled as PRESENT.
12	RW	WO_CLEAR	WO_OR	CPPM_CPMMR_CME_ERR_NOTIFY_DIS: By default, PPM sends notification to the OCC complex upon the rising edge of a CME error indication. When this bit is set, no action is taken by PPM in response to the CME error input.
13	RW	WO_CLEAR	WO_OR	CPPM_CPMMR_WKUP_NOTIFY_SELECT: Causes all enabled wake-up events (special and regular) to cause a wake-up notification to be automatically generated by PPM hardware to the OCC complex. When this bit is not set, no notification is sent to OCC because the events will instead be sent to CME.
14	RW	WO_CLEAR	WO_OR	CPPM_CPMMR_ENABLE_PECE: When zero, all regular wake-up interrupt sources cause the QUAD to wake up regardless of the PECE settings.
15	RWX	WOX_CLEAR	WOX_OR	CPPM_CPMMR_CME_SPECIAL_WKUP_DONE_DIS: When not set and when WKUP_NOTIFY_SELECT = 0, GPMMR[SPECIAL_WKUP_DONE] follows the signal input from CME and cannot be written by SCOM. When set (or when WKUP_NOTIFY_SELECT = 1), GPMMR[SPECIAL_WKUP_DONE] is only controllable through SCOM.
16:63	RO	RO	RO	constant = 0b000000000000000000000000000000000000000000000000

Register Name	PPM Special Wake-Up OTR Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_SPWKUP_OTR
Address	000000002E0F010A (SCOM)
Description	PPM special wake-up OTR register

Bits	SCOM	Field Mnemonic: Description
0	RW	PPM_SPWKUP_OTR_OTR_SPECIAL_WKUP: Chiplet special wake-up for other firmware use. Note: Protocol is required when setting this bit.
1:63	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000000

Register Name	PPM Special Wake-Up FSP Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_SPWKUP_FSP
Address	000000002E0F010B (SCOM)
Description	PPM special wake-up FSP register

Bits	SCOM	Field Mnemonic: Description
0	RW	PPM_SPWKUP_FSP_FSP_SPECIAL_WKUP: Chiplet special wake-up for FSP firmware use. Note: Protocol is required when setting this bit.
1:63	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000000

Register Name	PPM Special Wake-Up OCC Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_SPWKUP_OCC
Address	000000002E0F010C (SCOM)
Description	PPM special wake-up OCC register

Bits	SCOM	Field Mnemonic: Description
0	RW	PPM_SPWKUP_OCC_OCC_SPECIAL_WKUP: Chiplet special wake-up for OCC firmware use. Note: Protocol is required when setting this bit.
1:63	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000000

Register Name	PPM Special Wake-Up HYP Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_SPWKUP_HYP
Address	000000002E0F010D (SCOM)
Description	PPM special wake-up HYP register

Bits	SCOM	Field Mnemonic: Description
0	RW	PPM_SPWKUP_HYP_HYP_SPECIAL_WKUP: Chiplet special wake-up for HYP firmware use. Note: Protocol is required when setting this bit.
1:63	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000000

Register Name	PPM Stop State History SRC Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_SSHSRC
Address	000000002E0F0110 (SCOM)
Description	PPM stop state history SRC register

Bits	SCOM	Field Mnemonic: Description
0	RW	Reserved field.

Bits	SCOM	Field Mnemonic: Description
1	ROX	Reserved field.
2:3	RW	Reserved field.
4:7	RW	Reserved field.
8:11	RW	Reserved field.
12	WO_4P	Reserved field.
13	WO_4P	Reserved field.
14:63	RO	constant = 0b00000000000000000000000000000000000000000000000000

Register Name	PPM Stop State History FSP Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_SSHFSP
Address	000000002E0F0111 (SCOM)
Description	PPM stop state history FSP register

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	Reserved field.
2:3	ROX	Reserved field.
4:7	ROX	Reserved field.
8:11	ROX	Reserved field.
12:15	ROX_CLRPART	Reserved field.
16:19	ROX_CLRPART	Reserved field.
20	ROX_CLRPART	Reserved field.
21:63	RO	constant = 0b0000000000000000000000000000000000000000000

Register Name	PPM Stop State History OCC Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_SSHOCC
Address	000000002E0F0112 (SCOM)
Description	PPM stop state history OCC register

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	Reserved field.
2:3	ROX	Reserved field.
4:7	ROX	Reserved field.
8:11	ROX	Reserved field.
12:15	ROX_CLRPART	Reserved field.

Bits	SCOM	Field Mnemonic: Description
16:19	ROX_CLRPART	Reserved field.
20	ROX_CLRPART	Reserved field.
21:63	RO	constant = 0b0000000000000000000000000000000000000000000

Register Name	PPM Stop State History OTR Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_SSHOTR
Address	000000002E0F0113 (SCOM)
Description	PPM stop state history OTR register

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	Reserved field.
2:3	ROX	Reserved field.
4:7	ROX	Reserved field.
8:11	ROX	Reserved field.
12:15	ROX_CLRPART	Reserved field.
16:19	ROX_CLRPART	Reserved field.
20	ROX_CLRPART	Reserved field.
21:63	RO	constant = 0b0000000000000000000000000000000000000000000

Register Name	PPM Stop State History HYP Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_SSHHYP
Address	000000002E0F0114 (SCOM)
Description	PPM stop state history HYP register

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	Reserved field.
2:3	ROX	Reserved field.
4:7	ROX	Reserved field.
8:11	ROX	Reserved field.
12:15	ROX_CLRPART	Reserved field.
16:19	ROX_CLRPART	Reserved field.
20	ROX_CLRPART	Reserved field.

Bits	SCOM	Field Mnemonic: Description
21:63	RO	constant = 0b0000000000000000000000000000000000000000000

Register Name	PPM PFET Control State Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_PFCS
Address	000000002E0F0118 (SCOM) 000000002E0F0119 (SCOM1) 000000002E0F011A (SCOM2)
Description	PPM PFET control state register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:1	RW	WO_CLEAR	WO_OR	PPM_PFCS_VDD_PFET_FORCE_STATE: Domain VDD PFET force state. Provides a means for firmware to force the domain VDD PFETs to well known end states using the hardware sequencing mechanisms: b00 = No operation. b01 = Force Voff. b10 = No operation (reserved). b11 = Force Von. This field is valid only if bits 4:5 = 00 (that is, both vdd_pfet_val_override and vdd_pfet_sel_override are disabled).
2:3	RW	WO_CLEAR	WO_OR	PPM_PFCS_VCS_PFET_FORCE_STATE: Domain VCS PFET force state. This field is used only in QUAD PPM; it is unused in Core PPM. It provides a means for firmware to force the domain VCS PFETs to well known end states using the hardware sequencing mechanisms: b00 = No operation. b01 = Force Voff. b10 = No operation (reserved). b11 = Force Von. This field is valid only if bits 6:7 = 00 (that is, both vcs_pfet_val_override and vcs_pfet_sel_override are disabled).
4	RW	WO_CLEAR	WO_OR	PPM_PFCS_VDD_PFET_VAL_OVERRIDE: Domain VDD PFET value override.
5	RW	WO_CLEAR	WO_OR	PPM_PFCS_VDD_PFET_SEL_OVERRIDE: Domain VDD PFET stage select override.
6	RW	WO_CLEAR	WO_OR	PPM_PFCS_VCS_PFET_VAL_OVERRIDE: Domain VCS PFET value override. For QUAD PPM use only. Unused in Core PPM.
7	RW	WO_CLEAR	WO_OR	PPM_PFCS_VCS_PFET_SEL_OVERRIDE: Domain VCS PFET stage select override. For QUAD PPM use only. Unused in Core PPM.
8	RW	WO_CLEAR	WO_OR	PPM_PFCS_VDD_PFET_REGULATION_FINGER_EN: Domain VDD PFET regulation finger enable. Intended to be used to control the regulation PFET enable when iVRMs are enabled. If this bit is asserted, the value of the PFET finger (pfet_enable(0)) is controlled by vdd_pfet_regulation_finger_value. If this bit is not asserted, the PFET finger is controlled by the PFET FSM and/or any relevant overrides in place.
9	RW	WO_CLEAR	WO_OR	PPM_PFCS_VDD_PFET_REGULATION_FINGER_VALUE: Domain VDD PFET regulation finger value. Intended to be used to control the regulation PFET enable when IVRMs are enabled. If vdd_pfet_regulation_finger_enable = 1, a write to this bit sets the state of the VDD PFET enable(0) regardless of the setting of the regular pfet_enable FSM. If it is not asserted, the PFET sequencer controls this finger with the vdd_pfet_enable_value.
10:11	RW	WO_CLEAR	WO_OR	PPM_PFCS_RESERVED_10_11: Implemented but unused.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
12:19	RW	WO_CLEAR	WO_OR	PPM_PFCS_VDD_PFET_ENABLE_VALUE: VDD PFET enable value. Intended for manual control override usage. A write to this field sets the state of the Core Domain PFET Enables directly. If vdd_pfet_val_override = 1, a write to this field sets the state of the core PFET Enables until core_vdd_pfet_val_override is cleared. If vdd_pfet_val_override = 0, a write to this field takes on the value for one cycle and then returns to the value produced by the core_vdd_pfet_valN hard-coded facilities. A write of this type is not recommended and might produce undefined results. Reads will return the present state.

20:23	RW	WO_CLEAR	WO_OR	PPM_PFCS_VDD_PFET_SEL_VALUE: VDD PFET select value. Intended for manual control override usage. A write to this field will index value N into the vdd_power_enable register, where N is 0 to 8, if vdd_pfet_sel_override = 1. If vdd_pfet_sel_override = 0, the field is written but no further action is taken. 0x0 = 0b11111111 # On.
				0x1 = 0b01111111.
				0x2 = 0b00111111.
				0x3 = 0b00011111.
				0x4 = 0b00001111.
				0x5 = 0b00000111.
				0x6 = 0b00000011.
				0x7 = 0b00000001.
				0x8 = 0b00000000 # Off.
				0x9 to 0xF = Reserved reads will return the present state of the field.

24:31	RW	WO_CLEAR	WO_OR	PPM_PFCS_VCS_PFET_ENABLE_VALUE: VCS PFET enable value. This field is used only in QUAD PPM; it is unused in Core PPM. It is intended for manual control override usage. A write to this field sets the state of the VCS PFET Enables directly. If vcs_pfet_val_override = 1, a write to this field sets the state of the VCS PFET Enables until vcs_pfet_val_override is cleared. If eco_vdd_pfet_val_override = 0, a write to this field takes on the value for one cycle and then returns to the value produced by the eco_vdd_pfet_valN_slat registers. A write of this type is not recommended and might produce undefined results. Reads will return the present state.

32:35	RW	WO_CLEAR	WO_OR	PPM_PFCS_VCS_PFET_SEL_VALUE: VCS PFET select value. This field is used only in QUAD PPM; it is unused in Core PPM. It is intended for manual control override usage. A write to this field will index value N into the vcs_power_enable register, where N is 0 to 8, if vcs_pfet_sel_override = 1. If vcs_pfet_sel_override = 0, the field is written but no further action is taken.
				0x0 = 0b11111111 # On.
				0x1 = 0b01111111.
				0x2 = 0b00111111.
				0x3 = 0b00011111.
				0x4 = 0b00001111.
				0x5 = 0b00000111.
				0x6 = 0b00000011.
				0x7 = 0b00000001.
				0x8 = 0b00000000 # Off.
				0x9 to 0xF = Reserved. Reads will return the present state of the field.

36:41	RO	RO	RO	constant = 0b000000
42:45	ROX	NCX	NCX	PPM_PFCS_VDD_PG_STATE: Logic voltage power gate sequencer FSM (one hot): 0x8 = Idle. 0x4 = Increment. 0x2 = Decrement. 0x1 = Wait.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
46:49	ROX	NCX	NCX	PPM_PFCS_VDD_PG_SEL: For debug, contains the actual index N of the domain VDD PFET select value. See VDD_PFET_SEL_VALUE for encoding of N to power enable value.
50:53	ROX	NCX	NCX	PPM_PFCS_VCS_PG_STATE: Cache voltage domain power gate sequencer FSM (one hot). This field is used only in QUAD PPM; it is unused in Core PPM. 0x8 = Idle. 0x4 = Increment. 0x2 = Decrement. 0x1 = Wait.
54:57	ROX	NCX	NCX	PPM_PFCS_VCS_PG_SEL: This field is used only in QUAD PPM; it is unused in Core PPM. For debug, contains the actual index N of the domain VCS PFET select value. See VCS_PFET_SEL_VALUE for encoding of N to power enable value.
58:63	RO	RO	RO	constant = 0b000000

Register Name	PPM PFET Delay Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_PFDLY
Address	000000002E0F011B (SCOM)
Description	PPM PFET delay register

Bits	SCOM	Field Mnemonic: Description
0:3	RW	PPM_PFDLY_POWDN_DLY: Delay used between steps powering down the domain. The delays in this register are in terms of the PPM clock period (2 ns) ´ 2(15 minus this value). Note: Chooses the power of 2 bit position of pfet_pg_timer(0:15) which is running off pcb_nclk.
4:7	RW	PPM_PFDLY_POWUP_DLY: Delay used between steps powering up the domain. The delays in this register are in terms of the PPM clock period (2 ns) ´ 2(15 minus this value). Note: Chooses the power of 2 bit position of pfet_pg_timer(0:15) which is running off pcb_nclk.
8:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	PPM PFET Sense Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_PFSNS
Address	000000002E0F011C (SCOM)
Description	PPM PFET sense register

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field.
1	ROX	Reserved field.
2	ROX	Reserved field.
3	ROX	Reserved field.
4:15	RO	Reserved field.
16:23	ROX	Reserved field.
24:31	ROX	Reserved field.
32:41	RO	constant = 0b0000000000

Bits	SCOM	Field Mnemonic: Description
42:45	ROX	Reserved field.
46:49	ROX	Reserved field.
50:53	ROX	Reserved field.
54:57	ROX	Reserved field.
58:63	RO	constant = 0b000000

Register Name	PPM PFET Off Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_PFOFF
Address	000000002E0F011D (SCOM)
Description	PPM PFET off register

Bits	SCOM	Field Mnemonic: Description
0:3	RW	PPM_PFOFF_VDD_VOFF_SEL: Pointer to the stage representing the Voff value for the VDD PFETs. Power down sequences will stop after enabling this stage. Valid values: 0x0 through 0x8.
4:7	RW	PPM_PFOFF_VCS_VOFF_SEL: Pointer to the stage representing the Voff value for the VCS PFETs. Power down sequences will stop after enabling this stage. Valid values: 0x0 through 0x8. This field is used only in QUAD PPM; it is unused in Core PPM.
8:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	PPM SCRATCH0 Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_SCRATCH0
Address	000000002E0F011E (SCOM)
Description	PPM SCRATCH0 register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	PPM_SCRATCH0_DATA: Scratch Data 0.

Register Name	PPM SCRATCH1 Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_SCRATCH1
Address	000000002E0F011F (SCOM)
Description	PPM SCRATCH1 register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	PPM_SCRATCH1_DATA: Scratch Data 1.

Register Name	CPPM PERRSUM Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_PERRSUM
Address	000000002E0F0120 (SCOM)
Description	CPPM PERRSUM register

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	CPPM_PERRSUM_CPPM_ERROR: Indicates a CPPM error is present. Intended for use by special PCB multicast to see the error state of all chiplets with a single read.
1:63	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000000

Register Name	CPPM Error Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_ERR
Address	000000002E0F0121 (SCOM)
Description	CPPM error register

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	CPPM_ERR_PCB_INTERRUPT_PROTOCOL_ERR: Firmware wrote the PIG to request a PCB interrupt before its previously requested interrupt had been completed (that is, PIG[PENDING_SOURCE(0)] = 1 OR (PIG[INTR_GRANTED] AND [GRANTED_SOURCE](0)) = 1).
1	RWX_WCLEAR	CPPM_ERR_SPECIAL_WKUP_PROTOCOL_ERR: Firmware cleared its special wake-up request (indicated by GPMMR[SPECIAL_WKUP_REQUESTED] before GPMMR[SPECIAL_WKUP_DONE] was set. This violates the agreed upon protocol and potentially confuses the Hcode managing the state of the QUAD chiplets.
2	RWX_WCLEAR	CPPM_ERR_SPECIAL_WKUP_DONE_PROTOCOL_ERR: Hardware or firmware cleared the special wake-up done indicator after it was set although a special wake-up request was still active (indicated by GPMMR[SPECIAL_WKUP_REQUESTED]. This violates the agreed upon protocol and potentially confuses the Hcode managing the state of the QUAD (cache and core) chiplets.
3	RWX_WCLEAR	CPPM_ERR_PFET_SEQ_PROGRAM_ERR: The PFET sequencer reached an invalid state due to incorrect configuration by a program.
4	RWX_WCLEAR	CPPM_ERR_CLK_SYNC_ERR: The SKEWADJ macro violated the agreed protocol by changing the value of the CLK_SYNC_DONE without a corresponding CLK_SYNC_ENABLE change (that is, the rising edge of the DONE when ENABLE = 0 or the falling edge of the DONE when ENABLE = 1).
5	RWX_WCLEAR	CPPM_ERR_PECE_INTR_DISABLED: Any of the three core external interrupt wake-up sources (OS, HYP, and MSGSND) are present but disabled by the thread's PECE when it is in stop state. For lab use only to notify firmware that a PECE-masked interrupt is being sent without a core that is enabled to receive it. Note: This does not include the malfunction alert. Note: This can only logically occur when CPMMR[ENABLE_PECE] and USE_PECE for the corresponding thread are both set and chiplet enable is set and the corresponding PECE bit for that thread for that interrupt is 0.
6	RWX_WCLEAR	CPPM_ERR_DECONFIGURED_INTR: Any of the four core external interrupts (EBB, OS, HYP, or MSGSND) are present but the chiplet is deconfigured (based on the chiplet enable input from PCBSLAVE). Note: Does not include the malfunction alert.
7	RO	CPPM_ERR_RESERVED_7: Implemented but unused.
8:11	RO	CPPM_ERR_RESERVED_8_11: Implemented but unused.
12:63	RO	constant = 0b0000000000000000000000000000000000000000000000000000

Register Name	CPPM Error Mask Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_ERRMSK
Address	000000002E0F0122 (SCOM)
Description	CPPM error mask register

Bits	SCOM	Field Mnemonic: Description
0:11	RW	CPPM_ERRMSK_RESERVED_0_11: Mask for this error: 0 = Not masked. 1 = Masked. When set, the corresponding bit is set in the Error Register but masked from being reported in the ERRSUM Register and to the FIR.
12:63	RO	constant = 0b0000000000000000000000000000000000000000000000000000

Register Name	CPPM NC0 Indirect Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_NC0INDIR
Address	000000002E0F0130 (SCOM) 000000002E0F0131 (SCOM1) 000000002E0F0132 (SCOM2)
Description	CPPM NC0 indirect register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:31	RO	NC	NC	Reserved field.
32:63	RO	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	CPPM NC1 Indirect Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_NC1INDIR
Address	000000002E0F0133 (SCOM) 000000002E0F0134 (SCOM1) 000000002E0F0135 (SCOM2)
Description	CPPM NC1 indirect register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:31	RO	NC	NC	Reserved field.
32:63	RO	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	CPPM Core PPM Scratch Atomic Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_CSAR
Address	000000002E0F0138 (SCOM) 000000002E0F0139 (SCOM1) 000000002E0F013A (SCOM2)
Description	CPPM core PPM scratch atomic register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:31	RW	WO_CLEAR	WO_OR	CPPM_CSAR_SCRATCH_ATOMIC_DATA: Scratch atomic data.
32:63	RO	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	PPM Clock Grid Control Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_CGCR
Address	000000002E0F0164 (SCOM)
Description	PPM clock grid control register

Bits	SCOM	Field Mnemonic: Description
0	RW	PPM_CGCR_CLKGLM_ASYNC_RESET: Glitchless clock multiplexer asynchronous reset for this chiplet.
1:2	RW	PPM_CGCR_RESERVED_1_2: Implemented but not used.
3	RW	PPM_CGCR_CLKGLM_SEL: Glitchless clock multiplexer select for this chiplet. 0 = Reference clock. 1 = DPLL output (full speed Div1 for Core, half speed Div2 for Cache).
4:63	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000

Register Name	CPPM Core Analog Clock Control Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_CACCR
Address	000000002E0F0168 (SCOM) 000000002E0F0169 (SCOM1) 000000002E0F016A (SCOM2)
Description	CPPM core analog clock control register. Notes: 1. The first 8 bits (0:7) of this register are used if QUAD_CLK_SB_OVERRIDE is not set, otherwise use corresponding bits from the QACCR. 2. Bits 8 to 12 are used if QUAD_CLK_SW_OVERRIDE is not set, otherwise use corresponding bits from QACCR.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:3	RW	WO_CLEAR	WO_OR	CPPM_CACCR_CLK_SB_STRENGTH: Clock sector buffer strength(0:3) for this core chiplet.
4	RW	WO_CLEAR	WO_OR	CPPM_CACCR_CLK_SB_SPARE: Implemented but not used.
5	RW	WO_CLEAR	WO_OR	CPPM_CACCR_CLK_SB_PULSE_MODE_EN: Pulse mode enable to clock sector buffers for this core chiplet.
6:7	RW	WO_CLEAR	WO_OR	CPPM_CACCR_CLK_SB_PULSE_MODE: Pulse mode(0:1) to clock sector buffers for this core chiplet: 00 = Safest (Widest) Pulse. 01 = Wide Pulse. 10 = Narrow Pulse. 11 = Medium Pulse.
8:11	RW	WO_CLEAR	WO_OR	CPPM_CACCR_CLK_SW_RESCLK: Resonant clock inductor switch(0:3) for this core chiplet.
12	RW	WO_CLEAR	WO_OR	CPPM_CACCR_CLK_SW_SPARE: Implemented but not used.
13	RW	WO_CLEAR	WO_OR	CPPM_CACCR_QUAD_CLK_SB_OVERRIDE: Use input signals from QACCR(0:7) (instead of this register) to feed the clock sector buffer controls for this chiplet.
14	RW	WO_CLEAR	WO_OR	CPPM_CACCR_QUAD_CLK_SW_OVERRIDE: Use input signals from QACCR(8:12) (instead of this register) to feed the resonant clock switch controls for this chiplet.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
15	RW	WO_CLEAR	WO_OR	CPPM_CACCR_CLK_SYNC_ENABLE: Clock sync enable for this core chiplet to the analog clock SKEWADJ macro. Firmware must assert, then wait for the corresponding CACSR bit to assert, before enabling at-speed (non-reference clock) functional clocks on the grid. Likewise, firmware must must deassert, and wait for the corresponding CACSR bit to deassert, before switching the clock grid away from full speed clocks (that is, DPLL). This signal must remain asserted for the clock grid to remain synchronous with the other (L2 and L3) grids in the QUAD.
16:63	RO	RO	RO	constant = 0b000000000000000000000000000000000000000000000000

Register Name	CPPM Core Analog Clocking Status Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_CACSR
Address	000000002E0F016B (SCOM)
Description	CPPM core analog clocking status register

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	CPPM_CACSR_ACTUAL_CLK_SB_STRENGTH: Actual value being driven on the sector buffer strength(0:3) output for this core chiplet.
4	ROX	CPPM_CACSR_ACTUAL_CLK_SB_SPARE: Spare (not used).
5	ROX	CPPM_CACSR_ACTUAL_CLK_SB_PULSE_MODE_EN: Actual value being driven on the pulse mode enable output for this core chiplet.
6:7	ROX	CPPM_CACSR_ACTUAL_CLK_SB_PULSE_MODE: Actual value being driven on the pulse mode(0:1) output for this core chiplet.
8:11	ROX	CPPM_CACSR_ACTUAL_CLK_SW_RESCLK: Actual value being driven on the resonant clock inductor switch(0:3) output for this core chiplet.
12	ROX	CPPM_CACSR_ACTUAL_CLK_SW_SPARE: Spare (not used).
13	ROX	CPPM_CACSR_CLK_SYNC_DONE: Clock sync done for this core chiplet. When changing the CACCR[CLK_SYNC_ENABLE] bit, code must wait for this bit to transition to the same value before proceeding. The SKEWADJ macro is not allowed to change the value of this signal unless the corresponding enable changes first, otherwise the corresponding ERR_REG[CLK_SYNC_ERR] will be set. Note: This signal will be asserted whenever SKEWADJ is in hold mode.
14:63	RO	constant = 0b00000000000000000000000000000000000000000000000000

Register Name	PPM PCB Interrupt Generation Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_PIG
Address	000000002E0F0180 (SCOM)
Description	PPM PCB interrupt generation register

Bits	SCOM	Field Mnemonic: Description
0	RO	constant = 0b1
1:3	RW	PPM_PIG_REQ_INTR_TYPE: PCB interrupt request type (written by Hcode).
4:15	RW	PPM_PIG_REQ_INTR_PAYLOAD: PCB interrupt request payload (written by Hcode).

Bits	SCOM	Field Mnemonic: Description
16:31	ROX	PPM_PIG_GRANTED_PACKET: Granted interrupt packet content. If INTR_GRANTED is 1, this field contains the interrupt currently being sent; otherwise, this field contains the interrupt most recently sent. The format depends on the value of the GRANTED_SOURCE field: 01 = Copied from bits 0:15 of this register. 10 = Core = 0x[AB]YXW; QUAD = 0xE80W. 11 = Core = 0xD801; QUAD = 0xF80Z. where: [A or B] is decided by CPMMR[STOP_EXIT_TYPE_SEL]. Y = 0x8, or 0xC if malfunction alert is present. X = The state of the external interrupts (MSGSND, OS, HYP, '0'). W = The state of the four special wake-up sources (OTR, FSP, OCC, HYP). Z = Encoded hardware error indication (0; voltage droop; iVRM dropout; OCC heartbeat loss). Note: By convention, bit 4, when set, typically indicates a hardware-generated interrupt, although for the QUAD type 6 and 7, this bit is not latched in the OCB.
32	ROX	PPM_PIG_INTR_GRANTED: An interrupt request is in process. The value of this bit determines the meaning of the other bits in this register: 0 = Contains information about the most recent interrupt that was sent. 1 = Reflects the interrupt currently being sent. This bit is set when the arbiter issues a grant to the source reflected in the GRANTED_SOURCE field. This bit is cleared when the granted interrupt receives a Receive ACK.
33	RO	constant = 0b0
34:35	ROX	PPM_PIG_GRANTED_SOURCE: Interrupt source currently or most recently granted to place an interrupt on the PCB network (encoded). 00 = No interrupt has ever been processed. 01 = SCOM request (maps to PENDING_SOURCE 001). 10 = Hardware stop exit (maps to PENDING_SOURCE 010). 11 = Hardware error notification (maps to PENDING_SOURCE 100).
36	RO	constant = 0b0
37:39	ROX	PPM_PIG_PENDING_SOURCE: Bit per interrupt source indicating which are currently waiting for arbitration. xx1 = SCOM request from CME (in bits 0:15 of this register). x1x = Hardware stop exit. 1xx = Hardware error (CPPM: CME; QPPM: OCC heartbeat).
40	RWX_WCLEAR	PPM_PIG_NETWORK_RESET_OCCURRED: Sticky bit set when a network reset occurs (for debug use only) and cleared only on a SCOM write of this bit to one. Note: For indication only; network reset has no other effect on PPM.
41:63	RO	constant = 0b00000000000000000000000

Register Name	CPPM Core PPM CME Doorbell 0 Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_CMEDB0
Address	000000002E0F0190 (SCOM) 000000002E0F0191 (SCOM1) 000000002E0F0192 (SCOM2)
Description	CPPM core PPM CME doorbell register 0

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:7	RW	WO_CLEAR	WO_OR	CPPM_CMEDB0_CME_MESSAGE_NUMBER0: CME message number. These bits are ORed together with the resulting logical value pulsing the cme_doorbell_0 CME interrupt on an SCOM write to this register. 0x00 = Does not pulse the cme_doorbell_0. Allows code to modify this register without generating an interrupt to the CME. 0x01 through 0xFF = Usage meaning is defined by CME and GPE firmware design.
8:63	RW	WO_CLEAR	WO_OR	CPPM_CMEDB0_CME_MESSAGE_HI: CME message high portion GPE and CME firmware design may use CME_MESSAGE_REG for any low portion of a message.

Register Name	CPPM CME Doorbell 1 Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_CMEDB1
Address	000000002E0F0194 (SCOM) 000000002E0F0195 (SCOM1) 000000002E0F0196 (SCOM2)
Description	CPPM CME doorbell register 1

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:7	RW	WO_CLEAR	WO_OR	CPPM_CMEDB1_CME_MESSAGE_NUMBER_N: CME message number. These bits are ORed together with the resulting logical value pulsing the cme_doorbell_[n] CME interrupt on an SCOM write to this register. 0x00 = Does not pulse the cme_doorbell_[n]. Allows code to modify this register without generating an interrupt to the CME. 0x01 through 0xFF = Usage meaning is defined by CME and GPE firmware design.
8:63	RO	RO	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	CPPM CME Doorbell 2 Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_CMEDB2
Address	000000002E0F0198 (SCOM) 000000002E0F0199 (SCOM1) 000000002E0F019A (SCOM2)
Description	CPPM CME doorbell register 2

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:7	RW	WO_CLEAR	WO_OR	CPPM_CMEDB2_CME_MESSAGE_NUMBER_N: The CME message number. These bits are ORed together with the resulting logical value pulsing the cme_doorbell_[n] CME interrupt on an SCOM write to this register. 0x00 = Does not pulse the cme_doorbell_[n]. Allows code to modify this register without generating an interrupt to the CME. 0x01 through 0xFF = Usage meaning is defined by CME and GPE firmware design.
8:63	RO	RO	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	CPPM CME Doorbell 3 Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_CMEDB3
Address	000000002E0F019C (SCOM) 000000002E0F019D (SCOM1) 000000002E0F019E (SCOM2)
Description	CPPM CME doorbell register 3

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:7	RW	WO_CLEAR	WO_OR	CPPM_CMEDB3_CME_MESSAGE_NUMBER_N: The CME message number. These bits are ORed together with the resulting logical value pulsing the cme_doorbell_[n] CME interrupt on an SCOM write to this register. 0x00 = Does not pulse the cme_doorbell_[n]. Allows code to modify this register without generating an interrupt to the CME. 0x01 through 0xFF = Usage meaning is defined by CME and GPE firmware design.
8:63	RW	WO_CLEAR	WO_OR	CPPM_CMEDB3_CME_MESSAGE_HI: CME message high portion of GPE and CME firmware design can use CME_MESSAGE_REG for any low portion of a message.

Register Name	CPPM CME Data Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_CMEDATA
Address	000000002E0F01A8 (SCOM) 000000002E0F01A9 (SCOM1) 000000002E0F01AA (SCOM2)
Description	CPPM CME data register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:31	RW	WO_CLEAR	WO_OR	CPPM_CMEDATA_DATA: The CME data contents are defined by the GPE and/or CME Hcode design.
32:63	RO	RO	RO	constant = 0b00000000000000000000000000000000

Register Name	CPPM CME Message Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_CMEMSG
Address	000000002E0F01AB (SCOM)
Description	CPPM CME message register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CPPM_CMEMSG_CME_MESSAGE: The CME message contents are defined by GPE and CME firmware design.

Register Name	CPPM Core PPM Interrupt Injection Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_CIIR
Address	000000002E0F01AD (SCOM)
Description	CPPM core PPM interrupt injection register

Bits	SCOM	Field Mnemonic: Description
0:27	RO	constant = 0b0000000000000000000000000000
28:31	WO_4P	Reserved field.
32:63	RO	constant = 0b00000000000000000000000000000000

Register Name	**CPPM Core PPM Interrupt Source Register**
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_CISR
Address	000000002E0F01AE (SCOM)
Description	CPPM Core PPM interrupt source register

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	Reserved field.
4:7	ROX	Reserved field.
8:11	ROX	Reserved field.
12:15	ROX	Reserved field.
16:19	ROX	Reserved field.
20:23	ROX	Reserved field.
24:27	ROX	Reserved field.
28:31	ROX	Reserved field.
32	ROX	Reserved field.
33	ROX	Reserved field.
34	ROX	Reserved field.
35	ROX	Reserved field.
36:63	RO	constant = 0b0000000000000000000000000000

Register Name	**CPPM CME PECE Shadow Register**
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_PECES
Address	000000002E0F01AF (SCOM)
Description	CPPM CME PECE shadow register

Bits	SCOM	Field Mnemonic: Description
0:5	RW	Reserved field.
6:7	RO	constant = 0b00
8:13	RW	Reserved field.
14:15	RO	constant = 0b00
16:21	RW	Reserved field.
22:23	RO	constant = 0b00
24:29	RW	Reserved field.
30:31	RO	constant = 0b00
32:35	RW	Reserved field.

Bits	SCOM	Field Mnemonic: Description
36	RW	Reserved.
37:63	RO	constant = 0b000000000000000000000000000

Register Name	PPM iVRM Control Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_IVRMCR
Address	000000002E0F01B0 (SCOM) 000000002E0F01B1 (SCOM1) 000000002E0F01B2 (SCOM2)
Description	PPM iVRM Control Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_CLEAR	WO_OR	PPM_IVRMCR_IVRM_VID_VALID: VID valid signal. 0 = Deassert valid signal. 1 = Assert valid signal. Upon rising edge of this signal, the iVRM circuit samples the VID and PFET_STRENGTH values provided by the IVRMDVR. QUAD PPM usage: These bits are always sent to the cache iVRM and all core PPMs, where it is forwarded to each core chiplet iVRM unless it is locally overridden in its core PPM. Core PPM usage: If CIVRMLCR[IVRM_LOCAL_CONTROL] = 1, these values are driven to the Core iVRM. Otherwise, the value driven comes from input pins from the QUAD PPM IVRMDVR.
1	RW	WO_CLEAR	WO_OR	PPM_IVRMCR_IVRM_BYPASS_B: Internal VRM VDD bypass (negative active). QUAD PPM usage: These bits are always sent to the cache iVRM and all core PPMs, where it is forwarded to each core chiplet iVRM unless it is locally overridden in its core PPM. Core PPM usage: If CIVRMLCR[IVRM_LOCAL_CONTROL] = 1, these values are driven to the core iVRM. Otherwise, the value driven comes from input pins from the QUAD PPM IVRMDVR.
2	RW	WO_CLEAR	WO_OR	PPM_IVRMCR_IVRM_POWERON: Internal VRM VDD power on. QUAD PPM usage: These bits are always sent to the cache iVRM and all core PPMs, where it is forwarded to each core chiplet iVRM unless it is locally overridden in its core PPM. Core PPM usage: If CIVRMLCR[IVRM_LOCAL_CONTROL] = 1, these values are driven to the core iVRM. Otherwise, the value driven comes from input pins from the QUAD PPM IVRMDVR.
3	RW	WO_CLEAR	WO_OR	PPM_IVRMCR_IVRM_VREG_SLOW_DC: Must be set before doing rapid changes (for example, dropping to Vmin), even after turning off clocks. This is needed to avoid trying to get there too fast and losing stability of the internal iVRM VID movement loop. QUAD PPM usage: These bits are always sent to the cache iVRM and all core PPMs, where it is forwarded to each core chiplet iVRM unless it is locally overridden in its core PPM. Core PPM usage: If CIVRMLCR[IVRM_LOCAL_CONTROL] = 1, these values are driven to the core iVRM. Otherwise, the value driven comes input pins from the QUAD PPM IVRMDVR.
4:7	RW	WO_CLEAR	WO_OR	PPM_IVRMCR_RESERVED_4_7: Implemented but unused.
8:63	RO	RO	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	PPM iVRM Status Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_IVRMST
Address	000000002E0F01B3 (SCOM)
Description	PPM iVRM status register

Bits	SCOM	Field Mnemonic: Description
0	ROX	PPM_IVRMST_IVRM_VID_DONE: VDD iVRM done indicator. Raises when the iVRM circuits are done processing a change request, triggered by a rising edge of IVRMCR[IVRM_VID_VALID], and stays set until the VALID is cleared.
1:63	RO	constant = 0b000000000000000000000000000000000000000000000000000000000000000

Register Name	PPM iVRM Data Value Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_IVRMDVR
Address	000000002E0F01B4 (SCOM)
Description	PPM iVRM data value register

Bits	SCOM	Field Mnemonic: Description
0:7	RW	PPM_IVRMDVR_IVRM_IVID: Writes to this field will drive the VID value representing the requested voltage to the QUAD iVRMs (4 Core VDD and Cache VDD) 0:7 = ivid(0:7). Encoded based on zero origin at 512 mV with 4 mV granularity. 0x00 = 512 mV. 0x01 = 516 mV. 0x7F = 1.532 mV. QUAD PPM usage: These bits are always sent to the cache iVRM and all core PPMs, where it is forwarded to each core chiplet iVRM unless it is locally overridden in its core PPM. Core PPM usage: If CIVRMLCR[IVRM_LOCAL_CONTROL] = 1, these values are driven to the core iVRM. Otherwise, the value driven comes from input pins from the QUAD PPM IVRMDVR.
8:10	RW	PPM_IVRMDVR_RESERVED_8_10: Implemented but not used.
11:15	RW	PPM_IVRMDVR_IVRM_PFET_STRENGTH_CORE: PFET strength value driven to this chiplet's iVRMs. This value written is dependent on the current input voltage, the requested output voltage (IVRM_IVID), and the ratio of the power needed at the requested voltage to the maximum power. See iVRM documentation for details. QUAD PPM usage: This value is sent to all core PPMs, where it is forwarded to each core chiplet iVRM unless it is locally overridden in its core PPM. Core PPM usage: If CIVRMLCR[IVRM_LOCAL_CONTROL] = 1, these values are driven to the core iVRM. Otherwise, the value driven comes from QUAD PPM IVRMDVR.
16:18	RW	PPM_IVRMDVR_RESERVED_16_18: Implemented but not used.
19:23	RW	PPM_IVRMDVR_IVRM_PFET_STRENGTH_CACHE: QUAD PPM usage: PFET strength value driven to the cache iVRMs. The written value is dependent on the current input voltage, the requested output voltage (IVRM_IVID), and the ratio of the power needed at the request voltage to the maximum power. See iVRM documentation for details. Core PPM usage: This field is unused.
24:63	RO	constant = 0b0000000000000000000000000000000000000000

Register Name	PPM iVRM Actual Value Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_IVRMAVR
Address	000000002E0F01B5 (SCOM)
Description	PPM iVRM actual value register

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	Reserved field.
8	ROX	Reserved field.
9:10	RO	constant = 0b00
11:15	ROX	Reserved field.
16:23	RO	constant = 0b00000000
24	ROX	Reserved field.
25	ROX	Reserved field.
26	ROX	Reserved field.
27	ROX	Reserved field.
28:63	RO	constant = 0b000000000000000000000000000000000000

Register Name	CPPM Core iVRM Local Control Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_CIVRMLCR
Address	000000002E0F01B7 (SCOM)
Description	CPPM Core iVRM local control register

Bits	SCOM	Field Mnemonic: Description
0	RW	CPPM_CIVRMLCR_IVRM_LOCAL_CONTROL: Controls the iVRM interface multiplexer to determine which value gets sent to the core iVRMs. 0 = Global (QUAD PPM) sourced controls from IVRMCR are selected to drive this core chiplet's iVRM. 1 = Local (Core PPM) sourced controls from IVRMCR are selected.
1:2	RW	CPPM_CIVRMLCR_RESERVED_1_2: Implemented but not used.
3	RW	CPPM_CIVRMLCR_IVRM_UREG_TEST_EN: Enables UREG test where UREGs will activate only if selected by UREG_TEST_ID. Used to ensure that each was manufactured correctly to supply the high power core voltage grid.
4:7	RW	CPPM_CIVRMLCR_IVRM_UREG_TEST_ID: Selects one of sixteen UREGs to test if UREG_TEST_EN = 1. The UREGs that do not match this field when UREG_TEST_EN = 1 will be turned off internally.
8:63	RO	constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	PPM VDM Control Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_COMMON_REGS.PPM_VDMCR
Address	000000002E0F01B8 (SCOM) 000000002E0F01B9 (SCOM1) 000000002E0F01BA (SCOM2)
Description	PPM VDM control register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_CLEAR	WO_OR	PPM_VDMCR_VDM_POWERON: Enables analog circuits in the VDM for this chiplet to burn power (0.6 mW). Once this bit is set, it takes 10 ms for VDM output indicators to be valid.
1	RW	WO_CLEAR	WO_OR	PPM_VDMCR_VDM_DISABLE: VDM disable for this chiplet. Like a logical fence, setting this bit forces VDM droop indication outputs to all 1.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
2:63	RO	RO	RO	constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	CPPM Inter-PPM Command Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_IPPMCMD
Address	000000002E0F01C0 (SCOM)
Description	CPPM inter-PPM command register

Bits	SCOM	Field Mnemonic: Description
0:7	RW	CPPM_IPPMCMD_QPPM_REG: The QUAD PPM register offset to be accessed. All QUAD PPM registers are read accessible. Only a subset may be written.
8	RW	CPPM_IPPMCMD_QPPM_RNW: 0 = Write. 1 = Read.
9	RW	CPPM_IPPMCMD_RESERVED_9: Implemented but unused.
10:63	RO	constant = 0b000000000000000000000000000000000000000000000000000000

Register Name	CPPM Inter-PPM Status Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_IPPMSTAT
Address	000000002E0F01C1 (SCOM)
Description	CPPM inter-PPM status register

Bits	SCOM	Field Mnemonic: Description
0	ROX	CPPM_IPPMSTAT_QPPM_ONGOING: QPPM transfer ongoing. 0 = A transfer is not ongoing. 1 = A transfer is ongoing. Upon writing this register, hardware sets this bit and initiates the transfer from the Core PPM to the QUAD PPM. Upon completion of the transfer, this bit is cleared. Firmware should check for the clear state of this bit to ensure that the transfer is complete.
1:2	ROX	CPPM_IPPMSTAT_QPPM_STATUS: QPPM status(0:1). 00 = Operation success. 01 = Write operation not performed due to CME QPPM accesses not being enabled. See QUAD CPMMR[CME_INTERPPM_ENABLE] and CPMMR[CME_INTERPPM_SELECT]. 10 = Unsupported register. 11 = Fatal QPPM FSM error (Reserved). Upon writing this register, hardware clears this bit and, upon transfer completion, samples the status from the QUAD PPM. Firmware should check for the clear state of this field to ensure that the transfer has completed successfully.
3:63	RO	constant = 0b0000000000000000000000000000000000000000000000000000000000000

Register Name	CPPM Inter-PPM Write Data Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_IPPMWDATA
Address	000000002E0F01C2 (SCOM)
Description	CPPM inter-PPM write data register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CPPM_IPPMWDATA_QPPM_WDATA: Data to be written to the register defined in the CPPM Inter-PPM Command Register when a write command is executed.

Register Name	CPPM Inter-PPM Read Data Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMC.PPM_CORE_REGS.CPPM_IPPMRDATA
Address	000000002E0F01C3 (SCOM)
Description	CPPM inter-PPM read data register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CPPM_IPPMRDATA_QPPM_RDATA: Data read from register defined in the CPPM Inter-PPM Command Register when a read command is executed.

Register Name	Protect Mode Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.PROTECT_MODE_REG
Address	000000002E0F03FE (SCOM)
Description	Enables read and write protection.

Bits	SCOM	Field Mnemonic: Description
0	RW	READ_PROTECT_ENABLE: Enable read protection.
1	RW	WRITE_PROTECT_ENABLE: Enable write protection.

Register Name	Atomic Lock Register
Mnemonic	TP.TPCHIP.NET.PCBSLEC14.PPMPCBSLV.ATOMIC_LOCK_REG
Address	000000002E0F03FF (SCOM)
Description	A bit mask for atomic locking on a ring-by-ring basis.

Bits	SCOM	Field Mnemonic: Description
0	RW	ATOMIC_LOCK_ENABLE: Enable atomic lock.
1:4	ROX	ATOMIC_ID: Atomic ID.
5:7	RO	constant = 0b000
8:15	ROX	ATOMIC_ACTIVITY: Atomic lock counter.