POWER8 Processor with NVIDIA NVLink Interconnect Datasheet

OpenPOWER

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IBM Systems
294 Route 100, Building SOM4
Somers, NY 10589-3216

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Revision Log

Each release of this document supersedes all previously released versions. The revision log lists all significant changes made to the document since its initial release. In the rest of the document, change bars in the margin indicate that the adjacent text was modified from the previous release of this document.

Revision Date	Description
11 December 2017	Version 1.7. • Revised the notes in *Table 3-4 PCIe Interface Signals* on page 21. • Removed a note from *Table 6-2 Frequencies and TDP* on page 65.
28 September 2017	Version 1.6. • Revised *Table 3-3 Supported I/O Configurations* on page 20. • Revised *Section 3.3.4 PCIe Bus* on page 20. • Revised the table caption in *Table 3-4 PCIe Interface Signals* on page 21. • Revised the *Glossary* on page 99.
10 May 2017	Version 1.5. • Updated URL hyperlinks to the IBM Portal for OpenPOWER throughout the document. • Revised *Section 1 Introduction* on page 11. • Revised *Section 1.1 Processor Feature Summary* on page 11. • Revised *Section 1.2 Supported Technologies* on page 12. • Revised *Section 1.3 Interfaces* on page 12. • Revised *Section 1.10 Marking Specification* on page 13. • Revised *Section 3.3.1 Specification Compliance* on page 19. • Updated *Table 7-2 ESD Stress Qualification* on page 75. • Updated the *Glossary* on page 99.
14 October 2016	Version 1.4. • Changed FSI0 Clock to FSI Slave Clock and FSI0 Data to FSI Slave Data in *Table 5-10 FSI Signals* on page 39. • Changed FSI0 Clock to FSI Slave Clock and FSI0 Data to FSI Slave Data in *Table 6-7 Default FSI Settings* on page 72.
12 April 2016	Version 1.3. • Updated a note in *Table 3-4 PCIe Interface Signals* on page 21.
10 March 2016	Version 1.2. • Changed dc to DC throughout. • Changed ac to AC throughout. • Added a note to *Table 3-4 PCIe Interface Signals* on page 21. • Reworded a sentence in *Section 4.2 Efficient Power Supply Oversubscription Capability* on page 25. • Added a note to signals TS_CT_P_PIN_TDIODE_A5, TS_CT_P_PIN_TDIODE_C5, TS_CT_P_PIN_TDIODE_A13, and TS_CT_P_PIN_TDIODE_C13 in *Table 5-14 Thermal Diodes and Monitor Signals* on page 42. • Added notes 1 and 2 to *Table 5-20 JTAG Signals* on page 61. • Updated the *Glossary* on page 99.

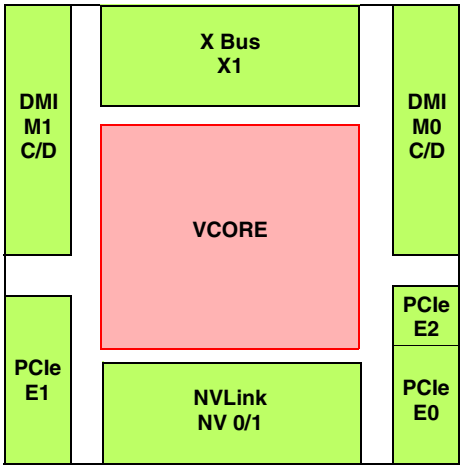
Revision Date	Description
4 January 2016	Version 1.1. • Revised *Section 1.4 Power Management Support* on page 12. • Updated the frequency range in *Table 2-1 POWER8 with NVLink SCM Technology* on page 15. • Added note 2 to *Table 3-4 PCIe Interface Signals* on page 21. • Reworded the first paragraph in *Section 4 Power Management* on page 25. • Revised the delta time range in *Table 4-1 System Power Sequencing* on page 28. • Updated *Section 5.1 Pin Naming Convention* on page 30. • Revised the TS_PIN_P_CT_STBY_RESET_B signal in *Table 5-7 Test Signals* on page 36. • Revised the PV_PIN_P_CT_SPARE2 signal in *Table 5-7 Test Signals* on page 36. • Added a note to the PV_PIN_P_CT_FSI_IN_ENA1 signal in *Table 5-8 Control Signals* on page 37. • Revised the notes in *Table 5-9 LPC Bus Signals* on page 38. • Revised the signal names for pins BD35, BC34, BB33, and BA32 in *Table 5-10 FSI Signals* on page 39. • Revised *Section 5.2.8 I^2C Signals* on page 41. • Revised a note in *Table 5-13 Time-of-Day and Bus Synchronization Signal* on page 42. • Revised *Section 5.2.10 Thermal Diode and Monitor Signals* on page 42. • Revised the description for the TS_CT_P_PIN_DTS2_MONI signal, the signal name for pin AY35, the pin assignments for PV_MSOP_M_CT_VREF_P/N, and updated the cross-references to table notes in *Table 5-14 Thermal Diodes and Monitor Signals* on page 42. • Updated the SDR memory values in *Table 6-1 POWER8 with NVLink Processor and POWER8 Memory Buffer Frequency Domains* on page 63. • Updated *Table 6-2 Frequencies and TDP* on page 65. • Changed “our systems” to “POWER systems” in *Section 6.3.1 Clock AC Specifications* on page 66. • Updated the *Glossary* on page 99.
16 October 2015	Version 1.0 (initial version).

1. Introduction

This datasheet describes the IBM® POWER8® processor with NVIDIA® NVLink™ Interconnect. The POWER8 with NVLink processor is a superscalar symmetric multiprocessor designed for use in high-performance computing (HPC) and data analytics systems. The NVLink interconnect enables ultra-fast communication between the central processing unit (CPU) and the graphics processing unit (GPU) and between GPUs. It uses a CMOS 22 nm SOI technology with 15 metal layers. Each POWER8 with NVLink processor can have up to 12 cores enabled on a single chip in a single-chip module (SCM) configuration. Each core has eight threads using simultaneous multithreading (SMT). The SMT is dynamically tunable, so that each core can have one, two, four, or eight threads.

Figure 1-1 illustrates the POWER8 with NVLink interconnect pinout diagram.

Figure 1-1. POWER8 with NVLink Interconnect Pinout Map



1.1 Processor Feature Summary

The POWER8 with NVLink processor consists of the following main components:

- Twelve POWER8 chiplets, which contain a POWER8 core, an L2 cache, and an L3 cache.
- One on-chip accelerator engine
  - On chip: compression, encryption, data move initiated by the hypervisor
  - In core: user invocation encryption (AES, SHA)
- Two memory controllers that support the POWER8 memory buffer chip
- Processor bus interconnect
- SMP interconnect that supports one coherent 8-byte X bus
- The interface controllers support the following interfaces:
  - Four differential memory buses (M0 C/D, M1 C/D)
  - One intra-node SMP bus (X1)
  - Configurable PCIe 3.0 buses: two ×16 lanes and one ×8 lane, or one ×16 lane and three ×8 lanes
  - Four NVLink version 1.0 links

- Power management
- Pervasive functions

1.2 Supported Technologies

The POWER8 with NVLink processor supports the following technologies:

- Power ISA Book I, II, and III version 2.07
- Linux on Power Architecture Platform Reference
- IEEE P754-2008 for binary and decimal floating-point compliant
- Big-endian, little-endian, strong-ordering support extension
- 50-bit real address, 68-bit virtual address

1.3 Interfaces

The primary service interface to the POWER8 with NVLink processor is the FRU service interface (FSI) that runs at 166 MHz. See *Section 3.1 Service Interfaces* on page 17 for more information.

1.4 Power Management Support

Key features of the POWER8 with NVLink processor in the SCM are:

- Hypervisor-directed power change requests using the Pstate mechanism
- Sensors
  - Digital thermal sensor (DTS2) ±5°C
  - Off-chip analog thermal diode ±1 - 2°C
  - Dedicated performance, microarchitecture, and event counters
- Accelerators
  - On-chip IBM PowerPC® 405 embedded processor core for real-time frequency and voltage modification
  - On-chiplet hardware assist (automated core chiplet management)
  - On-chip power management controls
    - Automated communications to the voltage regulation modules (VRMs)
    - Voltage and frequency sequencers for automated Pstate and idle state support
- Actuators
  - Per chiplet frequency control through the DPLL
  - Per-chiplet internal VRMs for independent voltage control
  - Architected idle states: nap, sleep, and winkle; each with increasing power savings capability (and latency)
  - SPR Power Management Control Registers (PMCR, PMICR, PMSR) for hypervisor support

- Memory and DIMM throttling for memory subsystem power and thermal management

1.5 Thermal Specification

Thermal junction temperature (T_J) is measured by digital thermal sensors located on the chip. There are four sensors per core, which are averaged. The specified T_J is the worst case of these averages or the hottest core average. The maximum T_J is not allowed to exceed 85°C. The average T_J, at which the reliability is calculated, is 70°C. Margin does not need to be applied when measuring against the worst-case specification because the chip is sorted using the same thermal sensors. The digital thermal sensor has an absolute accuracy of ±5% and can be read out in Celsius (°C).

1.6 Signals

Section 5 Signals on page 29 describes the POWER8 with NVLink processor signals.

1.7 Electrical

Section 6 Electrical Characteristics on page 63 discusses the DC and AC electrical characteristics of the POWER8 with NVLink processor in the SCM.

1.8 Package Support

Section 7 Mechanical Specifications on page 75 describes the POWER8 with NVLink SCM features and provides a pin list.

1.9 Processor Version Register

The POWER8 with NVLink processor has the following Processor Version Register (PVR) values for the respective design revision levels.

Table 1-1. POWER8 with NVLink Processor Version Register

POWER8 with NVLink Design Revision Level	POWER8 with NVLink PVR
DD 1.0	x‘004C0100’

1.10 Marking Specification

See the IBM Portal for OpenPOWER for the current mechanical drawings and recommended module layout.

1.11 Conventions

This section explains the number, bit field, instruction, and signal conventions that are used in this document.

1.11.1 Representation of Numbers

Numbers are generally shown in decimal format, unless designated as follows:

- Hexadecimal values are preceded by an “x” and enclosed in single quotation marks.
  For example: x‘0A00’.
- Binary values in sentences are shown in single quotation marks.
  For example: ‘1010’.

Note: A bit value that is immaterial, which is called a “don't care” bit, is represented by an “x.”

1.11.2 Bit Significance

The bit on the left represents the most-significant bit of a field. The bit on the right represents the least-significant bit of a field. For example, in CTL[0:31], 0 is the most-significant bit.

1.11.3 Other Conventions

- Instruction mnemonics are shown in lowercase, bold text. For example: **tlbivax**.
- I/O signal names are shown in uppercase.
- The notation [*] indicates all bits in a field or register.

An underscore indicates that a definition is displayed when you hoover your cursor over the underscored term.

1.12 Related Documents and Models

The documents available in the IBM Portal for OpenPOWER, an online IBM technical library, are helpful in understanding the IBM POWER8 with NVLink processor. Additional technical resources are available on the OpenPOWER Foundation web site. The following non-IBM documents are also useful:

- *For the Development of an Electrostatic Discharge Control Program for – Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices) (ANSI/ESD S20.20-2007)*
- *For the Protection of Electrostatic Discharge Susceptible Items - Packaging Materials for ESD Sensitive Items (ANSI/ESD S541-2008)*
- *I^2C Bus Specification (Version 2.1)*
- *PCI Local Bus Specification (Revision 3.0)*

2. Technologies

This section provides a high-level overview of the technologies implemented in the POWER8 with NVLink processor.

2.1 General Parameters

Table 2-1 lists general parameters for the POWER8 with NVLink processor.

Table 2-1. POWER8 with NVLink SCM Technology

Feature	Description
Technology	22 nm silicon-on-insulator (SOI), 15 metal layers
Die Size	659 mm^2
Chip Package (SCM)	See *Table 7-1 SCM Features* on page 75 for details.
Signal I/O	2296
Frequency Range (nominal)	2.860 - 3.259 GHz
Power	190 W

3. Interfaces

3.1 Service Interfaces

The POWER8 with NVLink processor has multiple service interfaces that are used for initialization during boot. The service interfaces are also accessible by using the debug box. The primary entry point to the POWER8 processor service interface is the FRU service interface (FSI), a serial interface that runs at 166 MHz.

The POWER8 with NVLink SCM provides the following FSIs:

- Two FSI slaves for connecting in the debug box and multichip SMP.
- Four FSI masters for communicating with the POWER8 memory buffer chip.
- One FSI master for communicating with other POWER8 with NVLink chips in the system. One POWER8 with NVLink chip is defined as the master and is responsible for initializing the other POWER8 with NVLink chips over these FSI interfaces.

The POWER8 with NVLink SCM provides the following additional service interfaces:

- One serial peripheral interconnect (SPI) master for controlling the core and cache voltage regulators.
- One SPI master for on-chip controller (OCC) management.
- One LPC bus for connecting to the BMC.
- One I^2C slave for BMC-to-OCC communication.
- Two SEEPROM interfaces to load the on-chip SEEPROMs. This path can be disabled for secure boot reasons.
- Two I^2C masters for controlling LEDs, PCIe cards, and so on. The I^2C masters can be manipulated from the OCC or hostboot code.
- Two high-speed SPI master buses for off-chip VRM control and voltage slewing.
- One time-of-day clock.

3.2 Supported Processor Interfaces

This section gives an overview of the physical layer and on-chip initialization provided by the POWER8 with NVLink processor.

The POWER8 with NVLink SCM supports the following types of drivers and receivers:

- X Bus: Generation 4 Elastic Interface (EI-4) at 4.8 Gb/s for fabric interconnect
- Memory I/O: High-speed differential at 9.6 Gbps for the memory interface

Table 3-1 lists the requirements relative to the operational mode definitions.

Table 3-1. Interface Operational Mode Definitions

Mode Name	Definition
Initialization	The act of aligning and locking the data eye and bit lanes plus additional deltas relative to re-alignment and re-locking.
Functional	Passing workload data and maintaining signal integrity post-initialization.
Power Saving	All related capabilities for minimizing unused and idle lane power consumption.
Test	Capabilities related to hardware manufacturability.
Diagnostic	Bringup lab characterization of interface performance capabilities.

3.2.1 Bus Highlights

Table 3-2 highlights the differences between the X bus and memory I/O bus. See the *POWER8 Processor with NVDIA NVLink Interconnect User's Manual* for additional information.

Table 3-2. X Bus and Memory Bus Highlights

	X Bus	Memory Bus
Frequency	4.8 Gb/s	9.6 Gb/s
Initialization Mode Requirement	4.8 - 3.2 Gb/s	9.6 - 8.0 Gb/s
Spare Lane Detect	Data failover One signal total per bus per port	Data failover Two signals total per bus per port
Functional Mode Specification	4.8 - 3.2 Gb/s	9.6 - 8.0 Gb/s
Power-Saving Mode Requirement	No power-saving mode support	No power-saving mode support
Test Mode Requirement	4.8 - 3.2 Gb/s[1]	9.6 - 8.0 Gb/s[1]
Driver Features	• 2:1 data serialization at 4.8 Gb/s • Programmable drive strengths • Precompensation • dc test mode	• 4:1 data serialization at 9.6 Gb/s • Programmable drive strengths • Impedance calibration • Post cursor FFE levels and amplitude margining • Feed forward equalization • Precompensation • dc test mode
Receiver Features	• Input descrambler • 4:1 de-serializer • Phase interpolator • dc offset calibration • DFE-1 (1-tap decision feedback equalizer)	• Input descrambler • 4:1 de-serializer • Phase interpolator • dc offset calibration • DFE-1 (1-tap decision feedback equalizer)

1. Subject to PLL range limitations and a test frequency of 200 MHz.

3.3 PCI Express Controller

The PCI Express controller (PEC) bridges between the internal processor bus and the high-speed serial (HSS) links that drive the PCI Express I/O. The PEC acts as a processor bus master on behalf of the PCI Express port, converting inbound memory read and write packets into processor bus DMA traffic. The PEC also acts as a processor bus slave, transferring processor load and store commands to the PCI Express devices attached to the port.

3.3.1 Specification Compliance

The PEC is compliant with the following IBM and industry standards:

- Linux on Power Architecture Platform Reference
- *PCI Express Base Specification Revision 3.0*, v0.71

3.3.2 PEC Feature Summary

- PCI Express Generation 3 root complex (RC)
  - Backwards compatible with generation 1 and generation 2
  - 2.5, 5.0, and 8 GT/s signalling rate
- Forty PCIe I/O lanes configurable to four independent root complexes
- Each root complex has 256 partitionable endpoints (PE) for LPAR support
- TCE-based address translation for DMA requests
  - 50-bit address support
  - Translation validation table based on PCI routing ID
- 2048 MSI interrupts per RC
- Eight LSI interrupts per RC
- IBM enhanced error handling (EEH) support
- Processor bus cache-inhibited space segmented by PEC
  - PCI 32-bit memory space segmented into 256 domains by the memory domain table
  - PCI 64-bit memory space segmented by 16 M64 BARs with 16 segments each
- Support for ECRC
- Support for lane wrapping
- Support for PCIe atomic operations and TLP hints

3.3.3 Supported Configuration

The 40 lanes of HSS I/O can be configured to support four independent PCIe buses. *Table 3-3* describes the maximum lane allocation. In addition to supporting PCI operations, the HSS I/O can be allocated for use by the processor bus SMP interface.

Table 3-3. Supported I/O Configurations

PECx	PHB0	PHB1	PHB2	PHB3
PEC0	×16[1]			
PEC1		×16[1]		
		×8[1]	×8	
PEC2				×8

1. CAPI-capable slot.

3.3.4 PCIe Bus

The POWER8 with NVLink SCM has a total of 40 PCIe Gen3 lanes. The PCIe Gen3 bandwidth is 1 GBps per lane. There are three PCIe controllers per processor. The number of PHBs per PEC is variable. PEC0 has a single PHB that is nonbifurcatible, ×16 lanes, and CAPI capable. PEC1 contains two PHBs. PEC1 can be run as a single ×16 interface or two ×8 lanes. PEC1 is CAPI capable either as a ×16 interface or the first ×8 lane. PEC2 has a single ×8 PHB. It is not CAPI capable.

Note: The lanes can be reversed for easier routing if required. The polarity can also be reversed on a lane-by-lane basis.

Table 3-4 lists the PCI interface signals.

Table 3-4. PCIe Interface Signals (Sheet 1 of 2)

Chip	Interface	Mode	Pins		Note
P0	E0	×16	Data Lanes	PE_PIN_P_E0_CK0_DAT_[00:07]_[P/N] PE_PIN_P_E0_CK1_DAT_[00:07]_[P/N]	1
			Clocks	PE_CT_P_PIN_E0_SLOT_CLK0_[P/N]	2
			Reset	PE_CT_P_PIN_E0_PERST0_B PE_CT_P_PIN_E0_PERST1_B	3
			Present	PE_PIN_P_CT_E0_PRSNT0_B PE_PIN_P_CT_E0_PRSNT1_B	4
P0	E1	×16	Data Lanes	PE_PIN_P_E1_CK0_DAT_[00:07]_[P/N] PE_PIN_P_E1_CK1_DAT_[00:07]_[P/N]	
			Clocks	PE_CT_P_PIN_E1_SLOT_CLK0_[P/N] PE_CT_P_PIN_E1_SLOT_CLK1_[P/N]	
			Reset	$\overline{\text{PE\_CT\_P\_PIN\_E1\_PERST0\_B}}$ $\overline{\text{PE\_CT\_P\_PIN\_E1\_PERST1\_B}}$	3
			Present	$\overline{\text{PE\_PIN\_P\_CT\_E1\_PRSNT0\_B}}$ $\overline{\text{PE\_PIN\_P\_CT\_E1\_PRSNT1\_B}}$	4
P0	E1	×8	Data Lanes	PE_PIN_P_E1_CK0_DAT_[00:07]_[P/N]	
			Clocks	PE_CT_P_PIN_E1_SLOT_CLK0_[P/N] PE_CT_P_PIN_E1_SLOT_CLK1_[P/N]	
			Reset	$\overline{\text{PE\_CT\_P\_PIN\_E1\_PERST0\_B}}$ $\overline{\text{PE\_CT\_P\_PIN\_E1\_PERST1\_B}}$	3
			Present	$\overline{\text{PE\_PIN\_P\_CT\_E1\_PRSNT0\_B}}$ $\overline{\text{PE\_PIN\_P\_CT\_E1\_PRSNT1\_B}}$	4
P0	E1	×8	Data Lanes	PE_PIN_P_E1_CK1_DAT_[00:07]_[P/N]	5
			Clocks	PE_CT_P_PIN_E1_SLOT_CLK0_[P/N] PE_CT_P_PIN_E1_SLOT_CLK1_[P/N]	
			Reset	$\overline{\text{PE\_CT\_P\_PIN\_E1\_PERST0\_B}}$ $\overline{\text{PE\_CT\_P\_PIN\_E1\_PERST1\_B}}$	3
			Present	$\overline{\text{PE\_PIN\_P\_CT\_E1\_PRSNT0\_B}}$ $\overline{\text{PE\_PIN\_P\_CT\_E1\_PRSNT1\_B}}$	4

1. If using only half of this bus and wiring to a ×8 slot that supports a ×4 adapter, the following rules must be followed:
   - For E0_CK0_DAT[00:07], the bus cannot be reversed.
   - For E0_CK1_DAT[00:07], the bus must be reversed.
2. This bus is ×16 mode only (non-bifurcatible). Thus, there is only one slot clock.
3. IBM uses a 4.7 KΩ pull-up. Follow PCIe slot/device endpoint specifications. If the bus is not used, this pin can be a no connect. See *Table 5-17* on page 54 for additional information.
4. The PRSNT signal has an internal 1 KΩ pull-up to 1.1 V. An additional onboard pull-up of the specified value range is only required if the signal is part of a level-translation circuit. See *Table 5-17* on page 54 for additional information.
5. When bifurcating PCIe bus E1, refer to hardware errata #11 in the *POWER8 Processor SCM and Memory Buffer Hardware Errata Notice* for implementation details on the bus E1_CK1_DAT[00:07] signals.

Table 3-4. PCIe Interface Signals (Sheet 2 of 2)

Chip	Interface	Mode	Pins		Note
P0	E2	×8	Data Lanes	PE_PIN_P_E2_CK0_DAT_[00:07]_[P/N]	
			Clocks	PE_CT_P_PIN_E2_SLOT_CLK0_[P/N]	
			Reset	$\overline{\text{PE\_CT\_P\_PIN\_E2\_PERST0\_B}}$	3
			Present	$\overline{\text{PE\_PIN\_P\_CT\_E2\_PRSNT0\_B}}$	4

1. If using only half of this bus and wiring to a ×8 slot that supports a ×4 adapter, the following rules must be followed:
   - For E0_CK0_DAT[00:07], the bus cannot be reversed.
   - For E0_CK1_DAT[00:07], the bus must be reversed.
2. This bus is ×16 mode only (non-bifurcatible). Thus, there is only one slot clock.
3. IBM uses a 4.7 KΩ pull-up. Follow PCIe slot/device endpoint specifications. If the bus is not used, this pin can be a no connect. See *Table 5-17* on page 54 for additional information.
4. The PRSNT signal has an internal 1 KΩ pull-up to 1.1 V. An additional onboard pull-up of the specified value range is only required if the signal is part of a level-translation circuit. See *Table 5-17* on page 54 for additional information.
5. When bifurcating PCIe bus E1, refer to hardware errata #11 in the *POWER8 Processor SCM and Memory Buffer Hardware Errata Notice* for implementation details on the bus E1_CK1_DAT[00:07] signals.

3.4 SMP Bus

The POWER8 with NVLink SCM supports one coherent SMP bus (X1) that can be used to connect two POWER8 with NVLink chips. The X bus carries coherency traffic, as well as data. The single-ended X bus runs at 4.8 Gb/s. It can be configured as 8 bytes or 4 bytes in width.

3.5 DMI Bus

The POWER8 with NVLink SCM brings out a total of four DMI interfaces at 9.6 Gbps. The total pin bandwidth of one DMI interface is 28.8 GBps.

See the *POWER8 Memory Buffer Datasheet for DDR3 Applications* and the *POWER8 Memory Buffer Datasheet for DDR4 Application User's Guide* for bandwidth requirements.

3.6 NVLink Controller

The NVLink controller is a high-speed connection that is used with a PCIe connection on the POWER8 with NVLink processor to create a high-bandwidth interconnect between the processor and 1 - 4 attached GPUs. The PCIe connection is used as the control path to initiate and report the status of large data transfers to and from the POWER8 with NVLink processor and the GPU memory. The data transfers themselves are subsequently initiated by the GPU as DMA read and write requests across the NVLink interconnect. The NVLink controller acts as the processor bus master on behalf of the GPU to complete the DMA requests within the processor memory subsystem.

The POWER8 with NVLink processor implements the NVLink 1 subset of the full NVLink coherent interconnect (NCI). The NVLink 1 subset does not include the coherency feature and some other additional features of the full NCI implementation.

An NVLink connection is composed of a minimum of one link between devices. Each link is an 8-lane, differential, dual-simplex bidirectional link. Multiple links can be ganged together to form higher bandwidth connections between the POWER8 with NVLink processor and the GPU. Links consist of a sublink[1] in each direction. One end of this sublink can also be referred to as a brick.

The NVLink controller contains facilities for address translation and validation. These facilities are substantially based on the IBM I/O Design Architecture v2 used by POWER8 with NVLink PCIe interfaces.

3.6.1 Specification Compliance

The NVLink controller supports the following architectural features:

- NVIDIA Coherent Interconnect (NCI) Specification (NVLink 1), Revision 1.11
- I/O Design Architecture v2

3.6.2 Features

- NVLink bricks
  - 4 - 8 bit transmit
  - 4 - 8 bit receive
- Supports 1 - 4 GPUs
  - Each GPU NVLink connection supports 1 - 4 NVLink links
- NVLink peak bandwidth per link:
  - Peak read bandwidth per link: 19.2 GB/s
  - Peak write bandwidth per link: 19.2 GB/s
- Total NVLink bandwidth:
  - Total peak read bandwidth: 76.8 GB/s
  - Total peak write bandwidth: 76.8 GB/s
- NVLink effective bandwidth per link:
  - Read bandwidth per link: 18 GB/s
  - Write bandwidth per link: 16 GB/s
- Total NVLink bandwidth:
  - Total effective read bandwidth: 72 GB/s
  - Total effective write bandwidth: 64 GB/s
- Transfer sizes supported
  - Minimum transfer size: 16 bytes
  - One byte minimum for masked writes
  - Maximum transfer size: 256 bytes
- TCE-based address translation for GPU DMA requests
  - 50-bit address support
  - Translation validation table based on a partitionable endpoint for each GPU
  - 1K entry, 4-way associative, TCE cache

1. A sublink is defined as the 8-lane connection between a transmitter and a receiver.

3.6.3 NVLink Bus

The POWER8 with NVLink SCM provides 32 lanes of NVLink 1.0 ports across four bricks that can be used to connect up to four GPUs. The four ×8 bricks run at 19.2 Gb/s and support up to 140 GB/s of bi-directional bandwidth.

4. Power Management

The POWER8 with NVLink processor chip uses several traditional power-saving techniques to reduce peak power and thermal design-point (TDP) power. For example, latches and arrays are clock gated when they are not needed. Also, individual cores, or full core chiplets, are dynamically power gated when the cores are not being used. That is, the power to the cores is turned off.

The POWER8 with NVLink processor uses adaptive power management techniques to reduce average power. These techniques, collectively known as IBM EnergyScale™, proactively take advantage of variations in workload, environmental condition, and overall system utilization. Coupled with a policy direction from the customer and feedback from the hypervisor or operating system that is running on the machine, this is used to determine modes of operation and the best power and performance trade-off to implement during runtime to meet customer goals and achieve the best possible performance.

4.1 Power Gating and On-Chip, Per-Core Voltage Regulation

Offering competitive chip and system designs requires the capability to dynamically adjust power consumption and performance levels to meet the needs of changing workloads. The POWER8 with NVLink processor offers industry-leading features to achieve this goal.

During idle periods, each chiplet can individually power gate or “turn off” the supply to either the core or to both the core and the associated L3 cache region to reduce chiplet idle power. The gating header in the POWER8 with NVLink processor is driven to an elevated voltage when off by using an on-chip charge pump. This technique increases the leakage power reduction, bringing the total DC power reduction achieved by power gating to 50 - 100x. As a result, the power-gated power consumption is less than 1% of the chiplet idle power.

Power gating can also be used to virtually eliminate the parasitic leakage power of deconfigured cores in a partial-good product offering by leaving the headers for unconfigured cores in an always gated state.

The idle power saved by power gating can be used to boost the frequency of the remaining operational cores. Using this technique, the nominal frequency of operating four cores can exceed the 12-core operating frequency by almost 30%.

4.2 Efficient Power Supply Oversubscription Capability

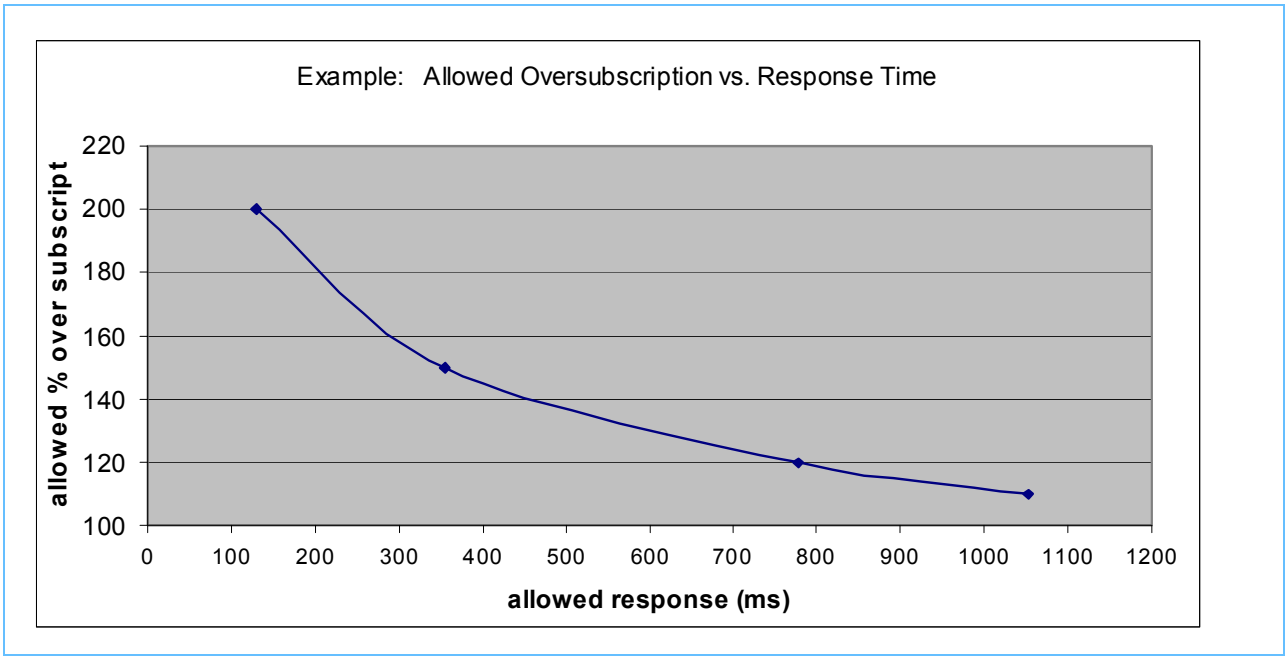
System bulk power supplies redundantly deliver worst-case power, which is significantly more power than is typically consumed. Typical workloads, parts, and environments are much less power hungry than the worst case. Also, power delivery failure is very uncommon.

This excess power capacity can be converted into performance by using oversubscription. By oversubscribing the power supply, the processor is allowed to run at voltages and frequencies that exceed the power limit of the system under a worst-case workload and with failure of one of the redundant supplies.

Robust system operation must be maintained in spite of oversubscription. To do this, the processor must be able to throttle back power quickly enough to avoid an overcurrent condition in the remaining bulk power supply in case of a failure in the redundant supply or a sudden power spike.

POWER8 with NVLink systems increase oversubscription capabilities to 1.5x resulting in performance gains. The fundamental limit to power supply oversubscription is the circuit breakers in the utility or UPS when the redundant power fails. The system must be able to throttle back to consuming power less than the non-oversubscribed limit before the EXP(Current) × Time limit of the breaker is violated. *Figure 4-1* shows a representative curve of allowed oversubscription versus response time.

Figure 4-1. Oversubscriptions versus Response Time



To improve response time, a dedicated C4 pin directly signals a power-supply error to the on-chip controller (OCC).

The OCC engine can then use its internal power-actuation capabilities to rapidly reduce power. The POWER8 with NVLink processor offers the following forms of power reduction:

- The OCC can force a halt in the fetch or issue of instructions to significantly reduce AC power within approximately 10 cycles.
- The OCC can use the DPLL to reduce frequency at a rate of approximately 25 MHz/µs. The AC power reduces linearly with the frequency reduction.

Based on these capabilities, the POWER8 with NVLink processor can throttle its power to a small fraction of the nominal operating power in less than 5 ms of receiving the system signal indicating a power supply failure.

The other key to enabling significant oversubscription is rapid detection of a power supply failure.

4.3 Chip Hardware Power-Management Features

4.3.1 Chiplet Voltage Control

The POWER8 with NVLink processor supports several voltage regulator module (VRM) control mechanisms for multiple system configurations. The core chiplets are on a separate voltage plane than the other Nest components of the chip. The chip-level power-management control (PMC) macro and the OCC are, in combination, programmable to support these configurations.

Core chiplets all share the same voltage plane and must run with the “highest common denominator,” which means that the core demanding the highest voltage sets the value of the voltage rail. The OCC is responsible for establishing the best frequency, and therefore voltage bounds based on the workload running, the power/performance efficiency policy selected by the customer, and the system budgets established by the thermal management component.

4.3.2 Chip-Level Voltage Control Sequencing

The external VRMs (eVRMs) sourcing the logic (V_{DD}) and array (V_{CS}) rails are controlled by voltage control interfaces from the POWER8 with NVLink chip. These interfaces use serial peripheral interconnect (SPI) signaling to a VRM chipset that converts the addressed VID command to industry-standard Intel VRM-11 interface components or others, as implemented by the VRMs.

4.3.3 SPIVID VRM Control Sequencing

The V_{DD} target voltage and the relevant V_{CS} offset is sent in one command to the VRM set. The target might be the full voltage swing request (V_{MAX} to V_{MIN} or vice-versa) or any subset. With the V_{DD} target and associated V_{CS} offset value, the VRMs, through sampling of load lines, manage the offset of the two rails during the slew.

4.4 System Power Sequencing

The power sequencing design must check the PGOOD status before continuing to the next step. The sequencer must allow for some amount of minimum time after PGOOD issues before continuing as specified in *Table 4-1*.

Table 4-1. System Power Sequencing

Voltage Domain	Delta Time (ms)	Comments
Typically, system rails associated with service processors, I/O, and storage are enabled before the processor/memory power is enabled. This guide does not cover these specifics.		
AV_{DD}	0.1 - 20	The POWER8 memory buffer and the POWER8 with NVLink processor can be combined.
V_{IO}	0.1 - 20	The POWER8 memory buffer and the POWER8 with NVLink processor can be combined.
POWER8 V_{DD}	0.1 - 20	
POWER8 V_{CS}	0.1 - 20	
Additional processors can be added here in the same sequence or paralleled, so that all V_{DD} come on at the same time followed by all V_{CS}.		
V_{PCIe}	0.1 - 20	
POWER8 memory buffer V_{DD}	0.1 - 20	
POWER8 memory buffer V_{CS}	0.1 - 20	
Additional POWER8 memory buffer chips can be added here in the same sequence or paralleled, so that all V_{DD} come on at the same time followed by all V_{CS}.		
Marks the beginning of the secondary sequence, memory initialization pause.[1]		
V_{PP}	0.1 - 20	DDR4 only. Must always be greater than V_{MEM}.
$V_{MEM/DDR}$	0.1 - 20	DDR3 or DDR4. Must be less than 200 ms after V_{PP}. V_{TERM} tracks this domain/2 and comes on at the same time.
Additional V_{PP}/V_{MEM} domains can be added in the same sequence or can be paralleled, so that they all come on together.		

1. The secondary sequence pause is required for the self-boot engine (SBE) to complete memory initialization tasks. At this step, the processor indicates to the service processor or power sequencer what the memory voltage must be programmed to and then indicates when to turn on the memory power rails. The memory voltage calculation is performed on the processor with information from the DIMM VPD and memory configuration.

5. Signals

This section describes the POWER8 with NVLink signal groups. They are arranged in functional groups according to their interface. *Table 5-1* lists the signal type notation.

Table 5-1. Signal Type Notation

Direction	Signal Type
Rec	Receiver (input).
RecDiff	Receiver differential pair signal polarity (P or N).
Drv	Driver (output).
DrvDiff	Driver differential pair signal polarity (P or N).
AnlgIn	Analog input.
AnlgOut	Analog output.
BiDi	Bi-directional input/output signal.
SH	Share test for manufacturing test only. No functional use.

Table 5-2 lists the buffer types.

Table 5-2. Signal Buffer Type Notation

Signal	Description
CMOS	CMOS buffers.
OD	Open drain.
Analog	Analog.
EI4	Elastic interface 4.
EDI	Elastic differential I/O.
PCIe	PCI Express interface signals. These signals are compatible with PCI Express 3.0.
REF	Voltage reference signal.
PLL/CLK	PLL clock.
IOO	NVLink interface signal.

5.1 Pin Naming Convention

The general pin-naming pattern is:

prefix_source_connectionType_sink_clockGroup_sigType_bitNumber_diffBit

Prefix - the type of bus or signal type being connected. The following abbreviations are used:

DR	DDR memory bus
MM	Memory bus
NX	X bus
PE	PCIe
NV	NVLink
PV	Pervasive
TS	Test

Source and Sink - the specific component and bus being connected. The following abbreviations are used:

CT	Chip test or pervasive
M0	Memory channel 0 bus
E0	PCIe 0 bus
X1	X1 bus
V0	NVLink 0 bus
PIN	Module pin

Connection Type

P	Point-to-point
B	Bidirectional
M	Multipoint

Clock Group

CK0	Clock group 0
CKA	Clock group A

Signal type (sigType)

CLK	Clock signal
DAT	Data signal

Bit Number - bit strand number, if needed; uses padding zeros.

Differential Bit (diffBit) - differential pair signal polarity (P or N), if needed.

5.2 Signals by Group

5.2.1 Voltage and Ground Signals

Table 5-3 lists the voltage and ground signals.

Table 5-3. Voltage and Ground Signals (Sheet 1 of 2)

Signal	Description	Pin
AVDD_1P50	Analog VDD	AC12, AC13
DVDD_1P50	Digital VDD	AB12, AB13
VCS_0P97	VCS	N19, N22, N27, N30, R19, R22, R27, R30, V19, V22, V27, V30, Y19, Y22, Y27, Y30, AB19, AB22, AB27, AB30, AG19, AG22, AG27, AG30, AJ19, AJ22, AJ27, AJ30, AL19, AL22, AL27, AL30, AP19, AP22, AP27, AP30, AT19, AT22, AT27, AT30
VDD_0P89	VDD	M15, M17, M19, M21, M23, M27, M29, M31, M33, N14, N16, N26, N28, N32, N34, P15, P17, P19, P21, P23, P25, P27, P29, P31, P33, R16, R18, R20, R24, R26, R28, R32, R34, T15, T17, T19, T21, T23, T27, T29, T31, T33, U14, U16, U18, U20, U22, U26, U28, U30, U32, U34, V15, V17, V21, V23, V25, V29, V31, V33, W14, W16, W18, W20, W22, W24, W26, W28, W30, W32, W34, Y15, Y17, Y21, Y23, Y29, Y31, Y33, AA14, AA16, AA18, AA20, AA22, AA24, AA26, AA28, AA30, AA32, AA34, AB15, AB17, AB21, AB23, AB29, AB31, AB33, AC14, AC16, AC18, AC20, AC22, AC26, AC28, AC30, AC32, AC34, AD15, AD19, AD21, AD23, AD27, AD31, AE14, AE18, AE22, AE26, AE28, AE30, AE32, AE34, AF15, AF17, AF19, AF21, AF23, AF25, AF27, AF29, AF31, AF33, AG14, AG16, AG18, AG20, AG24, AG26, AG28, AG32, AG34, AH15, AH17, AH19, AH21, AH23, AH25, AH27, AH29, AH31, AH33, AJ14, AJ16, AJ18, AJ20, AJ26, AJ28, AJ32, AJ34, AK15, AK17, AK19, AK21, AK23, AK25, AK27, AK29, AK31, AK33, AL14, AL16, AL20, AL24, AL26, AL28, AL34, AM15, AM17, AM19, AM21, AM23, AM27, AM29, AM31, AM33, AN14, AN16, AN18, AN20, AN22, AN26, AN28, AN30, AN32, AN34, AP15, AP17, AP21, AP23, AP29, AP31, AP33, AR14, AR16, AR18, AR20, AR22, AR24, AR26, AR28, AR30, AR32, AR34, AT15, AT17, AT21, AT23, AT25, AT29, AT31, AT33, AU14, AU16, AU18, AU20, AU22, AU26, AU28, AU30, AU32, AU34
VIO_1P10	VIO	K13, K15, K17, K19, K21, K23, K25, K27, K29, K31, K33, L14, L16, L18, L20, L22, L24, L26, L28, L30, L32, L34, M13, M25, M35, P24, P35, T13, T25, T35, V13, V24, W35, Y13, Y25, AA35, AB24, AC35, AD13, AD14, AD18, AD22, AD25, AD29, AD33, AD36, AE16, AE20, AE24, AE27, AE31, AE35, AF13, AF36, AG25, AG35, AH13, AH36, AJ24, AJ35, AK13, AK36, AL25, AL35, AM13, AM36, AN24, AN35, AR25, AR35, AT13, AU24, AU35, AV15, AV17, AV19, AV21, AV23, AV25, AV27, AV29, AW14, AW16, AW18, AW20, AW22, AW24, AW28, AW30, AW35
VPCI_1P20	VPCI	K35, L35, L36, M36, N35, P36, R35, T36, U36, V35, AN36, AP35, AR36, AT35, AU36, AV35

Table 5-3. Voltage and Ground Signals (Sheet 2 of 2)

Signal	Description	Pin
VSB_1P20	VSB	AV31, AV33
VSB_3P30	VSB	AF09, AG09
GND	Ground	A04, A07, A12, A13, A18, A23, A24, A27, A30, A33, A38, A39, A44, A46, A48, B03, B08, B13, B14, B19, B24, B25, B26, B29, B32, B37, B38, B43, B44, C04, C09, C14, C15, C20, C25, C28, C31, C36, C37, C42, C43, C45, D05, D10, D15, D16, D21, D24, D25, D27, D30, D35, D38, D43, D46, E01, E02, E03, E06, E11, E16, E17, E22, E25, E26, E29, E34, E35, E40, E41, E43, E47, F02, F04, F07, F12, F17, F18, F23, F26, F27, F30, F33, F35, F40, F42, F43, F48, G03, G04, G05, G06, G08, G13, G18, G19, G24, G25, G26, G29, G32, G34, G39, G40, G43, G44, H01, H04, H05, H07, H09, H14, H19, H20, H25, H28, H31, H33, H35, H40, H44, H45, J02, J05, J08, J10, J11, J12, J13, J14, J15, J18, J21, J24, J26, J31, J34, J36, J39, J40, J45, J46, K03, K06, K09, K10, K14, K16, K18, K20, K22, K24, K26, K28, K30, K32, K34, K36, K40, K41, K46, K47, L01, L04, L07, L10, L11, L15, L17, L19, L21, L23, L25, L27, L29, L31, L33, L38, L39, L40, L41, L42, L47, L48, M02, M05, M08, M11, M12, M14, M16, M18, M22, M26, M28, M30, M32, M34, M37, M39, M40, M42, M43, M48, N03, N06, N09, N11, N13, N15, N17, N21, N25, N29, N31, N33, N36, N39, N40, N43, N44, P01, P04, P07, P10, P11, P14, P16, P18, P20, P22, P26, P28, P30, P32, P34, P40, P41, P44, P45, R02, R05, R08, R11, R12, R15, R17, R21, R23, R25, R29, R31, R33, R36, R40, R42, R45, R46, T03, T06, T09, T11, T12, T16, T18, T20, T22, T26, T28, T30, T32, T34, T38, T40, T43, T46, T47, U01, U04, U07, U10, U11, U13, U15, U17, U19, U21, U25, U27, U29, U31, U33, U35, U37, U38, U39, U40, U41, U44, U47, U48, V01, V02, V05, V08, V11, V12, V14, V16, V18, V20, V26, V28, V32, V34, V36, V39, V41, V42, V45, V48, W02, W03, W06, W09, W11, W13, W15, W17, W19, W21, W23, W25, W27, W29, W31, W33, W36, W37, W38, W39, W42, W43, W46, Y01, Y03, Y04, Y07, Y10, Y11, Y14, Y16, Y18, Y20, Y24, Y26, Y28, Y32, Y34, Y35, Y38, Y40, Y43, Y44, Y47, AA02, AA04, AA05, AA08, AA11, AA12, AA13, AA15, AA17, AA19, AA21, AA23, AA25, AA27, AA29, AA31, AA33, AA36, AA37, AA38, AA41, AA44, AA45, AA48, AB01, AB03, AB05, AB06, AB09, AB11, AB14, AB16, AB18, AB20, AB26, AB28, AB32, AB34, AB35, AB37, AB38, AB39, AB42, AB45, AB46, AC02, AC04, AC06, AC07, AC10, AC11, AC15, AC17, AC19, AC21, AC23, AC27, AC29, AC31, AC33, AC38, AC40, AC43, AC46, AC47, AD01, AD03, AD05, AD07, AD08, AD10, AD11, AD12, AD16, AD20, AD24, AD26, AD28, AD30, AD32, AD34, AD35, AD38, AD41, AD44, AD47, AD48, AE02, AE04, AE06, AE08, AE09, AE15, AE19, AE21, AE23, AE25, AE29, AE33, AE36, AE37, AE38, AE39, AE42, AE45, AE48, AF01, AF03, AF05, AF07, AF08, AF11, AF12, AF14, AF16, AF18, AF20, AF22, AF24, AF26, AF28, AF30, AF32, AF34, AF35, AF38, AF39, AF40, AF43, AF46, AG02, AG04, AG06, AG08, AG11, AG15, AG17, AG21, AG23, AG29, AG31, AG33, AG36, AG38, AG40, AG41, AG44, AG47, AH01, AH03, AH05, AH07, AH09, AH11, AH14, AH16, AH18, AH20, AH22, AH24, AH26, AH28, AH30, AH32, AH34, AH35, AH37, AH38, AH41, AH42, AH45, AH48, AJ02, AJ04, AJ06, AJ08, AJ10, AJ12, AJ13, AJ15, AJ17, AJ21, AJ23, AJ25, AJ29, AJ31, AJ33, AJ36, AJ38, AJ39, AJ42, AJ43, AJ46, AK01, AK03, AK05, AK07, AK09, AK11, AK14, AK16, AK18, AK20, AK22, AK24, AK26, AK28, AK30, AK32, AK34, AK35, AK38, AK40, AK43, AK44, AK47, AL02, AL04, AL06, AL08, AL10, AL11, AL15, AL21, AL23, AL29, AL33, AL36, AL37, AL41, AL44, AL45, AL48, AM01, AM03, AM05, AM07, AM09, AM11, AM12, AM14, AM16, AM18, AM20, AM22, AM24, AM26, AM28, AM30, AM32, AM34, AM35, AM39, AM42, AM45, AM46, AN02, AN04, AN06, AN08, AN10, AN11, AN13, AN15, AN17, AN19, AN21, AN23, AN27, AN29, AN31, AN33, AN38, AN39, AN40, AN43, AN45, AN47, AP01, AP03, AP05, AP07, AP09, AP11, AP14, AP16, AP18, AP20, AP24, AP26, AP28, AP32, AP34, AP36, AP37, AP40, AP41, AP44, AP45, AP48, AR02, AR04, AR06, AR08, AR10, AR12, AR15, AR17, AR19, AR21, AR23, AR27, AR29, AR31, AR33, AR39, AR41, AR42, AR45, AR46, AT01, AT03, AT05, AT07, AT09, AT11, AT14, AT16, AT18, AT20, AT24, AT26, AT28, AT32, AT34, AT36, AT38, AT39, AT42, AT43, AT46, AT47, AU02, AU04, AU06, AU08, AU09, AU10, AU11, AU15, AU17, AU19, AU21, AU23, AU25, AU27, AU29, AU31, AU33, AU38, AU43, AU44, AU47, AU48, AV01, AV03, AV05, AV07, AV08, AV11, AV12, AV14, AV16, AV18, AV20, AV22, AV24, AV26, AV28, AV30, AV32, AV34, AV36, AV38, AV39, AV44, AV45, AV48, AW02, AW04, AW06, AW07, AW12, AW13, AW15, AW17, AW19, AW21, AW23, AW25, AW27, AW29, AW37, AW38, AW40, AW44, AW45, AW46, AY01, AY03, AY05, AY07, AY08, AY13, AY14, AY17, AY19, AY22, AY23, AY25, AY28, AY31, AY34, AY36, AY38, AY39, AY40, AY41, AY46, AY47, BA02, BA04, BA06, BA07, BA12, BA17, BA18, BA23, BA26, BA29, BA30, BA33, BA36, BA41, BA42, BA44, BA47, BA48, BB01, BB03, BB05, BB06, BB11, BB16, BB17, BB22, BB23, BB24, BB27, BB30, BB31, BB34, BB36, BB37, BB42, BB43, BB48, BC02, BC04, BC05, BC10, BC15, BC16, BC21, BC24, BC25, BC28, BC31, BC32, BC35, BC37, BC38, BC43, BC44, BD01, BD03, BD04, BD09, BD14, BD15, BD20, BD23, BD24, BD27, BD32, BD33, BD36, BD38, BD39, BD44, BD45, BE02, BE03, BE08, BE13, BE14, BE19, BE22, BE24, BE25, BE28, BE33, BE34, BE37, BE39, BE40, BE45, BE46, BF01, BF02, BF07, BF12, BF13, BF18, BF23, BF26, BF29, BF34, BF35, BF40, BF41, BF46, BF47, BG01, BG06, BG11, BG12, BG17, BG22, BG24, BG27, BG30, BG35, BG36, BG40, BG41, BG42, BG47, BG48, BH05, BH10, BH11, BH16, BH21, BH22, BH25, BH28, BH31, BH36, BH39, BH42, BH43, BH48

5.2.2 PLL and Reference Clock Signals

Table 5-4 lists the PLL signals.

Table 5-4. PLL Signals

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Notes
TS_CT_P_PIN_PXFM_PLL_ANATST	AE11	PLL analog test	PLL/Clock	Analog	AnlgOut	No	N/A	1
TS_CT_P_PIN_PXFM_PLL_HFC_P/N	AE12, AE13	PLL high-frequency characterization	PLL/Clock	CMOS	Drv	No	N/A	1
TS_CT_P_PIN_M0_PLL_ANATST	J25	Memory 0 PLL analog test	PLL/Clock	Analog	AnlgOut	No	N/A	1
TS_CT_P_PIN_M1_PLL_ANATST	AY18	Memory 1 PLL analog test	PLL/Clock	Analog	AnlgOut	No	N/A	1
TS_CT_P_PIN_PE0_PLL_ANATST	M38	PCIe PLL analog test	PLL/Clock	Analog	AnlgOut	No	N/A	1
TS_CT_P_PIN_PE1_PLL_ANATST	AY37	PCIe PLL analog test	PLL/Clock	Analog	AnlgOut	No	N/A	1
TS_CT_P_PIN_PE2_PLL_ANATST	N38	PCIe PLL analog test	PLL/Clock	Analog	AnlgOut	No	N/A	1
TS_CT_P_PIN_NV0_PLL_ANATST	P39	NVLink 0 PLL analog test	PLL/Clock	Analog	AnlgOut	No	N/A	1
TS_CT_P_PIN_NV0_PLL_HFC_P/N	T39, R39	PLL high-frequency characterization	PLL/Clock	CMOS	Drv	No	N/A	1
TS_CT_P_PIN_NV1_PLL_ANATST	AP39	NVLink 1 PLL analog test	PLL/Clock	Analog	AnlgOut	No	N/A	1
TS_CT_P_PIN_NV1_PLL_HFC_P/N	AR37, AT37	PLL high-frequency characterization	PLL/Clock	CMOS	Drv	No	N/A	1

1. No connect. For test points use dogbone via.

Table 5-5 lists the reference clock signals.

Table 5-5. Reference Clocks

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
PV_PIN_P_CT_OSC0_C1_REFCLK_P/N	W12, Y12	System Reference Clock [1]	PLL/Clock	CMOS	RecDiff				

1. No termination on chip. The clocking solution must include termination.

5.2.3 Test Signals

Table 5-6 lists the minikerf test signals.

Table 5-6. I/O Minikerf Test Signals

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Notes
TS_CT_P_PIN_M0_C_MKERF_P/N	J28, J27	I/O PHY test point	Test	Analog	AnlgOut	No		1
TS_CT_P_PIN_M0_T_PLLHFC_MKERF_P/N	J22, J23	I/O PHY test point	Test	Analog	AnlgOut	No		1
TS_CT_P_PIN_M1_T_PLLHFC_MKERF_P/N	AY16, AY15	I/O PHY test point	Test	Analog	AnlgOut	No		1
TS_CT_P_PIN_NV0_MKERF_P/N	P38, R38	I/O PHY test point	Test	Analog	AnlgOut	No		1
TS_CT_P_PIN_NV1_MKERF_P/N	AL38, AM38	I/O PHY test point	Test	Analog	AnlgOut	No		1

1. No connect.

Table 5-7 lists additional test signals.

Table 5-7. Test Signals

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
TS_PIN_P_CT_TEST_LSSD_TE	BD37	LSSD test mode[1]	Pervasive	CMOS	Rec	Pull-down 50 Ω ±5%	GND	N/A	N/A
TS_PIN_P_CT_TST_FORCE_PWR_ON	AR11	Test force power-on[1]	Pervasive	CMOS	Rec	Pull-down 50 Ω ±5%	GND	N/A	N/A
TS_CT_P_PIN_VCAL	AC24	Used to calibrate the iVRM output transistor strength during wafer test.	Pervasive	Analog	AnlgOut		N/A	N/A	N/A
TS_PIN_P_CT_STBY_RESET_B	BC36	Standby reset for FSI. Active during the power-on process. Requires pull-up.[3]	Pervasive	CMOS	Rec	Pull-up 10 kΩ ±5%	1.2 V AUX	N/A	N/A
TS_CT_P_PIN_PROBE0_P/N	AY29, AY30	Probe Out 0 differential high/differential low	Pervasive	CMOS	DrvDiff				
TS_CT_P_PIN_PROBE1_P/N	J16, J17	Probe Out 1 differential high/differential low	Pervasive	CMOS	DrvDiff				
TS_CT_P_PIN_PROBE2	AY27	Probe Out 2	Pervasive	CMOS	Drv				
TS_CT_P_PIN_PROBE3	AY24	Probe Out 3	Pervasive	CMOS	Drv				
TS_CT_P_PIN_PROBE4	AY26	Probe Out 4	Pervasive	CMOS	Drv				
TS_PIN_P_CT_EFUSE_FSOURCE	AP25	eFuse V_{DD}	Pervasive	Analog	Power	Pull-down 50 Ω ±5%	GND		
PV_PIN_P_CT_SPARE2	D26	Spare 2[2]	Pervasive	CMOS	Rec	Pull-up 50 Ω ±5%	1.1 V		

1. Not used at board or system level.
2. Signal can be left floating.
3. A 1 - 10 nF capacitor is recommended for noise dampering.

5.2.4 Control Signals

Table 5-8 lists the control signals.

Table 5-8. Control Signals

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
PV_CT_P_PIN_ATTENTION_B	BB35	Attention[1]	Pervasive	CMOS	Drv	Pull-up 4.7 KΩ	3.3 V AUX	N/A	Yes, up to 3.65 V
PV_PIN_P_CT_CHIP_ID0	BF39	Chip ID[2]	Pervasive	CMOS	Rec	50 Ω ±5%[3]	1.2 V AUX/GND		No
PV_PIN_P_CT_CHIP_ID1	BG38	Chip ID[2]	Pervasive	CMOS	Rec	50 Ω ±5%[3]	1.2 V AUX/GND		No
PV_PIN_P_CT_FSI_IN_ENA1	BG39	Enable incoming FSI clock[4,5]	Pervasive	CMOS	Rec	Pull-up 1.2 KΩ	1.2 V AUX		No
PV_PIN_P_CT_VIO_PGOOD	AW26	V_{IO} power good[6]	Pervasive	CMOS	Rec	Pull-up[7] 1.2 KΩ	1.2 V AUX	N/A	No
PV_CT_P_PIN_TPM_RESET	AJ11	TPM reset[1, 8]	Pervasive	OD	BiDi	Pull-down 10 KΩ	GND	No	No
PV_PIN_P_CT_TPM_INTERRUPT	AK10	TPM interrupt[9]	Pervasive	OD	Rec	Pull-up 1 KΩ ±5%	1.1 V	No	No

1. See the IBM reference design in the IBM Portal for OpenPOWER for implementation details.
2. Use to configure MFSI slave network.
3. See IBM 2-socket reference design for implementation details.
4. Active signal has an internal 10 KΩ pull-down. Requires a 1.2 KΩ pull-up to override.
5. This signal determines the source of the FSI clock, either internal or external. The signal must be asserted (driven high) by the BMC when the BMC is driving the FSI bus (for example. during the boot sequence to the POWER8 processor) and when the FSP2 debug box is being used.>>
6. Critical for boot/operation; use extra capacitance to GND for noise.
7. No pull-up is required if there is always an active driver on this signal. It should never be left floating.
8. System-dependent level shifting required.
9. The actual pull-up value might vary depending on the system implementation.

5.2.5 LPC Bus Signals

Table 5-9 lists the LPC bus signals.

Table 5-9. LPC Bus Signals

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
PV_CT_B_PIN_LPC_DATA_[00:03]	AY33, AW32, AY32, AW31	LPC Data. P/N of level shifter.[1]	Pervasive	CMOS	BiDi			No	No
PV_CT_P_PIN_LPC_FRAME_B	AW33	LPC Frame[1]	Pervasive	CMOS	Drv			No	No
PV_PIN_P_CT_LPC_RESET_B	AW34	LPC Reset[1]	Pervasive	CMOS	BIDI			No	No
PV_PIN_P_CT_LPC_CLK	AW36	LPC Clock[2]	Pervasive	CMOS	Rec			No	No
PV_CT_B_PIN_LPC_SERIRQ	BF36	LPC Serial Interrupt	Pervasive	CMOS	BIDI			No	No

1. Use level shifter FXLA0104. See the IBM reference design in the IBM Portal for OpenPOWER for implementation details.
2. See the IBM reference design in the IBM Portal for OpenPOWER for implementation details. V_{MAX} = 1.2 V for this pin.

5.2.6 FSI Signals

Table 5-10 lists the FSI signals.

Table 5-10. FSI Signals

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
PV_PIN_P_CT_FSP0_FSI_CLK	BH40	FSI Slave Clock	FSI	CMOS	Rec	No			No
PV_PIN_B_CT_FSP0_FSI_DATA	BH41	FSI Slave Data	FSI	CMOS	BiDi	No			No
SH_PIN_P_CT_FSP1_FSI_CLK	BG23	FSI1 Clock[1]	FSI	CMOS	Rec	50 Ω ±5% pull-down	GND		No
SH_PIN_P_CT_FSP1_FSI_DATA	BE23	FSI1 Data[1]	FSI	CMOS	BiDi	No			No
MM_CT_P_PIN_MB_FSI2_CLK	BD34	FSI Master 2 Clock	FSI	CMOS	Drv				No
MM_CT_B_PIN_MB_FSI2_DATA	BD35	FSI Master 2 Data	FSI	CMOS	BiDi	750 Ω pull-up[2]	1.2 V AUX		No
MM_CT_P_PIN_MB_FSI3_CLK	BC33	FSI Master 3 Clock	FSI	CMOS	Drv				No
MM_CT_B_PIN_MB_FSI3_DATA	BC34	FSI Master 3 Data	FSI	CMOS	BiDi	750 Ω pull-up[2]	1.2 V AUX		No
MM_CT_P_PIN_MB_FSI6_CLK	BB32	FSI Master 6 Clock	FSI	CMOS	Drv				No
MM_CT_B_PIN_MB_FSI6_DATA	BB33	FSI Master 6 Data	FSI	CMOS	BiDi	750 Ω pull-up[2]	1.2 V AUX		No
MM_CT_P_PIN_MB_FSI7_CLK	BA31	FSI Master 7 Clock	FSI	CMOS	Drv				No
MM_CT_B_PIN_MB_FSI7_DATA	BA32	FSI Master 7 Data	FSI	CMOS	BiDi	750 Ω pull-up[2]	1.2 V AUX		No
PV_CT_P_PIN_FSI1_CLK	BE35	FSI Master CP Clock[3]	FSI	CMOS	Drv	No			No
PV_CT_B_PIN_FSI1_DATA	BE36	FSI Master CP Clock[3]	FSI	CMOS	BiDi	No			No
PV_PIN_P_CT_FSI_SMD	BF38	FSI secure mode disable[3]	Pervasive	CMOS	Rec	50 Ω ±5% pull-up	1.2 V AUX		No

1. No connect.
2. The pull-up is on the POWER8 memory buffer side of the net. If the POWER8 memory buffer is on a DIMM card, no additional pull-ups are required on the processor planar.
3. See the IBM reference design in the IBM Portal for OpenPOWER for implementation details.

5.2.7 SPI Signals

Table 5-11 lists the SPI signals. See the IBM reference design examples in the IBM Portal for OpenPOWER and the *POWER8 with NVIDIA NVLink Systems Power Design and Validation Guide* for implementation details.

Table 5-11. SPI Signals

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
PV_CT_P_PIN_SPIVID0_MOSI	F34	SPI VIDs (to VRM0)	SPI	CMOS	Drv	No			No
PV_PIN_P_CT_SPIVID0_MISO	J30	SPI VIDs (to VRM0)	SPI	CMOS	Rec	No			No
PV_CT_P_PIN_SPIVID0_SCLK	G33	SPI VIDs (to VRM0)	SPI	CMOS	Drv	No			No
PV_CT_P_PIN_SPIVID0_CS	J29	SPI VIDs (to VRM0)	SPI	CMOS	Drv	No			No
PV_CT_P_PIN_SPIADC_MOSI	J32	SPISS MOSI	SPI	CMOS	Drv	No			No
PV_PIN_P_CT_SPIADC_MISO	J35	SPISS MISO	SPI	CMOS	Rec	No			No
PV_CT_P_PIN_SPIADC_SCLK	H34	SPISS SCLK	SPI	CMOS	Drv	No			No
PV_CT_P_PIN_SPIADC_CS0	H32	SPISS CS0	SPI	CMOS	Drv	No			No
PV_CT_P_PIN_SPIADC_CS1	J33	SPISS CS1[1]	SPI	CMOS	Drv	No			No

1. No connect.

5.2.8 I²C Signals

Table 5-12 lists the I²C signals. See the IBM reference design examples in the IBM Portal for OpenPOWER for implementation details.

Table 5-12. I²C Signals

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
PV_PIN_B_CT_I2CSL_SCL	BG37	I²C Slave Clock[1]	I²C	OD	BiDi		3.3 V AUX	Yes	Yes
PV_PIN_B_CT_I2CSL_SDA	BF37	I²C Slave Data[1]	I²C	OD	BiDi		3.3 V AUX	Yes	Yes
PV_CT_M_PIN_SEEPROM0_CLK	AG10	SEEPROM Clock[2]	I²C	OD	Drv	Pull-up 1.5 KΩ	3.3 V AUX	Yes	Yes
PV_CT_M_PIN_SEEPROM0_DATA	AH10	SEEPROM Data[2]	I²C	OD	BiDi	Pull-up 1.5 KΩ	3.3 V AUX	Yes	Yes
PV_CT_M_PIN_SEEPROM1_CLK	AF10	SEEPROM Clock[2]	I²C	OD	Drv	Pull-up 1.5 KΩ	3.3 V AUX	Yes	Yes
PV_CT_M_PIN_SEEPROM1_DATA	AE10	SEEPROM Data[2]	I²C	OD	BiDi	Pull-up 1.5 KΩ	3.3 V AUX	Yes	Yes
PV_CT_B_PIN_LP_I2C_SCL_B	BH38	I²C Master Data Lightpath	I²C	OD	BiDi	See note 3	3.3 V AUX	Yes	Yes
PV_CT_B_PIN_LP_I2C_SDA_B	BH37	I²C Master Clock Lightpath	I²C	OD	BiDi	See note 3	3.3 V AUX	Yes	Yes
PV_CT_B_PIN_PCI_I2C_SCL_B	AR38	I²C Master Data PCIe E1	I²C	OD	BiDi	See note 3	3.3 V AUX	Yes	Yes
PV_CT_B_PIN_PCI_I2C_SDA_B	AP38	I²C Master Data PCIe E1	I²C	OD	BiDi	See note 3	3.3 V AUX	Yes	Yes

1. Alternate path into the chip FSI; connect to the BMC. See the IBM reference design examples in the IBM Portal for OpenPOWER for implementation details.
2. Module VPD.
3. If the bus is unused, pull-down to GND through a 50 Ω resistor. If used, the total value of parallel resistance on each net must be greater than 1.2 KΩ including the tolerance.

5.2.9 Time-of-Day Signal

Table 5-13 lists the time-of-day (TOD) signal.

Table 5-13. Time-of-Day and Bus Synchronization Signal

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
PV_PIN_P_CT_OSC0_TODREFCLK	U12	TOD Reference Clock[1]	CLK	CMOS	Rec	No	No	N/A	No

1. See the IBM reference design in the IBM Portal for OpenPOWER implementation details. Signal pin V_{MAX} = 1.2 V.

5.2.10 Thermal Diode and Monitor Signals

Table 5-14 lists the thermal diode and monitor signals. See the IBM reference design examples in the IBM Portal for OpenPOWER for implementation details.

Table 5-14. Thermal Diodes and Monitor Signals (Sheet 1 of 3)

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
TS_CT_P_PIN_TDIODE_A5	AL18	Core Thermal Diode Anode[1]	Thermal	Analog	AnlgOut	No			
TS_CT_P_PIN_TDIODE_C5	AL17	Core Thermal Diode Cathode[1]	Thermal	Analog	AnlgOut	No			
TS_CT_P_PIN_TDIODE_A13	AL31	Core Thermal Diode Anode[1]	Thermal	Analog	AnlgOut	No			
TS_CT_P_PIN_TDIODE_C13	AL32	Core Thermal Diode Cathode[1]	Thermal	Analog	AnlgOut	No			
TS_CT_P_PIN_DTS2_MONI	N18	Digital Thermal Sensor Monitor[2]	Thermal	Analog	AnlgOut	No	N/A	N/A	No

1. IBM recommends that this signal be no connect (N/C) for OpenPOWER products. Accurate processor temperature readings are available from the OCC via the processor I^2C bus.
2. No connect.
3. Voltage sense signals are used only for characterization and debug.

Table 5-14. Thermal Diodes and Monitor Signals (Sheet 2 of 3)

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
TS_CT_P_PIN_AMX0_VSENSE	D36	West Analog Muxed Sense[3]	Vsense	Analog	AnlgOut	No	N/A	N/A	No
TS_CT_P_PIN_AMX0_GSENSE	D37	West Analog Muxed Ground Sense[3]	Vsense	Analog	AnlgOut	No	N/A	N/A	No
TS_CT_P_PIN_AMX1_VSENSE	AN25	West Analog Muxed Sense[3]	Vsense	Analog	AnlgOut	No	N/A	N/A	No
TS_CT_P_PIN_AMX1_GSENSE	AM25	West Analog Muxed Ground Sense[3]	Vsense	Analog	AnlgOut	No	N/A	N/A	No
TS_CT_P_PIN_GDDCORE0_GSENSE	T14	Chiplet Core Logic Ground Sense[3]	Vsense	Analog	AnlgOut				
TS_CT_P_PIN_VDDCORE0_VSENSE	R14	Chiplet Core Logic Sense[3]	Vsense	Analog	AnlgOut				
TS_CT_P_PIN_GDSCORE0_GSENSE	N20	Chiplet Core SRAM Ground Sense[3]	Vsense	Analog	AnlgOut				
TS_CT_P_PIN_VCSCORE0_VSENSE	M20	Chiplet Core SRAM Sense[3]	Vsense	Analog	AnlgOut				
TS_CT_P_PIN_GDECO0_GSENSE	M24	Chiplet ECO Logic Ground Sense[3]	Vsense	Analog	AnlgOut				
TS_CT_P_PIN_VDDECO0_VSENSE	N23	Chiplet ECO Logic Sense[3]	Vsense	Analog	AnlgOut				
TS_CT_P_PIN_VCSECO0_VSENSE	N24	Chiplet ECO SRAM Sense[3]	Vsense	Analog	AnlgOut				
TS_CT_P_PIN_VDDEX0_VSENSE	U24	EX VDD Logic Voltage Sense[3]	Vsense	Analog	AnlgOut				
TS_CT_P_PIN_EX0_GSENSE	T24	EX VCS Ground Sense[3]	Vsense	Analog	AnlgOut				
TS_CT_P_PIN_VCSEX0_VSENSE	U23	EX VCS Logic Voltage Sense[3]	Vsense	Analog	AnlgOut				
TS_CT_P_PIN_VIO_VSENSE	BA34	VIO Logic Voltage Sense[3]	Vsense	Analog	AnlgOut				

1. IBM recommends that this signal be no connect (N/C) for OpenPOWER products. Accurate processor temperature readings are available from the OCC via the processor I^2C bus.
2. No connect.
3. Voltage sense signals are used only for characterization and debug.

Table 5-14. Thermal Diodes and Monitor Signals (Sheet 3 of 3)

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
TS_CT_P_PIN_VIO_VPCI_GSENSE	BA35	VIO VPCI Ground Sense[3]	Vsense	Analog	AnlgOut				
TS_CT_P_PIN_VPCI1_VSENSE	AY35	VPCI Voltage Sense[3]	Vsense	Analog	AnlgOut				
TS_CT_P_PIN_PFAMX_VSENSE	AB25	PFET Analog Muxed Sense[3]	Vsense	Analog	AnlgOut				
TS_CT_P_PIN_PFAMX_GSENSE	AC25	PFET Analog Muxed Ground Sense[3]	Vsense	Analog	AnlgOut				
PV_MSOP_M_CT_VREF_P/N	AD17, AE17	Internal chip reference pins[2]	Pervasive	Analog	AnlgOut	No	N/A	No	N/A
VCS_CHIP_VSENSE	Y27	VCS Voltage Sense for the Voltage Regulators[3]	Vsense	Analog	AnlgOut	No-popped 100 Ω pull-up	V_{CS}		
VCS_CHIP_GSENSE	W27	VCS Voltage Sense for the Voltage Regulators[3]	Vsense	Analog	AnlgOut	No-popped 100 Ω pull-down	GND		
VDD_CHIP_VSENSE	AF23	VDD Voltage Sense for the Voltage Regulators[3]	Vsense	Analog	AnlgOut	No-popped 100 Ω pull-up	V_{DD}		
VDD_CHIP_GSENSE	AF24	VDD Voltage Sense for the Voltage Regulators[3]	Vsense	Analog	AnlgOut	No-popped 100 Ω pull-down	GND		

1. IBM recommends that this signal be no connect (N/C) for OpenPOWER products. Accurate processor temperature readings are available from the OCC via the processor I^2C bus.
2. No connect.
3. Voltage sense signals are used only for characterization and debug.

5.2.11 DMI Signals

Table 5-15 lists the DMI signals.

Table 5-15. DMI Signals (Sheet 1 of 6)

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
PV_PIN_P_CT_M0_TERMREF_P/N	J19, J20	Memory Termination Reference[1]	DMI	Analog	AnlgIn	No			
MM_M0_P_PIN_CKC_CLK_P/N	E12, E13	Memory Channel Downstream Forwarded Clock	Data	EDI	DrvDiff				
MM_M0_P_PIN_CKC_DAT_[00:16]_P	G16, H17, H15, F15, G14, E14, F13, D14, C13, B12, C11, A11, B10, A09, D12, B07, A06	Memory Channel Downstream	Data	EDI	DrvDiff				
MM_M0_P_PIN_CKC_DAT_[00:16]_N	G17, H18, H16, F16, G15, E15, F14, D13, C12, B11, C10, A10, B09, A08, D11, B06, A05,	Memory Channel Downstream	Data	EDI	DrvDiff				
MM_PIN_P_M0_CKC_CLK_P/N	C32, C33	Memory Channel Upstream Forwarded Clock	Data	EDI	RecDiff				
MM_PIN_P_M0_CKC_DAT_[00:23]_P	C26, H26, B27, A25, E27, D28, G27, A28, C29, B30, F28, A31, B33, A34, D31, B35, C35, A37, D34, E31, E33, F32, G31, H30	Memory Channel Upstream	Data	EDI	RecDiff				

1. Do not connect to any voltages or signals. Connect the P/N signals with a 169 Ω, 1% 0402 resistor.

Table 5-15. DMI Signals (Sheet 2 of 6)

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
MM_PIN_P_M0_CKC_DAT_[00:23]_N	C27, H27, B28, A26, E28, D29, G28, A29, C30, B31, F29, A32, B34, A35, D32, B36, C34, A36, D33, E30, E32, F31, G30, H29	Memory Channel Upstream	Data	EDI	RecDiff				
MM_M0_P_PIN_CKD_CLK_P/N	D06, D07	Memory Channel Downstream Forwarded Clock	Data	EDI	DrvDiff				
MM_M0_P_PIN_CKD_DAT_[00:16]_P	H12, G11, H10, F10, G10, E09, F08, E07, F05, E05, D02, D04, C03, D09, C06, B05, C08	Memory Channel Downstream	Data	EDI	DrvDiff				
MM_M0_P_PIN_CKD_DAT_[00:16]_N	H13, G12, H11, F11, G09, E10, F09, E08, F06, E04, D01, D03, C02, D08, C05, B04, C07	Memory Channel Downstream	Data	EDI	DrvDiff				
MM_PIN_P_M0_CKD_CLK_P/N	B17, B18	Memory Channel Upstream Forwarded Clock	Data	EDI	RecDiff				
MM_PIN_P_M0_CKD_DAT_[00:23]_P	H21, H23, G20, G23, F19, E18, D17, A14, C16, B15, C18, A16, D19, A19, E20, B20, C22, A22, B23, F22, C24, D23, E24, F25	Memory Channel Upstream	Data	EDI	RecDiff				

1. Do not connect to any voltages or signals. Connect the P/N signals with a 169 Ω, 1% 0402 resistor.

Table 5-15. DMI Signals (Sheet 3 of 6)

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
MM_PIN_P_M0_CKD_DAT_[00:23]_N	H22, H24, G21, G22, F20, E19, D18, A15, C17, B16, C19, A17, D20, A20, E21, B21, C21, A21, B22, F21, C23, D22, E23, F24	Memory Channel Upstream	Data	EDI	RecDiff				
PV_PIN_P_CT_M1_TERMREF_P/N	AY20, AY21	Memory Termination Reference[1]	DMI	Analog	AnlgIn	No			
MM_M1_P_PIN_CKC_CLK_P/N	BD11, BD10	Memory Channel Downstream Forwarded Clock	Data	EDI	DrvDiff				
MM_M1_P_PIN_CKC_DAT_[00:16]_P	BA15, BB14, BA13, BC13, BB12, BD12, BC11, BE11, BF11, BG10, BF08, BH09, BG07, BH07, BE10, BG05, BH04	Memory Channel Downstream	Data	EDI	DrvDiff				
MM_M1_P_PIN_CKC_DAT_[00:16]_N	BA16, BB15, BA14, BC14, BB13, BD13, BC12, BE12, BF10, BG09, BF09, BH08, BG08, BH06, BE09, BG04, BH03	Memory Channel Downstream	Data	EDI	DrvDiff				
MM_PIN_P_M1_CKC_CLK_P/N	BF30, BF31	Memory Channel Upstream Forwarded Clock	Data	EDI	RecDiff				

1. Do not connect to any voltages or signals. Connect the P/N signals with a 169 Ω, 1% 0402 resistor.

Table 5-15. DMI Signals (Sheet 4 of 6)

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
MM_PIN_P_M1_CKC_DAT_[00:23]_P	BF24, BA24, BG25, BH23, BD25, BE26, BB25, BH26, BF27, BG28, BC26, BH29, BG31, BH32, BE29, BG33, BF33, BH35, BE32, BD29, BD31, BC30, BB29, BA28	Memory Channel Upstream	Data	EDI	RecDiff				
MM_PIN_P_M1_CKC_DAT_[00:23]_N	BF25, BA25, BG26, BH24, BD26, BE27, BB26, BH27, BF28, BG29, BC27, BH30, BG32, BH33, BE30, BG34, BF32, BH34, BE31, BD28, BD30, BC29, BB28, BA27	Memory Channel Upstream	Data	EDI	RecDiff				
MM_M1_P_PIN_CKD_CLK_P/N	BC08, BC09	Memory Channel Downstream Forwarded Clock	Data	EDI	DrvDiff				
MM_M1_P_PIN_CKD_DAT_[00:16]_P	AY11, BA11, AW10, AV10, AY10, AW08, BB09, BA08, BB07, BC07, BD06, BD08, BE04, BE07, BF04, BG03, BF06	Memory Channel Downstream	Data	EDI	DrvDiff				

1. Do not connect to any voltages or signals. Connect the P/N signals with a 169 Ω, 1% 0402 resistor.

Table 5-15. DMI Signals (Sheet 5 of 6)

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
MM_M1_P_PIN_CKD_DAT_[00:16]_N	AY12, BA10, AW11, AV09, AY09, AW09, BB10, BA09, BB08, BC06, BD05, BD07, BE05, BE06, BF03, BG02, BF05	Memory Channel Downstream	Data	EDI	DrvDiff				
MM_PIN_P_M1_CKD_CLK_P/N	BG15, BG16	Memory Channel Upstream Forwarded Clock	Data	EDI	RecDiff				
MM_PIN_P_M1_CKD_DAT_[00:23]_P	BA19, BA21, BB18, BB20, BC17, BD17, BE15, BH12, BF14, BG13, BF16, BH14, BE17, BH17, BD18, BG18, BF20, BH20, BG21, BC20, BF22, BE21, BD22, BC23	Memory Channel Upstream	Data	EDI	RecDiff				

1. Do not connect to any voltages or signals. Connect the P/N signals with a 169 Ω, 1% 0402 resistor.

Table 5-15. DMI Signals (Sheet 6 of 6)

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
MM_PIN_P_M1_CKD_DAT_[00:23]_N	BA20, BA22, BB19, BB21, BC18, BD16, BE16, BH13, BF15, BG14, BF17, BH15, BE18, BH18, BD19, BG19, BF19, BH19, BG20, BC19, BF21, BE20, BD21, BC22	Memory Channel Upstream	Data	EDI	RecDiff				
MM_CT_P_PIN_MB_NEST_REFCLK2_P MM_CT_P_PIN_MB_NEST_REFCLK2_N MM_CT_P_PIN_MB_NEST_REFCLK3_P MM_CT_P_PIN_MB_NEST_REFCLK3_N MM_CT_P_PIN_MB_NEST_REFCLK6_P MM_CT_P_PIN_MB_NEST_REFCLK6_N MM_CT_P_PIN_MB_NEST_REFCLK7_P MM_CT_P_PIN_MB_NEST_REFCLK7_N	P13 R13 N12 P12 AP13 AR13 AN12 AP12	POWER8 Memory Buffer Nest Clock	CLK	CMOS	Drv				
MM_CT_P_PIN_MB_MEM_REFCLK2_P MM_CT_P_PIN_MB_MEM_REFCLK2_N MM_CT_P_PIN_MB_MEM_REFCLK3_P MM_CT_P_PIN_MB_MEM_REFCLK3_N MM_CT_P_PIN_MB_MEM_REFCLK6_P MM_CT_P_PIN_MB_MEM_REFCLK6_N MM_CT_P_PIN_MB_MEM_REFCLK7_P MM_CT_P_PIN_MB_MEM_REFCLK7_N	K12 K11 L13 L12 AU13 AV13 AU12 AT12	POWER8 Memory Buffer Memory Clock	CLK	CMOS	Drv				

1. Do not connect to any voltages or signals. Connect the P/N signals with a 169 Ω, 1% 0402 resistor.

5.2.12 X Bus Signals

Table 5-16 lists the X bus signals.

Table 5-16. X Bus Signals (Sheet 1 of 3)

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
NX_PIN_P_X1_CK0_CLK_P/N	M01, N01	Clock 0 Input	Data	EDI	RecDiff				
NX_PIN_P_X1_CK0_DAT_[0:19]	AD09, AC09, AC08, AB08, T01, R01, U02, T02, V03, U03, P02, N02, W04, V04, Y05, W05, AA06, Y06, AB07, AA07	20-Bit Pack Data Input [00:19]	Data	EDI	Rec				
NX_X1_P_PIN_CK0_CLK_P/N	AF02, AE01	Clock 0 Output	Data	EDI	DrvDiff				
NX_X1_P_PIN_CK0_DAT_[0:19]	AC05, W01, Y02, AA03, AA01, AB04, AB02, AC01, AC03, AD02, AD04, AG01, AE03, AH02, AF04, AE05, AG05, AD06, AF06, AE07	20-Bit Pack Data Output [00:19]	Data	EDI	Drv				
NX_PIN_P_X1_CK1_CLK_P/N	R07, T07	Clock 1 Input	Data	EDI	RecDiff				
NX_PIN_P_X1_CK1_DAT_[0:19]	AB10, AA10, AA09, Y09, Y08, W08, W07, V07, V06, U06, U05, T05, T04, R04, R03, P03, R06, P06, P05, N05	20-Bit Pack Data Input [00:19]	Data	EDI	Rec				
NX_X1_P_PIN_CK1_CLK_P/N	AK02, AJ01	Clock 1 Output	Data	EDI	DrvDiff				

Table 5-16. X Bus Signals (Sheet 2 of 3)

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
NX_X1_P_PIN_CK1_DAT_[0:19]	AJ09, AG07, AH08, AJ07, AG03, AH06, AH04, AJ05, AJ03, AK06, AK04, AL01, AL03, AM02, AN01, AL05, AM04, AR01, AP02, AN03	20-Bit Pack Data Output [00:19]	Data	EDI	Drv				
NX_PIN_P_X1_CK2_CLK_P/N	U09, V09	Clock 2 Input	Data	EDI	RecDiff				
NX_PIN_P_X1_CK2_DAT_[0:19]	K01, J01, L02, K02, M03, L03, N04, M04, U08, T08, N07, M07, P08, N08, R09, P09, W10, V10, R10, T10	20-Bit Pack Data Input [00:19]	Data	EDI	Rec				
NX_X1_P_PIN_CK2_CLK_P/N	AR07, AT06	Clock 2 Output	Data	EDI	DrvDiff				
NX_X1_P_PIN_CK2_DAT_[0:19]	AU01, AT02, AR03, AV02, AU03, AP04, AT04, AU05, AN05, AR05, AP06, AM06, AP08, AN07, AN09, AL07, AM10, AM08, AL09, AK08	20-Bit Pack Data Output [00:19]	Data	EDI	Drv				
NX_PIN_P_X1_CK3_CLK_P/N	L06, M06	Clock 3 Input	Data	EDI	RecDiff				

Table 5-16. X Bus Signals (Sheet 3 of 3)

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
NX_PIN_P_X1_CK3_DAT_[0:19]	G01, F01, H02, G02, J03, H03, K04, J04, L05, K05, H06, J06, J07, K07, K08, L08, L09, M09, M10, N10	20-Bit Pack Data Input [00:19]	Data	EDI	Rec				
NX_X1_P_PIN_CK3_CLK_P/N	BA01, AY02	Clock 3 Output	Data	EDI	DrvDiff				
NX_X1_P_PIN_CK3_DAT_[0:19]	AP10, AT10, AR09, AT08, AU07, AV06, AV04, AW03, AW01, AY04, BA03, BB02, BC01, AW05, AY06, BE01, BD02, BC03, BB04, BA05	20-Bit Pack Data Output [00:19]	Data	EDI	Drv				

5.2.13 PCIe Bus Signals

Table 5-17 lists the PCIe bus signals.

Table 5-17. PCIe Bus Signals (Sheet 1 of 4)

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
PV_PIN_P_CT_OSC0_E_REFCLK_P/N	Y37, Y36	PCIe Bus Input Reference Clock[1]	PLL/CLK	PCIE	RecDiff	No	N/A	Yes PCIe HCSL	No
PE_PIN_P_E0_CK0_DAT_[00:07]_P	G41, H42, J41, J43, J42, K44, L43, L45	Data Input (16× non-bifurcatable bus)	Data	PCIE	RecDiff				
PE_PIN_P_E0_CK0_DAT_[00:07]_N	F41, G42, H41, H43, K42, J44, K43, K45	Data Input (16× non-bifurcatable bus)	Data	PCIE	RecDiff				
PE_PIN_P_E0_CK1_DAT_[00:07]_P	M44, L46, N45, N47, N46, P48, R47, T48	Data Input (16× non-bifurcatable bus)	Data	PCIE	RecDiff				
PE_PIN_P_E0_CK1_DAT_[00:07]_N	L44, M46, M45, M47, P46, N48, P47, R48	Data Input (16× non-bifurcatable bus)	Data	PCIE	RecDiff				
PE_E0_P_PIN_CK0_DAT_[00:07]_P	D44, B45, E45, C46, A47, C48, F44, D47	Data Output (16× non-bifurcatable bus)	Data	PCIE	DrvDiff				
PE_E0_P_PIN_CK0_DAT_[00:07]_N	C44, A45, D45, B46, B47, B48, E44, C47	Data Output (16× non-bifurcatable bus)	Data	PCIE	DrvDiff				
PE_E0_P_PIN_CK1_DAT_[00:07]_P	F46, E48, F45, H48, F47, H46, J47, K48	Data Output (16× non-bifurcatable bus)	Data	PCIE	DrvDiff				
PE_E0_P_PIN_CK1_DAT_[00:07]_N	E46, D48, G45, G48, G47, G46, H47, J48	Data Output (16× non-bifurcatable bus)	Data	PCIE	DrvDiff				

1. See the IBM reference design for implementation details.
2. IBM uses a 4.7 KΩ pull-up. Follow the PCIe slot/device endpoint specifications. If the bus is not used, this pin can be a no connect. See *Section 3.3.4 PCIe Bus* on page 20 for additional information.
3. Do not connect to any voltages or signals. Connect the P/N signals with a 169 Ω, 1% 0402 resistor.
4. The PRSNT signal has an internal 1 KΩ pull-up to 1.1 V. An additional onboard pull-up of the specified value range is only required if the signal is part of a level-translation circuit. See *Section 3.3.4 PCIe Bus* on page 20 for additional information.

Table 5-17. PCIe Bus Signals (Sheet 2 of 4)

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
PE_CT_P_PIN_E0_PERST0_B	E39	PCIe Reset 0[2]	Control	OD	Drv		3.3 V AUX	Yes	Yes
PE_PIN_P_CT_E0_PRSNT0_B	E38	Present 0[4]	Control	OD	Rec	Pull-up ≤ 3 KΩ ±5%		No	No
PE_PIN_P_CT_E0_PRSNT1_B	E37	Present 1[4]	Control	OD	Rec	Pull-up ≤ 3 KΩ ±5%		No	No
PE_CT_P_PIN_E0_SLOT_CLK0_P/N	AC37, AD37	Clock 0 P/N	PLL	PCIE	DrvDiff	Pull-down 50 Ω ±5%	GND	Yes	Yes
PV_PIN_P_CT_E0_TERMREF_P/N	N37, P37	PHY Support[3]	PCIe	Analog	AnlgIn	No			
PV_PIN_P_CT_E1_TERMREF_P/N	AV37, AU37	PHY Support[3]	PCIe	Analog	AnlgIn	No			
PV_PIN_P_CT_E2_TERMREF_P/N	K37, L37	PHY Support[3]	PCIe	Analog	AnlgIn	No			
PE_PIN_P_E1_CK0_DAT_[00:07]_P	AU40, AR40, AW41, AT41, AW42, AU42, AY43, AW43	Data Input (16×/8× bifurcatable bus)	Data	PCIE	RecDiff				
PE_PIN_P_E1_CK0_DAT_[00:07]_N	AV40, AT40, AV41, AU41, AY42, AV42, BA43, AV43	Data Input (16×/8× bifurcatable bus)	Data	PCIE	RecDiff				
PE_PIN_P_E1_CK1_DAT_[00:07]_P	BE48, BD47, BC46, BD48, BC47, BB45, BA46, AY45	Data Input (16×/8× bifurcatable bus)	Data	PCIE	RecDiff				
PE_PIN_P_E1_CK1_DAT_[00:07]_N	BF48, BE47, BD46, BC48, BB47, BC45, BB46, BA45	Data Input (16×/8× bifurcatable bus)	Data	PCIE	RecDiff				
PE_E1_P_PIN_CK0_DAT_[00:07]_P	BA37, BB38, BA40, BC40, BB41, BD41, BC42, BE42	Data Output (16×/8× bifurcatable bus)	Data	PCIE	DrvDiff				

1. See the IBM reference design for implementation details.
2. IBM uses a 4.7 KΩ pull-up. Follow the PCIe slot/device endpoint specifications. If the bus is not used, this pin can be a no connect. See *Section 3.3.4 PCIe Bus* on page 20 for additional information.
3. Do not connect to any voltages or signals. Connect the P/N signals with a 169 Ω, 1% 0402 resistor.
4. The PRSNT signal has an internal 1 KΩ pull-up to 1.1 V. An additional onboard pull-up of the specified value range is only required if the signal is part of a level-translation circuit. See *Section 3.3.4 PCIe Bus* on page 20 for additional information.

Table 5-17. PCIe Bus Signals (Sheet 3 of 4)

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
PE_E1_P_PIN_CK0_DAT_[00:07]_N	BA38, BB39, BA39, BC39, BB40, BD40, BC41, BE41	Data Output (16×/8× bifurcatable bus)	Data	PCIE	DrvDiff				
PE_E1_P_PIN_CK1_DAT_[00:07]_P	BF43, BH45, BG44, BG46, BH46, BF45, BE44, BD43	Data Output (16×/8× bifurcatable bus)	Data	PCIE	DrvDiff				
PE_E1_P_PIN_CK1_DAT_[00:07]_N	BF42, BH44, BG43, BG45, BH47, BF44, BE43, BD42	Data Output (16×/8× bifurcatable bus)	Data	PCIE	DrvDiff				
$\overline{\text{PE\_CT\_P\_PIN\_E1\_PERST0\_B}}$	AW39	PCIe Reset 0[2]	Control	OD	Drv		3.3 V AUX	Yes	Yes
$\overline{\text{PE\_CT\_P\_PIN\_E1\_PERST1\_B}}$	AU39	PCIe Reset 1[2]	Control	OD	Drv		3.3 V AUX	Yes	Yes
$\overline{\text{PE\_PIN\_P\_CT\_E1\_PRSNT0\_B}}$	BB44	Present 0[4]	Control	OD	Rec	Pull-up ≤ 3 KΩ ±5%		No	No
$\overline{\text{PE\_PIN\_P\_CT\_E1\_PRSNT1\_B}}$	AY44	Present 1[4]	Control	OD	Rec	Pull-up ≤ 3 KΩ ±5%		No	No
PE_CT_P_PIN_E1_SLOT_CLK0_P/N	AF37, AG37	Clock 0	CLK	PCIE	DrvDiff	Pull-down 50 Ω ±5%	GND	Yes	No
PE_CT_P_PIN_E1_SLOT_CLK1_P/N	AJ37, AK37	Clock 1	CLK	PCIE	DrvDiff	Pull-down 50 Ω ±5%	GND	Yes	No
PE_PIN_P_E2_CK0_DAT_[00:07]_P	C39, B40, A41, B42, A42, C41, D40, D42	Data Input (8x bus)	Data	PCIE	RecDiff				
PE_PIN_P_E2_CK0_DAT_[00:07]_N	C38, B39, A40, B41, A43, C40, D39, D41	Data Input (8x bus)	Data	PCIE	RecDiff				

1. See the IBM reference design for implementation details.
2. IBM uses a 4.7 KΩ pull-up. Follow the PCIe slot/device endpoint specifications. If the bus is not used, this pin can be a no connect. See *Section 3.3.4 PCIe Bus* on page 20 for additional information.
3. Do not connect to any voltages or signals. Connect the P/N signals with a 169 Ω, 1% 0402 resistor.
4. The PRSNT signal has an internal 1 KΩ pull-up to 1.1 V. An additional onboard pull-up of the specified value range is only required if the signal is part of a level-translation circuit. See *Section 3.3.4 PCIe Bus* on page 20 for additional information.

Table 5-17. PCIe Bus Signals (Sheet 4 of 4)

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
PE_E2_P_PIN_CK0_DAT_[00:07]_P	K39, J38, H37, G36, H38, F37, G38, F39	Data Output (8x bus)	Data	PCIE	DrvDiff				
PE_E2_P_PIN_CK0_DAT_[00:07]_N	K38, J37, H36, G35, H39, F36, G37, F38	Data Output (8x bus)	Data	PCIE	DrvDiff				
PE_CT_P_PIN_E2_PERST0_B	E36	PCIe Reset 0[3]	Control	OD	Drv		3.3 V AUX	Yes	Yes
PE_PIN_P_CT_E2_PRSNT0_B	E42	Present 0[4]	Control	OD	Rec	Pull-up ≤ 3 KΩ ±5%		No	No
PE_CT_P_PIN_E2_SLOT_CLK0_P/N	AC36, AB36	Clock 0	Control	PCIE	DrvDiff	Pull-down 50 Ω ±5%	GND	Yes	No

1. See the IBM reference design for implementation details.
2. IBM uses a 4.7 KΩ pull-up. Follow the PCIe slot/device endpoint specifications. If the bus is not used, this pin can be a no connect. See *Section 3.3.4 PCIe Bus* on page 20 for additional information.
3. Do not connect to any voltages or signals. Connect the P/N signals with a 169 Ω, 1% 0402 resistor.
4. The PRSNT signal has an internal 1 KΩ pull-up to 1.1 V. An additional onboard pull-up of the specified value range is only required if the signal is part of a level-translation circuit. See *Section 3.3.4 PCIe Bus* on page 20 for additional information.

5.2.14 NVLink Bus Signals

Table 5-18 lists the NVLink bus signals.

Table 5-18. NVLink Bus Signals (Sheet 1 of 2)

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
PV_CT_P_PIN_MB_NV_REFCLK_P/N	V37, V38	NVLink Input Reference Clock[1]	PLL/CLK	CML	DrvDiff				
PV_PIN_P_CT_NV0_TERMREF_P/N	R37, T37	NVLink Terminal Reference[2]	NVLink	Analog	AnIgIn				
PV_PIN_P_CT_NV1_TERMREF_P/N	AM37, AN37	NVLink Terminal Reference[2]	NVLink	Analog	AnIgIn				
NV_PIN_P_V0_CK0_DAT_[00:15]_P	V43, V44, AC48, AA47, AA46, W48, Y45, V47, V46, U45, T44, R43, U42, P42, R41, N41	16-Bit Pack Data Input [00:15]	Data	IOO	RecDiff				
NV_PIN_P_V0_CK0_DAT_[00:15]_N	U43, W44, AB48, AB47, Y46, Y48, W45, W47, U46, T45, R44, P43, T42, N42, T41, M41	16-Bit Pack Data Input [00:15]	Data	IOO	RecDiff				
NV_V0_P_PIN_CK0_DAT_[00:15]_P	AK48, AJ47, AD45, AG48, AE46, AE47, AB44, AD43, AB43, AD42, Y42, AB41, W41, AA40, W40, Y39	16-Bit Pack Data Output [00:15]	Data	IOO	DrvDiff				
NV_V0_P_PIN_CK0_DAT_[00:15]_N	AJ48, AH47, AC45, AF48, AD46, AF47, AC44, AE43, AA43, AC42, AA42, AC41, Y41, AB40, V40, AA39	16-Bit Pack Data Output [00:15]	Data	IOO	DrvDiff				

1. See the IBM reference design for implementation details.
2. Do not connect to any voltages or signals. Connect the P/N signals with a 169 Ω, 1% 0402 resistor.

Table 5-18. NVLink Bus Signals (Sheet 2 of 2)

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
NV_PIN_P_V1_CK0_DAT_[00:15]_P	AW48, AW47, AU46, AU45, AR44, AR43, AN42, AN44, AG39, AH40, AK39, AJ41, AL42, AM40, AM43, AN41	16-Bit Pack Data Input [00:15]	Data	IOO	RecDiff				
NV_PIN_P_V1_CK0_DAT_[00:15]_N	AY48, AV47, AV46, AT45, AT44, AP43, AP42, AM44, AH39, AJ40, AL39, AK41, AK42, AL40, AL43, AM41	16-Bit Pack Data Input [00:15]	Data	IOO	RecDiff				
NV_V1_P_PIN_CK0_DAT_[00:15]_P	AC39, AD40, AF41, AG42, AH43, AJ44, AF44, AK45, AG46, AF45, AN48, AL47, AK46, AT48, AR47, AP46	16-Bit Pack Data Output [00:15]	Data	IOO	DrvDiff				
NV_V1_P_PIN_CK0_DAT_[00:15]_N	AD39, AE40, AE41, AF42, AG43, AH44, AE44, AJ45, AH46, AG45, AM48, AM47, AL46, AR48, AP47, AN46	16-Bit Pack Data Output [00:15]	Data	IOO	DrvDiff				

1. See the IBM reference design for implementation details.
2. Do not connect to any voltages or signals. Connect the P/N signals with a 169 Ω, 1% 0402 resistor.

5.2.15 PSI Signals

Table 5-19 lists the PSI signals. The PSI interface is not used in OpenPOWER systems; however, some of the nets require termination as shown in *Table 5-19*.

Table 5-19. PSI Signals

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
PV_CT_P_PIN_PSI_CLK_P/N	AG13, AG12	No connect. Float Output Clock.	PSI	EI4	DrvDiff	No	N/A	–	No
PV_CT_P_PIN_PSI_DATA	AH12	Output Data. No Connect.	PSI	EI4	Drv	No	N/A	–	No
PV_PIN_P_CT_PSI_DATA	AK12	Input Data. No Connect.	PSI	EI4	Rec	No	N/A	–	No
PV_PIN_P_CT_PSI_CLK_P	AL13	Unused. Terminate Input Clock.	PSI	EI4	RecDiff	Pull-down 49 Ω	GND	–	No
PV_PIN_P_CT_PSI_CLK_N	AL12	Unused. Terminate Input Clock.	PSI	EI4	RecDiff	Pull-up 49 Ω	1.1 V	–	No

5.2.16 Miscellaneous Signals

Table 5-20 lists the JTAG signals.

Note: JTAG is no longer widely use by IBM Power Systems™ except for debug.

Table 5-20. JTAG Signals

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
TS_PIN_P_CT_CARD_TEST	BE38	Unused. Tie Off.	Pervasive	CMOS	Rec	Pull-down ≤ 3 KΩ ±5%	GND	No	No
TS_PIN_P_CT_JTAG_TMS	H08	Unused. Tie Off.	Pervasive	CMOS	Drv	Pull-up ≤ 3 KΩ ±5%	1.1 V	No	No
TS_PIN_P_CT_JTAG_TDI	G07	Unused. Tie Off.	Pervasive	CMOS	Drv	Pull-up ≤ 3 KΩ ±5%	1.1 V	No	No
TS_CT_P_PIN_JTAG_TDO	F03	Unused. Tie Off.	Pervasive	CMOS	Rec	Pull-up ≤ 3 KΩ ±5%	1.1 V	No	No
TS_PIN_P_CT_EXT_TRIGGER_TCK	J09	Throttle Signal.[1, 2]	Pervasive	OD	BiDi	Pull-up ≥ 1 KΩ required	3.3 V	N/A	Yes, up to 3.65 V

1. The TS_PIN_P_CT_EXT_TRIGGER_TCK is an active low signal that can be asserted in the case of an emergency power drop situation. When asserted, it tells the OCC to go to the power state defined for the “N mode” attribute (OPEN_POWER_N_BULK_POWER_LIMIT_WATTS) in the XML file generated by the ServerWiz tool.
2. The reference design implements a possible use case for controlling the TS_PIN_P_CT_EXT_TRIGGER_TCK throttle pin. If one of the power supplies is powered off in a redundant power-supply system, the OCC is instructed to go to power-save mode, which can actuate in less than 10 ms via this throttle pin. This is useful if the total actual system power exceeds the capability of a single power supply (oversubscription). Another common use case is to tie TS_PIN_P_CT_EXT_TRIGGER_TCK to a BMC GPIO for software control.

6. Electrical Characteristics

This section provides AC and DC electrical specifications and thermal characteristics for the POWER8 with NVLink processor.

6.1 Frequency Domains

Table 6-1 lists the POWER8 with NVLink processor and POWER8 memory buffer frequency domains and scan frequency domains.

Table 6-1. POWER8 with NVLink Processor and POWER8 Memory Buffer Frequency Domains (Sheet 1 of 2)

Region	IP	Nominal Frequency	Maximum Frequency	Minimum Frequency	Supply Type	Functional Phase	ET Cycle (ps)	Scan Phase	Scan Cycles	Macro Pin
Core	C1, L2	Varied	5.5 GHz	1.2 GHz (200 MHz)	Adaptive and Dynamic	M, Mx2	208	S	416	nclk
Chiplet	L3, NCU	Varied	2.75 GHz	0.6 GHz (200 MHz)	Adaptive and Dynamic	M1x2	416	S1	416	cache_nclk
PB	Nest	2.4 GHz	2.7 GHz	1.9 GHz	Fixed (VIO)	NASYNC (x2), N[0:9] ASYNC (x2)	364	SN SN[0:9]	728	nest_nclk
MCIO	DMI	4.8 GHz	5.4 GHz	3.8 GHz	Fixed (VIO)	MCIO (x2lx4)	182/364/ 728	N/A	N/A	mcio_nclk
X	X0:3	2.4 GHz	2.6 GHz	1.7 GHz	Fixed (VIO)	X/X01 ASYNCH (x2)	364/728	SX/SX01	728	x_nclk
XIO	X0:3	2.4 GHz	2.6 GHz	1.7 GHz	Fixed (VIO)	XIO/XIOx2	364/728	N/A	N/A	xio_nclk
NVLink	NVLink	2.4 GHz	2.6 GHz	1.7 GHz	Fixed (VIO)	NVIOx4	340		680	nv_nclk
NVLinkIO	NVLink	9.6 GHz	10.08 GHz	7.67 GHz	Fixed (VIO)	NVIO/NVIO x4	85/340	N/A	N/A	nvio_nclk
PCIe	PCIe	1 GHz	1.1 GHz	0.9 GHz	Fixed (VIO)	PCIASYNC (x2lx4)	790/1580/ 3160	SPCI	790	pcie_nclk
PCIIO	PCI	8/5/2.5 GHz	8.8/5.5/2.5 GHz	7.2/4.5/2.25 GHz	Fixed (VPCI)	PCIIO (x2/x4/x8/ x16/x32/ x64/x128)	100	N/A	N/A	No grid clock; various tree clocks
PCIREF	PCI	0.1 GHz	0.1 GHz	0.1 GHz	Fixed (VPCI)	PCIREF	7900	N/A	N/A	No grid clock (trees)
PCIFB	PCI	0.1 GHz	0.1 GHz	0.1 GHz	Fixed (VPCI)	PCIFB	6400	N/A	N/A	No grid clock (trees)

1. Depends on PHY being at 1.2 V.

Table 6-1. POWER8 with NVLink Processor and POWER8 Memory Buffer Frequency Domains (Sheet 2 of 2)

Region	IP	Nominal Frequency	Maximum Frequency	Minimum Frequency	Supply Type	Functional Phase	ET Cycle (ps)	Scan Phase	Scan Cycles	Macro Pin
FSI	FSI	166 MHz	166 MHz	1 KHz	Fixed (VSB)	FS0CLK, FS1CLK, FSFCLK	5200	SFS	5200	fsi_ck
DDR Memory	MBU	2.4 GHz	2.6 GHz	1.33 GHz	Fixed (VDD)	MEM, MEM×2, MEM×4	326	SMEM	652	mem_nclk
SDR Memory	Combo PHY	1.2 GHz	1.2 GHz	667 MHz	Fixed (VDD, DDR)	DPHY0/1 (×2/×4), SYS, SYSC, SYSQ, SYSQC, RD, DQSMUX, WR	760[1]	SDPHY0 SDPHY1	760	dphy_nclk, sys_nclk, sysc_nclk, sysq_nclk, sysqc_nclk, rd_nclk, dqsmux_nclk, wr_nclk

1. Depends on PHY being at 1.2 V.

6.2 DC Electrical Characteristics

See the *POWER8 with NVIDIA NVLink Systems Power Design and Validation Guide* for voltage and current specifications.

6.2.1 Frequencies and TDP

Table 6-2 lists projected frequencies and TDPs for the POWER8 with NVLink processor.

Table 6-2. Frequencies and TDP

Part Number	Active Cores	Nominal Frequency (GHz)	Turbo Frequency (GHz)	Nominal TDP (W)	Turbo Power (W)	T_J Maximum (°C)	ADP T_J (°C)
00UL668	10	2.860	3.492	190	252	85	70
00UL670	8	3.259	3.857	190	260	85	70

6.2.2 Miscellaneous Signals

See the *I^2C Bus Specification (version 2.1)* for DC electrical details of the I^2C bus.

Table 6-3. I^2C DC Voltage

DC Voltage	Description
I^2C Voltage	3.3 V V_{DD}
V_{IH}	$V_{DD} \times 0.7 = 2.3$ V
V_{IL}	$V_{DD} \times 0.3 = 0.99$ V

See the *PCI Local Bus Specification (Revision 3.0)* for DC electrical details for the LPC bus.

See the *Signal Integrity Miscellaneous Nets Topology Design Guidelines for POWER8 with NVIDIA NVLink Power Systems* for additional information about the FSI signals.

6.3 AC Electrical Characteristics

This section provides the preliminary AC electrical characteristics for the POWER8 with NVLink processor. After fabrication, parts are sorted by maximum processor core frequency and tested for conformance to the AC specifications for that frequency.

6.3.1 Clock AC Specifications

System reference clocks are 133.33 MHz and use host clock signal level (HCSL) differential levels, which are the same as the PCIe standard levels. Termination of 50 Ω to GND on each phase is required and is built into the Silicon Labs clock generators that the POWER8 with NVLink processor uses. There is also the same 50 Ω to GND termination built into the differential receivers on the processor chip, but they are not enabled when the Silicon Labs clock generators are used. They must be enabled if some other vendor clock generator was used that did not have the integrated termination.

Spread spectrum is only allowed on the system reference clocks. It is limited to a spread percentage of 0.5% in the downward direction, which is the specification allowed by the DRAMs.

PCIe reference clocks are 100.00 MHz and use HCSL differential levels, which are the same as the PCIe standard levels. Termination of 50 Ω to GND on each phase is required and is built into the Silicon Labs clock generators that the POWER8 with NVLink processor uses. There is also the same 50 Ω to GND termination built into the differential receivers on the processor chip, but they are not enabled when the Silicon Labs clock generators are used. They must be enabled if some other vendor clock generator is used that does not have the integrated termination.

PCIe and system reference clocks are HCSL differential levels, which is the PCIe standard. Spread spectrum is not supported by POWER systems on PCIe.

The LPC clock to the processor is 33.33 MHz single-ended CMOS with an MPUL of 1.1 V. The IBM system has a resistor divider network on the board to support this. The reference clock skew specification for LPC is 2.0 ns.

The TOD reference clocks to the processor are 16.0 MHz (20 PPM frequency stability), single-ended CMOS with an MPUL of 1.1 V. There is a resistor divider network on the board to support this.

Figure 6-1 shows the differential HCSL reference clock waveforms.

Figure 6-1. Differential (HCSL) Reference Clock Waveform (System and PCIe)

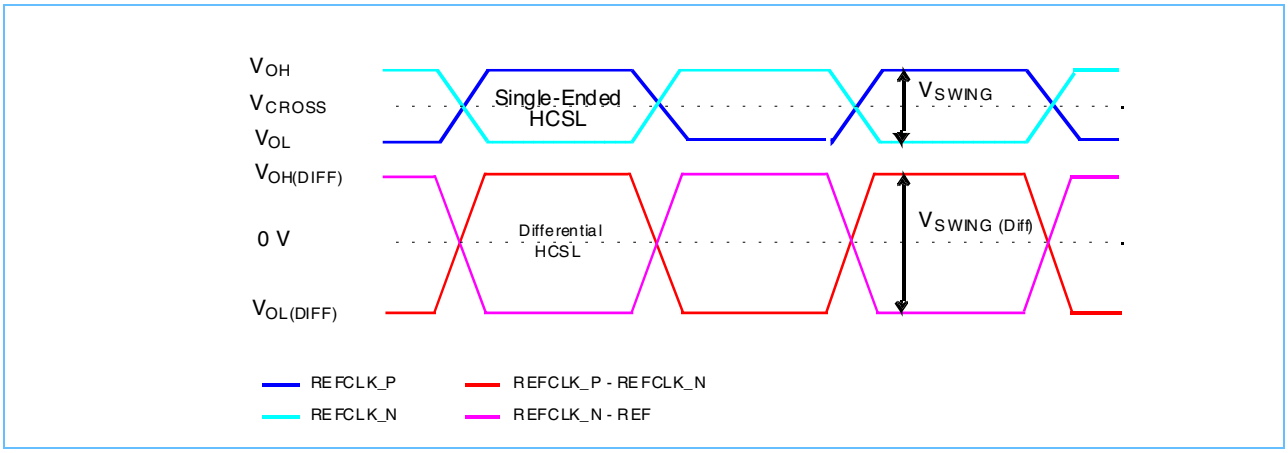


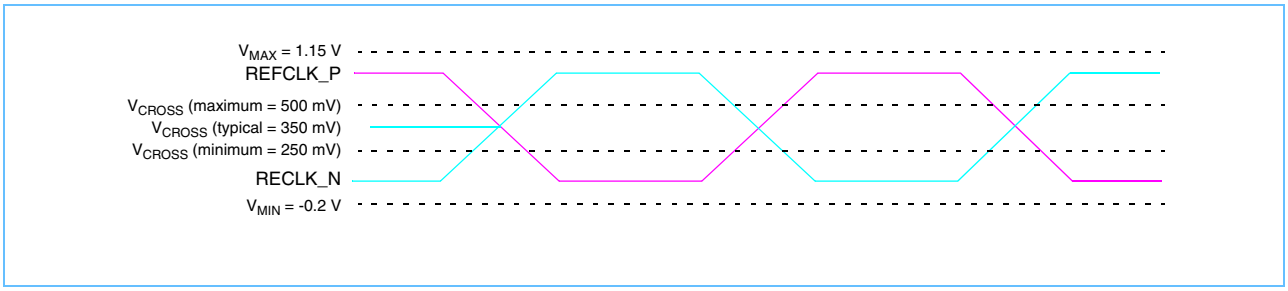
Table 6-4. Differential Reference Clock DC and AC Specification

Symbol	Parameter	Minimum	Typical	Maximum	Units	Notes
V_{OL}	Output low voltage	-0.10	0.0	0.1	V	1
V_{OH}	Output high voltage	0.50	0.70	0.90	V	1
V_{SWING}	Voltage swing	0.50	0.70	1.0	V	1
V_{CROSS}	Absolute crossing point (common mode voltage)	250	350	500	mV	1, 2, 3
V_{CROSS} Delta	Maximum variation in common mode voltage	–	–	100	mV	1, 2, 4
V_{MAX}	Absolute maximum voltage	–	–	1.15	V	1, 5
V_{MIN}	Absolute minimum voltage	-0.20	–	–	V	1, 6
V_{OL} (Diff)	Output low voltage	-0.5	-0.7	-0.9	V	7
V_{OH} (Diff)	Output high voltage	0.50	0.70	0.90	V	7
V_{SWING} (Diff)	Voltage swing (differential)	1.0	1.4	1.8	V	7
T_R, T_F (Diff)	Rising and falling edge rates (differential)	1.0	2.0	4.0	V/ns	7, 8
V_{RB}	Ringback voltage margin	-100	–	100	mV	7, 9
T_{STABLE}	Time before V_{RB} is allowed	500	–	–	ps	7, 9
Duty Cycle	Duty cycle	45	–	55	%	7
T Period Average	Average clock period accuracy	50	–	2550	PPM	7, 10, 11, 12

1. Measurement taken from a single-ended waveform (see *Table 6-1* on page 66).
2. Measured at the crossing point where the instantaneous voltage value of the rising edge of REFCLK_P equals the falling edge of REFCLK_N (see *Figure 6-2* on page 68).
3. Refers to the total variation from the lowest crossing point to the highest crossing point, regardless of which edges are crossing. Refers to all crossing points for this measurement (see *Figure 6-2* on page 68).
4. Defined as the total variation of all crossing voltages of rising REFCLK_P and falling REFCLK_N. This is the maximum allowed variance in V_{CROSS} for any particular system (see *Figure 6-3* on page 68).
5. Defined as the maximum instantaneous voltage including overshoot (see *Figure 6-2* on page 68).
6. Defined as the minimum instantaneous voltage including overshoot (see *Figure 6-2* on page 68).
7. Measurement taken from a differential waveform (see *Figure 6-1* on page 66).
8. Measured from -150 mV to +150 mV on the differential waveform (derived from REFCLK_P - REFCLK_N). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing (see *Figure 6-5* on page 69).
9. T_{STABLE} is the time that the differential clock must maintain a minimum ±150 mV differential voltage after the rising/falling edges before it is allowed to drop back into the V_{RB} ±100 mV differential range (see *Figure 6-6* on page 69).
10. Defined as the average period. This includes crystal PPM and spread spectrum.
11. Defined as the frequency accuracy specification of the crystal that is used to generate the reference clock (typically less than 100 PPM).
12. PPM refers to parts per million and is a DC absolute period accuracy specification. One PPM is 1/1,000,000th of the clock frequency. The period is to be measured with a frequency counter with the measurement window set to 100 ms or greater. For systems that use spread-spectrum clocking, there is an additional 2,500 PPM average shift in the maximum period resulting from a 0.5% down spread.

Figure 6-2 shows the single-ended measurement points for absolute cross points and swing.

Figure 6-2. Single-Ended Measurement Points for Absolute Cross Points and Swing



6.3.2 Differential Reference Clock Measurements

Figure 6-3 shows the single-ended measurement points for the delta cross point.

Figure 6-3. Single-Ended Measurement Points for Delta Cross Point

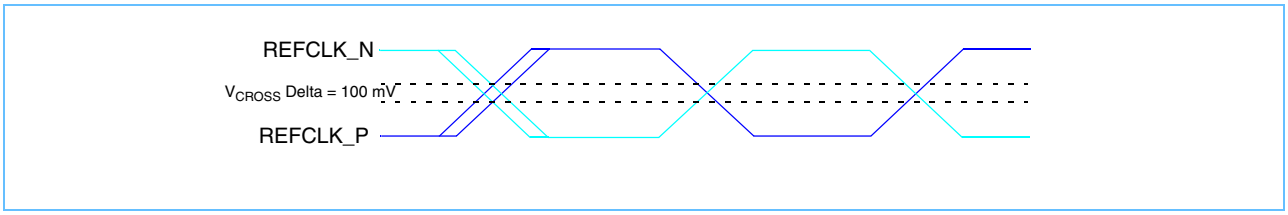


Figure 6-4 shows the differential measurement points for the duty cycle and period.

Figure 6-4. Differential Measurement Points for Duty Cycle and Period

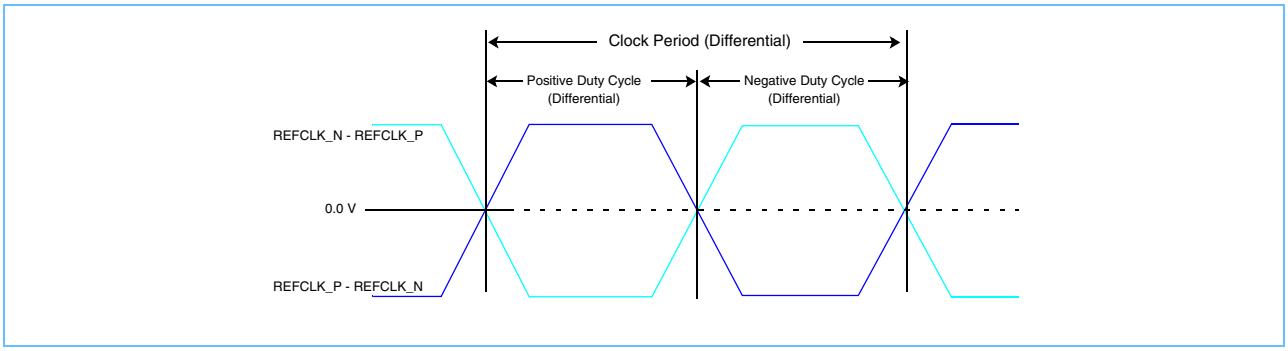


Figure 6-5 shows the differential measurement points for the rise and fall times.

Figure 6-5. Differential Measurement Points for Rise and Fall Times

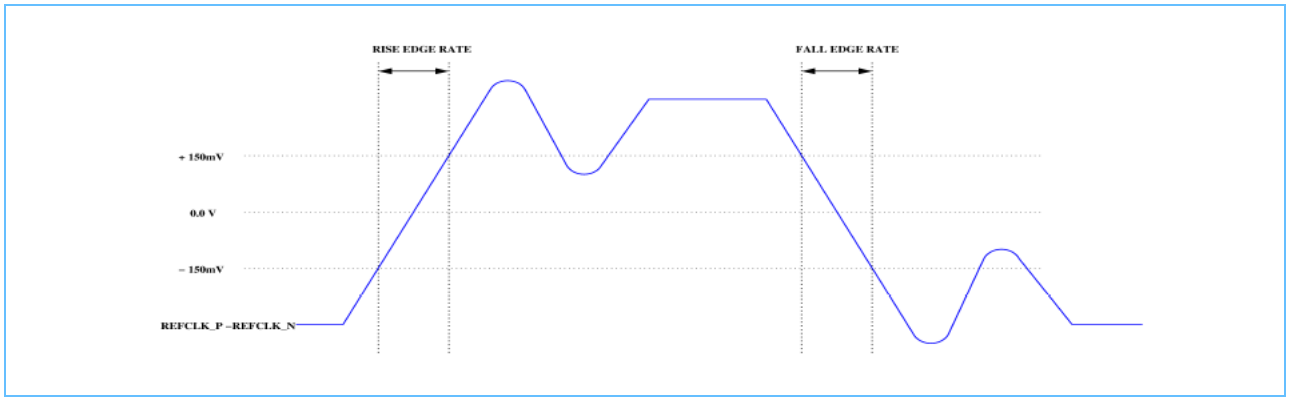


Figure 6-6 shows the differential measurement points for ringback.

Figure 6-6. Differential Measurement Points for Ringback

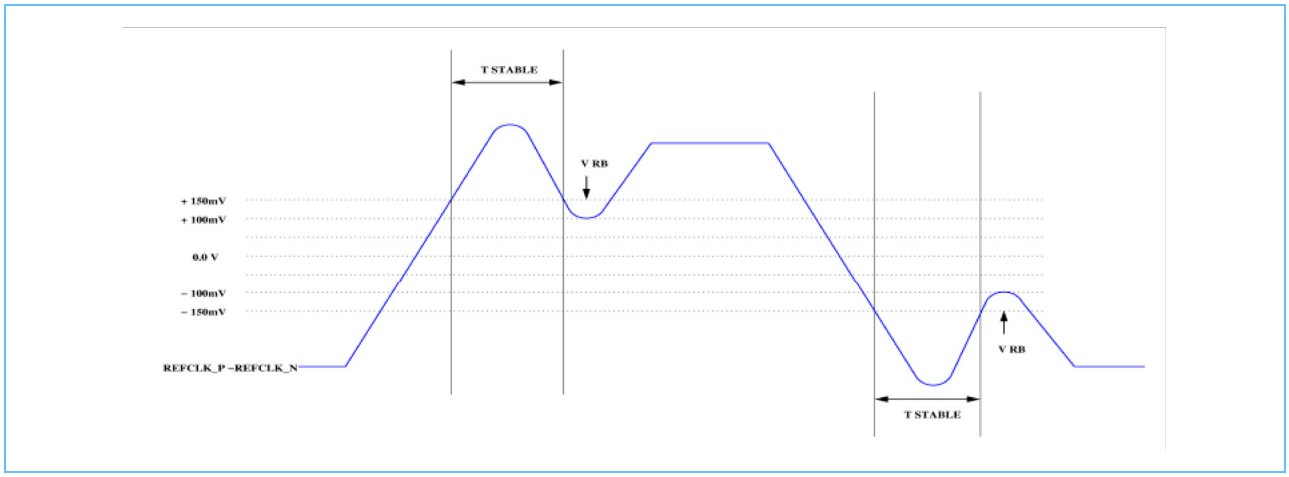


Table 6-5 lists general DC and AC specifications.

Table 6-5. DC and AC Specifications

Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units	Notes
Output Voltage	V_{OL}	Output low voltage	–	0	0.2	V	1
	V_{OH}	Output high voltage	0.8	1.0	1.15	V	1
	V_{SWING}	Peak-peak, single-ended swing	0.8	1.0	1,15	V	1, 2
Rise and Fall Times	T_R, T_F	20% - 80%	–	1.5	3.0	ns	1, 3
Duty Cycle	DC	Measured at $V_{SWING}/2$	45	–	55	%	1, 2, 4
Clock Period	T_{AVG}	Clock period accuracy	-50	–	+50	PPM	1, 2, 4, 5

1. Measurements taken from a single-ended waveform (see *Figure 6-7* on page 70).
2. Voltage swing is equal to V_{OH} - V_{OL} (see *Figure 6-7* on page 70).
3. Rise and fall time measurements taken between 20% and 80% of V_{OH} and V_{OL} (see *Figure 6-7* on page 70).
4. Measurements taken at a voltage equal to $V_{SWING}/2$ (see *Figure 6-8* on page 71).
5. PPM refers to parts per million and is a DC absolute period accuracy specification. It includes only the accuracy of the crystal that is used to generate the clock because spread spectrum is not enabled. The period is to be measured with a frequency counter with the measurement window set to 100 ms or greater,

Figure 6-7 shows the single-ended processor reference clocks and highlights the voltage and transition time measurement points.

Figure 6-7. Single-Ended Processor Reference Clocks (Voltage and Transition Time Measurement Points)

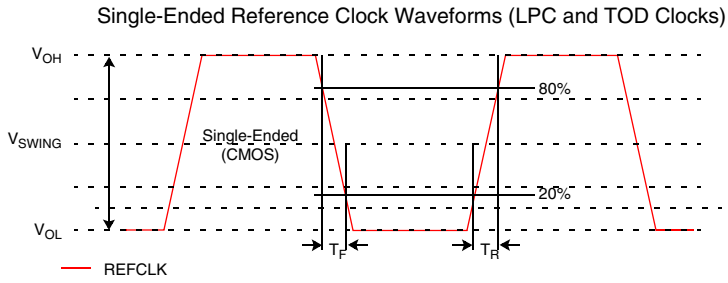
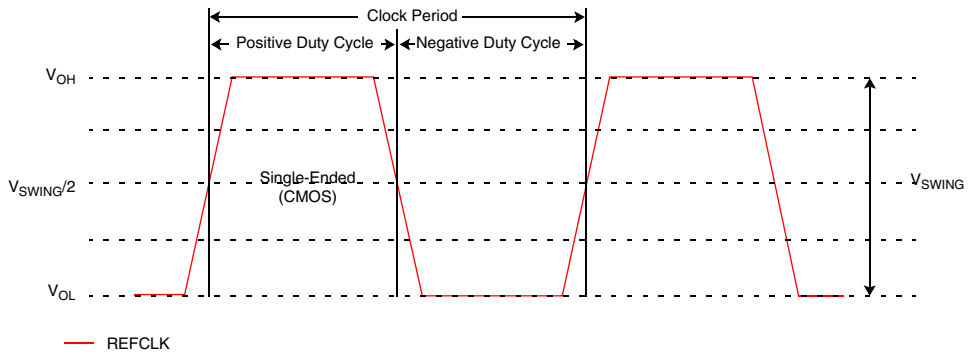


Figure 6-8 shows the single-ended processor reference clocks and highlights the period and duty cycle measurement points.

Figure 6-8. Single-Ended Processor Reference Clocks (Period and Duty-Cycle Measurement Points)



6.3.3 FSI AC Specifications

Table 6-6 lists the AC specifications for the FSI bus.

Table 6-6. FSI Electrical Specification

Description	Minimum	Typical	Maximum	Units	Notes
C4 V_{MAX}			1.65	V	Maximum voltage at the chip pad.
Receiver V_{IL}			$0.3 \times 1.2\ V_{SB}$	mV	For receiver input hysteresis.
Receiver V_{IH}	$0.7 \times 1.2\ V_{SB}$			mV	For receiver input hysteresis.
1 KΩ Pull-up Resistance	1 KΩ	1.25 KΩ	1.5 KΩ	Ω	Pull-up resistance without leakage. If external pull-ups are used, they must be returned to V_{DOUT} and have a combined impedance not smaller than 1 KΩ.
1 KΩ Pull-down Resistance	1 KΩ	1.25 KΩ	1.5 KΩ	Ω	Pull-down resistance without leakage. If external pull downs are used, they have a combined impedance not smaller than 1 KΩ in parallel with 10 KΩ.
10 KΩ Pull-down Resistance	10 KΩ	12.5 KΩ	15 KΩ	Ω	Pull-up resistance without leakage.
Driver V_{OL}	$-0.1 \times 1.2\ V_{SB}$		$0.2 \times 1.2\ V_{SB}$	mV	Output pad driver levels.
Driver V_{OH}	$0.8 \times 1.2\ V_{SB}$		$1.1 \times 1.2\ V_{SB}$	mV	Output pad driver levels.
Duty Cycle distortion at 533 MHz with a 2 pF load	44.8	0	55.2	%	
Rise/Fall Time (10% - 90% of V_{DOUT} with a 2 pF load)	100	300	500	ps	

Table 6-7 lists the default settings for the internal FSI pull-up and pull-down resistors.

Table 6-7. Default FSI Settings

Function	SCM Pin	Pull-Up Internal Value	Pull-Down Internal Value
FSI Slave Clock	BH40	–	10 KΩ
FSI Slave Data	BH41	1 KΩ	–
FSI1 Clock	BG23	–	10 KΩ
FSI1 Data	BE23	1 KΩ	–
FSI Master 2 Clock	BD34	–	–
FSI Master 2 Data	BD35	–	10 KΩ
FSI Master 3 Clock	BC33	–	–
FSI Master 3 Data	BC34	–	10 KΩ
FSI Master 6 Clock	BB32	–	–
FSI Master 6 Data	BB33	–	10 KΩ
FSI Master 7 Clock	BA31	–	–
FSI Master 7 Data	BA32	–	10 KΩ
FSI Master CP 1 Clock	BE35	–	–
FSI Master CP 1 Data	BE36	–	10 KΩ

6.3.4 SPI AC Specifications

Table 6-8 list the AC specifications for the SPI bus.

Table 6-8. SPI AC Specification

Description	Minimum	Typical	Maximum	Units	Notes
C4 V_{MAX}			1.65	V	Maximum voltage at the chip pad.
Receiver V_{IL}			$0.3 \times V_{I/O}$	mV	For receiver input hysteresis.
Receiver V_{IH}	$0.7 \times V_{I/O}$			mV	For receiver input hysteresis.
1 KΩ pull-up resistance	1 KΩ	1.25 KΩ	1.5 KΩ	Ω	Pull-up resistance without leakage. If external pull-ups are used, they must be returned to V_{DOUT} and have a combined impedance not smaller than 1 KΩ.
1 KΩ pull-down resistance	1 KΩ	1.25 KΩ	1.5 KΩ	Ω	Pull-down resistance without leakage. If external pull downs are used, they have a combined impedance not smaller than 1 KΩ in parallel with 10 KΩ.
10 KΩ pull-down resistance	10 KΩ	12.5 KΩ	15 KΩ	Ω	Pull-up resistance without leakage.
Driver V_{OL}	$-0.1 \times V_{I/O}$		$0.2 \times V_{I/O}$	mV	Output pad driver levels.
Driver V_{OH}	$0.8 \times V_{I/O}$		$1.1 \times V_{I/O}$	mV	Output pad driver levels.
Duty cycle distortion at 533 MHz with a 2 pF load	44.8	0	55.2	%	
Rise/fall time (10% - 90% of V_{DOUT} with a 2 pF load)	100	300	500	ps	

Table 6-9 lists the default settings for the internal SPI pull-up and pull-down resistors.

Table 6-9. Default SPI Settings

Function	SCM Pin	Pull-Up Internal Value	Pull-Down Internal Value
SPIVID0_MOSI	F34	–	–
SPIVID0_MISO	J30	–	–
SPIVID0_SCLK	G33	–	10 KΩ
SPIVID0_CS	J29	1 KΩ	–
SPIPSS_MOSI	J32	–	–
SPIPSS_MISO	J35	–	–
SPIPSS_SCLK	H34	–	10 KΩ
SPIPSS_CS0	H32	1 KΩ	–
SPIPSS_CS1	J33	1 KΩ	–

7. Mechanical Specifications

This section describes the POWER8 with NVLink SCM features and pin list.

7.1 Single-Chip Module

Table 7-1 describes the POWER8 Processor with NVLink Interconnect SCM.

Table 7-1. SCM Features

Feature	Description
Body Size	50 x 50 mm
Package Type	FC PLGA
Interconnect Technology	22 nm silicon-on-insulator (SOI)
	1.0 mm orthogonal pin pitch
	6-2-6 LGA
Buses	Four DMI interfaces at 9.6 Gbps
	One 8-byte X bus at 4.8 Gb/s
	Two ×16 and one ×8 PCIe Generation 3 at 8 Gb/s
	Four ×8 NVLink bricks at 19.2 Gb/s
Power	190 W
	Four ×8 NVLink bricks at 19.2 Gb/s
Package Pin Assignments	2296 total
SEEPROM Structure	Single SEEPROM

7.2 Electrostatic Discharge Considerations

The POWER8 with NVLink processor is electrostatic discharge (ESD) sensitive. An appropriate ESD handling procedure must be implemented and maintained by facilities handling this component. Handle according to the ANSI/ESD S20.20 or IEC 61340-5-1 standard. Packaging of this product in an ESD safe container must be maintained according to the ANSI/ESD S541 or IEC 61340-5-3 standard.

The POWER8 with NVLink processor has completed an ESD stress qualification in accordance with the JEDEC specification JESD47I. The levels shown in *Table 7-2* have been met.

Table 7-2. ESD Stress Qualification

ESD Model	Passing Level	Reference
Human Body Model	1000 V	JS-001[1]
Charged Device Model (CDM)	200 V	JESD22-C101[2]

1. JS-001-2014 is the Joint JEDEC/ESDA Standard for Electrostatic Discharge Sensitivity Test - Human Body Model (HBM) Component Level.
2. JESD22-C101F is the Field-Induced Charged-Device Model Test Method for Electrostatic Discharge Withstand Thresholds of Microelectronic Components.

7.3 Mechanical Drawings

See the IBM Portal for OpenPOWER for the current mechanical drawings and recommended module layout.

7.4 Pinout

Table 7-3 SCM Pin List on page 77 shows the signal pins for the POWER8 with NVLink processor by position.

Table 7-3. SCM Pin List

Position	Net Name
A04	GND
A05	MM_M0_P_PIN_CKC_DAT_16_N
A06	MM_M0_P_PIN_CKC_DAT_16_P
A07	GND
A08	MM_M0_P_PIN_CKC_DAT_13_N
A09	MM_M0_P_PIN_CKC_DAT_13_P
A10	MM_M0_P_PIN_CKC_DAT_11_N
A11	MM_M0_P_PIN_CKC_DAT_11_P
A12	GND
A13	GND
A14	MM_PIN_P_M0_CKD_DAT_07_P
A15	MM_PIN_P_M0_CKD_DAT_07_N
A16	MM_PIN_P_M0_CKD_DAT_11_P
A17	MM_PIN_P_M0_CKD_DAT_11_N
A18	GND
A19	MM_PIN_P_M0_CKD_DAT_13_P
A20	MM_PIN_P_M0_CKD_DAT_13_N
A21	MM_PIN_P_M0_CKD_DAT_17_N
A22	MM_PIN_P_M0_CKD_DAT_17_P
A23	GND
A24	GND
A25	MM_PIN_P_M0_CKC_DAT_03_P
A26	MM_PIN_P_M0_CKC_DAT_03_N
A27	GND
A28	MM_PIN_P_M0_CKC_DAT_07_P
A29	MM_PIN_P_M0_CKC_DAT_07_N
A30	GND
A31	MM_PIN_P_M0_CKC_DAT_11_P
A32	MM_PIN_P_M0_CKC_DAT_11_N
A33	GND
A34	MM_PIN_P_M0_CKC_DAT_13_P
A35	MM_PIN_P_M0_CKC_DAT_13_N
A36	MM_PIN_P_M0_CKC_DAT_17_N
A37	MM_PIN_P_M0_CKC_DAT_17_P
A38	GND
A39	GND
A40	PE_PIN_P_E2_CK0_DAT_02_N
A41	PE_PIN_P_E2_CK0_DAT_02_P
A42	PE_PIN_P_E2_CK0_DAT_04_P
A43	PE_PIN_P_E2_CK0_DAT_04_N
A44	GND
A45	PE_E0_P_PIN_CK0_DAT_01_N
A46	GND
A47	PE_E0_P_PIN_CK0_DAT_04_P
A48	GND
B03	GND
B04	MM_M0_P_PIN_CKD_DAT_15_N
B05	MM_M0_P_PIN_CKD_DAT_15_P
B06	MM_M0_P_PIN_CKC_DAT_15_N
B07	MM_M0_P_PIN_CKC_DAT_15_P
B08	GND
B09	MM_M0_P_PIN_CKC_DAT_12_N
B10	MM_M0_P_PIN_CKC_DAT_12_P
B11	MM_M0_P_PIN_CKC_DAT_09_N
B12	MM_M0_P_PIN_CKC_DAT_09_P
B13	GND
B14	GND
B15	MM_PIN_P_M0_CKD_DAT_09_P
B16	MM_PIN_P_M0_CKD_DAT_09_N
B17	MM_PIN_P_M0_CKD_CLK_P
B18	MM_PIN_P_M0_CKD_CLK_N
B19	GND
B20	MM_PIN_P_M0_CKD_DAT_15_P
B21	MM_PIN_P_M0_CKD_DAT_15_N
B22	MM_PIN_P_M0_CKD_DAT_18_N
B23	MM_PIN_P_M0_CKD_DAT_18_P
B24	GND
B25	GND
B26	GND
B27	MM_PIN_P_M0_CKC_DAT_02_P
B28	MM_PIN_P_M0_CKC_DAT_02_N
B29	GND
B30	MM_PIN_P_M0_CKC_DAT_09_P
B31	MM_PIN_P_M0_CKC_DAT_09_N
B32	GND
B33	MM_PIN_P_M0_CKC_DAT_12_P
B34	MM_PIN_P_M0_CKC_DAT_12_N
B35	MM_PIN_P_M0_CKC_DAT_15_P
B36	MM_PIN_P_M0_CKC_DAT_15_N
B37	GND
B38	GND
B39	PE_PIN_P_E2_CK0_DAT_01_N
B40	PE_PIN_P_E2_CK0_DAT_01_P
B41	PE_PIN_P_E2_CK0_DAT_03_N
B42	PE_PIN_P_E2_CK0_DAT_03_P
B43	GND
B44	GND
B45	PE_E0_P_PIN_CK0_DAT_01_P
B46	PE_E0_P_PIN_CK0_DAT_03_N
B47	PE_E0_P_PIN_CK0_DAT_04_N
B48	PE_E0_P_PIN_CK0_DAT_05_N
C02	MM_M0_P_PIN_CKD_DAT_12_N
C03	MM_M0_P_PIN_CKD_DAT_12_P
C04	GND
C05	MM_M0_P_PIN_CKD_DAT_14_N
C06	MM_M0_P_PIN_CKD_DAT_14_P
C07	MM_M0_P_PIN_CKD_DAT_16_N
C08	MM_M0_P_PIN_CKD_DAT_16_P
C09	GND
C10	MM_M0_P_PIN_CKC_DAT_10_N
C11	MM_M0_P_PIN_CKC_DAT_10_P
C12	MM_M0_P_PIN_CKC_DAT_08_N
C13	MM_M0_P_PIN_CKC_DAT_08_P
C14	GND
C15	GND
C16	MM_PIN_P_M0_CKD_DAT_08_P
C17	MM_PIN_P_M0_CKD_DAT_08_N
C18	MM_PIN_P_M0_CKD_DAT_10_P
C19	MM_PIN_P_M0_CKD_DAT_10_N
C20	GND
C21	MM_PIN_P_M0_CKD_DAT_16_N
C22	MM_PIN_P_M0_CKD_DAT_16_P
C23	MM_PIN_P_M0_CKD_DAT_20_N
C24	MM_PIN_P_M0_CKD_DAT_20_P

Position	Net Name
C25	GND
C26	MM_PIN_P_M0_CKC_DAT_00_P
C27	MM_PIN_P_M0_CKC_DAT_00_N
C28	GND
C29	MM_PIN_P_M0_CKC_DAT_08_P
C30	MM_PIN_P_M0_CKC_DAT_08_N
C31	GND
C32	MM_PIN_P_M0_CKC_CLK_P
C33	MM_PIN_P_M0_CKC_CLK_N
C34	MM_PIN_P_M0_CKC_DAT_16_N
C35	MM_PIN_P_M0_CKC_DAT_16_P
C36	GND
C37	GND
C38	PE_PIN_P_E2_CK0_DAT_00_N
C39	PE_PIN_P_E2_CK0_DAT_00_P
C40	PE_PIN_P_E2_CK0_DAT_05_N
C41	PE_PIN_P_E2_CK0_DAT_05_P
C42	GND
C43	GND
C44	PE_E0_P_PIN_CK0_DAT_00_N
C45	GND
C46	PE_E0_P_PIN_CK0_DAT_03_P
C47	PE_E0_P_PIN_CK0_DAT_07_N
C48	PE_E0_P_PIN_CK0_DAT_05_P
D01	MM_M0_P_PIN_CKD_DAT_10_N
D02	MM_M0_P_PIN_CKD_DAT_10_P
D03	MM_M0_P_PIN_CKD_DAT_11_N
D04	MM_M0_P_PIN_CKD_DAT_11_P
D05	GND
D06	MM_M0_P_PIN_CKD_CLK_P
D07	MM_M0_P_PIN_CKD_CLK_N
D08	MM_M0_P_PIN_CKD_DAT_13_N
D09	MM_M0_P_PIN_CKD_DAT_13_P
D10	GND
D11	MM_M0_P_PIN_CKC_DAT_14_N
D12	MM_M0_P_PIN_CKC_DAT_14_P
D13	MM_M0_P_PIN_CKC_DAT_07_N
D14	MM_M0_P_PIN_CKC_DAT_07_P

Position	Net Name
D15	GND
D16	GND
D17	MM_PIN_P_M0_CKD_DAT_06_P
D18	MM_PIN_P_M0_CKD_DAT_06_N
D19	MM_PIN_P_M0_CKD_DAT_12_P
D20	MM_PIN_P_M0_CKD_DAT_12_N
D21	GND
D22	MM_PIN_P_M0_CKD_DAT_21_N
D23	MM_PIN_P_M0_CKD_DAT_21_P
D24	GND
D25	GND
D26	PV_PIN_P_CT_SPARE2
D27	GND
D28	MM_PIN_P_M0_CKC_DAT_05_P
D29	MM_PIN_P_M0_CKC_DAT_05_N
D30	GND
D31	MM_PIN_P_M0_CKC_DAT_14_P
D32	MM_PIN_P_M0_CKC_DAT_14_N
D33	MM_PIN_P_M0_CKC_DAT_18_N
D34	MM_PIN_P_M0_CKC_DAT_18_P
D35	GND
D36	TS_CT_P_PIN_AMX0_VSENSE
D37	TS_CT_P_PIN_AMX0_GSENSE
D38	GND
D39	PE_PIN_P_E2_CK0_DAT_06_N
D40	PE_PIN_P_E2_CK0_DAT_06_P
D41	PE_PIN_P_E2_CK0_DAT_07_N
D42	PE_PIN_P_E2_CK0_DAT_07_P
D43	GND
D44	PE_E0_P_PIN_CK0_DAT_00_P
D45	PE_E0_P_PIN_CK0_DAT_02_N
D46	GND
D47	PE_E0_P_PIN_CK0_DAT_07_P
D48	PE_E0_P_PIN_CK1_DAT_01_N
E01	GND
E02	GND
E03	GND
E04	MM_M0_P_PIN_CKD_DAT_09_N

Position	Net Name
E05	MM_M0_P_PIN_CKD_DAT_09_P
E06	GND
E07	MM_M0_P_PIN_CKD_DAT_07_P
E08	MM_M0_P_PIN_CKD_DAT_07_N
E09	MM_M0_P_PIN_CKD_DAT_05_P
E10	MM_M0_P_PIN_CKD_DAT_05_N
E11	GND
E12	MM_M0_P_PIN_CKC_CLK_P
E13	MM_M0_P_PIN_CKC_CLK_N
E14	MM_M0_P_PIN_CKC_DAT_05_P
E15	MM_M0_P_PIN_CKC_DAT_05_N
E16	GND
E17	GND
E18	MM_PIN_P_M0_CKD_DAT_05_P
E19	MM_PIN_P_M0_CKD_DAT_05_N
E20	MM_PIN_P_M0_CKD_DAT_14_P
E21	MM_PIN_P_M0_CKD_DAT_14_N
E22	GND
E23	MM_PIN_P_M0_CKD_DAT_22_N
E24	MM_PIN_P_M0_CKD_DAT_22_P
E25	GND
E26	GND
E27	MM_PIN_P_M0_CKC_DAT_04_P
E28	MM_PIN_P_M0_CKC_DAT_04_N
E29	GND
E30	MM_PIN_P_M0_CKC_DAT_19_N
E31	MM_PIN_P_M0_CKC_DAT_19_P
E32	MM_PIN_P_M0_CKC_DAT_20_N
E33	MM_PIN_P_M0_CKC_DAT_20_P
E34	GND
E35	GND
E36	PE_CT_P_PIN_E2_PERST0_B
E37	PE_PIN_P_CT_E0_PRSNT1_B
E38	PE_PIN_P_CT_E0_PRSNT0_B
E39	PE_CT_P_PIN_E0_PERST0_B
E40	GND
E41	GND
E42	PE_PIN_P_CT_E2_PRSNT0_B

Position	Net Name
E43	GND
E44	PE_E0_P_PIN_CK0_DAT_06_N
E45	PE_E0_P_PIN_CK0_DAT_02_P
E46	PE_E0_P_PIN_CK1_DAT_00_N
E47	GND
E48	PE_E0_P_PIN_CK1_DAT_01_P
F01	NX_PIN_P_X1_CK3_DAT_01
F02	GND
F03	TS_CT_P_PIN_JTAG_TDO
F04	GND
F05	MM_M0_P_PIN_CKD_DAT_08_P
F06	MM_M0_P_PIN_CKD_DAT_08_N
F07	GND
F08	MM_M0_P_PIN_CKD_DAT_06_P
F09	MM_M0_P_PIN_CKD_DAT_06_N
F10	MM_M0_P_PIN_CKD_DAT_03_P
F11	MM_M0_P_PIN_CKD_DAT_03_N
F12	GND
F13	MM_M0_P_PIN_CKC_DAT_06_P
F14	MM_M0_P_PIN_CKC_DAT_06_N
F15	MM_M0_P_PIN_CKC_DAT_03_P
F16	MM_M0_P_PIN_CKC_DAT_03_N
F17	GND
F18	GND
F19	MM_PIN_P_M0_CKD_DAT_04_P
F20	MM_PIN_P_M0_CKD_DAT_04_N
F21	MM_PIN_P_M0_CKD_DAT_19_N
F22	MM_PIN_P_M0_CKD_DAT_19_P
F23	GND
F24	MM_PIN_P_M0_CKD_DAT_23_N
F25	MM_PIN_P_M0_CKD_DAT_23_P
F26	GND
F27	GND
F28	MM_PIN_P_M0_CKC_DAT_10_P
F29	MM_PIN_P_M0_CKC_DAT_10_N
F30	GND
F31	MM_PIN_P_M0_CKC_DAT_21_N
F32	MM_PIN_P_M0_CKC_DAT_21_P

Position	Net Name
F33	GND
F34	PV_CT_P_PIN_SPIVID0_MOSI
F35	GND
F36	PE_E2_P_PIN_CK0_DAT_05_N
F37	PE_E2_P_PIN_CK0_DAT_05_P
F38	PE_E2_P_PIN_CK0_DAT_07_N
F39	PE_E2_P_PIN_CK0_DAT_07_P
F40	GND
F41	PE_PIN_P_E0_CK0_DAT_00_N
F42	GND
F43	GND
F44	PE_E0_P_PIN_CK0_DAT_06_P
F45	PE_E0_P_PIN_CK1_DAT_02_P
F46	PE_E0_P_PIN_CK1_DAT_00_P
F47	PE_E0_P_PIN_CK1_DAT_04_P
F48	GND
G01	NX_PIN_P_X1_CK3_DAT_00
G02	NX_PIN_P_X1_CK3_DAT_03
G03	GND
G04	GND
G05	GND
G06	GND
G07	TS_PIN_P_CT_JTAG_TDI
G08	GND
G09	MM_M0_P_PIN_CKD_DAT_04_N
G10	MM_M0_P_PIN_CKD_DAT_04_P
G11	MM_M0_P_PIN_CKD_DAT_01_P
G12	MM_M0_P_PIN_CKD_DAT_01_N
G13	GND
G14	MM_M0_P_PIN_CKC_DAT_04_P
G15	MM_M0_P_PIN_CKC_DAT_04_N
G16	MM_M0_P_PIN_CKC_DAT_00_P
G17	MM_M0_P_PIN_CKC_DAT_00_N
G18	GND
G19	GND
G20	MM_PIN_P_M0_CKD_DAT_02_P
G21	MM_PIN_P_M0_CKD_DAT_02_N
G22	MM_PIN_P_M0_CKD_DAT_03_N

Position	Net Name
G23	MM_PIN_P_M0_CKD_DAT_03_P
G24	GND
G25	GND
G26	GND
G27	MM_PIN_P_M0_CKC_DAT_06_P
G28	MM_PIN_P_M0_CKC_DAT_06_N
G29	GND
G30	MM_PIN_P_M0_CKC_DAT_22_N
G31	MM_PIN_P_M0_CKC_DAT_22_P
G32	GND
G33	PV_CT_P_PIN_SPIVID0_SCLK
G34	GND
G35	PE_E2_P_PIN_CK0_DAT_03_N
G36	PE_E2_P_PIN_CK0_DAT_03_P
G37	PE_E2_P_PIN_CK0_DAT_06_N
G38	PE_E2_P_PIN_CK0_DAT_06_P
G39	GND
G40	GND
G41	PE_PIN_P_E0_CK0_DAT_00_P
G42	PE_PIN_P_E0_CK0_DAT_01_N
G43	GND
G44	GND
G45	PE_E0_P_PIN_CK1_DAT_02_N
G46	PE_E0_P_PIN_CK1_DAT_05_N
G47	PE_E0_P_PIN_CK1_DAT_04_N
G48	PE_E0_P_PIN_CK1_DAT_03_N
H01	GND
H02	NX_PIN_P_X1_CK3_DAT_02
H03	NX_PIN_P_X1_CK3_DAT_05
H04	GND
H05	GND
H06	NX_PIN_P_X1_CK3_DAT_10
H07	GND
H08	TS_PIN_P_CT_JTAG_TMS
H09	GND
H10	MM_M0_P_PIN_CKD_DAT_02_P
H11	MM_M0_P_PIN_CKD_DAT_02_N
H12	MM_M0_P_PIN_CKD_DAT_00_P

Position	Net Name
H13	MM_M0_P_PIN_CKD_DAT_00_N
H14	GND
H15	MM_M0_P_PIN_CKC_DAT_02_P
H16	MM_M0_P_PIN_CKC_DAT_02_N
H17	MM_M0_P_PIN_CKC_DAT_01_P
H18	MM_M0_P_PIN_CKC_DAT_01_N
H19	GND
H20	GND
H21	MM_PIN_P_M0_CKD_DAT_00_P
H22	MM_PIN_P_M0_CKD_DAT_00_N
H23	MM_PIN_P_M0_CKD_DAT_01_P
H24	MM_PIN_P_M0_CKD_DAT_01_N
H25	GND
H26	MM_PIN_P_M0_CKC_DAT_01_P
H27	MM_PIN_P_M0_CKC_DAT_01_N
H28	GND
H29	MM_PIN_P_M0_CKC_DAT_23_N
H30	MM_PIN_P_M0_CKC_DAT_23_P
H31	GND
H32	PV_CT_P_PIN_SPIADC_CS0
H33	GND
H34	PV_CT_P_PIN_SPIADC_SCLK
H35	GND
H36	PE_E2_P_PIN_CK0_DAT_02_N
H37	PE_E2_P_PIN_CK0_DAT_02_P
H38	PE_E2_P_PIN_CK0_DAT_04_P
H39	PE_E2_P_PIN_CK0_DAT_04_N
H40	GND
H41	PE_PIN_P_E0_CK0_DAT_02_N
H42	PE_PIN_P_E0_CK0_DAT_01_P
H43	PE_PIN_P_E0_CK0_DAT_03_N
H44	GND
H45	GND
H46	PE_E0_P_PIN_CK1_DAT_05_P
H47	PE_E0_P_PIN_CK1_DAT_06_N
H48	PE_E0_P_PIN_CK1_DAT_03_P
J01	NX_PIN_P_X1_CK2_DAT_01
J02	GND

Position	Net Name
J03	NX_PIN_P_X1_CK3_DAT_04
J04	NX_PIN_P_X1_CK3_DAT_07
J05	GND
J06	NX_PIN_P_X1_CK3_DAT_11
J07	NX_PIN_P_X1_CK3_DAT_12
J08	GND
J09	TS_PIN_P_CT_EXT_TRIGGER_TCK
J10	GND
J11	GND
J12	GND
J13	GND
J14	GND
J15	GND
J16	TS_CT_P_PIN_PROBE1_P
J17	TS_CT_P_PIN_PROBE1_N
J18	GND
J19	PV_PIN_P_CT_M0_TERMREF_P
J20	PV_PIN_P_CT_M0_TERMREF_N
J21	GND
J22	TS_CT_P_PIN_M0_T_PLLHFC_MKERF_P
J23	TS_CT_P_PIN_M0_T_PLLHFC_MKERF_N
J24	GND
J25	TS_CT_P_PIN_M0_PLL_ANATST
J26	GND
J27	TS_CT_P_PIN_M0_C_MKERF_N
J28	TS_CT_P_PIN_M0_C_MKERF_P
J29	PV_CT_P_PIN_SPIVID0_CS
J30	PV_PIN_P_CT_SPIVID0_MISO
J31	GND
J32	PV_CT_P_PIN_SPIADC_MOSI
J33	PV_CT_P_PIN_SPIADC_CS1
J34	GND
J35	PV_PIN_P_CT_SPIADC_MISO
J36	GND
J37	PE_E2_P_PIN_CK0_DAT_01_N
J38	PE_E2_P_PIN_CK0_DAT_01_P
J39	GND

Position	Net Name
J40	GND
J41	PE_PIN_P_E0_CK0_DAT_02_P
J42	PE_PIN_P_E0_CK0_DAT_04_P
J43	PE_PIN_P_E0_CK0_DAT_03_P
J44	PE_PIN_P_E0_CK0_DAT_05_N
J45	GND
J46	GND
J47	PE_E0_P_PIN_CK1_DAT_06_P
J48	PE_E0_P_PIN_CK1_DAT_07_N
K01	NX_PIN_P_X1_CK2_DAT_00
K02	NX_PIN_P_X1_CK2_DAT_03
K03	GND
K04	NX_PIN_P_X1_CK3_DAT_06
K05	NX_PIN_P_X1_CK3_DAT_09
K06	GND
K07	NX_PIN_P_X1_CK3_DAT_13
K08	NX_PIN_P_X1_CK3_DAT_14
K09	GND
K10	GND
K11	MM_CT_P_PIN_MB_MEM_REFCLK2_N
K12	MM_CT_P_PIN_MB_MEM_REFCLK2_P
K13	VIO_1P10
K14	GND
K15	VIO_1P10
K16	GND
K17	VIO_1P10
K18	GND
K19	VIO_1P10
K20	GND
K21	VIO_1P10
K22	GND
K23	VIO_1P10
K24	GND
K25	VIO_1P10
K26	GND
K27	VIO_1P10
K28	GND

Position	Net Name
K29	VIO_1P10
K30	GND
K31	VIO_1P10
K32	GND
K33	VIO_1P10
K34	GND
K35	VPCI_1P20
K36	GND
K37	PV_PIN_P_CT_E2_TERMREF_P
K38	PE_E2_P_PIN_CK0_DAT_00_N
K39	PE_E2_P_PIN_CK0_DAT_00_P
K40	GND
K41	GND
K42	PE_PIN_P_E0_CK0_DAT_04_N
K43	PE_PIN_P_E0_CK0_DAT_06_N
K44	PE_PIN_P_E0_CK0_DAT_05_P
K45	PE_PIN_P_E0_CK0_DAT_07_N
K46	GND
K47	GND
K48	PE_E0_P_PIN_CK1_DAT_07_P
L01	GND
L02	NX_PIN_P_X1_CK2_DAT_02
L03	NX_PIN_P_X1_CK2_DAT_05
L04	GND
L05	NX_PIN_P_X1_CK3_DAT_08
L06	NX_PIN_P_X1_CK3_CLK_P
L07	GND
L08	NX_PIN_P_X1_CK3_DAT_15
L09	NX_PIN_P_X1_CK3_DAT_16
L10	GND
L11	GND
L12	MM_CT_P_PIN_MB_MEM_ REFCLK3_N
L13	MM_CT_P_PIN_MB_MEM_ REFCLK3_P
L14	VIO_1P10
L15	GND
L16	VIO_1P10
L17	GND

Position	Net Name
L18	VIO_1P10
L19	GND
L20	VIO_1P10
L21	GND
L22	VIO_1P10
L23	GND
L24	VIO_1P10
L25	GND
L26	VIO_1P10
L27	GND
L28	VIO_1P10
L29	GND
L30	VIO_1P10
L31	GND
L32	VIO_1P10
L33	GND
L34	VIO_1P10
L35	VPCI_1P20
L36	VPCI_1P20
L37	PV_PIN_P_CT_E2_TERMREF_N
L38	GND
L39	GND
L40	GND
L41	GND
L42	GND
L43	PE_PIN_P_E0_CK0_DAT_06_P
L44	PE_PIN_P_E0_CK1_DAT_00_N
L45	PE_PIN_P_E0_CK0_DAT_07_P
L46	PE_PIN_P_E0_CK1_DAT_01_P
L47	GND
L48	GND
M01	NX_PIN_P_X1_CK0_CLK_P
M02	GND
M03	NX_PIN_P_X1_CK2_DAT_04
M04	NX_PIN_P_X1_CK2_DAT_07
M05	GND
M06	NX_PIN_P_X1_CK3_CLK_N
M07	NX_PIN_P_X1_CK2_DAT_11

Position	Net Name
M08	GND
M09	NX_PIN_P_X1_CK3_DAT_17
M10	NX_PIN_P_X1_CK3_DAT_18
M11	GND
M12	GND
M13	VIO_1P10
M14	GND
M15	VDD_0P89
M16	GND
M17	VDD_0P89
M18	GND
M19	VDD_0P89
M20	TS_CT_P_PIN_VCSCORE0_VSEN SE
M21	VDD_0P89
M22	GND
M23	VDD_0P89
M24	TS_CT_P_PIN_GDECO0_GSENSE
M25	VIO_1P10
M26	GND
M27	VDD_0P89
M28	GND
M29	VDD_0P89
M30	GND
M31	VDD_0P89
M32	GND
M33	VDD_0P89
M34	GND
M35	VIO_1P10
M36	VPCI_1P20
M37	GND
M38	TS_CT_P_PIN_PE0_PLL_ANATST
M39	GND
M40	GND
M41	NV_PIN_P_V0_CK0_DAT_15_N
M42	GND
M43	GND
M44	PE_PIN_P_E0_CK1_DAT_00_P
M45	PE_PIN_P_E0_CK1_DAT_02_N

Position	Net Name
M46	PE_PIN_P_E0_CK1_DAT_01_N
M47	PE_PIN_P_E0_CK1_DAT_03_N
M48	GND
N01	NX_PIN_P_X1_CK0_CLK_N
N02	NX_PIN_P_X1_CK0_DAT_11
N03	GND
N04	NX_PIN_P_X1_CK2_DAT_06
N05	NX_PIN_P_X1_CK1_DAT_19
N06	GND
N07	NX_PIN_P_X1_CK2_DAT_10
N08	NX_PIN_P_X1_CK2_DAT_13
N09	GND
N10	NX_PIN_P_X1_CK3_DAT_19
N11	GND
N12	MM_CT_P_PIN_MB_NEST_ REFCLK3_P
N13	GND
N14	VDD_0P89
N15	GND
N16	VDD_0P89
N17	GND
N18	TS_CT_P_PIN_DTS2_MONI
N19	VCS_0P97
N20	TS_CT_P_PIN_GDSCORE0_ GSENSE
N21	GND
N22	VCS_0P97
N23	TS_CT_P_PIN_VDDECO0_ VSENSE
N24	TS_CT_P_PIN_VCSECO0_ VSENSE
N25	GND
N26	VDD_0P89
N27	VCS_0P97
N28	VDD_0P89
N29	GND
N30	VCS_0P97
N31	GND
N32	VDD_0P89
N33	GND

Position	Net Name
N34	VDD_0P89
N35	VPCI_1P20
N36	GND
N37	PV_PIN_P_CT_E0_TERMREF_P
N38	TS_CT_P_PIN_PE2_PLL_ANATST
N39	GND
N40	GND
N41	NV_PIN_P_V0_CK0_DAT_15_P
N42	NV_PIN_P_V0_CK0_DAT_13_N
N43	GND
N44	GND
N45	PE_PIN_P_E0_CK1_DAT_02_P
N46	PE_PIN_P_E0_CK1_DAT_04_P
N47	PE_PIN_P_E0_CK1_DAT_03_P
N48	PE_PIN_P_E0_CK1_DAT_05_N
P01	GND
P02	NX_PIN_P_X1_CK0_DAT_10
P03	NX_PIN_P_X1_CK1_DAT_15
P04	GND
P05	NX_PIN_P_X1_CK1_DAT_18
P06	NX_PIN_P_X1_CK1_DAT_17
P07	GND
P08	NX_PIN_P_X1_CK2_DAT_12
P09	NX_PIN_P_X1_CK2_DAT_15
P10	GND
P11	GND
P12	MM_CT_P_PIN_MB_NEST_ REFCLK3_N
P13	MM_CT_P_PIN_MB_NEST_ REFCLK2_P
P14	GND
P15	VDD_0P89
P16	GND
P17	VDD_0P89
P18	GND
P19	VDD_0P89
P20	GND
P21	VDD_0P89
P22	GND

Position	Net Name
P23	VDD_0P89
P24	VIO_1P10
P25	VDD_0P89
P26	GND
P27	VDD_0P89
P28	GND
P29	VDD_0P89
P30	GND
P31	VDD_0P89
P32	GND
P33	VDD_0P89
P34	GND
P35	VIO_1P10
P36	VPCI_1P20
P37	PV_PIN_P_CT_E0_TERMREF_N
P38	TS_CT_P_PIN_NV0_MKERF_P
P39	TS_CT_P_PIN_NV0_PLL_ANATST
P40	GND
P41	GND
P42	NV_PIN_P_V0_CK0_DAT_13_P
P43	NV_PIN_P_V0_CK0_DAT_11_N
P44	GND
P45	GND
P46	PE_PIN_P_E0_CK1_DAT_04_N
P47	PE_PIN_P_E0_CK1_DAT_06_N
P48	PE_PIN_P_E0_CK1_DAT_05_P
R01	NX_PIN_P_X1_CK0_DAT_05
R02	GND
R03	NX_PIN_P_X1_CK1_DAT_14
R04	NX_PIN_P_X1_CK1_DAT_13
R05	GND
R06	NX_PIN_P_X1_CK1_DAT_16
R07	NX_PIN_P_X1_CK1_CLK_P
R08	GND
R09	NX_PIN_P_X1_CK2_DAT_14
R10	NX_PIN_P_X1_CK2_DAT_18
R11	GND
R12	GND

Position	Net Name
R13	MM_CT_P_PIN_MB_NEST_ REFCLK2_N
R14	TS_CT_P_PIN_VDDCORE0_ VSENSE
R15	GND
R16	VDD_0P89
R17	GND
R18	VDD_0P89
R19	VCS_0P97
R20	VDD_0P89
R21	GND
R22	VCS_0P97
R23	GND
R24	VDD_0P89
R25	GND
R26	VDD_0P89
R27	VCS_0P97
R28	VDD_0P89
R29	GND
R30	VCS_0P97
R31	GND
R32	VDD_0P89
R33	GND
R34	VDD_0P89
R35	VPCI_1P20
R36	GND
R37	PV_PIN_P_CT_NV0_TERMREF_P
R38	TS_CT_P_PIN_NV0_MKERF_N
R39	TS_CT_P_PIN_NV0_PLL_HFC_N
R40	GND
R41	NV_PIN_P_V0_CK0_DAT_14_P
R42	GND
R43	NV_PIN_P_V0_CK0_DAT_11_P
R44	NV_PIN_P_V0_CK0_DAT_10_N
R45	GND
R46	GND
R47	PE_PIN_P_E0_CK1_DAT_06_P
R48	PE_PIN_P_E0_CK1_DAT_07_N
T01	NX_PIN_P_X1_CK0_DAT_04

Position	Net Name
T02	NX_PIN_P_X1_CK0_DAT_07
T03	GND
T04	NX_PIN_P_X1_CK1_DAT_12
T05	NX_PIN_P_X1_CK1_DAT_11
T06	GND
T07	NX_PIN_P_X1_CK1_CLK_N
T08	NX_PIN_P_X1_CK2_DAT_09
T09	GND
T10	NX_PIN_P_X1_CK2_DAT_19
T11	GND
T12	GND
T13	VIO_1P10
T14	TS_CT_P_PIN_GDDCORE0_ GSENSE
T15	VDD_0P89
T16	GND
T17	VDD_0P89
T18	GND
T19	VDD_0P89
T20	GND
T21	VDD_0P89
T22	GND
T23	VDD_0P89
T24	TS_CT_P_PIN_EX0_GSENSE
T25	VIO_1P10
T26	GND
T27	VDD_0P89
T28	GND
T29	VDD_0P89
T30	GND
T31	VDD_0P89
T32	GND
T33	VDD_0P89
T34	GND
T35	VIO_1P10
T36	VPCI_1P20
T37	PV_PIN_P_CT_NV0_TERMREF_N
T38	GND
T39	TS_CT_P_PIN_NV0_PLL_HFC_P

Position	Net Name
T40	GND
T41	NV_PIN_P_V0_CK0_DAT_14_N
T42	NV_PIN_P_V0_CK0_DAT_12_N
T43	GND
T44	NV_PIN_P_V0_CK0_DAT_10_P
T45	NV_PIN_P_V0_CK0_DAT_09_N
T46	GND
T47	GND
T48	PE_PIN_P_E0_CK1_DAT_07_P
U01	GND
U02	NX_PIN_P_X1_CK0_DAT_06
U03	NX_PIN_P_X1_CK0_DAT_09
U04	GND
U05	NX_PIN_P_X1_CK1_DAT_10
U06	NX_PIN_P_X1_CK1_DAT_09
U07	GND
U08	NX_PIN_P_X1_CK2_DAT_08
U09	NX_PIN_P_X1_CK2_CLK_P
U10	GND
U11	GND
U12	PV_PIN_P_CT_OSC0_ TODREFCLK
U13	GND
U14	VDD_0P89
U15	GND
U16	VDD_0P89
U17	GND
U18	VDD_0P89
U19	GND
U20	VDD_0P89
U21	GND
U22	VDD_0P89
U23	TS_CT_P_PIN_VCSEX0_VSENSE
U24	TS_CT_P_PIN_VDDEX0_VSENSE
U25	GND
U26	VDD_0P89
U27	GND
U28	VDD_0P89
U29	GND

Position	Net Name
U30	VDD_0P89
U31	GND
U32	VDD_0P89
U33	GND
U34	VDD_0P89
U35	GND
U36	VPCI_1P20
U37	GND
U38	GND
U39	GND
U40	GND
U41	GND
U42	NV_PIN_P_V0_CK0_DAT_12_P
U43	NV_PIN_P_V0_CK0_DAT_00_N
U44	GND
U45	NV_PIN_P_V0_CK0_DAT_09_P
U46	NV_PIN_P_V0_CK0_DAT_08_N
U47	GND
U48	GND
V01	GND
V02	GND
V03	NX_PIN_P_X1_CK0_DAT_08
V04	NX_PIN_P_X1_CK0_DAT_13
V05	GND
V06	NX_PIN_P_X1_CK1_DAT_08
V07	NX_PIN_P_X1_CK1_DAT_07
V08	GND
V09	NX_PIN_P_X1_CK2_CLK_N
V10	NX_PIN_P_X1_CK2_DAT_17
V11	GND
V12	GND
V13	VIO_1P10
V14	GND
V15	VDD_0P89
V16	GND
V17	VDD_0P89
V18	GND
V19	VCS_0P97

Position	Net Name
V20	GND
V21	VDD_0P89
V22	VCS_0P97
V23	VDD_0P89
V24	VIO_1P10
V25	VDD_0P89
V26	GND
V27	VCS_0P97
V28	GND
V29	VDD_0P89
V30	VCS_0P97
V31	VDD_0P89
V32	GND
V33	VDD_0P89
V34	GND
V35	VPCI_1P20
V36	GND
V37	PV_CT_P_PIN_MB_NV_REFCLK_P
V38	PV_CT_P_PIN_MB_NV_REFCLK_N
V39	GND
V40	NV_V0_P_PIN_CK0_DAT_14_N
V41	GND
V42	GND
V43	NV_PIN_P_V0_CK0_DAT_00_P
V44	NV_PIN_P_V0_CK0_DAT_01_P
V45	GND
V46	NV_PIN_P_V0_CK0_DAT_08_P
V47	NV_PIN_P_V0_CK0_DAT_07_P
V48	GND
W01	NX_X1_P_PIN_CK0_DAT_01
W02	GND
W03	GND
W04	NX_PIN_P_X1_CK0_DAT_12
W05	NX_PIN_P_X1_CK0_DAT_15
W06	GND
W07	NX_PIN_P_X1_CK1_DAT_06
W08	NX_PIN_P_X1_CK1_DAT_05

Position	Net Name
W09	GND
W10	NX_PIN_P_X1_CK2_DAT_16
W11	GND
W12	PV_PIN_P_CT_OSC0_C1_REFCLK_P
W13	GND
W14	VDD_0P89
W15	GND
W16	VDD_0P89
W17	GND
W18	VDD_0P89
W19	GND
W20	VDD_0P89
W21	GND
W22	VDD_0P89
W23	GND
W24	VDD_0P89
W25	GND
W26	VDD_0P89
W27	GND
W28	VDD_0P89
W29	GND
W30	VDD_0P89
W31	GND
W32	VDD_0P89
W33	GND
W34	VDD_0P89
W35	VIO_1P10
W36	GND
W37	GND
W38	GND
W39	GND
W40	NV_V0_P_PIN_CK0_DAT_14_P
W41	NV_V0_P_PIN_CK0_DAT_12_P
W42	GND
W43	GND
W44	NV_PIN_P_V0_CK0_DAT_01_N
W45	NV_PIN_P_V0_CK0_DAT_06_N
W46	GND

Position	Net Name
W47	NV_PIN_P_V0_CK0_DAT_07_N
W48	NV_PIN_P_V0_CK0_DAT_05_P
Y01	GND
Y02	NX_X1_P_PIN_CK0_DAT_02
Y03	GND
Y04	GND
Y05	NX_PIN_P_X1_CK0_DAT_14
Y06	NX_PIN_P_X1_CK0_DAT_17
Y07	GND
Y08	NX_PIN_P_X1_CK1_DAT_04
Y09	NX_PIN_P_X1_CK1_DAT_03
Y10	GND
Y11	GND
Y12	PV_PIN_P_CT_OSC0_C1_ REFCLK_N
Y13	VIO_1P10
Y14	GND
Y15	VDD_0P89
Y16	GND
Y17	VDD_0P89
Y18	GND
Y19	VCS_0P97
Y20	GND
Y21	VDD_0P89
Y22	VCS_0P97
Y23	VDD_0P89
Y24	GND
Y25	VIO_1P10
Y26	GND
Y27	VCS_0P97
Y28	GND
Y29	VDD_0P89
Y30	VCS_0P97
Y31	VDD_0P89
Y32	GND
Y33	VDD_0P89
Y34	GND
Y35	GND

Position	Net Name
Y36	PV_PIN_P_CT_OSC0_E_REFCLK_ N
Y37	PV_PIN_P_CT_OSC0_E_REFCLK_ P
Y38	GND
Y39	NV_V0_P_PIN_CK0_DAT_15_P
Y40	GND
Y41	NV_V0_P_PIN_CK0_DAT_12_N
Y42	NV_V0_P_PIN_CK0_DAT_10_P
Y43	GND
Y44	GND
Y45	NV_PIN_P_V0_CK0_DAT_06_P
Y46	NV_PIN_P_V0_CK0_DAT_04_N
Y47	GND
Y48	NV_PIN_P_V0_CK0_DAT_05_N
AA01	NX_X1_P_PIN_CK0_DAT_04
AA02	GND
AA03	NX_X1_P_PIN_CK0_DAT_03
AA04	GND
AA05	GND
AA06	NX_PIN_P_X1_CK0_DAT_16
AA07	NX_PIN_P_X1_CK0_DAT_19
AA08	GND
AA09	NX_PIN_P_X1_CK1_DAT_02
AA10	NX_PIN_P_X1_CK1_DAT_01
AA11	GND
AA12	GND
AA13	GND
AA14	VDD_0P89
AA15	GND
AA16	VDD_0P89
AA17	GND
AA18	VDD_0P89
AA19	GND
AA20	VDD_0P89
AA21	GND
AA22	VDD_0P89
AA23	GND
AA24	VDD_0P89

Position	Net Name
AA25	GND
AA26	VDD_0P89
AA27	GND
AA28	VDD_0P89
AA29	GND
AA30	VDD_0P89
AA31	GND
AA32	VDD_0P89
AA33	GND
AA34	VDD_0P89
AA35	VIO_1P10
AA36	GND
AA37	GND
AA38	GND
AA39	NV_V0_P_PIN_CK0_DAT_15_N
AA40	NV_V0_P_PIN_CK0_DAT_13_P
AA41	GND
AA42	NV_V0_P_PIN_CK0_DAT_10_N
AA43	NV_V0_P_PIN_CK0_DAT_08_N
AA44	GND
AA45	GND
AA46	NV_PIN_P_V0_CK0_DAT_04_P
AA47	NV_PIN_P_V0_CK0_DAT_03_P
AA48	GND
AB01	GND
AB02	NX_X1_P_PIN_CK0_DAT_06
AB03	GND
AB04	NX_X1_P_PIN_CK0_DAT_05
AB05	GND
AB06	GND
AB07	NX_PIN_P_X1_CK0_DAT_18
AB08	NX_PIN_P_X1_CK0_DAT_03
AB09	GND
AB10	NX_PIN_P_X1_CK1_DAT_00
AB11	GND
AB12	DVDD_1P50
AB13	DVDD_1P50
AB14	GND

Position	Net Name
AB15	VDD_0P89
AB16	GND
AB17	VDD_0P89
AB18	GND
AB19	VCS_0P97
AB20	GND
AB21	VDD_0P89
AB22	VCS_0P97
AB23	VDD_0P89
AB24	VIO_1P10
AB25	TS_CT_P_PIN_PFAMX_VSENSE
AB26	GND
AB27	VCS_0P97
AB28	GND
AB29	VDD_0P89
AB30	VCS_0P97
AB31	VDD_0P89
AB32	GND
AB33	VDD_0P89
AB34	GND
AB35	GND
AB36	PE_CT_P_PIN_E2_SLOT_CLK0_N
AB37	GND
AB38	GND
AB39	GND
AB40	NV_V0_P_PIN_CK0_DAT_13_N
AB41	NV_V0_P_PIN_CK0_DAT_11_P
AB42	GND
AB43	NV_V0_P_PIN_CK0_DAT_08_P
AB44	NV_V0_P_PIN_CK0_DAT_06_P
AB45	GND
AB46	GND
AB47	NV_PIN_P_V0_CK0_DAT_03_N
AB48	NV_PIN_P_V0_CK0_DAT_02_N
AC01	NX_X1_P_PIN_CK0_DAT_07
AC02	GND
AC03	NX_X1_P_PIN_CK0_DAT_08
AC04	GND

Position	Net Name
AC05	NX_X1_P_PIN_CK0_DAT_00
AC06	GND
AC07	GND
AC08	NX_PIN_P_X1_CK0_DAT_02
AC09	NX_PIN_P_X1_CK0_DAT_01
AC10	GND
AC11	GND
AC12	AVDD_1P50
AC13	AVDD_1P50
AC14	VDD_0P89
AC15	GND
AC16	VDD_0P89
AC17	GND
AC18	VDD_0P89
AC19	GND
AC20	VDD_0P89
AC21	GND
AC22	VDD_0P89
AC23	GND
AC24	TS_CT_P_PIN_VCAL
AC25	TS_CT_P_PIN_PFAMX_GSENSE
AC26	VDD_0P89
AC27	GND
AC28	VDD_0P89
AC29	GND
AC30	VDD_0P89
AC31	GND
AC32	VDD_0P89
AC33	GND
AC34	VDD_0P89
AC35	VIO_1P10
AC36	PE_CT_P_PIN_E2_SLOT_CLK0_P
AC37	PE_CT_P_PIN_E0_SLOT_CLK0_P
AC38	GND
AC39	NV_V1_P_PIN_CK0_DAT_00_P
AC40	GND
AC41	NV_V0_P_PIN_CK0_DAT_11_N
AC42	NV_V0_P_PIN_CK0_DAT_09_N

Position	Net Name
AC43	GND
AC44	NV_V0_P_PIN_CK0_DAT_06_N
AC45	NV_V0_P_PIN_CK0_DAT_02_N
AC46	GND
AC47	GND
AC48	NV_PIN_P_V0_CK0_DAT_02_P
AD01	GND
AD02	NX_X1_P_PIN_CK0_DAT_09
AD03	GND
AD04	NX_X1_P_PIN_CK0_DAT_10
AD05	GND
AD06	NX_X1_P_PIN_CK0_DAT_17
AD07	GND
AD08	GND
AD09	NX_PIN_P_X1_CK0_DAT_00
AD10	GND
AD11	GND
AD12	GND
AD13	VIO_1P10
AD14	VIO_1P10
AD15	VDD_0P89
AD16	GND
AD17	PV_MSOP_M_CT_VREF_P
AD18	VIO_1P10
AD19	VDD_0P89
AD20	GND
AD21	VDD_0P89
AD22	VIO_1P10
AD23	VDD_0P89
AD24	GND
AD25	VIO_1P10
AD26	GND
AD27	VDD_0P89
AD28	GND
AD29	VIO_1P10
AD30	GND
AD31	VDD_0P89
AD32	GND

Position	Net Name
AD33	VIO_1P10
AD34	GND
AD35	GND
AD36	VIO_1P10
AD37	PE_CT_P_PIN_E0_SLOT_CLK0_N
AD38	GND
AD39	NV_V1_P_PIN_CK0_DAT_00_N
AD40	NV_V1_P_PIN_CK0_DAT_01_P
AD41	GND
AD42	NV_V0_P_PIN_CK0_DAT_09_P
AD43	NV_V0_P_PIN_CK0_DAT_07_P
AD44	GND
AD45	NV_V0_P_PIN_CK0_DAT_02_P
AD46	NV_V0_P_PIN_CK0_DAT_04_N
AD47	GND
AD48	GND
AE01	NX_X1_P_PIN_CK0_CLK_N
AE02	GND
AE03	NX_X1_P_PIN_CK0_DAT_12
AE04	GND
AE05	NX_X1_P_PIN_CK0_DAT_15
AE06	GND
AE07	NX_X1_P_PIN_CK0_DAT_19
AE08	GND
AE09	GND
AE10	PV_CT_M_PIN_SEEPROM1_DATA
AE11	TS_CT_P_PIN_PXFM_PLL_ ANATST
AE12	TS_CT_P_PIN_PXFM_PLL_HFC_P
AE13	TS_CT_P_PIN_PXFM_PLL_HFC_N
AE14	VDD_0P89
AE15	GND
AE16	VIO_1P10
AE17	PV_MSOP_M_CT_VREF_N
AE18	VDD_0P89
AE19	GND
AE20	VIO_1P10
AE21	GND
AE22	VDD_0P89

Position	Net Name
AE23	GND
AE24	VIO_1P10
AE25	GND
AE26	VDD_0P89
AE27	VIO_1P10
AE28	VDD_0P89
AE29	GND
AE30	VDD_0P89
AE31	VIO_1P10
AE32	VDD_0P89
AE33	GND
AE34	VDD_0P89
AE35	VIO_1P10
AE36	GND
AE37	GND
AE38	GND
AE39	GND
AE40	NV_V1_P_PIN_CK0_DAT_01_N
AE41	NV_V1_P_PIN_CK0_DAT_02_N
AE42	GND
AE43	NV_V0_P_PIN_CK0_DAT_07_N
AE44	NV_V1_P_PIN_CK0_DAT_06_N
AE45	GND
AE46	NV_V0_P_PIN_CK0_DAT_04_P
AE47	NV_V0_P_PIN_CK0_DAT_05_P
AE48	GND
AF01	GND
AF02	NX_X1_P_PIN_CK0_CLK_P
AF03	GND
AF04	NX_X1_P_PIN_CK0_DAT_14
AF05	GND
AF06	NX_X1_P_PIN_CK0_DAT_18
AF07	GND
AF08	GND
AF09	VSB_3P30
AF10	PV_CT_M_PIN_SEEPROM1_CLK
AF11	GND
AF12	GND

Position	Net Name
AF13	VIO_1P10
AF14	GND
AF15	VDD_0P89
AF16	GND
AF17	VDD_0P89
AF18	GND
AF19	VDD_0P89
AF20	GND
AF21	VDD_0P89
AF22	GND
AF23	VDD_0P89
AF24	GND
AF25	VDD_0P89
AF26	GND
AF27	VDD_0P89
AF28	GND
AF29	VDD_0P89
AF30	GND
AF31	VDD_0P89
AF32	GND
AF33	VDD_0P89
AF34	GND
AF35	GND
AF36	VIO_1P10
AF37	PE_CT_P_PIN_E1_SLOT_CLK0_P
AF38	GND
AF39	GND
AF40	GND
AF41	NV_V1_P_PIN_CK0_DAT_02_P
AF42	NV_V1_P_PIN_CK0_DAT_03_N
AF43	GND
AF44	NV_V1_P_PIN_CK0_DAT_06_P
AF45	NV_V1_P_PIN_CK0_DAT_09_P
AF46	GND
AF47	NV_V0_P_PIN_CK0_DAT_05_N
AF48	NV_V0_P_PIN_CK0_DAT_03_N
AG01	NX_X1_P_PIN_CK0_DAT_11
AG02	GND

Position	Net Name
AG03	NX_X1_P_PIN_CK1_DAT_04
AG04	GND
AG05	NX_X1_P_PIN_CK0_DAT_16
AG06	GND
AG07	NX_X1_P_PIN_CK1_DAT_01
AG08	GND
AG09	VSB_3P30
AG10	PV_CT_M_PIN_SEEPROM0_CLK
AG11	GND
AG12	PV_CT_P_PIN_PSI_CLK_N
AG13	PV_CT_P_PIN_PSI_CLK_P
AG14	VDD_0P89
AG15	GND
AG16	VDD_0P89
AG17	GND
AG18	VDD_0P89
AG19	VCS_0P97
AG20	VDD_0P89
AG21	GND
AG22	VCS_0P97
AG23	GND
AG24	VDD_0P89
AG25	VIO_1P10
AG26	VDD_0P89
AG27	VCS_0P97
AG28	VDD_0P89
AG29	GND
AG30	VCS_0P97
AG31	GND
AG32	VDD_0P89
AG33	GND
AG34	VDD_0P89
AG35	VIO_1P10
AG36	GND
AG37	PE_CT_P_PIN_E1_SLOT_CLK0_N
AG38	GND
AG39	NV_PIN_P_V1_CK0_DAT_08_P
AG40	GND

Position	Net Name
AG41	GND
AG42	NV_V1_P_PIN_CK0_DAT_03_P
AG43	NV_V1_P_PIN_CK0_DAT_04_N
AG44	GND
AG45	NV_V1_P_PIN_CK0_DAT_09_N
AG46	NV_V1_P_PIN_CK0_DAT_08_P
AG47	GND
AG48	NV_V0_P_PIN_CK0_DAT_03_P
AH01	GND
AH02	NX_X1_P_PIN_CK0_DAT_13
AH03	GND
AH04	NX_X1_P_PIN_CK1_DAT_06
AH05	GND
AH06	NX_X1_P_PIN_CK1_DAT_05
AH07	GND
AH08	NX_X1_P_PIN_CK1_DAT_02
AH09	GND
AH10	PV_CT_M_PIN_SEEPROM0_DATA
AH11	GND
AH12	PV_CT_P_PIN_PSI_DATA
AH13	VIO_1P10
AH14	GND
AH15	VDD_0P89
AH16	GND
AH17	VDD_0P89
AH18	GND
AH19	VDD_0P89
AH20	GND
AH21	VDD_0P89
AH22	GND
AH23	VDD_0P89
AH24	GND
AH25	VDD_0P89
AH26	GND
AH27	VDD_0P89
AH28	GND
AH29	VDD_0P89
AH30	GND

Position	Net Name
AH31	VDD_0P89
AH32	GND
AH33	VDD_0P89
AH34	GND
AH35	GND
AH36	VIO_1P10
AH37	GND
AH38	GND
AH39	NV_PIN_P_V1_CK0_DAT_08_N
AH40	NV_PIN_P_V1_CK0_DAT_09_P
AH41	GND
AH42	GND
AH43	NV_V1_P_PIN_CK0_DAT_04_P
AH44	NV_V1_P_PIN_CK0_DAT_05_N
AH45	GND
AH46	NV_V1_P_PIN_CK0_DAT_08_N
AH47	NV_V0_P_PIN_CK0_DAT_01_N
AH48	GND
AJ01	NX_X1_P_PIN_CK1_CLK_N
AJ02	GND
AJ03	NX_X1_P_PIN_CK1_DAT_08
AJ04	GND
AJ05	NX_X1_P_PIN_CK1_DAT_07
AJ06	GND
AJ07	NX_X1_P_PIN_CK1_DAT_03
AJ08	GND
AJ09	NX_X1_P_PIN_CK1_DAT_00
AJ10	GND
AJ11	PV_CT_P_PIN_TPM_RESET
AJ12	GND
AJ13	GND
AJ14	VDD_0P89
AJ15	GND
AJ16	VDD_0P89
AJ17	GND
AJ18	VDD_0P89
AJ19	VCS_0P97
AJ20	VDD_0P89

Position	Net Name
AJ21	GND
AJ22	VCS_0P97
AJ23	GND
AJ24	VIO_1P10
AJ25	GND
AJ26	VDD_0P89
AJ27	VCS_0P97
AJ28	VDD_0P89
AJ29	GND
AJ30	VCS_0P97
AJ31	GND
AJ32	VDD_0P89
AJ33	GND
AJ34	VDD_0P89
AJ35	VIO_1P10
AJ36	GND
AJ37	PE_CT_P_PIN_E1_SLOT_CLK1_P
AJ38	GND
AJ39	GND
AJ40	NV_PIN_P_V1_CK0_DAT_09_N
AJ41	NV_PIN_P_V1_CK0_DAT_11_P
AJ42	GND
AJ43	GND
AJ44	NV_V1_P_PIN_CK0_DAT_05_P
AJ45	NV_V1_P_PIN_CK0_DAT_07_N
AJ46	GND
AJ47	NV_V0_P_PIN_CK0_DAT_01_P
AJ48	NV_V0_P_PIN_CK0_DAT_00_N
AK01	GND
AK02	NX_X1_P_PIN_CK1_CLK_P
AK03	GND
AK04	NX_X1_P_PIN_CK1_DAT_10
AK05	GND
AK06	NX_X1_P_PIN_CK1_DAT_09
AK07	GND
AK08	NX_X1_P_PIN_CK2_DAT_19
AK09	GND
AK10	PV_PIN_P_CT_TPM_INTERRUPT

Position	Net Name
AK11	GND
AK12	PV_PIN_P_CT_PSI_DATA
AK13	VIO_1P10
AK14	GND
AK15	VDD_0P89
AK16	GND
AK17	VDD_0P89
AK18	GND
AK19	VDD_0P89
AK20	GND
AK21	VDD_0P89
AK22	GND
AK23	VDD_0P89
AK24	GND
AK25	VDD_0P89
AK26	GND
AK27	VDD_0P89
AK28	GND
AK29	VDD_0P89
AK30	GND
AK31	VDD_0P89
AK32	GND
AK33	VDD_0P89
AK34	GND
AK35	GND
AK36	VIO_1P10
AK37	PE_CT_P_PIN_E1_SLOT_CLK1_N
AK38	GND
AK39	NV_PIN_P_V1_CK0_DAT_10_P
AK40	GND
AK41	NV_PIN_P_V1_CK0_DAT_11_N
AK42	NV_PIN_P_V1_CK0_DAT_12_N
AK43	GND
AK44	GND
AK45	NV_V1_P_PIN_CK0_DAT_07_P
AK46	NV_V1_P_PIN_CK0_DAT_12_P
AK47	GND
AK48	NV_V0_P_PIN_CK0_DAT_00_P

Position	Net Name
AL01	NX_X1_P_PIN_CK1_DAT_11
AL02	GND
AL03	NX_X1_P_PIN_CK1_DAT_12
AL04	GND
AL05	NX_X1_P_PIN_CK1_DAT_15
AL06	GND
AL07	NX_X1_P_PIN_CK2_DAT_15
AL08	GND
AL09	NX_X1_P_PIN_CK2_DAT_18
AL10	GND
AL11	GND
AL12	PV_PIN_P_CT_PSI_CLK_N
AL13	PV_PIN_P_CT_PSI_CLK_P
AL14	VDD_0P89
AL15	GND
AL16	VDD_0P89
AL17	TS_CT_P_PIN_TDIODE_C5
AL18	TS_CT_P_PIN_TDIODE_A5
AL19	VCS_0P97
AL20	VDD_0P89
AL21	GND
AL22	VCS_0P97
AL23	GND
AL24	VDD_0P89
AL25	VIO_1P10
AL26	VDD_0P89
AL27	VCS_0P97
AL28	VDD_0P89
AL29	GND
AL30	VCS_0P97
AL31	TS_CT_P_PIN_TDIODE_A13
AL32	TS_CT_P_PIN_TDIODE_C13
AL33	GND
AL34	VDD_0P89
AL35	VIO_1P10
AL36	GND
AL37	GND
AL38	TS_CT_P_PIN_NV1_MKERF_P

Position	Net Name
AL39	NV_PIN_P_V1_CK0_DAT_10_N
AL40	NV_PIN_P_V1_CK0_DAT_13_N
AL41	GND
AL42	NV_PIN_P_V1_CK0_DAT_12_P
AL43	NV_PIN_P_V1_CK0_DAT_14_N
AL44	GND
AL45	GND
AL46	NV_V1_P_PIN_CK0_DAT_12_N
AL47	NV_V1_P_PIN_CK0_DAT_11_P
AL48	GND
AM01	GND
AM02	NX_X1_P_PIN_CK1_DAT_13
AM03	GND
AM04	NX_X1_P_PIN_CK1_DAT_16
AM05	GND
AM06	NX_X1_P_PIN_CK2_DAT_11
AM07	GND
AM08	NX_X1_P_PIN_CK2_DAT_17
AM09	GND
AM10	NX_X1_P_PIN_CK2_DAT_16
AM11	GND
AM12	GND
AM13	VIO_1P10
AM14	GND
AM15	VDD_0P89
AM16	GND
AM17	VDD_0P89
AM18	GND
AM19	VDD_0P89
AM20	GND
AM21	VDD_0P89
AM22	GND
AM23	VDD_0P89
AM24	GND
AM25	TS_CT_P_PIN_AMX1_GSENSE
AM26	GND
AM27	VDD_0P89
AM28	GND

Position	Net Name
AM29	VDD_0P89
AM30	GND
AM31	VDD_0P89
AM32	GND
AM33	VDD_0P89
AM34	GND
AM35	GND
AM36	VIO_1P10
AM37	PV_PIN_P_CT_NV1_TERMREF_P
AM38	TS_CT_P_PIN_NV1_MKERF_N
AM39	GND
AM40	NV_PIN_P_V1_CK0_DAT_13_P
AM41	NV_PIN_P_V1_CK0_DAT_15_N
AM42	GND
AM43	NV_PIN_P_V1_CK0_DAT_14_P
AM44	NV_PIN_P_V1_CK0_DAT_07_N
AM45	GND
AM46	GND
AM47	NV_V1_P_PIN_CK0_DAT_11_N
AM48	NV_V1_P_PIN_CK0_DAT_10_N
AN01	NX_X1_P_PIN_CK1_DAT_14
AN02	GND
AN03	NX_X1_P_PIN_CK1_DAT_19
AN04	GND
AN05	NX_X1_P_PIN_CK2_DAT_08
AN06	GND
AN07	NX_X1_P_PIN_CK2_DAT_13
AN08	GND
AN09	NX_X1_P_PIN_CK2_DAT_14
AN10	GND
AN11	GND
AN12	MM_CT_P_PIN_MB_NEST_ REFCLK7_P
AN13	GND
AN14	VDD_0P89
AN15	GND
AN16	VDD_0P89
AN17	GND
AN18	VDD_0P89

Position	Net Name
AN19	GND
AN20	VDD_0P89
AN21	GND
AN22	VDD_0P89
AN23	GND
AN24	VIO_1P10
AN25	TS_CT_P_PIN_AMX1_VSENSE
AN26	VDD_0P89
AN27	GND
AN28	VDD_0P89
AN29	GND
AN30	VDD_0P89
AN31	GND
AN32	VDD_0P89
AN33	GND
AN34	VDD_0P89
AN35	VIO_1P10
AN36	VPCI_1P20
AN37	PV_PIN_P_CT_NV1_TERMREF_N
AN38	GND
AN39	GND
AN40	GND
AN41	NV_PIN_P_V1_CK0_DAT_15_P
AN42	NV_PIN_P_V1_CK0_DAT_06_P
AN43	GND
AN44	NV_PIN_P_V1_CK0_DAT_07_P
AN45	GND
AN46	NV_V1_P_PIN_CK0_DAT_15_N
AN47	GND
AN48	NV_V1_P_PIN_CK0_DAT_10_P
AP01	GND
AP02	NX_X1_P_PIN_CK1_DAT_18
AP03	GND
AP04	NX_X1_P_PIN_CK2_DAT_05
AP05	GND
AP06	NX_X1_P_PIN_CK2_DAT_10
AP07	GND
AP08	NX_X1_P_PIN_CK2_DAT_12

Position	Net Name
AP09	GND
AP10	NX_X1_P_PIN_CK3_DAT_00
AP11	GND
AP12	MM_CT_P_PIN_MB_NEST_ REFCLK7_N
AP13	MM_CT_P_PIN_MB_NEST_ REFCLK6_P
AP14	GND
AP15	VDD_0P89
AP16	GND
AP17	VDD_0P89
AP18	GND
AP19	VCS_0P97
AP20	GND
AP21	VDD_0P89
AP22	VCS_0P97
AP23	VDD_0P89
AP24	GND
AP25	TS_PIN_P_CT_EFUSE_FSOURCE
AP26	GND
AP27	VCS_0P97
AP28	GND
AP29	VDD_0P89
AP30	VCS_0P97
AP31	VDD_0P89
AP32	GND
AP33	VDD_0P89
AP34	GND
AP35	VPCI_1P20
AP36	GND
AP37	GND
AP38	PV_CT_B_PIN_PCI_I2C_SDA_B
AP39	TS_CT_P_PIN_NV1_PLL_ANATST
AP40	GND
AP41	GND
AP42	NV_PIN_P_V1_CK0_DAT_06_N
AP43	NV_PIN_P_V1_CK0_DAT_05_N
AP44	GND
AP45	GND

Position	Net Name
AP46	NV_V1_P_PIN_CK0_DAT_15_P
AP47	NV_V1_P_PIN_CK0_DAT_14_N
AP48	GND
AR01	NX_X1_P_PIN_CK1_DAT_17
AR02	GND
AR03	NX_X1_P_PIN_CK2_DAT_02
AR04	GND
AR05	NX_X1_P_PIN_CK2_DAT_09
AR06	GND
AR07	NX_X1_P_PIN_CK2_CLK_P
AR08	GND
AR09	NX_X1_P_PIN_CK3_DAT_02
AR10	GND
AR11	TS_PIN_P_CT_TST_FORCE_PWR _ON
AR12	GND
AR13	MM_CT_P_PIN_MB_NEST_ REFCLK6_N
AR14	VDD_0P89
AR15	GND
AR16	VDD_0P89
AR17	GND
AR18	VDD_0P89
AR19	GND
AR20	VDD_0P89
AR21	GND
AR22	VDD_0P89
AR23	GND
AR24	VDD_0P89
AR25	VIO_1P10
AR26	VDD_0P89
AR27	GND
AR28	VDD_0P89
AR29	GND
AR30	VDD_0P89
AR31	GND
AR32	VDD_0P89
AR33	GND
AR34	VDD_0P89

Position	Net Name
AR35	VIO_1P10
AR36	VPCI_1P20
AR37	TS_CT_P_PIN_NV1_PLL_HFC_P
AR38	PV_CT_B_PIN_PCI_I2C_SCL_B
AR39	GND
AR40	PE_PIN_P_E1_CK0_DAT_01_P
AR41	GND
AR42	GND
AR43	NV_PIN_P_V1_CK0_DAT_05_P
AR44	NV_PIN_P_V1_CK0_DAT_04_P
AR45	GND
AR46	GND
AR47	NV_V1_P_PIN_CK0_DAT_14_P
AR48	NV_V1_P_PIN_CK0_DAT_13_N
AT01	GND
AT02	NX_X1_P_PIN_CK2_DAT_01
AT03	GND
AT04	NX_X1_P_PIN_CK2_DAT_06
AT05	GND
AT06	NX_X1_P_PIN_CK2_CLK_N
AT07	GND
AT08	NX_X1_P_PIN_CK3_DAT_03
AT09	GND
AT10	NX_X1_P_PIN_CK3_DAT_01
AT11	GND
AT12	MM_CT_P_PIN_MB_MEM_ REFCLK7_N
AT13	VIO_1P10
AT14	GND
AT15	VDD_0P89
AT16	GND
AT17	VDD_0P89
AT18	GND
AT19	VCS_0P97
AT20	GND
AT21	VDD_0P89
AT22	VCS_0P97
AT23	VDD_0P89
AT24	GND

Position	Net Name
AT25	VDD_0P89
AT26	GND
AT27	VCS_0P97
AT28	GND
AT29	VDD_0P89
AT30	VCS_0P97
AT31	VDD_0P89
AT32	GND
AT33	VDD_0P89
AT34	GND
AT35	VPCI_1P20
AT36	GND
AT37	TS_CT_P_PIN_NV1_PLL_HFC_N
AT38	GND
AT39	GND
AT40	PE_PIN_P_E1_CK0_DAT_01_N
AT41	PE_PIN_P_E1_CK0_DAT_03_P
AT42	GND
AT43	GND
AT44	NV_PIN_P_V1_CK0_DAT_04_N
AT45	NV_PIN_P_V1_CK0_DAT_03_N
AT46	GND
AT47	GND
AT48	NV_V1_P_PIN_CK0_DAT_13_P
AU01	NX_X1_P_PIN_CK2_DAT_00
AU02	GND
AU03	NX_X1_P_PIN_CK2_DAT_04
AU04	GND
AU05	NX_X1_P_PIN_CK2_DAT_07
AU06	GND
AU07	NX_X1_P_PIN_CK3_DAT_04
AU08	GND
AU09	GND
AU10	GND
AU11	GND
AU12	MM_CT_P_PIN_MB_MEM_ REFCLK7_P
AU13	MM_CT_P_PIN_MB_MEM_ REFCLK6_P

Position	Net Name
AU14	VDD_0P89
AU15	GND
AU16	VDD_0P89
AU17	GND
AU18	VDD_0P89
AU19	GND
AU20	VDD_0P89
AU21	GND
AU22	VDD_0P89
AU23	GND
AU24	VIO_1P10
AU25	GND
AU26	VDD_0P89
AU27	GND
AU28	VDD_0P89
AU29	GND
AU30	VDD_0P89
AU31	GND
AU32	VDD_0P89
AU33	GND
AU34	VDD_0P89
AU35	VIO_1P10
AU36	VPCI_1P20
AU37	PV_PIN_P_CT_E1_TERMREF_N
AU38	GND
AU39	PE_CT_P_PIN_E1_PERST1_B
AU40	PE_PIN_P_E1_CK0_DAT_00_P
AU41	PE_PIN_P_E1_CK0_DAT_03_N
AU42	PE_PIN_P_E1_CK0_DAT_05_P
AU43	GND
AU44	GND
AU45	NV_PIN_P_V1_CK0_DAT_03_P
AU46	NV_PIN_P_V1_CK0_DAT_02_P
AU47	GND
AU48	GND
AV01	GND
AV02	NX_X1_P_PIN_CK2_DAT_03
AV03	GND

Position	Net Name
AV04	NX_X1_P_PIN_CK3_DAT_06
AV05	GND
AV06	NX_X1_P_PIN_CK3_DAT_05
AV07	GND
AV08	GND
AV09	MM_M1_P_PIN_CKD_DAT_03_N
AV10	MM_M1_P_PIN_CKD_DAT_03_P
AV11	GND
AV12	GND
AV13	MM_CT_P_PIN_MB_MEM_ REFCLK6_N
AV14	GND
AV15	VIO_1P10
AV16	GND
AV17	VIO_1P10
AV18	GND
AV19	VIO_1P10
AV20	GND
AV21	VIO_1P10
AV22	GND
AV23	VIO_1P10
AV24	GND
AV25	VIO_1P10
AV26	GND
AV27	VIO_1P10
AV28	GND
AV29	VIO_1P10
AV30	GND
AV31	VSB_1P20
AV32	GND
AV33	VSB_1P20
AV34	GND
AV35	VPCI_1P20
AV36	GND
AV37	PV_PIN_P_CT_E1_TERMREF_P
AV38	GND
AV39	GND
AV40	PE_PIN_P_E1_CK0_DAT_00_N
AV41	PE_PIN_P_E1_CK0_DAT_02_N

Position	Net Name
AV42	PE_PIN_P_E1_CK0_DAT_05_N
AV43	PE_PIN_P_E1_CK0_DAT_07_N
AV44	GND
AV45	GND
AV46	NV_PIN_P_V1_CK0_DAT_02_N
AV47	NV_PIN_P_V1_CK0_DAT_01_N
AV48	GND
AW01	NX_X1_P_PIN_CK3_DAT_08
AW02	GND
AW03	NX_X1_P_PIN_CK3_DAT_07
AW04	GND
AW05	NX_X1_P_PIN_CK3_DAT_13
AW06	GND
AW07	GND
AW08	MM_M1_P_PIN_CKD_DAT_05_P
AW09	MM_M1_P_PIN_CKD_DAT_05_N
AW10	MM_M1_P_PIN_CKD_DAT_02_P
AW11	MM_M1_P_PIN_CKD_DAT_02_N
AW12	GND
AW13	GND
AW14	VIO_1P10
AW15	GND
AW16	VIO_1P10
AW17	GND
AW18	VIO_1P10
AW19	GND
AW20	VIO_1P10
AW21	GND
AW22	VIO_1P10
AW23	GND
AW24	VIO_1P10
AW25	GND
AW26	PV_PIN_P_CT_VIO_PGOOD
AW27	GND
AW28	VIO_1P10
AW29	GND
AW30	VIO_1P10
AW31	PV_CT_B_PIN_LPC_DATA_03

Position	Net Name
AW32	PV_CT_B_PIN_LPC_DATA_01
AW33	PV_CT_P_PIN_LPC_FRAME_B
AW34	PV_PIN_P_CT_LPC_RESET_B
AW35	VIO_1P10
AW36	PV_PIN_P_CT_LPC_CLK
AW37	GND
AW38	GND
AW39	PE_CT_P_PIN_E1_PERST0_B
AW40	GND
AW41	PE_PIN_P_E1_CK0_DAT_02_P
AW42	PE_PIN_P_E1_CK0_DAT_04_P
AW43	PE_PIN_P_E1_CK0_DAT_07_P
AW44	GND
AW45	GND
AW46	GND
AW47	NV_PIN_P_V1_CK0_DAT_01_P
AW48	NV_PIN_P_V1_CK0_DAT_00_P
AY01	GND
AY02	NX_X1_P_PIN_CK3_CLK_N
AY03	GND
AY04	NX_X1_P_PIN_CK3_DAT_09
AY05	GND
AY06	NX_X1_P_PIN_CK3_DAT_14
AY07	GND
AY08	GND
AY09	MM_M1_P_PIN_CKD_DAT_04_N
AY10	MM_M1_P_PIN_CKD_DAT_04_P
AY11	MM_M1_P_PIN_CKD_DAT_00_P
AY12	MM_M1_P_PIN_CKD_DAT_00_N
AY13	GND
AY14	GND
AY15	TS_CT_P_PIN_M1_T_PLLHFC_MKERF_N
AY16	TS_CT_P_PIN_M1_T_PLLHFC_MKERF_P
AY17	GND
AY18	TS_CT_P_PIN_M1_PLL_ANATST
AY19	GND
AY20	PV_PIN_P_CT_M1_TERMREF_P

Position	Net Name
AY21	PV_PIN_P_CT_M1_TERMREF_N
AY22	GND
AY23	GND
AY24	TS_CT_P_PIN_PROBE3
AY25	GND
AY26	TS_CT_P_PIN_PROBE4
AY27	TS_CT_P_PIN_PROBE2
AY28	GND
AY29	TS_CT_P_PIN_PROBE0_P
AY30	TS_CT_P_PIN_PROBE0_N
AY31	GND
AY32	PV_CT_B_PIN_LPC_DATA_02
AY33	PV_CT_B_PIN_LPC_DATA_00
AY34	GND
AY35	TS_CT_P_PIN_VPCI1_VSENSE
AY36	GND
AY37	TS_CT_P_PIN_PE1_PLL_ANATST
AY38	GND
AY39	GND
AY40	GND
AY41	GND
AY42	PE_PIN_P_E1_CK0_DAT_04_N
AY43	PE_PIN_P_E1_CK0_DAT_06_P
AY44	PE_PIN_P_CT_E1_PRSNT1_B
AY45	PE_PIN_P_E1_CK1_DAT_07_P
AY46	GND
AY47	GND
AY48	NV_PIN_P_V1_CK0_DAT_00_N
BA01	NX_X1_P_PIN_CK3_CLK_P
BA02	GND
BA03	NX_X1_P_PIN_CK3_DAT_10
BA04	GND
BA05	NX_X1_P_PIN_CK3_DAT_19
BA06	GND
BA07	GND
BA08	MM_M1_P_PIN_CKD_DAT_07_P
BA09	MM_M1_P_PIN_CKD_DAT_07_N
BA10	MM_M1_P_PIN_CKD_DAT_01_N

Position	Net Name
BA11	MM_M1_P_PIN_CKD_DAT_01_P
BA12	GND
BA13	MM_M1_P_PIN_CKC_DAT_02_P
BA14	MM_M1_P_PIN_CKC_DAT_02_N
BA15	MM_M1_P_PIN_CKC_DAT_00_P
BA16	MM_M1_P_PIN_CKC_DAT_00_N
BA17	GND
BA18	GND
BA19	MM_PIN_P_M1_CKD_DAT_00_P
BA20	MM_PIN_P_M1_CKD_DAT_00_N
BA21	MM_PIN_P_M1_CKD_DAT_01_P
BA22	MM_PIN_P_M1_CKD_DAT_01_N
BA23	GND
BA24	MM_PIN_P_M1_CKC_DAT_01_P
BA25	MM_PIN_P_M1_CKC_DAT_01_N
BA26	GND
BA27	MM_PIN_P_M1_CKC_DAT_23_N
BA28	MM_PIN_P_M1_CKC_DAT_23_P
BA29	GND
BA30	GND
BA31	MM_CT_P_PIN_MB_FSI7_CLK
BA32	MM_CT_B_PIN_MB_FSI7_DATA
BA33	GND
BA34	TS_CT_P_PIN_VIO_VSENSE
BA35	TS_CT_P_PIN_VIO_VPCI_GSENSE
BA36	GND
BA37	PE_E1_P_PIN_CK0_DAT_00_P
BA38	PE_E1_P_PIN_CK0_DAT_00_N
BA39	PE_E1_P_PIN_CK0_DAT_02_N
BA40	PE_E1_P_PIN_CK0_DAT_02_P
BA41	GND
BA42	GND
BA43	PE_PIN_P_E1_CK0_DAT_06_N
BA44	GND
BA45	PE_PIN_P_E1_CK1_DAT_07_N
BA46	PE_PIN_P_E1_CK1_DAT_06_P
BA47	GND
BA48	GND

Position	Net Name
BB01	GND
BB02	NX_X1_P_PIN_CK3_DAT_11
BB03	GND
BB04	NX_X1_P_PIN_CK3_DAT_18
BB05	GND
BB06	GND
BB07	MM_M1_P_PIN_CKD_DAT_08_P
BB08	MM_M1_P_PIN_CKD_DAT_08_N
BB09	MM_M1_P_PIN_CKD_DAT_06_P
BB10	MM_M1_P_PIN_CKD_DAT_06_N
BB11	GND
BB12	MM_M1_P_PIN_CKC_DAT_04_P
BB13	MM_M1_P_PIN_CKC_DAT_04_N
BB14	MM_M1_P_PIN_CKC_DAT_01_P
BB15	MM_M1_P_PIN_CKC_DAT_01_N
BB16	GND
BB17	GND
BB18	MM_PIN_P_M1_CKD_DAT_02_P
BB19	MM_PIN_P_M1_CKD_DAT_02_N
BB20	MM_PIN_P_M1_CKD_DAT_03_P
BB21	MM_PIN_P_M1_CKD_DAT_03_N
BB22	GND
BB23	GND
BB24	GND
BB25	MM_PIN_P_M1_CKC_DAT_06_P
BB26	MM_PIN_P_M1_CKC_DAT_06_N
BB27	GND
BB28	MM_PIN_P_M1_CKC_DAT_22_N
BB29	MM_PIN_P_M1_CKC_DAT_22_P
BB30	GND
BB31	GND
BB32	MM_CT_P_PIN_MB_FSI6_CLK
BB33	MM_CT_B_PIN_MB_FSI6_DATA
BB34	GND
BB35	PV_CT_P_PIN_ATTENTION_B
BB36	GND
BB37	GND
BB38	PE_E1_P_PIN_CK0_DAT_01_P

Position	Net Name
BB39	PE_E1_P_PIN_CK0_DAT_01_N
BB40	PE_E1_P_PIN_CK0_DAT_04_N
BB41	PE_E1_P_PIN_CK0_DAT_04_P
BB42	GND
BB43	GND
BB44	PE_PIN_P_CT_E1_PRSNT0_B
BB45	PE_PIN_P_E1_CK1_DAT_05_P
BB46	PE_PIN_P_E1_CK1_DAT_06_N
BB47	PE_PIN_P_E1_CK1_DAT_04_N
BB48	GND
BC01	NX_X1_P_PIN_CK3_DAT_12
BC02	GND
BC03	NX_X1_P_PIN_CK3_DAT_17
BC04	GND
BC05	GND
BC06	MM_M1_P_PIN_CKD_DAT_09_N
BC07	MM_M1_P_PIN_CKD_DAT_09_P
BC08	MM_M1_P_PIN_CKD_CLK_P
BC09	MM_M1_P_PIN_CKD_CLK_N
BC10	GND
BC11	MM_M1_P_PIN_CKC_DAT_06_P
BC12	MM_M1_P_PIN_CKC_DAT_06_N
BC13	MM_M1_P_PIN_CKC_DAT_03_P
BC14	MM_M1_P_PIN_CKC_DAT_03_N
BC15	GND
BC16	GND
BC17	MM_PIN_P_M1_CKD_DAT_04_P
BC18	MM_PIN_P_M1_CKD_DAT_04_N
BC19	MM_PIN_P_M1_CKD_DAT_19_N
BC20	MM_PIN_P_M1_CKD_DAT_19_P
BC21	GND
BC22	MM_PIN_P_M1_CKD_DAT_23_N
BC23	MM_PIN_P_M1_CKD_DAT_23_P
BC24	GND
BC25	GND
BC26	MM_PIN_P_M1_CKC_DAT_10_P
BC27	MM_PIN_P_M1_CKC_DAT_10_N
BC28	GND

Position	Net Name
BC29	MM_PIN_P_M1_CKC_DAT_21_N
BC30	MM_PIN_P_M1_CKC_DAT_21_P
BC31	GND
BC32	GND
BC33	MM_CT_P_PIN_MB_FSI3_CLK
BC34	MM_CT_B_PIN_MB_FSI3_DATA
BC35	GND
BC36	TS_PIN_P_CT_STBY_RESET_B
BC37	GND
BC38	GND
BC39	PE_E1_P_PIN_CK0_DAT_03_N
BC40	PE_E1_P_PIN_CK0_DAT_03_P
BC41	PE_E1_P_PIN_CK0_DAT_06_N
BC42	PE_E1_P_PIN_CK0_DAT_06_P
BC43	GND
BC44	GND
BC45	PE_PIN_P_E1_CK1_DAT_05_N
BC46	PE_PIN_P_E1_CK1_DAT_02_P
BC47	PE_PIN_P_E1_CK1_DAT_04_P
BC48	PE_PIN_P_E1_CK1_DAT_03_N
BD01	GND
BD02	NX_X1_P_PIN_CK3_DAT_16
BD03	GND
BD04	GND
BD05	MM_M1_P_PIN_CKD_DAT_10_N
BD06	MM_M1_P_PIN_CKD_DAT_10_P
BD07	MM_M1_P_PIN_CKD_DAT_11_N
BD08	MM_M1_P_PIN_CKD_DAT_11_P
BD09	GND
BD10	MM_M1_P_PIN_CKC_CLK_N
BD11	MM_M1_P_PIN_CKC_CLK_P
BD12	MM_M1_P_PIN_CKC_DAT_05_P
BD13	MM_M1_P_PIN_CKC_DAT_05_N
BD14	GND
BD15	GND
BD16	MM_PIN_P_M1_CKD_DAT_05_N
BD17	MM_PIN_P_M1_CKD_DAT_05_P
BD18	MM_PIN_P_M1_CKD_DAT_14_P

Position	Net Name
BD19	MM_PIN_P_M1_CKD_DAT_14_N
BD20	GND
BD21	MM_PIN_P_M1_CKD_DAT_22_N
BD22	MM_PIN_P_M1_CKD_DAT_22_P
BD23	GND
BD24	GND
BD25	MM_PIN_P_M1_CKC_DAT_04_P
BD26	MM_PIN_P_M1_CKC_DAT_04_N
BD27	GND
BD28	MM_PIN_P_M1_CKC_DAT_19_N
BD29	MM_PIN_P_M1_CKC_DAT_19_P
BD30	MM_PIN_P_M1_CKC_DAT_20_N
BD31	MM_PIN_P_M1_CKC_DAT_20_P
BD32	GND
BD33	GND
BD34	MM_CT_P_PIN_MB_FSI2_CLK
BD35	MM_CT_B_PIN_MB_FSI2_DATA
BD36	GND
BD37	TS_PIN_P_CT_TEST_LSSD_TE
BD38	GND
BD39	GND
BD40	PE_E1_P_PIN_CK0_DAT_05_N
BD41	PE_E1_P_PIN_CK0_DAT_05_P
BD42	PE_E1_P_PIN_CK1_DAT_07_N
BD43	PE_E1_P_PIN_CK1_DAT_07_P
BD44	GND
BD45	GND
BD46	PE_PIN_P_E1_CK1_DAT_02_N
BD47	PE_PIN_P_E1_CK1_DAT_01_P
BD48	PE_PIN_P_E1_CK1_DAT_03_P
BE01	NX_X1_P_PIN_CK3_DAT_15
BE02	GND
BE03	GND
BE04	MM_M1_P_PIN_CKD_DAT_12_P
BE05	MM_M1_P_PIN_CKD_DAT_12_N
BE06	MM_M1_P_PIN_CKD_DAT_13_N
BE07	MM_M1_P_PIN_CKD_DAT_13_P
BE08	GND

Position	Net Name
BE09	MM_M1_P_PIN_CKC_DAT_14_N
BE10	MM_M1_P_PIN_CKC_DAT_14_P
BE11	MM_M1_P_PIN_CKC_DAT_07_P
BE12	MM_M1_P_PIN_CKC_DAT_07_N
BE13	GND
BE14	GND
BE15	MM_PIN_P_M1_CKD_DAT_06_P
BE16	MM_PIN_P_M1_CKD_DAT_06_N
BE17	MM_PIN_P_M1_CKD_DAT_12_P
BE18	MM_PIN_P_M1_CKD_DAT_12_N
BE19	GND
BE20	MM_PIN_P_M1_CKD_DAT_21_N
BE21	MM_PIN_P_M1_CKD_DAT_21_P
BE22	GND
BE23	SH_PIN_P_CT_FSP1_FSI_DATA
BE24	GND
BE25	GND
BE26	MM_PIN_P_M1_CKC_DAT_05_P
BE27	MM_PIN_P_M1_CKC_DAT_05_N
BE28	GND
BE29	MM_PIN_P_M1_CKC_DAT_14_P
BE30	MM_PIN_P_M1_CKC_DAT_14_N
BE31	MM_PIN_P_M1_CKC_DAT_18_N
BE32	MM_PIN_P_M1_CKC_DAT_18_P
BE33	GND
BE34	GND
BE35	PV_CT_P_PIN_FSI1_CLK
BE36	PV_CT_B_PIN_FSI1_DATA
BE37	GND
BE38	TS_PIN_P_CT_CARD_TEST
BE39	GND
BE40	GND
BE41	PE_E1_P_PIN_CK0_DAT_07_N
BE42	PE_E1_P_PIN_CK0_DAT_07_P
BE43	PE_E1_P_PIN_CK1_DAT_06_N
BE44	PE_E1_P_PIN_CK1_DAT_06_P
BE45	GND
BE46	GND

Position	Net Name
BE47	PE_PIN_P_E1_CK1_DAT_01_N
BE48	PE_PIN_P_E1_CK1_DAT_00_P
BF01	GND
BF02	GND
BF03	MM_M1_P_PIN_CKD_DAT_14_N
BF04	MM_M1_P_PIN_CKD_DAT_14_P
BF05	MM_M1_P_PIN_CKD_DAT_16_N
BF06	MM_M1_P_PIN_CKD_DAT_16_P
BF07	GND
BF08	MM_M1_P_PIN_CKC_DAT_10_P
BF09	MM_M1_P_PIN_CKC_DAT_10_N
BF10	MM_M1_P_PIN_CKC_DAT_08_N
BF11	MM_M1_P_PIN_CKC_DAT_08_P
BF12	GND
BF13	GND
BF14	MM_PIN_P_M1_CKD_DAT_08_P
BF15	MM_PIN_P_M1_CKD_DAT_08_N
BF16	MM_PIN_P_M1_CKD_DAT_10_P
BF17	MM_PIN_P_M1_CKD_DAT_10_N
BF18	GND
BF19	MM_PIN_P_M1_CKD_DAT_16_N
BF20	MM_PIN_P_M1_CKD_DAT_16_P
BF21	MM_PIN_P_M1_CKD_DAT_20_N
BF22	MM_PIN_P_M1_CKD_DAT_20_P
BF23	GND
BF24	MM_PIN_P_M1_CKC_DAT_00_P
BF25	MM_PIN_P_M1_CKC_DAT_00_N
BF26	GND
BF27	MM_PIN_P_M1_CKC_DAT_08_P
BF28	MM_PIN_P_M1_CKC_DAT_08_N
BF29	GND
BF30	MM_PIN_P_M1_CKC_CLK_P
BF31	MM_PIN_P_M1_CKC_CLK_N
BF32	MM_PIN_P_M1_CKC_DAT_16_N
BF33	MM_PIN_P_M1_CKC_DAT_16_P
BF34	GND
BF35	GND
BF36	PV_CT_B_PIN_LPC_SERIRQ

Position	Net Name
BF37	PV_PIN_B_CT_I2CSL_SDA
BF38	PV_PIN_P_CT_FSI_SMD
BF39	PV_PIN_P_CT_CHIP_ID0
BF40	GND
BF41	GND
BF42	PE_E1_P_PIN_CK1_DAT_00_N
BF43	PE_E1_P_PIN_CK1_DAT_00_P
BF44	PE_E1_P_PIN_CK1_DAT_05_N
BF45	PE_E1_P_PIN_CK1_DAT_05_P
BF46	GND
BF47	GND
BF48	PE_PIN_P_E1_CK1_DAT_00_N
BG01	GND
BG02	MM_M1_P_PIN_CKD_DAT_15_N
BG03	MM_M1_P_PIN_CKD_DAT_15_P
BG04	MM_M1_P_PIN_CKC_DAT_15_N
BG05	MM_M1_P_PIN_CKC_DAT_15_P
BG06	GND
BG07	MM_M1_P_PIN_CKC_DAT_12_P
BG08	MM_M1_P_PIN_CKC_DAT_12_N
BG09	MM_M1_P_PIN_CKC_DAT_09_N
BG10	MM_M1_P_PIN_CKC_DAT_09_P
BG11	GND
BG12	GND
BG13	MM_PIN_P_M1_CKD_DAT_09_P
BG14	MM_PIN_P_M1_CKD_DAT_09_N
BG15	MM_PIN_P_M1_CKD_CLK_P
BG16	MM_PIN_P_M1_CKD_CLK_N
BG17	GND
BG18	MM_PIN_P_M1_CKD_DAT_15_P
BG19	MM_PIN_P_M1_CKD_DAT_15_N
BG20	MM_PIN_P_M1_CKD_DAT_18_N
BG21	MM_PIN_P_M1_CKD_DAT_18_P
BG22	GND
BG23	SH_PIN_P_CT_FSP1_FSI_CLK
BG24	GND
BG25	MM_PIN_P_M1_CKC_DAT_02_P
BG26	MM_PIN_P_M1_CKC_DAT_02_N

Position	Net Name
BG27	GND
BG28	MM_PIN_P_M1_CKC_DAT_09_P
BG29	MM_PIN_P_M1_CKC_DAT_09_N
BG30	GND
BG31	MM_PIN_P_M1_CKC_DAT_12_P
BG32	MM_PIN_P_M1_CKC_DAT_12_N
BG33	MM_PIN_P_M1_CKC_DAT_15_P
BG34	MM_PIN_P_M1_CKC_DAT_15_N
BG35	GND
BG36	GND
BG37	PV_PIN_B_CT_I2CSL_SCL
BG38	PV_PIN_P_CT_CHIP_ID1
BG39	PV_PIN_P_CT_FSI_IN_ENA1
BG40	GND
BG41	GND
BG42	GND
BG43	PE_E1_P_PIN_CK1_DAT_02_N
BG44	PE_E1_P_PIN_CK1_DAT_02_P
BG45	PE_E1_P_PIN_CK1_DAT_03_N
BG46	PE_E1_P_PIN_CK1_DAT_03_P
BG47	GND
BG48	GND
BH03	MM_M1_P_PIN_CKC_DAT_16_N
BH04	MM_M1_P_PIN_CKC_DAT_16_P
BH05	GND
BH06	MM_M1_P_PIN_CKC_DAT_13_N
BH07	MM_M1_P_PIN_CKC_DAT_13_P
BH08	MM_M1_P_PIN_CKC_DAT_11_N
BH09	MM_M1_P_PIN_CKC_DAT_11_P
BH10	GND
BH11	GND
BH12	MM_PIN_P_M1_CKD_DAT_07_P
BH13	MM_PIN_P_M1_CKD_DAT_07_N
BH14	MM_PIN_P_M1_CKD_DAT_11_P
BH15	MM_PIN_P_M1_CKD_DAT_11_N
BH16	GND
BH17	MM_PIN_P_M1_CKD_DAT_13_P
BH18	MM_PIN_P_M1_CKD_DAT_13_N

Position	Net Name
BH19	MM_PIN_P_M1_CKD_DAT_17_N
BH20	MM_PIN_P_M1_CKD_DAT_17_P
BH21	GND
BH22	GND
BH23	MM_PIN_P_M1_CKC_DAT_03_P
BH24	MM_PIN_P_M1_CKC_DAT_03_N
BH25	GND
BH26	MM_PIN_P_M1_CKC_DAT_07_P
BH27	MM_PIN_P_M1_CKC_DAT_07_N
BH28	GND
BH29	MM_PIN_P_M1_CKC_DAT_11_P
BH30	MM_PIN_P_M1_CKC_DAT_11_N
BH31	GND
BH32	MM_PIN_P_M1_CKC_DAT_13_P
BH33	MM_PIN_P_M1_CKC_DAT_13_N
BH34	MM_PIN_P_M1_CKC_DAT_17_N
BH35	MM_PIN_P_M1_CKC_DAT_17_P
BH36	GND
BH37	PV_CT_B_PIN_LP_I2C_SDA_B
BH38	PV_CT_B_PIN_LP_I2C_SCL_B
BH39	GND
BH40	PV_PIN_P_CT_FSP0_FSI_CLK
BH41	PV_PIN_B_CT_FSP0_FSI_DATA
BH42	GND
BH43	GND
BH44	PE_E1_P_PIN_CK1_DAT_01_N
BH45	PE_E1_P_PIN_CK1_DAT_01_P
BH46	PE_E1_P_PIN_CK1_DAT_04_P
BH47	PE_E1_P_PIN_CK1_DAT_04_N
BH48	GND

Glossary

AES	Advanced Encryption Standard
ASIC	Application-specific integrated circuit
BIST	Built-in self-test
BMC	Baseboard management controller
BR	Branch register unit
CAI	Coherent accelerator
CAPI	Coherent accelerator processor interface
CMOS	Complementary metal–oxide–semiconductor
CPM	Critical path monitor
CPU	Central processing unit
CR	Condition register unit
DDR	Double data rate
DFE	Decision feedback equalizer
DFU	Decimal floating-point unit
DIMM	Dual in-line memory module
DMA	Direct memory attach
DMI	Differential memory interface
DRAM	Dynamic random access memory
DTS	Digital thermal sensor
ECO	Extended cache option
ECID	Electronic chip identification
ECRC	End-to-end CRC
EDI	Elastic differential I/O
EEH	Enhance error handling
EEPROM	Electrically erasable programmable read-only memory
EI4	Elastic interface 4
ET	Early time
FC PLGA	Flip-chip plastic land grid array

FIFO	First-in, first-out
FRU	Field-replaceable unit
FSI	FRU service interface
FSP	Flexible service processor
FXU	Fixed-point units
GFW	Global firmware
GT/s	Gigatransfers per second
GPU	Graphics processing unit
HCSL	Host clock signal level
HPC	High-performance computing
HSS	High-speed serial
I^2C	Inter-integrated circuit
IEEE	Institute of Electrical and Electronics Engineers
IFU	Instruction fetch units
IP	Intellectual property
ISA	Instruction set architecture
iVRM	Internal voltage regulator module
JTAG	Joint Test Action Group
LCB	Logon control block
LED	Light-emitting diode
LGA	Land grid array
LPAR	Logical partition
LPC	Low pin count bus or lowest point of coherency
LPST	Local Pstate table
LSI	Level signalled interrupt
LSSD	Level-sensitive scan design
LSU	Load store units
MFSI	Master FSI
MPG	Multi-protocol gateway

MPUL	Most-positive up level
MSI	Message signalled interrupt
NCI	NVLink coherent interconnect
OCC	On-chip controller
OEM	Original equipment manufacturer
PAPR	Power Architecture Platform Reference
PCIe	Peripheral Component Interconnect Express
PE	Partitionable endpoints
PEC	PCI Express controller
PHB	PCI host bridge
PLL	Phase-locked loop
PMC	Power management control
PMCR	Power Management Control Register
PMICR	Power Management Idle Control Register
PMSR	Power Management Status Register
PPM	Parts per million
PSI	Processor support interface
PVR	Processor Version Register
RC	Root complex
SBE	Self-boot engine
SCM	Single-chip module
SCOM	Scan communications
SEEPROM	Serial electrically erasable programmable read-only memory
SMP	Symmetric multiprocessing
SHA	Secure Hash Algorithm
SOI	Silicon on insulator
SPI	Serial peripheral interconnect
SPR	Special-Purpose Register
SRAM	Static random access memory

SVIC	Special, vertical interconnect channel
TCE	Translation control entry
TDP	Thermal design point
TLP	Transaction layer packet
TPM	Trusted platform module
UPS	Uninterrupted power system
VID	Voltage ID
VPD	Vital product data
VLE	Variable length encoding
VRM	Voltage regulator module