POWER9 Sforza Single-Chip Module Datasheet

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Revision Log

Each release of this document supersedes all previously released versions. The revision log lists all significant changes made to the document since its initial release. In the rest of the document, change bars in the margin indicate that the adjacent text was modified from the previous release of this document.

Revision Date	Description
13 June 2019	Version 1.8. • Added the PVR for DD 2.3 to *Table 1-1 POWER9 Processor Version Register* on page 16. • Revised *Section 1.11 Related Documents* on page 16. • Revised *Table 2-1 POWER9 SCM Technology* on page 19. • Revised *Table 6-10 Power, Frequencies, and Junction Temperature*[1] on page 59. • Revised *Table 7-1 SCM Features* on page 71.
17 April 2017	Version 1.7. • Revised *Table 2-1 POWER9 SCM Technology* on page 19. • Revised the table notes in *Table 5-5 AVS Signals* on page 36. • Revised *Table 6-2 POWER9 Processor $V_{DD\ (Core)\ Voltage\ Requirements}$* on page 54. • Revised *Table 6-3 POWER9 Processor $V_{CS\ (Cache)\ Voltage\ Requirements}$* on page 55. • Revised *Table 6-4 POWER9 Processor $V_{DN\ Voltage\ Requirements}$* on page 55. • Revised *Table 6-5 POWER9 Processor $V_{IO\ Voltage\ Requirements}$* on page 56. • Added a part number to *Table 6-10 Power, Frequencies, and Junction Temperature*[1] on page 59. • Revised *Table 6-15 Default FSI Settings* on page 66. • Revised *Table 6-18 AVS AC Specification* on page 68. • Revised *Table 6-19 Default AVS Settings* on page 68.
18 October 2018	Version 1.61. • Revised *Section 1.11 Related Documents* on page 16.
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Revision Date	Description
30 January 2018	Version 1.3. • Revised *Table 2-1 POWER9 SCM Technology* on page 19. • Revised *Table 3-4 Chip P0* on page 24. • Revised *Section 4.1 Power Gating and On-Chip, Per-Core Voltage Regulation* on page 29. • Revised *Section 4.2 Efficient Power Supply Oversubscription Capability* on page 29. • Revised *Table 4-2 System Main Power Sequence* on page 32. • Revised *Table 6-2 POWER9 Frequency Domains* on page 54. • Revised *Table 6-2 POWER9 Processor $V_{DD\ (Core)\ Voltage\ Requirements}$* on page 54. • Revised *Table 6-3 POWER9 Processor $V_{CS\ (Cache)\ Voltage\ Requirements}$* on page 55. • Revised *Table 6-4 POWER9 Processor $V_{DN\ Voltage\ Requirements}$* on page 55. • Revised *Table 6-5 POWER9 Processor $V_{IO\ Voltage\ Requirements}$* on page 56. • Revised *Section 6.2.2 Power and Frequencies* on page 57. • Revised *Table 7-1 SCM Features* on page 71. • Revised *Table 7-3 Sforza SCM Pin List* on page 73.
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Revision Date	Description
16 January 2017	Version 1.1. • Revised *Section 1 Introduction* on page 13. • Revised *Section 1.1 Processor Feature Summary* on page 13. • Revised *Section 1.6 Signals* on page 15. • Revised *Section 1.7 Electrical* on page 15. • Revised *Section 1.8 Package Support* on page 15. • Revised *Section 1.12.2 Bit Significance* on page 17. • Revised *Section 3.1 Service Interfaces* on page 21. • Revised *Table 3-2 Inter-Node SMP X-Bus Highlights* on page 22. • Revised *Section 3.3.4 PCIe Bus* on page 24. • Revised *Table 3-4 Chip P0* on page 24. • Revised *Section 3.5 Inter-Node SMP X Bus* on page 27. • Revised *Section 5.1 Pin Naming Convention* on page 34. • Revised *Table 5-3 Voltage and Ground Signals* on page 35. • Revised *Section 5.2.2 APSS Signals* on page 36. • Added a note to *Table 5-4 APSS Signals* on page 36. • Revised *Table 5-5 AVS Signals* on page 36. • Revised *Table 5-6 FSI Signals* on page 37. • Revised *Table 5-7 Clock System Signals* on page 37. • Revised *Table 5-8 I^{2C} Signals* on page 38. • Revised *Table 5-9 X-Bus Signals* on page 39. • Revised *Table 5-10 PCIe Controller and Clock Bus Signals* on page 40. • Revised *Table 5-11 LPC Bus Signals* on page 42. • Revised *Table 5-12 Memory Signals* on page 42. • Revised *Table 5-13 JTAG Signals* on page 47 • Revised *Table 5-14 Miscellaneous Signals* on page 48. • Revised *Table 5-15 Test Signals* on page 50. • Revised *Table 6-2 POWER9 Processor $V_{DD\ (Core)}$ Voltage Requirements* on page 54. • Revised *Table 6-3 POWER9 Processor $V_{CS\ (Cache)}$ Voltage Requirements* on page 55. • Revised *Table 6-4 POWER9 Processor V_{DN} Voltage Requirements* on page 55. • Revised *Table 6-5 POWER9 Processor V_{IO} Voltage Requirements* on page 56. • Revised *Table 6-6 POWER9 Processor $AV_{DD/DVDD}$ Voltage Requirements* on page 56. • Revised *Table 6-7 POWER9 DDR4 Voltage Requirements* on page 56. • Revised *Table 6-8 1.1 $V_{SB:\ Standby/Auxiliary}$* on page 57. • Revised *Table 6-9 3.3 $V_{SB:\ Standby/Auxiliary}$* on page 57. • Revised *Section 6.2.3 Miscellaneous Signals* on page 60. • Revised *Section 6.3.1 Clock AC Specifications* on page 60. • Removed tables previously known as *Table 6-8 DIMM V_{TT} Voltage Requirements* and *Table 6-9 DIMM V_{PP} Voltage Requirements*. • Revised *Table 6-17 Default SPI Settings* on page 67. • Revised *Section 6.3.5 AVS AC Specifications* on page 68. • Revised a note in *Table 6-18 AVS AC Specification* on page 68. • Removed the Pull-Up column in *Table 6-19 Default AVS Settings* on page 68. • Revised *Section 6.3.5.1 Recommended AVSBus Topology* on page 69. • Updated the *Glossary* on page 97.
29 August 2016	Version 1.0 (initial version).

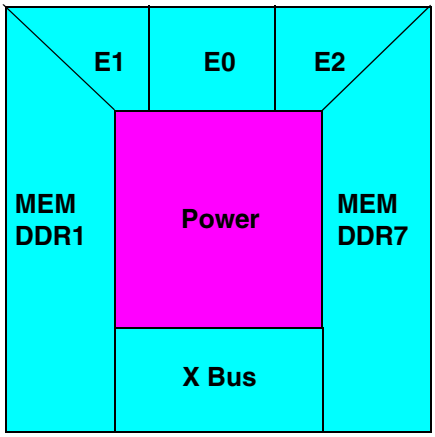
1. Introduction

This datasheet describes the IBM® POWER9™ processor in the Sforza single-chip module (SCM). The POWER9 processor is a superscalar symmetric multiprocessor designed for use in servers and large-cluster systems. It uses CMOS 14 nm technology with 17 metal layers.

The POWER9 processor can have up to 24 cores enabled on a single chip. It supports direct-attach memory, a maximum symmetric multiprocessing (SMP) size of two sockets, and is targeted for scale-out workloads. Each POWER9 core supports up to four threads using simultaneous multithreading (SMT). The SMT can be dynamically tuned so that each core has one, two, or four threads.

Figure 1-1 illustrates the POWER9 Sforza pinout diagram.

Figure 1-1. POWER9 Sforza Pinout Map



1.1 Processor Feature Summary

The POWER9 processor consists of the following main components:

- Twenty-four POWER9 cores with shared L2 and L3 caches and a noncacheable unit (NCU)
- On-chip accelerators.
  - CAPI allows an FPGA or ASIC to connect coherently to the POWER9 processor SMP interconnect via the PCIe bus.
  - On-chip: compression, encryption, data move initiated by the hypervisor, GZIP engine, or nest MMU to enable user access to all accelerators.
  - In-core: user invocation encryption (AES, SHA).
- Two memory controllers that support direct-attached DDR4 memory.
  - Supports four direct-attach memory buses (DDR 0, 1, 6, and 7).
  - Supports ×4 and ×8, 4 - 16 Gb DRAMs and 3D stacked DRAMs.
  - Supports RDIMMs and LRDIMMs.

- Processor SMP interconnect.
  - Supports one inter-node SMP X-bus link.
  - Maximum two-socket SMP.
- Three PCIe controllers (PEC) with 16 lanes of PCI Express Gen4 I/O.
  - PEC0: one ×16 lanes.
  - PEC1: two ×8 lanes (bifurcation).
  - PEC2: one ×16 lane mode, two ×8 lanes (bifurcation), or one ×8 lane and two ×4 lanes (trifurcation).
  - PEC0 and PEC2 support CAPI 2.0.
- Power management.
- Pervasive interface.

1.2 Supported Technologies

The POWER9 processor supports the following technologies:

- Power ISA Book I, II, and III (version 3.0)
- Linux on Power Architecture Platform Reference
- IEEE P754-2008 for binary and decimal floating-point compliant
- Big-endian, little-endian, strong-ordering support extension
- 51-bit real address, 68-bit virtual address

1.3 Interfaces

The primary service interface to the POWER9 processor is the field replaceable unit (FRU) service interface (FSI) that runs at 166 MHz. See *Section 3.1 Service Interfaces* on page 21 for more information.

1.4 Power Management Support

Key features of the POWER9 processor are as follows:

- Hypervisor-directed power change requests using the Pstate mechanism
  - Core/L2/L3 instant on and off
  - Halt state support
  - Controlled by 17 on-chip programmable PPE engines
  - Dynamic lane width reduction (SMP interconnect fabric, PCI)
- Sensors
  - Digital thermal sensor (DTS2) ±5°C
  - Off-chip analog thermal diode ±1 - 2°C
  - Voltage drop monitor

  - Dedicated performance, microarchitecture, and event counters
- Accelerators
  - On-chip IBM PowerPC® 405 embedded processor core for thermal management control
  - On-chiplet hardware assist (automated core chiplet management)
  - On-chip power management controls
    - Automated communications to the voltage regulation modules (VRMs)
    - Voltage and frequency sequencers for automated Pstate and idle state support
- Actuators
  - Per quad chiplet frequency control through the DPLL
  - Architected idle states: nap, sleep, and winkle; each with increasing power savings capability (and latency)
  - SPR power management control registers (PMCR, PMICR, and PMSR) for hypervisor support
- Memory and DIMM throttling for memory subsystem power and thermal management

1.5 Thermal Specification

Thermal junction temperature (T_J) is measured by digital thermal sensors located on the chip. There are four sensors per core, which are averaged. The specified T_J is the worst case of these averages or the hottest core average. The maximum T_J is not allowed to exceed 85°C. The average T_J, at which the reliability is calculated, is 70°C. Margin does not need to be applied when measuring against the worst-case specification because the chip is sorted using the same thermal sensors. The digital thermal sensor has an absolute accuracy of ±5% and can be read out in Celsius (°C).

1.6 Signals

Section 5 Signals on page 33 describes the POWER9 Sforza SCM signals.

1.7 Electrical

Section 6 Electrical Characteristics on page 53 discusses the DC and AC electrical characteristics of the POWER9 Sforza SCM.

1.8 Package Support

Section 7 Mechanical Specifications on page 71 describes the POWER9 Sforza SCM features and provides a pin list.

1.9 Processor Version Register

The POWER9 processor has the following Processor Version Register (PVR) values for the respective design revision levels.

Table 1-1. POWER9 Processor Version Register

POWER9 Design Revision Level	POWER9 PVR
DD 2.1	x'004E1201'
DD 2.2	x'004E1202'
DD 2.3	x'004E1203'

1.10 Marking Specification

The POWER9 Sforza single-chip module (SCM) marking drawing FC PLGA can be found in the IBM Portal for OpenPOWER. See the *POWER9 Thermal and Mechanical Reference Guide for the Sforza SCM* document.

1.11 Related Documents

The following documents can be helpful when reading this specification. Contact your IBM representative to obtain any documents that are not available through the IBM Portal for OpenPOWER, an online IBM technical library or the OpenPOWER Foundation web site.

POWER9 Processor DD 2.1 Use Restrictions Application Note

POWER9 Processor SCM Hardware Errata Notice DD 2.2

For the Development of an Electrostatic Discharge Control Program for – Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices) (ANSI/ESD S20.20-2007)

For the Protection of Electrostatic Discharge Susceptible Items - Packaging Materials for ESD Sensitive Items (ANSI/ESD S541-2008)

I^2C Bus Specification (Version 2.1)

PMBus™ Specification v1.3.1

PCI Express Base Specification, Revision 4.0

1.12 Conventions

This section explains the number, bit field, instruction, and signal conventions that are used in this document.

1.12.1 Representation of Numbers

Numbers are generally shown in decimal format, unless designated as follows:

- Hexadecimal values are preceded by an “x” and enclosed in single quotation marks.
  For example: x‘0A00’.
- Binary values in sentences are shown in single quotation marks.
  For example: ‘1010’.

Note: A bit value that is immaterial, which is called a “don't care” bit, is represented by an “x.”

1.12.2 Bit Significance

In the POWER9 documentation, big-endian notation is usually used. That is, the smallest bit number represents the most significant bit of a field, and the largest bit number represents the least significant bit of a field.

1.12.3 Typographical Conventions

Convention	Description
Footnote reference.[1] 1. Descriptive footnote text.	A footnote is an explanatory note or reference inserted at the foot of the page or under a table that explains or expands upon a point within the text or indicates the source of a citation or peripheral information.
Hyperlink	Web-based URLs are displayed in blue text to denote a virtual link to an external document. For example: http://www.ibm.com
Italic typeface	The italic typeface denotes user-specified components when describing command usage and functionality.
`Monospaced` typeface	The monospaced typeface is used for code examples and for commands in general descriptions.
Note: This is note text.	The note block denotes information that emphasizes a concept or provides critical information.
Underline	An underline indicates that the definition of an acronym is displayed when the user hovers the cursor over the term.

2. Technologies

This section provides a high-level overview of the technologies implemented in the POWER9 processor.

2.1 General Parameters

Table 2-1 lists general parameters for the POWER9 processor.

Table 2-1. POWER9 SCM Technology

Feature	Description
Technology	CMOS 14 nm technology with 17 metal layers
Die Size	695 mm^2
Chip Package (SCM)	See *Table 7-1 SCM Features* on page 71 for details.
Signal I/O	2601
Frequency Range (Base)	1.8 - 4.1 GHz
Power	90 W, 105 W, 130 W, 160 W, and 190 W

3. Interfaces

This section describes the interfaces supported on the POWER9 processor.

3.1 Service Interfaces

The POWER9 processor has multiple service interfaces that are used for initialization during boot. The service interfaces are also accessible by using the debug box. The primary entry point to the POWER9 processor service interface is the FRU service interface (FSI), a serial interface that runs at 166 MHz.

The POWER9 SCM provides the following FSIs:

- One FSI slave for connecting to the debug box or multichip SMP.
- One FSI master for communication to a second POWER9 chip in the system. One POWER9 chip is defined as the master and is responsible for initializing the other POWER9 chip over this FSI.

The POWER9 SCM provides the following additional service interfaces:

- Two adaptive voltage scaling (AVS) buses for controlling processor-related voltage regulators.
- One SPI master for on-chip controller (OCC) management.
- One LPC bus for connecting to the BMC.
- Four I^2C masters for controlling LEDs, PCIe cards, DDR, and so on. The I^2C masters can be manipulated from the OCC or hostboot code.

3.2 Supported Processor Interfaces

This section gives an overview of the physical layer and on-chip initialization provided by the POWER9 processor.

The POWER9 processor supports the following types of drivers and receivers:

- X-bus interface: high-speed differential at 16 Gbps for chip-to-chip interconnect
- DDR4 PHY memory interface

Table 3-1 lists the requirements relative to the operational mode definitions.

Table 3-1. Interface Operational Mode Definitions

Mode Name	Definition
Initialization	The act of aligning and locking the data eye and bit lanes plus additional deltas relative to re-alignment and re-locking.
Functional	Passing workload data and maintaining signal integrity post-initialization.
Power Saving	All related capabilities for minimizing unused and idle lane power consumption.
Test	Capabilities related to hardware manufacturability.
Diagnostic	Bringup lab characterization of interface performance capabilities.

3.2.1 Inter-Node SMP Bus Highlights

Table 3-2 highlights the inter-node SMP X bus. See the *POWER9 Processor User's Manual* for additional information.

Table 3-2. Inter-Node SMP X-Bus Highlights

Feature	Inter-Node SMP X Bus
Frequency	16 Gbps
Initialization Mode Requirement	16 Gbps, 9.6 Gbps
Spare Lane Detect	Data failover Two signals total per bus/port
Functional Mode Specification	16, 9.6 Gbps
Power-Saving Mode Requirement	Power-saving mode supports light power down with fast wakeup
Test Mode Requirement	16 Gbps, 9.6 Gbps[1]
Driver Features	• 16 Gbps with 8:1 serializer. • 9.6 Gbps in 4:1 serializer mode. • Full-rate SST driver. • Selectable 8:1 or 4:1 serializer with pre-cursor FFE. • R_{PRE} up to 1.30. • Selectable AC boost: analog post-cursor FFE. • Set and forget impedance calibrator. • Drive amplitude reduction (margining) up to 50%. For characterization only, not mission mode. • BIST error detector for at-speed loopback testing. • Shared test pin mode. Differential driver output only. • Time domain reflectometer (TDR).
Receiver Features	• RX clock macro with PLL – Same I/O specifications as the POWER8 processor: 2.0 - 2.4 GHz bus clock range – Programmable feedback divider for POWER8 memory buffer backward compatibility • RX data macro – Each data bit with a single data path (single bank) using shadow-lane protocol for calibration – Long-tail equalizer (LTE) for improved eye margins on lossiest channels – Continuous time linear equalizer (CTLE) with 12 dB of peaking range, 6 dB of gain range – CTLE applies common mode (differential zero) for DAC calibrations – 12-tap DFE with current integrating summer. Modes: no-DFE, DFE1, DFE12) – 16 Gbps with 1:8 deserialization mode – 9.6 Gbps with 1:4 deserialization mode – Cross-coupled PRBS streams for RX BIST testing

1. Subject to PLL range limitations and a test frequency of 200 MHz.

3.3 PCI Express Controller

The PCI Express controller (PEC) bridges between the internal processor bus and the high-speed serial (HSS) links that drive the PCI Express I/O. The PEC acts as a processor bus master on behalf of the PCI Express port, converting inbound memory read and write packets into processor bus DMA traffic. The PEC also acts as a processor bus slave, transferring processor load and store commands to the PCI Express devices attached to the port.

3.3.1 Specification Compliance

The PEC is compliant with the following IBM and industry standards:

- *Linux on Power Architecture Platform Reference*
- *I/O Design Architecture v2 (IODA2) Specification, Version 2.4+*
- *PCI Express Base Specification Revision 4.0*

3.3.2 PEC Feature Summary

- PCI Express Gen4 root complex (RC)
  - Backwards compatible with generation 1, generation 2, and generation 3
  - 2.5, 5, 8, and 16 GTps signalling rate
- Forty-eight PCIe I/O lanes configurable to six independent root complexes
- Each root complex has 256 partitionable endpoints (PE) for LPAR support
- TCE-based address translation for DMA requests
  - 51-bit address support
  - Translation validation table based on PCI routing ID
- 2048 MSI interrupts per RC
- Eight LSI interrupts per RC
- IBM enhanced error handling (EEH) support
- Processor bus cache-inhibited space segmented by PEC
  - PCI 32-bit memory space segmented into 256 domains by the memory domain table
  - PCI 64-bit memory space segmented by 16 M64 BARs with 16 segments each
- Support for ECRC
- Support for lane wrapping
- Support for PCIe atomic operations and TLP hints

3.3.3 Supported Configuration

The 48 lanes of HSS I/O can be configured to support six independent PCIe buses. *Table 3-3* describes the maximum lane allocation. In addition to supporting PCI operations, the HSS I/O can be allocated for use by the processor bus SMP interface.

Table 3-3. Supported I/O Configurations

PECx	PHB0	PHB1	PHB2	PHB3	PHB4	PHB5
PEC0	×16					
PEC1		×8	×8			
PEC2				×16		
				×8	×8	
				×8	×4	×4

3.3.4 PCIe Bus

The POWER9 Sforza SCM has a total of 48 PCIe Gen4 lanes. There are three PCIe controllers per processor. The number of PHBs per PEC is variable.

- PEC0 has a single PHB that is non-bifurcatible, ×16 lanes, and CAPI capable.
- PEC 1 has two PHBs that are each ×8 lanes. PEC1does not support being used as a single ×16 interface nor does it support CAPI.
- PEC2 contains up to three PHBs. PEC2 can be run as a single ×16 interface, two ×8 lanes, or a single ×8 lane plus two ×4 lanes. PEC2 is CAPI enabled only as a ×16 interface or the first ×8 lane.

Note: The lanes can be reversed for easier routing if required. The polarity can also be reversed on a lane-by-lane basis.

Table 3-4. Chip P0 (Sheet 1 of 2)

Chip	Interface	Mode	Pins		Notes
P0	E0	×16	Data Lanes	Receive: PE_E0_PIN_P_P0_DAT_[00:15]_P/N Transmit: PE_E0_P0_P_PIN_DAT_[00:15]_P/N	
			Clocks	PV_E0_P0_P_PIN_SLOT_CLK_P/N	1, 2
			Reset	$\overline{\text{PV\_E0\_P0\_P\_PIN\_PERST\_B}}$	3, 4
			Present	$\overline{\text{PV\_E0A\_PIN\_P\_P0\_PRSNT\_B}}$	4, 5
				$\overline{\text{PV\_E0B\_PIN\_P\_P0\_PRSNT\_B}}$	5

1. This bus is ×16 mode only (non-bifurcatible). Thus, there is only one slot clock.
2. A 49.9 Ω pull-down to GND is required on each of the nets of a clock pair whether the bus is used or unused.
3. If this bus is used, include a 3.3 KΩ pull-down resistor to GND. If the bus is not used, this pin should be tied-off with a 3.3 KΩ pull-up resistor to 3.3 V_{AUX}.
4. PERST and PRSNT are 3.3 V tolerant. Pull-ups should be to the same rail as used to power the VSB_V3P3.
5. For PRSNT signals, if the bus goes to a PCIe slot, use a 3.3 KΩ pull-up to 3.3 V_{AUX}. If the bus is wired to a device that is always present, use a 49.9 Ω pull-down resistor to GND. Unused PRSNT signals (such as, PV_E0B_PIN_P_P0_PRSNT_B) are tied-off with a 3.3 KΩ pull-up to 3.3 V_{AUX}.
6. This bus can be bifurcated into the following modes: ×16, ×8 + ×8, or ×8 + ×4 + ×4.

Table 3-4. Chip P0 (Sheet 2 of 2)

Chip	Interface	Mode	Pins		Notes
P0	E1	×8	Data Lanes	Receive: PE_E1_PIN_P_P0_DAT_[00:07]_P/N Transmit: PE_E1_P0_P_PIN_DAT_[00:07]_P/N	
			Clocks	PV_E1A_P0_P_PIN_SLOT_CLK_P/N	2
			Reset	$\overline{\text{PV\_E1A\_P0\_P\_PIN\_PERST\_B}}$	3, 4
			Present	$\overline{\text{PV\_E1A\_PIN\_P\_P0\_PRSNT\_B}}$	4, 5
P0	E1	×8	Data Lanes	Receive: PE_E1_PIN_P_P0_DAT_[08:15] Transmit: PE_E1_P0_P_PIN_DAT_[08:15]	
			Clocks	PV_E1B_P0_P_PIN_SLOT_CLK_P/N	2
			Reset	$\overline{\text{PV\_E1B\_P0\_P\_PIN\_PERST\_B}}$	3, 4
			Present	$\overline{\text{PV\_E1B\_PIN\_P\_P0\_PRSNT\_B}}$	4, 5
P0	E2	×16	Data Lanes	Receive: PE_E2_PIN_P_P0_DAT_[00:15]_P/N Transmit: PE_E2_P0_P_PIN_DAT_[00:15]_P/N	6
			Clocks	PV_E2A_P0_P_PIN_SLOT_CLK_P/N PV_E2B_P0_P_PIN_SLOT_CLK_P/N PV_E2C_P0_P_PIN_SLOT_CLK_P/N	2
			Reset	PV_E2A_P0_P_PIN_PERST_B PV_E2B_P0_P_PIN_PERST_B PV_E2C_P0_P_PIN_PERST_B	3, 4
			Present	PV_E2A_PIN_P_P0_PRSNT_B PV_E2B_PIN_P_P0_PRSNT_B PV_E2C_PIN_P_P0_PRSNT_B	4, 5

1. This bus is ×16 mode only (non-bifurcatible). Thus, there is only one slot clock.
2. A 49.9 Ω pull-down to GND is required on each of the nets of a clock pair whether the bus is used or unused.
3. If this bus is used, include a 3.3 KΩ pull-down resistor to GND. If the bus is not used, this pin should be tied-off with a 3.3 KΩ pull-up resistor to 3.3 V_{AUX}.
4. PERST and PRSNT are 3.3 V tolerant. Pull-ups should be to the same rail as used to power the VSB_V3P3.
5. For PRSNT signals, if the bus goes to a PCIe slot, use a 3.3 KΩ pull-up to 3.3 V_{AUX}. If the bus is wired to a device that is always present, use a 49.9 Ω pull-down resistor to GND. Unused PRSNT signals (such as, PV_E0B_PIN_P_P0_PRSNT_B) are tied-off with a 3.3 KΩ pull-up to 3.3 V_{AUX}.
6. This bus can be bifurcated into the following modes: ×16, ×8 + ×8, or ×8 + ×4 + ×4.

3.4 DDR4 Interface

The POWER9 processor incorporates DDR PHY memory interface physical units capable of supporting several memory topologies. It is optimized for DDR4 memories, as defined by the JEDEC, and incorporates all of the required features and many optional ones.

At a high level, the DDR unit is responsible for:

- Transporting and mapping command, control, address, and data signals presented from the embedded memory controller.
- Providing all necessary configuration registers, state machines, control logic, and status monitoring to execute all required DDR calibration functions (that is, read calibration, fine and coarse write leveling, ZQ calibration, and so on).
- Providing elastic interface style FIFOs (PHYs) for purposes of sampling, de-skewing, bit aligning incoming data, buffering, and launching outgoing data. These FIFOs also assist in crossing clock domains.

Each DDR unit is self-contained and consists of four independent ports that connect to DIMM slots. This unit is replicated twice on the POWER9 processor to provide a maximum of eight ports.

The DDR PHY supports the following memory devices on each port.

- DDR4 RDIMMs and DDR4 LRDIMMs, including 3D stacks up to eight high
- DRAM data widths of ×4 and ×8
- DRAM densities of 4 Gb, 8 Gb, 12 Gb, and 16 Gb
- One or two DIMMs per port
- DRAM speeds of 1866, 2133, 2400, and 2666 Mbps

To accommodate DRAM timing variability, and POWER9 process, voltage, and temperature corners, the DDR PHY implements the following calibration sequences:

- Write leveling
- DQS alignment
- Read clock alignment
- Read centering
- Write centering
- Coarse write alignment
- Coarse read alignment
- TX output impedance calibration

To accommodate voltage and temperature drifts, DQS alignment, read clock alignment, and read centering can be run periodically after the initial calibrations.

The DDR PHY on the POWER9 processor supports two ranks per DIMM, and enables rank-switching in three memory clock cycles or fewer, depending on the speed of operation and device type. The maximum DDR PHY read latency is five memory cycles.

To support DDR4 JEDEC specifications above speeds of 2400 Mbps, the following features are supported:

- Programmable preamble
- CRC support
- RX V_{REF} training

Other features include:

- Per buffer addressability mode (PBA)
- Per DRAM addressability mode (PDA)
- DDR4 maximum power-saving mode
- Per-bit tuning on all address, command, control, clock, data, and strobe signals
- Programmable output impedance and slew rates
- Rank grouping feature
- Extensive RAS support
- Power-down modes
- Custom calibration modes to support custom calibration patterns

3.5 Inter-Node SMP X Bus

The POWER9 processor brings out one X-bus link on the Sforza SCM. The X-bus link connects up to two POWER9 processor chips in a system. The X-bus link carries both coherency traffic and data and is inter-changeable as an inter-group processor link.

The differential X bus contains two clock groups. Each clock group consists of one clock, 16 data lanes, and one spare data lane. Both clock groups must be connected to the same processor. The X bus runs at 16 Gbps. Peak bandwidth is 60 GBps per link with a peak data bandwidth of 48 GBps due to CRC.

Note: CLK Group A within each bus must always connect to CLK Group A on another processor. Never connect CLK Group A to CLK Group B.

3.6 CAPI

The coherent accelerator processor interface (CAPI) allows an FPGA or ASIC accelerator to connect coherently to the POWER9 processor SMP interconnect via the PCIe interface.

4. Power Management

The POWER9 processor chip uses several traditional power-saving techniques to reduce peak power and thermal design-point (TDP) power. For example, latches and arrays are clock gated[1] when they are not required. Also, individual cores or full-core chiplets are dynamically power gated[2] when the cores are not in use.

The POWER9 processor uses adaptive power management techniques to reduce average power. These techniques, collectively known as IBM EnergyScale™, proactively take advantage of variations in workload, environmental condition, and overall system utilization. Coupled with a policy direction from the customer and feedback from the hypervisor or operating system that is running on the machine, this is used to determine modes of operation and the best power and performance trade-off to implement during runtime to meet customer goals and achieve the best possible performance.

4.1 Power Gating and On-Chip, Per-Core Voltage Regulation

Offering competitive chip and system designs requires the capability to dynamically adjust power consumption and performance levels to meet the needs of changing workloads. The POWER9 processor offers industry-leading features to achieve this goal.

During idle periods, each chiplet can individually power gate or “turn off” the supply to either the core or to both the core and the associated L3 cache region to reduce chiplet idle power. The gating header in the POWER9 processor is driven to an elevated voltage when off by using an on-chip charge pump. This technique increases the leakage power reduction, bringing the total DC power reduction achieved by power gating to 50 - 100x. As a result, the power-gated power consumption is less than 1% of the chiplet idle power.

Power gating can also be used to virtually eliminate the parasitic leakage power of deconfigured cores in a partial-good product offering by leaving the headers for unconfigured cores in an always gated state.

The idle power saved by power gating can be used to boost the frequency of the remaining operational cores. Using this technique, the base frequency of operating four cores can exceed the 12-core operating frequency by almost 30%.

4.2 Efficient Power Supply Oversubscription Capability

System bulk power supplies redundantly deliver worst-case power, which is significantly more power than is typically consumed. Typical workloads, parts, and environments use much less power than the worst case. Also, power delivery failure is very uncommon.

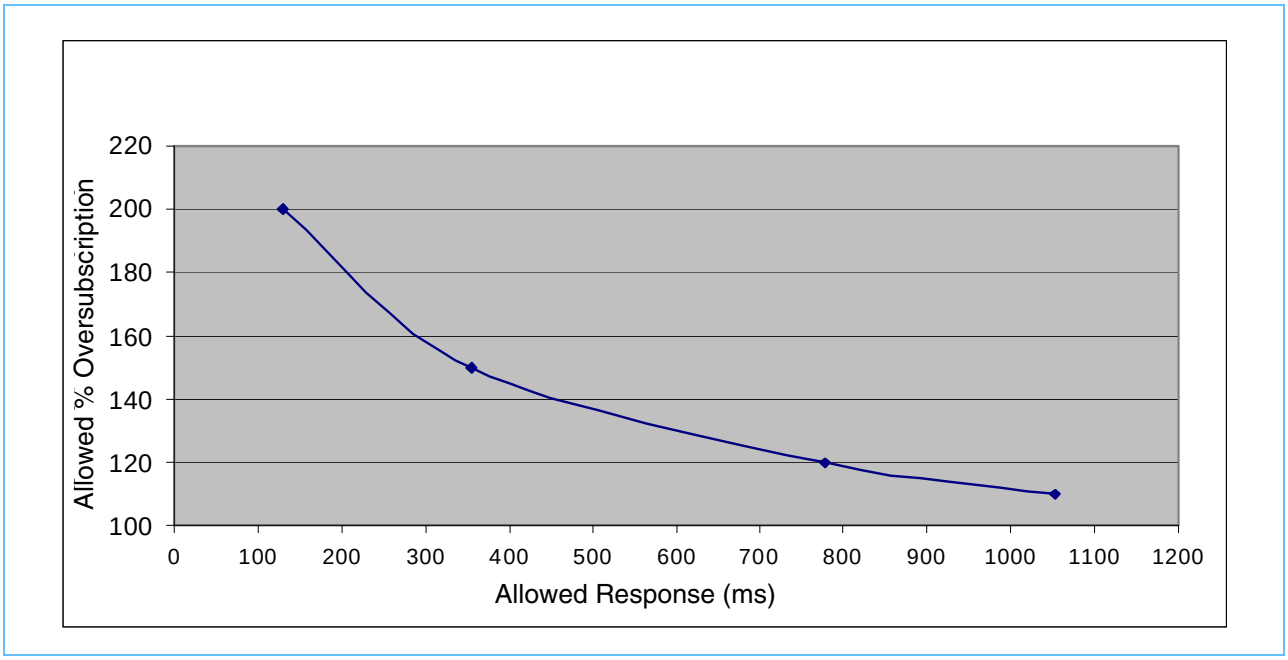
This excess power capacity can be converted into performance by using oversubscription. By oversubscribing the power supply, the processor is allowed to run at voltages and frequencies that exceed the power limit of the system under a worst-case workload and with failure of one of the redundant supplies.

Robust system operation must be maintained in spite of oversubscription. To do this, the processor must be able to throttle back power quickly enough to avoid an overcurrent condition in the remaining bulk power supply in case of a failure in the redundant supply or a sudden power spike.

1. Clock gating involves deactivating clocks for portions of a circuit that are not in use.
2. Power gating involves turning off the current to portions of a circuit that are not in use.

POWER9 systems increase oversubscription capabilities to 1.5x resulting in performance gains. The fundamental limit to power supply oversubscription is the circuit breakers in the utility or UPS when the redundant power fails. The system must be able to throttle back to consuming power less than the non-oversubscribed limit before the EXP(Current) × Time limit of the breaker is violated. *Figure 4-1* shows a representative curve of allowed oversubscription versus response time.

Figure 4-1. Oversubscriptions versus Response Time



To improve response time, a dedicated C4 pin directly signals a power-supply error to the on-chip controller (OCC).

The OCC engine can then use its internal power-actuation capabilities to rapidly reduce power. The POWER9 processor offers the following forms of power reduction:

- The OCC can force a halt in the fetch or issue of instructions to significantly reduce AC power within approximately 10 cycles.
- The OCC can use the DPLL to reduce frequency at a rate of approximately 25 MHz/µs. The AC power reduces linearly with the frequency reduction.

Using these capabilities, the POWER9 processor can reduce its power consumption in less than 5 ms after receiving the system signal indicating a power-supply failure.

The other key to enabling significant oversubscription is rapid detection of a power supply failure.

4.3 Chip Hardware Power-Management Features

4.3.1 Chiplet Voltage Control

The POWER9 processor supports several voltage regulator module (VRM) control mechanisms for multiple system configurations. The core chiplets are on a separate voltage plane than the other Nest components of the chip. The chip-level power-management control (PMC) macro and the OCC are, in combination, programmable to support these configurations.

Core chiplets all share the same voltage plane and must run with the “highest common denominator,” which means that the core demanding the highest voltage sets the value of the voltage rail. The OCC is responsible for establishing the best frequency and therefore, the voltage bounds based on the workload running, the power/performance efficiency policy selected by the customer, and the system budgets established by the thermal management component.

4.4 System Power Sequencing

The rails in *Table 4-1* must be enabled before main system power is turned on.

Table 4-1. System Standby/Auxiliary Power Sequence

Voltage Domain	Delta Time (ms)	Comments
VSB_1P10	0.1 - 20	
VSB0_3P30, VSB1_3P30	0.1 - 20	Connect VSB0_3P30 and VSB1_3P30 to the same voltage rail.

The power sequencing design must check the PGOOD status before continuing to the next step. The sequencer must allow for some amount of minimum time after PGOOD issues before continuing, as specified in *Table 4-2*.

Table 4-2. System Main Power Sequence

Voltage Domain	Delta Time (ms)	Comments
Typically, system rails associated with service processors, I/O, and storage are enabled before the processor/memory power is enabled. This guide does not cover these specifics.		
V_{PP}	0.1 - 20	Must always be greater than V_{DDR}.
V_{DN}	0.1 - 20	
AV_{DD}	0.1 - 20	This voltage can be combined for multiple POWER9 processors.
V_{IO}	0.1 - 20	
POWER9 V_{DD}	0.1 - 20	
POWER9 V_{CS}	0.1 - 20	
Additional processors can be added here in the same sequence or paralleled, so that all V_{DD} come on at the same time followed by all V_{CS}.		
V_{DDR} and V_{TT}	0.1 - 20	Must be less than 200 ms after V_{PP}. V_{TERM} tracks this domain/2 and comes on at the same time.
Notes: 1. Additional V_{PP}/V_{DDR} domains can be added in the same sequence or can be paralleled, so that they all come on together. 2. Deassert the signal to the PV_PRV_PIN_P_P0_STBY_RESET_B pin after PGOOD (SYS_PWROK) is released. It is recommend that the BMC also control the signal on this pin.		

The recommendation for the power-down sequence is the reverse of the power-up sequence. V_{DN} must be brought down after AV_{DD}, V_{IO}, V_{DD}, and V_{CS}.

5. Signals

This section describes the POWER9 signal groups, which are arranged in functional groups according to their interface. *Table 5-1* lists the signal I/O type notation.

Table 5-1. Signal I/O Type Notation

Direction	Signal Type
Rec	Receiver (input).
RecDiff	Receiver differential pair signal polarity (P or N).
Drv	Driver (output).
DrvDiff	Driver differential pair signal polarity (P or N).
AnlgIn	Analog input.
AnlgOut	Analog output.
BiDi	Bi-directional input/output signal.

Table 5-2 lists the buffer types.

Table 5-2. Signal Family Type Notation

Signal	Description
Analog	Analog.
CMOS	CMOS buffers.
EDI	Elastic differential I/O.
OD	Open drain.
PCIe	PCI Express interface signals. These signals are compatible with PCI Express 3.0.

5.1 Pin Naming Convention

The general pin-naming pattern is:

prefix_source_connection type_sink_clock group_Sig Type_bit Number_diffBit_B

Prefix - the type of bus or signal type being connected. The following abbreviations are used:

DM	DDR4 memory
NX	X bus
PE	PCIe
PV	Pervasive
TS	Test

Source and Sink - the specific component and bus being connected. The following abbreviations are used:

E0	PCIe 0 bus
E1	PCIe 1 bus
E2	PCIe 2 bus
X1	X1 bus

Connection Type

P	Point-to-point
B	Bidirectional
M	Multipoint

Clock Group

CKA	Clock group A
CKB	Clock group B

Signal Type (sigType)

CLK	Clock signal
DAT	Data signal

Bit Number - bit strand number, if required; uses padding zeros.
Differential Bit (diffBit) - differential pair signal polarity (P or N), if required.
_B - denotes a negative active signal.

5.2 Signals by Group

5.2.1 Voltage and Ground Signals

Table 5-3 lists the voltage and ground signals.

Table 5-3. Voltage and Ground Signals

Signal	Description	Pin Count
AVDD_1P50	Analog V_{DD} PLL Power	2
DVDD_1P50	Digital V_{DD} PLL Power	2
VCS_0P96	V_{CS}	34
VDD_0P80	V_{DD}	186
VDDR01_1P20, VDDR67_1P20	V_{DDR}	186
VDN_0P70	V_{DN}	103
VIO_1P00	V_{IO}	22
VSB_1P10	V_{SB}	2
VSB0_3P30, VSB1_3P30	V_{SB}	4
GND	Ground	948

5.2.2 APSS Signals

The APSS connections are only used with the first (master) processor of a system to connect to an APSS module. Use of this module is not required.

Signals on the second processor (or if no APSS is present in the system) are left as no connect (N/C); except for the MISO signal, which must be pulled down to GND through a 49.9 Ω resistor if it is unused. *Table 5-4* describes the APSS signals.

Table 5-4. APSS Signals

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
PV_APSS_P0_P_PIN_CS0	OCC SPI Chip Select	APSS	VSB0_3P30	CMOS	Drv	1	1
PV_APSS_P0_P_PIN_CS1	OCC SPI Chip Select	APSS	VSB0_3P30	CMOS	Drv	1	
PV_APSS_P0_P_PIN_MOSI	OCC SPI Master Out Slave In	APSS	VSB0_3P30	CMOS	Drv	1	1
PV_APSS_P0_P_PIN_SCLK	OCC SPI Clock	APSS	VSB0_3P30	CMOS	Drv	1	1
PV_APSS_PIN_P_P0_MISO	OCC SPI Master In Slave Out	APSS	VSB0_3P30	CMOS	Rec	1	2

1. Use a 0 Ω series resistor on the processor side of the net and connect a nopopped 47 pF capacitor to GND at the processor.
2. Use a 0 Ω series resistor on the processor side of the net, a 22 Ω series resistor at the APSS, and connect a nopopped 47 pF capacitor to GND at the processor. If the APSS SPI bus is unused, tie off MISO to GND using a 49.9 Ω resistor; other nets can be N/C.

5.2.3 AVS Signals

Table 5-5 describes the adaptive voltage scaling (AVS) signals. See the *PMBus Specification 1.3* for additional information.

Table 5-5. AVS Signals

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
PV_AVS0_P0_P_PIN_CLK	AVS 0 Clock	AVS	VIO	CMOS	Drv	1	1, 2
PV_AVS0_P0_P_PIN_MDATA	AVS 0 Master Data	AVS	VIO	CMOS	Drv	1	1, 2
PV_AVS0_PIN_P_P0_SDATA	AVS 0 Slave Data	AVS	VIO	CMOS	Rec	1	1, 2
PV_AVS1_P0_P_PIN_CLK	AVS 1 Clock	AVS	VIO	CMOS	Drv	1	1, 2
PV_AVS1_P0_P_PIN_MDATA	AVS 1 Master Data	AVS	VIO	CMOS	Drv	1	1, 2
PV_AVS1_PIN_P_P0_SDATA	AVS 1 Slave Data	AVS	VIO	CMOS	Rec	1	1, 2

1. Series resistor is 0 Ω (on the processor side).
2. Use a nopopped 47 pF capacitor to GND.

5.2.4 FSI Signals

Table 5-6 describes the FSI signals.

Table 5-6. FSI Signals

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
PV_CP1_P0_B_PIN_FSI_DAT	FSI Data Master	FSI	VSB_1P10	CMOS	BiDI	1	1, 2
PV_CP1_P0_P_PIN_FSI_CLK	FSI Clock Master	FSI	VSB_1P10	CMOS	Drv	1	1, 3
PV_FSP0_P0_B_PIN_FSI_DAT	FSI Data Slave	FSI	VSB_1P10	CMOS	BiDI	1	4
PV_FSP0_PIN_P_P0_FSI_CLK	FSI Clock Slave	FSI	VSB_1P10	CMOS	Rec	1	5
PV_PRV_PIN_P_P0_FSI_IN_ENA	FSI Enable	FSI	VSB_1P10	CMOS	Rec	1	6
PV_PRV_PIN_P_P0_FSI_SMD	FSI Secure Mode Disable	FSI	VSB_1P10	CMOS	Rec	1	6

1. Connect from the first CPU socket to the FSI slave port on the second CPU socket.
2. In a single-socket (1S) system, tie to GND with a 49.9 Ω resistor. In a two-socket (2S) system, tie processor #1 to GND with a 40.2 KΩ resistor placed near the socket and tie processor #2 to GND with a 49.9 Ω resistor.
3. N/C if unused (in a single-socket system or the second socket of a two-socket system).
4. For a single-socket system or the first processor of a two-socket system, connect to the BMC using a level translator and the debug connector through a mux (see the CRB for implementation details). Also, include a nopopped 3 KΩ pull-up to 1.1 V_{AUX} placed near the first processor. For the second processor, connect back to the FSI Master data port of the first processor and include a nopopped 3 KΩ pull-up to 1.1 V_{AUX} placed near the slave processor.
5. For a single-socket system or the first processor of a two-socket system, connect to the BMC using a level translator and the debug connector through a mux (see the CRB for implementation details). Place a nopopped 15 KΩ pull-down to GND near the first processor. For the second processor, connect back to the FSI Master clock on the first processor, and place a nopopped 15 KΩ pull-down resistor to GND near the slave processor.
6. Pull-up to 1.1 V_{AUX} using a 50 Ω resistor.

5.2.5 Clock System Signals

Table 5-7 lists the clock system signals.

Table 5-7. Clock System Signals

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
PV_SYS0_PIN_P_P0_REFCLK_N	System 133 MHz Reference Clock In	Clock System	VIO	CMOS	RecDiff	1	1
PV_SYS0_PIN_P_P0_REFCLK_P	System 133 MHz Reference Clock In	Clock System	VIO	CMOS	RecDiff	1	1
PV_PCI0_PIN_P_P0_REFCLK_N	PCIe 100 MHz Input Clock	Clock PCIe	VIO	PCIe	RecDiff	1	2
PV_PCI0_PIN_P_P0_REFCLK_P	PCIe 100 MHz Input Clock	Clock PCIe	VIO	PCIe	RecDiff	1	2

1. This REFCLK can use spread spectrum.
2. This REFCLK cannot use spread spectrum.

5.2.6 I²C Signals

Table 5-8 lists the I²C signals.

Table 5-8. I²C Signals

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
PV_LP_P0_B_PIN_I2C_SCL_B	LightPath I²C Serial Clock	I2C	VSB0_3P30	OD	BiDi	1	1, 2
PV_LP_P0_B_PIN_I2C_SDA_B	LightPath I²C Serial Clock	I2C	VSB0_3P30	OD	BiDi	1	1, 2
PV_PCI_P0_B_PIN_I2C_SCL_B	Hotplug PCI I²C Serial Clock	I2C	VSB0_3P30	OD	BiDi	1	1, 2
PV_PCI_P0_B_PIN_I2C_SDA_B	Hotplug PCI I²C Serial Clock	I2C	VSB0_3P30	OD	BiDi	1	1, 2

1. If the port is unused, tie off with a pull-down to GND through a 49.9 Ω resistor.
2. Signal is an I²C master.

5.2.7 X-Bus Signals

Table 5-9 lists the X-bus signals.

Table 5-9. X-Bus Signals

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
NX_X1_P0_P_PIN_CKA_CLK_N	X Bus 1 Clock A Output	X Bus	VIO	EDI	DrvDiff	1	
NX_X1_P0_P_PIN_CKA_CLK_P	X Bus 1 Clock A Output	X Bus	VIO	EDI	DrvDiff	1	
NX_X1_P0_P_PIN_CKA_DAT_[00:16]_N	X Bus 1 Clock Group A Data Output	X Bus	VIO	EDI	DrvDiff	17	
NX_X1_P0_P_PIN_CKA_DAT_[00:16]_P	X Bus 1 Clock Group A Data Output	X Bus	VIO	EDI	DrvDiff	17	
NX_X1_P0_P_PIN_CKB_CLK_N	X Bus 1 Clock B Output	X Bus	VIO	EDI	DrvDiff	1	
NX_X1_P0_P_PIN_CKB_CLK_P	X Bus 1 Clock B Output	X Bus	VIO	EDI	DrvDiff	1	
NX_X1_P0_P_PIN_CKB_DAT_[00:16]_N	X Bus 1 Clock Group B Data Output	X Bus	VIO	EDI	DrvDiff	17	
NX_X1_P0_P_PIN_CKB_DAT_[00:16]_P	X Bus 1 Clock Group B Data Output	X Bus	VIO	EDI	DrvDiff	17	
NX_X1_PIN_P_P0_CKA_CLK_N	X Bus 1 Clock A Input	X Bus	VIO	EDI	RecDiff	1	
NX_X1_PIN_P_P0_CKA_CLK_P	X Bus 1 Clock A Input	X Bus	VIO	EDI	RecDiff	1	
NX_X1_PIN_P_P0_CKA_DAT_[00:16]_N	X Bus 1 Clock Group A Data Input	X Bus	VIO	EDI	RecDiff	17	
NX_X1_PIN_P_P0_CKA_DAT_[00:16]_P	X Bus 1 Clock Group A Data Input	X Bus	VIO	EDI	RecDiff	17	
NX_X1_PIN_P_P0_CKB_CLK_N	X Bus 1 Clock B Input	X Bus	VIO	EDI	RecDiff	1	
NX_X1_PIN_P_P0_CKB_CLK_P	X Bus 1 Clock B Input	X Bus	VIO	EDI	RecDiff	1	
NX_X1_PIN_P_P0_CKB_DAT_[00:16]_N	X Bus 1 Clock Group B Data Input	X Bus	VIO	EDI	RecDiff	17	
NX_X1_PIN_P_P0_CKB_DAT_[00:16]_P	X Bus 1 Clock Group B Data Input	X Bus	VIO	EDI	RecDiff	17	
PV_X1TX_P0_P_PIN_TERMREF_N	X Bus 1 Terminal Reference Negative	X Bus	Analog	Analog	Analogin	1	1
PV_X1TX_P0_P_PIN_TERMREF_P	X Bus 1 Terminal Reference Positive	X Bus	Analog	Analog	Analogin	1	1
TS_X1RXA_P0_P_PIN_ATST	X Bus 1 Analog Test	X Bus	Analog	Analog		1	2
TS_X1RXA_P0_P_PIN_HFC_N	X Bus 1 High Frequency Characterization	X Bus	VIO			1	2
TS_X1RXA_P0_P_PIN_HFC_P	X Bus 1 High Frequency Characterization	X Bus	VIO			1	2

1. TERMREF value is 169 Ω, 0.1%. For the external resistor value, a 0.1% tolerance is preferred, but a 1% tolerance is acceptable.
2. These nets are unused (N/C).

5.2.8 PCIe Controller and Clock Signals

Table 5-10 lists the PCIe controller and clock bus signals.

Table 5-10. PCIe Controller and Clock Bus Signals (Sheet 1 of 2)

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
PE_E0_P0_P_PIN_DAT_[00:15]_N	PCIe Controller 0 Data Output	PCIe	VIO	PCIe	DrvDiff	16	1
PE_E0_P0_P_PIN_DAT_[00:15]_P	PCIe Controller 0 Data Output	PCIe	VIO	PCIe	DrvDiff	16	1
PE_E0_PIN_P_P0_DAT_[00:15]_N	PCIe Controller 0 Data Input	PCIe	VIO	PCIe	RecDiff	16	1
PE_E0_PIN_P_P0_DAT_[00:15]_P	PCIe Controller 0 Data Input	PCIe	VIO	PCIe	RecDiff	16	1
PE_E1_P0_P_PIN_DAT_[00:15]_N	PCIe Controller 1 Data Output	PCIe	VIO	PCIe	DrvDiff	16	
PE_E1_P0_P_PIN_DAT_[00:15]_P	PCIe Controller 1 Data Output	PCIe	VIO	PCIe	DrvDiff	16	
PE_E1_PIN_P_P0_DAT_[00:15]_N	PCIe Controller 1 Data Input	PCIe	VIO	PCIe	RecDiff	16	
PE_E1_PIN_P_P0_DAT_[00:15]_P	PCIe Controller 1 Data Input	PCIe	VIO	PCIe	RecDiff	16	
PE_E2_P0_P_PIN_DAT_[00:15]_N	PCIe Controller 2 Data Output	PCIe	VIO	PCIe	DrvDiff	16	
PE_E2_P0_P_PIN_DAT_[00:15]_P	PCIe Controller 2 Data Output	PCIe	VIO	PCIe	DrvDiff	16	
PE_E2_PIN_P_P0_DAT_[00:15]_N	PCIe Controller 2 Data Input	PCIe	VIO	PCIe	RecDiff	16	
PE_E2_PIN_P_P0_DAT_[00:15]_P	PCIe Controller 2 Data Input	PCIe	VIO	PCIe	RecDiff	16	
PV_E0_P0_P_PIN_PERST_B	PCIe Controller 0 Reset Output	PCIe	VSB0_3P30	OD	Drv	1	2
PV_E1A_P0_P_PIN_PERST_B	PCIe Controller 1A Reset Output	PCIe	VSB0_3P30	OD	Drv	1	2
PV_E1B_P0_P_PIN_PERST_B	PCIe Controller 1B Reset Output	PCIe	VSB0_3P30	OD	Drv	1	2
PV_E2A_P0_P_PIN_PERST_B	PCIe Controller 2A Reset Output	PCIe	VSB0_3P30	OD	Drv	1	2
PV_E2B_P0_P_PIN_PERST_B	PCIe Controller 2B Reset Output	PCIe	VSB0_3P30	OD	Drv	1	2
PV_E2C_P0_P_PIN_PERST_B	PCIe Controller 2C Reset Output	PCIe	VSB0_3P30	OD	Drv	1	2
PV_E0A_PIN_P_P0_PRSNT_B	PCIe Controller 0A Present Input	PCIe	VSB0_3P30	OD	Rec	1	2
PV_E0B_PIN_P_P0_PRSNT_B	PCIe Controller 0B Present Input	PCIe	VSB0_3P30	OD	Rec	1	2, 3
PV_E1A_PIN_P_P0_PRSNT_B	PCIe Controller 1A Present Input	PCIe	VSB0_3P30	OD	Rec	1	2
PV_E1B_PIN_P_P0_PRSNT_B	PCIe Controller 1B Present Input	PCIe	VSB0_3P30	OD	Rec	1	2
PV_E2A_PIN_P_P0_PRSNT_B	PCIe Controller 2A Present Input	PCIe	VSB0_3P30	OD	Rec	1	2
PV_E2B_PIN_P_P0_PRSNT_B	PCIe Controller 2B Present Input	PCIe	VSB0_3P30	OD	Rec	1	2
PV_E2C_PIN_P_P0_PRSNT_B	PCIe Controller 2C Present Input	PCIe	VSB0_3P30	OD	Rec	1	2
PV_E0_P0_P_PIN_SLOT_CLK_N	PCIe Controller 0 Clock Output	PCIe	VIO	PCIe	DrvDiff	1	2
PV_E0_P0_P_PIN_SLOT_CLK_P	PCIe Controller 0 Clock Output	PCIe	VIO	PCIe	DrvDiff	1	2
PV_E1A_P0_P_PIN_SLOT_CLK_N	PCIe Controller 1A Clock Output	PCIe	VIO	PCIe	DrvDiff	1	2
PV_E1A_P0_P_PIN_SLOT_CLK_P	PCIe Controller 1A Clock Output	PCIe	VIO	PCIe	DrvDiff	1	2

1. The E0 bus is not bifurcatable.
2. See *Section 3.3.4* on page 24 for additional information on CLOCK, PERST, and PRSNT connectivity.
3. This input is not used and cannot be N/C. Tie off with a 3.3 KΩ pull-up to 3.3 V_{AUX}.
4. TERMREF must have a 200 Ω, 0.1% resistor between the P and N legs.
5. ATST nets are unused, N/C.

Table 5-10. PCIe Controller and Clock Bus Signals (Sheet 2 of 2)

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
PV_E1B_P0_P_PIN_SLOT_CLK_N	PCIe Controller 1B Clock Output	PCIe	VIO	PCIe	DrvDiff	1	2
PV_E1B_P0_P_PIN_SLOT_CLK_P	PCIe Controller 1B Clock Output	PCIe	VIO	PCIe	DrvDiff	1	2
PV_E2A_P0_P_PIN_SLOT_CLK_N	PCIe Controller 2A Clock Output	PCIe	VIO	PCIe	DrvDiff	1	2
PV_E2A_P0_P_PIN_SLOT_CLK_P	PCIe Controller 2A Clock Output	PCIe	VIO	PCIe	DrvDiff	1	2
PV_E2B_P0_P_PIN_SLOT_CLK_N	PCIe Controller 2B Clock Output	PCIe	VIO	PCIe	DrvDiff	1	2
PV_E2B_P0_P_PIN_SLOT_CLK_P	PCIe Controller 2B Clock Output	PCIe	VIO	PCIe	DrvDiff	1	2
PV_E2C_P0_P_PIN_SLOT_CLK_N	PCIe Controller 2C Clock Output	PCIe	VIO	PCIe	DrvDiff	1	2
PV_E2C_P0_P_PIN_SLOT_CLK_P	PCIe Controller 2C Clock Output	PCIe	VIO	PCIe	DrvDiff	1	2
PV_E0_P0_P_PIN_TERMREF_N	PCIe Controller 0 Terminal Reference	PCIe	Analog			1	4
PV_E0_P0_P_PIN_TERMREF_P	PCIe Controller 0 Terminal Reference	PCIe	Analog			1	4
PV_E1_P0_P_PIN_TERMREF_N	PCIe Controller 1 Terminal Reference	PCIe	Analog			1	4
PV_E1_P0_P_PIN_TERMREF_P	PCIe Controller 1 Terminal Reference	PCIe	Analog			1	4
PV_E2_P0_P_PIN_TERMREF_N	PCIe Controller 2C Clock Output	PCIe	Analog			1	4
PV_E2_P0_P_PIN_TERMREF_P	PCIe Controller 2C Clock Output	PCIe	Analog			1	4
TS_E0_P0_P_PIN_ATST	PCIe Controller 0 Analog Test Output	PCIe	Analog				5
TS_E1_P0_P_PIN_ATST	PCIe Controller 0 Analog Test Output	PCIe	Analog				5
TS_E2_P0_P_PIN_ATST	PCIe Controller 0 Analog Test Output	PCIe	Analog				5

1. The E0 bus is not bifurcatable.
2. See *Section 3.3.4* on page 24 for additional information on CLOCK, PERST, and PRSNT connectivity.
3. This input is not used and cannot be N/C. Tie off with a 3.3 KΩ pull-up to 3.3 V_{AUX}.
4. TERMREF must have a 200 Ω, 0.1% resistor between the P and N legs.
5. ATST nets are unused, N/C.

5.2.9 LPC Bus Signals

Table 5-11 lists the LPC bus signals.

Table 5-11. LPC Bus Signals

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
PV_PRV_P0_B_PIN_LPC_DAT_[0:3]	LPC Data 0 - 3	LPC	VSB0_3P30		BiDi	4	1
PV_PRV_P0_P_PIN_LPC_FRAME_B	LPC Frame Output	LPC	VSB0_3P30		Drv	1	2
PV_PRV_P0_P_PIN_LPC_RESET_B	LPC Reset Output	LPC	VSB0_3P30		BiDi	1	3
PV_PRV_PIN_P_P0_LPC_CLK	LPC 33 MHz Clock Input	LPC	VIO	CMOS	Rec	1	4
PV_PRV_PIN_P_P0_LPC_IRQ	LPC Interrupt BiDi	LPC	VSB0_3P30		Rec	1	5

1. For the first processor of a two-socket system, connect to the BMC through a 22 Ω series resistor placed at the CPU and a 33 Ω series resistor placed at the BMC. N/C for the second processor.
2. For the first processor of a two-socket system, connect to the BMC through a 22 Ω series resistor placed at the CPU. N/C for the second processor.
3. The first processor requires a 3.3 KΩ pull-up resistor to 3.3 V_{AUX}. IBM suggests a 10 nF cap to GND for noise. For the second processor of a two-socket system, tie off with a 49.9 Ω pull-up resistor to 3.3 V_{AUX}.
4. V_{MAX} is 1.26 V for this pin; a voltage divider might be required depending on the clock driver used. For the second processor of a two-socket system, tie off with 49.9 Ω pull-down resistor to GND.
5. For the first processor of a two-socket system, connect to the BMC through a 22 Ω series resistor placed at the processor and a 33 Ω series resistor placed at the BMC. For the second processor, tie off with a 49.9 Ω pull-up resistor to 3.3 V_{AUX}.

5.2.10 Memory Signals

Table 5-12 lists the memory signals.

Table 5-12. Memory Signals (Sheet 1 of 5)

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
DM_DDR0_BI_DQ_[0:71]	DDR Port0 Data Query	Memory	VDDR01			72	
DM_DDR0_BI_DQS_[00:17]_N	DDR Port0 Data Query Strobe	Memory	VDDR01			18	
DM_DDR0_BI_DQS_[00:17]_P	DDR Port0 Data Query Strobe	Memory	VDDR01			18	
DM_DDR0_P0_P_PIN_ACT_B	DDR Port 0 Address and Command	Memory	VDDR01			1	
DM_DDR0_P0_P_PIN_ADDR_[00:17]	DDR Port 0 Address and Command	Memory	VDDR01			18	
DM_DDR0_P0_P_PIN_BANK_ADR_[0:1]	DDR Port 0 Address and Command	Memory	VDDR01			2	

1. CKE[2:3] are N/C for single drop DIMMs.
2. This signal is N/C for single-drop DIMMs.
3. CS_B_[2:3] are N/C for single-drop DIMMs.
4. ODT_[2:3] are N/C for single-drop DIMMs.
5. Requires a 1 KΩ pull-down to GND. IBM also recommends a 1nF capacitor to GND for noise reduction.
6. Requires a 1 KΩ pull-up to V_{DDR}.
7. Each TERMREF requires a 240 Ω, 0.1% resistor connected between the P and N legs.
8. This signal is N/C; unused in the system.
9. All memory I^2C nets require a 1 KΩ pull-up to 2.5 V_{AUX}.

Table 5-12. Memory Signals (Sheet 2 of 5)

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
DM_DDR0_P0_P_PIN_BANK_GRP_[0:1]	DDR Port 0 Address and Command	Memory	VDDR01			2	
DM_DDR0_P0_P_PIN_CHIPID_[0:2]	DDR Port 0 Address and Command	Memory	VDDR01			3	
DM_DDR0_P0_P_PIN_CKE_[0:3]	DDR Port0 Control	Memory	VDDR01			4	1
DM_DDR0_P0_P_PIN_CLK_0_N	DDR Port 0 DIMM Clock	Memory	VDDR01			1	
DM_DDR0_P0_P_PIN_CLK_0_P	DDR Port 0 DIMM Clock	Memory	VDDR01			1	
DM_DDR0_P0_P_PIN_CLK_1_N	DDR Port 0 DIMM Clock	Memory	VDDR01			1	2
DM_DDR0_P0_P_PIN_CLK_1_P	DDR Port 0 DIMM Clock	Memory	VDDR01			1	2
DM_DDR0_P0_P_PIN_CS_B_[0:3]	DDR Port 0 Control	Memory	VDDR01			4	3
DM_DDR0_P0_P_PIN_ODT_[0:3]	DDR Port 0 Control	Memory	VDDR01			4	4
DM_DDR0_P0_P_PIN_PAR	DDR Port 0 Address and Command	Memory	VDDR01			1	
DM_DDR0_P0_P_PIN_RESET_B	DDR Port 0 Address and Command	Memory	VDDR01			1	5
DM_DDR0_PIN_P_P0_ERR_B	DDR Port 0 Address and Command	Memory	VDDR01			1	6
DM_DDR0_PIN_P_P0_EVENT_B	DDR Port 0 Address and Command	Memory	VDDR01			1	6
DM_DDR1_BI_DQ_[00:71]	DDR Port1 Data Query Signal	Memory	VDDR01			72	
DM_DDR1_BI_DQS_[00:17]_N	DDR Port1 Data Query Strobe	Memory	VDDR01			18	
DM_DDR1_BI_DQS_[00:17]_P	DDR Port1 Data Query Strobe	Memory	VDDR01			18	
DM_DDR1_P0_P_PIN_ACT_B	DDR Port1 Address and Command	Memory	VDDR01			1	
DM_DDR1_P0_P_PIN_ADDR_[00:17]	DDR Port1 Address and Command	Memory	VDDR01			18	
DM_DDR1_P0_P_PIN_BANK_ADR_[0:1]	DDR Port1 Address and Command	Memory	VDDR01			2	
DM_DDR1_P0_P_PIN_BANK_GRP_[0:1]	DDR Port1 Address and Command	Memory	VDDR01			2	
DM_DDR1_P0_P_PIN_CHIPID_[0:2]	DDR Port1 Address and Command	Memory	VDDR01			3	

1. CKE[2:3] are N/C for single drop DIMMs.
2. This signal is N/C for single-drop DIMMs.
3. CS_B_[2:3] are N/C for single-drop DIMMs.
4. ODT_[2:3] are N/C for single-drop DIMMs.
5. Requires a 1 KΩ pull-down to GND. IBM also recommends a 1nF capacitor to GND for noise reduction.
6. Requires a 1 KΩ pull-up to V_{DDR}.
7. Each TERMREF requires a 240 Ω, 0.1% resistor connected between the P and N legs.
8. This signal is N/C; unused in the system.
9. All memory I^2C nets require a 1 KΩ pull-up to 2.5 V_{AUX}.

Table 5-12. Memory Signals (Sheet 3 of 5)

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
DM_DDR1_P0_P_PIN_CKE_[0:3]	DDR Port1 Control	Memory	VDDR01			4	1
DM_DDR1_P0_P_PIN_CLK_0_N	DDR Port1 DIMM Clock	Memory	VDDR01			1	
DM_DDR1_P0_P_PIN_CLK_0_P	DDR Port1 DIMM Clock	Memory	VDDR01			1	
DM_DDR1_P0_P_PIN_CLK_1_N	DDR Port1 DIMM Clock	Memory	VDDR01			1	2
DM_DDR1_P0_P_PIN_CLK_1_P	DDR Port1 DIMM Clock	Memory	VDDR01			1	2
DM_DDR1_P0_P_PIN_CS_B_[0:3]	DDR Port1 Control	Memory	VDDR01			4	3
DM_DDR1_P0_P_PIN_ODT_[0:3]	DDR Port1 Control	Memory	VDDR01			4	4
DM_DDR1_P0_P_PIN_PAR	DDR Port1 Address and Command	Memory	VDDR01			1	
DM_DDR1_P0_P_PIN_RESET_B	DDR Port1 Address and Command	Memory	VDDR01			1	5
DM_DDR1_PIN_P_P0_ERR_B	DDR Port1 Address and Command	Memory	VDDR01			1	6
DM_DDR1_PIN_P_P0_EVENT_B	DDR Port1 Address and Command	Memory	VDDR01			1	6
DM_DDR6_BI_DQ_[00:71]	DDR Port6 Data Query Signal	Memory	VDDR67			72	
DM_DDR6_BI_DQS_[00:17]_N	DDR Port6 Data Query Strobe	Memory	VDDR67			18	
DM_DDR6_BI_DQS_[00:17]_P	DDR Port6 Data Query Strobe	Memory	VDDR67			18	
DM_DDR6_P0_P_PIN_ACT_B	DDR Port6 Address and Command	Memory	VDDR67			1	
DM_DDR6_P0_P_PIN_ADDR_[00:17]	DDR Port6 Address and Command	Memory	VDDR67			18	
DM_DDR6_P0_P_PIN_BANK_ADR_[0:1]	DDR Port6 Address and Command	Memory	VDDR67			2	
DM_DDR6_P0_P_PIN_BANK_GRP_[0:1]	DDR Port6 Address and Command	Memory	VDDR67			2	
DM_DDR6_P0_P_PIN_CHIPID_[0:2]	DDR Port6 Address and Command	Memory	VDDR67			3	
DM_DDR6_P0_P_PIN_CKE_[0:3]	DDR Port6 Control	Memory	VDDR67			4	1
DM_DDR6_P0_P_PIN_CLK_0_N	DDR Port6 DIMM Clock	Memory	VDDR67			1	
DM_DDR6_P0_P_PIN_CLK_0_P	DDR Port6 DIMM Clock	Memory	VDDR67			1	
DM_DDR6_P0_P_PIN_CLK_1_N	DDR Port6 DIMM Clock	Memory	VDDR67			1	2
DM_DDR6_P0_P_PIN_CLK_1_P	DDR Port6 DIMM Clock	Memory	VDDR67			1	2

1. CKE[2:3] are N/C for single drop DIMMs.
2. This signal is N/C for single-drop DIMMs.
3. CS_B_[2:3] are N/C for single-drop DIMMs.
4. ODT_[2:3] are N/C for single-drop DIMMs.
5. Requires a 1 KΩ pull-down to GND. IBM also recommends a 1nF capacitor to GND for noise reduction.
6. Requires a 1 KΩ pull-up to V_{DDR}.
7. Each TERMREF requires a 240 Ω, 0.1% resistor connected between the P and N legs.
8. This signal is N/C; unused in the system.
9. All memory I^2C nets require a 1 KΩ pull-up to 2.5 V_{AUX}.

Table 5-12. Memory Signals (Sheet 4 of 5)

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
DM_DDR6_P0_P_PIN_CS_B_[0:3]	DDR Port6 Control	Memory	VDDR67			4	3
DM_DDR6_P0_P_PIN_ODT_[0:3]	DDR Port6 Control	Memory	VDDR67			4	4
DM_DDR6_P0_P_PIN_PAR	DDR Port6 Address and Command	Memory	VDDR67			1	
DM_DDR6_P0_P_PIN_RESET_B	DDR Port6 Address and Command	Memory	VDDR67			1	5
DM_DDR6_PIN_P_P0_ERR_B	DDR Port6 Address and Command	Memory	VDDR67			1	6
DM_DDR6_PIN_P_P0_EVENT_B	DDR Port6 Address and Command	Memory	VDDR67			1	6
DM_DDR7_BI_DQ_[00:71]	DDR Port7 Data Query Signal	Memory	VDDR67			72	
DM_DDR7_BI_DQS_[00:17]_N	DDR Port7 Data Query Strobe	Memory	VDDR67			18	
DM_DDR7_BI_DQS_[00:17]_P	DDR Port7 Data Query Strobe	Memory	VDDR67			18	
DM_DDR7_P0_P_PIN_ACT_B	DDR Port7 Address and Command	Memory	VDDR67			1	
DM_DDR7_P0_P_PIN_ADDR_[00:17]	DDR Port7 Address and Command	Memory	VDDR67			18	
DM_DDR7_P0_P_PIN_BANK_ADR_[0:1]	DDR Port7 Address and Command	Memory	VDDR67			2	
DM_DDR7_P0_P_PIN_BANK_GRP_[0:1]	DDR Port7 Address and Command	Memory	VDDR67			2	
DM_DDR7_P0_P_PIN_CHIPID_[0:2]	DDR Port7 Address and Command	Memory	VDDR67			3	
DM_DDR7_P0_P_PIN_CKE_[0:3]	DDR Port7 Control	Memory	VDDR67			4	1
DM_DDR7_P0_P_PIN_CLK_0_N	DDR Port7 DIMM Clock	Memory	VDDR67			1	
DM_DDR7_P0_P_PIN_CLK_0_P	DDR Port7 DIMM Clock	Memory	VDDR67			1	
DM_DDR7_P0_P_PIN_CLK_1_N	DDR Port7 DIMM Clock	Memory	VDDR67			1	2
DM_DDR7_P0_P_PIN_CLK_1_P	DDR Port7 DIMM Clock	Memory	VDDR67			1	2
DM_DDR7_P0_P_PIN_CS_B_[0:3]	DDR Port7 Control	Memory	VDDR67			4	3
DM_DDR7_P0_P_PIN_ODT_[0:3]	DDR Port7 Control	Memory	VDDR67			4	4
DM_DDR7_P0_P_PIN_PAR	DDR Port7 Address and Command	Memory	VDDR67			1	
DM_DDR7_P0_P_PIN_RESET_B	DDR Port7 Address and Command	Memory	VDDR67			1	5

1. CKE[2:3] are N/C for single drop DIMMs.
2. This signal is N/C for single-drop DIMMs.
3. CS_B_[2:3] are N/C for single-drop DIMMs.
4. ODT_[2:3] are N/C for single-drop DIMMs.
5. Requires a 1 KΩ pull-down to GND. IBM also recommends a 1nF capacitor to GND for noise reduction.
6. Requires a 1 KΩ pull-up to V_{DDR}.
7. Each TERMREF requires a 240 Ω, 0.1% resistor connected between the P and N legs.
8. This signal is N/C; unused in the system.
9. All memory I^2C nets require a 1 KΩ pull-up to 2.5 V_{AUX}.

Table 5-12. Memory Signals (Sheet 5 of 5)

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
DM_DDR7_PIN_P_P0_ERR_B	DDR Port7 Address and Command	Memory	VDDR67			1	6
DM_DDR7_PIN_P_P0_EVENT_B	DDR Port7 Address and Command	Memory	VDDR67			1	6
PV_DDR0123_P0_P_PIN_TERMREF_N	DDR0123 Terminal Reference Negative	Memory	Analog			1	7
PV_DDR0123_P0_P_PIN_TERMREF_P	DDR0123 Terminal Reference Positive	Memory	Analog			1	7
PV_DDR4567_P0_P_PIN_TERMREF_N	DDR4567 Terminal Reference Negative	Memory	Analog			1	7
PV_DDR4567_P0_P_PIN_TERMREF_P	DDR4567 Terminal Reference Positive	Memory	Analog			1	7
TS_DDR0123_P0_P_PIN_ATST	DDR0123 Analog Test Output	Memory	Analog			1	8
TS_DDR4567_P0_P_PIN_ATST	DDR4567 Analog Test Output	Memory	Analog			1	8
PV_DDR0123_P0_B_PIN_I2C_SCL_B	DDR0123 I^2C Serial Clock	Memory	VSB0_3P30	OD	BiDi	1	9
PV_DDR0123_P0_B_PIN_I2C_SDA_B	DDR0123 I^2C Serial Data	Memory	VSB0_3P30	OD	BiDi	1	9
PV_DDR4567_P0_B_PIN_I2C_SCL_B	DDR4567 I^2C Serial Clock	Memory	VSB0_3P30	OD	BiDi	1	9
PV_DDR4567_P0_B_PIN_I2C_SDA_B	DDR4567 I^2C Serial Data	Memory	VSB0_3P30	OD	BiDi	1	9

1. CKE[2:3] are N/C for single drop DIMMs.
2. This signal is N/C for single-drop DIMMs.
3. CS_B_[2:3] are N/C for single-drop DIMMs.
4. ODT_[2:3] are N/C for single-drop DIMMs.
5. Requires a 1 KΩ pull-down to GND. IBM also recommends a 1nF capacitor to GND for noise reduction.
6. Requires a 1 KΩ pull-up to V_{DDR}.
7. Each TERMREF requires a 240 Ω, 0.1% resistor connected between the P and N legs.
8. This signal is N/C; unused in the system.
9. All memory I^2C nets require a 1 KΩ pull-up to 2.5 V_{AUX}.

5.2.11 JTAG Signals

Table 5-13 lists the JTAG signals.

Table 5-13. JTAG Signals

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
PV_PRV_P0_P_PIN_ATTENTION_B	OCC Attention Output	JTAG	VSB0_3P30	CMOS	Drv	1	1
TS_JTAG_P0_P_PIN_TDO	Test Data Out	JTAG	VIO	CMOS	Drv	1	2
TS_JTAG_PIN_P_P0_TDI	Test Data In	JTAG	VIO	CMOS	Rec	1	2
TS_JTAG_PIN_P_P0_TMS	Test Mode Select	JTAG	VIO	CMOS	Rec	1	2
TS_JTAG_PIN_P_P0_CARD_TEST	Card Test	JTAG	VSB_1P10	CMOS	Rec	1	3
TS_JTAG_PIN_P_P0_TCK	Test Clock	JTAG	VIO	OD	Rec	1	4

1. For a single-socket system or the first processor of a two-socket system, connect to the BMC with a 4.7 KΩ pull-up to 3.3 V_{AUX} and a 10 nF capacitor to GND at the BMC. For the second processor, this signal is unused, N/C.
2. Signal requires a 2 KΩ pull-up to V_{IO} whether the bus is used or unused.
3. Tie off with a 49.9 Ω pull-down to GND.
4. If the bus is used, the signal requires a 2 KΩ pull-down to GND. If the bus is unused, tie off with a 49.9 Ω pull-down to GND.

5.2.12 Miscellaneous Signals

Table 5-14 lists the miscellaneous signals.

Table 5-14. Miscellaneous Signals (Sheet 1 of 2)

Signal	Description	Interface	I/O Voltage Domain	Family	Pin Count	Type	Notes
SCM_PRESENT_B	SCM Socket Present Signal	Misc			1		1
PV_IVRM_V1_M_P0_VREF_N	iVRM External Voltage Reference	Misc	Analog		1		2
PV_IVRM_V1_M_P0_VREF_P	iVRM External Voltage Reference	Misc	Analog		1		2
PV_PRV_P0_B_PIN_GPIO0	GPIO0	Misc	VSB0_3P30		1	BiDi	3
PV_PRV_P0_B_PIN_GPIO1	GPIO1	Misc	VSB0_3P30		1	BiDi	3
PV_PRV_P0_B_PIN_GPIO2	GPIO2	Misc	VSB0_3P30		1	BiDi	3
PV_PRV_P0_B_PIN_SPARE0	Spare 0	Misc	VSB_1P10	CMOS	1	BiDi	4
PV_PRV_PIN_P_P0_CHIP_MASTER	Chip Master Input	Misc	VSB_1P10	CMOS	1	Rec	5
PV_PRV_PIN_P_P0_STBY_RESET_B	Standby Reset Input	Misc	VSB_1P10	CMOS	1	Rec	6
PV_PRV_PIN_P_P0_VDN_PGOOD	Nest Voltage Power Good Input	Misc	VSB_1P10	CMOS	1	Rec	7
PV_SEEPROM0_P0_B_PIN_I2C_SDA_B	SEEPROM 0 I2C Serial Data	Misc	VSB0_3P30	OD	1	BiDi	8
PV_SEEPROM0_P0_P_PIN_I2C_SCL_B	SEEPROM 0 I2C Serial Clock	Misc	VSB0_3P30	OD	1	BiDi	8
PV_SEEPROM1_P0_B_PIN_I2C_SDA_B	SEEPROM 1 I2C Serial Data	Misc	VSB0_3P30	OD	1	BiDi	8
PV_SEEPROM1_P0_P_PIN_I2C_SCL_B	SEEPROM 1 I2C Serial Clock	Misc	VSB0_3P30	OD	1	BiDi	8
PV_SEEPROM3_P0_B_PIN_I2C_SDA_B	SEEPROM 3 I2C Serial Data	Misc	VSB0_3P30	OD	1	BiDi	8

1. For the Master processor, tie to GND. For additional processors: tie to GND if the processor will always be there or to the BMC for presence detection.
2. Do not connect to anything (N/C).
3. If used, pull up to 3.3 V_{AUX} with a 3.3 KΩ resistor. If not used, tie to GND with a 49.9 Ω resistor.
4. Unused. Tie off with a nopopped 49.9 Ω pull-up to 1.1 V_{AUX} and a populated 49.9 Ω pull-down to GND.
5. For a single-socket system or the first processor of a two-socket system, tie to GND through a 49.9 Ω resistor (this indicates the Master processor). For the second processor, tie to 1.1 V_{AUX} through a 49.9 Ω resistor (this indicates the Slave processor).
6. This signal has a 1 KΩ internal pull-up resistor; add a nopopped 10 KΩ pull-up resistor to 1.1 V_{AUX} on board. IBM recommends a 1 nF - 10 nF capacitor to GND for noise dampening.
7. Requires a 1.2 KΩ pull-up to 1.1 V_{AUX} or must always be actively driven (like an AUC17 gate). IBM recommends a 1 nF capacitor to GND for noise dampening.
8. This signal has an internal pull-up; N/C on the planar.
9. Tie off with a pull down to GND through a 49.9 Ω resistor.
10. Digital thermal sensor analog test output. This pin is used for debug only; leave as N/C on the system board.
11. Throttle signal, active low. This pin can be asserted through hardware in the case of an emergency power down to tell the OCC to go to the power state defined for N mode. Validate the throttle pin use case with your IBM AE. Created from power supply PGOOD signals. Connect using a 1 KΩ series resistor at the processor; also connect to the BMC. No pull-up is required if this signal is always actively driven. Otherwise, pull up with a resistor between 1 - 5 KΩ to 3.3 V_{AUX}. If not using this signal, tie off with a resistor between 1 - 4.7 KΩ to 3.3 V_{AUX}.
12. The first processor requires a 1 KΩ pull-up resistor to V_{IO}; combine with system reset and wire to reset the TPM device. For additional processors or an unused TPM, tie off with a 2 KΩ pull-up to V_{IO}.
13. The first processor requires a pull-up resistor ≤1 KΩ to V_{IO}; wire to the TPM interrupt logic. Note that the actual value of the pull-up might be system-application dependent. For additional processors or an unused TPM, tie off with a 1 KΩ pull-down to GND.

Table 5-14. Miscellaneous Signals (Sheet 2 of 2)

Signal	Description	Interface	I/O Voltage Domain	Family	Pin Count	Type	Notes
PV_SEEPROM3_P0_P_PIN_I2C_SCL_B	SEEPROM 3 I2C Serial Clock	Misc	VSB0_3P30	OD	1	BiDi	8
TS_DTSNPU_P0_P_PIN_TEST_OUT	Digital Thermal Sensor Analog Output	Misc	VDN	Analog	1		10
TS_EFUSE_PIN_P_P0_FSOURCE	Module Test Efuse Source	Misc	Analog	Analog	1	Rec	9
TS_NESTLCPLL_P0_P_PIN_ATST	Nest LC Analog Test	Misc	Analog		1		2
TS_NESTLCPLL_P0_P_PIN_HFC_N	Nest LC PLL High Frequency Characterization	Misc	VIO		1		2
TS_NESTLCPLL_P0_P_PIN_HFC_P	Nest LC PLL High Frequency Characterization	Misc	VIO		1		2
TS_OCC_PIN_P_P0_ALERT_B	OCC Alert Input	Misc	VSB0_3P30		1		11
TS_TST_PIN_P_P0_FORCE_PWR_ON	Force Power On	Misc	VIO	CMOS	1	Rec	9
TS_TST_PIN_P_P0_LSSD_TE	LSSD Test Enable	Misc	VSB_1P10	CMOS	1	Rec	9
PV_TPM_P0_P_PIN_RESET	TPM Reset Output	TPM	VIO	CMOS	1	Drv	12
PV_TPM_PIN_P_P0_INT	TPM Interrupt Input	TPM	VIO	CMOS	1	Rec	13

1. For the Master processor, tie to GND. For additional processors: tie to GND if the processor will always be there or to the BMC for presence detection.
2. Do not connect to anything (N/C).
3. If used, pull up to 3.3 V_{AUX} with a 3.3 KΩ resistor. If not used, tie to GND with a 49.9 Ω resistor.
4. Unused. Tie off with a nopopped 49.9 Ω pull-up to 1.1 V_{AUX} and a populated 49.9 Ω pull-down to GND.
5. For a single-socket system or the first processor of a two-socket system, tie to GND through a 49.9 Ω resistor (this indicates the Master processor). For the second processor, tie to 1.1 V_{AUX} through a 49.9 Ω resistor (this indicates the Slave processor).
6. This signal has a 1 KΩ internal pull-up resistor; add a nopopped 10 KΩ pull-up resistor to 1.1 V_{AUX} on board. IBM recommends a 1 nF - 10 nF capacitor to GND for noise dampening.
7. Requires a 1.2 KΩ pull-up to 1.1 V_{AUX} or must always be actively driven (like an AUC17 gate). IBM recommends a 1 nF capacitor to GND for noise dampening.
8. This signal has an internal pull-up; N/C on the planar.
9. Tie off with a pull down to GND through a 49.9 Ω resistor.
10. Digital thermal sensor analog test output. This pin is used for debug only; leave as N/C on the system board.
11. Throttle signal, active low. This pin can be asserted through hardware in the case of an emergency power down to tell the OCC to go to the power state defined for N mode. Validate the throttle pin use case with your IBM AE. Created from power supply PGOOD signals. Connect using a 1 KΩ series resistor at the processor; also connect to the BMC. No pull-up is required if this signal is always actively driven. Otherwise, pull up with a resistor between 1 - 5 KΩ to 3.3 V_{AUX}. If not using this signal, tie off with a resistor between 1 - 4.7 KΩ to 3.3 V_{AUX}.
12. The first processor requires a 1 KΩ pull-up resistor to V_{IO}; combine with system reset and wire to reset the TPM device. For additional processors or an unused TPM, tie off with a 2 KΩ pull-up to V_{IO}.
13. The first processor requires a pull-up resistor ≤1 KΩ to V_{IO}; wire to the TPM interrupt logic. Note that the actual value of the pull-up might be system-application dependent. For additional processors or an unused TPM, tie off with a 1 KΩ pull-down to GND.

5.2.13 Test Signals

Table 5-15 lists the test signals.

Table 5-15. Test Signals (Sheet 1 of 2)

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
TS_CACHE0001_P0_P_PIN_VDD_ VSENSE	Internal Kelvin Monitors for Characterization Connector	Char	Analog			1	1
TS_CACHE0203_P0_P_PIN_GSENSE	Internal Kelvin Monitors for Characterization Connector	Char	Analog			1	1
TS_CACHE0203_P0_P_PIN_VCS_ VSENSE		Char	Analog			1	1
TS_CLK_P0_P_PIN_PROBE0_N	Characterization Probe 0 Output Negative	Char	VIO			1	1
TS_CLK_P0_P_PIN_PROBE0_P	Characterization Probe 0 Output Positive	Char	VIO			1	1
TS_CLK_P0_P_PIN_PROBE1_N	Characterization Probe 1 Output Negative	Char	VIO			1	1
TS_CLK_P0_P_PIN_PROBE1_P	Characterization Probe 1 Output Positive	Char	VIO			1	1
TS_EQ0_P0_P_PIN_GSENSE		Char	Analog			1	1
TS_EQ0_P0_P_PIN_VDDIN_VSENSE		Char	Analog			1	1
TS_EQ1_P0_P_PIN_VCSIN_VSENSE		Char	Analog			1	1
TS_EQALL_P0_P_PIN_AMUX_GSENSE		Char	Analog			1	1
TS_EQALL_P0_P_PIN_AMUX_VSENSE		Char	Analog			1	1
TS_EX00C0_P0_P_PIN_GSENSE		Char	Analog			1	1
TS_EX00C0_P0_P_PIN_VSENSE		Char	Analog			1	1
TS_EX00C1_P0_P_PIN_GSENSE		Char	Analog			1	1
TS_EX00C1_P0_P_PIN_VSENSE		Char	Analog			1	1
TS_EX01C0_P0_P_PIN_GSENSE		Char	Analog			1	1
TS_EX01C0_P0_P_PIN_VSENSE		Char	Analog			1	1
TS_EX01C1_P0_P_PIN_GSENSE		Char	Analog			1	1
TS_EX01C1_P0_P_PIN_VSENSE		Char	Analog			1	1
TS_EX0203_P0_P_PIN_L3_GSENSE		Char	Analog			1	1
TS_EX0203_P0_P_PIN_VBL_VSENSE		Char	Analog			1	2
TS_EX0203_P0_P_PIN_VPP_VSENSE		Char	Analog			1	2
TS_EX0203_P0_P_PIN_VWL_VSENSE		Char	Analog			1	1
TS_PRV_P0_P_PIN_PROBE2	Characterization Probe 2 Output	Char	VSB_1P10	CMOS	Drv	1	1
TS_PRV_P0_P_PIN_PROBE3	Characterization Probe 3 Output	Char	VSB_1P10	CMOS	Drv	1	1

1. Connect to debug connector as shown in the CRB.
2. Unused, N/C.

Table 5-15. Test Signals (Sheet 2 of 2)

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
TS_PRV_P0_P_PIN_PROBE4	Characterization Probe 4 Output	Char	VSB_1P10	CMOS	Drv	1	1
TS_VCS_P0_P_PIN_VSENSE	Internal Kelvin Monitors for Characterization Connector	Char	Analog			1	1
TS_VDDR0_P0_P_PIN_GSENSE	Internal Kelvin Monitors for Characterization Connector	Char	Analog			1	1
TS_VDDR0_P0_P_PIN_VSENSE	Internal Kelvin Monitors for Characterization Connector	Char	Analog			1	1
TS_VDDR6_P0_P_PIN_GSENSE	Internal Kelvin Monitors for Characterization Connector	Char	Analog			1	1
TS_VDDR6_P0_P_PIN_VSENSE	Internal Kelvin Monitors for Characterization Connector	Char	Analog			1	1
TS_VDN_P0_P_PIN_GSENSE	Internal Kelvin Monitors for Characterization Connector	Char	Analog			1	1
TS_VDN_P0_P_PIN_VSENSE	Internal Kelvin Monitors for Characterization Connector	Char	Analog			1	1
TS_VIO0_P0_P_PIN_GSENSE	Internal Kelvin Monitors for Characterization Connector	Char	Analog			1	1
TS_VIO0_P0_P_PIN_VSENSE	Internal Kelvin Monitors for Characterization Connector	Char	Analog			1	1

1. Connect to debug connector as shown in the CRB.
2. Unused, N/C.

5.2.14 Thermal Diode and Monitor Signals

Table 5-16 lists the thermal diode and monitor signals.

Table 5-16. Thermal Diode and Monitor Signals

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
TS_EX05_P0_P_PIN_TDIODE_A	Core 05 Thermal Diode Anode	Thermal Diode	Analog			1	1
TS_EX05_P0_P_PIN_TDIODE_C	Core 05 Thermal Diode Cathode	Thermal Diode	Analog			1	1
TS_EX06_P0_P_PIN_TDIODE_A	Core 06 Thermal Diode Anode	Thermal Diode	Analog			1	1
TS_EX06_P0_P_PIN_TDIODE_C	Core 06 Thermal Diode Cathode	Thermal Diode	Analog			1	1

1. Do not connect.

5.2.15 Regulator Sense Signals

Table 5-16 lists the regulator sense signals.

Table 5-17. Regulator Sense Signals

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
VCS_CHIP_GSENSE	Regulator GND Sense Point on Socket for VCS	Regulator Sense				1	1
VCS_CHIP_VSENSE	Regulator Positive Sense Point on Socket for VCS	Regulator Sense				1	2
VDD_CHIP_GSENSE	Regulator GND Sense Point on Socket for VDD	Regulator Sense				1	3
VDD_CHIP_VSENSE	Regulator Positive Sense Point on Socket for VDD	Regulator Sense				1	4
VDN_CHIP_GSENSE	Regulator GND Sense Point on Socket for VDN	Regulator Sense				1	5
VDN_CHIP_VSENSE	Regulator Positive Sense Point on Socket for VDN	Regulator Sense				1	6

1. Negative sense point for VCS regulator.
2. Positive sense point for VCS regulator.
3. Negative sense for VDD regulator.
4. Positive sense for VDD regulator.
5. Negative sense for VDN regulator.
6. Positive sense for VDN regulator.

6. Electrical Characteristics

This section provides AC and DC electrical specifications and thermal characteristics for the POWER9 processor.

6.1 Frequency Domains

Table 6-1 on page 53 lists the POWER9 chip frequency domains and scan frequency domains.

Table 6-1. POWER9 Frequency Domains

Region	IP	Ship Frequency	Maximum Frequecy	Minimum Frequency	Supply Type	Notes
Core/L2	Core, L2	Varied	4.2 GHz	1.2 GHz (200 MHz)	Adaptive, Dynamic	
Chiplet	L3, NCU	Varied	2.1 GHz	1.2 GHz (200 MHz)	Adaptive, Dynamic	
Nest Logic	Nest	1.867 GHz	2.40 GHz	1.6 GHz	Adaptive, Static	1
MCA DDR Logic	DDR	2.667 GHz	2.667 GHz	1.866 GHz	Adaptive, Static	2
		1.866 GHz	2.40 GHz	1.866 GHz		3
MCIO DDR	DDR	1.33 GHz	1.33 GHz	0.8 GHz	Adaptive, Static (VDN)	
MCIO DDR	DDR	1.33 GHz	1.33 GHz	0.8 GHz	Adaptive, Static (VDN)	
X Logic Async	X0 - 5	2.0 GHz	2.0 GHz	2.0 GHz	Adaptive, Static	
XIO PHY	X0 - 5	8.0 GHz	8.0 GHz	8.0 GHz	Fixed (VIO)	
PCIe	PCIe	2.0 GHz	2.0 GHz	2.0 GHz	Adaptive, Static	
PCI PHY	PCI	16/8/5.5/2.5 GHz	16/8/5.5/2.5 GHz	16/8/5.5/2.5 GHz	Fixed (VIO)	
PCIREF	PCI	100 MHz	100 MHz	100 MHz	Fixed (VDN)	
FSI	FSI	166 MHz	166 MHz	1 KHz	Fixed (VSB)	
JTAG	JTAG macro	50 MHz	50 MHz	50 Mhz	Fixed (VIO)	
JTAG TCK	DDR / PCIe	50 MHz	50 MHz	50 MHz	Adaptive, Static (VDN)	
LPC	Perv	33 MHz	33 MHz	33 MHz	Adaptive, Static	

1. A nest frequency of 1.6 GHz limits the maximum DRAM frequency to 2400 MHz.
2. Memory is asynchronous to the nest.
3. Memory is synchronous with the nest.

6.2 DC Electrical Characteristics

Table 6-2 through *Table 6-7* on page 56 provide the V_{DD}, V_{CS}, V_{DN}, V_{IO}, AV_{DD}/DV_{DD}, and V_{DDR} voltage requirements for the POWER9 processor.

Table 6-2. POWER9 Processor V_{DD} (Core) Voltage Requirements

DC Voltage[1]	Maximum	1.155 V			Specifies the DC voltage range at the remote sense pin.
	Boot Voltage	1.0 V			
	Minimum	0.6 V			
AC Voltage	Maximum	1.2			Duration must not exceed 20 µs at a time.
Load Line	200 - 300 µΩ				The value, 254 µΩ, is highly recommended to minimize system characterization and software coding.
Regulation Set-Point Tolerance	±5.0 mV				Based on the VID table for 5 mV settings.
Dynamic VID Slew Rate	±10.0 mV/µs				Deviations must be reviewed by IBM.
AC Noise (any source)	±9% at remote sense pin				AC noise budget contains an allowable regulation ripple and transient load-step/release response.
Maximum Current Load	190 W	234 A (TDC)	261 A (RDC)	313 A (Boost)[2]	TDC, RDC, and boost values.
	160 W	200 A (TDC)	221 A (RDC)	266 A (Boost)[2]	
	130 W	154 (TDC)	171 A (RDC)	205 (Boost)[2]	
	90 W	77 (TDC)	90 A (RDC)	108 (Boost)[2]	
Minimum Current Load	2 A				
Current Load Step [3]	190 W	184 A 220 A			Idle to TDP. Idle to RDP to boost peak current.
	160 W	142 A 170 A			Idle to TDP. Idle to RDP to boost peak current.
	130 W	115 A 137 A			Idle to TDP. Idle to RDP to boost peak current.
	90 W	46 A 56 A			Idle to TDP. Idle to RDP to boost peak current.
Load Step Slew Rate	400 A/µs				Slew rate as seen by the socket for the purpose of power validation testing.
Remote Sense Required?	Yes				

1. Voltage ID (VID) is set via the AVSBus using OCC code.
2. Boost current sustained for ≤ 4 ms at 5% duty cycle.
3. Both idle-to-TDP and idle-to-RDP assume boost is enabled.

Table 6-3. POWER9 Processor V_{CS} (Cache) Voltage Requirements

DC Voltage[1]	Maximum	1.155 V	Specifies the DC voltage range at the remote sense pin.
	Boot Voltage	1.03 V	
	Minimum	0.96 V	
Load Line	0 - 300 µΩ		A 0 µΩ value is highly recommended to minimize system characterization and software coding.
Regulation Set-Point Tolerance	±5.0 mV		
AC Noise (any source)	±4%		AC noise budget contains an allowable regulation ripple and transient load-step/release response.
Maximum Current Load	18 A (TDC)	20 A (RDC)	
Minimum Current Load	0 A		
Current Load Step	12 A		
Load Step Slew Rate	30 A/µs		
Remote Sense Required?	Yes		

1. Voltage is set via the AVSBus. It is recommended to use a second loop from the V_{DD} or V_{DN} regulator.

Table 6-4. POWER9 Processor V_{DN} Voltage Requirements

DC Voltage[1]	Maximum	1.155 V	Specifies the DC voltage range at the remote sense pin.
	Boot Voltage	0.8 V	
	Minimum Voltage	0.65 V	
Regulation Set-Point Tolerance	±5 mV		
Dynamic VID Slew Rate	±10 mV/µs		
AC Noise (any source)	±3.0%		AC noise budget contains an allowable regulation ripple.
Maximum Current Load	40 (TDC)	50 A (RDC)	One-socket system at 1.867 GHz Nest
	50 (TDC)	60 A (RDC)	Two-socket system at 1.867 GHz Nest
Minimum Current Load	10 A		
Current Load Step	25 A		
Load Step Slew Rate	100 A/µs		
Remote Sense Required?	Yes		

1. Voltage set via the AVSBus.

Table 6-5. POWER9 Processor V_{IO} Voltage Requirements

DC Voltage	1.05 V	Measured at the socket interface pins.
Regulation Set-Point Tolerance	±2.0%	Not to exceed the C4 maximum of 1.155 V.
AC Noise (any source)	±5.0%	AC noise budget contains an allowable regulation ripple and transient load-step/release response. **Note:** Measured at the socket interface pins.
Maximum Current Load	21 A	All part numbers
Current Load Step	7 A	
Load Step Slew Rate	30 A/µs	
Remote Sense Required?	Yes	Remote sense is required but socket pins are not dedicated to this voltage rail. The designer must ensure that the regulator DC voltage ± regulation setpoint tolerance is maintained at the socket interface pins.

Table 6-6. POWER9 Processor AV_{DD}/DV_{DD} Voltage Requirements

DC Voltage	1.5 V	
Regulation Set-Point Tolerance	±2%	
AC Noise (any source)	±8%	AC noise budget contains an allowable regulation ripple and transient load-step/release response. **Note:** Measured at the socket interface pins.
Maximum Current Load	2.0 A	**Note:** This is the total current for both AV_{DD} and DV_{DD}.
Maximum I_{AVDD}	1.0 A	
Maximum I_{DVDD}	1.0 A	
Current Load Step	0.1 A	
Load Step Slew Rate	1 A/µs	

Table 6-7. POWER9 DDR4 Voltage Requirements

DC Voltage	1.2 V	
Regulation Set-Point Tolerance	±0.5%	
DC and AC Noise (any source)	±5%	Required at each load by the JEDEC specification.
Maximum Current Load	7.5 A	Per VDDR domain.
	13 A	Total per socket.
Current Load Step	5 A	
Load Step Slew Rate	30 A/µs	

6.2.1 General System Voltage Requirements

Table 6-8 and *Table 6-9* show the voltages expected to be supplied to various loads around the system. These voltages can be shared with other devices in the system as long as the DC and AC levels are met at the processor.

Table 6-8. 1.1 V_{SB}: Standby/Auxiliary

DC Voltage	1.1 V	
Regulation Set-Point Tolerance	±1%	
AC Noise (any source)	±3.0%	AC noise budget contains an allowable regulation ripple and transient load-step/release response.
Maximum Current Load (Processor)	0.5 A	
Load Step Slew Rate	1 A/µs	

Table 6-9. 3.3 V_{SB}: Standby/Auxiliary

DC Voltage	3.3 V	
Regulation Set-Point Tolerance	±1.5%	
AC Noise (any source)	±4.5%	AC noise budget contains an allowable regulation ripple and transient load-step/release response.
Maximum Current Load (processor)	0.1 A	
Load Step Slew Rate	1 A/µs	

6.2.2 Power and Frequencies

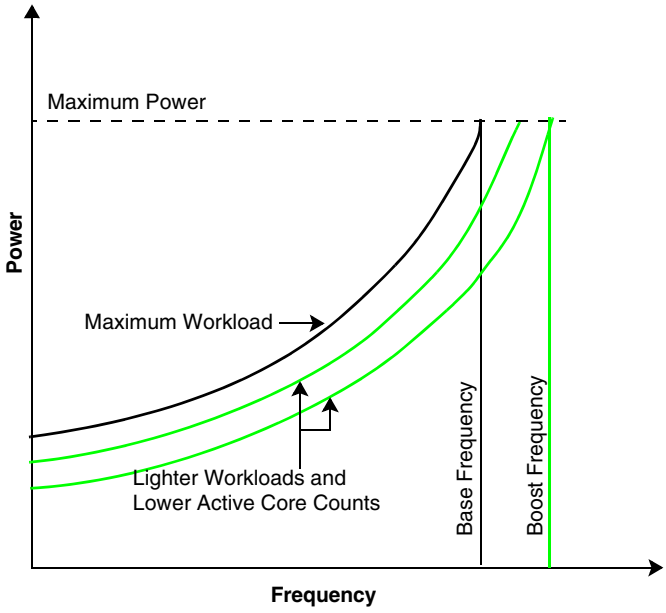
The maximum socket power shown in *Table 6-10* on page 59 represents the power consumed under maximum workload conditions with all cores active and in any allowed environmental condition (ambient temperature or altitude). It is possible to exceed this maximum power with a contrived power virus workload that toggles transistors in the processor on and off, but does not do any real work. This virus-like code can cause the processor to exceed the maximum power for a thermally-significant period of time. Consequently, the thermal subsystem must be designed such that the T_J (maximum) can be maintained while dissipating that maximum power and while under all specified environmental conditions. If T_J cannot be maintained as previously described, the frequency is reduced by the on-chip controller (OCC) to below base frequency and errors are surfaced to the user.

Additionally, the OCC takes advantage of inactive cores, lower-power consuming workloads, and favorable environmental conditions to allow the frequency to be increased above base frequency up to the boost frequency. The maximum socket power remains the same[3], but the frequency is increased to take advantage of the available power headroom. Note that the actual frequency is still selected by Linux based on the governor and that the OCC only sets the maximum frequency that is allowed.

Figure 6-1 on page 58 shows an example of frequency ranges and various governor settings.

3. During boost conditions, a change in workload can cause a momentary spike in power that can exceed the socket power limit for a period no longer than 4 ms at a 5% duty cycle. To support boost frequency, the system and regulator should be designed with these conditions in mind.

Figure 6-1. Workloads and Frequencies



Notes:

- Maximum frequency attained.
  - Base frequency is guaranteed under all workloads, environmental conditions, and active core counts.
  - Boost frequency is attained under favorable environmental conditions, low workloads, and low active core counts.
- Standard Linux governors used to control frequency.
  - Ondemand: The frequency selected varies with utilization across the entire range from minimum to boost.
  - Maximum performance: Always try to run at the boost frequency.
  - Powersave: Always run at the minimum frequency.
  - User-defined fixed frequency: Try to run at a fixed point anywhere in the range from minimum to boost.

Table 6-10 lists the power and frequencies for the POWER9 Sforza SCM part numbers.

Table 6-10. Power, Frequencies, and Junction Temperature[1]

Part Number	Processor Design Revision	Active Cores	Nest Frequency (GHz)	Boost Frequency (GHz)[2]	Base Frequency (GHz)	Maximum Socket Power (W)	L3 Cache (MB)	T_J Maximum (°C)
02CY296	DD2.2	22	1.867	3.80	2.75	190	110	85
02CY642	DD2.3							
02CY227	DD2.2	22	1.867	3.80	2.60	190	110	85
02CY639	DD2.3							
02CY228	DD2.2	20	1.867	3.80	2.70	190	100	85
02CY637	DD2.3							
02CY489	DD2.2	18	1.867	3.80	2.80	190	90	85
02CY646	DD2.3							
02CY230	DD2.2	16	1.867	3.80	2.90	190	80	85
02CY640	DD2.3							
02AA986	DD2.1[3]	16	1.600	3.80	2.90	190	80	85
02CY977	DD2.2	8	1.867	4.10	3.80	190	80	85
02WP000	DD2.3							
02CY414	DD2.2	22	1.867	3.80	2.25	160	110	85
02CY644	DD2.3							
02CY415	DD2.2	20	1.867	3.80	2.40	160	100	85
02CY645	DD2.3							
02CY231	DD2.2	16	1.867	3.80	2.50	160	80	85
02CY641	DD2.3							
02AA882	DD2.1[3]	16	1.600	3.40	2.20	160	80	85
02CY089	DD2.2	8[4]	1.867	3.80	3.50	160	80	85
02CY649	DD2.3							
02CY416	DD2.2	18	1.867	3.80	2.25	130	90	85
02CY647	DD2.3							
02CY417	DD2.2	16	1.867	3.80	2.30	130	80	85
02CY648	DD2.3							
02CY771	DD2.2	12	1.867	3.80	2.20	105	60	85
02CY781	DD2.3							
02CY297	DD2.2	4[4]	1.867	3.80	3.20	90	40	85
02CY650	DD2.3							

1. Values in this table are pending hardware qualification and are subject to change.
2. Indicates the maximum frequency achievable under favorable environmental conditions, low workloads, and low-active core counts.
3. Refer to the *POWER9 Processor DD 2.1 Use Restrictions Application Note*.
4. Leverages one active core per chiplet to maximize the L2/L3 bandwidth and capacity per core.

6.2.3 Miscellaneous Signals

See the *I^2C Bus Specification (version 2.1)* for DC electrical details of the I^2C bus.

Table 6-11. I^2C DC Voltage

DC Voltage	Description
I^2C Voltage	3.3 V V_{DD}
V_{IH}	$V_{DD} \times 0.7 = 2.3$ V
V_{IL}	$V_{DD} \times 0.3 = 0.99$ V

See the *PCI Local Bus Specification (Revision 3.0)* for DC electrical details for the LPC bus.

6.3 AC Electrical Characteristics

This section provides the preliminary AC electrical characteristics for the POWER9 processor. After fabrication, parts are sorted by maximum processor core frequency and tested for conformance to the AC specifications for that frequency.

6.3.1 Clock AC Specifications

System reference clocks are 133.33 MHz and use host clock signal level (HCSL) differential levels, which are the same as the PCIe standard levels. The POWER9 processor defaults to no internal termination on the reference clock inputs. Care must be taken to ensure that the clocks are properly terminated.

Spread spectrum is only allowed on the system reference clocks. It is limited to a spread percentage of 0.5% in the downward direction, which is the specified maximum allowed by the DRAMs and PCIe.

The PCIe reference clocks are 100.0 MHz and use HCSL differential levels, which are the same as the PCIe standard levels. The POWER9 processor defaults to no internal termination on the reference clock inputs. Care must be taken to ensure that the clocks are properly terminated. The POWER9 processor chip can be configured to allow the system reference clock to be used to generate the PCIe reference clocks if spread spectrum on the PCIe interfaces is required.

The LPC clock to the processor is a 33.33 MHz single-ended CMOS with an MPUL of 1.1 V. The IBM system has a resistor divider network on the board to support this. The reference clock skew specification for LPC is 2.0 ns.

Figure 6-2 shows the differential HCSL reference clock waveforms.

Figure 6-2. Differential (HCSL) Reference Clock Waveform (System and PCIe)

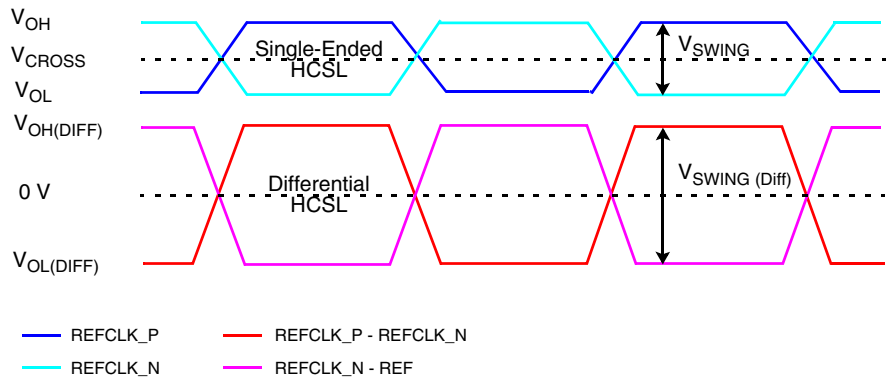


Table 6-12. Differential Reference Clock DC and AC Specification (Sheet 1 of 2)

Symbol	Parameter	Minimum	Typical	Maximum	Units	Notes
V_{OL}	Output low voltage	-0.10	0.0	0.1	V	1
V_{OH}	Output high voltage	0.50	0.70	0.90	V	1
V_{SWING}	Voltage swing	0.50	0.70	1.0	V	1
V_{CROSS}	Absolute crossing point (common mode voltage)	250	350	500	mV	1, 2, 3
V_{CROSS} Delta	Maximum variation in common mode voltage	–	–	100	mV	1, 2, 4
V_{MAX}	Absolute maximum voltage	–	–	1.15	V	1, 5
V_{MIN}	Absolute minimum voltage	-0.20	–	–	V	1, 6

1. Measurement taken from a single-ended waveform (see *Table 6-2* on page 61).
2. Measured at the crossing point where the instantaneous voltage value of the rising edge of REFCLK_P equals the falling edge of REFCLK_N (see *Figure 6-3* on page 62).
3. Refers to the total variation from the lowest crossing point to the highest crossing point, regardless of which edges are crossing. Refers to all crossing points for this measurement (see *Figure 6-3* on page 62).
4. Defined as the total variation of all crossing voltages of rising REFCLK_P and falling REFCLK_N. This is the maximum allowed variance in V_{CROSS} for any system (see *Figure 6-4* on page 63).
5. Defined as the maximum instantaneous voltage including overshoot (see *Figure 6-3* on page 62).
6. Defined as the minimum instantaneous voltage including overshoot (see *Figure 6-3* on page 62).
7. Measurement taken from a differential waveform (see *Figure 6-2* on page 61).
8. Measured from -150 mV to +150 mV on the differential waveform (derived from REFCLK_P - REFCLK_N). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing (see *Figure 6-6* on page 63).
9. T_{STABLE} is the time that the differential clock must maintain a minimum ±150 mV differential voltage after the rising/falling edges before it is allowed to drop back into the V_{RB} ±100 mV differential range (see *Figure 6-7* on page 64).
10. Defined as the average period. This includes crystal PPM and spread spectrum.
11. Defined as the frequency accuracy specification of the crystal that is used to generate the reference clock (typically less than 100 PPM).
12. PPM refers to parts per million and is a DC absolute period accuracy specification. One PPM is 1/1,000,000 of the clock frequency. The period is measured with a frequency counter with the measurement window set to 100 ms or greater. For systems that use spread-spectrum clocking, there is an additional 2500 PPM average shift in the maximum period resulting from a 0.5% down spread.

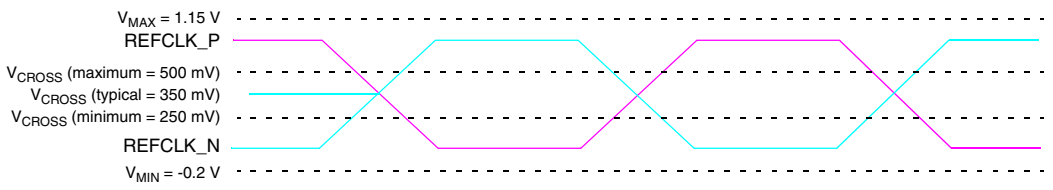
Table 6-12. Differential Reference Clock DC and AC Specification (Sheet 2 of 2)

Symbol	Parameter	Minimum	Typical	Maximum	Units	Notes
V_{OL} (Diff)	Output low voltage	-0.5	-0.7	-0.9	V	7
V_{OH} (Diff)	Output high voltage	0.50	0.70	0.90	V	7
V_{SWING} (Diff)	Voltage swing (differential)	1.0	1.4	1.8	V	7
T_R, T_F (Diff)	Rising and falling edge rates (differential)	1.0	2.0	4.0	V/ns	7, 8
V_{RB}	Ringback voltage margin	-100	–	100	mV	7, 9
T_{STABLE}	Time before V_{RB} is allowed	500	–	–	ps	7, 9
Duty Cycle	Duty cycle	45	–	55	%	7
T Period Average	Average clock period accuracy	50	–	2550	PPM	7, 10, 11, 12

1. Measurement taken from a single-ended waveform (see *Table 6-2* on page 61).
2. Measured at the crossing point where the instantaneous voltage value of the rising edge of REFCLK_P equals the falling edge of REFCLK_N (see *Figure 6-3* on page 62).
3. Refers to the total variation from the lowest crossing point to the highest crossing point, regardless of which edges are crossing. Refers to all crossing points for this measurement (see *Figure 6-3* on page 62).
4. Defined as the total variation of all crossing voltages of rising REFCLK_P and falling REFCLK_N. This is the maximum allowed variance in V_{CROSS} for any system (see *Figure 6-4* on page 63).
5. Defined as the maximum instantaneous voltage including overshoot (see *Figure 6-3* on page 62).
6. Defined as the minimum instantaneous voltage including overshoot (see *Figure 6-3* on page 62).
7. Measurement taken from a differential waveform (see *Figure 6-2* on page 61).
8. Measured from -150 mV to +150 mV on the differential waveform (derived from REFCLK_P - REFCLK_N). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing (see *Figure 6-6* on page 63).
9. T_{STABLE} is the time that the differential clock must maintain a minimum ±150 mV differential voltage after the rising/falling edges before it is allowed to drop back into the V_{RB} ±100 mV differential range (see *Figure 6-7* on page 64).
10. Defined as the average period. This includes crystal PPM and spread spectrum.
11. Defined as the frequency accuracy specification of the crystal that is used to generate the reference clock (typically less than 100 PPM).
12. PPM refers to parts per million and is a DC absolute period accuracy specification. One PPM is 1/1,000,000 of the clock frequency. The period is measured with a frequency counter with the measurement window set to 100 ms or greater. For systems that use spread-spectrum clocking, there is an additional 2500 PPM average shift in the maximum period resulting from a 0.5% down spread.

Figure 6-3 shows the single-ended measurement points for absolute cross points and swing.

Figure 6-3. Single-Ended Measurement Points for Absolute Cross Points and Swing



6.3.2 Differential Reference Clock Measurements

Figure 6-4 shows the single-ended measurement points for the delta cross point.

Figure 6-4. Single-Ended Measurement Points for Delta Cross Point

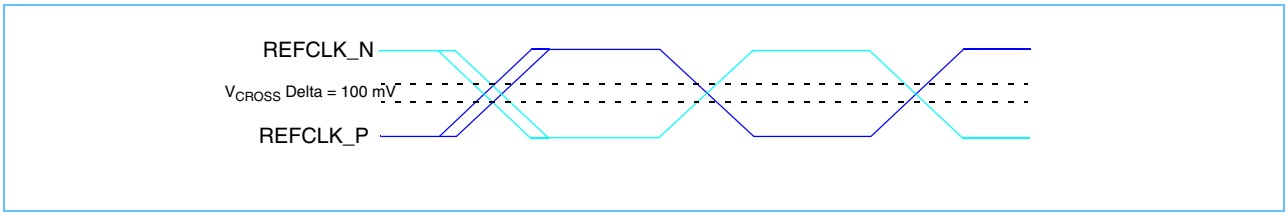


Figure 6-5 shows the differential measurement points for the duty cycle and period.

Figure 6-5. Differential Measurement Points for Duty Cycle and Period

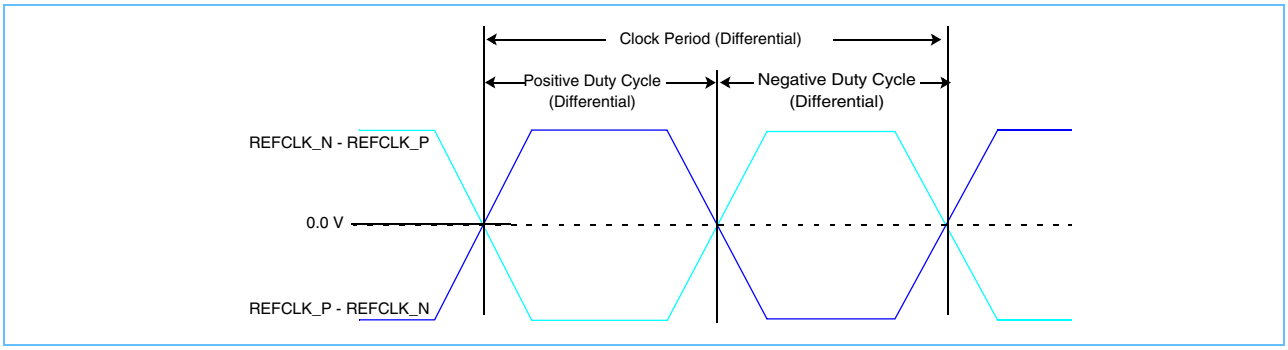


Figure 6-6 shows the differential measurement points for the rise and fall times.

Figure 6-6. Differential Measurement Points for Rise and Fall Times

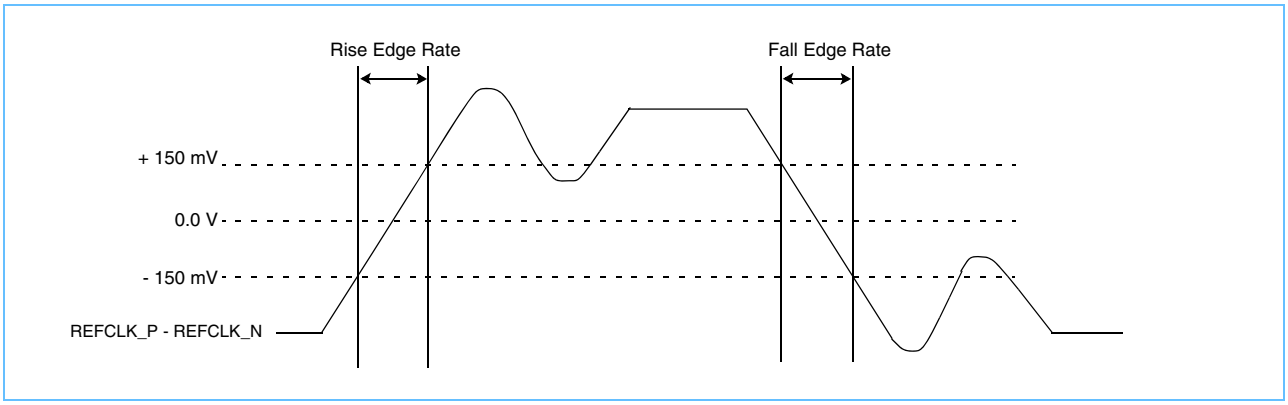


Figure 6-7 shows the differential measurement points for ringback.

Figure 6-7. Differential Measurement Points for Ringback

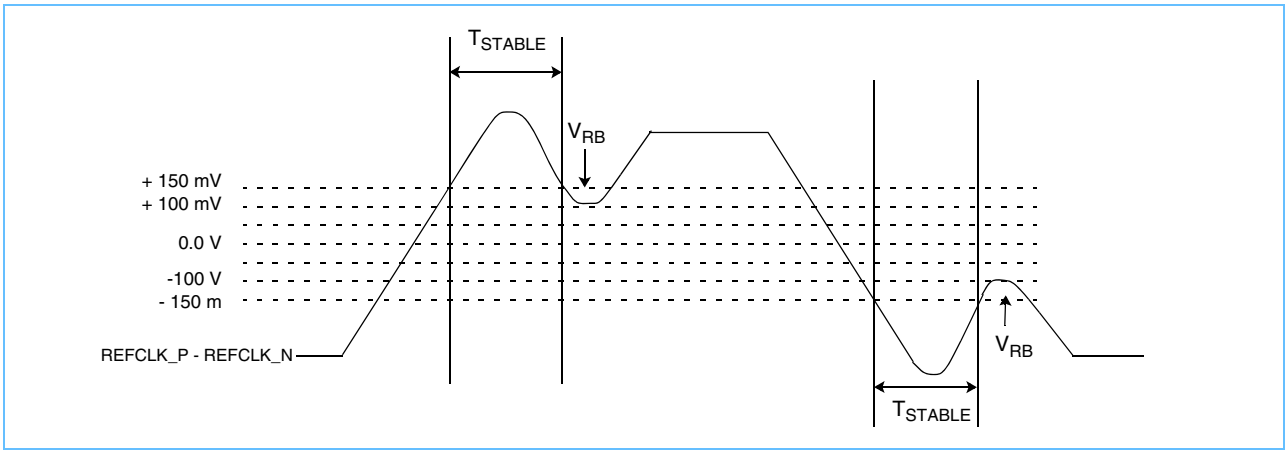


Table 6-13 lists general DC and AC specifications.

Table 6-13. DC and AC Specifications

Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units	Notes
Output Voltage	V_{OL}	Output low voltage	–	0	0.2	V	1
	V_{OH}	Output high voltage	0.8	1.0	1.15	V	1
	V_{SWING}	Peak-peak, single-ended swing	0.8	1.0	1,15	V	1, 2
Rise and Fall Times	T_R, T_F	20% - 80%	–	1.5	3.0	ns	1, 3
Duty Cycle	DC	Measured at $V_{SWING}/2$	45	–	55	%	1, 2, 4
Clock Period	T_{AVG}	Clock period accuracy	-50	–	+50	PPM	1, 2, 4, 5

1. Measurements taken from a single-ended waveform (see *Figure 6-8* on page 65).
2. Voltage swing is equal to V_{OH} - V_{OL} (see *Figure 6-8* on page 65).
3. Rise and fall time measurements taken between 20% and 80% of V_{OH} and V_{OL} (see *Figure 6-8* on page 65).
4. Measurements taken at a voltage equal to $V_{SWING}/2$ (see *Figure 6-9* on page 65).
5. PPM refers to parts per million and is a DC absolute period accuracy specification. It includes only the accuracy of the crystal that is used to generate the clock because spread spectrum is not enabled. The period is to be measured with a frequency counter with the measurement window set to 100 ms or greater.

Figure 6-8 shows the single-ended processor reference clocks and highlights the voltage and transition time measurement points.

Figure 6-8. Single-Ended Processor Reference Clocks (Voltage and Transition Time Measurement Points)

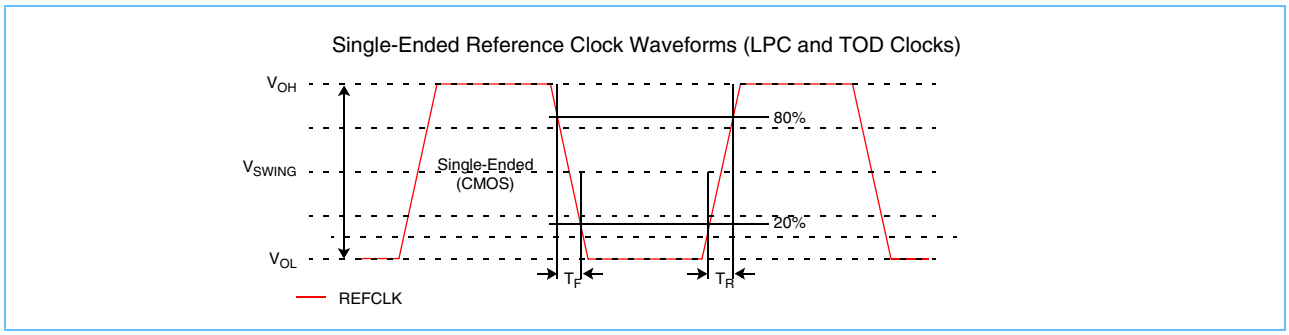
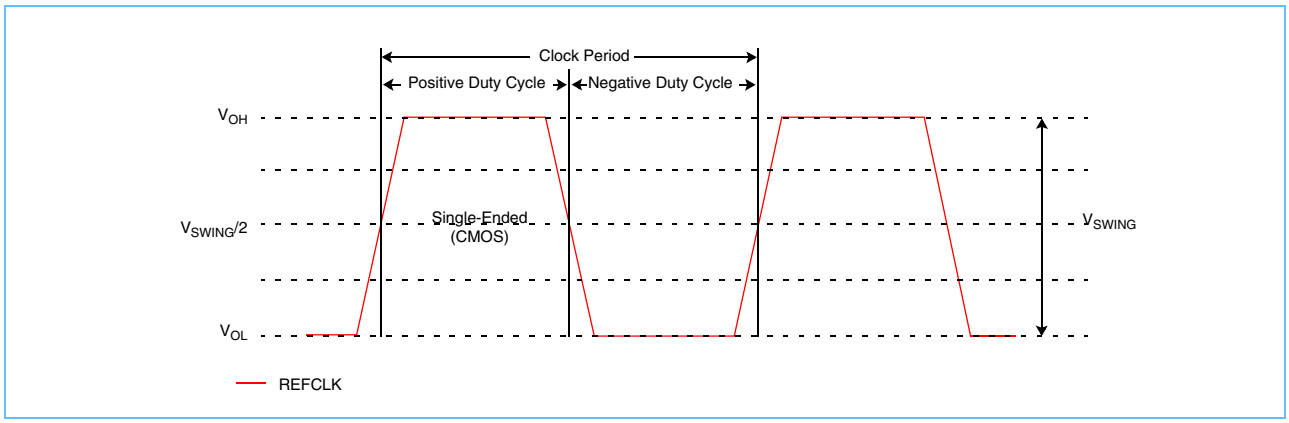


Figure 6-9 shows the single-ended processor reference clocks and highlights the period and duty cycle measurement points.

Figure 6-9. Single-Ended Processor Reference Clocks (Period and Duty-Cycle Measurement Points)



6.3.3 FSI AC Specifications

Table 6-14 lists the AC specifications for the FSI bus.

Table 6-14. FSI Electrical Specification

Description	Minimum	Typical	Maximum	Units	Notes
C4 V_{MAX}			1.15	V	Maximum voltage at the chip pad.
Receiver V_{IL}			$0.4 \times 1.1\ V_{SB}$	mV	For receiver input hysteresis.
Receiver V_{IH}	$0.6 \times 1.1\ V_{SB}$			mV	For receiver input hysteresis.
1 KΩ pull-up resistance	0.75	1.0	1.25	KΩ	Pull-up resistance without leakage. If external pull-ups are used, they must be returned to V_{DOUT} and have a combined impedance not less than 1 KΩ.
1 KΩ pull-down resistance	0.75	1.0	1.25	KΩ	Pull-down resistance without leakage. If external pull downs are used, they must have a combined impedance not less than 1 KΩ in parallel with 10 KΩ.
10 KΩ pull-down resistance	8	10	12	KΩ	Pull-up resistance without leakage.
Driver V_{OL}	$-0.1 \times 1.1\ V_{SB}$		$0.2 \times 1.1\ V_{SB}$	mV	Output pad driver levels.
Driver V_{OH}	$0.8 \times 1.1\ V_{SB}$		$1.1 \times 1.1\ V_{SB}$	mV	Output pad driver levels.
Rise/Fall time (10% - 90% of V_{DOUT} with a 2 pF load)	100	300	500	ps	

Table 6-15 lists the default settings for the internal FSI pull-up and pull-down resistors.

Table 6-15. Default FSI Settings

Function	SCM Pin	Pull-Up Internal Value	Pull-Down Internal Value
FSI0 Clock	M54	–	1 KΩ
FSI0 Data	L55	1 KΩ	–
FSI Master CP 1 Clock	M58	–	–
FSI Master CP 1 Data	L59	–	10 KΩ

6.3.4 SPI AC Specifications

Table 6-16 list the AC specifications for the SPI bus.

Table 6-16. SPI AC Specification

Description	Minimum	Typical	Maximum	Units	Notes
C4 V_{MAX}			3.3 V	V	Maximum voltage at the chip pad.
Receiver V_{IL}			$0.3 \times 3.3\ V_{SB}$	mV	For receiver input hysteresis.
Receiver V_{IH}	$0.7 \times 3.3\ V_{SB}$			mV	For receiver input hysteresis.
1 KΩ Pull-up Resistance	1	1.25	1.5	KΩ	Pull-up resistance without leakage. If external pull ups are used, they must be returned to V_{DOUT} and have a combined impedance not less than 1 KΩ.
1 KΩ Pull-down Resistance	1	1.25	1.5	KΩ	Pull-down resistance without leakage. If external pull downs are used, they have a combined impedance not less than 1 KΩ in parallel with 10 KΩ.
10 KΩ Pull-down Resistance	10	12.5	15	KΩ	Pull-up resistance without leakage.
Driver V_{OL}	$-0.1 \times 3.3\ V_{SB}$		$0.2 \times 3.3\ V_{SB}$	mV	Output pad driver levels.
Driver V_{OH}	$0.8 \times 3.3\ V_{SB}$		$1.1 \times 3.3\ V_{SB}$	mV	Output pad driver levels.
Rise/Fall Time (10% - 90% of V_{DOUT} with a 2 pF load)	100	300	500	ps	

Table 6-17 lists the default settings for the internal SPI pull-up and pull-down resistors.

Table 6-17. Default SPI Settings

Function	Signal Name	SCM Pin	Pull-Up Internal Value	Pull-Down Internal Value	Notes
SPIPSS_MOSI	PV_APSS_P0_P_PIN_MOSI	B64	–	10 KΩ	
SPIPSS_MISO	PV_APSS_PIN_P_P0_MISO	C61		10 KΩ	
SPIPSS_SCLK	PV_APSS_P0_P_PIN_SCLK	A65		10 KΩ	1
SPIPSS_CS0	PV_APSS_P0_P_PIN_CS0	B62	1 KΩ	–	
SPIPSS_CS1	PV_APSS_P0_P_PIN_CS1	A63	1 KΩ	–	

1. For the PV_APSS_P0_P_PIN_SCLK pin, the minimum clock frequency is 1 MHz and maximum clock frequency is 10 MHz.

6.3.5 AVS AC Specifications

Table 6-18 list the AC specifications for the AVSBus.

Table 6-18. AVS AC Specification

Description	Minimum	Typical	Maximum	Units	Notes
C4 V_{MAX}			1.15	V	Maximum voltage at the chip pad.
Receiver V_{IL}			$0.4 \times V_{IO}$	mV	For receiver input hysteresis.
Receiver V_{IH}	$0.6 \times V_{IO}$			mV	For receiver input hysteresis.
10 KΩ Pull-Down Resistance	8	10	12	KΩ	Internal pull-down.
Driver V_{OL}	$-0.1 \times V_{IO}$		$0.2 \times V_{IO}$	mV	Output pad driver levels.
Driver V_{OH}	$0.8 \times V_{IO}$		$1.1 \times V_{IO}$	mV	Output pad driver levels.
Rise/Fall Time (10% - 90% of V_{DOUT} with a 2 pF load)	100	300	500	ps	

Table 6-19 lists the default settings for the internal AVS pull-down resistors.

Table 6-19. Default AVS Settings

Function	Signal Name	SCM Pin	Pull-Down Internal Value	Pull-Up Internal Value	Notes
AVS 0 Clock	PV_AVS0_P0_P_PIN_CLK	K52	1 KΩ		1, 2
AVS 0 Master Data	PV_AVS0_P0_P_PIN_MDATA	J51		1 KΩ	
AVS 0 Slave Data	PV_AVS0_PIN_P_P0_SDATA	H54		1 KΩ	
AVS 1 Clock	PV_AVS1_P0_P_PIN_CLK	J53	1 KΩ		1, 2
AVS 1 Master Data	PV_AVS1_P0_P_PIN_MDATA	H52		1 KΩ	
AVS 1 Slave Data	PV_AVS1_PIN_P_P0_SDATA	J55		1 KΩ	

1. For the PV_AVS0_P0_P_PIN_CLK pin, the minimum clock frequency is 1 MHz and the maximum clock frequency is 25 MHz.
2. For DD 2.0, the pull-down internal value is 1 KΩ.

6.3.5.1 Recommended AVSBus Topology

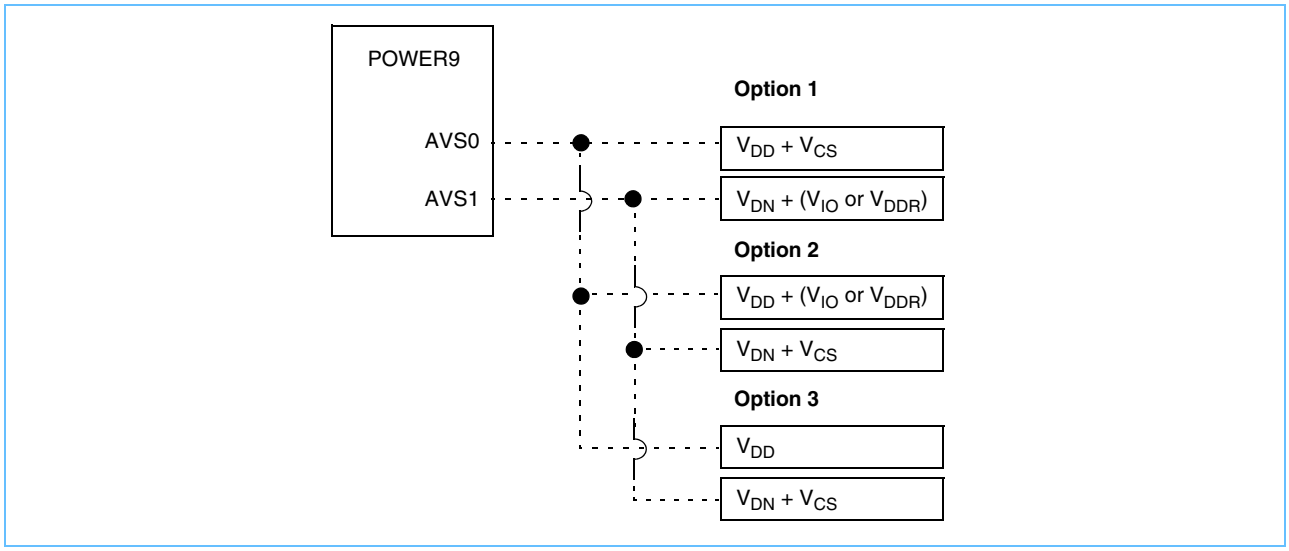
The AVSBus is part of the *PMBus 1.3 Specification*. See that document for more specific infomation. The AVSBus is a point-to-point communication interface for use with point-of-load (POL) control devices. The POWER9 processor makes use of both the Master data (MData) and Slave data (SData) connections. The Slave data connection is necessary for the OCC to get regulator telemetry. This section covers the three supported AVSBus topologies for use with the POWER9 processor.

Most AVS-compliant regulators have two regulation control loops. For both Option 1 and Option 2, the V_{DD} and V_{DN} rails should be on the first regulator control loops. V_{DD} must always be connected on AVS bus0 and V_{DN} must be connected to AVS bus1. The secondary control loop can either be V_{CS} or either V_{IO} or V_{DDR}. Option 3 is for designs that need all available regulation phases available on the controller to supply enough current for V_{DD}. In this case, V_{DN} should be on AVS bus1 and use V_{CS} on the secondary control loop. V_{IO} does not have to be connected to an AVS bus controller but should be a PMBus-compliant device. This device should be connected to the BMC.

In all options, it is highly recommended to connect the PMBus from the regulator controller to the BMC. This enables the system-management software to perform diagnostics and telemetry. It is also recommended that all voltage regulator controllers for a processor socket be on the same I^2C/PMBus. A different I^2C/PMBus should be used for each socket.

Figure 6-10 illustrates these regulation control loop options.

Figure 6-10. AVS-Compliant Regulator Options



7. Mechanical Specifications

This section describes the POWER9 SCM features and pin list.

7.1 Single-Chip Module

Table 7-1 describes the SCM.

Table 7-1. SCM Features

Feature	Description
Body Size	50 x 50 mm
Package Type	FC PLGA
Interconnect Technology	CMOS 14 nm technology
	Hybrid LGA socket
	1.016 mm hexagonal LGA pitch
	4-4-4 organic package construction
Buses	Four DDR4 interfaces: • Up to 2666 MHz with one DIMM per channel • Up to 2400 MHz for two DIMMs per channel
	One X bus at 16 Gbps
	Three ×16 PCIe Generation 4 buses at 16 GTps
Power	90 W, 105 W, 130 W, 160 W, and 190 W
Package Pin Assignments	2601 total
SEEPROM Structure	Single SEEPROM

7.2 Electrostatic Discharge Considerations

The POWER9 processor is electrostatic discharge (ESD) sensitive. An appropriate ESD-handling procedure must be implemented and maintained by facilities handling this component. Handle according to the ANSI/ESD S20.20 or IEC 61340-5-1 standard. Packaging of this product in an ESD safe container must be maintained according to the ANSI/ESD S541 or IEC 61340-5-3 standard.

Table 7-2 on page 71 will be updated after the POWER9 processor has completed an ESD stress qualification in accordance with the JEDEC specification JESD47I.

Table 7-2. ESD Stress Qualification

ESD Model	Passing Level (V)	Reference
Human Body Model	1000	JS-001[1]
Charged Device Model (CDM)	200	JESD22-C101[2]

1. JS-001-2014 is the Joint JEDEC/ESDA Standard for Electrostatic Discharge Sensitivity Test - Human Body Model (HBM) Component Level.
2. JESD22-C101F is the Field-Induced Charged-Device Model Test Method for Electrostatic Discharge Withstand Thresholds of Microelectronic Components.

7.3 Mechanical Drawings

See the IBM Portal for OpenPOWER for the current mechanical drawings and recommended module layout.

7.4 Pinout

Table 7-3 Sforza SCM Pin List on page 73 shows the signal pins for the POWER9 Sforza SCM by position.

Table 7-3. Sforza SCM Pin List

Pin Number	Signal
A09	GND
A11	GND
A13	PE_E1_P0_P_PIN_DAT_02_P
A15	PE_E1_P0_P_PIN_DAT_02_N
A17	GND
A19	PE_E1_P0_P_PIN_DAT_00_P
A21	PE_E1_P0_P_PIN_DAT_00_N
A23	GND
A25	PE_E0_P0_P_PIN_DAT_03_N
A27	PE_E0_P0_P_PIN_DAT_03_P
A29	GND
A31	PE_E0_P0_P_PIN_DAT_07_P
A33	PE_E0_P0_P_PIN_DAT_07_N
A35	GND
A37	PE_E0_P0_P_PIN_DAT_11_N
A39	PE_E0_P0_P_PIN_DAT_11_P
A41	GND
A43	GND
A45	PE_E0_PIN_P_P0_DAT_10_P
A47	PE_E0_PIN_P_P0_DAT_10_N
A49	GND
A51	PE_E0_PIN_P_P0_DAT_13_N
A53	PE_E0_PIN_P_P0_DAT_13_P
A55	GND
A57	PV_DDR4567_P0_B_PIN_I2C_S-CL_B
A59	PV_DDR0123_P0_B_PIN_I2C_S-CL_B
A61	GND
A63	PV_APSS_P0_P_PIN_CS1
A65	PV_APSS_P0_P_PIN_SCLK
A67	GND
A69	PE_E2_PIN_P_P0_DAT_05_P
A71	PE_E2_PIN_P_P0_DAT_05_N
A73	GND
A75	PE_E2_PIN_P_P0_DAT_09_N
A77	PE_E2_PIN_P_P0_DAT_09_P
A79	GND
A81	PE_E2_PIN_P_P0_DAT_12_P

Pin Number	Signal
A83	PE_E2_PIN_P_P0_DAT_12_N
A85	GND
A87	GND
A89	PE_E2_P0_P_PIN_DAT_13_N
A91	PE_E2_P0_P_PIN_DAT_13_P
A93	GND
A95	GND
B02	SCM_PRESENT_B
B04	GND
B06	PE_E1_PIN_P_P0_DAT_00_N
B08	PE_E1_PIN_P_P0_DAT_00_P
B10	GND
B12	PE_E1_P0_P_PIN_DAT_03_P
B14	PE_E1_P0_P_PIN_DAT_03_N
B16	GND
B18	PE_E1_P0_P_PIN_DAT_01_P
B20	PE_E1_P0_P_PIN_DAT_01_N
B22	GND
B24	PE_E0_P0_P_PIN_DAT_02_N
B26	PE_E0_P0_P_PIN_DAT_02_P
B28	GND
B30	PE_E0_P0_P_PIN_DAT_06_P
B32	PE_E0_P0_P_PIN_DAT_06_N
B34	GND
B36	PE_E0_P0_P_PIN_DAT_10_N
B38	PE_E0_P0_P_PIN_DAT_10_P
B40	GND
B42	GND
B44	PE_E0_PIN_P_P0_DAT_09_P
B46	PE_E0_PIN_P_P0_DAT_09_N
B48	GND
B50	PE_E0_PIN_P_P0_DAT_14_N
B52	PE_E0_PIN_P_P0_DAT_14_P
B54	GND
B56	PV_DDR4567_P0_B_PIN_I2C_S-DA_B
B58	PV_DDR0123_P0_B_PIN_I2C_S-DA_B
B60	GND

Pin Number	Signal
B62	PV_APSS_P0_P_PIN_CS0
B64	PV_APSS_P0_P_PIN_MOSI
B66	GND
B68	PE_E2_PIN_P_P0_DAT_04_P
B70	PE_E2_PIN_P_P0_DAT_04_N
B72	GND
B74	PE_E2_PIN_P_P0_DAT_08_N
B76	PE_E2_PIN_P_P0_DAT_08_P
B78	GND
B80	PE_E2_PIN_P_P0_DAT_13_P
B82	PE_E2_PIN_P_P0_DAT_13_N
B84	GND
B86	GND
B88	PE_E2_P0_P_PIN_DAT_14_N
B90	PE_E2_P0_P_PIN_DAT_14_P
B92	GND
B94	GND
C01	GND
C03	VDDR01_1P20
C05	GND
C07	PE_E1_PIN_P_P0_DAT_01_P
C09	PE_E1_PIN_P_P0_DAT_01_N
C11	GND
C13	GND
C15	GND
C17	PE_E1_P0_P_PIN_DAT_04_P
C19	PE_E1_P0_P_PIN_DAT_04_N
C21	GND
C23	PE_E0_P0_P_PIN_DAT_01_P
C25	PE_E0_P0_P_PIN_DAT_01_N
C27	GND
C29	PE_E0_P0_P_PIN_DAT_08_N
C31	PE_E0_P0_P_PIN_DAT_08_P
C33	GND
C35	PE_E0_P0_P_PIN_DAT_12_N
C37	PE_E0_P0_P_PIN_DAT_12_P
C39	GND
C41	GND

Pin Number	Signal
C43	PE_E0_PIN_P_P0_DAT_08_P
C45	PE_E0_PIN_P_P0_DAT_08_N
C47	GND
C49	PE_E0_PIN_P_P0_DAT_15_N
C51	PE_E0_PIN_P_P0_DAT_15_P
C53	GND
C55	GND
C57	GND
C59	GND
C61	PV_APSS_PIN_P_P0_MISO
C63	PV_PRV_P0_B_PIN_GPIO0
C65	GND
C67	PE_E2_PIN_P_P0_DAT_03_N
C69	PE_E2_PIN_P_P0_DAT_03_P
C71	GND
C73	PE_E2_PIN_P_P0_DAT_10_N
C75	PE_E2_PIN_P_P0_DAT_10_P
C77	GND
C79	PE_E2_PIN_P_P0_DAT_14_N
C81	PE_E2_PIN_P_P0_DAT_14_P
C83	GND
C85	GND
C87	PE_E2_P0_P_PIN_DAT_12_N
C89	PE_E2_P0_P_PIN_DAT_12_P
C91	GND
C93	VDDR67_1P20
C95	GND
D02	DM_DDR0_BI_DQ_59
D04	GND
D06	GND
D08	PE_E1_PIN_P_P0_DAT_02_N
D10	PE_E1_PIN_P_P0_DAT_02_P
D12	GND
D14	GND
D16	PE_E1_P0_P_PIN_DAT_05_N
D18	PE_E1_P0_P_PIN_DAT_05_P
D20	GND
D22	PE_E0_P0_P_PIN_DAT_00_N
D24	PE_E0_P0_P_PIN_DAT_00_P

Pin Number	Signal
D26	GND
D28	PE_E0_P0_P_PIN_DAT_05_P
D30	PE_E0_P0_P_PIN_DAT_05_N
D32	GND
D34	PE_E0_P0_P_PIN_DAT_13_P
D36	PE_E0_P0_P_PIN_DAT_13_N
D38	GND
D40	GND
D42	PE_E0_PIN_P_P0_DAT_07_N
D44	PE_E0_PIN_P_P0_DAT_07_P
D46	GND
D48	PE_E0_PIN_P_P0_DAT_12_N
D50	PE_E0_PIN_P_P0_DAT_12_P
D52	GND
D54	GND
D56	TS_PRV_P0_P_PIN_PROBE2
D58	GND
D60	PV_E0B_PIN_P_P0_PRSNT_B
D62	PV_E0A_PIN_P_P0_PRSNT_B
D64	GND
D66	PE_E2_PIN_P_P0_DAT_02_N
D68	PE_E2_PIN_P_P0_DAT_02_P
D70	GND
D72	PE_E2_PIN_P_P0_DAT_11_P
D74	PE_E2_PIN_P_P0_DAT_11_N
D76	GND
D78	PE_E2_PIN_P_P0_DAT_15_P
D80	PE_E2_PIN_P_P0_DAT_15_N
D82	GND
D84	GND
D86	PE_E2_P0_P_PIN_DAT_15_P
D88	PE_E2_P0_P_PIN_DAT_15_N
D90	GND
D92	GND
D94	DM_DDR6_BI_DQ_59
E01	DM_DDR0_BI_DQ_62
E03	DM_DDR0_BI_DQ_63
E05	VDDR01_1P20
E07	GND

Pin Number	Signal
E09	PE_E1_PIN_P_P0_DAT_03_P
E11	PE_E1_PIN_P_P0_DAT_03_N
E13	GND
E15	PE_E1_P0_P_PIN_DAT_07_P
E17	PE_E1_P0_P_PIN_DAT_07_N
E19	GND
E21	PE_E1_P0_P_PIN_DAT_06_N
E23	PE_E1_P0_P_PIN_DAT_06_P
E25	GND
E27	PE_E0_P0_P_PIN_DAT_04_N
E29	PE_E0_P0_P_PIN_DAT_04_P
E31	GND
E33	PE_E0_P0_P_PIN_DAT_14_P
E35	PE_E0_P0_P_PIN_DAT_14_N
E37	GND
E39	GND
E41	PE_E0_PIN_P_P0_DAT_06_N
E43	PE_E0_PIN_P_P0_DAT_06_P
E45	GND
E47	PE_E0_PIN_P_P0_DAT_11_N
E49	PE_E0_PIN_P_P0_DAT_11_P
E51	GND
E53	PV_PRV_PIN_P_P0_CHIP_MAS-TER
E55	TS_PRV_P0_P_PIN_PROBE3
E57	PV_PRV_P0_B_PIN_GPIO2
E59	GND
E61	PV_E0_P0_P_PIN_PERST_B
E63	GND
E65	GND
E67	PE_E2_PIN_P_P0_DAT_06_N
E69	PE_E2_PIN_P_P0_DAT_06_P
E71	GND
E73	GND
E75	GND
E77	GND
E79	GND
E81	GND
E83	GND
E85	PE_E2_P0_P_PIN_DAT_11_P

Pin Number	Signal
E87	PE_E2_P0_P_PIN_DAT_11_N
E89	GND
E91	VDDR67_1P20
E93	DM_DDR6_BI_DQ_63
E95	DM_DDR6_BI_DQ_62
F02	DM_DDR0_BI_DQS_16_N
F04	DM_DDR0_BI_DQ_58
F06	GND
F08	GND
F10	PE_E1_PIN_P_P0_DAT_04_N
F12	PE_E1_PIN_P_P0_DAT_04_P
F14	GND
F16	GND
F18	GND
F20	PE_E1_P0_P_PIN_DAT_09_P
F22	PE_E1_P0_P_PIN_DAT_09_N
F24	GND
F26	PE_E1_P0_P_PIN_DAT_08_P
F28	PE_E1_P0_P_PIN_DAT_08_N
F30	GND
F32	PE_E0_P0_P_PIN_DAT_15_N
F34	PE_E0_P0_P_PIN_DAT_15_P
F36	GND
F38	GND
F40	PE_E0_PIN_P_P0_DAT_05_P
F42	PE_E0_PIN_P_P0_DAT_05_N
F44	GND
F46	GND
F48	GND
F50	GND
F52	PV_SEEPROM1_P0_P_PIN_I2C_SCL_B
F54	TS_PRV_P0_P_PIN_PROBE4
F56	PV_SEEPROM0_P0_B_PIN_I2C_SDA_B
F58	PV_PRV_P0_B_PIN_GPIO1
F60	GND
F62	PV_PRV_PIN_P_P0_LPC_CLK
F64	GND
F66	GND

Pin Number	Signal
F68	PE_E2_PIN_P_P0_DAT_07_P
F70	PE_E2_PIN_P_P0_DAT_07_N
F72	GND
F74	GND
F76	TS_OCC_PIN_P_P0_ALERT_B
F78	PV_PRV_P0_B_PIN_SPARE0
F80	GND
F82	GND
F84	PE_E2_P0_P_PIN_DAT_10_N
F86	PE_E2_P0_P_PIN_DAT_10_P
F88	GND
F90	GND
F92	DM_DDR6_BI_DQ_58
F94	DM_DDR6_BI_DQS_16_N
G01	GND
G03	DM_DDR0_BI_DQS_16_P
G05	DM_DDR0_BI_DQS_07_N
G07	VDDR01_1P20
G09	GND
G11	PE_E1_PIN_P_P0_DAT_05_P
G13	PE_E1_PIN_P_P0_DAT_05_N
G15	GND
G17	GND
G19	PE_E1_P0_P_PIN_DAT_11_P
G21	PE_E1_P0_P_PIN_DAT_11_N
G23	GND
G25	PE_E1_P0_P_PIN_DAT_12_P
G27	PE_E1_P0_P_PIN_DAT_12_N
G29	GND
G31	PE_E0_P0_P_PIN_DAT_09_N
G33	PE_E0_P0_P_PIN_DAT_09_P
G35	GND
G37	GND
G39	PE_E0_PIN_P_P0_DAT_04_N
G41	PE_E0_PIN_P_P0_DAT_04_P
G43	GND
G45	PV_SEEPROM3_P0_P_PIN_I2C_SCL_B
G47	PV_SEEPROM3_P0_B_PIN_I2C_SDA_B

Pin Number	Signal
G49	TS_TST_PIN_P_P0_FORCE_PWR_ON
G51	PV_SEEPROM1_P0_B_PIN_I2C_SDA_B
G53	GND
G55	PV_SEEPROM0_P0_P_PIN_I2C_SCL_B
G57	PV_PRV_PIN_P_P0_VDN_PGOOD
G59	TS_JTAG_PIN_P_P0_CARD_TEST
G61	GND
G63	PV_PRV_P0_B_PIN_LPC_DAT_2
G65	PV_PRV_P0_B_PIN_LPC_DAT_3
G67	GND
G69	PE_E2_PIN_P_P0_DAT_01_P
G71	PE_E2_PIN_P_P0_DAT_01_N
G73	GND
G75	GND
G77	PV_PRV_P0_P_PIN_ATTENTION_B
G79	GND
G81	GND
G83	PE_E2_P0_P_PIN_DAT_09_P
G85	PE_E2_P0_P_PIN_DAT_09_N
G87	GND
G89	VDDR67_1P20
G91	DM_DDR6_BI_DQS_07_N
G93	DM_DDR6_BI_DQS_16_P
G95	GND
H02	VDDR01_1P20
H04	DM_DDR0_BI_DQ_61
H06	DM_DDR0_BI_DQS_07_P
H08	GND
H10	GND
H12	PE_E1_PIN_P_P0_DAT_06_N
H14	PE_E1_PIN_P_P0_DAT_06_P
H16	GND
H18	PE_E1_P0_P_PIN_DAT_10_N
H20	PE_E1_P0_P_PIN_DAT_10_P
H22	GND
H24	GND
H26	GND

Pin Number	Signal
H28	GND
H30	GND
H32	GND
H34	GND
H36	GND
H38	PE_E0_PIN_P_P0_DAT_03_P
H40	PE_E0_PIN_P_P0_DAT_03_N
H42	GND
H44	GND
H46	TS_JTAG_PIN_P_P0_TDI
H48	PV_TPM_PIN_P_P0_INT
H50	GND
H52	PV_AVS1_P0_P_PIN_MDATA
H54	PV_AVS0_PIN_P_P0_SDATA
H56	GND
H58	PV_PRV_PIN_P_P0_FSI_IN_ENA
H60	PV_PRV_PIN_P_P0_FSI_SMD
H62	GND
H64	PV_PRV_PIN_P_P0_LPC_IRQ
H66	PV_PRV_P0_B_PIN_LPC_DAT_0
H68	GND
H70	PE_E2_PIN_P_P0_DAT_00_P
H72	PE_E2_PIN_P_P0_DAT_00_N
H74	GND
H76	TS_CLK_P0_P_PIN_PROBE0_N
H78	TS_CLK_P0_P_PIN_PROBE0_P
H80	GND
H82	PE_E2_P0_P_PIN_DAT_08_N
H84	PE_E2_P0_P_PIN_DAT_08_P
H86	GND
H88	GND
H90	DM_DDR6_BI_DQS_07_P
H92	DM_DDR6_BI_DQ_61
H94	VDDR67_1P20
J01	DM_DDR1_BI_DQ_51
J03	GND
J05	DM_DDR0_BI_DQ_60
J07	DM_DDR0_BI_DQ_56
J09	VDDR01_1P20

Pin Number	Signal
J11	GND
J13	PE_E1_PIN_P_P0_DAT_07_P
J15	PE_E1_PIN_P_P0_DAT_07_N
J17	GND
J19	GND
J21	GND
J23	PV_E0_P0_P_PIN_SLOT_CLK_N
J25	PV_E0_P0_P_PIN_SLOT_CLK_P
J27	GND
J29	PE_E1_P0_P_PIN_DAT_13_N
J31	PE_E1_P0_P_PIN_DAT_13_P
J33	GND
J35	GND
J37	PE_E0_PIN_P_P0_DAT_02_N
J39	PE_E0_PIN_P_P0_DAT_02_P
J41	GND
J43	GND
J45	TS_JTAG_PIN_P_P0_TMS
J47	PV_TPM_P0_P_PIN_RESET
J49	GND
J51	PV_AVS0_P0_P_PIN_MDATA
J53	PV_AVS1_P0_P_PIN_CLK
J55	PV_AVS1_PIN_P_P0_SDATA
J57	GND
J59	GND
J61	GND
J63	PV_PRV_P0_B_PIN_LPC_DAT_1
J65	PV_PRV_P0_P_PIN_LPC_-FRAME_B
J67	GND
J69	GND
J71	GND
J73	GND
J75	PV_E2C_P0_P_PIN_SLOT_CLK_P
J77	PV_E2C_P0_P_PIN_SLOT_CLK_N
J79	GND
J81	PE_E2_P0_P_PIN_DAT_06_N
J83	PE_E2_P0_P_PIN_DAT_06_P
J85	GND
J87	VDDR67_1P20

Pin Number	Signal
J89	DM_DDR6_BI_DQ_56
J91	DM_DDR6_BI_DQ_60
J93	GND
J95	DM_DDR7_BI_DQS_06_P
K02	DM_DDR1_BI_DQ_50
K04	VDDR01_1P20
K06	DM_DDR0_BI_DQ_55
K08	DM_DDR0_BI_DQ_57
K10	GND
K12	GND
K14	PE_E1_PIN_P_P0_DAT_08_N
K16	PE_E1_PIN_P_P0_DAT_08_P
K18	GND
K20	GND
K22	PV_E1A_P0_P_PIN_SLOT_CLK_N
K24	PV_E1A_P0_P_PIN_SLOT_CLK_P
K26	GND
K28	PE_E1_P0_P_PIN_DAT_15_N
K30	PE_E1_P0_P_PIN_DAT_15_P
K32	GND
K34	GND
K36	PE_E0_PIN_P_P0_DAT_01_P
K38	PE_E0_PIN_P_P0_DAT_01_N
K40	GND
K42	TS_NESTLCPLL_P0_P_PIN_HF-C_N
K44	TS_NESTLCPLL_P0_P_PIN_HF-C_P
K46	TS_JTAG_P0_P_PIN_TDO
K48	GND
K50	TS_JTAG_PIN_P_P0_TCK
K52	PV_AVS0_P0_P_PIN_CLK
K54	GND
K56	GND
K58	GND
K60	GND
K62	GND
K64	PV_PRV_P0_P_PIN_LPC_RE-SET_B
K66	GND
K68	PV_LP_P0_B_PIN_I2C_SCL_B

Pin Number	Signal
K70	GND
K72	GND
K74	PV_E2B_P0_P_PIN_SLOT_CLK_P
K76	PV_E2B_P0_P_PIN_SLOT_CLK_N
K78	GND
K80	PE_E2_P0_P_PIN_DAT_07_P
K82	PE_E2_P0_P_PIN_DAT_07_N
K84	GND
K86	GND
K88	DM_DDR6_BI_DQ_57
K90	DM_DDR6_BI_DQ_55
K92	VDDR67_1P20
K94	DM_DDR7_BI_DQS_06_N
L01	DM_DDR1_BI_DQS_06_P
L03	DM_DDR1_BI_DQ_55
L05	GND
L07	DM_DDR0_BI_DQ_54
L09	DM_DDR0_BI_DQ_50
L11	VDDR01_1P20
L13	GND
L15	PE_E1_PIN_P_P0_DAT_09_P
L17	PE_E1_PIN_P_P0_DAT_09_N
L19	GND
L21	PV_E1B_P0_P_PIN_SLOT_CLK_N
L23	PV_E1B_P0_P_PIN_SLOT_CLK_P
L25	GND
L27	PE_E1_P0_P_PIN_DAT_14_N
L29	PE_E1_P0_P_PIN_DAT_14_P
L31	GND
L33	GND
L35	PE_E0_PIN_P_P0_DAT_00_P
L37	PE_E0_PIN_P_P0_DAT_00_N
L39	GND
L41	GND
L43	GND
L45	GND
L47	GND
L49	GND
L51	GND

Pin Number	Signal
L53	GND
L55	PV_FSP0_P0_B_PIN_FSI_DAT
L57	GND
L59	PV_CP1_P0_B_PIN_FSI_DAT
L61	GND
L63	TS_TST_PIN_P_P0_LSSD_TE
L65	GND
L67	PV_LP_P0_B_PIN_I2C_SDA_B
L69	PV_PCI_P0_B_PIN_I2C_SCL_B
L71	GND
L73	PV_E2A_P0_P_PIN_SLOT_CLK_P
L75	PV_E2A_P0_P_PIN_SLOT_CLK_N
L77	GND
L79	PE_E2_P0_P_PIN_DAT_05_P
L81	PE_E2_P0_P_PIN_DAT_05_N
L83	GND
L85	VDDR67_1P20
L87	DM_DDR6_BI_DQ_50
L89	DM_DDR6_BI_DQ_54
L91	GND
L93	DM_DDR7_BI_DQS_15_N
L95	DM_DDR7_BI_DQ_49
M02	DM_DDR1_BI_DQS_06_N
M04	DM_DDR1_BI_DQ_54
M06	VDDR01_1P20
M08	DM_DDR0_BI_DQS_15_N
M10	DM_DDR0_BI_DQ_51
M12	GND
M14	GND
M16	PE_E1_PIN_P_P0_DAT_10_P
M18	PE_E1_PIN_P_P0_DAT_10_N
M20	GND
M22	PV_E1_P0_P_PIN_TERMREF_P
M24	PV_E1_P0_P_PIN_TERMREF_N
M26	GND
M28	GND
M30	GND
M32	GND
M34	GND

Pin Number	Signal
M36	GND
M38	GND
M40	GND
M42	PV_SYS0_PIN_P_P0_REFCLK_N
M44	PV_SYS0_PIN_P_P0_REFCLK_P
M46	GND
M48	PV_PCI0_PIN_P_P0_REFCLK_P
M50	PV_PCI0_PIN_P_P0_REFCLK_N
M52	GND
M54	PV_FSP0_PIN_P_P0_FSI_CLK
M56	GND
M58	PV_CP1_P0_P_PIN_FSI_CLK
M60	GND
M62	GND
M64	PV_PRV_PIN_P_P0_STBY_RE-SET_B
M66	GND
M68	GND
M70	PV_PCI_P0_B_PIN_I2C_SDA_B
M72	GND
M74	GND
M76	GND
M78	PE_E2_P0_P_PIN_DAT_04_N
M80	PE_E2_P0_P_PIN_DAT_04_P
M82	GND
M84	GND
M86	DM_DDR6_BI_DQ_51
M88	DM_DDR6_BI_DQS_15_N
M90	VDDR67_1P20
M92	DM_DDR7_BI_DQS_15_P
M94	DM_DDR7_BI_DQ_48
N01	GND
N03	DM_DDR1_BI_DQ_49
N05	DM_DDR1_BI_DQS_15_N
N07	GND
N09	DM_DDR0_BI_DQS_15_P
N11	DM_DDR0_BI_DQS_06_N
N13	VDDR01_1P20
N15	GND
N17	PE_E1_PIN_P_P0_DAT_11_P

Pin Number	Signal
N19	PE_E1_PIN_P_P0_DAT_11_N
N21	GND
N23	GND
N25	VIO_1P00
N27	VIO_1P00
N29	TS_E1_P0_P_PIN_ATST
N31	PV_E0_P0_P_PIN_TERMREF_P
N33	PV_E0_P0_P_PIN_TERMREF_N
N35	VIO_1P00
N37	GND
N39	TS_E0_P0_P_PIN_ATST
N41	VIO_1P00
N43	TS_NESTLCPLL_P0_P_PIN_ATST
N45	VIO_1P00
N47	GND
N49	GND
N51	VSB_1P10
N53	VSB_1P10
N55	GND
N57	VSB0_3P30
N59	VSB0_3P30
N61	VIO_1P00
N63	VIO_1P00
N65	TS_E2_P0_P_PIN_ATST
N67	VIO_1P00
N69	VIO_1P00
N71	GND
N73	PV_E2_P0_P_PIN_TERMREF_P
N75	GND
N77	PE_E2_P0_P_PIN_DAT_03_N
N79	PE_E2_P0_P_PIN_DAT_03_P
N81	GND
N83	VDDR67_1P20
N85	DM_DDR6_BI_DQS_06_N
N87	DM_DDR6_BI_DQS_15_P
N89	GND
N91	DM_DDR7_BI_DQ_53
N93	DM_DDR7_BI_DQ_52
N95	GND

Pin Number	Signal
P02	VDDR01_1P20
P04	DM_DDR1_BI_DQ_48
P06	DM_DDR1_BI_DQS_15_P
P08	VDDR01_1P20
P10	DM_DDR0_BI_DQ_53
P12	DM_DDR0_BI_DQS_06_P
P14	GND
P16	GND
P18	PE_E1_PIN_P_P0_DAT_12_P
P20	PE_E1_PIN_P_P0_DAT_12_N
P22	GND
P24	GND
P26	VDN_0P70
P28	GND
P30	VDN_0P70
P32	GND
P34	VDN_0P70
P36	GND
P38	VDN_0P70
P40	GND
P42	VDN_0P70
P44	GND
P46	VIO_1P00
P48	GND
P50	VDN_0P70
P52	GND
P54	VDN_0P70
P56	GND
P58	VDN_0P70
P60	GND
P62	VDN_0P70
P64	GND
P66	VDN_0P70
P68	GND
P70	VDN_0P70
P72	PV_E2_P0_P_PIN_TERMREF_N
P74	GND
P76	PE_E2_P0_P_PIN_DAT_02_N
P78	PE_E2_P0_P_PIN_DAT_02_P

Pin Number	Signal
P80	GND
P82	GND
P84	DM_DDR6_BI_DQS_06_P
P86	DM_DDR6_BI_DQ_53
P88	VDDR67_1P20
P90	DM_DDR7_BI_DQ_55
P92	DM_DDR7_BI_DQ_54
P94	VDDR67_1P20
R01	DM_DDR1_BI_DQ_43
R03	GND
R05	DM_DDR1_BI_DQ_52
R07	DM_DDR1_BI_DQ_53
R09	GND
R11	DM_DDR0_BI_DQ_52
R13	DM_DDR0_BI_DQ_48
R15	VDDR01_1P20
R17	GND
R19	PE_E1_PIN_P_P0_DAT_13_N
R21	PE_E1_PIN_P_P0_DAT_13_P
R23	GND
R25	VIO_1P00
R27	GND
R29	GND
R31	VDD_0P80
R33	GND
R35	VDD_0P80
R37	GND
R39	VDD_0P80
R41	GND
R43	VDD_0P80
R45	GND
R47	VDD_0P80
R49	TS_EX06_P0_P_PIN_TDIODE_A
R51	VDD_0P80
R53	GND
R55	VDN_0P70
R57	GND
R59	VDD_0P80
R61	GND

Pin Number	Signal
R63	VDD_0P80
R65	GND
R67	VDD_0P80
R69	GND
R71	VIO_1P00
R73	GND
R75	PE_E2_P0_P_PIN_DAT_01_P
R77	PE_E2_P0_P_PIN_DAT_01_N
R79	GND
R81	VDDR67_1P20
R83	DM_DDR6_BI_DQ_48
R85	DM_DDR6_BI_DQ_52
R87	GND
R89	DM_DDR7_BI_DQ_51
R91	DM_DDR7_BI_DQ_50
R93	GND
R95	DM_DDR7_BI_DQS_05_P
T02	DM_DDR1_BI_DQ_42
T04	VDDR01_1P20
T06	DM_DDR1_BI_DQ_60
T08	DM_DDR1_BI_DQ_61
T10	VDDR01_1P20
T12	DM_DDR0_BI_DQ_47
T14	DM_DDR0_BI_DQ_49
T16	GND
T18	GND
T20	PE_E1_PIN_P_P0_DAT_14_N
T22	PE_E1_PIN_P_P0_DAT_14_P
T24	GND
T26	VDN_0P70
T28	VDD_0P80
T30	GND
T32	VDD_0P80
T34	GND
T36	VCS_0P96
T38	TS_EX0203_P0_P_PIN_VWL_V-SENSE
T40	VDN_0P70
T42	TS_EX0203_P0_P_PIN_L3_G-SENSE

Pin Number	Signal
T44	VCS_0P96
T46	GND
T48	VDD_0P80
T50	TS_EX06_P0_P_PIN_TDIODE_C
T52	VDD_0P80
T54	GND
T56	VDD_0P80
T58	GND
T60	VCS_0P96
T62	GND
T64	VDD_0P80
T66	GND
T68	VDD_0P80
T70	VDN_0P70
T72	GND
T74	PE_E2_P0_P_PIN_DAT_00_N
T76	PE_E2_P0_P_PIN_DAT_00_P
T78	GND
T80	GND
T82	DM_DDR6_BI_DQ_49
T84	DM_DDR6_BI_DQ_47
T86	VDDR67_1P20
T88	DM_DDR7_BI_DQ_61
T90	DM_DDR7_BI_DQ_60
T92	VDDR67_1P20
T94	DM_DDR7_BI_DQS_05_N
U01	DM_DDR1_BI_DQ_46
U03	DM_DDR1_BI_DQ_47
U05	GND
U07	DM_DDR1_BI_DQ_56
U09	DM_DDR1_BI_DQ_57
U11	GND
U13	DM_DDR0_BI_DQ_46
U15	DM_DDR0_BI_DQ_42
U17	VDDR01_1P20
U19	GND
U21	PE_E1_PIN_P_P0_DAT_15_N
U23	PE_E1_PIN_P_P0_DAT_15_P
U25	GND

Pin Number	Signal
U27	GND
U29	VDD_0P80
U31	GND
U33	VDD_0P80
U35	TS_CACHE0203_P0_P_PIN_G-SENSE
U37	VDD_0P80
U39	TS_EX0203_P0_P_PIN_VBL_V-SENSE
U41	VDD_0P80
U43	TS_EX0203_P0_P_PIN_VPP_V-SENSE
U45	VDD_0P80
U47	GND
U49	VDD_0P80
U51	GND
U53	VDN_0P70
U55	GND
U57	VDD_0P80
U59	GND
U61	VDD_0P80
U63	GND
U65	VDD_0P80
U67	GND
U69	GND
U71	VIO_1P00
U73	GND
U75	GND
U77	GND
U79	VDDR67_1P20
U81	DM_DDR6_BI_DQ_42
U83	DM_DDR6_BI_DQ_46
U85	GND
U87	DM_DDR7_BI_DQ_57
U89	DM_DDR7_BI_DQ_56
U91	GND
U93	DM_DDR7_BI_DQS_14_N
U95	DM_DDR7_BI_DQ_41
V02	DM_DDR1_BI_DQS_05_N
V04	DM_DDR1_BI_DQS_05_P
V06	VDDR01_1P20

Pin Number	Signal
V08	DM_DDR1_BI_DQS_16_P
V10	DM_DDR1_BI_DQS_16_N
V12	VDDR01_1P20
V14	DM_DDR0_BI_DQS_14_N
V16	DM_DDR0_BI_DQ_43
V18	GND
V20	GND
V22	GND
V24	GND
V26	VDN_0P70
V28	GND
V30	VDD_0P80
V32	GND
V34	TS_EQ1_P0_P_PIN_VCSIN_ VSENSE
V36	TS_-CACHE0203_P0_P_PIN_VCS_V-SENSE
V38	VCS_0P96
V40	GND
V42	VCS_0P96
V44	GND
V46	VDD_0P80
V48	GND
V50	VDD_0P80
V52	GND
V54	VDN_0P70
V56	GND
V58	VCS_0P96
V60	GND
V62	VDD_0P80
V64	GND
V66	VDD_0P80
V68	GND
V70	VDN_0P70
V72	GND
V74	PV_E2C_PIN_P_P0_PRSNT_B
V76	PV_E2B_PIN_P_P0_PRSNT_B
V78	GND
V80	DM_DDR6_BI_DQ_43
V82	DM_DDR6_BI_DQS_14_N

Pin Number	Signal
V84	VDDR67_1P20
V86	DM_DDR7_BI_DQS_07_N
V88	DM_DDR7_BI_DQS_16_P
V90	VDDR67_1P20
V92	DM_DDR7_BI_DQS_14_P
V94	DM_DDR7_BI_DQ_40
W01	GND
W03	DM_DDR1_BI_DQS_14_P
W05	DM_DDR1_BI_DQS_14_N
W07	GND
W09	DM_DDR1_BI_DQS_07_N
W11	DM_DDR1_BI_DQS_07_P
W13	GND
W15	DM_DDR0_BI_DQS_14_P
W17	DM_DDR0_BI_DQS_05_N
W19	VDDR01_1P20
W21	PV_E1A_PIN_P_P0_PRSNT_B
W23	PV_E1A_P0_P_PIN_PERST_B
W25	VDN_0P70
W27	GND
W29	GND
W31	VDD_0P80
W33	GND
W35	VDD_0P80
W37	GND
W39	VDD_0P80
W41	GND
W43	VDD_0P80
W45	GND
W47	VDD_0P80
W49	GND
W51	VDD_0P80
W53	GND
W55	VDD_0P80
W57	GND
W59	VDD_0P80
W61	GND
W63	VDD_0P80
W65	GND

Pin Number	Signal
W67	VDD_0P80
W69	GND
W71	GND
W73	PV_E2A_PIN_P_P0_PRSNT_B
W75	PV_E2C_P0_P_PIN_PERST_B
W77	VDDR67_1P20
W79	DM_DDR6_BI_DQS_05_N
W81	DM_DDR6_BI_DQS_14_P
W83	GND
W85	DM_DDR7_BI_DQS_07_P
W87	DM_DDR7_BI_DQS_16_N
W89	GND
W91	DM_DDR7_BI_DQ_46
W93	DM_DDR7_BI_DQ_44
W95	GND
Y02	VDDR01_1P20
Y04	DM_DDR1_BI_DQ_40
Y06	DM_DDR1_BI_DQ_41
Y08	VDDR01_1P20
Y10	DM_DDR1_BI_DQ_62
Y12	DM_DDR1_BI_DQ_63
Y14	VDDR01_1P20
Y16	DM_DDR0_BI_DQ_45
Y18	DM_DDR0_BI_DQS_05_P
Y20	GND
Y22	PV_E1B_P0_P_PIN_PERST_B
Y24	GND
Y26	VDD_0P80
Y28	VDD_0P80
Y30	GND
Y32	VDD_0P80
Y34	GND
Y36	VCS_0P96
Y38	GND
Y40	VDD_0P80
Y42	GND
Y44	VCS_0P96
Y46	GND
Y48	VDD_0P80

Pin Number	Signal
Y50	GND
Y52	VDD_0P80
Y54	GND
Y56	VDD_0P80
Y58	GND
Y60	VCS_0P96
Y62	GND
Y64	VDD_0P80
Y66	GND
Y68	VDD_0P80
Y70	VDD_0P80
Y72	GND
Y74	PV_E2B_P0_P_PIN_PERST_B
Y76	GND
Y78	DM_DDR6_BI_DQS_05_P
Y80	DM_DDR6_BI_DQ_45
Y82	VDDR67_1P20
Y84	DM_DDR7_BI_DQ_63
Y86	DM_DDR7_BI_DQ_62
Y88	VDDR67_1P20
Y90	DM_DDR7_BI_DQ_47
Y92	DM_DDR7_BI_DQ_45
Y94	VDDR67_1P20
AA01	DM_DDR1_BI_DQ_35
AA03	GND
AA05	DM_DDR1_BI_DQ_44
AA07	DM_DDR1_BI_DQ_45
AA09	GND
AA11	DM_DDR1_BI_DQ_58
AA13	DM_DDR1_BI_DQ_59
AA15	GND
AA17	DM_DDR0_BI_DQ_44
AA19	DM_DDR0_BI_DQ_40
AA21	VDDR01_1P20
AA23	PV_E1B_PIN_P_P0_PRSNT_B
AA25	GND
AA27	GND
AA29	VDD_0P80
AA31	GND

Pin Number	Signal
AA33	VDD_0P80
AA35	GND
AA37	VDD_0P80
AA39	GND
AA41	VDD_0P80
AA43	GND
AA45	VDD_0P80
AA47	GND
AA49	VDD_0P80
AA51	GND
AA53	VDD_0P80
AA55	GND
AA57	VDD_0P80
AA59	GND
AA61	VDD_0P80
AA63	GND
AA65	VDD_0P80
AA67	GND
AA69	VDN_0P70
AA71	GND
AA73	PV_E2A_P0_P_PIN_PERST_B
AA75	VDDR67_1P20
AA77	DM_DDR6_BI_DQ_40
AA79	DM_DDR6_BI_DQ_44
AA81	GND
AA83	DM_DDR7_BI_DQ_59
AA85	DM_DDR7_BI_DQ_58
AA87	GND
AA89	DM_DDR7_BI_DQ_42
AA91	DM_DDR7_BI_DQ_39
AA93	GND
AA95	DM_DDR7_BI_DQS_04_P
AB02	DM_DDR1_BI_DQ_38
AB04	VDDR01_1P20
AB06	DM_DDR1_BI_DQ_39
AB08	DM_DDR1_BI_DQ_34
AB10	VDDR01_1P20
AB12	GND
AB14	GND

Pin Number	Signal
AB16	VDDR01_1P20
AB18	DM_DDR0_BI_DQ_39
AB20	DM_DDR0_BI_DQ_41
AB22	GND
AB24	GND
AB26	VDN_0P70
AB28	GND
AB30	VDD_0P80
AB32	GND
AB34	VDD_0P80
AB36	GND
AB38	VCS_0P96
AB40	GND
AB42	VCS_0P96
AB44	GND
AB46	VDD_0P80
AB48	GND
AB50	VDD_0P80
AB52	GND
AB54	VDN_0P70
AB56	GND
AB58	VCS_0P96
AB60	GND
AB62	VDD_0P80
AB64	GND
AB66	VDD_0P80
AB68	GND
AB70	VDN_0P70
AB72	GND
AB74	GND
AB76	DM_DDR6_BI_DQ_41
AB78	DM_DDR6_BI_DQ_39
AB80	VDDR67_1P20
AB82	GND
AB84	GND
AB86	VDDR67_1P20
AB88	DM_DDR7_BI_DQ_43
AB90	DM_DDR7_BI_DQ_38
AB92	VDDR67_1P20

Pin Number	Signal
AB94	DM_DDR7_BI_DQS_04_N
AC01	DM_DDR1_BI_DQS_13_N
AC03	DM_DDR1_BI_DQS_13_P
AC05	GND
AC07	DM_DDR1_BI_DQS_04_P
AC09	DM_DDR1_BI_DQS_04_N
AC11	GND
AC13	DM_DDR0_BI_DQS_04_P
AC15	DM_DDR0_BI_DQS_13_N
AC17	GND
AC19	DM_DDR0_BI_DQ_38
AC21	DM_DDR0_BI_DQ_34
AC23	GND
AC25	VDDR01_1P20
AC27	GND
AC29	GND
AC31	VDD_0P80
AC33	GND
AC35	VDD_0P80
AC37	GND
AC39	VDD_0P80
AC41	GND
AC43	VDD_0P80
AC45	GND
AC47	VDD_0P80
AC49	GND
AC51	VDD_0P80
AC53	GND
AC55	VDN_0P70
AC57	GND
AC59	VDD_0P80
AC61	GND
AC63	VDD_0P80
AC65	GND
AC67	VDD_0P80
AC69	GND
AC71	VDDR67_1P20
AC73	GND
AC75	DM_DDR6_BI_DQ_34

Pin Number	Signal
AC77	DM_DDR6_BI_DQ_38
AC79	GND
AC81	DM_DDR6_BI_DQS_13_N
AC83	DM_DDR6_BI_DQS_04_P
AC85	GND
AC87	DM_DDR7_BI_DQ_35
AC89	DM_DDR7_BI_DQS_13_N
AC91	GND
AC93	DM_DDR7_BI_DQ_32
AC95	DM_DDR7_BI_DQ_33
AD02	DM_DDR1_BI_DQ_32
AD04	DM_DDR1_BI_DQ_33
AD06	VDDR01_1P20
AD08	DM_DDR1_BI_DQ_37
AD10	DM_DDR1_BI_DQ_36
AD12	VDDR01_1P20
AD14	DM_DDR0_BI_DQS_04_N
AD16	DM_DDR0_BI_DQS_13_P
AD18	VDDR01_1P20
AD20	DM_DDR0_BI_DQ_37
AD22	DM_DDR0_BI_DQ_35
AD24	GND
AD26	VDN_0P70
AD28	VDD_0P80
AD30	GND
AD32	VDD_0P80
AD34	GND
AD36	VCS_0P96
AD38	GND
AD40	VDN_0P70
AD42	GND
AD44	VCS_0P96
AD46	GND
AD48	VDD_0P80
AD50	GND
AD52	VDD_0P80
AD54	GND
AD56	VDD_0P80
AD58	GND

Pin Number	Signal
AD60	VCS_0P96
AD62	GND
AD64	VDD_0P80
AD66	GND
AD68	VDD_0P80
AD70	VDN_0P70
AD72	GND
AD74	DM_DDR6_BI_DQ_35
AD76	DM_DDR6_BI_DQ_32
AD78	VDDR67_1P20
AD80	DM_DDR6_BI_DQS_13_P
AD82	DM_DDR6_BI_DQS_04_N
AD84	VDDR67_1P20
AD86	DM_DDR7_BI_DQ_34
AD88	DM_DDR7_BI_DQS_13_P
AD90	VDDR67_1P20
AD92	DM_DDR7_BI_DQ_37
AD94	GND
AE01	GND
AE03	GND
AE05	GND
AE07	GND
AE09	GND
AE11	GND
AE13	GND
AE15	DM_DDR0_BI_DQ_33
AE17	DM_DDR0_BI_DQ_32
AE19	GND
AE21	DM_DDR0_BI_DQ_36
AE23	GND
AE25	GND
AE27	GND
AE29	VDD_0P80
AE31	GND
AE33	VDD_0P80
AE35	GND
AE37	VDD_0P80
AE39	GND
AE41	VDD_0P80

Pin Number	Signal
AE43	GND
AE45	VDD_0P80
AE47	GND
AE49	VDD_0P80
AE51	TS_DTSNPU_P0_P_PIN_TEST_OUT
AE53	VDD_0P80
AE55	GND
AE57	VDD_0P80
AE59	GND
AE61	VDD_0P80
AE63	GND
AE65	VDD_0P80
AE67	GND
AE69	VDD_0P80
AE71	GND
AE73	GND
AE75	DM_DDR6_BI_DQ_36
AE77	GND
AE79	DM_DDR6_BI_DQ_37
AE81	DM_DDR6_BI_DQ_33
AE83	GND
AE85	GND
AE87	GND
AE89	GND
AE91	GND
AE93	DM_DDR7_BI_DQ_36
AF02	GND
AF04	GND
AF06	DM_DDR1_P0_P_PIN_CHIPID_1
AF08	GND
AF10	GND
AF12	DM_DDR1_P0_P_PIN_CHIPID_0
AF14	VDDR01_1P20
AF16	GND
AF18	GND
AF20	VDDR01_1P20
AF22	GND
AF24	VDDR01_1P20
AF26	VDN_0P70

Pin Number	Signal
AF28	GND
AF30	VDN_0P70
AF32	GND
AF34	VDN_0P70
AF36	GND
AF38	VDN_0P70
AF40	GND
AF42	VDN_0P70
AF44	GND
AF46	TS_EQALL_P0_P_PIN_AMUX_VSENSE
AF48	TS_EQALL_P0_P_PIN_AMUX_GSENSE
AF50	VDN_0P70
AF52	GND
AF54	VDN_0P70
AF56	GND
AF58	VDN_0P70
AF60	GND
AF62	VDN_0P70
AF64	GND
AF66	VDN_0P70
AF68	GND
AF70	VDN_0P70
AF72	VDDR67_1P20
AF74	GND
AF76	VDDR67_1P20
AF78	GND
AF80	GND
AF82	GND
AF84	DM_DDR7_P0_P_PIN_CHIPID_0
AF86	VDDR67_1P20
AF88	GND
AF90	DM_DDR7_P0_P_PIN_CHIPID_2
AF92	VDDR67_1P20
AG01	DM_DDR1_P0_P_PIN_CHIPID_2
AG03	DM_DDR1_P0_P_PIN_ODT_3
AG05	DM_DDR1_P0_P_PIN_CS_B_1
AG07	DM_DDR1_P0_P_PIN_ODT_0
AG09	DM_DDR1_P0_P_PIN_ADDR_15

Pin Number	Signal
AG11	DM_DDR1_P0_P_PIN_ADDR_17
AG13	DM_DDR1_P0_P_PIN_ODT_1
AG15	GND
AG17	GND
AG19	GND
AG21	PV_DDR0123_P0_P_PIN_TERMREF_P
AG23	GND
AG25	VDN_0P70
AG27	VDN_0P70
AG29	GND
AG31	VDN_0P70
AG33	GND
AG35	VCS_0P96
AG37	GND
AG39	VCS_0P96
AG41	GND
AG43	VDN_0P70
AG45	GND
AG47	VDN_0P70
AG49	GND
AG51	VDN_0P70
AG53	GND
AG55	VDN_0P70
AG57	GND
AG59	VDN_0P70
AG61	GND
AG63	VDN_0P70
AG65	GND
AG67	VDN_0P70
AG69	GND
AG71	GND
AG73	PV_DDR4567_P0_P_PIN_TERMREF_N
AG75	GND
AG77	VDDR67_1P20
AG79	GND
AG81	VDDR67_1P20
AG83	DM_DDR7_P0_P_PIN_CHIPID_1
AG85	DM_DDR7_P0_P_PIN_ODT_3

Pin Number	Signal
AG87	DM_DDR7_P0_P_PIN_ODT_1
AG89	DM_DDR7_P0_P_PIN_CS_B_1
AG91	DM_DDR7_P0_P_PIN_ADDR_17
AG93	GND
AH02	VDDR01_1P20
AH04	DM_DDR1_P0_P_PIN_CS_B_0
AH06	VDDR01_1P20
AH08	DM_D-DR1_P0_P_PIN_BANK_ADR_0
AH10	VDDR01_1P20
AH12	DM_DDR1_P0_P_PIN_ADDR_16
AH14	VDDR01_1P20
AH16	DM_DDR1_P0_P_PIN_ADDR_00
AH18	VDDR01_1P20
AH20	PV_DDR0123_P0_P_PIN_TERMREF_N
AH22	VDDR01_1P20
AH24	GND
AH26	GND
AH28	VDN_0P70
AH30	GND
AH32	VDN_0P70
AH34	GND
AH36	VCS_0P96
AH38	GND
AH40	VCS_0P96
AH42	GND
AH44	AVDD_1P50
AH46	AVDD_1P50
AH48	VDN_0P70
AH50	DVDD_1P50
AH52	DVDD_1P50
AH54	GND
AH56	VDN_0P70
AH58	GND
AH60	VDN_0P70
AH62	GND
AH64	VDN_0P70
AH66	GND
AH68	VDN_0P70

Pin Number	Signal
AH70	VDDR67_1P20
AH72	PV_DDR4567_P0_P_PIN_TERM-REF_P
AH74	VDDR67_1P20
AH76	GND
AH78	GND
AH80	DM_DDR7_P0_P_PIN_ADDR_13
AH82	GND
AH84	DM_DDR7_P0_P_PIN_ODT_0
AH86	GND
AH88	DM_DDR7_P0_P_PIN_ODT_2
AH90	GND
AH92	DM_DDR7_P0_P_PIN_CS_B_3
AJ01	DM_DDR1_P0_P_PIN_ADDR_13
AJ03	DM_DDR1_P0_P_PIN_CS_B_3
AJ05	DM_DDR1_P0_P_PIN_ADDR_10
AJ07	DM_D-DR1_P0_P_PIN_BANK_ADR_1
AJ09	DM_DDR1_P0_P_PIN_PAR
AJ11	DM_DDR1_P0_P_PIN_ADDR_01
AJ13	DM_DDR1_P0_P_PIN_ADDR_05
AJ15	DM_DDR1_P0_P_PIN_ADDR_09
AJ17	DM_D-DR1_P0_P_PIN_BANK_GRP_1
AJ19	DM_DDR1_P0_P_PIN_RESET_B
AJ21	GND
AJ23	GND
AJ25	VDDR01_1P20
AJ27	GND
AJ29	VDN_0P70
AJ31	GND
AJ33	VDN_0P70
AJ35	GND
AJ37	VDN_0P70
AJ39	GND
AJ41	VDN_0P70
AJ43	GND
AJ45	VDN_0P70
AJ47	GND
AJ49	VDN_0P70
AJ51	GND

Pin Number	Signal
AJ53	VDN_0P70
AJ55	VDN_CHIP_GSENSE
AJ57	VDN_CHIP_VSENSE
AJ59	TS_VCS_P0_P_PIN_VSENSE
AJ61	VDN_0P70
AJ63	GND
AJ65	VDN_0P70
AJ67	GND
AJ69	VDN_0P70
AJ71	GND
AJ73	GND
AJ75	GND
AJ77	DM_DDR7_PIN_P_P0_ERR_B
AJ79	DM_DDR7_P0_P_PIN_ADDR_04
AJ81	DM_DDR7_P0_P_PIN_ADDR_01
AJ83	DM_D-DR7_P0_P_PIN_BANK_ADR_1
AJ85	DM_DDR7_P0_P_PIN_ADDR_16
AJ87	DM_DDR7_P0_P_PIN_CS_B_2
AJ89	DM_DDR7_P0_P_PIN_ADDR_14
AJ91	DM_DDR7_P0_P_PIN_CS_B_0
AJ93	DM_DDR7_P0_P_PIN_ADDR_15
AJ95	GND
AK02	DM_DDR1_P0_P_PIN_ODT_2
AK04	GND
AK06	DM_DDR1_PIN_P_P0_EVENT_B
AK08	GND
AK10	DM_DDR1_P0_P_PIN_ADDR_02
AK12	GND
AK14	DM_DDR1_P0_P_PIN_ADDR_07
AK16	GND
AK18	DM_DDR1_P0_P_PIN_CKE_0
AK20	GND
AK22	GND
AK24	GND
AK26	VDN_0P70
AK28	GND
AK30	VDN_0P70
AK32	TS_EX01C1_P0_P_PIN_VSENSE
AK34	VDN_0P70

Pin Number	Signal
AK36	GND
AK38	VDN_0P70
AK40	GND
AK42	VCS_CHIP_VSENSE
AK44	GND
AK46	VDD_CHIP_VSENSE
AK48	GND
AK50	VDN_0P70
AK52	TS_EFUSE_PIN_P_P0_FSOURCE
AK54	VDN_0P70
AK56	GND
AK58	VDN_0P70
AK60	TS_VDN_P0_P_PIN_GSENSE
AK62	VCS_0P96
AK64	GND
AK66	VDN_0P70
AK68	GND
AK70	VDN_0P70
AK72	GND
AK74	TS_DDR4567_P0_P_PIN_ATST
AK76	VDDR67_1P20
AK78	DM_DDR7_P0_P_PIN_CKE_3
AK80	VDDR67_1P20
AK82	DM_DDR7_P0_P_PIN_ADDR_11
AK84	VDDR67_1P20
AK86	DM_DDR7_PIN_P_P0_EVENT_B
AK88	VDDR67_1P20
AK90	DM_D-DR7_P0_P_PIN_BANK_ADR_0
AK92	VDDR67_1P20
AK94	DM_DDR7_P0_P_PIN_ADDR_10
AL01	DM_DDR1_P0_P_PIN_ADDR_14
AL03	DM_DDR1_P0_P_PIN_CS_B_2
AL05	DM_DDR1_P0_P_PIN_CLK_0_P
AL07	DM_DDR1_P0_P_PIN_CLK_1_N
AL09	DM_DDR1_P0_P_PIN_CLK_1_P
AL11	DM_DDR1_P0_P_PIN_ADDR_04
AL13	DM_DDR1_P0_P_PIN_ADDR_08
AL15	DM_DDR1_P0_P_PIN_ADDR_11
AL17	DM_DDR1_P0_P_PIN_ACT_B

Pin Number	Signal
AL19	DM_DDR1_P0_P_PIN_CKE_1
AL21	GND
AL23	GND
AL25	GND
AL27	GND
AL29	GND
AL31	VDD_0P80
AL33	TS_EX01C1_P0_P_PIN_GSENSE
AL35	VDD_0P80
AL37	GND
AL39	VDD_0P80
AL41	VCS_CHIP_GSENSE
AL43	VDD_0P80
AL45	VDD_CHIP_GSENSE
AL47	VDD_0P80
AL49	TS_EX05_P0_P_PIN_TDIODE_A
AL51	VDD_0P80
AL53	GND
AL55	VDN_0P70
AL57	GND
AL59	VDD_0P80
AL61	TS_VDN_P0_P_PIN_VSENSE
AL63	VDD_0P80
AL65	GND
AL67	VDD_0P80
AL69	GND
AL71	GND
AL73	GND
AL75	GND
AL77	DM_DDR7_P0_P_PIN_RESET_B
AL79	DM_DDR7_P0_P_PIN_ACT_B
AL81	DM_DDR7_P0_P_PIN_ADDR_12
AL83	DM_DDR7_P0_P_PIN_ADDR_07
AL85	DM_DDR7_P0_P_PIN_ADDR_03
AL87	DM_DDR7_P0_P_PIN_ADDR_02
AL89	DM_DDR7_P0_P_PIN_CLK_0_P
AL91	DM_DDR7_P0_P_PIN_CLK_1_P
AL93	DM_DDR7_P0_P_PIN_PAR
AL95	DM_DDR7_P0_P_PIN_ADDR_00

Pin Number	Signal
AM02	VDDR01_1P20
AM04	DM_DDR1_P0_P_PIN_CLK_0_N
AM06	VDDR01_1P20
AM08	DM_DDR1_P0_P_PIN_ADDR_03
AM10	VDDR01_1P20
AM12	DM_DDR1_P0_P_PIN_ADDR_06
AM14	VDDR01_1P20
AM16	DM_DDR1_PIN_P_P0_ERR_B
AM18	VDDR01_1P20
AM20	GND
AM22	TS_DDR0123_P0_P_PIN_ATST
AM24	VDDR01_1P20
AM26	VDN_0P70
AM28	VDD_0P80
AM30	GND
AM32	VDD_0P80
AM34	GND
AM36	VCS_0P96
AM38	GND
AM40	VDN_0P70
AM42	GND
AM44	VCS_0P96
AM46	GND
AM48	VDD_0P80
AM50	TS_EX05_P0_P_PIN_TDIODE_C
AM52	VDD_0P80
AM54	GND
AM56	VDD_0P80
AM58	GND
AM60	VCS_0P96
AM62	GND
AM64	VDD_0P80
AM66	GND
AM68	VDD_0P80
AM70	VDN_0P70
AM72	VDDR67_1P20
AM74	GND
AM76	GND
AM78	GND

Pin Number	Signal
AM80	DM_D-DR7_P0_P_PIN_BANK_GRP_0
AM82	GND
AM84	DM_DDR7_P0_P_PIN_ADDR_06
AM86	GND
AM88	DM_DDR7_P0_P_PIN_CLK_0_N
AM90	GND
AM92	DM_DDR7_P0_P_PIN_CLK_1_N
AM94	GND
AN01	DM_D-DR0_P0_P_PIN_BANK_ADR_1
AN03	DM_DDR0_P0_P_PIN_ADDR_10
AN05	DM_DDR0_P0_P_PIN_ADDR_14
AN07	DM_DDR0_P0_P_PIN_CS_B_0
AN09	DM_DDR0_P0_P_PIN_ODT_0
AN11	DM_DDR0_P0_P_PIN_ADDR_13
AN13	DM_DDR1_P0_P_PIN_ADDR_12
AN15	DM_D-DR1_P0_P_PIN_BANK_GRP_0
AN17	DM_DDR1_P0_P_PIN_CKE_2
AN19	DM_DDR1_P0_P_PIN_CKE_3
AN21	GND
AN23	GND
AN25	GND
AN27	GND
AN29	VDD_0P80
AN31	GND
AN33	VDD_0P80
AN35	TS_EX01C0_P0_P_PIN_VSENSE
AN37	VDD_0P80
AN39	GND
AN41	VDD_0P80
AN43	GND
AN45	VDD_0P80
AN47	GND
AN49	VDD_0P80
AN51	GND
AN53	VDN_0P70
AN55	GND
AN57	VDD_0P80
AN59	GND

Pin Number	Signal
AN61	VDD_0P80
AN63	GND
AN65	VDD_0P80
AN67	GND
AN69	VDD_0P80
AN71	GND
AN73	GND
AN75	GND
AN77	DM_DDR7_P0_P_PIN_CKE_1
AN79	DM_DDR7_P0_P_PIN_CKE_0
AN81	DM_DDR7_P0_P_PIN_CKE_2
AN83	DM_D-DR7_P0_P_PIN_BANK_GRP_1
AN85	DM_DDR7_P0_P_PIN_ADDR_09
AN87	DM_DDR7_P0_P_PIN_ADDR_08
AN89	DM_DDR7_P0_P_PIN_ADDR_05
AN91	DM_DDR6_P0_P_PIN_CS_B_2
AN93	DM_DDR6_P0_P_PIN_ADDR_15
AN95	DM_DDR6_P0_P_PIN_CS_B_0
AP02	DM_D-DR0_P0_P_PIN_BANK_ADR_0
AP04	GND
AP06	DM_DDR0_P0_P_PIN_ADDR_00
AP08	GND
AP10	DM_DDR0_P0_P_PIN_ADDR_15
AP12	GND
AP14	DM_DDR0_P0_P_PIN_ODT_1
AP16	GND
AP18	DM_DDR0_P0_P_PIN_CHIPID_0
AP20	GND
AP22	GND
AP24	GND
AP26	VDN_0P70
AP28	GND
AP30	VDD_0P80
AP32	GND
AP34	TS_EX01C0_P0_P_PIN_GSENSE
AP36	GND
AP38	VCS_0P96
AP40	GND

Pin Number	Signal
AP42	VCS_0P96
AP44	GND
AP46	VDD_0P80
AP48	GND
AP50	VDD_0P80
AP52	GND
AP54	VDN_0P70
AP56	GND
AP58	VDD_0P80
AP60	GND
AP62	VDD_0P80
AP64	GND
AP66	VDD_0P80
AP68	GND
AP70	VDN_0P70
AP72	GND
AP74	GND
AP76	VDDR67_1P20
AP78	DM_DDR6_P0_P_PIN_ODT_1
AP80	VDDR67_1P20
AP82	DM_DDR6_P0_P_PIN_ODT_0
AP84	VDDR67_1P20
AP86	DM_DDR6_P0_P_PIN_ADDR_00
AP88	VDDR67_1P20
AP90	DM_DDR6_P0_P_PIN_ADDR_10
AP92	VDDR67_1P20
AP94	DM_D-DR6_P0_P_PIN_BANK_ADR_1
AR01	DM_DDR0_P0_P_PIN_CLK_0_N
AR03	DM_DDR0_P0_P_PIN_CLK_0_P
AR05	DM_DDR0_P0_P_PIN_PAR
AR07	DM_DDR0_PIN_P_P0_EVENT_B
AR09	DM_DDR0_P0_P_PIN_CLK_1_P
AR11	DM_DDR0_P0_P_PIN_ODT_2
AR13	DM_DDR0_P0_P_PIN_CS_B_1
AR15	DM_DDR0_P0_P_PIN_ODT_3
AR17	DM_DDR0_P0_P_PIN_CHIPID_2
AR19	DM_DDR0_P0_P_PIN_CHIPID_1
AR21	GND
AR23	VDDR01_1P20

Pin Number	Signal
AR25	VDDR01_1P20
AR27	GND
AR29	GND
AR31	VDD_0P80
AR33	GND
AR35	VDD_0P80
AR37	GND
AR39	VDD_0P80
AR41	GND
AR43	VDD_0P80
AR45	GND
AR47	VDD_0P80
AR49	GND
AR51	VDD_0P80
AR53	GND
AR55	VDD_0P80
AR57	GND
AR59	VCS_0P96
AR61	GND
AR63	VDD_0P80
AR65	GND
AR67	VDD_0P80
AR69	GND
AR71	VDDR67_1P20
AR73	GND
AR75	DM_DDR6_P0_P_PIN_CHIPID_0
AR77	DM_DDR6_P0_P_PIN_ODT_3
AR79	DM_DDR6_P0_P_PIN_CS_B_1
AR81	DM_DDR6_P0_P_PIN_ADDR_13
AR83	DM_DDR6_P0_P_PIN_ODT_2
AR85	DM_D-DR6_P0_P_PIN_BANK_ADR_0
AR87	DM_DDR6_P0_P_PIN_CLK_1_P
AR89	DM_DDR6_P0_P_PIN_CLK_0_P
AR91	DM_DDR6_P0_P_PIN_CLK_0_N
AR93	DM_DDR6_P0_P_PIN_ADDR_05
AR95	DM_DDR6_P0_P_PIN_ADDR_08
AT02	VDDR01_1P20
AT04	DM_DDR0_P0_P_PIN_ADDR_02
AT06	VDDR01_1P20
AT08	DM_DDR0_P0_P_PIN_CLK_1_N
AT10	VDDR01_1P20
AT12	DM_DDR0_P0_P_PIN_CS_B_3
AT14	VDDR01_1P20
AT16	DM_DDR0_P0_P_PIN_ADDR_17
AT18	VDDR01_1P20
AT20	VDDR01_1P20
AT22	GND
AT24	TS_VDDR0_P0_P_PIN_GSENSE
AT26	VDN_0P70
AT28	VDD_0P80
AT30	GND
AT32	VDD_0P80
AT34	GND
AT36	VCS_0P96
AT38	TS_CACHE0001_P0_P_PIN_VD-D_VSENSE
AT40	VDN_0P70
AT42	GND
AT44	VCS_0P96
AT46	GND
AT48	VDD_0P80
AT50	GND
AT52	VDD_0P80
AT54	GND
AT56	VDD_0P80
AT58	GND
AT60	VCS_0P96
AT62	GND
AT64	VDD_0P80
AT66	GND
AT68	VDD_0P80
AT70	VDN_0P70
AT72	TS_VDDR6_P0_P_PIN_GSENSE
AT74	VDDR67_1P20
AT76	DM_DDR6_P0_P_PIN_CHIPID_1
AT78	GND
AT80	DM_DDR6_P0_P_PIN_ADDR_17
AT82	GND
AT84	DM_DDR6_P0_P_PIN_ADDR_16
AT86	GND
AT88	DM_DDR6_P0_P_PIN_CLK_1_N
AT90	GND
AT92	DM_DDR6_P0_P_PIN_ADDR_03
AT94	GND
AU01	DM_DDR0_P0_P_PIN_ADDR_08
AU03	DM_DDR0_P0_P_PIN_ADDR_07
AU05	DM_DDR0_P0_P_PIN_ADDR_04
AU07	DM_DDR0_P0_P_PIN_ADDR_03
AU09	DM_DDR0_P0_P_PIN_ADDR_01
AU11	DM_DDR0_P0_P_PIN_ADDR_16
AU13	DM_DDR0_P0_P_PIN_CS_B_2
AU15	DM_DDR0_P0_P_PIN_ADDR_05
AU17	DM_DDR0_P0_P_PIN_ADDR_06
AU19	DM_DDR0_P0_P_PIN_CKE_1
AU21	GND
AU23	TS_VDDR0_P0_P_PIN_VSENSE
AU25	GND
AU27	GND
AU29	VDD_0P80
AU31	TS_EX00C1_P0_P_PIN_GSENSE
AU33	VDD_0P80
AU35	TS_EQ0_P0_P_PIN_VDDIN_VSENSE
AU37	TS_EQ0_P0_P_PIN_GSENSE
AU39	GND
AU41	VCS_0P96
AU43	VDD_0P80
AU45	VDD_0P80
AU47	GND
AU49	VDD_0P80
AU51	GND
AU53	VDD_0P80
AU55	GND
AU57	VDD_0P80
AU59	GND
AU61	VDD_0P80
AU63	GND
AU65	VDD_0P80
AU67	GND

Pin Number	Signal
AU69	GND
AU71	GND
AU73	TS_VDDR6_P0_P_PIN_VSENSE
AU75	GND
AU77	DM_DDR6_P0_P_PIN_ADDR_14
AU79	DM_DDR6_P0_P_PIN_CS_B_3
AU81	DM_DDR6_P0_P_PIN_CHIPID_2
AU83	DM_DDR6_P0_P_PIN_PAR
AU85	DM_DDR6_P0_P_PIN_ADDR_02
AU87	DM_DDR6_P0_P_PIN_ADDR_04
AU89	DM_DDR6_P0_P_PIN_ADDR_06
AU91	DM_DDR6_P0_P_PIN_ADDR_11
AU93	DM_D-DR6_P0_P_PIN_BANK_GRP_1
AU95	DM_D-DR6_P0_P_PIN_BANK_GRP_0
AV02	DM_DDR0_P0_P_PIN_ADDR_11
AV04	GND
AV06	DM_DDR0_P0_P_PIN_ADDR_09
AV08	GND
AV10	DM_DDR0_P0_P_PIN_ADDR_12
AV12	GND
AV14	VDDR01_1P20
AV16	GND
AV18	DM_DDR0_P0_P_PIN_RESET_B
AV20	GND
AV22	DM_DDR1_BI_DQ_04
AV24	VDDR01_1P20
AV26	VDN_0P70
AV28	GND
AV30	TS_EX00C1_P0_P_PIN_VSENSE
AV32	GND
AV34	VDD_0P80
AV36	VDD_0P80
AV38	VDD_0P80
AV40	GND
AV42	VDD_0P80
AV44	GND
AV46	VDD_0P80
AV48	GND

Pin Number	Signal
AV50	VDD_0P80
AV52	GND
AV54	VDN_0P70
AV56	GND
AV58	VCS_0P96
AV60	GND
AV62	VDD_0P80
AV64	GND
AV66	VDD_0P80
AV68	GND
AV70	VDN_0P70
AV72	VDDR67_1P20
AV74	GND
AV76	GND
AV78	DM_DDR6_PIN_P_P0_EVENT_B
AV80	VDDR67_1P20
AV82	DM_DDR6_P0_P_PIN_ADDR_01
AV84	VDDR67_1P20
AV86	DM_DDR6_P0_P_PIN_ADDR_09
AV88	VDDR67_1P20
AV90	DM_DDR6_P0_P_PIN_ADDR_12
AV92	VDDR67_1P20
AV94	DM_DDR6_P0_P_PIN_CKE_3
AW01	DM_D-DR0_P0_P_PIN_BANK_GRP_1
AW03	DM_DDR0_P0_P_PIN_CKE_2
AW05	DM_DDR0_PIN_P_P0_ERR_B
AW07	DM_D-DR0_P0_P_PIN_BANK_GRP_0
AW09	DM_DDR0_P0_P_PIN_ACT_B
AW11	DM_DDR0_P0_P_PIN_CKE_0
AW13	GND
AW15	GND
AW17	GND
AW19	GND
AW21	DM_DDR1_BI_DQ_01
AW23	GND
AW25	GND
AW27	GND
AW29	VDD_0P80

Pin Number	Signal
AW31	VDD_0P80
AW33	GND
AW35	VDD_0P80
AW37	GND
AW39	VDD_0P80
AW41	GND
AW43	VDD_0P80
AW45	GND
AW47	VDD_0P80
AW49	GND
AW51	VDD_0P80
AW53	GND
AW55	VDN_0P70
AW57	GND
AW59	VDD_0P80
AW61	GND
AW63	VDD_0P80
AW65	GND
AW67	VDD_0P80
AW69	GND
AW71	GND
AW73	GND
AW75	DM_DDR7_BI_DQ_05
AW77	VDDR67_1P20
AW79	DM_DDR6_P0_P_PIN_CKE_0
AW81	DM_DDR6_P0_P_PIN_ADDR_07
AW83	DM_DDR6_PIN_P_P0_ERR_B
AW85	DM_DDR6_P0_P_PIN_ACT_B
AW87	GND
AW89	GND
AW91	DM_DDR6_P0_P_PIN_CKE_2
AW93	GND
AW95	GND
AY02	VDDR01_1P20
AY04	DM_DDR0_P0_P_PIN_CKE_3
AY06	VDDR01_1P20
AY08	GND
AY10	VDDR01_1P20
AY12	VDDR01_1P20

Pin Number	Signal
AY14	DM_DDR0_BI_DQ_69
AY16	DM_DDR0_BI_DQ_68
AY18	VDDR01_1P20
AY20	DM_DDR1_BI_DQ_07
AY22	DM_DDR1_BI_DQ_05
AY24	GND
AY26	VDN_0P70
AY28	VDD_0P80
AY30	GND
AY32	VDD_0P80
AY34	GND
AY36	VCS_0P96
AY38	GND
AY40	VDD_0P80
AY42	GND
AY44	VCS_0P96
AY46	GND
AY48	VDD_0P80
AY50	GND
AY52	VDD_0P80
AY54	GND
AY56	VDD_0P80
AY58	GND
AY60	VCS_0P96
AY62	GND
AY64	VDD_0P80
AY66	GND
AY68	VDD_0P80
AY70	VDN_0P70
AY72	GND
AY74	DM_DDR7_BI_DQ_04
AY76	DM_DDR7_BI_DQ_01
AY78	GND
AY80	DM_DDR6_P0_P_PIN_CKE_1
AY82	GND
AY84	DM_DDR6_P0_P_PIN_RESET_B
AY86	GND
AY88	GND
AY90	GND

Pin Number	Signal
AY92	VDDR67_1P20
AY94	GND
BA01	GND
BA03	GND
BA05	GND
BA07	GND
BA09	GND
BA11	GND
BA13	DM_DDR0_BI_DQ_70
BA15	DM_DDR0_BI_DQ_64
BA17	GND
BA19	DM_DDR1_BI_DQS_09_N
BA21	DM_DDR1_BI_DQ_00
BA23	VDDR01_1P20
BA25	VDDR01_1P20
BA27	GND
BA29	VDD_0P80
BA31	VDD_0P80
BA33	TS_EX00C0_P0_P_PIN_GSENSE
BA35	TS_EX00C0_P0_P_PIN_VSENSE
BA37	VDD_0P80
BA39	GND
BA41	VDD_0P80
BA43	GND
BA45	VDD_0P80
BA47	GND
BA49	VDD_0P80
BA51	GND
BA53	VDD_0P80
BA55	GND
BA57	VDD_0P80
BA59	GND
BA61	VDD_0P80
BA63	GND
BA65	VDD_0P80
BA67	GND
BA69	GND
BA71	VDDR67_1P20
BA73	GND

Pin Number	Signal
BA75	DM_DDR7_BI_DQ_00
BA77	DM_DDR7_BI_DQS_09_N
BA79	VDDR67_1P20
BA81	GND
BA83	GND
BA85	VDDR67_1P20
BA87	DM_DDR6_BI_DQ_64
BA89	DM_DDR6_BI_DQS_08_P
BA91	GND
BA93	DM_DDR6_BI_DQ_70
BA95	DM_DDR6_BI_DQ_71
BB02	DM_DDR1_BI_DQ_67
BB04	VDDR01_1P20
BB06	DM_DDR1_BI_DQ_66
BB08	DM_DDR1_BI_DQ_71
BB10	VDDR01_1P20
BB12	DM_DDR0_BI_DQ_71
BB14	DM_DDR0_BI_DQ_65
BB16	VDDR01_1P20
BB18	DM_DDR1_BI_DQS_00_P
BB20	DM_DDR1_BI_DQS_09_P
BB22	GND
BB24	GND
BB26	VDN_0P70
BB28	GND
BB30	VDN_0P70
BB32	GND
BB34	VDN_0P70
BB36	GND
BB38	VDN_0P70
BB40	GND
BB42	VDN_0P70
BB44	GND
BB46	VDN_0P70
BB48	GND
BB50	VDN_0P70
BB52	GND
BB54	VDN_0P70
BB56	GND

Pin Number	Signal
BB58	VDN_0P70
BB60	GND
BB62	VDN_0P70
BB64	GND
BB66	VDN_0P70
BB68	GND
BB70	DM_DDR6_BI_DQ_26
BB72	DM_DDR6_BI_DQ_27
BB74	VDDR67_1P20
BB76	DM_DDR7_BI_DQS_09_P
BB78	DM_DDR7_BI_DQS_00_P
BB80	GND
BB82	DM_DDR7_BI_DQ_67
BB84	GND
BB86	GND
BB88	DM_DDR6_BI_DQS_08_N
BB90	VDDR67_1P20
BB92	DM_DDR6_BI_DQ_67
BB94	DM_DDR6_BI_DQ_66
BC01	DM_DDR1_BI_DQ_70
BC03	GND
BC05	DM_DDR1_BI_DQS_08_P
BC07	DM_DDR1_BI_DQS_08_N
BC09	GND
BC11	DM_DDR0_BI_DQ_67
BC13	DM_DDR0_BI_DQS_17_P
BC15	GND
BC17	DM_DDR1_BI_DQ_03
BC19	DM_DDR1_BI_DQS_00_N
BC21	GND
BC23	VDDR01_1P20
BC25	VIO_1P00
BC27	NX_X1_P0_P_PIN_CKA_DAT_02_N
BC29	VIO_1P00
BC31	TS_CLK_P0_P_PIN_PROBE1_P
BC33	TS_CLK_P0_P_PIN_PROBE1_N
BC35	VIO_1P00
BC37	GND
BC39	VIO_1P00

Pin Number	Signal
BC41	GND
BC43	GND
BC45	VIO_1P00
BC47	PV_X1TX_P0_P_PIN_TERMREF_P
BC49	PV_X1TX_P0_P_PIN_TERMREF_N
BC51	VIO_1P00
BC53	GND
BC55	TS_X1RXA_P0_P_PIN_ATST
BC57	VIO_1P00
BC59	TS_VIO0_P0_P_PIN_VSENSE
BC61	TS_VIO0_P0_P_PIN_GSENSE
BC63	VIO_1P00
BC65	TS_X1RXA_P0_P_PIN_HFC_P
BC67	TS_X1RXA_P0_P_PIN_HFC_N
BC69	VIO_1P00
BC71	GND
BC73	GND
BC75	GND
BC77	DM_DDR7_BI_DQS_00_N
BC79	DM_DDR7_BI_DQ_07
BC81	VDDR67_1P20
BC83	DM_DDR7_BI_DQ_66
BC85	DM_DDR7_BI_DQ_71
BC87	VDDR67_1P20
BC89	GND
BC91	DM_DDR6_BI_DQS_17_P
BC93	DM_DDR6_BI_DQS_17_N
BC95	GND
BD02	VDDR01_1P20
BD04	DM_DDR1_BI_DQS_17_N
BD06	DM_DDR1_BI_DQS_17_P
BD08	VDDR01_1P20
BD10	DM_DDR0_BI_DQ_66
BD12	DM_DDR0_BI_DQS_17_N
BD14	VDDR01_1P20
BD16	DM_DDR1_BI_DQ_13
BD18	DM_DDR1_BI_DQ_06
BD20	VDDR01_1P20
BD22	GND

Pin Number	Signal
BD24	GND
BD26	GND
BD28	NX_X1_P0_P_PIN_CKA_DAT_02_P
BD30	GND
BD32	NX_X1_P0_P_PIN_CKA_DAT_00_P
BD34	NX_X1_P0_P_PIN_CKA_DAT_00_N
BD36	GND
BD38	NX_X1_P0_P_PIN_CKB_DAT_00_N
BD40	NX_X1_P0_P_PIN_CKB_DAT_00_P
BD42	GND
BD44	GND
BD46	NX_X1_PIN_P_P0_CKA_DAT_00_N
BD48	NX_X1_PIN_P_P0_CKA_DAT_00_P
BD50	GND
BD52	NX_X1_PIN_P_P0_CKB_DAT_16_P
BD54	NX_X1_PIN_P_P0_CKB_DAT_16_N
BD56	GND
BD58	NX_X1_PIN_P_P0_CKB_DAT_00_N
BD60	NX_X1_PIN_P_P0_CKB_DAT_00_P
BD62	GND
BD64	VDDR67_1P20
BD66	DM_DDR6_BI_DQ_04
BD68	DM_DDR6_BI_DQ_05
BD70	GND
BD72	VSB1_3P30
BD74	VSB1_3P30
BD76	VDDR67_1P20
BD78	DM_DDR7_BI_DQ_06
BD80	DM_DDR7_BI_DQ_03
BD82	GND
BD84	DM_DDR7_BI_DQ_70
BD86	DM_DDR7_BI_DQS_08_P
BD88	GND
BD90	DM_DDR6_BI_DQ_68
BD92	DM_DDR6_BI_DQ_65
BD94	VDDR67_1P20
BE01	GND
BE03	DM_DDR1_BI_DQ_65
BE05	DM_DDR1_BI_DQ_64

Pin Number	Signal
BE07	GND
BE09	DM_DDR0_BI_DQS_08_P
BE11	DM_DDR0_BI_DQS_08_N
BE13	GND
BE15	DM_DDR1_BI_DQ_09
BE17	DM_DDR1_BI_DQ_02
BE19	GND
BE21	DM_DDR0_BI_DQ_04
BE23	DM_DDR0_BI_DQ_05
BE25	GND
BE27	NX_X1_P0_P_PIN_CKA_DAT_03_P
BE29	NX_X1_P0_P_PIN_CKA_DAT_03_N
BE31	GND
BE33	NX_X1_P0_P_PIN_CKA_DAT_01_P
BE35	NX_X1_P0_P_PIN_CKA_DAT_01_N
BE37	GND
BE39	NX_X1_P0_P_PIN_CKB_DAT_02_N
BE41	NX_X1_P0_P_PIN_CKB_DAT_02_P
BE43	GND
BE45	GND
BE47	NX_X1_PIN_P_P0_CKA_DAT_01_P
BE49	NX_X1_PIN_P_P0_CKA_DAT_01_N
BE51	GND
BE53	NX_X1_PIN_P_P0_CKB_DAT_15_N
BE55	NX_X1_PIN_P_P0_CKB_DAT_15_P
BE57	GND
BE59	NX_X1_PIN_P_P0_CKB_DAT_01_P
BE61	NX_X1_PIN_P_P0_CKB_DAT_01_N
BE63	GND
BE65	GND
BE67	DM_DDR6_BI_DQ_00
BE69	DM_DDR6_BI_DQS_09_P
BE71	VDDR67_1P20
BE73	DM_DDR6_BI_DQ_30
BE75	DM_DDR6_BI_DQ_31
BE77	GND
BE79	DM_DDR7_BI_DQ_02
BE81	DM_DDR7_BI_DQ_13
BE83	VDDR67_1P20

Pin Number	Signal
BE85	DM_DDR7_BI_DQS_08_N
BE87	DM_DDR7_BI_DQS_17_N
BE89	VDDR67_1P20
BE91	DM_DDR6_BI_DQ_69
BE93	GND
BE95	GND
BF02	DM_DDR1_BI_DQ_69
BF04	DM_DDR1_BI_DQ_68
BF06	VDDR01_1P20
BF08	GND
BF10	GND
BF12	VDDR01_1P20
BF14	DM_DDR1_BI_DQ_15
BF16	DM_DDR1_BI_DQ_12
BF18	VDDR01_1P20
BF20	DM_DDR0_BI_DQ_00
BF22	DM_DDR0_BI_DQ_01
BF24	GND
BF26	GND
BF28	NX_X1_P0_P_PIN_CKA_DAT_04_N
BF30	NX_X1_P0_P_PIN_CKA_DAT_04_P
BF32	GND
BF34	NX_X1_P0_P_PIN_CKA_DAT_05_P
BF36	NX_X1_P0_P_PIN_CKA_DAT_05_N
BF38	GND
BF40	NX_X1_P0_P_PIN_CKB_DAT_01_N
BF42	NX_X1_P0_P_PIN_CKB_DAT_01_P
BF44	GND
BF46	GND
BF48	NX_X1_PIN_P_P0_CKA_DAT_02_P
BF50	NX_X1_PIN_P_P0_CKA_DAT_02_N
BF52	GND
BF54	NX_X1_PIN_P_P0_CKB_DAT_03_P
BF56	NX_X1_PIN_P_P0_CKB_DAT_03_N
BF58	GND
BF60	NX_X1_PIN_P_P0_CKB_DAT_02_P
BF62	NX_X1_PIN_P_P0_CKB_DAT_02_N
BF64	GND
BF66	VDDR67_1P20

Pin Number	Signal
BF68	DM_DDR6_BI_DQ_01
BF70	DM_DDR6_BI_DQS_09_N
BF72	GND
BF74	DM_DDR6_BI_DQS_03_N
BF76	DM_DDR6_BI_DQS_03_P
BF78	VDDR67_1P20
BF80	DM_DDR7_BI_DQ_12
BF82	DM_DDR7_BI_DQ_09
BF84	GND
BF86	DM_DDR7_BI_DQS_17_P
BF88	DM_DDR7_BI_DQ_65
BF90	GND
BF92	VDDR67_1P20
BF94	DM_DDR7_BI_DQ_27
BG01	DM_DDR1_BI_DQ_27
BG03	DM_DDR1_BI_DQ_26
BG05	GND
BG07	DM_DDR1_BI_DQ_31
BG09	DM_DDR1_BI_DQS_12_P
BG11	GND
BG13	DM_DDR1_BI_DQS_10_N
BG15	DM_DDR1_BI_DQ_08
BG17	GND
BG19	DM_DDR0_BI_DQS_09_P
BG21	DM_DDR0_BI_DQS_09_N
BG23	VDDR01_1P20
BG25	GND
BG27	GND
BG29	NX_X1_P0_P_PIN_CKA_DAT_06_N
BG31	NX_X1_P0_P_PIN_CKA_DAT_06_P
BG33	GND
BG35	NX_X1_P0_P_PIN_CKA_DAT_14_P
BG37	NX_X1_P0_P_PIN_CKA_DAT_14_N
BG39	GND
BG41	NX_X1_P0_P_PIN_CKB_DAT_04_N
BG43	NX_X1_P0_P_PIN_CKB_DAT_04_P
BG45	GND
BG47	GND
BG49	NX_X1_PIN_P_P0_CKA_DAT_03_N

Pin Number	Signal
BG51	NX_X1_PIN_P_P0_CKA_DAT_03_P
BG53	GND
BG55	NX_X1_PIN_P_P0_CKB_DAT_12_N
BG57	NX_X1_PIN_P_P0_CKB_DAT_12_P
BG59	GND
BG61	NX_X1_PIN_P_P0_CKB_DAT_04_P
BG63	NX_X1_PIN_P_P0_CKB_DAT_04_N
BG65	GND
BG67	GND
BG69	DM_DDR6_BI_DQS_00_N
BG71	DM_DDR6_BI_DQ_06
BG73	VDDR67_1P20
BG75	DM_DDR6_BI_DQS_12_P
BG77	DM_DDR6_BI_DQS_12_N
BG79	GND
BG81	DM_DDR7_BI_DQ_08
BG83	DM_DDR7_BI_DQS_10_N
BG85	VDDR67_1P20
BG87	DM_DDR7_BI_DQ_64
BG89	DM_DDR7_BI_DQ_69
BG91	GND
BG93	DM_DDR7_BI_DQ_26
BG95	DM_DDR7_BI_DQ_30
BH02	DM_DDR1_BI_DQ_30
BH04	VDDR01_1P20
BH06	DM_DDR1_BI_DQS_03_P
BH08	DM_DDR1_BI_DQS_12_N
BH10	VDDR01_1P20
BH12	DM_DDR1_BI_DQS_01_P
BH14	DM_DDR1_BI_DQS_10_P
BH16	VDDR01_1P20
BH18	DM_DDR0_BI_DQS_00_N
BH20	DM_DDR0_BI_DQS_00_P
BH22	GND
BH24	DM_DDR0_BI_DQ_06
BH26	VDDR01_1P20
BH28	GND
BH30	NX_X1_P0_P_PIN_CKA_DAT_07_N
BH32	NX_X1_P0_P_PIN_CKA_DAT_07_P

Pin Number	Signal
BH34	GND
BH36	NX_X1_P0_P_PIN_CKA_DAT_15_N
BH38	NX_X1_P0_P_PIN_CKA_DAT_15_P
BH40	GND
BH42	NX_X1_P0_P_PIN_CKB_DAT_03_N
BH44	NX_X1_P0_P_PIN_CKB_DAT_03_P
BH46	GND
BH48	GND
BH50	NX_X1_PIN_P_P0_CKA_DAT_04_N
BH52	NX_X1_PIN_P_P0_CKA_DAT_04_P
BH54	GND
BH56	NX_X1_PIN_P_P0_CKB_DAT_13_N
BH58	NX_X1_PIN_P_P0_CKB_DAT_13_P
BH60	GND
BH62	NX_X1_PIN_P_P0_CKB_DAT_05_N
BH64	NX_X1_PIN_P_P0_CKB_DAT_05_P
BH66	GND
BH68	VDDR67_1P20
BH70	DM_DDR6_BI_DQS_00_P
BH72	DM_DDR6_BI_DQ_07
BH74	GND
BH76	DM_DDR6_BI_DQ_24
BH78	DM_DDR6_BI_DQ_25
BH80	VDDR67_1P20
BH82	DM_DDR7_BI_DQS_10_P
BH84	DM_DDR7_BI_DQS_01_P
BH86	GND
BH88	DM_DDR7_BI_DQ_68
BH90	VDDR67_1P20
BH92	DM_DDR7_BI_DQS_03_P
BH94	DM_DDR7_BI_DQS_03_N
BJ01	GND
BJ03	GND
BJ05	DM_DDR1_BI_DQS_03_N
BJ07	GND
BJ09	GND
BJ11	DM_DDR1_BI_DQ_11
BJ13	DM_DDR1_BI_DQS_01_N
BJ15	GND

Pin Number	Signal
BJ17	DM_DDR0_BI_DQ_27
BJ19	DM_DDR0_BI_DQ_03
BJ21	VDDR01_1P20
BJ23	DM_DDR0_BI_DQ_02
BJ25	DM_DDR0_BI_DQ_07
BJ27	GND
BJ29	GND
BJ31	NX_X1_P0_P_PIN_CKA_CLK_N
BJ33	NX_X1_P0_P_PIN_CKA_CLK_P
BJ35	GND
BJ37	NX_X1_P0_P_PIN_CKA_DAT_16_P
BJ39	NX_X1_P0_P_PIN_CKA_DAT_16_N
BJ41	GND
BJ43	NX_X1_P0_P_PIN_CKB_DAT_16_N
BJ45	NX_X1_P0_P_PIN_CKB_DAT_16_P
BJ47	GND
BJ49	GND
BJ51	NX_X1_PIN_P_P0_CKA_DAT_16_P
BJ53	NX_X1_PIN_P_P0_CKA_DAT_16_N
BJ55	GND
BJ57	NX_X1_PIN_P_P0_CKB_DAT_14_P
BJ59	NX_X1_PIN_P_P0_CKB_DAT_14_N
BJ61	GND
BJ63	NX_X1_PIN_P_P0_CKB_DAT_06_N
BJ65	NX_X1_PIN_P_P0_CKB_DAT_06_P
BJ67	GND
BJ69	GND
BJ71	DM_DDR6_BI_DQ_02
BJ73	DM_DDR6_BI_DQ_12
BJ75	VDDR67_1P20
BJ77	DM_DDR6_BI_DQ_28
BJ79	DM_DDR6_BI_DQ_29
BJ81	GND
BJ83	DM_DDR7_BI_DQS_01_N
BJ85	DM_DDR7_BI_DQ_15
BJ87	VDDR67_1P20
BJ89	GND
BJ91	DM_DDR7_BI_DQS_12_N
BJ93	DM_DDR7_BI_DQS_12_P

Pin Number	Signal
BJ95	GND
BK02	VDDR01_1P20
BK04	DM_DDR1_BI_DQ_24
BK06	DM_DDR1_BI_DQS_02_P
BK08	DM_DDR1_BI_DQS_02_N
BK10	GND
BK12	DM_DDR1_BI_DQ_14
BK14	VDDR01_1P20
BK16	DM_DDR0_BI_DQ_26
BK18	DM_DDR0_BI_DQ_31
BK20	GND
BK22	DM_DDR0_BI_DQ_19
BK24	DM_DDR0_BI_DQ_20
BK26	VDDR01_1P20
BK28	VDDR01_1P20
BK30	GND
BK32	NX_X1_P0_P_PIN_CKA_DAT_08_P
BK34	NX_X1_P0_P_PIN_CKA_DAT_08_N
BK36	GND
BK38	NX_X1_P0_P_PIN_CKB_DAT_05_P
BK40	NX_X1_P0_P_PIN_CKB_DAT_05_N
BK42	GND
BK44	NX_X1_P0_P_PIN_CKB_DAT_15_N
BK46	NX_X1_P0_P_PIN_CKB_DAT_15_P
BK48	GND
BK50	GND
BK52	NX_X1_PIN_P_P0_CKA_DAT_15_N
BK54	NX_X1_PIN_P_P0_CKA_DAT_15_P
BK56	GND
BK58	NX_X1_PIN_P_P0_CKA_DAT_13_P
BK60	NX_X1_PIN_P_P0_CKA_DAT_13_N
BK62	GND
BK64	NX_X1_PIN_P_P0_CKB_DAT_07_P
BK66	NX_X1_PIN_P_P0_CKB_DAT_07_N
BK68	GND
BK70	VDDR67_1P20
BK72	DM_DDR6_BI_DQ_03
BK74	DM_DDR6_BI_DQ_13
BK76	GND

Pin Number	Signal
BK78	DM_DDR6_BI_DQ_20
BK80	DM_DDR6_BI_DQ_19
BK82	VDDR67_1P20
BK84	DM_DDR7_BI_DQ_14
BK86	DM_DDR7_BI_DQ_11
BK88	GND
BK90	DM_DDR7_BI_DQ_31
BK92	DM_DDR7_BI_DQ_24
BK94	VDDR67_1P20
BL01	DM_DDR1_BI_DQ_25
BL03	GND
BL05	DM_DDR1_BI_DQ_29
BL07	DM_DDR1_BI_DQ_16
BL09	GND
BL11	DM_DDR1_BI_DQ_10
BL13	GND
BL15	DM_DDR0_BI_DQ_30
BL17	DM_DDR0_BI_DQS_03_P
BL19	VDDR01_1P20
BL21	DM_DDR0_BI_DQ_18
BL23	DM_DDR0_BI_DQ_21
BL25	GND
BL27	DM_DDR0_BI_DQS_10_P
BL29	GND
BL31	GND
BL33	NX_X1_P0_P_PIN_CKA_DAT_09_N
BL35	NX_X1_P0_P_PIN_CKA_DAT_09_P
BL37	GND
BL39	NX_X1_P0_P_PIN_CKB_DAT_06_N
BL41	NX_X1_P0_P_PIN_CKB_DAT_06_P
BL43	GND
BL45	NX_X1_P0_P_PIN_CKB_DAT_14_P
BL47	NX_X1_P0_P_PIN_CKB_DAT_14_N
BL49	GND
BL51	GND
BL53	NX_X1_PIN_P_P0_CKA_DAT_14_N
BL55	NX_X1_PIN_P_P0_CKA_DAT_14_P
BL57	GND
BL59	NX_X1_PIN_P_P0_CKA_DAT_12_P

Pin Number	Signal
BL61	NX_X1_PIN_P_P0_CKA_DAT_12_N
BL63	GND
BL65	NX_X1_PIN_P_P0_CKB_CLK_N
BL67	NX_X1_PIN_P_P0_CKB_CLK_P
BL69	GND
BL71	GND
BL73	DM_DDR6_BI_DQ_08
BL75	DM_DDR6_BI_DQS_10_P
BL77	VDDR67_1P20
BL79	DM_DDR6_BI_DQ_21
BL81	DM_DDR6_BI_DQ_18
BL83	GND
BL85	DM_DDR7_BI_DQ_10
BL87	VDDR67_1P20
BL89	DM_DDR7_BI_DQ_25
BL91	DM_DDR7_BI_DQ_28
BL93	GND
BL95	DM_DDR7_BI_DQ_19
BM02	DM_DDR1_BI_DQ_28
BM04	VDDR01_1P20
BM06	DM_DDR1_BI_DQS_11_N
BM08	DM_DDR1_BI_DQ_21
BM10	GND
BM12	VDDR01_1P20
BM14	DM_DDR0_BI_DQS_12_N
BM16	DM_DDR0_BI_DQS_03_N
BM18	GND
BM20	DM_DDR0_BI_DQ_23
BM22	DM_DDR0_BI_DQ_16
BM24	VDDR01_1P20
BM26	DM_DDR0_BI_DQS_10_N
BM28	DM_DDR0_BI_DQ_13
BM30	VDDR01_1P20
BM32	GND
BM34	NX_X1_P0_P_PIN_CKA_DAT_10_P
BM36	NX_X1_P0_P_PIN_CKA_DAT_10_N
BM38	GND
BM40	NX_X1_P0_P_PIN_CKB_DAT_07_N
BM42	NX_X1_P0_P_PIN_CKB_DAT_07_P

Pin Number	Signal
BM44	GND
BM46	NX_X1_P0_P_PIN_CKB_DAT_10_N
BM48	NX_X1_P0_P_PIN_CKB_DAT_10_P
BM50	GND
BM52	GND
BM54	NX_X1_PIN_P_P0_CKA_CLK_P
BM56	NX_X1_PIN_P_P0_CKA_CLK_N
BM58	GND
BM60	NX_X1_PIN_P_P0_CKA_DAT_11_P
BM62	NX_X1_PIN_P_P0_CKA_DAT_11_N
BM64	GND
BM66	NX_X1_PIN_P_P0_CKB_DAT_08_P
BM68	NX_X1_PIN_P_P0_CKB_DAT_08_N
BM70	GND
BM72	VDDR67_1P20
BM74	DM_DDR6_BI_DQ_09
BM76	DM_DDR6_BI_DQS_10_N
BM78	GND
BM80	DM_DDR6_BI_DQ_16
BM82	DM_DDR6_BI_DQ_22
BM84	VDDR67_1P20
BM86	GND
BM88	DM_DDR7_BI_DQ_29
BM90	DM_DDR7_BI_DQ_23
BM92	VDDR67_1P20
BM94	DM_DDR7_BI_DQ_22
BN01	DM_DDR1_BI_DQ_19
BN03	DM_DDR1_BI_DQ_18
BN05	GND
BN07	DM_DDR1_BI_DQS_11_P
BN09	DM_DDR1_BI_DQ_20
BN11	GND
BN13	DM_DDR0_BI_DQS_12_P
BN15	DM_DDR0_BI_DQ_24
BN17	VDDR01_1P20
BN19	DM_DDR0_BI_DQ_22
BN21	DM_DDR0_BI_DQ_17
BN23	GND
BN25	DM_DDR0_BI_DQ_15

Pin Number	Signal
BN27	DM_DDR0_BI_DQS_01_N
BN29	GND
BN31	GND
BN33	GND
BN35	NX_X1_P0_P_PIN_CKA_DAT_11_N
BN37	NX_X1_P0_P_PIN_CKA_DAT_11_P
BN39	GND
BN41	NX_X1_P0_P_PIN_CKB_CLK_N
BN43	NX_X1_P0_P_PIN_CKB_CLK_P
BN45	GND
BN47	NX_X1_P0_P_PIN_CKB_DAT_11_N
BN49	NX_X1_P0_P_PIN_CKB_DAT_11_P
BN51	GND
BN53	GND
BN55	NX_X1_PIN_P_P0_CKA_DAT_07_N
BN57	NX_X1_PIN_P_P0_CKA_DAT_07_P
BN59	GND
BN61	NX_X1_PIN_P_P0_CKA_DAT_10_N
BN63	NX_X1_PIN_P_P0_CKA_DAT_10_P
BN65	GND
BN67	NX_X1_PIN_P_P0_CKB_DAT_09_N
BN69	NX_X1_PIN_P_P0_CKB_DAT_09_P
BN71	GND
BN73	GND
BN75	DM_DDR6_BI_DQS_01_N
BN77	DM_DDR6_BI_DQ_15
BN79	VDDR67_1P20
BN81	DM_DDR6_BI_DQ_17
BN83	DM_DDR6_BI_DQ_23
BN85	GND
BN87	DM_DDR7_BI_DQ_18
BN89	DM_DDR7_BI_DQS_11_N
BN91	GND
BN93	DM_DDR7_BI_DQS_02_P
BN95	DM_DDR7_BI_DQS_02_N
BP02	DM_DDR1_BI_DQ_22
BP04	DM_DDR1_BI_DQ_23
BP06	GND
BP08	DM_DDR1_BI_DQ_17

Pin Number	Signal
BP10	GND
BP12	DM_DDR0_BI_DQ_25
BP14	DM_DDR0_BI_DQ_29
BP16	GND
BP18	DM_DDR0_BI_DQS_02_N
BP20	DM_DDR0_BI_DQS_11_N
BP22	VDDR01_1P20
BP24	DM_DDR0_BI_DQ_10
BP26	DM_DDR0_BI_DQS_01_P
BP28	VDDR01_1P20
BP30	DM_DDR0_BI_DQ_08
BP32	VDDR01_1P20
BP34	GND
BP36	NX_X1_P0_P_PIN_CKA_DAT_12_P
BP38	NX_X1_P0_P_PIN_CKA_DAT_12_N
BP40	GND
BP42	NX_X1_P0_P_PIN_CKB_DAT_08_P
BP44	NX_X1_P0_P_PIN_CKB_DAT_08_N
BP46	GND
BP48	NX_X1_P0_P_PIN_CKB_DAT_12_P
BP50	NX_X1_P0_P_PIN_CKB_DAT_12_N
BP52	GND
BP54	GND
BP56	NX_X1_PIN_P_P0_CKA_DAT_05_P
BP58	NX_X1_PIN_P_P0_CKA_DAT_05_N
BP60	GND
BP62	NX_X1_PIN_P_P0_CKA_DAT_09_N
BP64	NX_X1_PIN_P_P0_CKA_DAT_09_P
BP66	GND
BP68	NX_X1_PIN_P_P0_CKB_DAT_10_P
BP70	NX_X1_PIN_P_P0_CKB_DAT_10_N
BP72	GND
BP74	VDDR67_1P20
BP76	DM_DDR6_BI_DQS_01_P
BP78	DM_DDR6_BI_DQ_10
BP80	GND
BP82	DM_DDR6_BI_DQS_11_N
BP84	DM_DDR6_BI_DQS_02_N
BP86	VDDR67_1P20

Pin Number	Signal
BP88	DM_DDR7_BI_DQS_11_P
BP90	VDDR67_1P20
BP92	DM_DDR7_BI_DQ_16
BP94	DM_DDR7_BI_DQ_17
BR09	PV_IVRM_V1_M_P0_VREF_N
BR11	PV_IVRM_V1_M_P0_VREF_P
BR13	DM_DDR0_BI_DQ_28
BR15	VDDR01_1P20
BR17	DM_DDR0_BI_DQS_02_P
BR19	DM_DDR0_BI_DQS_11_P
BR21	GND
BR23	DM_DDR0_BI_DQ_11
BR25	DM_DDR0_BI_DQ_14
BR27	GND
BR29	DM_DDR0_BI_DQ_09
BR31	DM_DDR0_BI_DQ_12
BR33	GND
BR35	GND
BR37	NX_X1_P0_P_PIN_CKA_DAT_13_N
BR39	NX_X1_P0_P_PIN_CKA_DAT_13_P
BR41	GND
BR43	NX_X1_P0_P_PIN_CKB_DAT_09_N
BR45	NX_X1_P0_P_PIN_CKB_DAT_09_P
BR47	GND
BR49	NX_X1_P0_P_PIN_CKB_DAT_13_N
BR51	NX_X1_P0_P_PIN_CKB_DAT_13_P
BR53	GND
BR55	GND
BR57	NX_X1_PIN_P_P0_CKA_DAT_06_N
BR59	NX_X1_PIN_P_P0_CKA_DAT_06_P
BR61	GND
BR63	NX_X1_PIN_P_P0_CKA_DAT_08_P
BR65	NX_X1_PIN_P_P0_CKA_DAT_08_N
BR67	GND
BR69	NX_X1_PIN_P_P0_CKB_DAT_11_N
BR71	NX_X1_PIN_P_P0_CKB_DAT_11_P
BR73	GND
BR75	GND
BR77	DM_DDR6_BI_DQ_14

Pin Number	Signal
BR79	DM_DDR6_BI_DQ_11
BR81	VDDR67_1P20
BR83	DM_DDR6_BI_DQS_11_P
BR85	DM_DDR6_BI_DQS_02_P
BR87	GND
BR89	GND
BR91	DM_DDR7_BI_DQ_21
BR93	DM_DDR7_BI_DQ_20
BR95	GND

Glossary

AES	Advanced Encryption Standard
APSS	Analog power subsystem sweep
ASIC	Application-specific integrated circuit
AVS	Adaptive voltage scaling
BEOL	Back-end of the line
BMC	Baseboard management controller
CAPI	Coherent accelerator processor interface
CAPP	Coherent accelerator processor proxy
CDR	Clock and data recovery
CMOS	Complementary metal–oxide–semiconductor
CRB	Customer reference board
CRC	Cyclic redundancy check
CTLE	Continuous time linear equalizer
DAC	Digital-to-analog converter
DDR	Double data rate
DFE	Decision feedback equalizer
DIMM	Dual in-line memory module
DMA	Direct memory attach
DRAM	Dynamic random-access memory
DTS	Digital thermal sensor
ECO	Extended cache option
ECRC	End-to-end CRC
EDI	Elastic differential I/O
EEH	Enhance error handling
EI4	Elastic interface 4
ET	Early time
eVRM	External voltage regulator module
FBC	Fabric controller

FC PLGA	Flip-chip plastic land grid array
FFE	Feed-forward equalizer
FPGA	Field-programmable gate array
FRU	Field replaceable unit
FSI	FRU service interface
GTps	Gigatransfers per second
GPU	Graphics processing unit
HCSL	Host clock signal level
HSS	High-speed serial
I^2C	Inter-integrated circuit
IEEE	Institute of Electrical and Electronics Engineers
IODA	I/O Design Architecture
IP	Intellectual property
ISA	Instruction set architecture
iVRM	Internal voltage regulator module
JEDEC	Formerly the Joint Electron Device Engineering Council
JTAG	Joint Test Action Group
LED	Light-emitting diode
LGA	Land grid array
LPAR	Logical partition
LPC	Low pin count bus or lowest point of coherency
LRDIMM	Load-reduced dual in-line memory module
LSI	Level signalled interrup
LSSD	Level-sensitive scan design
LTE	Long-tail equalizer
MFSI	Master FSI
MPUL	Most-positive up level
MSI	Message signalled interrupt
Mux	Multiplexer

OCC	On-chip controller
PAPR	Power Architecture Platform Reference
PBA	Per buffer addressability mode
PCIe	Peripheral Component Interconnect Express
PDA	Per DRAM addressability mode
PE	Partitionable endpoints
PEC	PCI Express controller
PHB	PCI Host Bridge
PHY	Physical layer
PLL	Phase-locked loop
PMC	Power management control
PMCR	Power Management Control Register
PMICR	Power Management Idle Control Register
PMSR	Power Management Status Register
POL	Point of load
PPE	Programmable PowerPC-lite engine
PPM	Parts per million
PRBS	Pseudo-random binary sequence
PSI	Processor support interface
PVR	Processor Version Register
QR	Quad rank
RC	Root complex
RDC	Regulator design current
RDIMM	Registered dual in-line memory module
RDP	Regulator design power
RX	Receive
SBE	Self-boot engine
SC	Small core
SCM	Single-chip module

SCOM	Scan communications
SEEPROM	Serial electrically erasable programmable read-only memory
SerDes	Serializer/deserializer
SMP	Symmetric multiprocessor
SMT	Simultaneous multithreading
SHA	Secure hash algorithm
SOI	Silicon-on-insulator
SPI	Serial peripheral interconnect
SPR	Special Purpose Register
SRAM	Static random access memory
SST	Source series terminated
SSC	Single small core
TCE	Translation control entry
TDC	Thermal design current
TDP	Thermal design power
TDR	Time domain reflectometer
T_A	Thermal junction temperature
T_J	Thermal junction temperature
TLP	Transaction layer packet
TPM	Trusted platform module
TX	Transmit
UPS	Uninterrupted power system
USC	Unpaired small core
VID	Voltage ID
VPD	Vital product data
VRM	Voltage regulator module