RAPTOR
COMPUTING SYSTEMS

Arctic Tern ModBMC System / PCIe Development Kit

User's Guide
For System Configuration
and Set Up

AT1PEC1 User's Guide Version 1.00
https://www.raptorcs.com

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Safety Information

ELECTRICAL SAFETY

- To reduce the risk of electric shock, disconnect the power cable before relocating or servicing the system.
- When adding or removing devices to or from the system, ensure that the power cables for the devices are unplugged before the signal cables are connected. If possible, disconnect all power cables from the existing system before you add a device.
- Before connecting or removing signal cables from the motherboard, ensure that all power cables are unplugged.
- Seek professional assistance before using an adapter or extension cord. These devices could interrupt the grounding circuit.
- Make sure that your power supply is set to the correct voltage in your area. If you are not sure about the voltage of the electrical outlet you are using, contact your local power company.
- If your power supply is not functioning, do not attempt to repair it. Contact a qualified service technician or your retailer.

OPERATIONAL SAFETY

- Before installing the carrier card or connecting devices to it, carefully read any and all provided manuals for the devices in question.
- Before using the product, make sure all cables are correctly connected and the power cables are not damaged. If you find any damage, contact your dealer immediately.
- To avoid short circuits, keep paper clips, screws, staples, and other foreign metallic objects away from connectors, slots, sockets and circuitry.
- Avoid dust, humidity, and temperature extremes. Do not locate the product in any area where it may become wet or damp.
- Place the product on a stable surface at all times.
- If you encounter technical problems with the product, contact a qualified service technician or your retailer.

Notices

FEDERAL COMMUNICATIONS COMMISSION STATEMENT

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- This device may not cause harmful interference, and
- This device must accept any interference received including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with manufacturer's instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment to an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

ENVIRONMENTAL DISPOSAL STATEMENTS

DO NOT throw the system or its components in municipal waste. This product has been designed to enable proper reuse of parts and recycling. This symbol of the crossed out wheeled bin indicates that the product (electrical and electronic equipment) should not be placed in municipal waste. Check local regulations for disposal of electronic products.

DO NOT throw the mercury-containing button cell battery in municipal waste. This symbol of the crossed out wheeled bin indicates that the battery should not be placed in municipal waste.

Arctic Tern Module Specifications

Primary Logic Element		1x Lattice ECP5 85k LUT FPGA
Form Factor		ModBMC Standard (DDR4 SODIMM dimensions)
Power Requirements		Single 3.3V supply, < 2A
Memory	**Type**	DDR3
	Capacity	1GB
	Organization	2x 512MB 16-bit devices (32-bit parallel capable)
Storage	**Type**	1x SPI Parallel NOR Flash
	Total Capacity	16MB
Networking	**Micrel 9021 PHY**	1 GbE
Graphics	**ITE 66121 HDMI PHY**	HDMI (up to 1920x1200)
PCIe	**Lattice SERDES**	1x PCIe 2.0 (commercial variant) 1x PCIe 1.0 (industrial variant)
High Speed Interconnect	**Lattice SERDES**	2x 5.0G/s full duplex (commercial variant) 2x 2.5G/s full duplex (industrial variant)
Serial	**Host**	1x TTL port
	BMC	1x TTL port
RTC	**Epson RX8900**	Battery backed I2C RTC
Thermal Sensors	**Winbond W83773**	2x I2C Thermal Sensors (single controller)
GPIO	**ECP5 Direct I/O**	3.3V TTL GPIO
	TI GPIO Expander	2x I2C dedicated 3.3V GPIO expanders
Environmental Requirements		Operation: 10°C - 35°C
		Storage: -40°C - 70°C
		Humidity: 20% - 90%, non-condensing

NOTE: Specifications are subject to change without notice.

System Overview

DESIGN

The Arctic Tern module has been specifically designed for applications requiring high security, small form factor, and minimal power requirements. Multiple modules may be connected together for enhanced functionality, using the on-board SERDES links. The AT1PEC1 carrier card allows up to two modules to be installed, although most on-card features will function with only the first module installed.

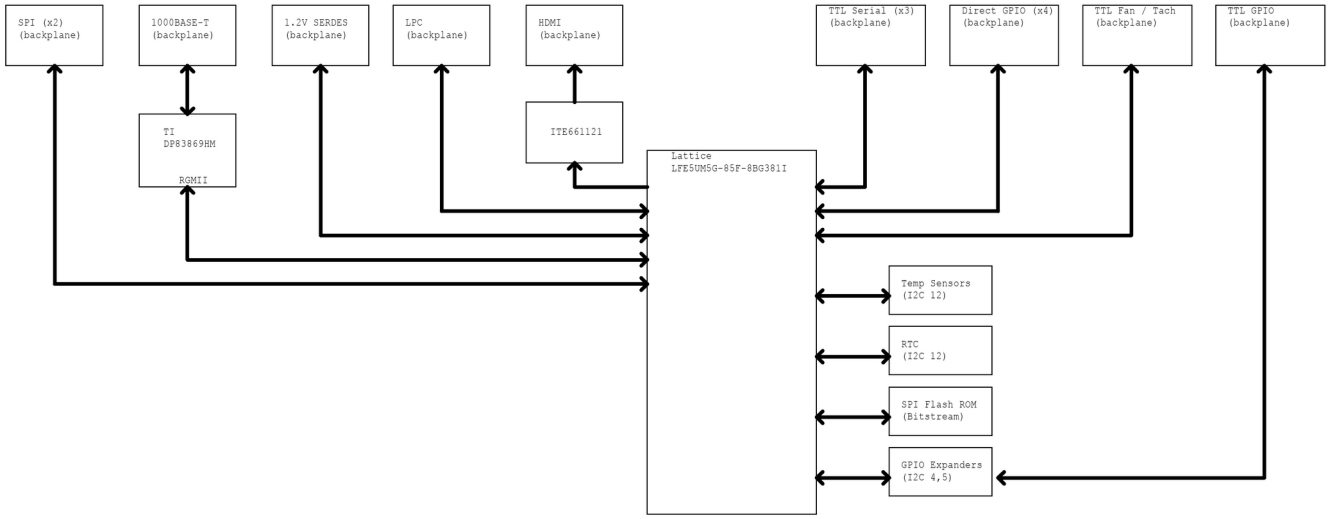


Illustration 1: Arctic Tern Block Diagram

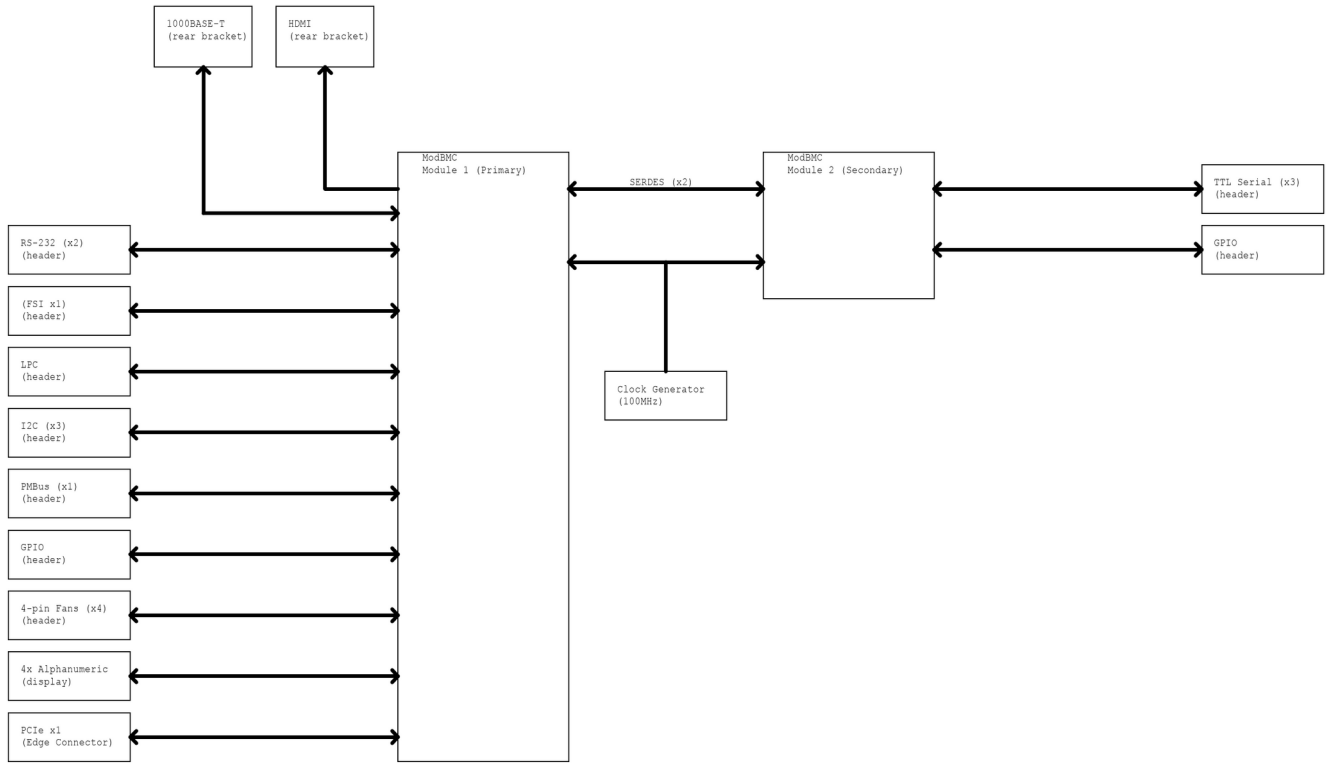


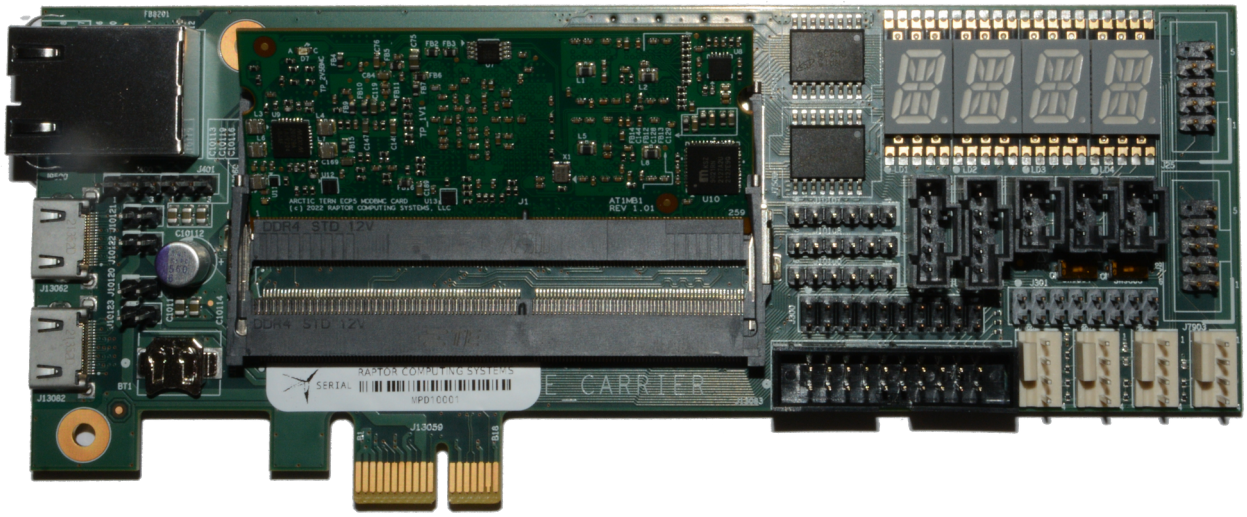
Illustration 2: Arctic Tern Dual Module PCIe Carrier Block Diagram

Module Installation and Removal

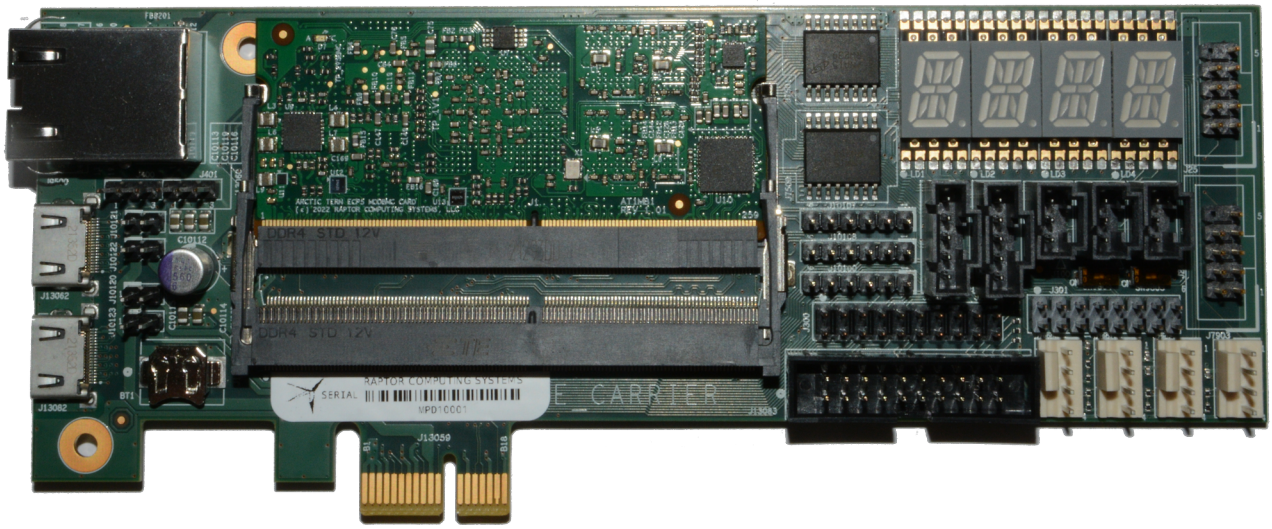
MODULE INSERTION

Modules are inserted at an angle, then rotated downward into the socket latches in the same manner as standard SODIMM memory modules. Module 1 must be installed before Module 2 (if applicable) due to mechanical interference between the two modules during the installation process.

To install, first gently insert the module at an approximate 45 degree angle to the carrier card as shown. The module must be fully inserted to the hard stop, otherwise it will not latch during the second part of the installation process.



Once inserted, carefully but firmly press the module flat toward the carrier card. Use your thumbs and press on the upper two corners of the module during this process. Installation is complete once the latches engage and the module no longer attempts to return to an angled position away from the carrier card.



MODULE REMOVAL

Modules must be removed in the reverse order to installation. Module 2 must be removed before Module 1 due to mechanical interference between the two modules during the removal process.

To remove, gently spread the two black plastic socket latches on either side of the module until the module “pops” up and sits at an angle to the carrier card. Once the module is at an angle to the carrier card, grasp the module by the two short edges and gently but firmly pull the module directly away from the socket until it releases from the carrier card.

CAUTION: Attempting to over-rotate or otherwise mechanically force the module away from the carrier card can result in damage to the socket and/or module. **Damage caused by improper installation or removal is not covered under warranty.**

Headers and Connectors

PIN NUMBERING CONVENTIONS

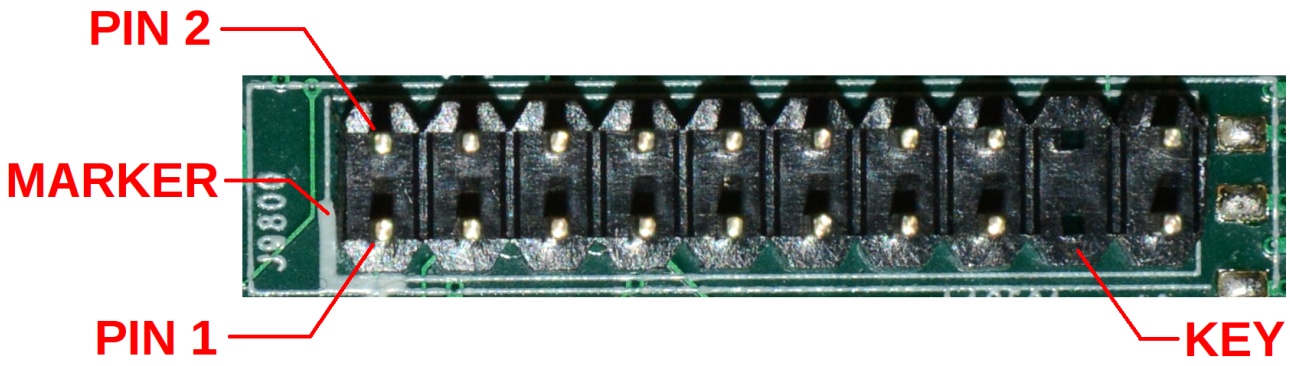
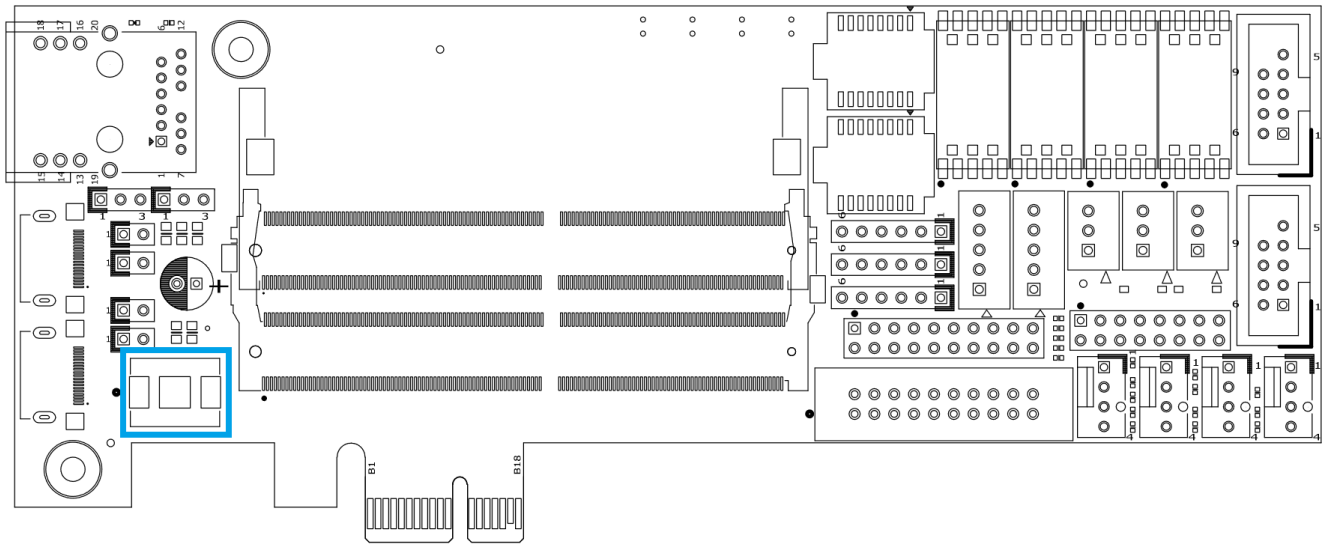


Illustration 3: Dual Row Header with Annotated Pins, Marker, and Key

All headers on the AT1PEC1 follow a standard layout, with pin 1 being denoted with a white silkscreen marking. Dual row headers follow the numbering convention shown above, where all even pins are on one side of the header and all odd pins are on the other. Single row headers use a monotonically increasing pin number, starting from pin 1. Key pins are not physically present, but are still counted as pins in the numbering scheme.

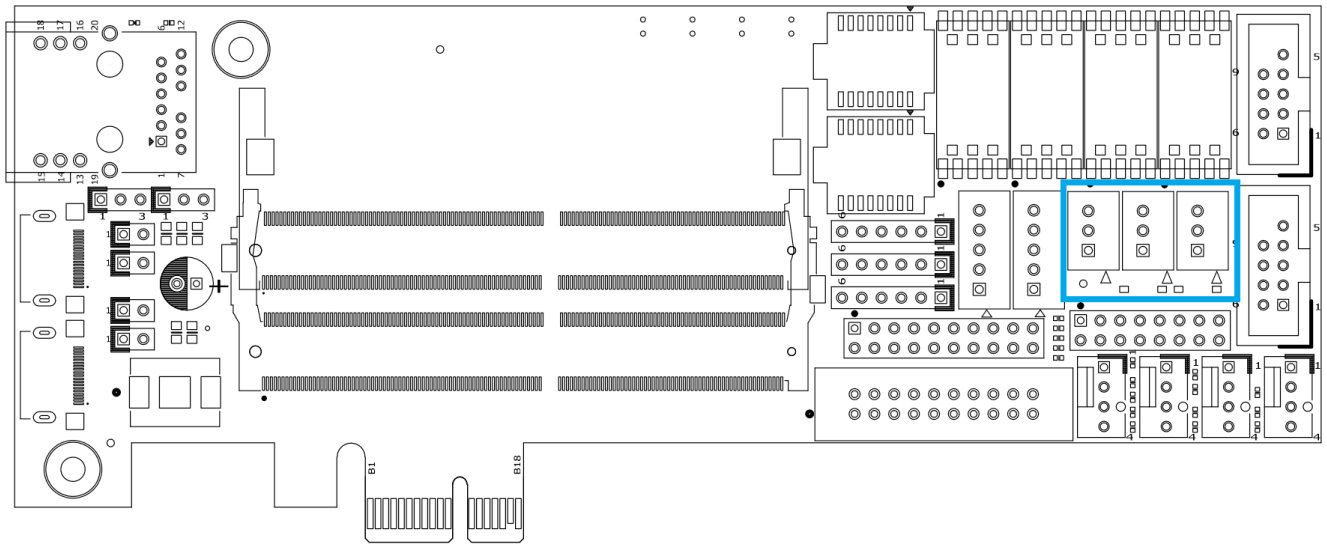
RTC BACKUP BATTERY SOCKET



376 / 377 Coin Cell Battery (+ up)

BT`1			
Pin	**Function**	**Pin**	**Function**
1	+ Power	2	+ Power
3	Ground		

BMC I2C PORTS

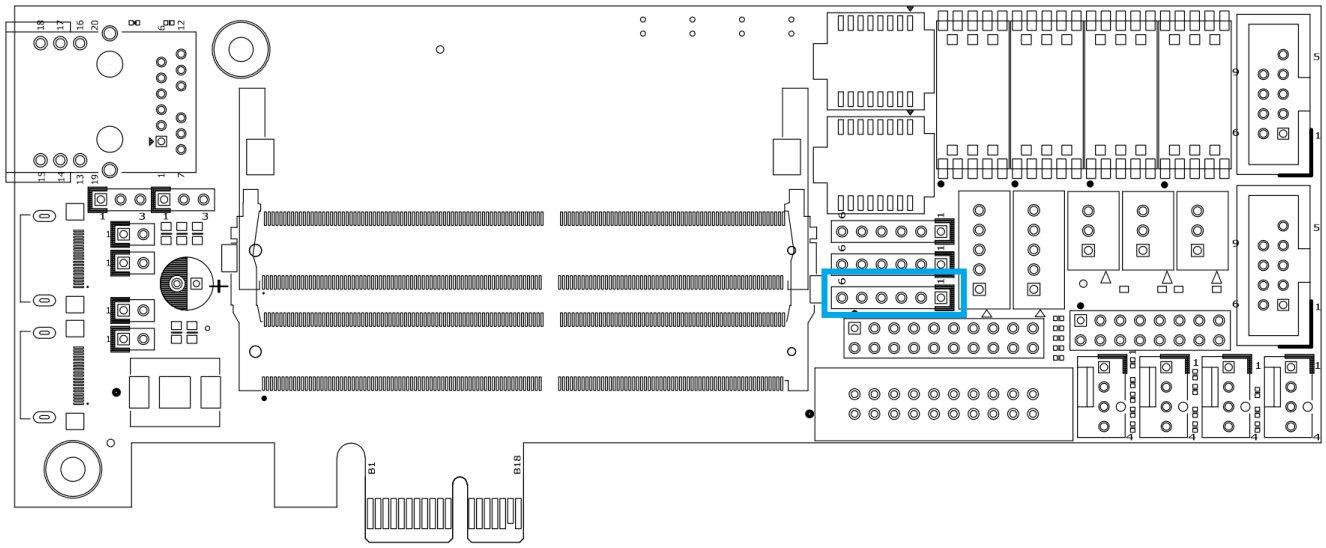


J100 (Left)		
Pin	**FPGA Pin**	**Function**
1	D5	I2C_BMC_SCL
2	-	Ground
3	E4	I2C_BMC_SDA

J101 (Middle)		
Pin	**FPGA Pin**	**Function**
1	B2	I2C_BMC_SCL
2	-	Ground
3	B1	I2C_BMC_SDA

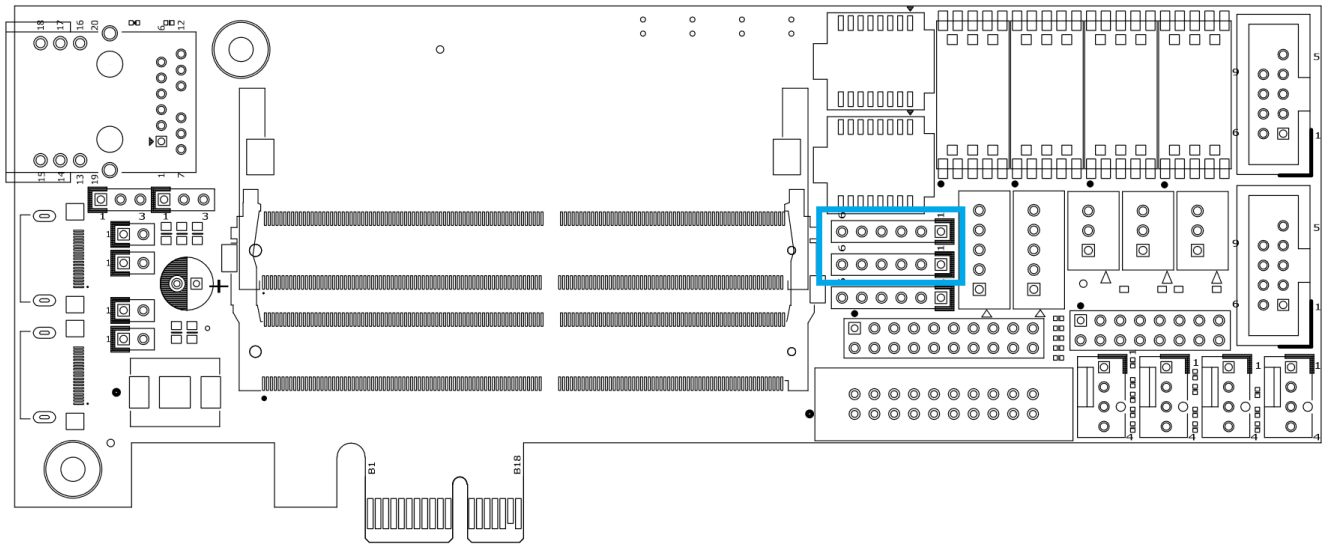
J102 (Right)		
Pin	**FPGA Pin**	**Function**
1	E8	I2C_BMC_SCL
2	-	Ground
3	C7	I2C_BMC_SDA

PCIE JTAG HEADER



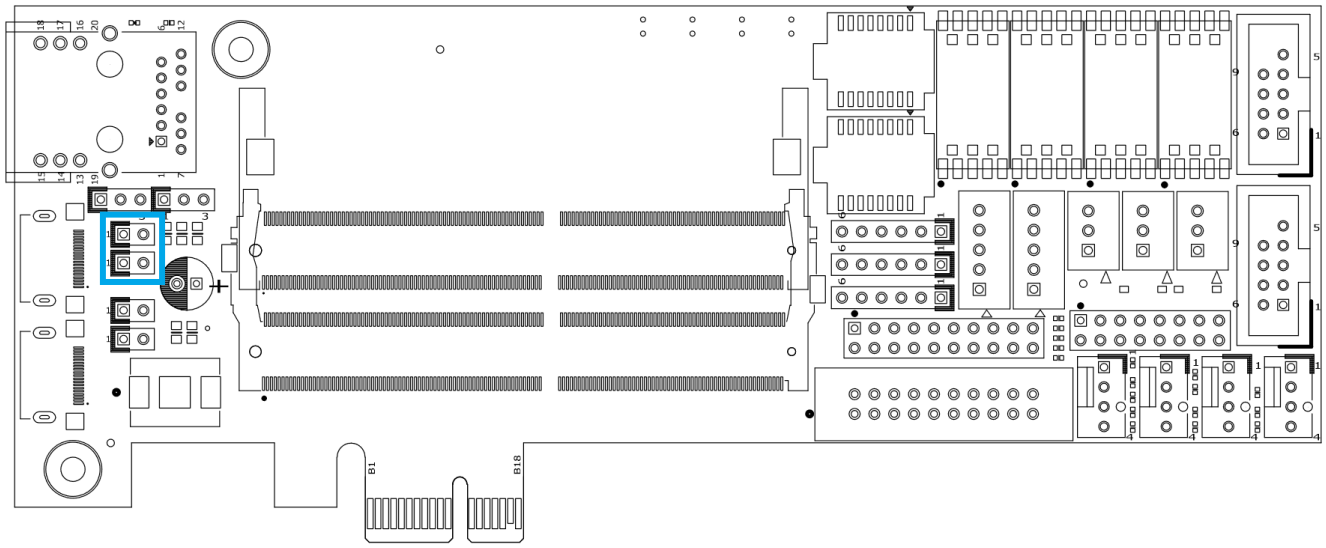
J10100					
Pin	FPGA Pin	Function	Pin	FPGA Pin	Function
1	T5	JTAG_TCK	2	V4	JTAG_TDO
3	R5	JTAG_TDI	4	U5	JTAG_TMS
5	V3	JTAG_TRST_N	6	-	Ground

JTAG PROGRAMMING HEADERS



J10107 / J10108 (Top / Bottom) (Module 1 / Module 2)					
Pin	FPGA Pins	Function	Pin	FPGA Pins	Function
1	U5	JTAG_TMS	2	R5	JTAG_TDI
3	V4	JTAG_TDO	4	T5	JTAG_TCK
5	-	Ground	6	-	+3.3V Aux Power

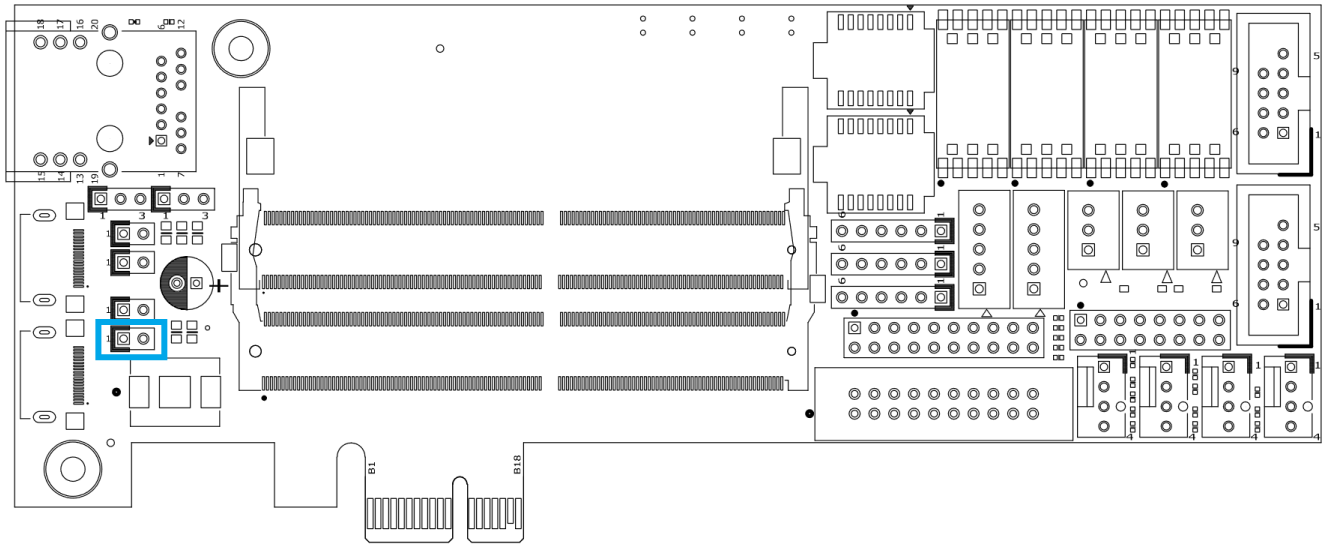
POWER JUMPERS (3.3V AUX)



J10121 / J10122			
Pin	**Function**	**Pin**	**Function**
1	PCIe connector power pins	2	+3.3V Aux power

Place jumper caps across pins 1 and 2 on J10121 and J10122 to connect 3.3V Aux power to PCIe.

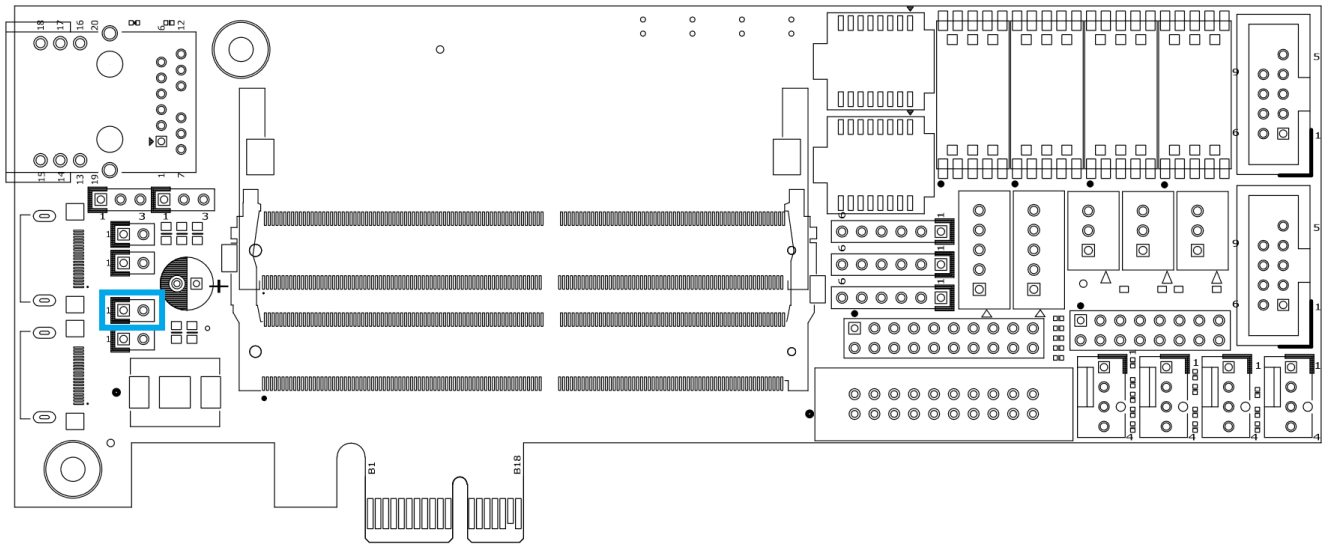
POWER JUMPERS (12V)



J10123			
Pin	**Function**	**Pin**	**Function**
1	+12V power	2	PCIe power pins

Place jumper cap across pins 1 and 2 to connect 12V Aux power to PCIe.

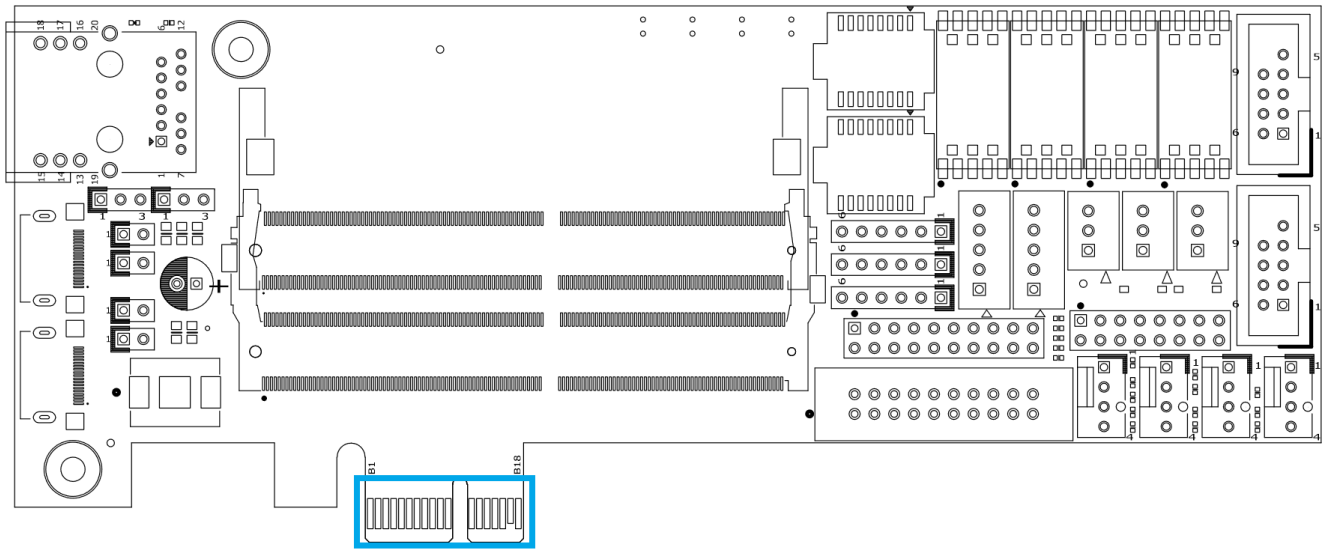
POWER JUMPERS (3.3V HOST)



J10120			
Pin	**Function**	**Pin**	**Function**
1	+3.3V host power	2	PCIe connector power pins

Place jumper cap across pins 1 and 2 to connect 3.3V Host power to PCIe.

PCI EXPRESS

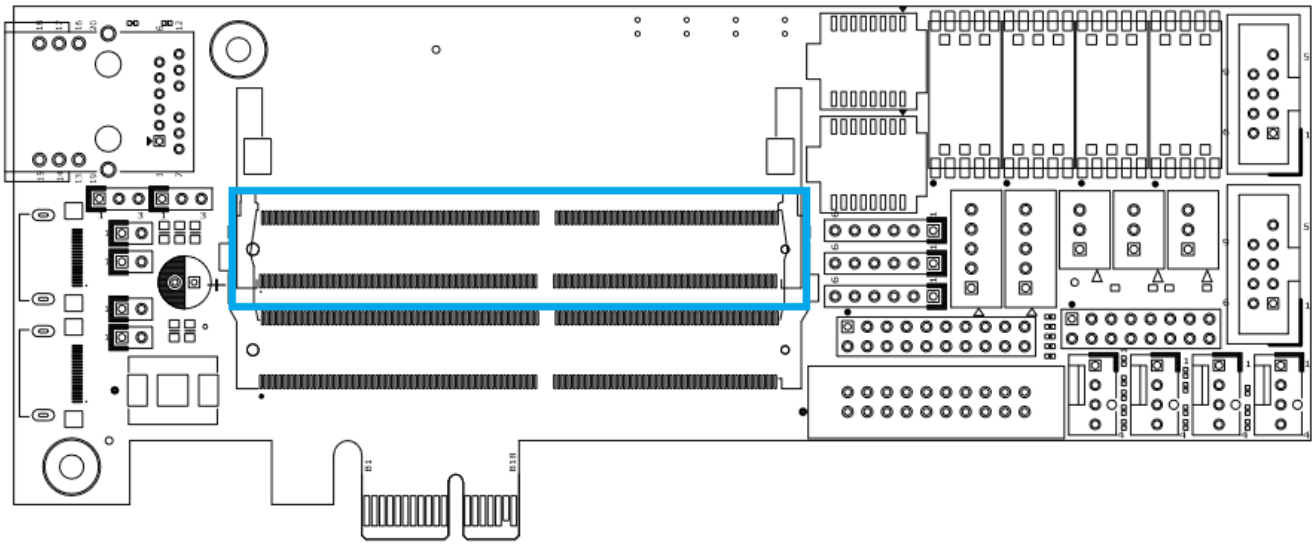


J13059					
Pin	**FPGA Pins**	**Function**	**Pin**	**FPGA Pins**	**Function**
A1	-	PRSNT1_N (Connected to PRSNT2_N)	B5	-	SMCLK
A5	T5	JTAG_TCK	B6	-	SMDAT
A6	R5	JTAG_TDI	B9	V3	JTAG_TRST_N
A7	V4	JTAG_TDO	B11	EXP1/GPIO1	WAKE_N
A8	U5	JTAG_TMS	B12	-	RSVD1 (No connect)
A11	A6	PERST_N	B14	Y5	PET_0_P
A13	Y11	REFCLK_P	B15	Y6	PET_0_N
A14	Y12	REFCLK_N	B17	-	PRSNT2_N (Connected to PRSNT1_N)
A16	W4	PER_0_P			
A17	W5	PER_0_N			
Power					
A2	12V Power		B1	12V Power	
A3	12V Power		B2	12V Power	
A9	3.3V Power		B3	12V Power	
A10	3.3V Power		B8	3.3V Power	

		B10	3.3 Aux Power
Ground			
A4	Ground	B4	Ground
A12	Ground	B7	Ground
A15	Ground	B13	Ground
A18	Ground	B16	Ground
		B18	Ground

Note: EXP0 and EXP1 are used to refer to the GPIO expanders onboard each Arctic Tern module, where EXP0 is attached to I2C bus 4 and EXP1 is attached to I2C bus 5.

MODBMC SOCKET 1



J13060 (Bottom)					
Pin	FPGA Pin	Function	Pin	FPGA Pin	Function
1	-	VDD_12V_STBY	2	-	VDD_RGMII_REF
3	-	VDD3_3V_STBY	4	-	VDD3_3V_STBY
5	-	VDD3_3V_STBY	6	-	VDD3_3V_STBY
7	-	VDD3_3V_RTC_BATT	8	-	Ground
9	-	Ground	10	-	DACG (No connect)
11	-	Ground	12	-	DACB (No connect)
13	A18	GPIO0	14	-	DACR
15	B18	GPIO1	16	-	HSYNC
17	T2	GPIO3	18	-	VSYNC
19	T3	GPIO5	20	-	DDC_CLK
21	C1	CONSOLE_RX	22	-	DDC_DAT
23	C2	CONSOLE_TX	24	-	Ground
25	EXP0/GPOI0	GPIO7	26	B5	PWM0
27	E1	PWM2	28	C5	PWM1
29	-	PWM4 (No connect)	30	H3	PWM3
31	-	PWM6 (No connect)	32	-	PWM5 (No connect)
33	-	Ground	34	-	PWM7 (No connect)
35	EXP0/GPOI1	GPIO15	36	EXP0/GPOI3	GPIO19

37	EXP0/GPOI2	GPIO17	38	EXP0/GPOI4	GPIO20
39	-	Ground	40	EXP0/GPOI5	GPIO21
41	B8	UART1_RX	42	C8	UART2_RX
43	A7	UART1_TX	44	D8	UART2_TX
45	-	Ground	46	EXP0/GPOI6	GPIO25
47	-	I2C8_SCL (No connect)	48	-	I2C13_SCL (No connect)
49	-	I2C8_SDA (No connect)	50	-	I2C13_SDA (No connect)
51	-	Ground	52	-	Ground
53	-	I2C7_SCL (No connect)	54	-	I2C6_SCL (No connect)
55	-	I2C7_SDA (No connect)	56	-	I2C6_SDA (No connect)
57	-	Ground	58	-	Ground
59	EXP0/GPOI7	GPIO35	60	EXP1/SCL	I2C5_SCL
61	EXP0/GPOI8	GPIO37	62	EXP1/SDA	I2C5_SDA
63	E2	FW_SPI_CS0#	64	-	Ground
65	F2	FW_SPI_IO0	66	-	HDMI_TX0_N
67	F3	FW_SPI_IO1	68	-	HDMI_TX0_P
69	D1	FW_SPI_IO2	70	-	HDMI_TX1_N
71	A2	FW_SPI_IO3	72	-	HDMI_TX1_P
73	G3	FW_SPI_CLK	74	EXP0/GPOI9	GPIO44
75	-	FW_SPI_CS1# (No connect)	76	EXP0/GPOI10	GPIO45
77	-	PWRGOOD (No connect)	78	D7	TACH0
79	-	HDMI_TX2_N	80	C6	TACH1
81	-	HDMI_TX2_P	82	E7	TACH2
83	EXP0/GPOI11	GPIO51	84	D6	TACH3
85	-	HDMI_CLK_N	86	A4	TACH4
87	-	HDMI_CLK_P	88	-	TACH5 (No connect)
89	EXP0/GPOI12	GPIO57	90	-	TACH6 (No connect)
91	EXP0/GPOI13	GPIO59	92	-	TACH7 (No connect)
93	EXP0/GPOI14	GPIO61	94	-	TACH8 (No connect)
95	EXP0/GPOI15	GPIO63	96	-	TACH9 (No connect)
97	-	CPU_RST# (No connect)	98	-	TACH10 (No connect)
99	EXP0/GPOI16	GPIO67	100	-	TACH11 (No connect)
101	EXP0/GPOI17	GPIO69	102	-	TACH12 (No connect)
103	EXP1/GPOI0	GPIO71	104	-	TACH13 (No connect)
105	EXP1/GPOI1	GPIO73	106	-	TACH14 (No connect)

107	EXP1/GPOI2	GPIO75	108	-	TACH15 (No connect)
109	EXP1/GPOI3	GPIO76	110	-	Ground
113	EXP1/GPOI4	GPIO77	114	-	Ground
115	EXP1/GPOI5	GPIO79	116	-	SPI3_CLK (No connect)
117	EXP1/GPOI6	GPIO81	118	-	SPI3_MISO (No connect)
119	EXP1/GPOI7	GPIO83	120	-	SPI3_MOSI (No connect)
121	EXP1/GPOI8	GPIO85	122	-	SPI3_CS0# (No connect)
123	B2	I2C2_SCL	124	-	SPI3_CS1# (No connect)
125	B1	I2C2_SDA	126	-	Ground
127	-	Ground	128	D5	I2C1_SCL
129	-	I2C14_SCL (No connect)	130	E4	I2C1_SDA
131	-	I2C14_SDA (No connect)	132	-	Ground
133	-	Ground	134	EXP0/SCL	I2C4_SCL
135	-	I2C16_SCL (No connect)	136	EXP0/SDA	I2C4_SDA
137	-	I2C16_SDA (No connect)	138	EXP1/GPOI9	GPIO98
139	-	Ground	140	EXP1/GPOI10	GPIO99
141	T1	I2C12_SCL	142	A6	PCIE_RST#
143	V1	I2C12_SDA	144	-	UART3_RX
145	-	Ground	146	-	UART3_TX
147	W5	PCIE_RX_N	148	-	UART4_RX
149	W4	PCIE_RX_P	150	-	UART4_TX
151	-	Ground	152	-	VDD_LPC3V3
153	Y6	PCIE_TX_N	154	EXP1/GPOI11	GPIO106
155	Y5	PCIE_TX_P	156	EXP1/GPOI12	GPIO107
157	-	Ground	158	-	GPIO108 (No connect)
159	Y12	PCIE_CLK_N	160	-	GPIO109 (No connect)
161	Y11	PCIE_CLK_P	162	V3	JTAG_RST
163	-	Ground	164	V4	JTAG_TDO
165	C3	LPC_RST#	166	R5	JTAG_TDI
167	A3	LPC_LAD1	168	T5	JTAG_RTCK
169	C4	LPC_LAD0	170	T5	JTAG_TCK
171	F4	LPC_IRQ#	172	U5	JTAG_TMS
173	D3	LPC_FRAME#	175	B3	LPC_LAD3
177	B4	LPC_LAD2	179	H5	LPC_CLK
181	U2	I2C9_SCL	183	R3	I2C9_SDA
185	-	Ground	187	-	I2C10_SCL (No connect)

189	-	I2C10_SDA (No connect)	190	-	SPI2_CS# (No connect)
191	-	Ground	192	-	SPI2_MISO (No connect)
193	-	I2C15_SCL (No connect)	194	-	SPI2_MOSI (No connect)
195	-	I2C15_SDA (No connect)	196	-	SPI2_CLK (No connect)
197	-	Ground	198	G5	AUX_SPI_CS0#
199	-	I2C11_SCL (No connect)			

COLOR CODES

GPIO

PWM / TACH

Serial (UART)

SPI

HDMI / HSYNC / VSYNC / DDC

I2C

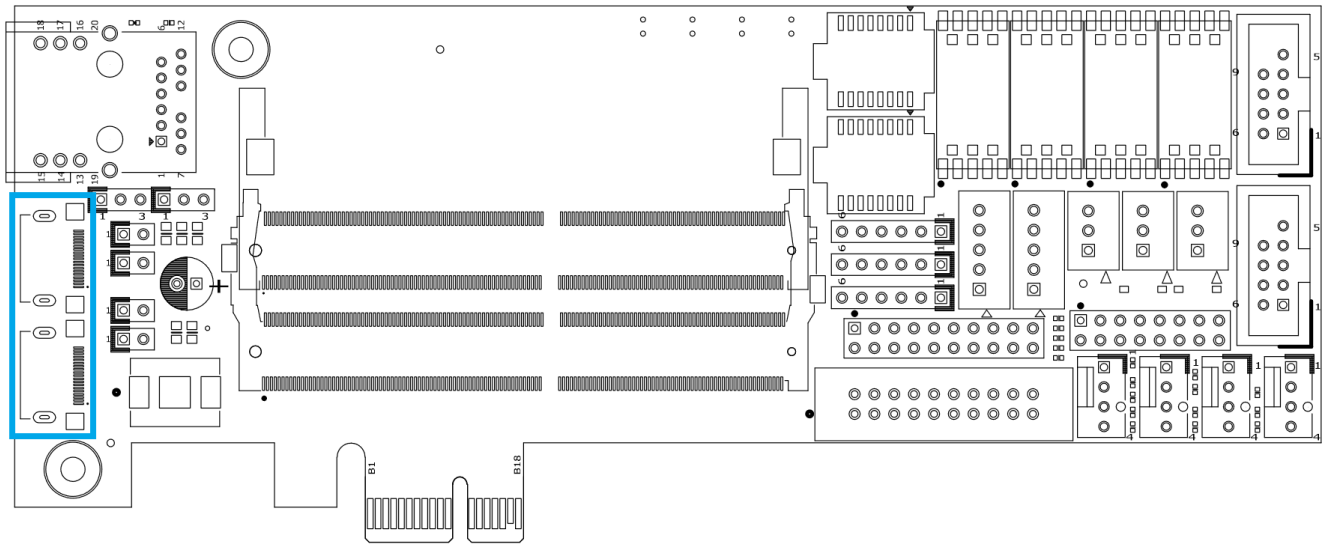
DAC

PCIE

LPC

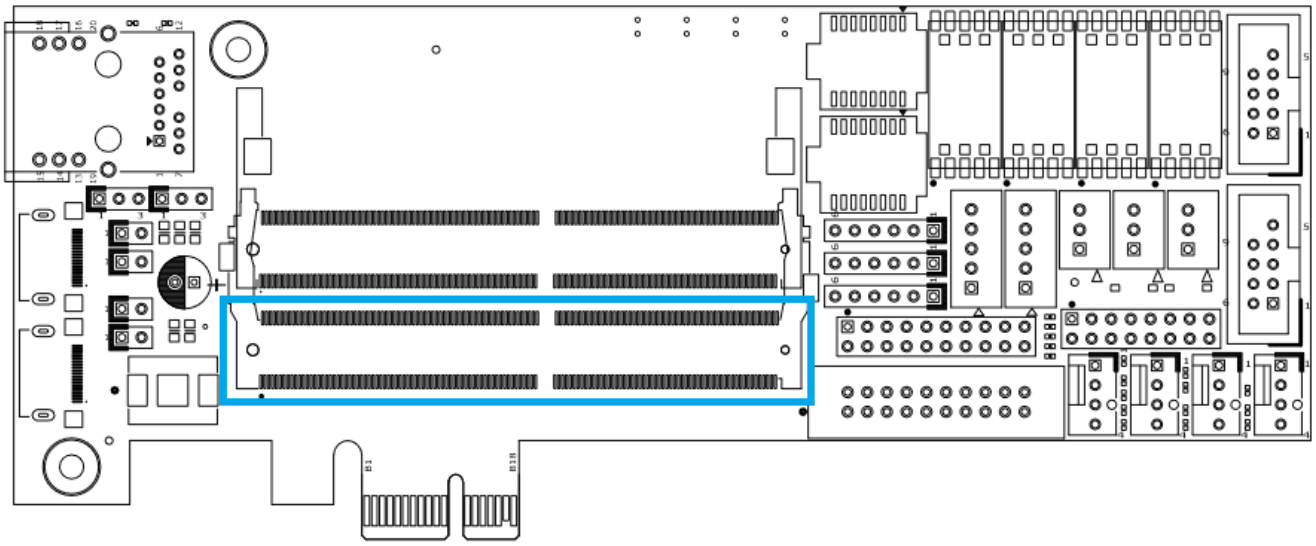
JTAG

MINI HDMI



J13062 / J13082 (top / bottom)			
Pin	**Function**	**Pin**	**Function**
1	TMDS2_GND	2	TMDS2_P
3	TMDS2_N	4	TMDS1_GND
5	TMDS1_P	6	TMDS1_N
7	TMDS0_GND	8	TMDS0_P
9	TMDS0_N	10	TMDS_CLK_GND
11	TMDS_CLK_P	12	TMDS_CLK_N
13	DDC_CEC_GND	14	CEC
15	DDC1	16	DDC2
17	NC (No connect)	18	5V
19	HOT_PLUG_DET		
S1	MH1	S2	MH2
S3	MH3	S4	MH4

MODBMC SOCKET 2

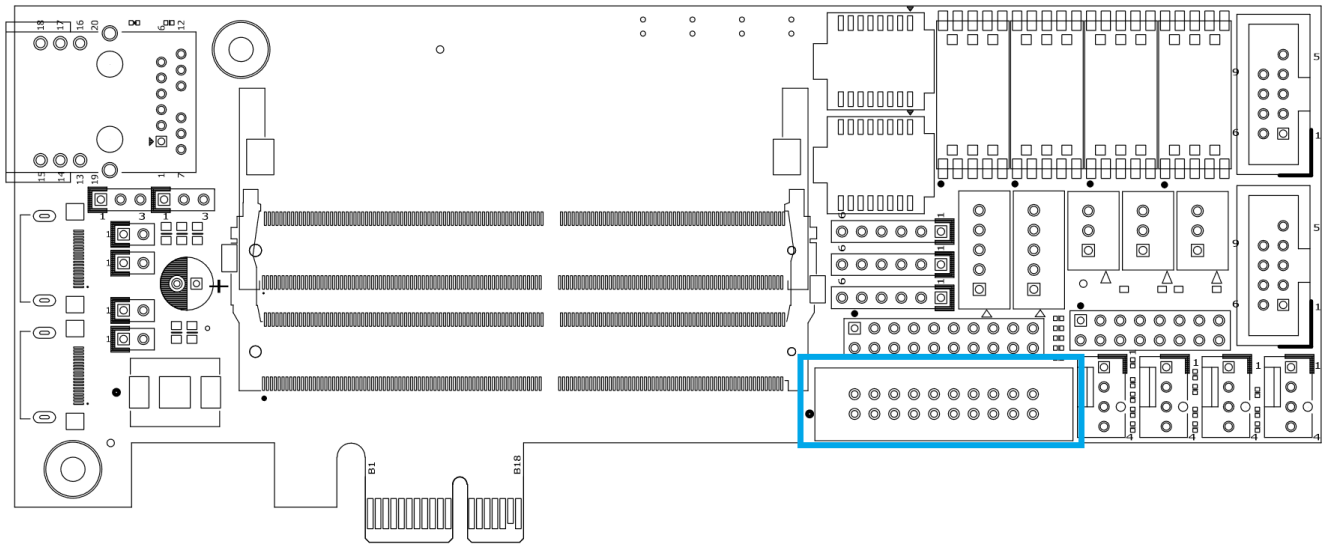


J13080 (Top)					
Pin	FPGA Pin	Function	Pin	FPGA Pin	Function
1	-	VDD_12V_STBY	2	-	VDD_RGMII_REF
3	-	VDD3_3V_STBY	4	-	VDD3_3V_STBY
5	-	VDD3_3V_STBY	6	-	VDD3_3V_STBY
7	-	VDD3_3V_RTC_BATT	8	-	Ground
9	-	Ground	10	-	DACG (No connect)
11	-	Ground	12	-	DACB (No connect)
13	A18	GPIO0	14	-	DACR
15	B18	GPIO1	16	-	HSYNC
17	T2	GPIO3	18	-	VSYNC
19	T3	GPIO5	20	-	DDC_CLK
21	C1	CONSOLE_RX	22	-	DDC_DAT
23	C2	CONSOLE_TX	24	-	Ground
25	EXP0/GPOI0	GPIO7	33	-	Ground
35	EXP0/GPOI1	GPIO15	36	EXP0/GPOI3	GPIO19
37	EXP0/GPOI2	GPIO17	38	EXP0/GPOI4	GPIO20
39	-	Ground	40	EXP0/GPOI5	GPIO21
41	B8	UART1_RX	42	C8	UART2_RX
43	A7	UART2_TX	44	D8	UART2_TX

45	-	Ground	46	EXP0/GPOI6	GPIO25
47	-	I2C8_SCL (No connect)	48	-	I2C13_SCL (No connect)
49	-	I2C8_SDA (No connect)	50	-	I2C13_SDA (No connect)
51	-	Ground	52	-	Ground
53	-	I2C7_SCL (No connect)	54	-	I2C6_SCL (No connect)
55	-	I2C7_SDA (No connect)	56	-	I2C6_SDA (No connect)
57	-	Ground	58	-	Ground
59	EXP0/GPOI7	GPIO35	60	EXP1/SCL	I2C5_SCL
61	EXP0/GPOI8	GPIO37	62	EXP1/SDA	I2C5_SDA
64	-	Ground	66	-	HDMI_TX0_N
68	-	HDMI_TX0_P	70	-	HDMI_TX1_N
72	-	HDMI_TX1_P	74	EXP0/GPOI9	GPIO44
76	EXP0/GPOI10	GPIO45 (No connect)	77	-	PWRGOOD (No connect)
79	-	HDMI_TX2_N	81	-	HDMI_TX2_P
83	EXP0/GPOI11	GPIO51 (No connect)	85	-	HDMI_CLK_N
87	-	HDMI_CLK_P	89	EXP0/GPOI12	GPIO57 (No connect)
91	EXP0/GPOI13	GPIO59 (No connect)	93	EXP0/GPOI14	GPIO61 (No connect)
95	EXP0/GPOI15	GPIO63 (No connect)	97	-	CPU_RST# (No connect)
99	EXP0/GPOI16	GPIO67 (No connect)	101	EXP0/GPOI17	GPIO69 (No connect)
103	EXP1/GPOI0	GPIO71 (No connect)	105	EXP1/GPOI1	GPIO73 (No connect)
107	EXP1/GPOI2	GPIO75 (No connect)	109	EXP1/GPOI3	GPIO76 (No connect)
110	-	Ground	113	EXP1/GPOI4	GPIO77 (No connect)
114	-	Ground	115	EXP1/GPOI5	GPIO79 (No connect)
117	EXP1/GPOI6	GPIO81 (No connect)	119	EXP1/GPOI7	GPIO83 (No connect)
121	EXP1/GPOI8	GPIO85 (No connect)	123	B2	I2C2_SCL
125	B1	I2C2_SDA	126	-	Ground
127	-	Ground	128	D5	I2C1_SCL
129	-	I2C14_SCL (No connect)	130	E4	I2C1_SDA
131	-	I2C14_SDA (No connect)	132	-	Ground
133	-	Ground	134	EXP0/SCL	I2C4_SCL
135	-	I2C16_SCL (No connect)	136	EXP0/SDA	I2C4_SDA
137	-	I2C16_SDA (No connect)	138	EXP1/GPOI9	GPIO98 (No connect)
139	-	Ground	140	EXP1/GPOI10	GPIO99 (No connect)
141	T1	I2C12_SCL	142	A6	PCIE_RST#
143	V1	I2C12_SDA	144	-	UART3_RX
145	-	Ground	146	-	UART3_TX

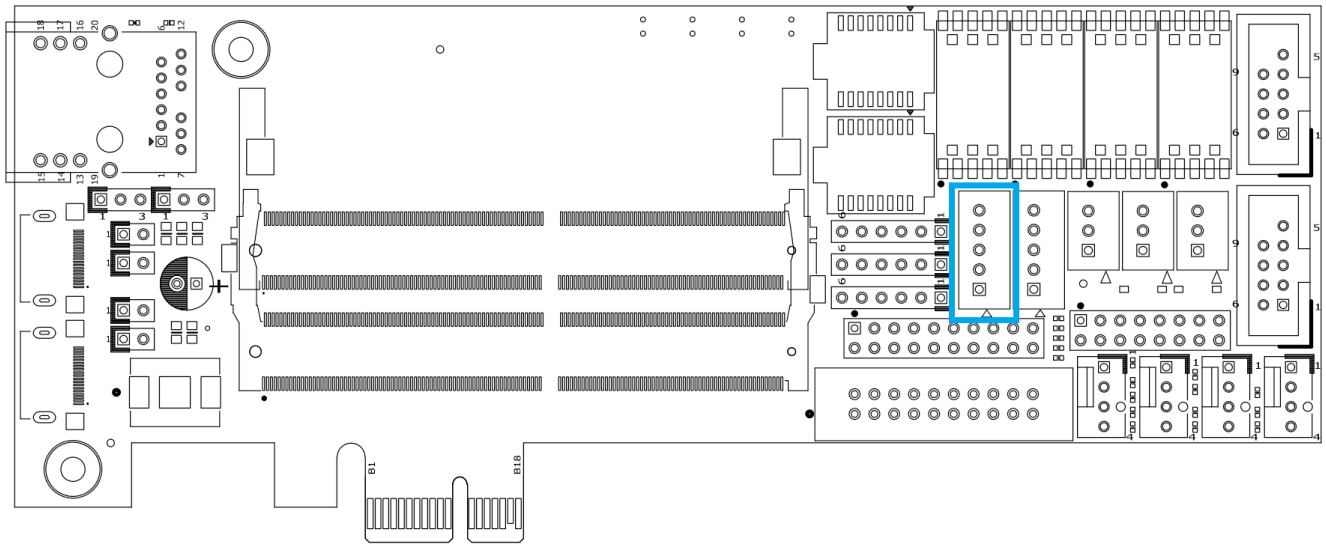
147	W5	PCIE_RX_N	148	-	UART4_RX
149	W4	PCIE_RX_P	150	-	UART4_TX
151	-	Ground	152	-	VDD_LPC3V3
153	Y6	PCIE_TX_N	154	EXP1/GPOI11	GPIO106 (No connect)
155	Y5	PCIE_TX_P	156	EXP1/GPOI12	GPIO107 (No connect)
157	-	Ground	158	-	GPIO108 (No connect)
159	Y12	PCIE_CLK_N	160	-	GPIO109 (No connect)
161	Y11	PCIE_CLK_P			

LOW PIN COUNT (LPC)



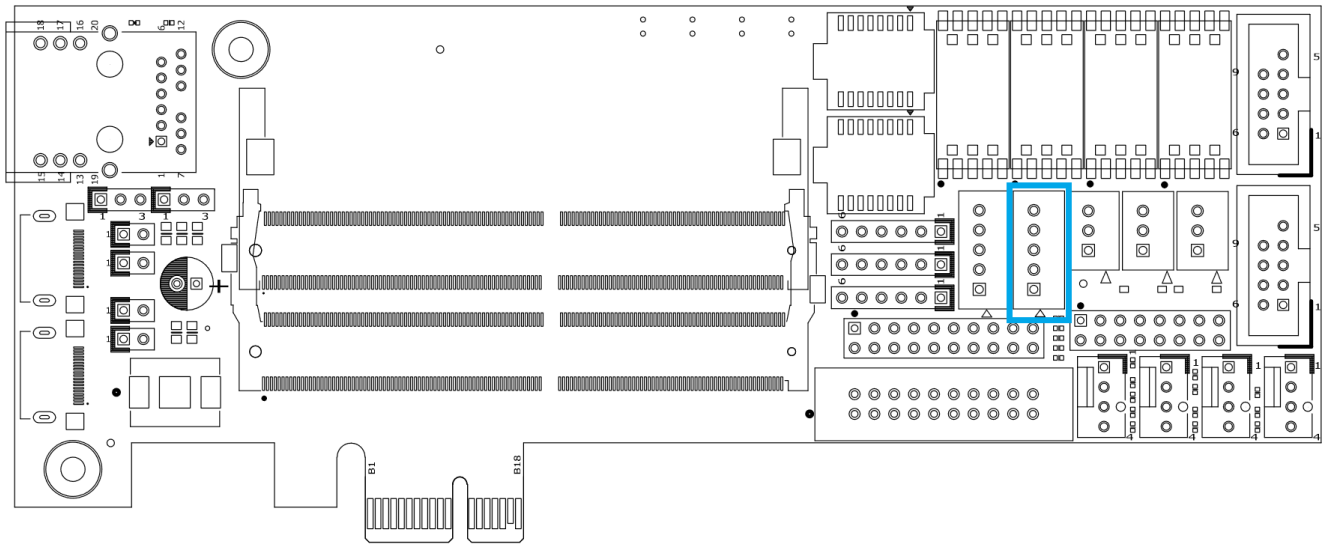
J13083					
Pin	**FPGA Pin**	**Function**	**Pin**	**FPGA Pin**	**Function**
1	H5	LPC_CLK	2	-	Ground
3	D3	LPC_FRAME_N	4	-	NC2 (No connect)
5	C3	LPC_RESET_N	6	-	NC1 (No connect)
7	B3	LPC_AD3	8	B4	LPC_AD2
9	-	3V3_AUX	10	A3	LPC_AD1
11	C4	LPC_AD0	12	-	Ground
13	-	TPM_SCL	14	-	TPM_SDA
15	-	3V3_AUX	16	F4	LPC_SERIRQ
17	-	Ground	18	-	LPC_CLKRUN_N
19	-	WINDOW_OPEN_N	20	-	TPM_GPIO0

FLEXIBLE SERVICE INTERFACE (FSI)



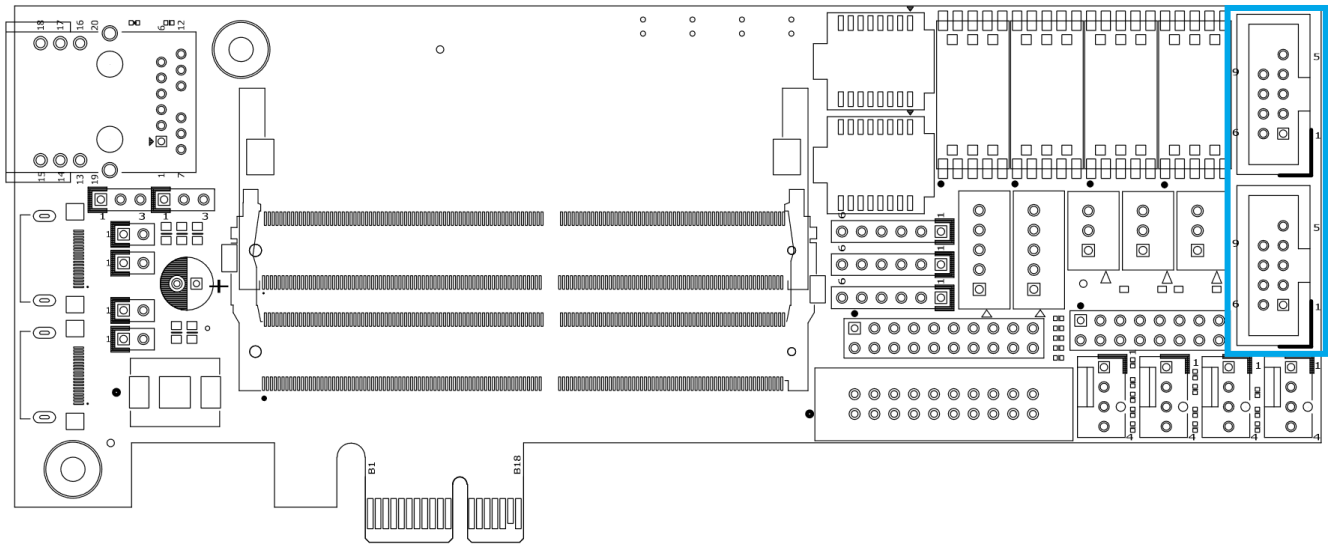
J200				
Pin	FPGA Pin	Function	Pin	Function
1	T2	GPIO_CARD1_3	2	Ground
3	B18	GPIO_CARD1_1	4	Ground
5	A18	GPIO_CARD1_0		

PMBUS



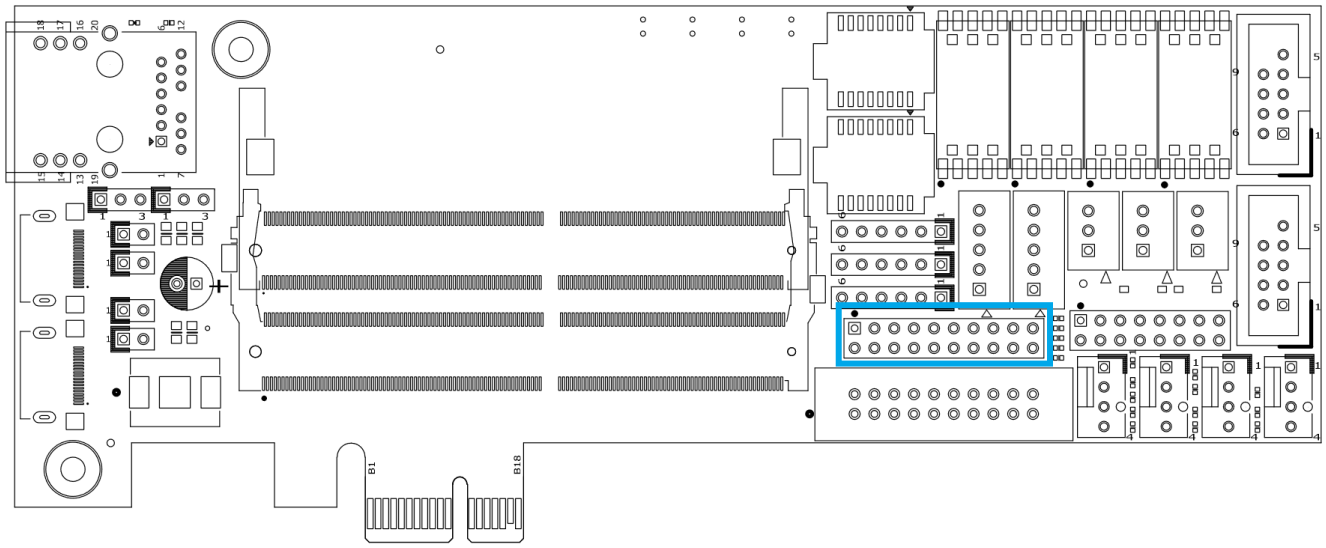
J201					
Pin		**Function**	**Pin**		**Function**
1	T1	I2C_BMC12_SCL	2	V1	I2C_BMC12_SDA
3	EXP1/GPOI0	GPIO_CARD1_71	4	-	Ground
5	-	No connect			

CARD 1 COM PORTS



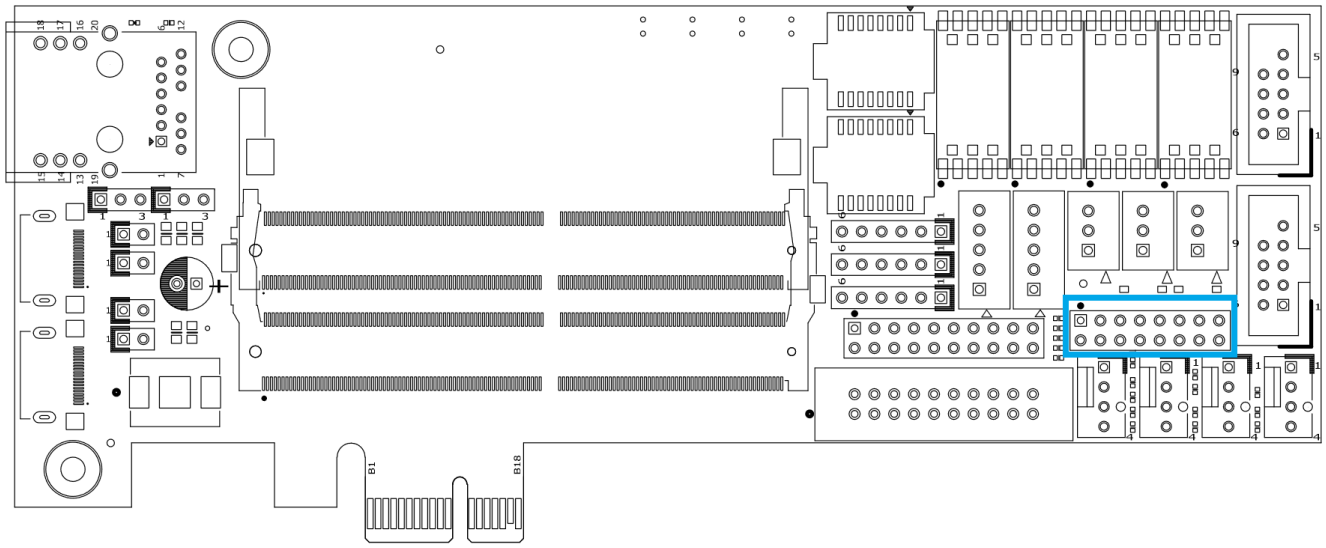
J24 / J25 (Bottom/Top) (COM1 / COM2)			
Pin	**Function**	**Pin**	**Function**
1	COM_DCD	2	COM_RXD
3	COM_TXD	4	COM_DTR
5	Ground	6	COM_DSR
7	COM_RTS	8	COM_CTS
9	COM_NRI		

GPIO BANK 1



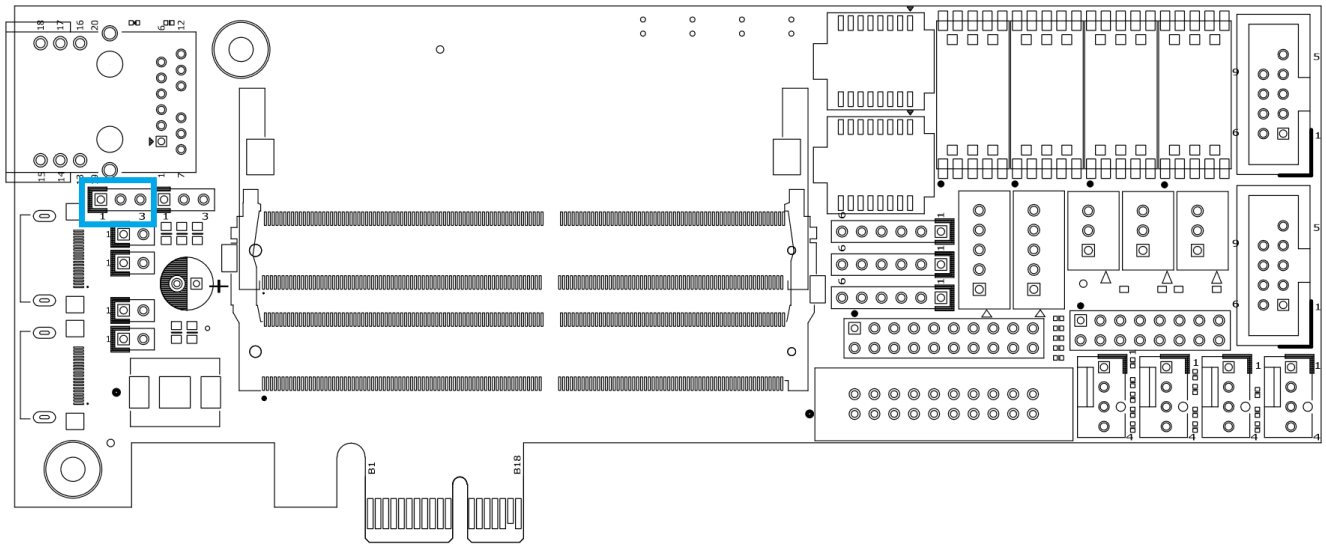
J300					
Pin	FPGA Pin	Function	Pin	FPGA Pin	Function
1	EXP1/GPOI2	GPIO_CARD1_75	2	EXP1/GPOI3	GPIO_CARD1_76
3	EXP1/GPOI4	GPIO_CARD1_77	4	EXP1/GPOI5	GPIO_CARD1_79
5	EXP1/GPOI6	GPIO_CARD1_81	6	EXP1/GPOI7	GPIO_CARD1_83
7	EXP1/GPOI8	GPIO_CARD1_85	8	EXP1/GPOI9	GPIO_CARD1_98
9	EXP1/GPOI10	GPIO_CARD1_99	10	EXP1/GPOI11	GPIO_CARD1_106
11	EXP1/GPOI12	GPIO_CARD1_107	12	A18	GPIO_CARD2_0
13	B18	GPIO_CARD2_1	14	T2	GPIO_CARD2_3
15	EXP0/GPOI0	GPIO_CARD2_7	16	EXP0/GPOI1	GPIO_CARD2_15
17	-	+3.3 Aux Power	18	-	+3.3 Aux Power
19	-	Ground	20	-	Ground

GPIO BANK 2



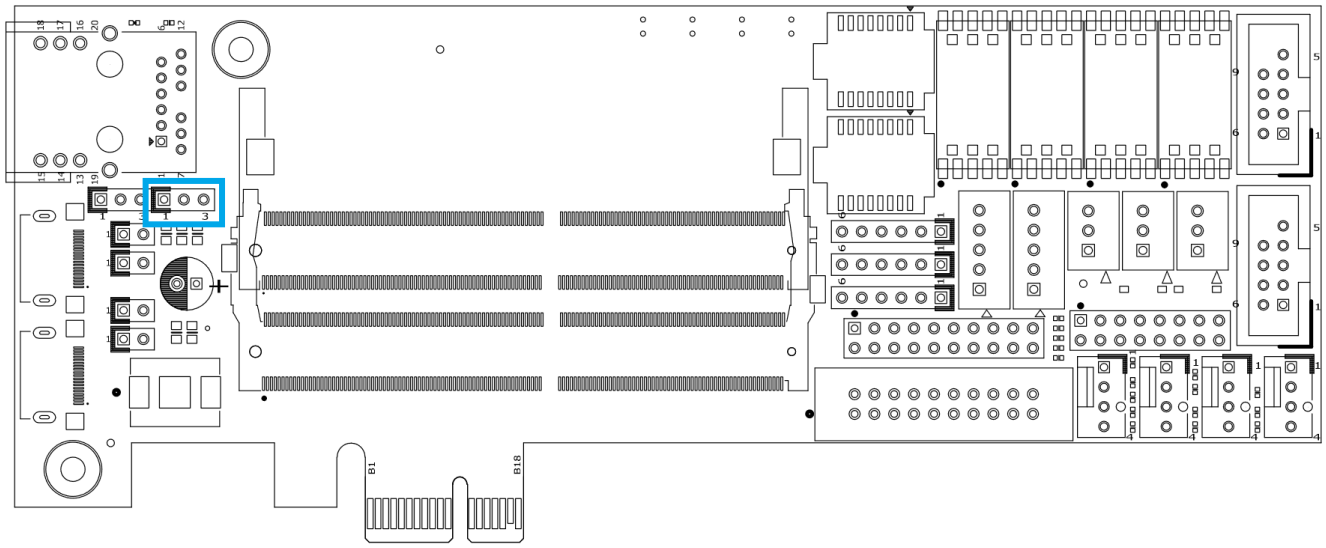
J301					
Pin	FPGA Pin	Function	Pin	FPGA Pin	Function
1	EXP0/GPOI2	GPIO_CARD2_17	2	EXP0/GPOI3	GPIO_CARD2_19
3	EXP0/GPOI4	GPIO_CARD2_20	4	EXP0/GPOI5	GPIO_CARD2_21
5	EXP0/GPOI6	GPIO_CARD2_25	6	EXP0/GPOI7	GPIO_CARD2_35
7	EXP0/GPOI8	GPIO_CARD2_37	8	EXP0/GPOI9	GPIO_CARD2_44
9	-	Ground	10	-	Ground
11	-	+3.3V Host Power	12	-	+3.3V Aux Power
13	-	Ground	14	-	Ground
15	-	+12V Power	16	-	+12V Power

CARD 2 CONSOLE COM PORT



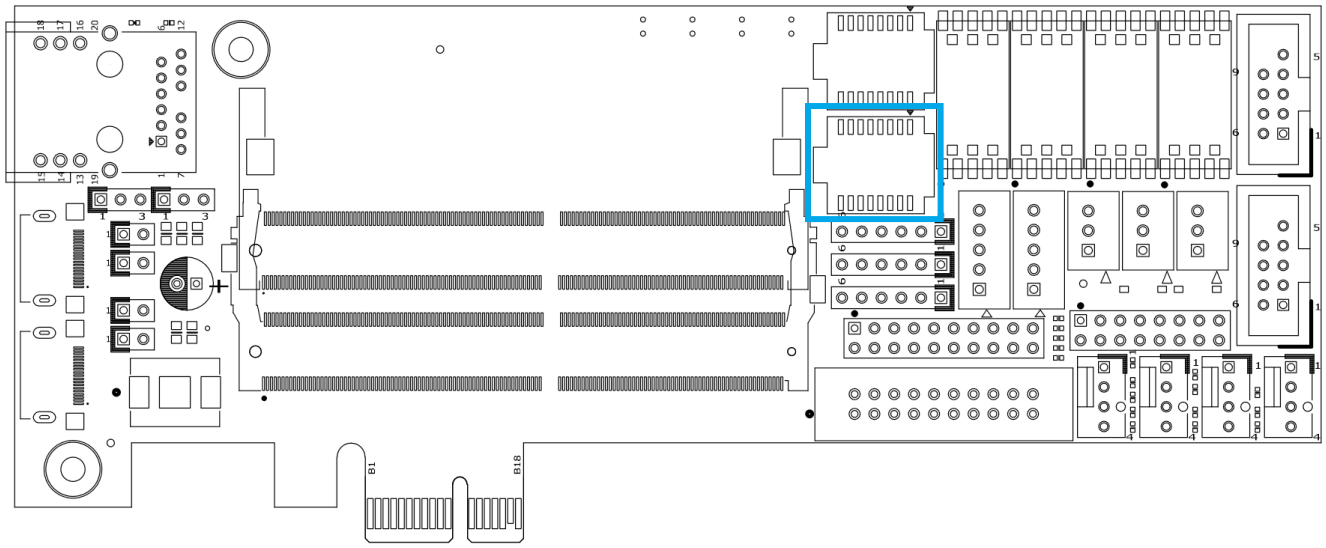
J400		
Pin	**FPGA Pin**	**Function**
1	-	Ground
2	C1	CONSOLE_RX (ModBMC Socket 2)
3	C2	CONSOLE_TX (ModBMC Socket 2)

CARD 2 HOST COM PORT



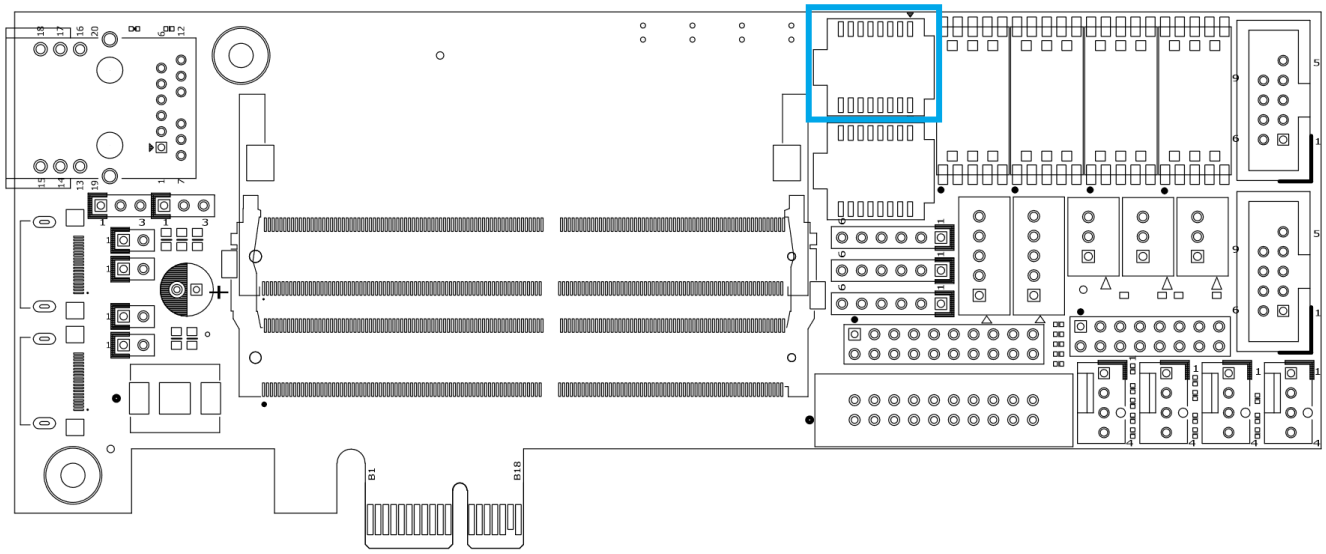
J401		
Pin	**FPGA Pin**	**Function**
1	-	Ground
2	B8	UART1_RX (ModBMC Socket 2)
3	A7	UART1_TX (ModBMC Socket 2)

BMC FIRMWARE ROM



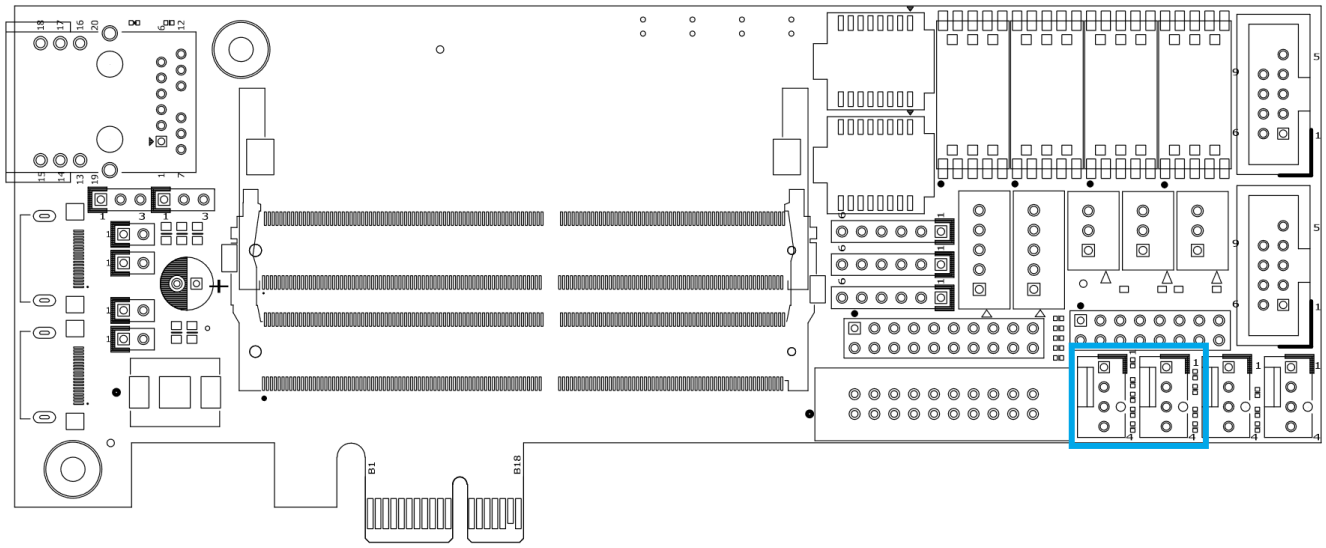
J7500					
Pin	**FPGA Pin**	**Function**	**Pin**	**FPGA Pin**	**Function**
1	H4	HOLD (Active low) / SIO3	2	-	+3.3V Aux Power
3	H4	RESET (Active low)	4	-	NC1 (No connect)
5	-	NC2	6	-	NC3
7	G5	CS (Active low)	8	F5	SO / SIO1
9	Y2	WP (Active low) / SIO2	10	-	Ground
11	-	NC4	12	-	NC5
13	-	NC6	14	-	NC7
15	E3	SI / SIO0	16	E5	SCLK

PNOR FLASH ROM



J7501					
Pin	**FPGA Pins**	**Function**	**Pin**	**FPGA Pins**	**Function**
1	A2	HOLD (Active low) / SIO3	2	-	+3.3V Aux Power
3	A2	RESET (Active low)	4	-	NC1 (No connect)
5	-	NC2	6	-	NC3
7	E2	CS (Active low)	8	F3	SO / SIO1
9	D1	WP (Active low) / SIO2	10	-	Ground
11	-	NC4	12	-	NC5
13	-	NC6	14	-	NC7
15	F2	SI / SIO0	16	G3	SCLK

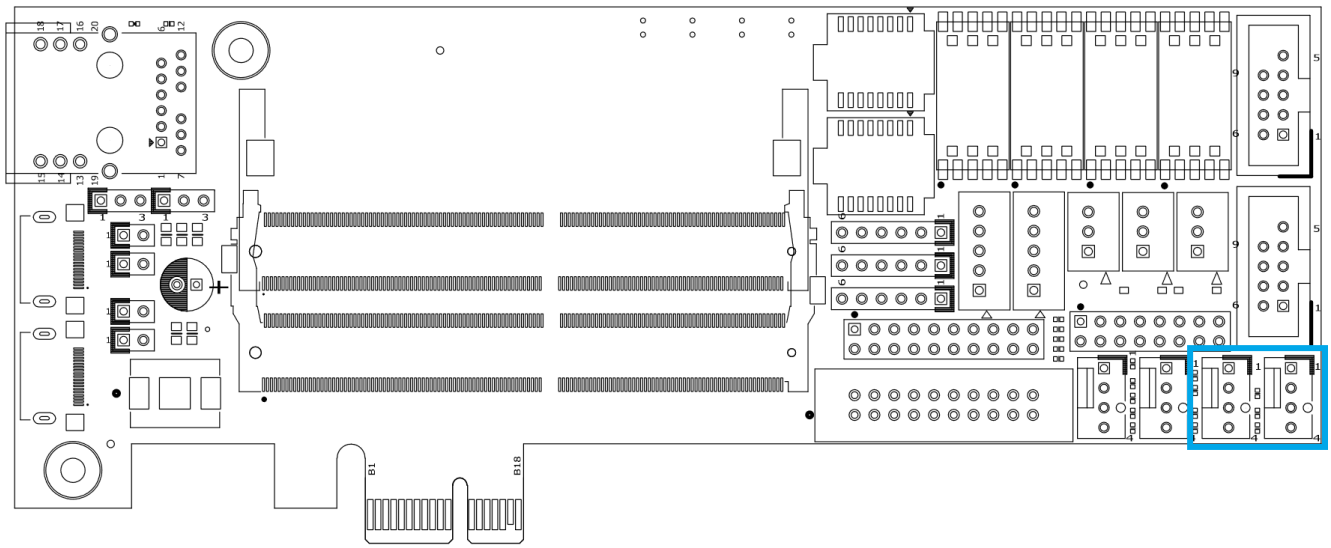
SYSTEM FANS



J7900 (Left)		
Pin	**FPGA Pin**	**Function**
1	-	Ground
2	-	+12V Power
3	E7	Tachometer
4	E1	PWM

J7901 (Right)		
Pin	**FPGA Pin**	**Function**
1	-	Ground
2	-	+12V Power
3	D6	Tachometer
4	H3	PWM

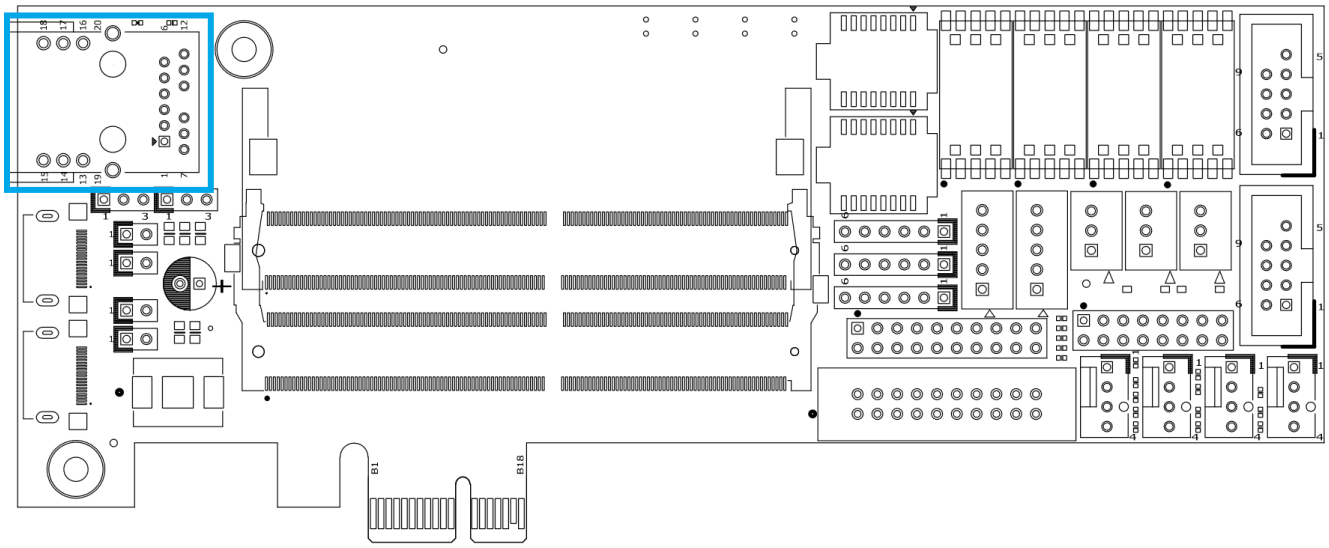
CPU FANS



J7902 (Left)		
Pin	**FPGA Pin**	**Function**
1	-	Ground
2	-	+12V Power
3	D7	Tachometer
4	B5	PWM

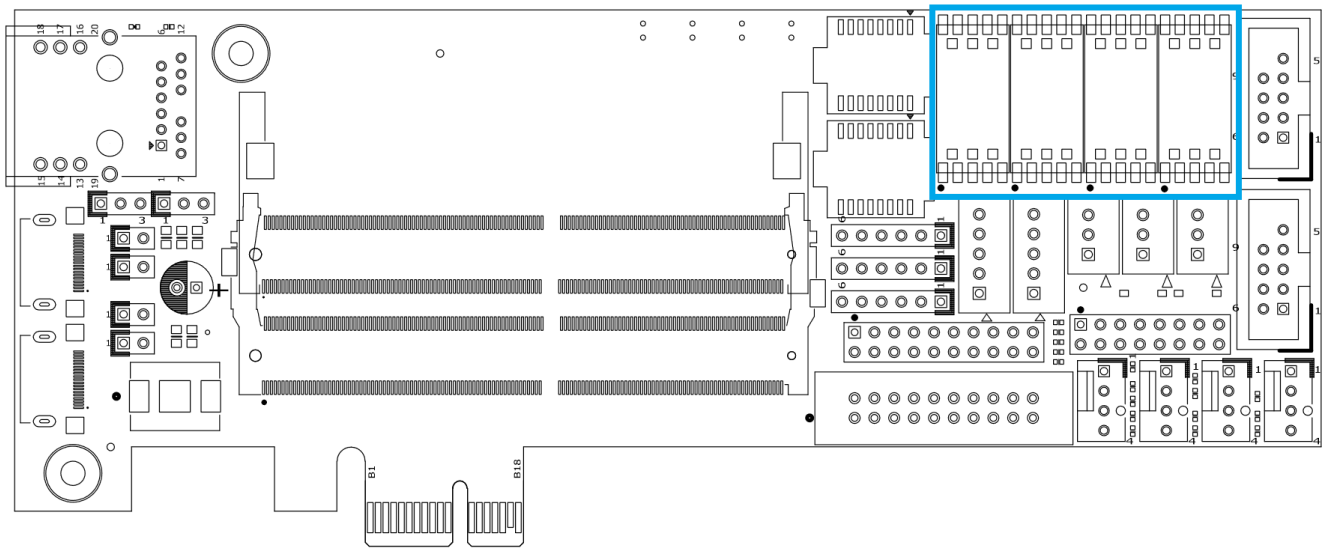
J7903 (Right)		
Pin	**FPGA Pin**	**Function**
1	-	Ground
2	-	+12V Power
3	C6	Tachometer
4	C5	PWM

ETHERNET



J9500			
Pin	**Function**	**Pin**	**Function**
1	TRCT3	2	TRD3-
3	TRD3+	4	TRD2+
5	TRD2-	6	TRCT2
7	TRCT4	8	TRD4+
9	TRD4-	10	TRD1-
11	TRD1+	12	TRCT1
13	D / ORG-	14	D / GRN-
15	COMM	16	Ground
17	GRN-	18	GRN+
19	Ground	20	Ground

LED DISPLAYS



LD1 / LD2 / LD3 / LD4 (left to right)			
Pin	**Function**	**Pin**	**Function**
1	P	2	N
3	M	4	I
5	DP	6	C
7	D	8	E
9	G	10	A
11	B	12	K
13	J	14	CATHODE
15	H	16	F

Support

GETTING HELP

If you require assistance operating your Arctic Tern system, you may contact Raptor Computing Systems technical support directly at support@raptorcs.com. Alternatively, we also have a Wiki and other support resources available online at https://www.raptorcs.com; the information you require may already be available on one of these resources.