POWER9 Processor Registers Specification

Volume 3

Advance

9 May 2017—IBM Confidential
Version 1.2

Printed in the United States of America May 2017

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Revision Log

Each release of this document supersedes all previously released versions. The revision log lists all significant changes made to the document since its initial release.

Version	Revision Date	Description
1.2	9 May 2017	Updated the following registers: ADR DLL VREG Control Register DP16 DFT/PDA Control Register DP16 DLL VREG Control 0 Register DP16 DLL VREG Control 1 Register DP16 DQSClk Offset Register DP16 Read Clock Enable and Selection Register DP16 Read Delay Value {0-11} Register DP16 Read Diagnostic Configuration 5 Register DP16 Write Clock Enable and Clock Selection DP16 Write Delay Value {0-23} Register DP16 Write VREF Error 0 Register DP16 Write VREF Error 1 Register PC Initial Calibration Config0 Register PC Mode 0 Register PC Mode 1 Register PC Mode 2 Register PC Mode 3 Register PC Mode 4 Register PC Mode 5 Register PC Mode 6 Register PC Mode 7 Register PC Rank Pair 0 Register PC Rank Pair 1 Register PC Rank Pair 2 Register PC Rank Pair 3 Register RC Configuration 0 Register RC Configuration 2 Register RC Error Status 0 Register WC Configuration 2 Register
1.1	31 January 2017	In additon to editorial changes, the following registers were updated or added: ADR DCD Control Register ADR DFT Wrap Status and Control Register ADR DLL Control Register ADR DLL DAC Lower Register ADR DLL DAC Upper Register ADR DLL Software Control 0 Register ADR DLL Software Control 1 Register ADR DLL VREG Coarse Register ADR DLL VREG Control Register ADR DLL/VREG Configuration 1 Register ADR Power Down 2 Register ADR SysClk Phase Rotator Control Register ADR SysClk Phase Rotator Value Register ADR WRClk Phase Rotator Offset Value Register APB ATEST Multiplexer Select Register APB Error Status 0 Register APB FIR Error 0 Register DP16 Config 0 Register DP16 Configuration 0 Register DP16 CTLE Control Byte 0 Register DP16 DCD Control 0 Register DP16 DCD Control 1 Register

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1.0	30 August 2016	Initial release.

About this Document

This document describes the registers used by the IBM® POWER9 processor. To ensure you have the most current version of this document, visit the IBM Portal for OpenPOWER.

Who Should Read this Document

This document is intended for system software and hardware developers and application programmers who are developing products that use the POWER9 registers. It is assumed that the reader understands operating systems, microprocessor system design, basic principles of reduced instruction set computer (RISC) processing, and details of the Power Instruction Set Architecture (ISA).

Organization

This document is divided into three volumes, of approximately equal sizes, organized by address ranges.

Volume	Address Range	Contents
1	0x0000_0000 - 0x050F_FFFF	Chip logic registers Processor bus registers
2	0x0600_0000 - 0x200F_FFFF	X bus chiplet registers[1] OB chiplet registers[1] PCI registers Cache and core registers
3	0x0700_0000 - 0x070F_FFFF	Memory controller registers[1]

1. These registers use indirect addresses in the range 0x8000_0000_0000_0000 - 0x8000_0000_0901143F.

In each volume, the table of contents lists the primary divisions in the document. Address maps at the beginning of each chapter list the registers in each chiplet in alphabetical order by mnemonic. Within each chapter, the registers themselves are arranged by their addresses. A register can have multiple addresses with different addresses for different chiplets.

Bit Significance

In the POWER9 documentation, the smallest bit number represents the most significant bit of a field, and the largest bit number represents the least significant bit of a field.

Representation of Numbers

Numbers are generally shown in decimal format, unless otherwise designated. One of the following conventions is used to indicate the numeral system, where "nn" or "NN" indicates the numerical value:

- Binary values are represented as 0bn, `nn'b, or `n'.
  Examples: 0b01, `01'b, or `01'
- Decimal values are represented as nn or `nn'd.
  Examples: 1 or `1'd
- Hexadecimal values are represented as 0xN, x`N', or `NN'h.
  Examples: 0x000000000204000D, x`000000000204000D', or `000000000204000D'h

Note: A bit value that is immaterial, which is called a “don't care” bit, is represented by an “X” or "x."

Representation of Enumerated Registers

To succinctly describe registers that are identical except for a numeral in the register name and mnemonic, a syntax is used that enables these “enumerated registers” to be described in a single register table.

The registers in the DP16 section are enumerated because there are five instances of the DP16 unit for each DDR PHY port. All five instances are required for each DDR PHY port, and, at the chip level, there are eight DDR PHY ports. Each DDR PHY unit is self-contained and comprises four independent ports that connect to DIMM slots. This unit is replicated twice on the POWER9 system to provide a maximum of eight ports. All of the DP16 registers are documented in one replication. The address is the only difference between the two. The first replication is on 0x0000_0000_0700_0000, and the second replication is on 0x0000_0000_0800_0000.

For example: IOM0.DDRPHY_DP16_DATA_BIT_ENABLE0_P0_[n]
8000000007 01103F (SCOM), +0x0400_0000_0000

IOM1.DDRPHY_DP16_DATA_BIT_ENABLE0_P0_[n]
8000000008 01103F (SCOM), +0x0400_0000_0000

Register Names

The following syntax is used for enumerated register names:

<register name> [n] (n = m:p) where m and p are integers

For example: TWG Control Register [n] (n = 0:15)

Mnemonic

The following syntax is used for enumerated mnemonics:

<mnemonic>_[n], where n is an integer from the enumerated register name

For example: REG_TWGDATA_[n]
REG[n]_TWGDATA

Address Offset

The following syntax is used for enumerated address offsets so that enumerated registers can be described in a single register table. The stride defines the hexadecimal integer to add to the address for each enumeration.

<address_offset>, +<stride>

For example: 0x80030, +0x10

Register Name	**DP16 DQ Enable 0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQ_BIT_ENABLE0_P0_[n]
Address	800000000701103F (SCOM), +0x0400_0000_0000
Description	A DP16 has 24 possible single-ended data pins that can send or receive data. This register is used to enable and disable each of the 24 pins for data sending or receiving. Any pins on the DP16 that are used as strobes or clocks to capture the data must not be marked as enabled in this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DATA_BIT_ENABLE_0_15: 1b = Indicates that the DP16 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. 0b = Indicates that the DP16 bit is not used to send or receive data. Bit 48 controls MEMINTD00B(n). Bit 49 controls MEMINTD01B(n). Bit 50 controls MEMINTD02B(n). ... Bit 63 controls MEMINTD15B(n). where n is the DP16 instance number.

Related Documents

The following documents can be helpful when reading this specification. They are available on the IBM Portal for OpenPOWER.

POWER9 Processor User's Manual
POWER9 Processor Datasheets
Power ISA User Instruction Set Architecture - Book I (Version 3.0)
Power ISA Virtual Environment Architecture - Book II (Version 3.0)
Power ISA Operating Environment Architecture (Server Environment) - Book III-S (Version 3.0)

Terminolgy

The following terms are used in volumes 1, 2, or 3 of the *POWER9 Processor Registers Specification*.

Note: Acronyms are not typically expanded in the body of this document.

1D	One dimensional
2D	Two dimensional
3DS	Three-dimensional stacking
AADR	Array Access Data Register
AAER	Array Access ECC Register
ABIST	Array built-in self test
ABIST/IOBIST	Array built-in self test / input/output built-in self test
ABUS	**Note:** This is not really an acronym but a name (A bus).
AC	Alternating current
ACK	Acknowledgment or acknowledge. A transmission that is sent as an affirmative response to a data transmission.
ACT	Activate
ACT#	Activate (inverted)
ADC	APSS with analog-to-digital converter
ADDR	Address
ADR	Address
ADU	Alter-display unit
AES	Advanced Encryption Standard
AFSR	Average Frequency Sample Register
AFTR	Average Frequency Threshold Register
AIB	1. ASIC interconnect bus 2. ASIC interface bus
AL	Additive latency. For more information, see the JEDEC DDR3 and DDR4 DRAM specifications.
AMF	Availability management framework
AMux	Analog multiplexer
ANA16	Analog 16 bits
AND write	Current register content is ANDed with write data and the result is stored in the register (access type WO_AND / WOX_AND).
AP	Auto-predischarge. For more information, see the JEDEC DDR3 and DDR4 DRAM specifications.
APB	Advanced peripheral bus
APIN	ADR pin. The logic macro inside DDR units for sending data to the ADR bus.
APSS	Analog power subsystem sweep. Provides real-time power measurements of voltage rails.
ARB	Architecture Review Board

ARE	Address error
ARY	Array
ASB	Advanced system bus
ASBE	Array single-bit error
ASIC	Application-specific integrated circuit
AT	Address translation
ATEST	Analog test pin
ATPG	Advanced test pattern generator
AUE	Array uncorrectable error (UE)
AVP	Architectural verification program. A custom payload used to test a processor or other host hardware or software function.
AVS	Adaptive voltage scaling
Âµ	Micron
Âµs	Microsecond
B	Byte
BA	Bank address
BAR	Base Address Register
BCDE	Block copy download engine
BCE	Block copy engine
BCEBAR	Block Copy Engine Base Address Register
BCECSR	Block Copy Engine Control and Status Register
BCUE	Block copy upload engine
BCW	Buffer control word
BDF	Bus device function
BE	1. Big-endian 2. Branch Trace Enable bit in the MSR (MSRBE) 3. Byte enable
BER	Bit error rate
BG	Bank group
BI	Burn in
BIST	Built-in self test
BL	Bit length
BL8	Burst length 8
BNDY	Boundary I/Os
BSC	Boundary scan cells

BW	Bandwidth
BYPASSN	Bypass low active
c_err_rpt	Common lib error report
CACCR	Core Analog Clock Control Register
CACSR	Core Analog Clocking Status Register
CAL	Calibration
CAM	Content-addressable memory
CAPI	Coherent Accelerator Processor Interface
CAPP	Coherent accelerator processor proxy
CAS	Column-address select
CASN	Column-address select (inverted)
CAW2	An internal pipeline stage designator
CBS	CFAM boot sequencer
CC	1. Clock controller 2. Congruence class
CCB	Change control board
CCFG	Clock control configuration
CCS	Configured command sequencer
CD	Compact disc
CDIMM	Custom dual in-line memory module
CDR	Clock and data recovery
CE	Correctable error. A hardware error that the firmware detects and corrects without impacting the state of the system.
CERR	Common lib error report
CFAM	Common field-replaceable unit (FRU) access macro
CFIR	Chiplet Fault Isolation Register
CGC	Congruence class
checkstop	A severe error inside a processor core that causes a processor core to stop all processing activities. This is the same as a system crash. The operating system is not functional.
chip select	A signal that selects one or more memory modules to respond to a command/address. An exact one-to-one correspondence exists between chip selects and ranks.
CI	1. Cache-inhibited 2. Cast-in
CID	Completer ID. When returning the completion for a transaction, the completer attaches its Bus/Dev/Func to the transaction as a CID. See also RID.
CIDSR	Core IVRM Dropout Sample Register

CK	Clock
CK#	Clock (inverted)
CKE	Clock enable
CKSW	Chicken switch: A programmable mode bit that disables a certain function or changes its behavior.
CL	Column-address select (CAS) latency
CLK	Clock
CMD, cmd	Command
CME	Core management engine
CMOS	Complementary metal-oxide semiconductor
CMSK	Logical built-in self test (LBIST) channel mask
CO	Cast-out
CP	Chip pump
CPB	Coprocessor parameter block
CPI	Cycles per instruction
CPLT	Chiplet
CPLT_CTRL	Chiplet control
CPM	Critical path monitor
CPPM	Core PCB-slave power management macro (PPM)
CPS	Cycle-per-step
CQ	1. Common queue. Refers to the interface to the SMP interconnect. 2. Completion queue
CRC	Cyclic redundancy check
CRESP	Combined response
CS	Chip select
CSID	Chip select ID
CSN	Chip select (inverted)
CTL	Control
CTLE	1. Continuous time linear equalization 2. Continuous time linear equalizer
CTRL	Control
CWL	CAS write latency
D/A	Display/alter
DAC	Digital-to-analog converter
DACTEST	DAC test

DBG	Debug
DBSR	Debug Status Register
DC	Direct current
DCACHE	Data cache
DCBZ	Data cache block set to zero
DCD	Duty cycle distortion
DCM	Dual-chip module
DCTEST	This is a mode where test operations are executed at very low frequencies.
DDR	Double data rate
DDR3	Double data rate type three
DDR4	Double data rate type four
DDRPHY	Double data rate physical interface
DEC	Decrementer
DERR	Distributed elastic round robin
DFE	1. Decision feedback equalization 2. Decision feedback equalizer
DFI	DDR PHY interface bus
DFT	Design for test
DGEN	Data pattern generator
diag	Diagnostic
DIMM	Dual in-line memory module. A small circuit board with memory-integrated circuits containing signal and power pins on both sides of the board.
DIN	Data in
DL	Downlink
DLDCH	Downlink data channel
DLL	1. Delay-locked loop 2. Dynamic link library
DLL/VREG	Delay-locked loop/voltage regulator
DLL/ZCAL	Delay-locked loop/impedance (Z) calibrator
DMA	1. Direct memory access. A technique for using a special-purpose controller to generate the source and destination addresses for a memory or I/O transfer. 2. Direct memory attach
DP16	Data path 16
DPC	DIMMs per port
DPLL	Digital phase-locked loop
DPLLFREQ	DPLL frequency control

DQ	1. Data 2. Data bit
DQS	Data strobe
DQSCLK	Data strobe clock
DR	1. Data Relocate bit in MSR (MSRDR) 2. Dynamic reconfiguration. The capability of a system to adapt to changes in the hardware/firmware physical or logical configuration, and to be able to use the new configuration, all without having to turn the platform power off or restart the operating system. See the *Power Architecture Platform Requirements (PAPR)* document for more information.
DRAM	Dynamic random-access memory. Storage in which the cells require repetitive application of control signals to retain stored data.
DRTM	Dynamic root of trust for measurement
DSI	Data storage interrupt.
DSM	Digital state machine
DSMP	Distributed symmetric multiprocessing
DTS	Digital thermal sensor
EA	Effective address. An address generated or used by a program to reference memory. A memory-management unit translates an EA to a virtual address (VA), which it then translates to a real address (RA) that accesses real (physical) memory. The maximum size of the effective-address space is 264 bytes.
EAT	1. Effective address translation 2. Event assignment table
ECC	See error correction code
EDAT	Even data
EDI	Elastic differential interface. A bus that consists of high-speed differential I/O links. The memory bus instance of an EDI bus is a “DMI bus,” and the off-module, fabric bus (between processors) instance of an EDI bus is an “A bus.”
EDR	Error Data Register
eDRAM	Embedded dynamic random access memory
EH	Exclusive access hint
EICR	Error Inject Control Register
EIIR	External Interrupt Injection Register
EIMR	External Interrupt Mask Register
EINR	External Interrupt Input Register
EIPR	External Interrupt Polarity Register
EISR	External Interrupt Status Register
EITR	External Interrupt Type Register
ELPR	Error Log Pointer Register
EM	Electron migration

EMC	Extended memory controller
ENOP	End sync/wait step; no operation
EOT	End of transfer
EPS	1. Entry-level power supply 2. Pervasive end points
EQ	Event queue
ERAT	Effective-to-real-address translation, or a buffer or table that contains such translations, or a table entry that contains such a translation.
ERR	Error
error correction code	A code appended to a data block that can detect and correct bit errors within the block.
ERRSUM	Error summary
ERS	Early read start
ETE	Error threshold exceeded
ETU	Express transaction unit
EXT	JTAG EXTEST instruction mode
FARB	Final arbiter. Part of the memory interface command sequencer (scheduler).
FARR	Fast array unload
FBC	Fabric bus connection
FET	Field-effect transistor
FFDC	First failure data capture. A collection of data used upon fail to analyze the root cause of the failure.
FIFO	First in, first out. Refers to one way elements in a queue are processed. It is analogous to “people standing in line.”
FIR	Fault Isolation Register. Register bits that show which piece of hardware failed.
FMAX, fmax	Maximum frequency
FMIN, fmin	Minimum frequency
FMULT	Frequency multiplier
FPGA	Field-programmable gate array
FSAFE	Safe frequency
FSI	1. Flexible service interface. The FSI covers all resources, except FSI slave 0 and slave 1, when addressed from an external service element via the FSI. 2. FRU support interface
FSI2PIB	FRU support/service interface to the pervasive interconnect bus
FSM	Finite state machine

FSP	Flexible service processor. An embedded controller for internal system control tasks in IBM Power Systems™. In addition to the processor core, the following I/O interfaces are integrated into the embedded controller: I²C, JTAG, UART, GPIO, FSI.
FUNC	Functional
FW	Firmware
FWMR	Firmware Mode Register
Gbps	Gigabits per second
GCR	Global control ring
glsmux	Glitchless multiplexer
GND	Ground
GPE	General-purpose engine
GPIO	General-purpose input/output
GPO	Global PHY offset
GPR	General Purpose Register
GPTR	General Purpose Test Register
GZIP	A file format used for file compression and decompression.
H/W	Hardware
HCA	1. Host channel adapter 2. Hot/cold affinity
HID	Hardware implementation dependent
HIRES	High resolution
HLD	High-level design
HMER	Hypervisor Maintenance Exception Register
HMI	Hypervisor maintenance interrupt
HP	High performance
HPC	High-performance computing
HSS	High-speed serial
HTB	Hierarchical test block
HTML	Hypertext Markup Language
HW	Hardware
HWCTRL	Hardware control
HYP	Hypervisor
I/O	Input/output
IAR	Instruction Address Register
IAUE	Intermittent array uncorrectable error

IC	Integrated circuit
ICACHE	Instruction cache
ICE	Intermittent chip error
ICP	Interrupt control presenter
ICRR	Inter-CME Communication Receive Register
ICS	Interrupt controller source
ICSW	Initiate coprocessor store word
ID	Identification
IDCR	IVRM Dropout Configuration Register
IE	Input enable
IEEE	Institute of Electrical and Electronics Engineers
IF	Interface
IFU	Instruction fetch unit
IMA	In-memory accumulate
IMA/PPE/HTM	In-memory accumulate/Power PC® element/hardware trace macro
IMPE	Intermittent mark placed error (MPE)
INIT	Initialization
INOP	Initial sync/wait step; no operation
INT	INTEST instruction support. The INTEST instruction can be triggered through JTAG or through register control.
INTP	Interrupt presenter
INV	JTAG enable inversion macro
IO or I/O	Input/output
IOBIST	Input/output built-in self test
IOOPPE	PPE used for control of I/O macros
IOP	1. I/O processor 2. Internal operation
IOTK	I/O toolkit
IP	1. Interrupt Prefix bit in MSR (MSRIP) 2. Internet protocol
IPL	1. Initial program load. The time between when power is applied to the platform hardware and when the payload is fully functional. 2. Interrupt presenter layer
IPW	Initial pattern write
IR	1. Infrared 2. Instruction Relocate bit in the MSR register (MSRIR)
IRCD	Intermittent register clock driver

IS	Industry standard
ISA	Instruction set architecture
ISU	1. Instruction sequencing unit 2. Interrupt source unit
ITR	Inherent time redundancy
IUE	Intermittent uncorrectable error
IVRM	Internal Voltage Regulation Module
IVRMCR	IVRM Control Register
IVRMDVR	IVRM Data Value Register
JEDEC	Formerly the Joint Electron Device Engineering Council
KHz	Kilohertz
L2SFF	Level 2 (L2) star flip flop
LBIST	Logical built-in self test
LBS	LBIST
LBUS	Local bus
LCB	1. Local clock buffer 2. Logon control block
LEM	Local error macro
LFSR	Linear Feedback Shift Register
LPID	Logical partition identification
LRDIMM	Load-reduced dual in-line memory module
LSB	Least-significant bit or byte
M/S	Master/slave
MA	Memory address
malf	Malfunction alert
MASK	A pattern of bits used to accept or reject bit patterns in another set of data. Hardware interrupts are enabled and disabled by setting or clearing a string of bits, with each interrupt assigned a bit position in a mask register.
MB	1. Mailbox 2. Megabyte
MBA	Memory buffer asynchronous
MBASE	Memory base
Mbps	Megabits per second
MBR	Member
MBS	Memory buffer synchronous
MC	1. Memory channel 2. Memory controller

MCA	The portion of the memory controller that runs synchronously to the memory interface.
MCB	The portion of the memory controller that runs synchronously to the DMI interface.
MCBCM	Memory controller built-in self-test compare mask
MCBCMQ	Memory Controller Built-In Self-Test Compare Mask Register
MCBIST	Memory card built-in self test
MCBIST-RQ	Memory controller built-in self-test to sequencer reorder queue interface
MCBMCAT	Memory controller built-in self-test maintenance current address trap
MCD	Memory coherency directory
MCE	1. Machine check exception 2. Mark corrected error 3. Marked chip correctable error
MCHK	Machine check
MCU	Memory control unit
MDI	Memory directory indicator. The MDI bit specifies the current scope of the data (local versus global).
MEM	Memory
MEMCTL	Memory control
MEMCTLCLKI	Memory controller interface clock
MEMINT	Memory interface
MEMINTCLKO	Memory interface clock
MFSI	Master flexible service interface
MHz	Megahertz
MIB	Memory interface bolt-on. Enables the programmable PowerPC-lite engine (PPE) to access its local memory and pervasive interconnect bus (PIB) interface.
MISO	Master input/slave output
MISR	Multiple Input Shift Register
MMIO	Memory-mapped input/output. Refers to the mapping of the address space required by an I/O device for Load or Store operations into the system's address space.
MOSI	Master output/slave input
MPE	Mark placed error
MPR	Multipurpose Register
MPW	Modify pulse width
MR3	Mode Register 3
MR6	Mode Register 6

MR7	Mode Register 7
MRS	Mode register set
MSB	Most-significant byte
MSGSND	Message send
MSR	Machine State Register
MT/s	Megatransfers per second
MTMSR	Move to Machine State Register instruction
MTSPR	Move to Special Purpose Register instruction
MULT	Multiplier
Multiple ranks	More than one rank of memory modules, where the data buses from each rank are connected to a common data bus of a single port. Data bus connections have multiple drops equal to the number of ranks attached. When more than one rank exists, this memory is depth-expanded memory.
MUX	Multiplexer
N/A	Not applicable
N/M	Memory command throttling mechanism specifying how many (N) commands are allowed to be issued to memory within every M-wide time window.
N/P	N-channel or p-channel transistor type
N1L	The name of a type of latch
NA	Not applicable
NACK	Negative acknowledgment
NBTI	Negative bias temperature instability
NC	Not connected; that is, the data cannot be written or read by that access.
NCE	New correctable error
NCF	NVIDIA® NVLink™ configuration fatal
NCLK	Nest clock
NCU	Noncacheable unit
NCX	Same as NC, but unstable (can be changed functionally)
NFET	Negative field-effect transistor
NHTM	Nest hardware trace macro
NM	See N/M.
NMMU	Nest memory management unit
NOP	No operation. A single-cycle operation that does not affect registers or generate bus activity.
NPU	NVLink processing unit
NVF	NVLink fatal

NVLD	Non-valid read/write data address
NVT	NFET threshold voltage
NX	Nest accelerator
OCB	On-chip controller (OCC) control bridge
OCC	On-chip controller. Provides power and thermal management, power cap enforcement, over-temperature protection, and low-power mode management.
OCCERRPT	OCC Error Reporting Register
OCI	On-chip-controller interface. Interface used by power management.
ODAT	Odd data
ODT	On-die termination
OE	Output enable
OEAR	OCI Error Address Register
OESR	OCI Error Status Register
OF	Open firmware
OHA	On-chiplet hardware assist
OISR	OCC Interrupt Source Register
OITR	OCC Interrupt Type Register
OJCFG	OCC JTAG Configuration Register
OJIC	OCC JTAG Instruction and Control Register
OJSTAT	OCC JTAG Status Register
OJTDI	OCC JTAG TDI Register
OOB	Out-of-band bus
OPB	On-chip peripheral bus
OPCG	On-product clock generator
OPCGGO	On-product clock generator “GO” signal
OR write	Current register content is ORed with write data and the result is stored in the register (access type WO_OR/WOX_OR).
OS	1. Open source 2. Operating system
OSC	Oscillator
OSCSW	Oscillator switch
OTP	One-time programmable
OTPROM	One-time programmable read-only memory
p2s	Parallel-to-serial machine

PBA	1. Pending bit array 2. Per buffer addressability 3. Power management processor bus interface 4. Power bus access (used by power management)
PBAX	PBA messaging
PC	1. Performance counter 2. Personal computer 3. Pervasive core unit 4. PHY control
PCB	1. Pervasive control bus. Processor logic that provides a generic, modular structure for communication between pervasive (glue logic between chiplets) elements. The PCB is used for read and full write access. 2. Printed circuit board
PCBIF	Pervasive control bus interface
PCBMS	PCB multiplexer
PCBSLAVE	Pervasive control bus slave macro
PCI	Peripheral Component Interconnect. An all-encompassing term referring to conventional PCI, PCI-X, and PCI Express.
PCIEX	Peripheral Component Interface Express
PCIS	The synchronous part of the PCI domain
PCLK	Processor clock
PD	1. Power down 2. Phase detector 3. Presence detect
PDA	Per DRAM addressability
PDR	Power Down Register
PE	1. Parity error 2. Partitionable endpoint. The smallest entity that can be partitioned in endpoint partitioning. 3. Product engineering
PEC	PCI Express controller
PECE	Power-savings exit control enable
PECESR	PECE Sample Register
PERCAL	Periodic calibration
PERV	Pervasive
PF	1. Pad fill keyword 2. Physical function. The physical function of an IOV adapter. For more information, see the PCI-SIG *I/O Virtualization (IOV) Specifications*. 3. Prefetch machine
PFET	Positive field-effect transistor

phase rotator step	Phase rotators are used extensively within the DDR PHY to adjust delays of signals. Each phase rotator has 128 phase-rotator steps in a clock period. Therefore, delay values, or phase-rotator settings, have a granularity of 1/128 of a clock period.
PHB	1. PCIe host bridge. An entity that attaches a PCIe bus to the system. 2. Power Systems host bridge
PHY	Physical layer
PHYP	Power hypervisor
PHYTOP	Physical layer top of hierarchy
PIB	Pervasive interconnect bus. A bus that provides access from masters through external interfaces and internal masters to common PIB attached slaves. The PIB is used for read and full write access.
PIB/LPC	Pervasive interconnect bus/low pin count
PIBMEM	Memory attached to the PIB bus and used by the self-boot engine (SBE)
PID	Process ID
PIG	Programmable interrupt generator
PIN	External C4 chip input pin
PIT	Programmable interval timer
plat	Pipeline staging latch
PLL	Phase-locked loop
PLLREG	Phase-Locked Loop Register
PM	Power management
PMC	1. Performance monitor counter 2. Power management control
PMCR	Power Management Control Register
PMCRS	Power Management Control Register shadow
PMISC	Pervasive miscellaneous
PMU	Performance monitor unit
POR	Power-on reset
port	A memory interface of variable width, consisting of an address/command bus and a data bus, connected to one or more ranks of memory. When multiple ranks are connected to a port, this memory is depth-expanded memory.
PPE	Programmable PowerPC-lite engine
PPM	1. Parts per million 2. PCB-slave power-management component
PPMPIG	PPM programmable interrupt generator
PR	1. Phase rotator 2. Privileged bit in the MSR (MSRPR)

PRBS	Pseudo-random binary sequence
PRD	Processor runtime diagnostic
PRE	Mnemonic for the DDR3 and DDR4 precharge command
PRESP	Processor response
PRPG	Pseudo-random pattern generator
PSC	Parallel-to-serial communication
PSCOM	Parallel-to-serial communication
PSCOMLE	Parallel-to-serial communication light edition
PSCR	Processor Stop Control Register
PSCRS	Processor Stop Control Register shadow
PSI	Processor support interface
PSRO	Performance sort-ring oscillator
PSU	Power supply unit
PUP	Pull-up
PURR	Processor Utilization Resource Register
PVREF	Precision voltage reference
PVT	Process voltage temperature
PVTN	Process voltage temperature N-type field effect transistor
PVTP	Process voltage temperature P-type field effect transistor
PW	Partial write
QACSR	Quad Analog Clock Status Register
QCSR	Quad Configuration Status Register
QFMR	Quad Frequency Measurement Register
QIDSR	Quad/Cache IVRM Dropout Sample Register
QMFR	Quad Frequency Measurement Register
QOS, QoS	Quality of service. This usually relates to a guarantee of minimum bandwidth for streaming applications.
QPMMR	Quad Power Management Mode Register
QPMMR[FSAFE]	A field in the QPMMR register to indicate the safe frequency to drop to in the event a heartbeat is lost.
QPPM	Quad PCB slave power management (cache)
R/W	Read/write
RA	Real address. An address for physical storage, which includes physical memory, local storage, and memory-mapped I/O registers. The maximum size of the real address space is 262 bytes.
RAM	1. Random-access memory 2. Resource allocation management

RAMDBG	A register that provides access to the PPE core's XIR3 debug register
RAMEDR	A register that provides access to the PPE core's XIR4 debug register
RAMGA	A register that provides access to the PPE core's XIR2 debug register
RAMRA	A register that provides access to the PPE core's XIR1 debug register
Rank	One or more memory modules that have a common command/address bus, a common chip select, and separate data bus connections. When more than one memory module exists, this memory is width-expanded memory.
Rank group	Up to four ranks of memory that have nearly identical timing characteristics such that the same DDR PHY delay and configuration values can be used to access all ranks. This configuration allows resources in the DDR PHY to be shared.
RAS	1. Reliability, availability, and serviceability. A combination of design methodologies, system policies, and intrinsic capabilities that, taken together, balance improved hardware availability with the costs required to achieve it. Reliability is the degree to which the hardware remains free of faults. Availability is the ability of the system to continue operating despite predicted or experienced faults. Serviceability is how efficiently and nondisruptively broken hardware can be fixed. 2. Row-address strobe
RASN	Row-address strobe (inverted)
RC	1. Read control 2. Root complex. Connects a PCIe bus into the system.
RCD	Register clock driver
RCD/LRDIM	Register clock driver/load-reduced dual in-line memory module
RCE	Retry CE: A correctable data error (CE) that occurs on the retry of a previous read.
RD	Read
RDATA	Read data
RDCLK	Read clock
RDDACK	Read acknowledgment
RDIMM	Registered dual in-line memory module
RDIV	Reference clock divide
RECR	Read ECC Control Register
REF	Mnemonic used for the DDR3 and DDR4 refresh command.
REFCLK	Reference clock
REG	Register
REGF	Register file
REPR	Array repair
REQ	Request
RFIR	Recoverable FIR

RISC	Reduced instruction set computing
RISCTRACE	A tool used to reconstruct a code flow from a hardware debug trace
RJR	Receiver random jitter
RLDRAM	Reduced latency dynamic random access memory
RLO	Read latency offset
RMW	Read-modify-write
RNG	Random number generator
RO	Read only
ROM	Read-only memory
ROX	Read only but unstable. Can be changed functionally. Hardware can change the value between reads of the register.
RRQ	Read reorder queue
RTL	Register transfer level
RTT	Requester ID (RID) translation table
RTY	Retry
RUN-N, RUNN	Run the engine for N cycles
RUNTIMECTRQ	Runtime counter facility
RW	Readable and writable
RW_WAND	Readable and writable. A write ANDs written data with existing data and stores the result.
RW_WCLEAR	Readable and writable. Any write to the address clears the bits regardless of value.
RW_WOR	Readable and writable. A write ORs written data with existing data and stores the result.
RWITM	Read with intent to modify
RWX	Same as RW, but unstable. Can be changed functionally.
RWX_WAND	Same as RW_WAND, but unstable. Can be changed functionally.
RWX_WCLEAR	Same as RW_WCLEAR, but unstable. Can be changed functionally.
RWX_WCLRPART	Same as RW_WCLRPART, but unstable. Can be changed functionally.
RWX_WOR	Same as RW_WOR, but unstable. Can be changed functionally.
RWX_WSETPART	Same as RW_WSETPART, but unstable. Can be changed functionally.
RX	Receive
RXBIST	Receive built-in self test
RXCTL	Receive control
SAB	Secure access bit
SBASE	SRAM base address in the core management engine (CME), used by the CME block copy engine (BCE)

SBE	1. Self-boot engine. Initializes the processor chip and then loads or invokes the hostboot IPL firmware base image. 2. State bit entry
SC	Store clean (transactional memory value before a speculative store)
SCAN	Refers to shifting groups of latch states internal to a chip to read or write them when functionally not in use.
SCE	Symbol mark corrected error
SCM	Single-chip module
SCOM	Serial communications. SCOM is used for read and full write access.
SCOM1	Serial communications 1. SCOM1 is used for AND write access.
SCOM2	Serial communications 2. SCOM2 is used for OR write access.
SDM	Secure debug mode
SE	1. Scan enable 2. Single-step trace enabled bit in the MSR (MSRSE)
SEC	Single error correction
SEEPROM	Serial electrically erasable programmable read-only memory. An EEPROM memory device that can only be read, but which can be reprogrammed by an external programmer. Note that the hostboot is able to initiate writes to SEEPROMS connected to the circuit board through a serial bus.
SEL	Select
SEQ	Sequencer
SG	Scan gate
SHA	Secure hash algorithm
SIB	Service interface bolt-on. Allows the GPE to communicate with the PIB and the I^2C interface.
SICR	Stop Interface Control Register
Single rank	One rank of memory modules, where all the data bus connections are wired point-to-point to the DDR PHY. The data bus connections include read data, write data, read clocks/strobes, and write clock/strobes.
SIR	Security Isolation Register. Similar to a Fault Isolation Register.
SISR	Stop Interface Status Register
SKEWADJ	Analog clock skew adjust macro
SLB	Segment lookaside buffer. This buffer is used to map an effective address to a virtual address.
SM	State machine
SMDR	Same master rank, different slave rank
SMP	Symmetric multiprocessing
SMT	1. Simultaneous multithreading 2. Surface mount
SN	Snoop machine

SNOE	Scan net optimization enhancement
SNOP	Start sync/wait step; no operation
SOI	Silicon-on-insulator
SP	Service processor
SPATTN	Special attention
SPCIF	Specification
SPI	Serial peripheral interface. Refers to a 4-wire, serial, full-duplex bus with masters and slaves. Commonly used to interface with sensors, control devices, and so on in embedded systems.
SPR	Special-purpose register
SPRD	Special-purpose register data
SPS	1. Steps per sync 2. Sleep Pstate
SPURR	Scaled Processor Utilization Resource Register
SRAM	Static random access memory
SRC	Service reference code
SRQ	Store reorder queue
STEP	Supplier test enablement program
STR	Self time refresh
SUE	Special uncorrectable error
SUE/UE	Special uncorrectable error/uncorrectable error
SW	Software
SYNC	Synchronize
SYS	System
SYSCLK	System clock
TB	Time base
TBD	To be determined
TC	Traffic class. In PCIe, this defines a priority between PCI transactions within a virtual channel (VC).
TCE	1. Translation control entry. Used to translate an I/O address page number to a real page number in system memory. 2. Two-symbol correctable error
TCK	JTAG clock; test clock
TDI	Test data in
TDM	1. Time division multiplexed 2. Time domain multiplexing

TDM command mode	A DDR PHY configuration that supports two ports that share a common address/command bus. The addresses and commands for both ports are time division multiplexed on the common address/command bus. Individual chip selects select which ranks respond to a given address/command. Ranks connected to different ports can be selected to respond to the same command.
TDO	Test data out
TDR	1. Translation control entry (TCE) data random-access memory (RAM) 2. Time-domain reflectometry
TE	Test enable
TFMR	Time Facility Management Register
THD	Thread
TI	Terminate immediately
TID	Thread ID
TLB	Translation lookaside buffer. An on-chip cache that translates virtual addresses (VAs) to real addresses (RAs). A TLB caches page-table entries for the most recently accessed pages, thereby eliminating the necessity to access the page table from memory during load-store operations.
TLBI	Translation lookaside buffer invalidate
TLBIE	Translation lookaside buffer invalidate entry instruction
TM	Transactional memory
TMR	Timer
TMS	Test mode select
TOD	Time of day
TPM	1. Top of peripheral memory 2. Trusted platform module
TPMD	Trusted platform module
tREFI	Refresh interval
TSV	Trans silicon via
TWSM	Table walk state machine
TX	Transmit
TXBIST	Transmit built-in self test
TXCTL	Transmit control
TZ	Tile zone
UDE	Unconditional debug event
UE	Uncorrectable error
UI	1. User interface 2. Unit interval
UL	Uplink
ULCCH	Uplink control channel

ULDCH	Uplink data channel
UMAC	User-mode access control
VAS	Virtual accelerator switchboard
VC	Virtual channel
VCC	Voltage supply
VCO	Voltage controlled oscillator
VCTR	VDM Count Threshold Register
VDCR	VDM Droop Count Register
VDM	Voltage droop monitor
VDSR	VDM Data Sample Register
VECR	VDM Event Count Register
VGA	1. Variable gain amplifier 2. Video graphics array
VHDL	VHSIC hardware description language
VHSIC	Very high speed integrated circuit
VID	Voltage identification
VIO	Voltage I/O
VITL	Vital
VMEAS	Voltage measurement
VMX	Vector multimedia extension
VNCR	VDM Non-Droop Count Register
VPAD	Pad voltage
VPROTH	Voltage protect high
VREF	Voltage reference
VREG	1. Voltage regulator 2. Voltage regulation
VRM	Voltage regulator module
VSU	Vector scalar unit
VT	Voltage control
WAT	Workaround macro
WC	1. Worst case 2. Write control
Wdata, WDATA	Write data
WDF	Designator for the memory controller's read-modify-write data flow and associated control.
WDFCFG	Configuration facilities for the WDF logic.

WECR	Write ECC Control Register
WEN	Write enable
WLO	Write latency offset
WO	Write only
WO_1P	Write only; one pulse length is equal to one register cycle.
WO_AND	Same as RW_WAND, but the bits are write-only.
WO_CLEAR	Same as RW_WCLEAR, but the bits are write-only.
WO_CLRPART	Same as RW_WCLRPART, but the bits are write-only.
WO_n_mP	Write only pulsed. A write of ‘1’ creates a pulse for a minimum of n register clocks and a maximum of m register clocks. A read returns ‘0’.
WO_nP	Write only pulsed. A write of ‘1’ creates a pulse for n register clocks. A read returns ‘0’.
WO_OR	Same as RW_WOR, but the bits are write-only.
WO_SETPART	Same as RW_WSETPART, but the bits are write-only.
WOF	1. Who's on first? 2. Workload optimized frequency
WOX_AND	Same as WO_AND, but unstable. Can be changed functionally.
WOX_CLEAR	Same as WO_CLEAR, but unstable. Can be changed functionally.
WOX_CLRPART	Same as WO_CLRPART, but unstable. Can be changed functionally.
WOX_n_mP	Same as WO_n_mP, but unstable. Can be changed functionally.
WOX_nP	Same as WO_nP, but unstable. Can be changed functionally.
WOX_OR	Same as WO_OR, but unstable. Can be changed functionally.
WOX_SETPART	Same as WO_SETPART, but unstable. Can be changed functionally.
WR	Write
WRCNTL	Write control
WRD	Write data. Designator for the portion of the memory controller's write data flow that generates the outbound memory ECC check bits.
WRQ	Write reorder queue
WRT	Designator for the memory controller's write data flow.
WRTCFG	Configuration facilities for the memory controller's WRT logic.
XBUS	Note: This is not really an acronym but a name (X bus).
XCR	External Control Register
XER	Fixed-Point Exception Register
XFIR	X Fault Isolation Register
XIR	1. External Interface Register 2. External interface to the PPE IR Register

XIVR	External Interrupt Vector Register for the OCC (405)
XOR	Exclusive OR
XSCOM	Extended SCOM. Special, fast SCOM that allows the processor cores to directly SCOM the PIB. Processor buses must be enabled to the slave processor chips for the master processor to XSCOM them.
XSR	External Status Register for PPE
XSTOP	Checkstop
ZCAL	Impedance (Z) calibration
ZCNTLCPURO	Periodic impedance (Z) calibration
ZCONTROL	Impedance (Z) control
ZQ	I/O impedance
ZQCal	I/O impedance calibration

1. POWER9 Processor Overview

The POWER9 processor is a superscalar symmetric multiprocessor designed for use in servers and large-cluster systems. It uses 14 nm technology with 17 metal layers. The POWER9 processor can have up to 24 cores enabled on a single chip. It supports direct-attach memory. It supports a maximum symmetric multiprocessing (SMP) size of two sockets and is targeted for scale-out workloads. Each POWER9 core supports up to four threads using simultaneous multithreading (SMT). The SMT can be dynamically tuned so that each core has one, two, or four threads

This document describes the POWER9 registers and related accessing method.

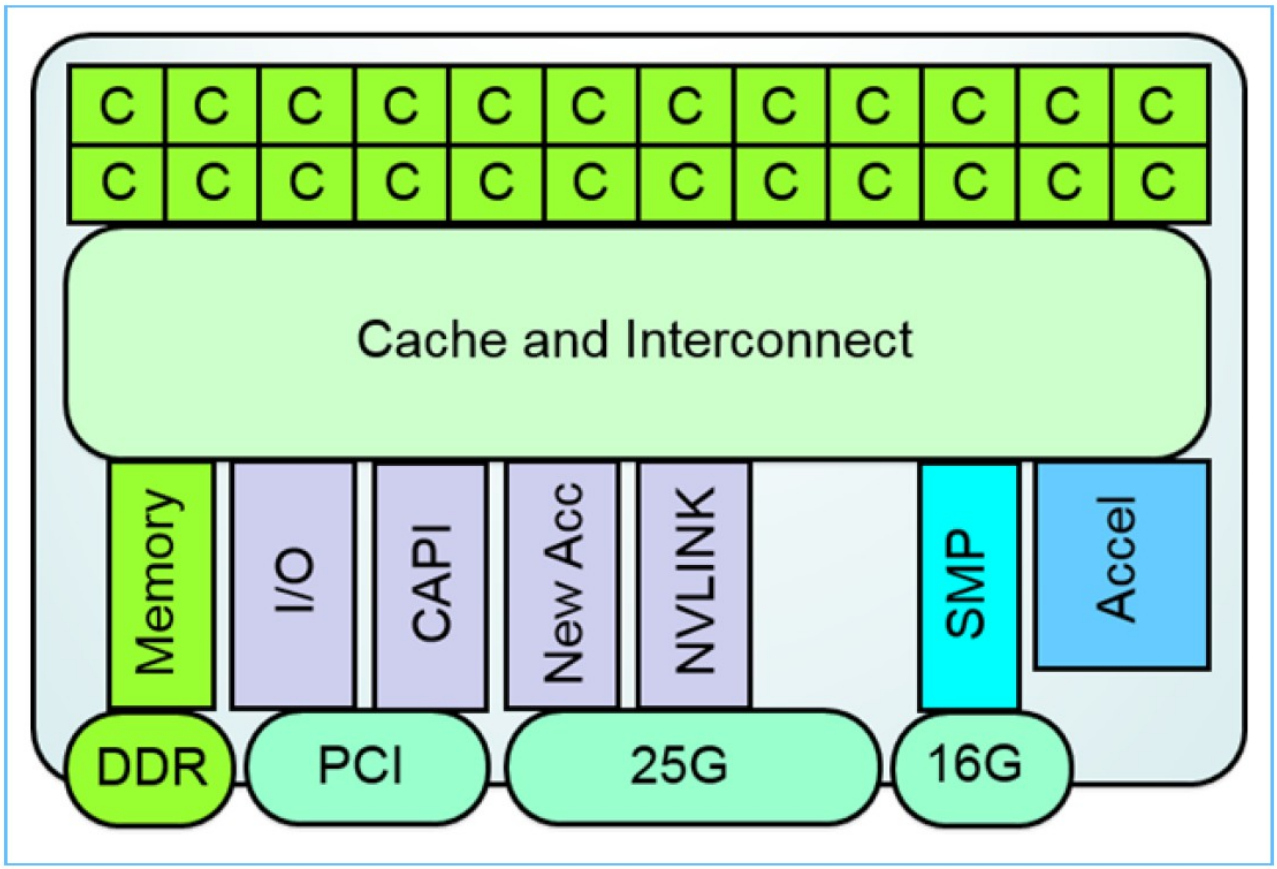
1.1 POWER9 Processor Features

Figure 1 on page 35 shows the POWER9 processor, which supports the following features:

- Twenty-four POWER9 chiplets, which contain one POWER9 core, an L2 cache, and an L3 cache.
- On-chip accelerators.
  - Coherent Accelerator Processor Interface (CAPI), which enables an FPGA or ASIC to connect coherently to the POWER9 processor SMP interconnect via the PCIe bus.
  - On-chip compression, encryption, and data movement initiated by the hypervisor, GZIP engine, or nest MMU to enable user access to all accelerators.
  - In-core user invocation of encryption using the Advanced Encryption Standard (AES) and the secure hash algorithm (SHA).
- Two memory controllers that support direct-attached DDR4 memory:
  - Support four direct-attach memory buses (DDR 0, 1, 6, and 7).
  - Support ×4 and ×8, 4 - 16 Gb DRAMs and 3D stacked DRAMs.

    - Support registered dual in-line memory modules (RDIMMs) and load-reduced dual in-line memory modules (LRDIMMs).
- Processor SMP interconnect.
    - Supports one inter-node SMP X bus link.
    - Maximum two-socket SMP.
- Three PCIe controllers (PEC) with 16 lanes of PCI Express Gen 4 I/O.
    - PEC0: one ×16 lanes.
    - PEC1: two ×8 lanes (bifurcation).
    - PEC2: one ×16 lane mode, two ×8 lanes (bifurcation), or one ×8 lane and two ×4 lanes (trifurcation).
    - PEC0 and PEC2 support CAPI 2.0.
- Power management.
- Pervasive interface.

Figure 1: POWER9 Processor General Diagram



1.2 POWER9 Processor Pervasive Structure

Figure 2 on page 36 shows the POWER9 chip from a pervasive-centric point of view. The different colors denote different chiplets from a pervasive perspective. Each chiplet consists of one global clock controller and multiple local clock controllers, which enable a chiplet to service multiple different clock regions. Multiple clock regions can run at the same frequency, but can be turned off independently. The chip contains 24 cores capable of running at different frequencies. The pervasive logic supports these 24 cores.

Figure 2: POWER9 Processor from a Pervasive Point of View

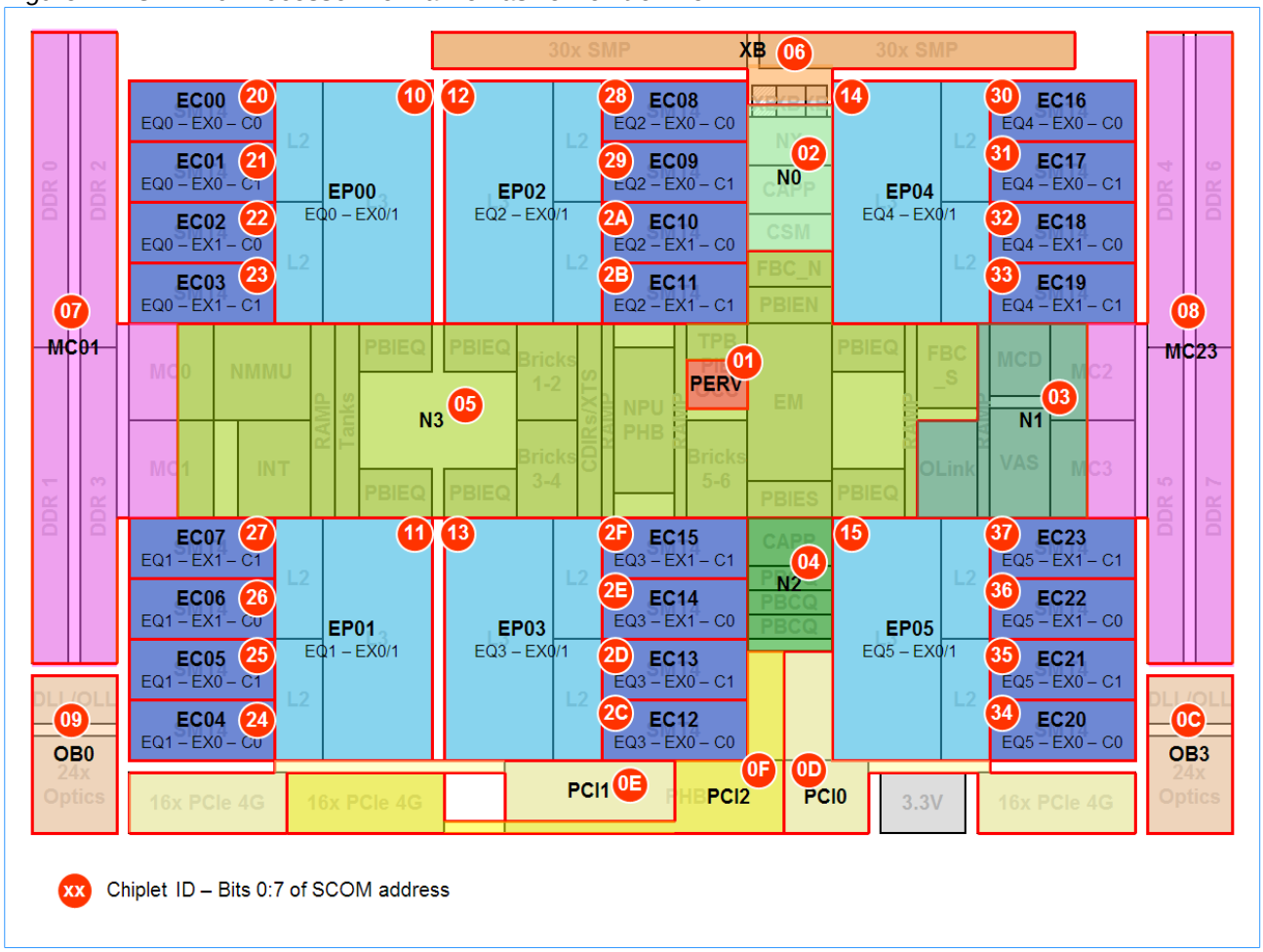
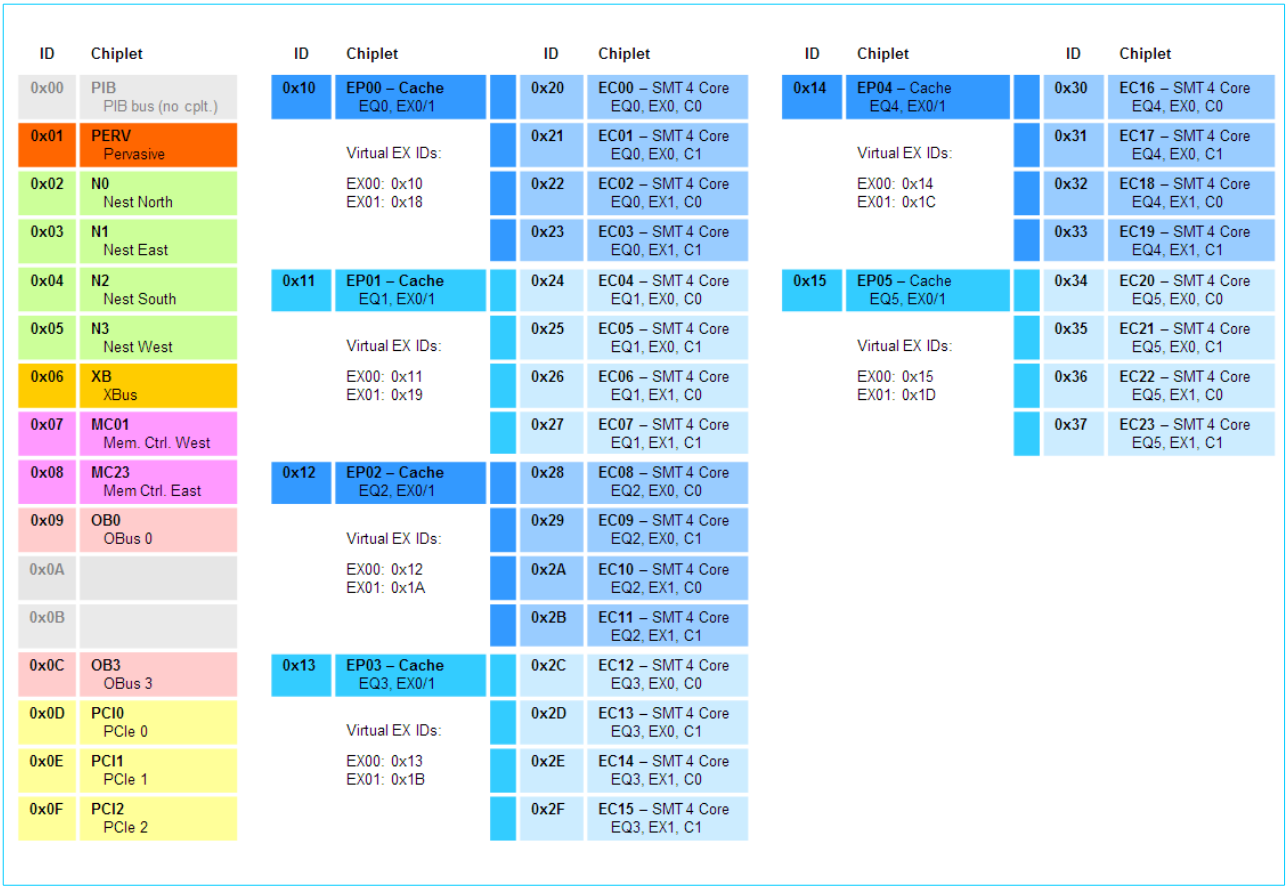


Figure 3 on page 37 lists the chiplets in the design, and their controlling pervasive blocks, by chiplet ID.

Figure 3 POWER9 Chiplets and IDs



ID	Chiplet
0x00	PIB PIB bus (no cplt.)
0x01	PERV Pervasive
0x02	N0 Nest North
0x03	N1 Nest East
0x04	N2 Nest South
0x05	N3 Nest West
0x06	XB XBus
0x07	MC01 Mem. Ctrl. West
0x08	MC23 Mem Ctrl. East
0x09	OB0 OBus 0
0x0A	
0x0B	
0x0C	OB3 OBus 3
0x0D	PCI0 PCIe 0
0x0E	PCI1 PCIe 1
0x0F	PCI2 PCIe 2

ID	Chiplet	ID	Chiplet
0x10	EP00 – Cache EQ0, EX0/1	0x20	EC00 – SMT 4 Core EQ0, EX0, C0
	Virtual EX IDs: EX00: 0x10 EX01: 0x18	0x21	EC01 – SMT 4 Core EQ0, EX0, C1
		0x22	EC02 – SMT 4 Core EQ0, EX1, C0
		0x23	EC03 – SMT 4 Core EQ0, EX1, C1
0x11	EP01 – Cache EQ1, EX0/1	0x24	EC04 – SMT 4 Core EQ1, EX0, C0
	Virtual EX IDs: EX00: 0x11 EX01: 0x19	0x25	EC05 – SMT 4 Core EQ1, EX0, C1
		0x26	EC06 – SMT 4 Core EQ1, EX1, C0
		0x27	EC07 – SMT 4 Core EQ1, EX1, C1
0x12	EP02 – Cache EQ2, EX0/1	0x28	EC08 – SMT 4 Core EQ2, EX0, C0
	Virtual EX IDs: EX00: 0x12 EX01: 0x1A	0x29	EC09 – SMT 4 Core EQ2, EX0, C1
		0x2A	EC10 – SMT 4 Core EQ2, EX1, C0
		0x2B	EC11 – SMT 4 Core EQ2, EX1, C1
0x13	EP03 – Cache EQ3, EX0/1	0x2C	EC12 – SMT 4 Core EQ3, EX0, C0
	Virtual EX IDs: EX00: 0x13 EX01: 0x1B	0x2D	EC13 – SMT 4 Core EQ3, EX0, C1
		0x2E	EC14 – SMT 4 Core EQ3, EX1, C0
		0x2F	EC15 – SMT 4 Core EQ3, EX1, C1

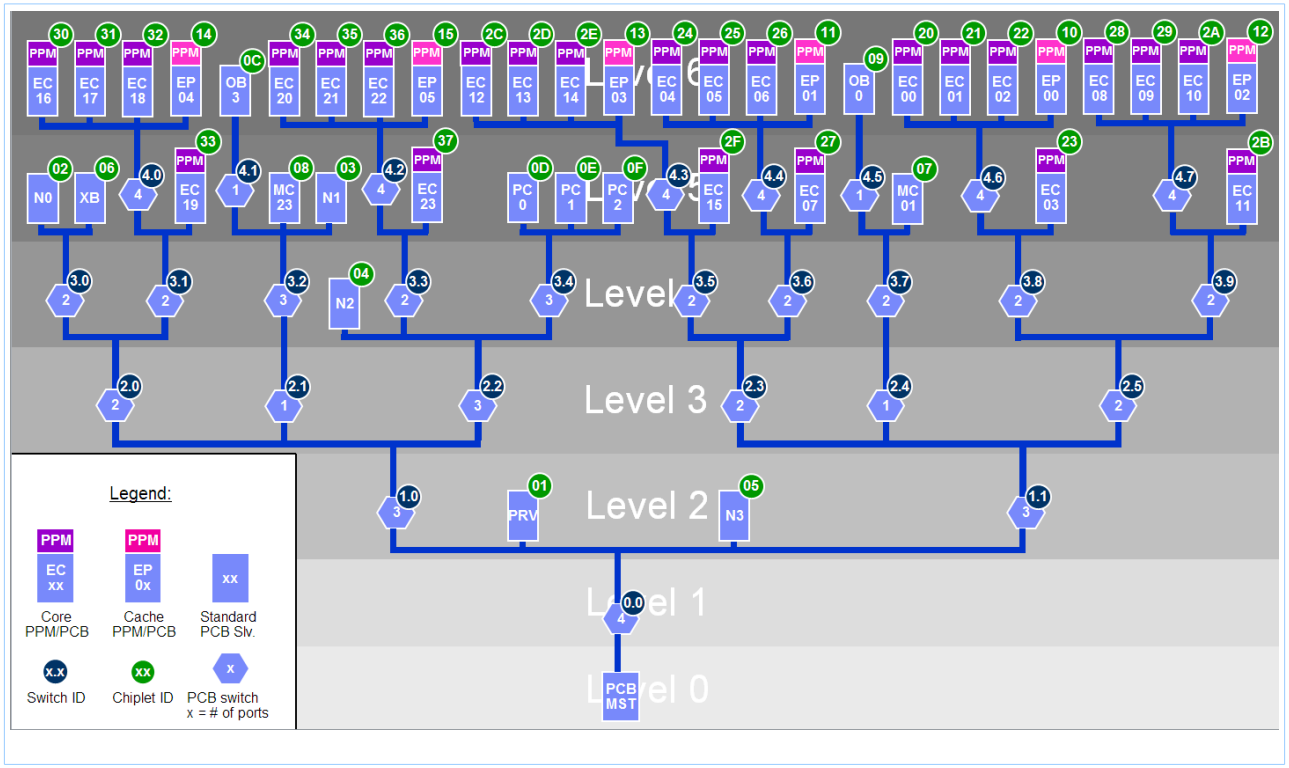
ID	Chiplet	ID	Chiplet
0x14	EP04 – Cache EQ4, EX0/1	0x30	EC16 – SMT 4 Core EQ4, EX0, C0
	Virtual EX IDs: EX00: 0x14 EX01: 0x1C	0x31	EC17 – SMT 4 Core EQ4, EX0, C1
		0x32	EC18 – SMT 4 Core EQ4, EX1, C0
		0x33	EC19 – SMT 4 Core EQ4, EX1, C1
0x15	EP05 – Cache EQ5, EX0/1	0x34	EC20 – SMT 4 Core EQ5, EX0, C0
	Virtual EX IDs: EX00: 0x15 EX01: 0x1D	0x35	EC21 – SMT 4 Core EQ5, EX0, C1
		0x36	EC22 – SMT 4 Core EQ5, EX1, C0
		0x37	EC23 – SMT 4 Core EQ5, EX1, C1

1.2.1 Pervasive Control Bus and Pervasive Interconnect Bus

The pervasive control bus (PCB) provides a generic, modular structure for communication between the pervasive elements. The PCB provides the POWER9 pervasive unit with an interface to the pervasive functions on the various POWER9 processor chiplets. For this purpose, a PCB master is implemented inside the POWER9 pervasive logic. This master, by means of the PCB interconnect, communicates with the PCB slave located in each chiplet. The PCB master sends commands, such as read and write requests, to the PCB slaves. The slaves, on the other hand, respond to the commands received from the master, and also notify the master of interrupts that occur in the slave's chiplet.

Figure 4 on page 38 shows the PCB structure that services all the chiplets.

Figure 4: Pervasive Control Bus Structure and Chiplets



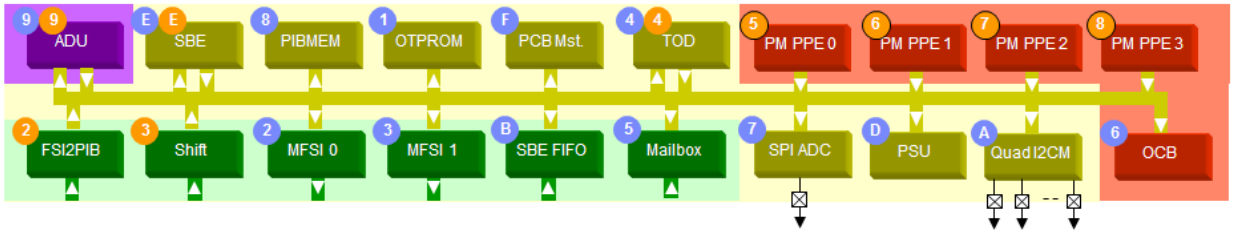
The PCB switch features two independent channels for the PCB topology. The downstream input channel provides a fan-out to the downstream output ports, which are connected either to another switch in a multistage topology or directly to a slave. The upstream output channel is arbitrated between requests from the upstream input ports, which is the case when replying to a multicast operation.

The pervasive interconnect bus (PIB) provides access from the masters via the external interfaces and the internal masters to the common PIB-attached slaves. *Figure 5* on page 39 shows the PIB masters and slaves.

- The external interfaces include the I²C slave and the flexible service interface (FSI).
- The internal masters include the FSI shift engine, FSI2PIB, and the XSCOM/alter-display unit (ADU).
- The PIB-attached slaves include the PCB master, PIB2OPB, general-purpose register (GPR), I²C master, and the I²C slave.

The PIB facilitates transactions between multiple PIB masters and multiple PIB slaves. For each transaction, the PIB arbiter establishes a point-to-point connection between a single requesting master and a single slave uniquely addressed by the master.

Figure 5: PIB Masters and Slaves



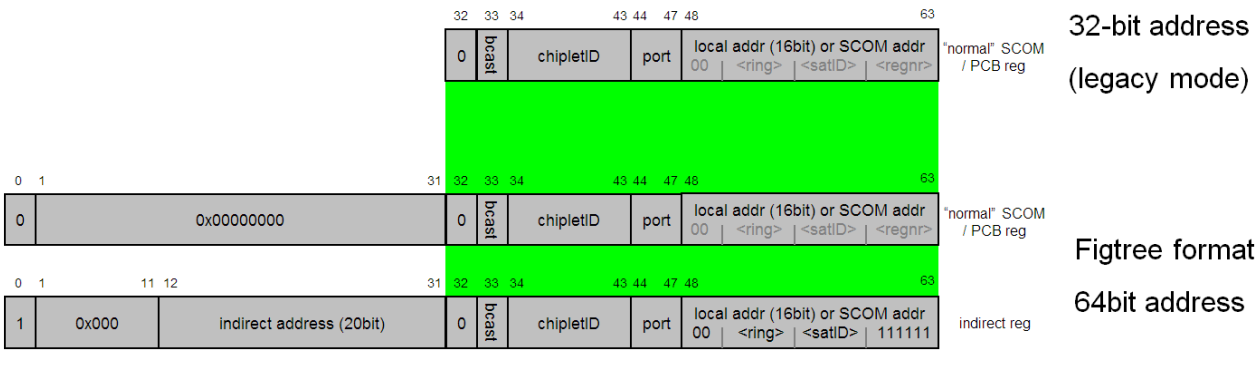
- Pervasive Interconnect Bus (PIB):
  - 9 PIB master (2x CFAM, 4x OCC, 1x Bridge, 2x PIB domain)
  - 13 PIB slaves (4x CFAM, 1x OCC, 1x Bridge, 7x PIB domain)
- Pervasive Connect Bus (PCB):
  - Root in PIB (PCB Master)
  - Provides tree-like switch network to all chiplets
  - 30 Chiplets defined as of now
- PIB & PCB domain run at 465 - 600 MHz (Nest Clock 4:1)
- PIB & PCB domain get initialized (scan0 & clock start) by the pervasive clock controller which is controlled by the new *CFAM Boot Sequencer* (CBS)
- PIB & PCB are trusted domains – no direct access from Service Elements (FSP/BMC) in secured chips

ID #	Master	Domain	Slave	Domain
0x0	LBUS		LBUS	
0x1	free		OTPROM	pib
0x2	FSI2PIB	cfam	FSI Master 0	cfam
0x3	FSISHIFT	cfam	FSI Master 1	cfam
0x4	TOD	pib	TOD	pib
0x5	PM PPE 0	occ	FSI Mailbox	cfam
0x6	PM PPE 1	occ	OCI Bridge	occ
0x7	PM PPE 2	occ	SPI ADC	pib
0x8	PM PPE 3	occ	PIBMEM	pib
0x9	ADU	bridge	ADU	bridge
0xA	free		I2C master	pib
0xB	free		SBE FIFO	cfam
0xC	free		free	
0xD	free		PSU	pib
0xE	SBE	pib	SBE	pib
0xF	CME		PCB Master	pib

1.2.2 PCB Address Space

Figure 6 shows the address format used to access all pervasive facilities. The legacy 32-bit format is shown as well as the translation in the 64-bit format (add 32 zeros as the most-significant bits). The new extended address format that enables access to the large address SCOM satellites (up to 31 bits) is also listed. The most significant bit is '1' in that case.

Figure 6: Common Pervasive Address Map Format

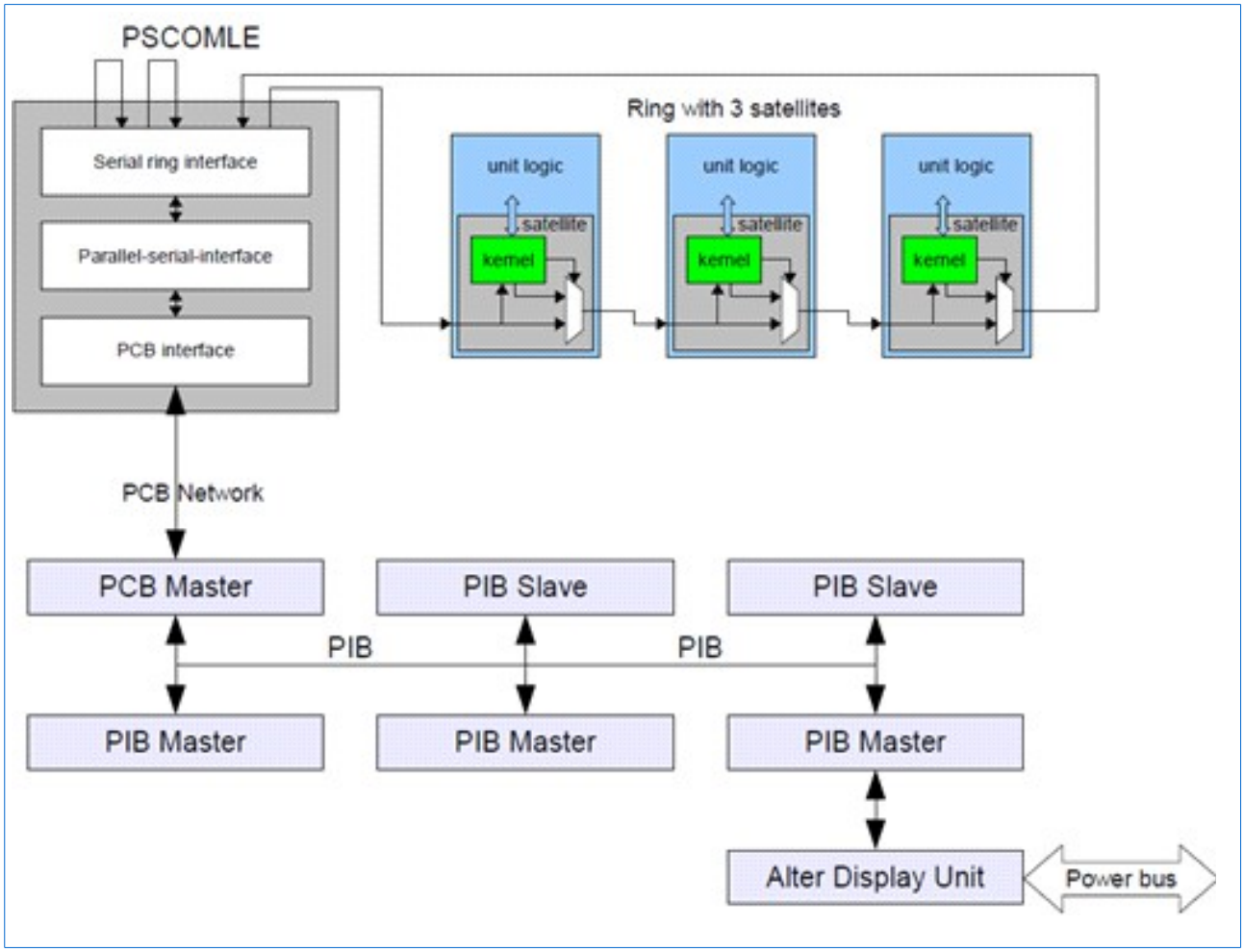


1.2.3 SCOM

SCOM provides a serial communication infrastructure within the pervasive infrastructure. The central control unit is referred to as the parallel-to-serial communication light edition (PSCOMLE). It controls all communication with respect to the serial interface. The end-point nodes are referred to as satellites. A satellite is located in the unit logic. The satellites are connected to the PSCOMLE and each other in a physical ring. The PSCOMLE can support up to 15 rings. Each ring has a local address space that is used to address an individual satellite in a given ring and within the unit logic that uses the satellite with a dedicated register. If this address space is not sufficient, an indirect address can be used to further extend the address range within a satellite.

Figure 7 shows the principal pervasive infrastructure to access the SCOM-enabled registers in a chiplet. A SCOM access can be initiated from the masters connected to the PIB, such as the ADU. SCOM satellites are distributed inside the chiplet and are organized in serial SCOM rings. For each chiplet, there is one instance of the PSCOMLE macro that receives the request from the PCB network.

Figure 7: Infrastructure to Access SCOM Registers

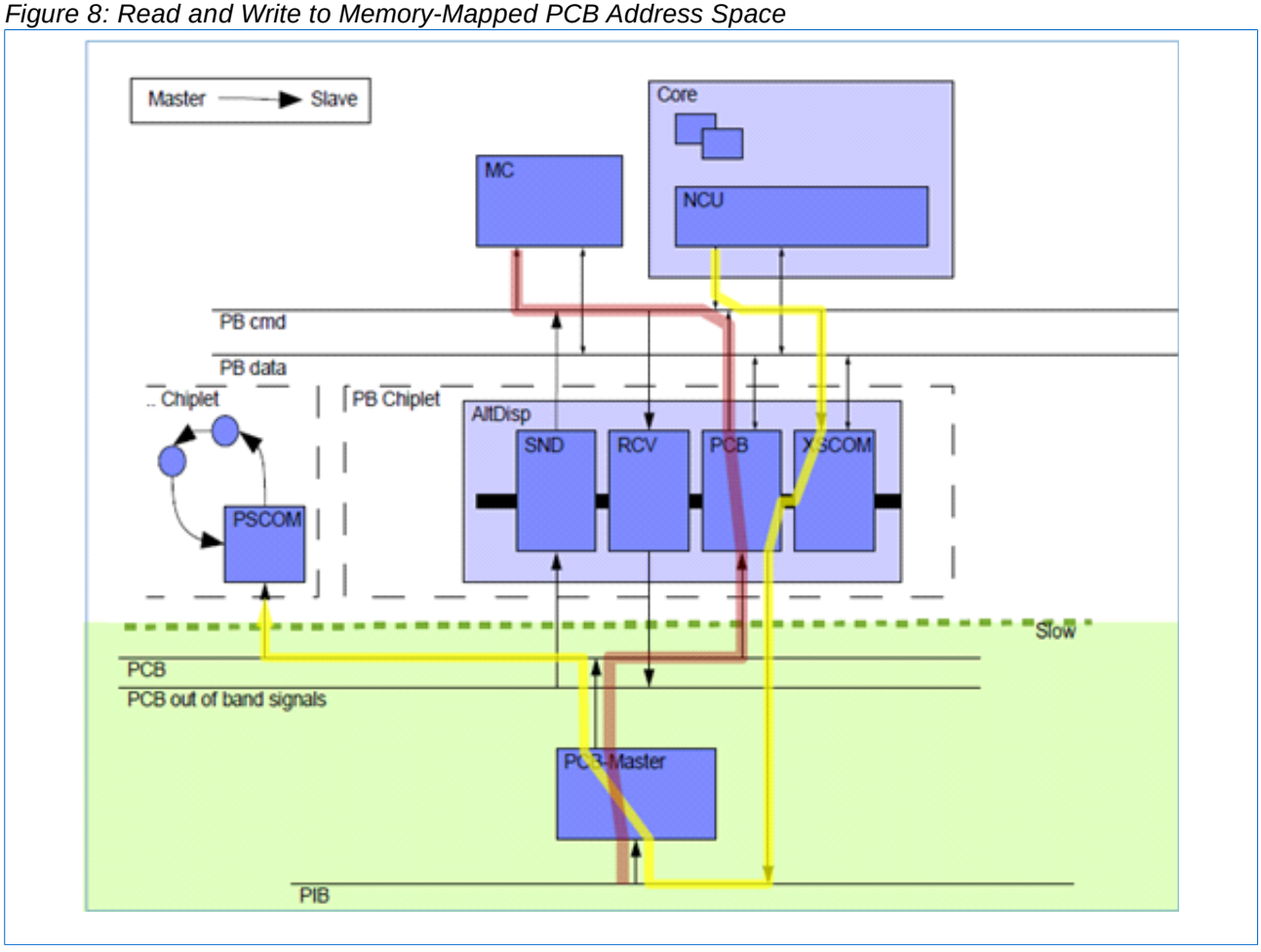


1.2.4 XSCOM

The alter/display unit (ADU) acts as a bridge between the processor bus and the PCB. The ADU enables access to any memory-mapped PIB/PCB register in the system by external SCOM (XSCOM.) The XSCOM is responsible for handling memory-mapped PIB/PCB register access, which originates from the non-pervasive logic of the processor. For example, a read/write operation can originate from a processor core and is presented on the processor bus by the non-cacheable unit (NCU). The alter/display unit XSCOM routes the request through a PIB master to the PIB. The PIB master notifies the ADU when it is complete. For a read operation, the ADU routes the resulting data to the processor bus, which sends the information back to the requester (in the example, the NCU). It then arrives at the core. The XSCOM memory-mapped address range, by default, locates at 0x0003FC0000000000.

Figure 8 shows an example of a read and write to a memory-mapped PCB address space.

Figure 8: Read and Write to Memory-Mapped PCB Address Space



1.3 Register Accessing Type

A register can have multiple addresses, with a different address for different chiplets. The types of access permitted can vary by chiplets. *Table 1* on page 42 summarizes the valid register access types.

Table 1: Register Access Types

Access Type	Description
NC	Not connected; the data cannot be written or read by that access.
NCX	Same as NC, but unstable. Can be changed functionally.
RO	Read only. Only to be used if a bit is tied. Status bits should be ROX.
ROX	Same as RO, but unstable. Can be changed functionally.
ROX_CLRPART	Same as ROX, but a read access clears the bits after they have been accessed.
RW	Readable and writable.
RW_WAND	Readable and writable. A write ANDs written data with existing data and stores the result.
RW_WCLEAR	Readable and writable. A write of a '1' clears the bit. A write of a '0' does nothing.
RW_WCLRPART	Readable and writable. Any write to the address clears the bits regardless of the value.
RW_WOR	Readable and writable. A write ORs written data with existing data and stores the result.
RW_WSETPART	Readable and writable. Any write to the address sets the bits regardless of the value.
RWX	Same as RW, but unstable. Can be changed functionally.
RWX_WAND	Same as RW_WAND, but unstable. Can be changed functionally.
RWX_WCLEAR	Same as RW_WCLEAR, but unstable. Can be changed functionally.
RWX_WCLRPART	Same as RW_WCLRPART, but unstable. Can be changed functionally.
RWX_WOR	Same as RW_WOR, but unstable. Can be changed functionally.
RWX_WSETPART	Same as RW_WSETPART, but unstable. Can be changed functionally.
WO	Same as RW, but bits are write-only.
WO_1P	Write only; one pulse length is equal to one register cycle.
WO_AND	Same as RW_WAND, but bits are write-only.
WO_CLEAR	Same as RW_WCLEAR, but bits are write-only.
WO_CLRPART	Same as RW_WCLRPART, but bits are write-only.
WO_n_mP	Write-only pulsed. A write of '1' creates a pulse for a minimum of n register clocks and a maximum of m register clocks. A read returns '0'.
WO_nP	Write-only pulsed. A write of '1' creates a pulse for n register clocks. A read returns '0'.
WO_OR	Same as RW_WOR, but bits are write-only.
WO_SETPART	Same as RW_WSETPART, but bits are write-only.
WOX	Same as WO, but unstable. Can be changed functionally.
WOX_AND	Same as WO_AND, but unstable. Can be changed functionally.
WOX_CLEAR	Same as WO_CLEAR, but unstable. Can be changed functionally.
WOX_CLRPART	Same as WO_CLRPART, but unstable. Can be changed functionally.
WOX_n_mP	Same as WO_n_mP, but unstable. Can be changed functionally.

Access Type	Description
WOX_nP	Same as WO_nP, but unstable. Can be changed functionally.
WOX_OR	Same as WO_OR, but unstable. Can be changed functionally.
WOX_SETPART	Same as WO_SETPART, but unstable. Can be changed functionally.

2. POWER9 Memory Controller Overview

The POWER9 memory controller unit (MCU) provides the system memory interface between the on-chip simultaneous multiprocessing (SMP) interconnect fabric and the double data rate (DDR) physical layer (PHY) unit. The DDR PHY connects directly to industry-standard (IS) memory DDR4 dual in-line memory modules (DIMMs).

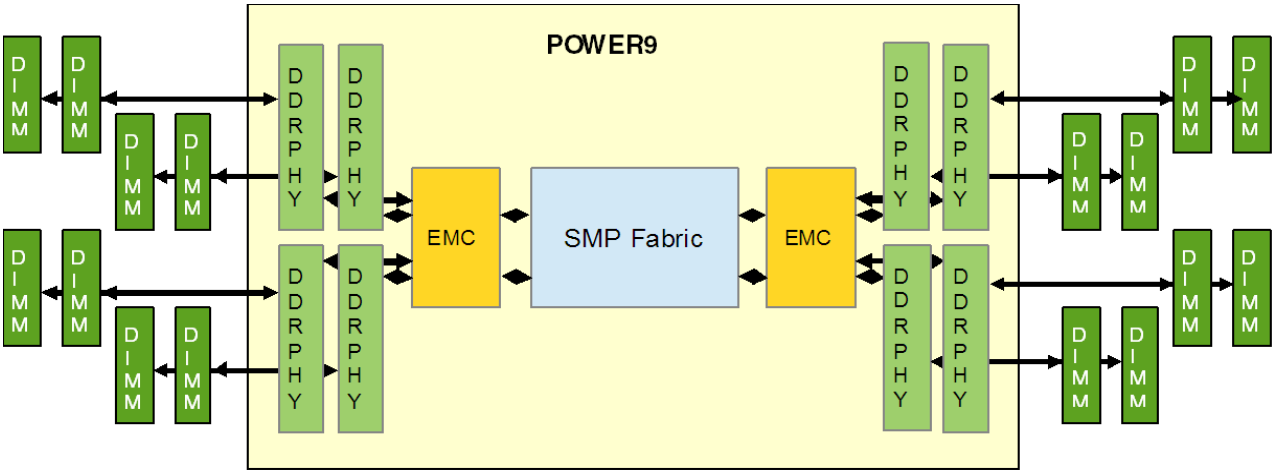
The MCU acts as a slave only. It does not source any commands to the SMP fabric. There are logically eight, essentially independent, MCUs on the chip interfacing to eight, 9-byte wide, DDR4 JEDEC-standard memory buses. As shown in *Figure 9*, each memory channel (or “port”) supports up to two DDR4 DIMM slots. Physically, the MCUs are grouped into two instances of an extended memory controller (EMC) chiplet. Each EMC chiplet contains four MCUs. The EMC is simply a physical level of hierarchy on the chip that contains the MCU plus pervasive logic. The MCUs process is as follows:

- 64-byte and 128-byte read and write requests from processor cores and I/O host bridges
- 1 - 128-byte partial-line writes
- Atomic memory operations (AMOs)

They also handle address-only operations for address protection, acting as the lowest-point of coherency (LPC). While executing these operations, the MCU is also managing DRAM memory refresh and DRAM power states. The MCU also communicates with the DDR PHY to initiate periodic memory bus calibration sequences.

The eight MCUs on the chip can be configured into one or more address-interleave groups. Within each group, the address space is divided into portions, such that each sequential cache line is handled by a different MCU in a round-robin fashion. The maximum memory addressing capability per interleave group is 4 TB. The maximum memory addressing per POWER9 chip is 8 TB.

Figure 9. POWER9 Memory System



For more information about the MCU and the SMP interconnect, see the *POWER9 Processor User's Manual*.

2.1 DDR PHY Unit

At a high level, the DDR PHY unit is responsible for:

- Transporting and mapping command, control, address, and data signals presented from the embedded memory controller.
- Providing all necessary configuration registers, state machines, control logic, and status monitoring to execute all required DDR calibration functions, such as read calibration, fine and coarse write leveling, and I/O impedance (ZQ) calibration.
- Providing elastic-interface-style FIFOs (PHYs) for sampling, deskewing, and bit aligning incoming data, as well as buffering and launching outgoing data. These FIFOs also assist in crossing clock domains.

Each DDR PHY unit is self-contained and comprises four independent ports that connect to the DIMM slots. This unit is replicated twice on the POWER9 processor to provide a maximum of eight ports. As described in *Representation of Enumerated Registers* on page 8, all instances of each DP16 register are documented in one replication.

The DDR PHY unit supports the following memory devices on each port:

- DDR4 registered dual in-line memory modules (RDIMMs) and DDR4 load-reduced dual in-line memory modules (LRDIMMs), including 3D stacks up to eight high
- DRAM data widths of ×4 and ×8
- DRAM densities of 4, 8, 12, and 16 Gb
- One or two DIMMs per port (DPC)
- DRAM speeds of 1867, 2133, 2400, and 2667 Mbps

To accommodate DRAM timing variability and the POWER9 process, voltage, and temperature corners; the DDR PHY unit implements the following calibration sequences:

- Write leveling
- Data strobe (DQS) alignment
- Read clock alignment
- Read centering
- Write centering
- Coarse write alignment
- Coarse read alignment
- Transmit output impedance calibration

To accommodate voltage and temperature drifts; DQS alignment, read clock alignment, and read centering can be run periodically after the initial calibrations.

The DDR PHY unit on the POWER9 processor supports two ranks per DIMM, and enables rank switching in three memory clock cycles or fewer, depending on the speed of operation and device type. The maximum DDR PHY read latency is five memory cycles.

To support DDR4 JEDEC specifications above speeds of 2400 Mbps, the following features are supported:

- Programmable preamble
- Cyclic redundancy check (CRC) support for writes
- Receive V_{REF} calibration

Other features include:

- Per-buffer addressability (PBA) mode
- Per-DRAM addressability (PDA) mode
- DDR4 maximum power-saving mode
- Per-bit tuning on all address, command, control, clock, data, and strobe signals
- Programmable output impedance
- Rank grouping feature
- Extensive RAS support
- Power-down modes
- Custom calibration modes to support custom calibration patterns

2.1.1 Operation

The DDR PHY unit must support all mainline functions initiated by the POWER9 memory controller. These include:

- Clock enable (CKE) controls for power down and powering up ranks, as well as entering and exiting self-refresh mode.
- Bank activate commands
- Burst length 8 and burst chop 4 read and write operations
- Periodic refreshes

The memory controller (MC) must ensure proper spacing and timing of all command, control, and data signals, and adherence to the JEDEC specifications. The primary responsibility of the DDR unit is to propagate all command, address, data, and control signals from the MC unit to and from the DRAM devices. Communication between the memory buffer asynchronous (MBA) and DDR units is accomplished by using an internal bus. The command, control, and address bits flow through a unidirectional ADR43 unit in each DDR PHY port, which can drive up to 43 interface pins. Data is transceived through four bidirectional DP16 units and one DP8 unit in each DDR PHY port, which can accommodate 72 bits (9 bytes) per port.

2.1.2 Configuration Requirements

The DDR PHY core has the following feature and protocol requirements for configuration:

- Either ×4 or ×8 devices are supported.
- The minimum supported burst length is 42.
- Ranks in a rank group must be identical in timing, speed grade, and configuration.
- Data pins and data mask pins (if used) must be common to all ranks.
- Address and control signals must be common to all ranks except chip selects and replicated signals (typically clocks).
- The memory space must consist of sixteen consecutive address locations, in every memory module, in each primary rank to be reserved exclusively for the DDR PHY core. This memory space is used to write and read patterns to perform the initialization and runtime calibrations. Memory space in each bank group must be reserved.
- In systems with multiple ranks, the programmed write latency of all ranks must be equal, and the programmed read latency of all ranks must be equal.
- Before calibration, the BL field in the PC Mode Register MR0 must be set to BL8 or OTF (not BC4).

2.2 Memory Address Space

The POWER9 memory address space consists of the following regions:

- Memory Registers.
- Memory Pervasive Control Bus (PCB) Slave Registers.

- DDRPHY: ADR Registers. These address (ADR) registers are specific to each address/command lane of one of the 12 or 8 lane groups, supporting lanes 0:11, 12:23, 24:35, and 36:43.
- DDRPHY: APB Registers. These advanced peripheral bus (ADP) registers are common to address/command lane groups 0:23 or 24:43.
- DDRPHY: PC Registers. These are the PHY control (PC) registers.
- DDRPHY: RC Registers. These are the read control (RC) registers.
- DDRPHY: SEQ Registers. These are the sequencer (SEQ) registers.
- DDRPHY: WC Registers. These are the write control (WC) registers.
- DDRPHY: DP16 Registers. These are data path 16 (DP16) registers. Each instance 0:3 supports 16 DQs; instance 4 supports eight DQs, for a total of 72 DQs.

3. Memory Registers

The memory registers are listed alphabetically by mnemonic in the following address table.

Mnemonic	Address	Page
MC01.MCBIST.CCS.CCS_INST_ARR0_18	0x0000000007012327	345
MC01.MCBIST.CCS.CCS_INST_ARR0_19	0x0000000007012328	346
MC01.MCBIST.CCS.CCS_INST_ARR0_20	0x0000000007012329	348
MC01.MCBIST.CCS.CCS_INST_ARR0_21	0x000000000701232A	349
MC01.MCBIST.CCS.CCS_INST_ARR0_22	0x000000000701232B	351
MC01.MCBIST.CCS.CCS_INST_ARR0_23	0x000000000701232C	352
MC01.MCBIST.CCS.CCS_INST_ARR0_24	0x000000000701232D	354
MC01.MCBIST.CCS.CCS_INST_ARR0_25	0x000000000701232E	355
MC01.MCBIST.CCS.CCS_INST_ARR0_26	0x000000000701232F	357
MC01.MCBIST.CCS.CCS_INST_ARR0_27	0x0000000007012330	358
MC01.MCBIST.CCS.CCS_INST_ARR0_28	0x0000000007012331	360
MC01.MCBIST.CCS.CCS_INST_ARR0_29	0x0000000007012332	361
MC01.MCBIST.CCS.CCS_INST_ARR0_30	0x0000000007012333	363
MC01.MCBIST.CCS.CCS_INST_ARR0_31	0x0000000007012334	364
MC01.MCBIST.CCS.CCS_INST_ARR1_00	0x0000000007012335	366
MC01.MCBIST.CCS.CCS_INST_ARR1_01	0x0000000007012336	366
MC01.MCBIST.CCS.CCS_INST_ARR1_02	0x0000000007012337	366
MC01.MCBIST.CCS.CCS_INST_ARR1_03	0x0000000007012338	367
MC01.MCBIST.CCS.CCS_INST_ARR1_04	0x0000000007012339	367
MC01.MCBIST.CCS.CCS_INST_ARR1_05	0x000000000701233A	368
MC01.MCBIST.CCS.CCS_INST_ARR1_06	0x000000000701233B	368
MC01.MCBIST.CCS.CCS_INST_ARR1_07	0x000000000701233C	369
MC01.MCBIST.CCS.CCS_INST_ARR1_08	0x000000000701233D	369
MC01.MCBIST.CCS.CCS_INST_ARR1_09	0x000000000701233E	370
MC01.MCBIST.CCS.CCS_INST_ARR1_10	0x000000000701233F	370
MC01.MCBIST.CCS.CCS_INST_ARR1_11	0x0000000007012340	371
MC01.MCBIST.CCS.CCS_INST_ARR1_12	0x0000000007012341	371
MC01.MCBIST.CCS.CCS_INST_ARR1_13	0x0000000007012342	371
MC01.MCBIST.CCS.CCS_INST_ARR1_14	0x0000000007012343	372
MC01.MCBIST.CCS.CCS_INST_ARR1_15	0x0000000007012344	372
MC01.MCBIST.CCS.CCS_INST_ARR1_16	0x0000000007012345	373
MC01.MCBIST.CCS.CCS_INST_ARR1_17	0x0000000007012346	373
MC01.MCBIST.CCS.CCS_INST_ARR1_18	0x0000000007012347	374
MC01.MCBIST.CCS.CCS_INST_ARR1_19	0x0000000007012348	374
MC01.MCBIST.CCS.CCS_INST_ARR1_20	0x0000000007012349	375
MC01.MCBIST.CCS.CCS_INST_ARR1_21	0x000000000701234A	375
MC01.MCBIST.CCS.CCS_INST_ARR1_22	0x000000000701234B	376
MC01.MCBIST.CCS.CCS_INST_ARR1_23	0x000000000701234C	376
MC01.MCBIST.CCS.CCS_INST_ARR1_24	0x000000000701234D	376
MC01.MCBIST.CCS.CCS_INST_ARR1_25	0x000000000701234E	377
MC01.MCBIST.CCS.CCS_INST_ARR1_26	0x000000000701234F	377
MC01.MCBIST.CCS.CCS_INST_ARR1_27	0x0000000007012350	378
MC01.MCBIST.CCS.CCS_INST_ARR1_28	0x0000000007012351	378

Mnemonic	Address	Page
MC01.MCBIST.CCS.CCS_INST_ARR1_29	0x0000000007012352	379
MC01.MCBIST.CCS.CCS_INST_ARR1_30	0x0000000007012353	379
MC01.MCBIST.CCS.CCS_INST_ARR1_31	0x0000000007012354	380
MC01.MCBIST.MBA_SCOMFIR.CCSARRERRINJQ	0x00000000070123DE	435
MC01.MCBIST.MBA_SCOMFIR.CCS_CNTLQ	0x00000000070123A5	408
MC01.MCBIST.MBA_SCOMFIR.CCS_FIXED_DATA0Q	0x00000000070123E5	439
MC01.MCBIST.MBA_SCOMFIR.CCS_FIXED_DATA1Q	0x00000000070123E6	439
MC01.MCBIST.MBA_SCOMFIR.CCS_MODEQ	0x00000000070123A7	408
MC01.MCBIST.MBA_SCOMFIR.CCS_STATQ	0x00000000070123A6	408
MC01.MCBIST.MBA_SCOMFIR.DBGCFG0Q	0x00000000070123E8	440
MC01.MCBIST.MBA_SCOMFIR.DBGCFG1Q	0x00000000070123E9	441
MC01.MCBIST.MBA_SCOMFIR.DBGCFG2Q	0x00000000070123EA	441
MC01.MCBIST.MBA_SCOMFIR.DBGCFG3Q	0x00000000070123EB	442
MC01.MCBIST.MBA_SCOMFIR.MBAUER0Q	0x000000000701236E	396
MC01.MCBIST.MBA_SCOMFIR.MBAUER1Q	0x0000000007012373	398
MC01.MCBIST.MBA_SCOMFIR.MBAUER2Q	0x0000000007012378	400
MC01.MCBIST.MBA_SCOMFIR.MBAUER3Q	0x000000000701237D	402
MC01.MCBIST.MBA_SCOMFIR.MBA_MCBERRPTQ	0x00000000070123E7	439
MC01.MCBIST.MBA_SCOMFIR.MBECTLQ	0x0000000007012310	317
MC01.MCBIST.MBA_SCOMFIR.MBMPER0Q	0x000000000701236C	396
MC01.MCBIST.MBA_SCOMFIR.MBMPER1Q	0x0000000007012371	398
MC01.MCBIST.MBA_SCOMFIR.MBMPER2Q	0x0000000007012376	400
MC01.MCBIST.MBA_SCOMFIR.MBMPER3Q	0x000000000701237B	402
MC01.MCBIST.MBA_SCOMFIR.MBNCER0Q	0x000000000701236A	395
MC01.MCBIST.MBA_SCOMFIR.MBNCER1Q	0x000000000701236F	397
MC01.MCBIST.MBA_SCOMFIR.MBNCER2Q	0x0000000007012374	399
MC01.MCBIST.MBA_SCOMFIR.MBNCER3Q	0x0000000007012379	401
MC01.MCBIST.MBA_SCOMFIR.MBRCER0Q	0x000000000701236B	395
MC01.MCBIST.MBA_SCOMFIR.MBRCER1Q	0x0000000007012370	397
MC01.MCBIST.MBA_SCOMFIR.MBRCER2Q	0x0000000007012375	399
MC01.MCBIST.MBA_SCOMFIR.MBRCER3Q	0x000000000701237A	401
MC01.MCBIST.MBA_SCOMFIR.MBSEC0Q	0x0000000007012355	380
MC01.MCBIST.MBA_SCOMFIR.MBSEC1Q	0x0000000007012356	381
MC01.MCBIST.MBA_SCOMFIR.MBSEVR0Q	0x000000000701237E	403
MC01.MCBIST.MBA_SCOMFIR.MBSEVR1Q	0x000000000701237F	403
MC01.MCBIST.MBA_SCOMFIR.MBSMODESQ	0x0000000007012362	394
MC01.MCBIST.MBA_SCOMFIR.MBSMSECQ	0x0000000007012369	394
MC01.MCBIST.MBA_SCOMFIR.MBSSYMEC0Q	0x0000000007012358	382
MC01.MCBIST.MBA_SCOMFIR.MBSSYMEC1Q	0x0000000007012359	384
MC01.MCBIST.MBA_SCOMFIR.MBSSYMEC2Q	0x000000000701235A	385
MC01.MCBIST.MBA_SCOMFIR.MBSSYMEC3Q	0x000000000701235B	386
MC01.MCBIST.MBA_SCOMFIR.MBSSYMEC4Q	0x000000000701235C	387
MC01.MCBIST.MBA_SCOMFIR.MBSSYMEC5Q	0x000000000701235D	389

Mnemonic	Address	Page
MC01.MCBIST.MBA_SCOMFIR.MBSSYMEC6Q	0x000000000701235E	390
MC01.MCBIST.MBA_SCOMFIR.MBSSYMEC7Q	0x000000000701235F	391
MC01.MCBIST.MBA_SCOMFIR.MBSSYMEC8Q	0x0000000007012360	392
MC01.MCBIST.MBA_SCOMFIR.MBSTRQ	0x0000000007012357	381
MC01.MCBIST.MBA_SCOMFIR.MBUER0Q	0x000000000701236D	396
MC01.MCBIST.MBA_SCOMFIR.MBUER1Q	0x0000000007012372	398
MC01.MCBIST.MBA_SCOMFIR.MBUER2Q	0x0000000007012377	400
MC01.MCBIST.MBA_SCOMFIR.MBUER3Q	0x000000000701237C	402
MC01.MCBIST.MBA_SCOMFIR.MCBACQ	0x00000000070123D5	432
MC01.MCBIST.MBA_SCOMFIR.MCBAGRAQ	0x00000000070123D6	432
MC01.MCBIST.MBA_SCOMFIR.MCBAMR0A0Q	0x00000000070123C8	428
MC01.MCBIST.MBA_SCOMFIR.MCBAMR1A0Q	0x00000000070123C9	428
MC01.MCBIST.MBA_SCOMFIR.MCBAMR2A0Q	0x00000000070123CA	429
MC01.MCBIST.MBA_SCOMFIR.MCBAMR3A0Q	0x00000000070123CB	429
MC01.MCBIST.MBA_SCOMFIR.MCBCFGQ	0x00000000070123E0	438
MC01.MCBIST.MBA_SCOMFIR.MCBDRCRQ	0x00000000070123BD	425
MC01.MCBIST.MBA_SCOMFIR.MCBDRSRQ	0x00000000070123BC	425
MC01.MCBIST.MBA_SCOMFIR.MCBEA0Q	0x00000000070123CE	430
MC01.MCBIST.MBA_SCOMFIR.MCBEA1Q	0x00000000070123CF	430
MC01.MCBIST.MBA_SCOMFIR.MCBEA2Q	0x00000000070123D2	431
MC01.MCBIST.MBA_SCOMFIR.MCBEA3Q	0x00000000070123D3	431
MC01.MCBIST.MBA_SCOMFIR.MCBFD0Q	0x00000000070123BE	426
MC01.MCBIST.MBA_SCOMFIR.MCBFD1Q	0x00000000070123BF	426
MC01.MCBIST.MBA_SCOMFIR.MCBFD2Q	0x00000000070123C0	426
MC01.MCBIST.MBA_SCOMFIR.MCBFD3Q	0x00000000070123C1	426
MC01.MCBIST.MBA_SCOMFIR.MCBFD4Q	0x00000000070123C2	426
MC01.MCBIST.MBA_SCOMFIR.MCBFD5Q	0x00000000070123C3	427
MC01.MCBIST.MBA_SCOMFIR.MCBFD6Q	0x00000000070123C4	427
MC01.MCBIST.MBA_SCOMFIR.MCBFD7Q	0x00000000070123C5	427
MC01.MCBIST.MBA_SCOMFIR.MCBFDQ	0x00000000070123C6	427
MC01.MCBIST.MBA_SCOMFIR.MCBISTFIRACT0	0x0000000007012306	316
MC01.MCBIST.MBA_SCOMFIR.MCBISTFIRACT1	0x0000000007012307	316
MC01.MCBIST.MBA_SCOMFIR.MCBISTFIRMASK	0x0000000007012303	316
MC01.MCBIST.MBA_SCOMFIR.MCBISTFIRQ	0x0000000007012300	314
MC01.MCBIST.MBA_SCOMFIR.MCBISTFIRWOF	0x0000000007012308	317
MC01.MCBIST.MBA_SCOMFIR.MCBLFSRA0Q	0x00000000070123D4	432
MC01.MCBIST.MBA_SCOMFIR.MCBMCATQ	0x00000000070123D7	433
MC01.MCBIST.MBA_SCOMFIR.MCBMR0Q	0x00000000070123A8	410
MC01.MCBIST.MBA_SCOMFIR.MCBMR1Q	0x00000000070123A9	412
MC01.MCBIST.MBA_SCOMFIR.MCBMR2Q	0x00000000070123AA	413
MC01.MCBIST.MBA_SCOMFIR.MCBMR3Q	0x00000000070123AB	415
MC01.MCBIST.MBA_SCOMFIR.MCBMR4Q	0x00000000070123AC	417
MC01.MCBIST.MBA_SCOMFIR.MCBMR5Q	0x00000000070123AD	419

Mnemonic	Address	Page
MC01.MCBIST.MBA_SCOMFIR.MCBMR6Q	0x00000000070123AE	421
MC01.MCBIST.MBA_SCOMFIR.MCBMR7Q	0x00000000070123DF	436
MC01.MCBIST.MBA_SCOMFIR.MCBPARMQ	0x00000000070123AF	422
MC01.MCBIST.MBA_SCOMFIR.MCBRCRQ	0x00000000070123B1	423
MC01.MCBIST.MBA_SCOMFIR.MCBRDS0Q	0x00000000070123B2	424
MC01.MCBIST.MBA_SCOMFIR.MCBRDS1Q	0x00000000070123B3	424
MC01.MCBIST.MBA_SCOMFIR.MCBSA0Q	0x00000000070123CC	430
MC01.MCBIST.MBA_SCOMFIR.MCBSA1Q	0x00000000070123CD	430
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MC01.MCBIST.MBA_SCOMFIR.WATCFG0AQ	0x0000000007012380	404
MC01.MCBIST.MBA_SCOMFIR.WATCFG0BQ	0x0000000007012381	404
MC01.MCBIST.MBA_SCOMFIR.WATCFG0CQ	0x0000000007012382	404
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MC01.MCBIST.MBA_SCOMFIR.WATCFG1BQ	0x0000000007012386	405
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MC01.PORT3.ECC64.SCOM.FWMS6	0x0000000007010ADE	288
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MC01.PORT3.ECC64.SCOM.HWMS0	0x0000000007010AD0	283
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MC01.PORT3.SRQ.MBA_PMU3Q	0x00000000070109FA	200
MC01.PORT3.SRQ.MBA_PMU4Q	0x00000000070109FB	201
MC01.PORT3.SRQ.MBA_PMU5Q	0x00000000070109FC	201
MC01.PORT3.SRQ.MBA_PMU6Q	0x00000000070109FD	201
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TP.TCMC01.MCFAST.TRA1.TR0.TRACE_TRDATA_CONFIG_5	0x0000000007010C48	303
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TP.TCMC01.MCSLOW.CLK_REGION	0x0000000007030006	448
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TP.TCMC01.MCSLOW.CPLT_CONF0	0x0000000007000008	66
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TP.TCMC01.MCSLOW.CTRL_ATOMIC_LOCK_REG	0x00000000070003FF	70
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TP.TCMC01.MCSLOW.EPS.DBG.DEBUG_TRACE_CONTROL	0x00000000070107D0	91
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TP.TCMC01.MCSLOW.EPS.FIR.GXSTOP0_MASK_REG	0x0000000007040014	466
TP.TCMC01.MCSLOW.EPS.FIR.GXSTOP1_MASK_REG	0x0000000007040015	467
TP.TCMC01.MCSLOW.EPS.FIR.GXSTOP2_MASK_REG	0x0000000007040016	467
TP.TCMC01.MCSLOW.EPS.FIR.GXSTOP_TRIG_REG	0x0000000007040013	466
TP.TCMC01.MCSLOW.EPS.FIR.LOCAL_FIR_ACTION0	0x0000000007040010	466
TP.TCMC01.MCSLOW.EPS.FIR.LOCAL_FIR_ACTION1	0x0000000007040011	466
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TP.TCMC01.MCSLOW.EPS.PSC.PSC.PSCOM_STATUS_ERROR_REG	0x0000000007010001	70
TP.TCMC01.MCSLOW.EPS.PSC.PSC.RING_FENCE_MASK_LATCH_REG	0x0000000007010008	73
TP.TCMC01.MCSLOW.EPS.PSC.PSC.WRITE_PROTECT_ENABLE_REG	0x0000000007010005	73
TP.TCMC01.MCSLOW.EPS.PSC.PSC.WRITE_PROTECT_RINGS_REG	0x0000000007010006	73
TP.TCMC01.MCSLOW.EPS.THERM.CONTROL_REG	0x0000000007050012	472
TP.TCMC01.MCSLOW.EPS.THERM.DTS_RESULT0	0x0000000007050000	469
TP.TCMC01.MCSLOW.EPS.THERM.DTS_TRC_RESULT	0x0000000007050003	470
TP.TCMC01.MCSLOW.EPS.THERM.ERR_STATUS_REG	0x0000000007050013	473
TP.TCMC01.MCSLOW.EPS.THERM.INJECT_REG	0x0000000007050011	472
TP.TCMC01.MCSLOW.EPS.THERM.SKITTER_CLKSRC_REG	0x0000000007050016	474
TP.TCMC01.MCSLOW.EPS.THERM.SKITTER_DATA0	0x0000000007050019	475
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TP.TCMC01.MCSLOW.EPS.THERM.SKITTER_FORCE_REG	0x0000000007050014	474
TP.TCMC01.MCSLOW.EPS.THERM.SKITTER_MODE_REG	0x0000000007050010	471
TP.TCMC01.MCSLOW.EPS.THERM.THERM_MODE_REG	0x000000000705000F	470
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TP.TCMC01.MCSLOW.ERROR_STATUS	0x000000000703000F	456
TP.TCMC01.MCSLOW.FIR_MASK	0x0000000007040002	461
TP.TCMC01.MCSLOW.HOSTATTN	0x0000000007040009	463
TP.TCMC01.MCSLOW.HOSTATTN_MASK	0x000000000704001A	469
TP.TCMC01.MCSLOW.LOCAL_FIR	0x000000000704000A	464
TP.TCMC01.MCSLOW.LOCAL_XSTOP_ERR	0x0000000007040018	468
TP.TCMC01.MCSLOW.LOCAL_XSTOP_MASK	0x0000000007040019	469
TP.TCMC01.MCSLOW.OPCG_ALIGN	0x0000000007030001	444
TP.TCMC01.MCSLOW.OPCG_CAPT1	0x0000000007030010	457
TP.TCMC01.MCSLOW.OPCG_CAPT2	0x0000000007030011	458
TP.TCMC01.MCSLOW.OPCG_CAPT3	0x0000000007030012	458
TP.TCMC01.MCSLOW.OPCG_REG0	0x0000000007030002	445
TP.TCMC01.MCSLOW.OPCG_REG1	0x0000000007030003	446
TP.TCMC01.MCSLOW.OPCG_REG2	0x0000000007030004	447
TP.TCMC01.MCSLOW.RFIR	0x0000000007040001	461
TP.TCMC01.MCSLOW.SCAN_REGION_TYPE	0x0000000007030005	447
TP.TCMC01.MCSLOW.SPATTN	0x0000000007040004	462
TP.TCMC01.MCSLOW.SPA_MASK	0x0000000007040007	463
TP.TCMC01.MCSLOW.SYNC_CONFIG	0x0000000007030000	443
TP.TCMC01.MCSLOW.TRA0.TR0.TRACE_HI_DATA_REG	0x0000000007010400	74
TP.TCMC01.MCSLOW.TRA0.TR0.TRACE_LO_DATA_REG	0x0000000007010401	74
TP.TCMC01.MCSLOW.TRA0.TR0.TRACE_TRCTRL_CONFIG	0x0000000007010402	74
TP.TCMC01.MCSLOW.TRA0.TR0.TRACE_TRDATA_CONFIG_0	0x0000000007010403	75
TP.TCMC01.MCSLOW.TRA0.TR0.TRACE_TRDATA_CONFIG_1	0x0000000007010404	75

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TP.TCMC01.MCSLOW.TRA0.TR0.TRACE_TRDATA_CONFIG_3	0x0000000007010406	75
TP.TCMC01.MCSLOW.TRA0.TR0.TRACE_TRDATA_CONFIG_4	0x0000000007010407	76
TP.TCMC01.MCSLOW.TRA0.TR0.TRACE_TRDATA_CONFIG_5	0x0000000007010408	76
TP.TCMC01.MCSLOW.TRA0.TR0.TRACE_TRDATA_CONFIG_9	0x0000000007010409	76
TP.TCMC01.MCSLOW.XFIR	0x0000000007040000	460
TP.TCMC01.MCSLOW.XSTOP1	0x000000000703000C	453
TP.TCMC01.MCSLOW.XSTOP2	0x000000000703000D	454
TP.TCMC01.MCSLOW.XSTOP3	0x000000000703000E	455

The memory registers are listed in the following tables.

Register Name	**Chiplet Control Register 0**
Mnemonic	TP.TCMC01.MCSLOW.CPLT_CTRL0
Address	0000000007000000 (SCOM) 0000000007000010 (SCOM1) 0000000007000020 (SCOM2)
Description	This register contains the first set of vital chiplet controls.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_OR	WO_CLEAR	CTRL_CC_ABSTCLK_MUXSEL_DC: Select the ABIST clock source for arrays on a chiplet boundary. When set to 1, clocks are used from a chiplet with ABIST.
1	RW	WO_OR	WO_CLEAR	TC_UNIT_SYNCCLK_MUXSEL_DC: Select the synchronous clock for asynchronous latches. (The initial value is 1.)
2	RW	WO_OR	WO_CLEAR	CTRL_CC_FLUSHMODE_INH_DC: Prevent pipeline latches from going into flush mode. (The initial value is 1.)
3	RW	WO_OR	WO_CLEAR	CTRL_CC_FORCE_ALIGN_DC: Force an alignment signal to be sent. (The initial value is 1. Drop before dropping flushmode_inh.)
4	RW	WO_OR	WO_CLEAR	TC_UNIT_ARY_WRT_THRU_DC: Set the array into write-through mode. Used for LBIST.
5	RW	WO_OR	WO_CLEAR	TC_UNIT_AVP_MODE: AVP mode. Switches from the refresh pulse to the phase counter.
6	RW	WO_OR	WO_CLEAR	FREE_USAGE_6A: Free usage.
7	RW	WO_OR	WO_CLEAR	FREE_USAGE_7A: Free usage.
8	RW	WO_OR	WO_CLEAR	CTRL_CC_ABIST_RECOV_DISABLE_DC: New signal to disable recovery.
9	RW	WO_OR	WO_CLEAR	FREE_USAGE_9A: Free usage.
10	RW	WO_OR	WO_CLEAR	TC_UNIT_IOBIST_TX_WRAP_ENABLE_DC: Unused.
11	RW	WO_OR	WO_CLEAR	RESERVED_11A: Reserved.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
12	RW	WO_OR	WO_CLEAR	TC_SKIT_MODE_BIST_DC: Enables skitter to be used functionally during the BIST. When set to 1, the scan chain is bypassed and scan enable (SE) is degated.
13	RW	WO_OR	WO_CLEAR	TC_UNIT_DETERMINISTIC_TEST_ENABLE_DC: Forces login into deterministic test mode. For example, for LBIST.
14	RW	WO_OR	WO_CLEAR	TC_UNIT_CONSTRAIN_SAFESCAN_DC: Safe scan of the N1L latches. Prevent a lock when switching the SE.
15	RW	WO_OR	WO_CLEAR	TC_UNIT_RRFA_TEST_ENABLE_DC: Enables test-only logic and latches to increase the test coverage.
16	RW	WO_OR	WO_CLEAR	TC_NBTI_HDR_ENABLE_OVR_DC: NBTI.
17	RW	WO_OR	WO_CLEAR	TC_NBTI_PROBE_GATE_DC: NBTI.
18	RW	WO_OR	WO_CLEAR	RESERVED_18A: Reserved.
19	RW	WO_OR	WO_CLEAR	RESERVED_19A: Reserved.
20:27	RW	WO_OR	WO_CLEAR	TC_PSRO_SEL_DC: PSRO select.
28	RW	WO_OR	WO_CLEAR	TC_BSC_WRAPSEL_DC: Wrap select for BSC.
29	RW	WO_OR	WO_CLEAR	TC_BSC_INTMODE_DC: INTEST instruction support (INT) mode for BSC. The IEEE 1149.1 INTEST instruction can be triggered through JTAG or through this register.
30	RW	WO_OR	WO_CLEAR	TC_BSC_INV_DC: INV for BSC mode.
31	RW	WO_OR	WO_CLEAR	TC_BSC_EXTMODE_DC: EXT mode for BSC.
32	RW	WO_OR	WO_CLEAR	TC_REFCLK_DRVR_EN_DC: Reference clock driver enable.
33	RW	WO_OR	WO_CLEAR	RESERVED_33A: Reserved.
34	RW	WO_OR	WO_CLEAR	RESERVED_34A: Reserved.
35	RW	WO_OR	WO_CLEAR	RESERVED_35A: Reserved.
36	RW	WO_OR	WO_CLEAR	TC_OELCC_EDGE_DELAYED_DC: Enables delaying the alignment by one fast cycle. Only used in dual mesh chiplets.
37	RW	WO_OR	WO_CLEAR	TC_OELCC_ALIGN_FLUSH_DC: Forces the alignment and odd/even toggling latch into the flush state. For DFT only.
38	RW	WO_OR	WO_CLEAR	RESERVED_38A: Reserved.
39	RW	WO_OR	WO_CLEAR	RESERVED_39A: Reserved.
40:41	RW	WO_OR	WO_CLEAR	CTRL_MISC_CLKDIV_SEL_DC: Clock divider select. 00 = 1024:1 01 = 64:1 10 = 16:1 11 = 4:1
42	RW	WO_OR	WO_CLEAR	RESERVED_42A: Reserved.
43	RW	WO_OR	WO_CLEAR	RESERVED_43A: Reserved.
44	RW	WO_OR	WO_CLEAR	CTRL_CC_DCTEST_DC: TE = 1 only. Enable DCTEST.
45	RW	WO_OR	WO_CLEAR	CTRL_CC_OTP_PRGMODE_DC: TE = 1 only. OTP ROM program mode
46	RW	WO_OR	WO_CLEAR	CTRL_CC_SSS_CALIBRATE_DC: TE = 1 only. Sensors calibration.
47	RW	WO_OR	WO_CLEAR	CTRL_CC_PIN_LBIST_DC: TE = 1 only. PIN LBIST mode. The LBIST is controlled by the pin, not by the OPCG.
48	RW	WO_OR	WO_CLEAR	FREE_USAGE_48A: Free usage.
49	RW	WO_OR	WO_CLEAR	FREE_USAGE_49A: Free usage.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
50	RW	WO_OR	WO_CLEAR	FREE_USAGE_50A: Free usage.
51	RW	WO_OR	WO_CLEAR	FREE_USAGE_51A: Free usage.
52	RW	WO_OR	WO_CLEAR	FREE_USAGE_52A: Free usage.
53	RW	WO_OR	WO_CLEAR	FREE_USAGE_53A: Free usage.
54	RW	WO_OR	WO_CLEAR	FREE_USAGE_54A: Free usage.
55	RW	WO_OR	WO_CLEAR	FREE_USAGE_55A: Free usage.
56	RW	WO_OR	WO_CLEAR	FREE_USAGE_56A: Free usage.
57	RW	WO_OR	WO_CLEAR	FREE_USAGE_57A: Free usage.
58	RW	WO_OR	WO_CLEAR	FREE_USAGE_58A: Free usage.
59	RW	WO_OR	WO_CLEAR	FREE_USAGE_59A: Free usage.
60	RW	WO_OR	WO_CLEAR	FREE_USAGE_60A: Free usage.
61	RW	WO_OR	WO_CLEAR	FREE_USAGE_61A: Free usage.
62	RW	WO_OR	WO_CLEAR	FREE_USAGE_62A: Free usage.
63	RW	WO_OR	WO_CLEAR	FREE_USAGE_63A: Free usage.

Register Name	Chiplet Control Register 1
Mnemonic	TP.TCMC01.MCSLOW.CPLT_CTRL1
Address	0000000007000001 (SCOM) 0000000007000011 (SCOM1) 0000000007000021 (SCOM2)
Description	This register contains the second set of vital chiplet controls.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_OR	WO_CLEAR	UNUSED_0B: Unused.
1	RW	WO_OR	WO_CLEAR	UNUSED_1B: Unused.
2	RW	WO_OR	WO_CLEAR	UNUSED_2B: Unused.
3	RW	WO_OR	WO_CLEAR	TC_VITL_REGION_FENCE: VITL fence. Protect the VITL region logic from pollution by other regions during LBIST, or when the chiplet is not initialized and running yet.
4	RW	WO_OR	WO_CLEAR	TC_PERV_REGION_FENCE: Fence for the pervasive region.
5	RW	WO_OR	WO_CLEAR	TC_REGION1_FENCE: Fence for regions mc01 - mcu.
6	RW	WO_OR	WO_CLEAR	TC_REGION2_FENCE: Fence for regions iom01 - d3, iod.
7	RW	WO_OR	WO_CLEAR	TC_REGION3_FENCE: Fence for regions iom23 - d3, iod.
8	RW	WO_OR	WO_CLEAR	UNUSED_8B: Unused.
9	RW	WO_OR	WO_CLEAR	UNUSED_9B: Unused.
10	RW	WO_OR	WO_CLEAR	UNUSED_10B: Unused.
11	RW	WO_OR	WO_CLEAR	UNUSED_11B: Unused.
12	RW	WO_OR	WO_CLEAR	UNUSED_12B: Unused.
13	RW	WO_OR	WO_CLEAR	UNUSED_13B: Unused.
14	RW	WO_OR	WO_CLEAR	UNUSED_14B: Unused.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
15	RW	WO_OR	WO_CLEAR	RESERVED: Reserved.
16	RW	WO_OR	WO_CLEAR	TC_UNIT_MULTICYCLE_TEST_FENCE: Fence logic that is indeterminate at any frequency.
17	RW	WO_OR	WO_CLEAR	UNUSED_17B: Unused.
18	RW	WO_OR	WO_CLEAR	UNUSED_18B: Unused.
19	RW	WO_OR	WO_CLEAR	UNUSED_19B: Unused.
20	RW	WO_OR	WO_CLEAR	UNUSED_20B: Unused.
21	RW	WO_OR	WO_CLEAR	UNUSED_21B: Unused.
22	RW	WO_OR	WO_CLEAR	UNUSED_22B: Unused.
23	RW	WO_OR	WO_CLEAR	UNUSED_23B: Unused.
24	RW	WO_OR	WO_CLEAR	UNUSED_24B: Unused.
25	RW	WO_OR	WO_CLEAR	UNUSED_25B: Unused.
26	RW	WO_OR	WO_CLEAR	UNUSED_26B: Unused.
27	RW	WO_OR	WO_CLEAR	UNUSED_27B: Unused.
28	RW	WO_OR	WO_CLEAR	UNUSED_28B: Unused.
29	RW	WO_OR	WO_CLEAR	UNUSED_29B: Unused.
30	RW	WO_OR	WO_CLEAR	UNUSED_30B: Unused.
31	RW	WO_OR	WO_CLEAR	UNUSED_31B: Unused.

Register Name	**Chiplet Configuration Register 0**
Mnemonic	TP.TCMC01.MCSLOW.CPLT_CONF0
Address	0000000007000008 (SCOM) 0000000007000018 (SCOM1) 0000000007000028 (SCOM2)
Description	This register contains the first set of vital chiplet configuration functions.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:5	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE0_SEL_DC: Probe 0 select.
6	RW	WO_OR	WO_CLEAR	RESERVED_6C: Reserved.
7	RW	WO_OR	WO_CLEAR	RESERVED_7C: Reserved.
8:13	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE1_SEL_DC: Probe 1 select.
14	RW	WO_OR	WO_CLEAR	RESERVED_14C: Reserved.
15	RW	WO_OR	WO_CLEAR	RESERVED_15C: Reserved.
16:21	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE2_SEL_DC: Probe 2 select.
22	RW	WO_OR	WO_CLEAR	RESERVED_22C: Reserved.
23	RW	WO_OR	WO_CLEAR	RESERVED_23C: Reserved.
24:29	RW	WO_OR	WO_CLEAR	CTRL_MISC_PROBE3_SEL_DC: Probe 3 select.
30	RW	WO_OR	WO_CLEAR	RESERVED_30C: Reserved.
31	RW	WO_OR	WO_CLEAR	RESERVED_31C: Reserved.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
32	RW	WO_OR	WO_CLEAR	CTRL_CC_OFLOW_FEH_SEL_DC: Selects an ABIST overflow or failure indication.
33	RW	WO_OR	WO_CLEAR	CTRL_CC_SCAN_PROTECT_DC: Enables scan protection. Enables the scan collision error mechanism.
34	RW	WO_OR	WO_CLEAR	CTRL_CC_SDIS_DC_N: Disables the scan diagnostic scan path.
35	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_35C: Reserved for test control.
36	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_36C: Reserved for test control.
37	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_37C: Reserved for test control.
38	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_38C: Reserved for test control.
39	RW	WO_OR	WO_CLEAR	RESERVED_TEST_CONTROL_39C: Reserved for test control.
40	RW	WO_OR	WO_CLEAR	CTRL_EPS_MASK_VITL_PCB_ERR_DC: Mask VITL PCB errors from the CC or CPLT_CTRL.
41	RW	WO_OR	WO_CLEAR	CTRL_CC_MASK_VITL_SCAN_OPCG_ERR_DC: Mask VITL errors in the CC that are not PCB related.
42	RW	WO_OR	WO_CLEAR	RESERVED_42C: Reserved.
43	RW	WO_OR	WO_CLEAR	RESERVED_43C: Reserved.
44	RW	WO_OR	WO_CLEAR	FREE_USAGE_44C: Free usage.
45	RW	WO_OR	WO_CLEAR	FREE_USAGE_45C: Free usage.
46	RW	WO_OR	WO_CLEAR	FREE_USAGE_46C: Free usage.
47	RW	WO_OR	WO_CLEAR	FREE_USAGE_47C: Free usage.
48:51	RW	WO_OR	WO_CLEAR	TC_UNIT_GROUP_ID_DC: Group ID.
52:54	RW	WO_OR	WO_CLEAR	TC_UNIT_CHIP_ID_DC: Chip ID.
55	RW	WO_OR	WO_CLEAR	RESERVED_ID_55C: Reserved ID.
56:60	RW	WO_OR	WO_CLEAR	TC_UNIT_SYS_ID_DC: System ID.
61	RW	WO_OR	WO_CLEAR	RESERVED_ID_61C: Reserved ID.
62	RW	WO_OR	WO_CLEAR	RESERVED_ID_62C: Reserved ID.
63	RW	WO_OR	WO_CLEAR	RESERVED_ID_63C: Reserved ID.

Register Name	**Chiplet Configuration Register 1**
Mnemonic	TP.TCMC01.MCSLOW.CPLT_CONF1
Address	0000000007000009 (SCOM) 0000000007000019 (SCOM1) 0000000007000029 (SCOM2)
Description	This register contains the second set of vital chiplet configuration functions.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_OR	WO_CLEAR	UNUSED_0D: Unused.
1	RW	WO_OR	WO_CLEAR	UNUSED_1D: Unused.
2	RW	WO_OR	WO_CLEAR	UNUSED_2D: Unused.
3	RW	WO_OR	WO_CLEAR	UNUSED_3D: Unused.
4	RW	WO_OR	WO_CLEAR	IOVALID_4D:

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
5	RW	WO_OR	WO_CLEAR	IOVALID_5D:
6	RW	WO_OR	WO_CLEAR	IOVALID_6D:
7	RW	WO_OR	WO_CLEAR	IOVALID_7D:
8	RW	WO_OR	WO_CLEAR	IOVALID_8D:
9	RW	WO_OR	WO_CLEAR	IOVALID_9D:
10	RW	WO_OR	WO_CLEAR	IOVALID_10D:
11	RW	WO_OR	WO_CLEAR	IOVALID_11D:
12	RW	WO_OR	WO_CLEAR	TC_IOM01_FORCETOKNOWN_DC:
13	RW	WO_OR	WO_CLEAR	TC_IOM01_DDR0_DFI_RESET_ALL:
14	RW	WO_OR	WO_CLEAR	TC_IOM01_DDR1_DFI_RESET_ALL:
15	RW	WO_OR	WO_CLEAR	TC_IOM01_DDR2_DFI_RESET_ALL:
16	RW	WO_OR	WO_CLEAR	TC_IOM01_DDR3_DFI_RESET_ALL:
17	RW	WO_OR	WO_CLEAR	FREE_USAGE_17D: Free usage.
18	RW	WO_OR	WO_CLEAR	FREE_USAGE_18D: Free usage.
19	RW	WO_OR	WO_CLEAR	FREE_USAGE_19D: Free usage.
20	RW	WO_OR	WO_CLEAR	FREE_USAGE_20D: Free usage.
21	RW	WO_OR	WO_CLEAR	FREE_USAGE_21D: Free usage.
22	RW	WO_OR	WO_CLEAR	FREE_USAGE_22D: Free usage.
23	RW	WO_OR	WO_CLEAR	FREE_USAGE_23D: Free usage.
24	RW	WO_OR	WO_CLEAR	FREE_USAGE_24D: Free usage.
25	RW	WO_OR	WO_CLEAR	FREE_USAGE_25D: Free usage.
26	RW	WO_OR	WO_CLEAR	FREE_USAGE_26D: Free usage.
27	RW	WO_OR	WO_CLEAR	FREE_USAGE_27D: Free usage.
28	RW	WO_OR	WO_CLEAR	FREE_USAGE_28D: Free usage.
29	RW	WO_OR	WO_CLEAR	FREE_USAGE_29D: Free usage.
30	RW	WO_OR	WO_CLEAR	FREE_USAGE_30D: Free usage.
31	RW	WO_OR	WO_CLEAR	FREE_USAGE_31D: Free usage.

Register Name	Chiplet Status Register
Mnemonic	TP.TCMC01.MCSLOW.CPLT_STAT0
Address	0000000007000100 (SCOM)
Description	An interrupt is sent out on a bit change if not masked by the Chiplet Mask Register. A mask only masks the interrupt, *not* the status register.

Bits	SCOM	Field Mnemonic: Description
0	ROX	SRAM_ABIST_DONE_DC: SRAM and eDRAM ABIST done.
1	ROX	DRAM_ABIST_DONE_DC: Unused in POWER9 DD1.
2	ROX	RESERVED_2E: Reserved.
3	ROX	RESERVED_3E: Reserved.

Bits	SCOM	Field Mnemonic: Description
4	ROX	TC_DIAG_PORT0_OUT: Diagnostic output port.
5	ROX	TC_DIAG_PORT1_OUT: Diagnostic output port.
6	ROX	RESERVED_6E: Reserved.
7	ROX	PLL_DESTOUT: Reserved.
8	ROX	CC_CTRL_OPCG_DONE_DC: OPCG done. Used for LBIST, ABIST, or other OPCG runs.
9	ROX	CC_CTRL_CHIPLET_IS_ALIGNED_DC: Indicates that the chiplet is aligned.
10	ROX	FREE_USAGE_10E: Free usage.
11	ROX	FREE_USAGE_11E: Free usage.
12	ROX	MC_TC_0_FIR_HOST_ATTN: Chiplet specific.
13	ROX	MC_TC_1_FIR_HOST_ATTN: Chiplet specific.
14	ROX	MC_TC_2_FIR_HOST_ATTN: Chiplet specific.
15	ROX	MC_TC_3_FIR_HOST_ATTN: Chiplet specific.
16	ROX	MC_TC_4_FIR_HOST_ATTN: Chiplet specific.
17	ROX	MC_TC_5_FIR_HOST_ATTN: Chiplet specific.
18	ROX	MC_TC_6_FIR_HOST_ATTN: Chiplet specific.
19	ROX	MC_TC_7_FIR_HOST_ATTN: Chiplet specific.
20	ROX	MC_TC_8_FIR_HOST_ATTN: Chiplet specific.
21	ROX	FREE_USAGE_21E: Free usage.
22	ROX	FREE_USAGE_22E: Free usage.
23	ROX	FREE_USAGE_23E: Free usage.

Register Name	**Chiplet Mask Register**
Mnemonic	TP.TCMC01.MCSLOW.CPLT_MASK0
Address	0000000007000101 (SCOM)
Description	This register masks an interrupt when a bit changes in the Chiplet Status Register. It does *not* mask the status itself.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CPLTMASK0: This field provides bitwise masking of the Chiplet Status Register.

Register Name	**CTRL Protect Mode Register**
Mnemonic	TP.TCMC01.MCSLOW.CTRL_PROTECT_MODE_REG
Address	00000000070003FE (SCOM)
Description	This register enables read and write protection.

Bits	SCOM	Field Mnemonic: Description
0	RW	CTRL_READ_PROTECT_ENABLE: This bit enables read protection.
1	RW	CTRL_WRITE_PROTECT_ENABLE: This bit enables write protection.

Register Name	Atomic Lock Register
Mnemonic	TP.TCMC01.MCSLOW.CTRL_ATOMIC_LOCK_REG
Address	00000000070003FF (SCOM)
Description	This register enables an atomic lock and an atomic lock counter.

Bits	SCOM	Field Mnemonic: Description
0	RW	CTRL_ATOMIC_LOCK_ENABLE: This bit enables an atomic lock.
1:4	ROX	CTRL_ATOMIC_ID: This field contains the atomic ID.
5:7	RO	Constant = 0b000
8:15	ROX	CTRL_ATOMIC_ACTIVITY: This field is an atomic lock counter.

Register Name	PSCOMLE Mode Register
Mnemonic	TP.TCMC01.MCSLOW.EPS.PSC.PSC.PSCOM_MODE_REG
Address	0000000007010000 (SCOM)
Description	This is the parallel-to-serial communication light edition (PSCOMLE) mode register.

Bits	SCOM	Field Mnemonic: Description
0	RW	ABORT_ON_PCB_ADDR_PARITY_ERROR: Abort on a PCB address parity error.
1	RW	ABORT_ON_PCB_WDATA_PARITY_ERROR: Abort on a PCB write data parity error.
2	RW	UNUSED_2B. Unused.
3	RW	ABORT_ON_DL_RETURN_WDATA_PARITY_ERROR: Abort on a DL return write data parity error.
4	RW	WATCHDOG_ENABLE: Watchdog enable.
5:6	RW	SCOM_HANG_LIMIT: 11 = 256 10 = 512 01 = 768 00 = 1023
7	RW	FORCE_ALL_RINGS: This bit is set to a logical 1 if all rings must be enabled independent of the ring address.
8	RW	FSM_SELFRESET_ON_STATEVEC_PARITYERROR_ENABLE: FSM self reset on statevec parity error enable.
9:11	RW	RESERVED_PSCOM_MODE_LT: Reserved.

Register Name	PSCOMLE Error Register
Mnemonic	TP.TCMC01.MCSLOW.EPS.PSC.PSC.PSCOM_STATUS_ERROR_REG
Address	0000000007010001 (SCOM)
Description	This is the parallel-to-serial communication light edition (PSCOMLE) error register.

Bits	SCOM	Field Mnemonic: Description
0	RWX	ACCUMULATED_PCB_WDATA_PARITY_ERROR: Accumulated PCB write data parity error.
1	RWX	ACCUMULATED_PCB_ADDRESS_PARITY_ERROR: Accumulated PCB address parity error.
2	RWX	ACCUMULATED_DL_RETURN_WDATA_PARITY_ERROR: Accumulated DL return write data parity error.
3	RWX	ACCUMULATED_DL_RETURN_P0_ERROR: Accumulated DL return P0 error.

Bits	SCOM	Field Mnemonic: Description
4	RWX	ACCUMULATED_UL_RDATA_PARITY_ERROR: Accumulated UL read data parity error.
5	RWX	ACCUMULATED_UL_P0_ERROR: Accumulated UL P0 error.
6	RWX	ACCUMULATED_PARITY_ERROR_ON_INTERFACE_MACHINE: Accumulated parity error on the interface machine.
7	RWX	ACCUMULATED_PARITY_ERROR_ON_P2S_MACHINE: Accumulated parity error on the parallel-to-serial (p2s) machine.
8	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_ULCCH: Accumulated timeout while waiting for ULCCH.
9	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: Accumulated timeout while waiting for DLDCH return.
10	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_ULDCH: Accumulated timeout while waiting for ULDCH.
11	RWX	ACCUMULATED_PSCOM_PARALLEL_WRITE_NVLD: Accumulated PSCOM parallel write NVLD.
12	RWX	ACCUMULATED_PSCOM_PARALLEL_READ_NVLD: Accumulated PSCOM parallel read NVLD.
13	RWX	ACCUMULATED_PSCOM_PARALLEL_ADDR_INVALID: Accumulated PSCOM parallel address invalid.
14	RWX	ACCUMULATED_PCB_COMMAND_PARITY_ERROR: Accumulated PCB command parity error.
15	RWX	ACCUMULATED_GENERAL_TIMEOUT: Accumulated general timeout.
16	RWX	ACCUMULATED_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: Accumulated satellite acknowledge access violation.
17	RWX	ACCUMULATED_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: Accumulated satellite acknowledge invalid register.
18	RWX	TRAPPED_PCB_WDATA_PARITY_ERROR: Trapped PCB write data parity error.
19	RWX	TRAPPED_PCB_ADDRESS_PARITY_ERROR: Trapped PCB address parity error.
20	RWX	TRAPPED_DL_RETURN_WDATA_PARITY_ERROR: Trapped DL return write data parity error.
21	RWX	TRAPPED_DL_RETURN_P0_ERROR: Trapped DL return P0 error.
22	RWX	TRAPPED_UL_RDATA_PARITY_ERROR: Trapped UL read data parity error.
23	RWX	TRAPPED_UL_P0_ERROR: Trapped UL P0 error.
24	RWX	TRAPPED_PARITY_ERROR_ON_INTERFACE_MACHINE: Trapped parity error on the interface machine.
25	RWX	TRAPPED_PARITY_ERROR_ON_P2S_MACHINE: Trapped parity error on the parallel-to-serial machine.
26	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_ULCCH: Trapped timeout while waiting for ULCCH.
27	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: Trapped timeout while waiting for DLDCH return.
28	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_ULDCH: Trapped timeout while waiting for ULDCH.
29	RWX	TRAPPED_PSCOM_PARALLEL_WRITE_NVLD: Trapped PSCOM parallel write NVLD.
30	RWX	TRAPPED_PSCOM_PARALLEL_READ_NVLD: Trapped PSCOM parallel read NVLD.
31	RWX	TRAPPED_PSCOM_PARALLEL_ADDR_INVALID: Trapped PSCOM parallel address invalid.
32	RWX	TRAPPED_PCB_COMMAND_PARITY_ERROR: Trapped PCB command parity error.
33	RWX	TRAPPED_GENERAL_TIMEOUT: Trapped general timeout.
34	RWX	TRAPPED_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: Trapped satellite acknowledge access violation.
35	RWX	TRAPPED_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: Trapped satellite acknowledge invalid register.

Register Name	PSCOMLE Error Mask Register
Mnemonic	TP.TCMC01.MCSLOW.EPS.PSC.PSC.PSCOM_ERROR_MASK
Address	0000000007010002 (SCOM)
Description	This is the parallel-to-serial communication light edition (PSCOMLE) error mask register.

Bits	SCOM	Field Mnemonic: Description
0	RW	MASK_PCB_WDATA_PARITY_ERROR: Mask PCB write data parity error.
1	RW	MASK_PCB_ADDRESS_PARITY_ERROR: Mask PCB address parity error.
2	RW	MASK_DL_RETURN_WDATA_PARITY_ERROR: Mask DL return write data parity error.
3	RW	MASK_DL_RETURN_P0_ERROR: Mask DL return P0 error.
4	RW	MASK_UL_RDATA_PARITY_ERROR: Mask UL read data parity error.
5	RW	MASK_UL_P0_ERROR: Mask UL P0 error.
6	RW	MASK_PARITY_ERROR_ON_INTERFACE_MACHINE: Mask parity error on the interface machine.
7	RW	MASK_PARITY_ERROR_ON_P2S_MACHINE: Mask parity error on the parallel-to-serial machine.
8	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_ULCCH: Mask timeout while waiting for ULCCH.
9	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: Mask timeout while waiting for DLDCH return.
10	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_ULDCH: Mask timeout while waiting or ULDCH.
11	RW	MASK_PSCOM_PARALLEL_WRITE_NVLD: Mask PSCOM parallel write NVLD.
12	RW	MASK_PSCOM_PARALLEL_READ_NVLD: Mask PSCOM parallel read NVLD.
13	RW	MASK_PSCOM_PARALLEL_ADDR_INVALID: Mask PSCOM parallel address invalid.
14	RW	MASK_PCB_COMMAND_PARITY_ERROR: Mask PCB command parity error.
15	RW	MASK_GENERAL_TIMEOUT: Mask general timeout.
16	RW	MASK_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: Mask satellite acknowledge access violation.
17	RW	MASK_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: Mask satellite acknowledge invalid register.

Register Name	PSCOMLE Address Trap Register
Mnemonic	TP.TCMC01.MCSLOW.EPS.PSC.PSC.ADDR_TRAP_REG
Address	0000000007010003 (SCOM)
Description	This is the parallel-to-serial communication light edition (PSCOMLE) address trap register.

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	PCB_ADDRESS_OF_LAST_TRANSACTION_WITH_ERROR: This field contains the PCB address of the last transaction with an error.
16	ROX	PCB_READ_NOTWRITE_OF_LAST_TRANSACTION_WITH_ERROR: PCB read, not write, of the last transaction with an error.
17	ROX	RESERVED_ADDR_LAST_TRAP_LT: Reserved 0.
18:30	ROX	SERIAL2PARALLEL_STATE_MACHINE_AT_TIME_OF_ERROR: Serial-to-parallel state machine at the time of the error.
31	ROX	SATELLITE_ACKNOWLEDGE_BIT_RETURN_PARITY: Satellite acknowledge bit. This bit is set to 1 if no parity error is detected in the satellite number or acknowledgment bits.

Bits	SCOM	Field Mnemonic: Description
32	ROX	SATELLITE_ACKNOWLEDGE_BIT_WRITE_PARITY_ERROR: This bit is set if a write parity error is detected by the satellite.
33	ROX	SATELLITE_ACKNOWLEDGE_BIT_ACCESS_VIOLATION: This bit is set if an invalid read or write access is detected by the satellite.
34	ROX	SATELLITE_ACKNOWLEDGE_BIT_INVALID_REGISTER: This bit is set if an invalid register address is detected by the satellite.

Register Name	Ring Lock Enable Register
Mnemonic	TP.TCMC01.MCSLOW.EPS.PSC.PSC.WRITE_PROTECT_ENABLE_REG
Address	0000000007010005 (SCOM)
Description	This register enables the ring lock.

Bits	SCOM	Field Mnemonic: Description
0	RW	ENABLE_RING_LOCKING: General enable of ring locking upon a write to a specific ring.
1	RW	RESERVED_RING_LOCKING: Reserved.

Register Name	Write Protect Rings Register
Mnemonic	TP.TCMC01.MCSLOW.EPS.PSC.PSC.WRITE_PROTECT_RINGS_REG
Address	0000000007010006 (SCOM)
Description	This register writes ring-protect bit maps.

Bits	SCOM	Field Mnemonic: Description
0:15	RW	WRITE_PROTECT_RINGS: Writes a protect bit map for each ring.

Register Name	Atomic Lock Mask Register
Mnemonic	TP.TCMC01.MCSLOW.EPS.PSC.PSC.ATOMIC_LOCK_MASK_LATCH_REG
Address	0000000007010007 (SCOM)
Description	This register provides a bit mask for atomic locking.

Bits	SCOM	Field Mnemonic: Description
0:15	RW	ATOMIC_LOCK_MASK: This field provides a bit mask for atomic locking on a ring-by-ring basis.

Register Name	Ring Fence Enable Mask Register
Mnemonic	TP.TCMC01.MCSLOW.EPS.PSC.PSC.RING_FENCE_MASK_LATCH_REG
Address	0000000007010008 (SCOM)
Description	This register provides a bit mask for ring fencing.

Bits	SCOM	Field Mnemonic: Description
0	RO	Constant = 0b0
1:15	RW	RING_FENCE_ENABLE_MASK: This field provides a bit mask for ring fencing on a ring-by-ring basis.

Register Name	Trace Array High Data Register
Mnemonic	TP.TCMC01.MCSLOW.TRA0.TR0.TRACE_HI_DATA_REG
Address	0000000007010400 (SCOM)
Description	This register provides the high trace-array data.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: This field contains trace array data 0:63.

Register Name	Trace Array Low Data Register
Mnemonic	TP.TCMC01.MCSLOW.TRA0.TR0.TRACE_LO_DATA_REG
Address	0000000007010401 (SCOM)
Description	This register provides the low trace-array data.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace array data 64:95.
32:41	ROX	TRACE_ADDRESS: Trace address.
42:50	ROX	TRACE_LAST_BANK: Trace last bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace last bank valid.
52	ROX	TRACE_WRITE_ON_RUN: Trace write-on-run indicator.
53	ROX	TRACE_RUNNING: Trace run indicator.
54:63	ROX	TRACE_HOLD_ADDRESS: Trace hold address (pointing to last entry).

Register Name	Trace Control Configuration Register
Mnemonic	TP.TCMC01.MCSLOW.TRA0.TR0.TRACE_TRCTRL_CONFIG
Address	0000000007010402 (SCOM)
Description	This register contains trace control configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	STORE_ON_TRIG_MODE: This bit enables store-on-trigger mode.
1	RW	WRITE_ON_RUN_MODE: This bit enables an unconditional forced write when a trace is run.
2:9	RW	EXTEND_TRIG_MODE: This field contains the counter value for extended trigger mode.
10	RW	BANK_MODE: This bit enables bank mode.
11	RW	ENH_TRACE_MODE: This bit enables enhanced trace mode.
12	RW	LOCAL_CLOCK_GATE_CONTROL: When this bit is set, internal clock gating is disabled. The trace control logic and the trace data pipeline are always clocked.
13	RW	UNUSED_13B. Unused.
14:17	RW	TRACE_SELCT_CONTROL: This field is a selector for two sets of external trace bus multiplexers: tra_mux0_sel(0:1) and tra_mux1_sel(0:1).
18:21	RW	SPARE_CONTROL: This field contains spare control bits.

Register Name	Trace Data Configuration Register 0
Mnemonic	TP.TCMC01.MCSLOW.TRA0.TR0.TRACE_TRDATA_CONFIG_0
Address	0000000007010403 (SCOM)
Description	This register contains a trace data compare mask for bits 0 - 63.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: This field contains a trace data compare mask for bits 0 - 63.

Register Name	Trace Data Configuration Register 1
Mnemonic	TP.TCMC01.MCSLOW.TRA0.TR0.TRACE_TRDATA_CONFIG_1
Address	0000000007010404 (SCOM)
Description	This register contains a trace data compare mask for bits 64 - 87.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: This field contains a trace data compare mask for bits 64 - 87.

Register Name	Trace Data Configuration Register 2
Mnemonic	TP.TCMC01.MCSLOW.TRA0.TR0.TRACE_TRDATA_CONFIG_2
Address	0000000007010405 (SCOM)
Description	This register contains patterns A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: Pattern match pattern A 0 - 23. Pattern A is used to perform a data compare on the trace data. When the data compare matches, a trigger is generated that can be used for a "store on trigger" function or as a trace trigger to the debug macro.
24:47	RW	PATTERNB: Pattern match pattern B 0 - 23. Pattern B is used to perform a data compare on the trace data. When the data compare matches, a trigger is generated that can be used for a "store on trigger" function or as a trace trigger to the debug macro.

Register Name	Trace Data Configuration Register 3
Mnemonic	TP.TCMC01.MCSLOW.TRA0.TR0.TRACE_TRDATA_CONFIG_3
Address	0000000007010406 (SCOM)
Description	This register contains patterns C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNC: Pattern match pattern C 0 - 23. Pattern C is used to perform a data compare on the trace data. When the data compare matches, a trigger is generated that can be used for a "store on trigger" function or as a trace trigger to the debug macro.
24:47	RW	PATTERND: Pattern match pattern D 0 - 23. Pattern D is used to perform a data compare on the trace data. When the data compare matches, a trigger is generated that can be used for a "store on trigger" function or as a trace trigger to the debug macro.

Register Name	Trace Data Configuration Register 4
Mnemonic	TP.TCMC01.MCSLOW.TRA0.TR0.TRACE_TRDATA_CONFIG_4
Address	0000000007010407 (SCOM)
Description	This register contains masks A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: Mask A. When set to '1', masks off bits from Pattern A. This field is used to mask off individual bits of Pattern A so that they are "don't care" for the data compare match function.
24:47	RW	MASKB: Mask B. When set to '1', masks off bits from Pattern B. This field is used to mask off individual bits of Pattern B so that they are "don't care" for the data compare match function.

Register Name	Trace Data Configuration Register 5
Mnemonic	TP.TCMC01.MCSLOW.TRA0.TR0.TRACE_TRDATA_CONFIG_5
Address	0000000007010408 (SCOM)
Description	This register contains masks C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: Mask C. When set to '1', masks off bits from Pattern C. This field is used to mask off individual bits of Pattern C so that they are "don't care" for the data compare match function.
24:47	RW	MASKD: Mask D. When set to '1', masks off bits from Pattern D. This field is used to mask off individual bits of Pattern D so that they are "don't care" for the data compare match function.

Register Name	Trace Data Configuration Register 9
Mnemonic	TP.TCMC01.MCSLOW.TRA0.TR0.TRACE_TRDATA_CONFIG_9
Address	0000000007010409 (SCOM)
Description	This register contains trace data configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disable trace data compression (store data every cycle).
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Take into account (care about) changes in the error bit for trace data compression (default = 0).
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 00 = Debug bus bits(00:23) 01 = Debug bus bits(24:47) 10 = Debug bus bits(48:71) 11 = Debug bus bits(72:87) | 8 zeros
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 00 = Debug bus bits(00:23) 01 = Debug bus bits(24:47) 10 = Debug bus bits(48:71) 11 = Debug bus bits(72:87) | 8 zeros
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 00 = Debug bus bits(00:23) 01 = Debug bus bits(24:47) 10 = Debug bus bits(48:71) 11 = Debug bus bits(72:87) | 8 zeros

Bits	SCOM	Field Mnemonic: Description
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 00 = Debug bus bits(00:23) 01 = Debug bus bits(24:47) 10 = Debug bus bits(48:71) 11 = Debug bus bits(72:87) | 8 zeros
10:13	RW	TRIG0_OR_MASK: **Note**: The OR of all selected MATCHes is ORed with the result of TRIG0_AND: 1XXX selects MATCHA OR. X1XX selects MATCHB OR. XX1X selects MATCHC OR. XXX1 selects MATCHD OR. 0000 selects to not OR any MATCHes.
14:17	RW	TRIG0_AND_MASK: **Note**: The AND of the following selected MATCHes is ORed with the result of TRIG0_OR: 1XXX selects MATCHA AND. X1XX selects MATCHB AND. XX1X selects MATCHC AND. XXX1 selects MATCHD AND. 0000 selects to not AND any MATCHes together to form TRIG0.
18:21	RW	TRIG1_OR_MASK: **Note**: The OR of all selected MATCHes is ORed with the result of TRIG1_AND: 1XXX selects MATCHA OR. X1XX selects MATCHB OR. XX1X selects MATCHC OR. XXX1 selects MATCHD OR. 0000 selects to not OR any MATCHes to form TRIG1.
22:25	RW	TRIG1_AND_MASK: **Note**: The AND of the following selected MATCHes is ORed with the result of TRIG1_OR: 1XXX selects MATCHA AND. X1XX selects MATCHB AND. XX1X selects MATCHC AND. XXX1 selects MATCHD AND. 0000 selects to not AND any MATCHes together to form TRIG1.
26	RW	TRIG0_NOT_MODE: Invert TRIG0 before using it.
27	RW	TRIG1_NOT_MODE: Invert TRIG1 before using it.
28:31	RW	MATCH_NOT_MODE: Invert the match polarity before using it to form a TRIGger: 1000 inverts MATCHA. 0100 inverts MATCHB. 0010 inverts MATCHC. 0001 inverts MATCHD.
32:35	RW	Reserved.
36	RW	DD1_STRETCH_TRIGGER_PULSES: (DD1 workaround) Stretches the trigger output pulses to two clocks. This bit must be enabled for MCFAST and L2FAST traces.
37	RW	Reserved.

Register Name	Debug Mode Register
Mnemonic	TP.TCMC01.MCSLOW.EPS.DBG.DBG_MODE_REG
Address	00000000070107C0 (SCOM)
Description	This is debug macro configuration register 0 for the configuration component.

Bits	SCOM	Field Mnemonic: Description
0:2	RW	GLB_BRCST_MODE: Global broadcast mode (0 - 2): 100 = dbg_trace_run and dbg_trace_freeze. 101 = pc_tcdbg_trace_run_fncd and dbg_trace_freeze. 110 = dbg_triggers_out(0 to 1). 111 = pc_tcdbg_triggers(0 to 1) (from core.)
3:5	RW	TRACE_SEL_MODE: Selects the source for trace_run and bank: 001 = core trace run and bank. 010 = tp broadcast run and 0. 011 = tc_dbg_inter_brcst latched. 100 = tc_dbg_dbg_sync_brcst_rcv. else: dbg_trace_run and dbg_trace_bank.
6:7	RW	TRIG_SEL_MODE: Selects the source for tcdbg_trigger(0): 10 = global broadcast. 11 = pc_tcdbg_trigger (from core). else: dbg_triggers_out(0:1).
8	RW	STOP_ON_XSTOP_SELECTION: This bit enables a trace stop on a checkstop.
9	RW	STOP_ON_RECOV_ERR_SELECTION: This bit enables a trace stop on a recoverable error.
10	RW	STOP_ON_SPATTN_SELECTION: This bit enables a trace stop on special attention.
11	RW	FREEZE_SEL_MODE: Select the freeze source: 0 = Local debug freeze. 1 = Via broadcast: tp_tcdbg_glb_brcst(1).
12:13	RW	SYNC_BRCST_MODE: Originally used for synchronous broadcast mode; currently unused because obsolete. See TRACE_SEL_MODE.
14	RO	Constant = 0b0 See SYNC_BRCST_MODE.
15	RO	Constant = 0b0
16:31	ROX	DBG_STATUS: Read-only debug status bits.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Debug Instance 1 Condition 1 Register
Mnemonic	TP.TCMC01.MCSLOW.EPS.DBG.DBG_INST1_COND_REG_1
Address	00000000070107C1 (SCOM)
Description	This is debug macro configuration register 1 for front-end component 1.

Bits	SCOM	Field Mnemonic: Description
0:7	RW	INST1_COND1_SEL_A: Multiplexer for cond1_trig_in(0): 000 select constant 0 001 select constant 1 -- CONDITION FEEDBACK -- 002 select inst1_dbg_cond1 003 select inst1_dbg_cond2 004 select inst1_dbg_cond3 005 select inst1_dbg_cond2timeout 006 select inst2_dbg_cond1 007 select inst2_dbg_cond2 008 select inst2_dbg_cond3 009 select inst2_dbg_cond2timeout 010 select inst3_dbg_cond1 - unused, tied down 011 select inst3_dbg_cond2 - unused, tied down

Bits	SCOM	Field Mnemonic: Description
		012 select inst3_dbg_cond3 - unused, tied down 013 select inst3_dbg_cond2timeout - unused, tied down 014 select inst4_dbg_cond1 - unused, tied down 015 select inst4_dbg_cond2 - unused, tied down 016 select inst4_dbg_cond3 - unused, tied down 017 select inst4_dbg_cond2timeout - unused, tied down 018 select inst1_dbg_trig_sp 019 select inst2_dbg_trig_sp 020 select inst3_dbg_trig_sp - unused, tied down 021 select inst4_dbg_trig_sp - unused, tied down 022 select tctrc_tcdbg_trigger_a(0) 023 select tctrc_tcdbg_trigger_b(0) 024 select tctrc_tcdbg_trigger_a(0) and tctrc_tcdbg_trigger_b(0) 025 select tctrc_tcdbg_trigger_a(1) 026 select tctrc_tcdbg_trigger_b(1) 027 select tctrc_tcdbg_trigger_a(1) and tctrc_tcdbg_trigger_b(1) 028 select tctrc_tcdbg_trigger_a(2) 029 select tctrc_tcdbg_trigger_b(2) 030 select tctrc_tcdbg_trigger_a(2) and tctrc_tcdbg_trigger_b(2) 031 select tctrc_tcdbg_trigger_a(3) 032 select tctrc_tcdbg_trigger_b(3) 033 select tctrc_tcdbg_trigger_a(3) and tctrc_tcdbg_trigger_b(3) 034 select tctrc_tcdbg_trigger_a(4) 035 select tctrc_tcdbg_trigger_b(4) 036 select tctrc_tcdbg_trigger_a(4) and tctrc_tcdbg_trigger_b(4) 037 select tctrc_tcdbg_trigger_a(5) 038 select tctrc_tcdbg_trigger_b(5) 039 select tctrc_tcdbg_trigger_a(5) and tctrc_tcdbg_trigger_b(5) 040 select tctrc_tcdbg_trigger_a(6) 041 select tctrc_tcdbg_trigger_b(6) 042 select tctrc_tcdbg_trigger_a(6) and tctrc_tcdbg_trigger_b(6) 043 select tctrc_tcdbg_trigger_a(7) 044 select tctrc_tcdbg_trigger_b(7) 045 select tctrc_tcdbg_trigger_a(7) and tctrc_tcdbg_trigger_b(7) 046 select tctrc_tcdbg_trigger_a(8) 047 select tctrc_tcdbg_trigger_b(8) 048 select tctrc_tcdbg_trigger_a(8) and tctrc_tcdbg_trigger_b(8) 049 select tctrc_tcdbg_trigger_a(9) 050 select tctrc_tcdbg_trigger_b(9) 051 select tctrc_tcdbg_trigger_a(9) and tctrc_tcdbg_trigger_b(9) 052 select tctrc_tcdbg_trigger_a(10) 053 select tctrc_tcdbg_trigger_b(10) 054 select tctrc_tcdbg_trigger_a(10) and tctrc_tcdbg_trigger_b(10) 055 select tctrc_tcdbg_trigger_a(11) 056 select tctrc_tcdbg_trigger_b(11) 057 select tctrc_tcdbg_trigger_a(11) and tctrc_tcdbg_trigger_b(11) 058 select tctrc_tcdbg_trigger_a(12) 059 select tctrc_tcdbg_trigger_b(12) 060 select tctrc_tcdbg_trigger_a(12) and tctrc_tcdbg_trigger_b(12) 061 select tctrc_tcdbg_trigger_a(13) 062 select tctrc_tcdbg_trigger_b(13) 063 select tctrc_tcdbg_trigger_a(13) and tctrc_tcdbg_trigger_b(13) 064 select tctrc_tcdbg_trigger_a(14) 065 select tctrc_tcdbg_trigger_b(14) 066 select tctrc_tcdbg_trigger_a(14) and tctrc_tcdbg_trigger_b(14) 067 select tctrc_tcdbg_trigger_a(15) 068 select tctrc_tcdbg_trigger_b(15) 069 select tctrc_tcdbg_trigger_a(15) and tctrc_tcdbg_trigger_b(15) 070 select tctrc_tcdbg_trigger_a(16) 071 select tctrc_tcdbg_trigger_b(16)

Bits	SCOM	Field Mnemonic: Description
		072 select tctrc_tcdbg_trigger_a(16) and tctrc_tcdbg_trigger_b(16) 073 select tctrc_tcdbg_trigger_a(17) 074 select tctrc_tcdbg_trigger_b(17) 075 select tctrc_tcdbg_trigger_a(17) and tctrc_tcdbg_trigger_b(17) -- LOGIC (UNIT) TRIGGERS -- EP: 0:3 L3C0, 4:7 L3C1, 8:9 local core checkstop, 10 TP (hang), 11 spare, 12:13 MCA, 14:15 spare ES: 0:4 L4C, 5:6 L4F, 7:8 TPTOD, 9 TP (hang), 10:15 spare 076 select logic_trigger_in(0) 077 select logic_trigger_in(1) 078 select logic_trigger_in(2) 079 select logic_trigger_in(3) 080 select logic_trigger_in(4) 081 select logic_trigger_in(5) 082 select logic_trigger_in(6) 083 select logic_trigger_in(7) 084 select logic_trigger_in(8) 085 select logic_trigger_in(9) 086 select logic_trigger_in(10) 087 select logic_trigger_in(11) 088 select logic_trigger_in(12) 089 select logic_trigger_in(13) 090 select logic_trigger_in(14) 091 select logic_trigger_in(15) 092 select pc_tcdbg_trigger(0) 093 select pc_tcdbg_trigger(1) 094 select tctrc_tcdbg_glb_brcst(0) 095 select tctrc_tcdbg_glb_brcst(1) 096 select xstop_err 097 select recov_err 098 select spattn 099 select fir_dbg_local_xstop_err 100 select tc_dbg_inter_brcst(0) 101 select tc_dbg_inter_brcst(1) -- CORE TRIGGERS (EP chip only) -- **Note**: set core_slave_mode to honor ec[0:5]_tc_trace_run 102 select core trigger 0: any rising edge of ec[0:5]_tc_trace_run(0) 103 select core trigger 1: any rising edge of ec[0:5]_tc_trace_run(1) 104 select core trigger 2: any falling edge of ec[0:5]_tc_trace_run(0) 105 select core trigger 3: any falling edge of ec[0:5]_tc_trace_run(1) 106 select glb_trig_or_trace_in(0) 107 select glb_trig_or_trace_in(1) 108 select core_local_brcst_trc(0) 109 select core_local_brcst_trc(1) 110 select glb_freeze_brcst_rec(0) 111 select trig_2_extern_in(0) 112 select trig_2_extern_in(1) 113 select dbg_triggers_out(2) 114 select dbg_triggers_out(3) 115 select dbg_triggers_out(4) 116 select dbg_triggers_out(5) 117 select dbg_triggers_out(6) 118 select tcdbg_trigger_in(0) 119 select tcdbg_trigger_in(1)
8:15	RW	INST1_COND1_SEL_B: Multiplexer for cond1_trig_in(1). Selection as cond1_trig_in(0).
16:23	RW	INST1_COND2_SEL_A: Multiplexer for cond2_trig_in(0). Selection as cond1_trig_in(0).

Bits	SCOM	Field Mnemonic: Description
24:31	RW	INST1_COND2_SEL_B: Multiplexer for cond2_trig_in(1). Selection as cond1_trig_in(0).
32	RW	INST1_C1_INAROW_MODE: Counter 1 in-a-row mode for front-end instance (or component) 1.
33	RW	INST1_AND_TRIGGER_MODE1: Front-end instance 1 and trigger mode condition 1.
34	RW	INST1_NOT_TRIGGER_MODE1: Front-end instance 1 inverted trigger mode condition 1.
35	RW	INST1_EDGE_TRIGGER_MODE1: Front-end instance 1 edge trigger mode condition 1.
36:38	RWX	INST1_UNUSED_1: Unused.
39	RW	INST1_C2_INAROW_MODE: Counter 2 in-a-row mode for front-end instance (or component) 1.
40	RW	INST1_AND_TRIGGER_MODE2: Front-end instance 1 and trigger mode2.
41	RW	INST1_NOT_TRIGGER_MODE2: Front-end instance 1 inverted (not) trigger.
42	RW	INST1_EDGE_TRIGGER_MODE2: Front-end instance 1 edge trigger.
43:45	RWX	INST1_UNUSED_2: Unused
46	RW	INST1_COND3_ENABLE_RESET: Front-end instance 1 condition 3 enable.
47	RW	INST1_EXACT_TO_MODE: Front-end instance 1 exact timeout mode.
48	RW	INST1_RESET_C2TIMER_ON_C1: Front-end instance 1 reset condition 2 timer on condition 1.
49	RW	INST1_RESET_C3_ON_C0: Front-end instance 1 reset condition 3 on condition 0.
50	RW	INST1_SLOW_TO_MODE: Front-end instance 1 slow timeout mode.
51	RW	INST1_EXACT_RESET_C3_ON_TO: Front-end instance 1 exact reset condition 3 on timeout.
52:55	RW	INST1_C1_COUNT_LT: Instance 1 condition 1 counter compare value.
56:59	RW	INST1_C2_COUNT_LT: Instance 1 condition 2 counter compare value.
60:62	RW	INST1_RESET_C3_SELECT: Front-end instance 1: reset condition 3 for reset_c3_on_c0: 100 = dbg_cross_couple_triggers(4) 101 = dbg_cross_couple_triggers(12) 110 = dbg_cross_couple_triggers(20) 111 = dbg_cross_couple_triggers(28)

Register Name	**Debug Instance 1 Condition 2 Register**
Mnemonic	TP.TCMC01.MCSLOW.EPS.DBG.DBG_INST1_COND_REG_2
Address	00000000070107C2 (SCOM)
Description	This is debug macro configuration register 2 for front-end component 1.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	INST1_CROSS_COUPLE_SELECT_1_A: Cross coupling is the same for all selectors: 00000 selects inst1_cond1_trig_a 00001 selects inst1_cond1_trig_b 00010 selects inst1_cond2_trig_a 00011 selects inst1_cond2_trig_b 00100 selects inst1_condition1 00101 selects inst1_condition2 00110 selects inst1_condition3 00111 selects inst1_cond2_timeout 01000 selects inst2_cond1_trig_a 01001 selects inst2_cond1_trig_b 01010 selects inst2_cond2_trig_a 01011 selects inst2_cond2_trig_b 01100 selects inst2_condition1 01101 selects inst2_condition2 01110 selects inst2_condition3 01111 selects inst2_cond2_timeout 10000 selects inst3_cond1_trig_a 10001 selects inst3_cond1_trig_b 10010 selects inst3_cond2_trig_a 10011 selects inst3_cond2_trig_b 10100 selects inst3_condition1 10101 selects inst3_condition2 10110 selects inst3_condition3 10111 selects inst3_cond2_timeout 11000 selects inst4_cond1_trig_a 11001 selects inst4_cond1_trig_b 11010 selects inst4_cond2_trig_a 11011 selects inst4_cond2_trig_b 11100 selects inst4_condition1 11101 selects inst4_condition2 11110 selects inst4_condition3 11111 selects inst4_cond2_timeout
5:9	RW	INST1_CROSS_COUPLE_SELECT_1_B: Instance 1 cross couple select 1 b.
10:14	RW	INST1_CROSS_COUPLE_SELECT_2_A: Instance 1 cross couple select 2 a.
15:19	RW	INST1_CROSS_COUPLE_SELECT_2_B: Instance 1 cross couple select 2 b.
20:43	RW	INST1_TO_CMP_LT: Compare value for special counter sp_cnt_lt in debug component 1.
44	RW	INST1_FORCE_TEST_MODE: Force test mode to indicate to compare without an actual compare.

Register Name	**Debug Instance 1 Condition 3 Register**
Mnemonic	TP.TCMC01.MCSLOW.EPS.DBG.DBG_INST1_COND_REG_3
Address	00000000070107C3 (SCOM)
Description	This is debug macro configuration register 2 for the front-end 1 component.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	INST1_SP_COUNT_LT: Timeout counter to_cmp compare value for dbg_cond_comp_1.

Register Name	Debug Instance 2 Condition 1 Register
Mnemonic	TP.TCMC01.MCSLOW.EPS.DBG.DBG_INST2_COND_REG_1
Address	00000000070107C4 (SCOM)
Description	This is debug macro configuration register 1 for the front-end 1 component.

Bits	SCOM	Field Mnemonic: Description
0:7	RW	INST2_COND1_SEL_A: Multiplexer for cond1_trig_in(0): 000 = Select constant 0 001 = Select constant 1 -- CONDITION FEEDBACK -- 002 = Select inst2_dbg_cond1 003 = Select inst2_dbg_cond2 004 = Select inst2_dbg_cond3 005 = Select inst2_dbg_cond2timeout 006 = Select inst2_dbg_cond1 007 = Select inst2_dbg_cond2 008 = Select inst2_dbg_cond3 009 = Select inst2_dbg_cond2timeout 010 = Select inst3_dbg_cond1 - unused, tied down 011 = Select inst3_dbg_cond2 - unused, tied down 012 = Select inst3_dbg_cond3 - unused, tied down 013 = Select inst3_dbg_cond2timeout - unused, tied down 014 = Select inst4_dbg_cond1 - unused, tied down 015 = Select inst4_dbg_cond2 - unused, tied down 016 = Select inst4_dbg_cond3 - unused, tied down 017 = Select inst4_dbg_cond2timeout - unused, tied down 018 = Select inst2_dbg_trig_sp 019 = Select inst2_dbg_trig_sp 020 = Select inst3_dbg_trig_sp - unused, tied down 021 = Select inst4_dbg_trig_sp - unused, tied down 022 = Select tctrc_tcdbg_trigger_a(0) 023 = Select tctrc_tcdbg_trigger_b(0) 024 = Select tctrc_tcdbg_trigger_a(0) and tctrc_tcdbg_trigger_b(0) 025 = Select tctrc_tcdbg_trigger_a(1) 026 = Select tctrc_tcdbg_trigger_b(1) 027 = Select tctrc_tcdbg_trigger_a(1) and tctrc_tcdbg_trigger_b(1) 028 = Select tctrc_tcdbg_trigger_a(2) 029 = Select tctrc_tcdbg_trigger_b(2) 030 = Select tctrc_tcdbg_trigger_a(2) and tctrc_tcdbg_trigger_b(2) 031 = Select tctrc_tcdbg_trigger_a(3) 032 = Select tctrc_tcdbg_trigger_b(3) 033 = Select tctrc_tcdbg_trigger_a(3) and tctrc_tcdbg_trigger_b(3) 034 = Select tctrc_tcdbg_trigger_a(4) 035 = Select tctrc_tcdbg_trigger_b(4) 026 = Select tctrc_tcdbg_trigger_a(4) and tctrc_tcdbg_trigger_b(4) 027 = Select tctrc_tcdbg_trigger_a(5) 028 = Select tctrc_tcdbg_trigger_b(5) 029 = Select tctrc_tcdbg_trigger_a(5) and tctrc_tcdbg_trigger_b(5) 030 = Select tctrc_tcdbg_trigger_a(6) 031 = Select tctrc_tcdbg_trigger_b(6) 032 = Select tctrc_tcdbg_trigger_a(6) and tctrc_tcdbg_trigger_b(6) 033 = Select tctrc_tcdbg_trigger_a(7) 034 = Select tctrc_tcdbg_trigger_b(7) 035 = Select tctrc_tcdbg_trigger_a(7) and tctrc_tcdbg_trigger_b(7) 036 = Select tctrc_tcdbg_trigger_a(8) 037 = Select tctrc_tcdbg_trigger_b(8) 038 = Select tctrc_tcdbg_trigger_a(8) and tctrc_tcdbg_trigger_b(8) 039 = Select tctrc_tcdbg_trigger_a(9)

Bits	SCOM	Field Mnemonic: Description
		040 = Select tctrc_tcdbg_trigger_b(9) 041 = Select tctrc_tcdbg_trigger_a(9) and tctrc_tcdbg_trigger_b(9) 042 = Select xstop_err 043 = Select recov_err 044 = Select spattn 045 select fir_dbg_local_xstop_err 046 select tc_dbg_inter_brcst(0) 047 select tc_dbg_inter_brcst(1) -- LOGIC (UNIT) TRIGGERS -- EP: 0:3 L3C0, 4:7 L3C1, 8:9 local core checkstop, 10 TP (hang), 11 spare, 12:13 MCA, 14:15 spare ES: 0:4 L4C, 5:6 L4F, 7:8 TPTOD, 9 TP (hang), 10:15 spare 102 select logic_trigger_in(0) 103 select logic_trigger_in(1) 104 select logic_trigger_in(2) 105 select logic_trigger_in(3) 106 select logic_trigger_in(4) 107 select logic_trigger_in(5) 108 select logic_trigger_in(6) 109 select logic_trigger_in(7) 110 select logic_trigger_in(8) 111 select logic_trigger_in(9) 112 select logic_trigger_in(10) 113 select logic_trigger_in(11) 114 select logic_trigger_in(12) 115 select logic_trigger_in(13) 116 select logic_trigger_in(14) 117 select logic_trigger_in(15) -- CORE TRIGGERS (EP chip only) -- **Note**: set core_slave_mode to honor ec[0:5]_tc_trace_run 118 select core trigger 0: any rising edge of ec[0:5]_tc_trace_run(0) 119 select core trigger 1: any rising edge of ec[0:5]_tc_trace_run(1) 120 select core trigger 2: any falling edge of ec[0:5]_tc_trace_run(0) 121 select core trigger 3: any falling edge of ec[0:5]_tc_trace_run(1) -- BROADCAST / ERRORS 122 select glb_trc_bdcst_recv (received global broadcast) 123 select edge detected fir_dbg_xstop_err 124 select edge detected fir_dbg_recov_err 125 select edge detected fir_dbg_spatn 126 ... 127 select constant 0 (unused)
8:15	RW	INST2_COND1_SEL_B: Multiplexer for cond1_trig_in(1). Selection as cond1_trig_in(0).
16:23	RW	INST2_COND2_SEL_A: Multiplexer for cond2_trig_in(0). Selection as cond1_trig_in(0).
24:31	RW	INST2_COND2_SEL_B: Multiplexer for cond2_trig_in(1). Selection as cond1_trig_in(0).
32	RW	INST2_C1_INAROW_MODE: Counter 1 in-a-row mode for front-end instance (or component) 2.
33	RW	INST2_AND_TRIGGER_MODE1: Front-end instance 1 and trigger mode condition1.
34	RW	INST2_NOT_TRIGGER_MODE1: Front-end instance 1 inverted trigger mode condition1.
35	RW	INST2_EDGE_TRIGGER_MODE1: Front-end instance 1 edge trigger mode condition1.
36:38	RWX	INST2_UNUSED_1: Unused.
39	RW	INST2_C2_INAROW_MODE: Counter 2 in-a-row mode for front-end instance (or component) 2.
40	RW	INST2_AND_TRIGGER_MODE2: Front-end instance 1 and trigger mode2.
41	RW	INST2_NOT_TRIGGER_MODE2: Front-end instance 1 inverted (not) trigger.

Bits	SCOM	Field Mnemonic: Description
42	RW	INST2_EDGE_TRIGGER_MODE2: Front-end instance 1 edge trigger.
43:45	RWX	INST2_UNUSED_2: Unused.
46	RW	INST2_COND3_ENABLE_RESET: Front-end instance 1 condition 3 enable.
47	RW	INST2_EXACT_TO_MODE: Front-end instance 1 exact timeout mode.
48	RW	INST2_RESET_C2TIMER_ON_C1: Front-end instance 1 reset condition 2 timer on condition 1.
49	RW	INST2_RESET_C3_ON_C0: Front-end instance 1 reset condition 3 on condition 0.
50	RW	INST2_SLOW_TO_MODE: Front-end instance 1 slow timeout mode.
51	RW	INST2_EXACT_RESET_C3_ON_TO: Front-end instance 1 exact reset condition 3 on timeout.
52:55	RW	INST2_C1_COUNT_LT: Instance 2 condition 1 counter compare value.
56:59	RW	INST2_C2_COUNT_LT: Instance 2 condition 2 counter compare value.
60:62	RW	INST2_RESET_C3_SELECT: Front-end instance 1, reset condition 3 for reset_c3_on_c0: 100 = dbg_cross_couple_triggers(4). 101 = dbg_cross_couple_triggers(12). 110 = dbg_cross_couple_triggers(20). 111 = dbg_cross_couple_triggers(28).

Register Name	**Debug Instance 2 Condition 2 Register**
Mnemonic	TP.TCMC01.MCSLOW.EPS.DBG.DBG_INST2_COND_REG_2
Address	00000000070107C5 (SCOM)
Description	This is debug macro configuration register 2 for the front-end 1 component.

Bits	SCOM	Field Mnemonic: Description
0:4	RW	INST2_CROSS_COUPLE_SELECT_1_A: Cross coupling is the same for all selectors: 00000 selects inst2_cond1_trig_a 00001 selects inst2_cond1_trig_b 00010 selects inst2_cond2_trig_a 00011 selects inst2_cond2_trig_b 00100 selects inst2_condition1 00101 selects inst2_condition2 00110 selects inst2_condition3 00111 selects inst2_cond2_timeout 01000 selects inst2_cond1_trig_a 01001 selects inst2_cond1_trig_b 01010 selects inst2_cond2_trig_a 01011 selects inst2_cond2_trig_b 01100 selects inst2_condition1 01101 selects inst2_condition2 01110 selects inst2_condition3 01111 selects inst2_cond2_timeout 10000 selects inst3_cond1_trig_a 10001 selects inst3_cond1_trig_b 10010 selects inst3_cond2_trig_a 10011 selects inst3_cond2_trig_b 10100 selects inst3_condition1 10101 selects inst3_condition2 10110 selects inst3_condition3 10111 selects inst3_cond2_timeout 11000 selects inst4_cond1_trig_a 11001 selects inst4_cond1_trig_b 11010 selects inst4_cond2_trig_a 11011 selects inst4_cond2_trig_b 11100 selects inst4_condition1 11101 selects inst4_condition2 11110 selects inst4_condition3 11111 selects inst4_cond2_timeout
5:9	RW	INST2_CROSS_COUPLE_SELECT_1_B: Instance 2 cross couple select 1 b.
10:14	RW	INST2_CROSS_COUPLE_SELECT_2_A: Instance 2 cross couple select 2 a.
15:19	RW	INST2_CROSS_COUPLE_SELECT_2_B: Instance 2 cross couple select 2 b.
20:43	RW	INST2_TO_CMP_LT: Compare value for special counter sp_cnt_lt in debug component 2.
44	RW	INST2_FORCE_TEST_MODE: Force test mode to indicate to compare without actual compare.

Register Name	**Debug Instance 2 Condition 3 Register**
Mnemonic	TP.TCMC01.MCSLOW.EPS.DBG.DBG_INST2_COND_REG_3
Address	00000000070107C6 (SCOM)
Description	This is debug macro configuration register 3 for the front-end 1 component.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	INST2_SP_COUNT_LT: Timeout counter to_cmp compare value for dbg_cond_comp_1.

Register Name	Debug Trace 0 Register
Mnemonic	TP.TCMC01.MCSLOW.EPS.DBG.DBG_TRACE_REG_0
Address	00000000070107CD (SCOM)
Description	This is debug macro configuration register 0 for the debug back-end component.

Bits	SCOM	Field Mnemonic: Description
0	RW	INST1_COND3_ENABLE: This bit enables instance 1 condition 3.
1	RW	INST2_COND3_ENABLE: This bit enables instance 2 condition 3.
2	RW	INST3_COND3_ENABLE: Unused.
3	RW	INST4_COND3_ENABLE: Unused.
	RW	INST1_SLOW_LFSR_MODE: This bit enables slow LFSR mode for front-end instance 1.
5	RW	INST2_SLOW_LFSR_MODE: This bit enables slow LFSR mode for front-end instance 2.
6	RW	INST3_SLOW_LFSR_MODE: Unused.
7	RW	INST4_SLOW_LFSR_MODE: Unused.
8:9	RW	INST1_CONDITION1_TRIG_SEL: This field selects instance 1 condition 1 for output (external) triggers: 00 = Do nothing 01 = trigger_out(0) 10 = trigger_out(1) 11 = trigger_out(2)
10:11	RW	INST1_CONDITION2_TRIG_SEL: This field selects instance 1 condition 2 for output (external) triggers: 00 = Do nothing 01 = trigger_out(0) 10 = trigger_out(1) 11 = trigger_out(2)
12:13	RW	INST1_C2_TIMEOUT_TRIG_SEL: This field selects instance 1 condition 2 time-out counter for output: (external) triggers: 00 = Do nothing 01 = trigger_out(0) 10 = trigger_out(1) 11 = trigger_out(2)
14:15	RW	INST2_CONDITION1_TRIG_SEL: This field selects instance 2 condition 1 for output (external) triggers: 00 = Do nothing 01 = trigger_out(0) 10 = trigger_out(1) 11 = trigger_out(2)
16:17	RW	INST2_CONDITION2_TRIG_SEL: This field selects instance 2 condition 2 trigger for output (external) triggers: 00 = Do nothing 01 = trigger_out(0) 10 = trigger_out(1) 11 = trigger_out(2)
18:19	RW	INST2_C2_TIMEOUT_TRIG_SEL: This field selects instance 2 condition 2 time-out counter for output (external) triggers: 00 = Do nothing 01 = trigger_out(0) 10 = trigger_out(1) 11 = trigger_out(2)
20:31	RO	Constant = 0b000000000000
32	RW	EXT_TRIG_ON_STOP: This bit enables trigger on stop.

Bits	SCOM	Field Mnemonic: Description
33	RW	EXT_TRIG_ON_FREEZE: This bit enables trigger on freeze.
34:38	RW	CORE_RAS0_TRIG_SEL: This field selects which debug event of the debug front-end components is used for dbg_triggers_out(3) of the debug back-end component. 00001 = inst1_condition1_lt 00010 = inst1_cond2_3_event 00100 = inst1_cond2_timeout 01001 = inst2_condition1_lt 01010 = inst2_cond2_3_event 01100 = inst2_cond2_timeout 10001 = inst3_condition1_lt unused 10010 = inst3_cond2_3_event unused 10100 = inst3_cond2_timeout unused 11001 = inst4_condition1_lt unused 11010 = inst4_cond2_3_event unused 11100 = inst4_cond2_timeout unused
39:43	RW	CORE_RAS1_TRIG_SEL: This field selects which debug event of the debug front-end components is multiplexed to dbg_triggers_out(4) of the debug back-end component ' 00001 = inst1_condition1_lt 00010 = inst1_cond2_3_event 00100 = inst1_cond2_timeout 01001 = inst2_condition1_lt 01010 = inst2_cond2_3_event 01100 = inst2_cond2_timeout 10001 = inst3_condition1_lt unused 10010 = inst3_cond2_3_event unused 10100 = inst3_cond2_timeout unused 11001 = inst4_condition1_lt unused 11010 = inst4_cond2_3_event unused 11100 = inst4_cond2_timeout unused
44:45	RW	PC_TP_TRIG_SEL: This field selects which debug event of the debug front-end components is multiplexed to dbg_triggers_out(5 to 6) of the debug back-end component. 00 = triggers_out_lt(0) & triggers_out_lt(1) 01 = triggers_out_lt(0) & triggers_out_lt(2) 10 = triggers_out_lt(1) & triggers_out_lt(2) 11 = Unused
46:49	RW	DBG_ARM_SEL: This field selects which debug event is multiplexed to dbg_wat_arm (unused). XXXX = don't care, unused.
50:53	RW	TRIG0_LEVEL_SEL: This field selects additional conditions for output (external) trigger signal trigger_out(0). **Note:** Some are N/A (inst3/4 conditions are tied to zero). 0001 = inst1_cond3_state_int(1) 0010 = inst1_cond3_state_int(0) 0011 = inst2_cond3_state_int(1) 0100 = inst2_cond3_state_int(0) 0101 = inst3_cond3_state_int(1) 0110 = inst3_cond3_state_int(0) 0111 = inst4_cond3_state_int(1) 1000 = inst4_cond3_state_int(0) 1001 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) 1010 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1) 1011 = inst3_cond3_state_int(1) or inst4_cond3_state_int(1) 1100 = inst3_cond3_state_int(1) and inst4_cond3_state_int(1) 1101 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1) 1110 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1) and inst3_cond3_state_int(1) 1111 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1) or inst4_cond3_state_int(1)

Bits	SCOM	Field Mnemonic: Description
54:57	RW	TRIG1_LEVEL_SEL: This field selects additional conditions for output (external) trigger signal trigger_out(1). **Note:** Some are N/A (inst3/4 conditions are tied to zero). 0001 = inst1_cond3_state_int(1) 0010 = inst1_cond3_state_int(0) 0011 = inst2_cond3_state_int(1) 0100 = inst2_cond3_state_int(0) 0101 = inst3_cond3_state_int(1) 0110 = inst3_cond3_state_int(0) 0111 = inst4_cond3_state_int(1) 1000 = inst4_cond3_state_int(0) 1001 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) 1010 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1) 1011 = inst3_cond3_state_int(1) or inst4_cond3_state_int(1) 1100 = inst3_cond3_state_int(1) and inst4_cond3_state_int(1) 1101 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1) 1110 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1) and inst3_cond3_state_int(1) 1111 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1) or inst4_cond3_state_int(1)
58:63	RO	Constant = 0b000000

Register Name	**Debug Trace 1 Register**
Mnemonic	TP.TCMC01.MCSLOW.EPS.DBG.DBG_TRACE_REG_1
Address	00000000070107CE (SCOM)
Description	This is debug macro configuration register 1 for the back-end component.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	INST1_CONDITION1_ACTION_DO: Instance 1 action selection, condition 1: 00 = Nothing 01 = Start 10 = Stop 11 = Run-N (start now, stop after N cycles)
2:3	RW	INST1_CONDITION2_ACTION_DO: Instance 1 action selection, condition 2: 00 = Nothing 01 = Start 10 = Stop 11 = Run-N (start now, stop after N cycles)
4:5	RW	INST1_C2_TIMEOUT_ACTION_DO: Instance 1 action selection, c2_timeout: 00 = Nothing 01 = Start 10 = Stop 11 = Run-N (start now, stop after N cycles)
6:7	RW	INST2_CONDITION1_ACTION_DO: Instance 2 action selection, condition 1: 00 = Nothing 01 = Start 10 = Stop 11 = Run-N (start now, stop after N cycles)
8:9	RW	INST2_CONDITION2_ACTION_DO: Instance 2 action selection, condition 2: 00 = Nothing 01 = Start 10 = Stop 11 = Run-N (start now, stop after N cycles)

Bits	SCOM	Field Mnemonic: Description
10:11	RW	INST2_C2_TIMEOUT_ACTION_DO: Instance 2 action selection, c2_timeout: 00 = Nothing 01 = Start 10 = Stop 11 = Run-N (start now, stop after N cycles)
12:23	RO	Constant = 0b000000000000
24	RW	INST1_CONDITION1_ACTION_WAITN: For wait-N.
25	RW	INST1_CONDITION2_ACTION_WAITN: For wait-N.
26	RW	INST1_C2_TIMEOUT_ACTION_WAITN: For wait-N.
27	RW	INST2_CONDITION1_ACTION_WAITN: For wait-N.
28	RW	INST2_CONDITION2_ACTION_WAITN: For wait-N.
29	RW	INST2_C2_TIMEOUT_ACTION_WAITN: For wait-N.
30:35	RO	Constant = 0b000000
36	RW	INST1_CONDITION1_ACTION_BANK: Trace bank switch (instance 1, condition1).
37	RW	INST1_CONDITION2_ACTION_BANK: Trace bank switch (instance 1, condition2).
38	RW	INST1_C2_TIMEOUT_ACTION_BANK: Trace bank switch (instance 1, c2_timeout).
39	RW	INST2_CONDITION1_ACTION_BANK: Trace bank switch (instance 2, condition1).
40	RW	INST2_CONDITION2_ACTION_BANK: Trace bank switch (instance 2, condition2).
41	RW	INST2_C2_TIMEOUT_ACTION_BANK: Trace bank switch (instance 2, c2_timeout).
42:47	RO	Constant = 0b000000
48:50	RW	INST1_CHECKSTOP_MODE_LT: Select an additional condition with fir_error_lt for dbg_fir_xstop_on_trig output: 000 = inst1_condition1_lt 001 = inst1_condition2_lt 010 = inst1_condition3_lt 011 = inst1_cond2_timeout_lt 1XX = Disable checkstop_mode
51	RW	INST1_CHECKSTOP_MODE_SELECTOR: Enable_fir_trig_xstop: Enable a checkstop on the debug trigger: 0 = Disable a checkstop on the debug trigger 1 = Enable a checkstop on the debug trigger
52:54	RW	INST2_CHECKSTOP_MODE_LT: Select an additional condition with fir_error_lt for dbg_fir_xstop_on_trig output: 000 = inst2_condition1_lt 001 = inst2_condition2_lt 010 = inst2_condition3_lt 011 = inst2_cond2_timeout_lt 1XX = Disable checkstop_mode
55	RW	INST2_CHECKSTOP_MODE_SELECTOR: enable_fir_error_xstop: Enable a checkstop on a FIR error: 0 = Disable a checkstop on a FIR error. 1 = Enable a checkstop on a FIR error.
56:63	RO	Constant = 0b00000000

Register Name	Debug Trace Mode 2 Register
Mnemonic	TP.TCMC01.MCSLOW.EPS.DBG.DBG_TRACE_MODE_REG_2
Address	00000000070107CF (SCOM)
Description	This is debug macro configuration register 2 for the back-end component.

Bits	SCOM	Field Mnemonic: Description
0:15	RW	RUNN_COUNT_COMPARE_VALUE: Compare value for the run-N counter used in trace modes run-N and wait-N.
16	RW	IMM_FREEZE_MODE: Immediate freeze mode.
17	RW	STOP_ON_ERR: Stop and freeze on a checkstop.
18	RW	BANK_ON_RUNN_MATCH: Bank switch on run-N match.
19	RW	FORCE_TEST_MODE: Force the run-N condition to be true.
20	RW	ACCUM_HIST_MODE: Accumulate history mode; do not clear history mode when trace_run is active.
21	RW	FRZ_COUNT_ON_FRZ: Freeze condition counters on trace freeze.

Register Name	Debug Trace Control Register
Mnemonic	TP.TCMC01.MCSLOW.EPS.DBG.DEBUG_TRACE_CONTROL
Address	00000000070107D0 (SCOM)
Description	This is the trace start/stop/rest using SCOM command register. This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0	WOX	Reserved.
1	WOX	Reserved.
2	WOX	Reserved.

Register Name	Extra Trace Mode Register
Mnemonic	TP.TCMC01.MCSLOW.EPS.DBG.XTRA_TRACE_MODE
Address	00000000070107D1 (SCOM)
Description	This register provides an extra or dedicated trace mode register for core triggers

Bits	SCOM	Field Mnemonic: Description
0:37	RW	XTRA_TRACE_MODE_DATA: Extra or dedicated trace mode register for core triggers.

Register Name	MBA CAL FIR Register
Mnemonic	MC01.PORT0.SRQ.MBACALFIRQ
Address	0000000007010900 (SCOM) 0000000007010901 (SCOM1) 0000000007010902 (SCOM2)
Description	MBA CAL FIR Register (MBACALFIR)

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	MBACALFIRQ_MBA_RECOVERABLE_ERROR: When set, an MBA recoverable error has occurred. These errors include cal[0:3]_cfg, rrq, wrq, and power control parity errors.
1	RWX	WOX_AND	WOX_OR	MBACALFIRQ_MBA_NONRECOVERABLE_ERROR: When set, an MBA nonrecoverable error has occurred. These errors include dsm, tmr, farb, and SIR parity errors.
2	RWX	WOX_AND	WOX_OR	MBACALFIRQ_REFRESH_OVERRUN: When set, nine refreshes have been enqueued to any single rank.
3	RWX	WOX_AND	WOX_OR	MBACALFIRQ_WAT_ERROR: When set, an error has been detected in the MBA debug WAT logic.
4	RWX	WOX_AND	WOX_OR	MBACALFIRQ_RCD_PARITY_ERROR: When set, an RCD parity error has been detected on DDR port 0. If the error was seen during a calibration, FIR 14 will fire instead.
5	RWX	WOX_AND	WOX_OR	MBACALFIRQ_DDR_CAL_TIMEOUT_ERR: When set, a calibration complete indication was not received in the calibration timeout time for DDR0.
6	RWX	WOX_AND	WOX_OR	MBACALFIRQ_EMERGENCY_THROTTLE: Emergency throttle engaged either due to an OCC request or a deadman timer pop.
7	RWX	WOX_AND	WOX_OR	MBACALFIRQ_DDR_CAL_RESET_TIMEOUT: When set, indicates that a soft reset issued to the DDR PHY did not clear a pending calibration update request.
8	RWX	WOX_AND	WOX_OR	MBACALFIRQ_DDR_MBA_EVENT_N: When set, indicates event_n was active on the DDR interface.
9	RWX	WOX_AND	WOX_OR	MBACALFIRQ_WRQ_RRQ_HANG_ERR: When set, indicates that the WRQ or RRQ is in a hung state.
10	RWX	WOX_AND	WOX_OR	MBACALFIRQ_SM_1HOT_ERR: When set, indicates a state machine one hot error.
11	RWX	WOX_AND	WOX_OR	MBACALFIRQ_ASYNC_IF_ERROR: Sequencer error seen when crossing an asynchronous interface from the MCS.
12	RWX	WOX_AND	WOX_OR	MBACALFIRQ_CMD_PARITY_ERROR: Address parity error seen internal to the sequencer on a read or write command.
13	RWX	WOX_AND	WOX_OR	MBACALFIRQ_PORT_FAIL: The port has failed due to a persistent retry. All reads returned with ab RCD error so that the SUE will be delivered upstream.
14	RWX	WOX_AND	WOX_OR	MBACALFIRQ_RCD_CAL_PARITY_ERROR: When set, an RCD parity error has been detected during a calibration.
15	RWX	WOX_AND	WOX_OR	MBACALFIRQ_INTERNAL_SCOM_ERROR: When set, an internal SCOM error has occurred.
16	RWX	WOX_AND	WOX_OR	MBACALFIRQ_INTERNAL_SCOM_ERROR_COPY: Copy of internal SCOM error.
17:63	RO	RO	RO	Constant = 0b00000000000000000000000000000000000000000000000000000

Register Name	MBA CAL FIR Mask Register (MBACALFIR_MASK)
Mnemonic	MC01.PORT0.SRQ.MBACALFIR_MASK
Address	0000000007010903 (SCOM) 0000000007010904 (SCOM1) 0000000007010905 (SCOM2)
Description	MBA CAL FIR mask register (MBACALFIR_MASK)

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	MBACALFIR_MASK_MBA_RECOVERABLE_ERROR: When set, an MBA recoverable error occurred. These errors include cal[0:3]_cfg, rrq, wrq, and power-control parity errors.
1	RW	WO_AND	WO_OR	MBACALFIR_MASK_MBA_NONRECOVERABLE_ERROR: When set, an MBA nonrecoverable error occurred. These errors include dsm, tmr, farb, and SIR parity errors.
2	RW	WO_AND	WO_OR	MBACALFIR_MASK_REFRESH_OVERRUN: When set, nine refreshes have been enqueued to any single rank.
3	RW	WO_AND	WO_OR	MBACALFIR_MASK_WAT_ERROR: When set, an error has been detected in the MBA debug WAT logic.
4	RW	WO_AND	WO_OR	MBACALFIR_MASK_RCD_PARITY_ERROR: When set, an RCD parity error has been detected on DDR port 0.
5	RW	WO_AND	WO_OR	MBACALFIR_MASK_DDR_CAL_TIMEOUT_ERR: When set, a calibration complete indication was not received in the calibration timeout time for DDR0.
6	RW	WO_AND	WO_OR	MBACALFIR_MASK_EMERGENCY_THROTTLE: Emergency throttle engaged either due to an OCC request or a deadman timer pop.
7	RW	WO_AND	WO_OR	MBACALFIR_MASK_DDR_CAL_RESET_TIMEOUT: When set, indicates that a soft reset issued to the DDR PHY did not clear a pending calibration update request.
8	RW	WO_AND	WO_OR	MBACALFIR_MASK_DDR_MBA_EVENT_N: When set, indicates event_n was active on the DDR interface.
9	RW	WO_AND	WO_OR	MBACALFIR_MASK_WRQ_RRQ_HANG_ERR: When set, indicates that the WRQ or RRQ is in a hung state.
10	RW	WO_AND	WO_OR	MBACALFIR_MASK_SM_1HOT_ERR: When set, indicates a state machine one hot error.
11	RW	WO_AND	WO_OR	MBACALFIR_MASK_ASYNC_IF_ERROR: Sequencer error seen when crossing an asynchronous interface from the MCS.
12	RW	WO_AND	WO_OR	MBACALFIR_MASK_CMD_PARITY_ERROR: Address parity error seen internal to the sequencer on a read or write command.
13	RW	WO_AND	WO_OR	MBACALFIRQ_MASK_PORT_FAIL: The port has failed due to a persistent retry. All reads returned with an RCD error so that the SUE will be delivered upstream.
14	RW	WO_AND	WO_OR	MBACALFIRQ_MASK_RCD_CAL_PARITY_ERROR: When set, an RCD parity error has been detected during a calibration.
15	RW	WO_AND	WO_OR	MBACALFIR_MASK_INTERNAL_SCOM_ERROR: When set, an internal SCOM error has occurred.
16	RW	WO_AND	WO_OR	MBACALFIR_MASK_INTERNAL_SCOM_ERROR_COPY: Copy of internal SCOM error.
17:63	RO	RO	RO	Constant = 0b00000000000000000000000000000000000000000000000000000

Register Name	MBA CAL FIR Action 0 Register
Mnemonic	MC01.PORT0.SRQ.MBACALFIR_ACTION0
Address	0000000007010906 (SCOM)
Description	MBA CAL FIR Action 0 Register (MBACALFIR_ACTION0)

Bits	SCOM	Field Mnemonic: Description
0:16	RW	MBACALFIR_ACTION0_FIR_ACTION0: MBA action0 select for the corresponding bit in the FIR. (Action0, Action1, Mask) = Action Select: (0,0,X) = No error reported (0,1,0) = Recoverable error (1,0,0) = Checkstop error (1,1,0) = Local core checkstop freeze (X,X,1) = Masked
17:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000

Register Name	MBA CAL FIR Action 1 Register
Mnemonic	MC01.PORT0.SRQ.MBACALFIR_ACTION1
Address	0000000007010907 (SCOM)
Description	MBA CAL FIR Action 1 Register (MBACALFIR_ACTION1)

Bits	SCOM	Field Mnemonic: Description
0:16	RW	MBACALFIR_ACTION1_FIR_ACTION1: MBA action1 select for the corresponding bit in the FIR. (Action0, Action1, Mask) equals Action Select: (0,0,X) = No error reported (0,1,0) = Recoverable error (1,0,0) = Checkstop error (1,1,0) = Local core checkstop freeze (X,X,1) = Masked
17:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000

Register Name	Data State Machine Configuration Register
Mnemonic	MC01.PORT0.SRQ.MBA_DSM0Q
Address	000000000701090A (SCOM)
Description	Data state machine configurations

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MBA_DSM0Q_CFG_RODT_START_DLY: Delay from the read command to ODT turn on.
6:11	RW	MBA_DSM0Q_CFG_RODT_END_DLY: Delay from the read command to ODT turn off.
12:17	RW	MBA_DSM0Q_CFG_WODT_START_DLY: Delay from the write command to ODT turn on.
18:23	RW	MBA_DSM0Q_CFG_WODT_END_DLY: Delay from the write command to ODT turn off.
24:29	RW	MBA_DSM0Q_CFG_WRDONE_DLY: Delay from the write command to write done to MBS.
30:35	RW	MBA_DSM0Q_CFG_WRDATA_DLY: Delay from the write command to stating the write data flow.
36:41	RW	MBA_DSM0Q_CFG_RDTAG_DLY: Delay from the read command to rd data valid back to MBS.

Bits	SCOM	Field Mnemonic: Description
42	RW	MBA_DSM0Q_CFG_RDTAG_MBX_CYCLE: Determines the memory clock 1/2 cycle that the rdtag entry is released from the DSM queue: 0 = Release when the MBX clock is low. 1 = Release when the MBX clock is high.
43:48	RW	MBA_DSM0Q_CFG_RODT_BC4_END_DLY: Delay from the read command to ODT turn off for the BC4 command.
49:54	RW	MBA_DSM0Q_CFG_WODT_BC4_END_DLY: Delay from the write command to ODT turn off for the BC4 command.
55:63	RW	MBA_DSM0Q_RESERVED_55_63: Reserved.

Register Name	DDR Data Bus Timing Parameters Register
Mnemonic	MC01.PORT0.SRQ.MBA_TMR0Q
Address	000000000701090B (SCOM)
Description	DDR data bus timing parameters

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MBA_TMR0Q_RRDM_DLY: Read to Read to different master.
4:7	RW	MBA_TMR0Q_RRSMSR_DLY: Read to Read same master, same rank.
8:11	RW	MBA_TMR0Q_RRSMDR_DLY: Read to Read same master, different rank.
12:15	RW	MBA_TMR0Q_RROP_DLY: Read open page to read delay.
16:19	RW	MBA_TMR0Q_WWDM_DLY: Write to Write different master.
20:23	RW	MBA_TMR0Q_WWSMSR_DLY: Write to Write same master, same rank.
24:27	RW	MBA_TMR0Q_WWSMDR_DLY: Write to Write same master, different rank.
28:31	RW	MBA_TMR0Q_WWOP_DLY: Write open page to write delay.
32:36	RW	MBA_TMR0Q_RWDM_DLY: Read to Write different master.
37:41	RW	MBA_TMR0Q_RWSMSR_DLY: Read to Write same master, same rank.
42:46	RW	MBA_TMR0Q_RWSMDR_DLY: Read to Write same master, different rank.
47:50	RW	MBA_TMR0Q_WRDM_DLY: Write to Read different master.
51:56	RW	MBA_TMR0Q_WRSMSR_DLY: Write to read same master, same rank.
57:62	RW	MBA_TMR0Q_WRSMDR_DLY: Write to read same master, different rank.
63	RW	MBA_TMR0Q_RESERVED_63: Reserved.

Register Name	DDR Bank Busy Parameters Register
Mnemonic	MC01.PORT0.SRQ.MBA_TMR1Q
Address	000000000701090C (SCOM)
Description	DDR bank busy parameters

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MBA_TMR1Q_RRSBG_DLY: Read to read same bank group.
4:9	RW	MBA_TMR1Q_WRSBG_DLY: Write to read same bank group.

Bits	SCOM	Field Mnemonic: Description
10:15	RW	MBA_TMR1Q_CFG_TFAW: Four activate window time.
16:20	RW	MBA_TMR1Q_CFG_TRCD: RAS to CAS delay.
21:25	RW	MBA_TMR1Q_CFG_TRP: Precharge to activate delay.
26:31	RW	MBA_TMR1Q_CFG_TRAS: Activate to precharge delay.
32:40	RW	MBA_TMR1Q_RESERVED_32_40: Reserved.
41:47	RW	MBA_TMR1Q_CFG_WR2PRE: Write to precharge delay.
48:51	RW	MBA_TMR1Q_CFG_RD2PRE: Read to precharge delay.
52:55	RW	MBA_TMR1Q_TRRD: Activate to activate delay.
56:59	RW	MBA_TMR1Q_TRRD_SBG: Activate to activate same bank group delay.
60:63	RW	MBA_TMR1Q_CFG_ACT_TO_DIFF_RANK_DLY: Activate to activate different rank delay.

Register Name	DDR Write Command Parameters Register
Mnemonic	MC01.PORT0.SRQ.MBA_WRQ0Q
Address	000000000701090D (SCOM)
Description	DDR write command parameters

Bits	SCOM	Field Mnemonic: Description
0:4	RW	MBA_WRQ0Q_CFG_WRITE_HW_MARK: Write high-water mark (force writes HPenables writes).
5	RW	MBA_WRQ0Q_CFG_WRQ_FIFO_MODE: Prevent reordering in the WRQ (only entry0 can be selected). HP cleaner writes are not selected until they are in entry 0.
6	RW	MBA_WRQ0Q_CFG_DISABLE_WR_PG_MODE: Disable page commands for the WRQ.
7:18	RW	MBA_WRQ0Q_CFG_WRQ_ENTRY0_HP_DLY: Time for entry0 of the WRQ before it forces HP setting this dial to a 0; will disable entry0 HP.
19	RW	MBA_WRQ0Q_CFG_WRQ_FLUSH_WR_RANK: When one write is issued to a rank, try to force more writes to that rank to avoid multiple write to read same rank penalties.
20	RW	MBA_WRQ0Q_CFG_WRQ_ENABLE_NON_HP_WR: Allow writes when they do not meet a condition such as entry0_flush or rd_idle_allow_wr.
21:32	RW	MBA_WRQ0Q_CFG_ENTRY0_MIN_FOR_RRQ_IDLE_WR: This is an added condition to allow writes when the RRQ is idle. This addition allows for multiple writes to stack up in the WRQ before starting the write burst.
33:37	RW	MBA_WRQ0Q_CFG_WRITE_LW_MARK: Write low-water mark. After write high priority has been asserted due to the writes exceeding the programmed high-water mark, write priority remains asserted until the write low-water mark is reached. Set to 8. If there are more then eight entries in the WRQ, the condition allows writes when the rrq_idle period is met.
38:43	RW	MBA_WRQ0Q_CFG_WRQ_SKIP_LIMIT: The number of times entry0 of the WRQ can be skipped before entry0 prevents older writes from being issued until entry0 is sent.
44	RW	MBA_WRQ0Q_CFG_WRQ_SINGLE_THREAD_MODE: WRQ wrq_single thread mode setting. This ensures that all reads are issued one at a time. With this mode set, we only issue from the bottom entry in the WRQ, and we will not issue an activate for the subsequent operation until the prior write is sent.
45:52	RW	MBA_WRQ0Q_CFG_RQ_HANG_THRESHOLD: Hang detection for entry0 of the reorder queue. A counter increments every mcbist_srq_hang_pulse (2048 phase hold cycles). It sets a FIR when the count = threshold and another pulse is received. Since this checks for count = threshold, a value of 0 is not valid.
53:54	RW	MBA_WRQ0Q_RESERVED_53_54: Reserved.

Bits	SCOM	Field Mnemonic: Description
55:58	RW	MBA_WRQ0Q_CFG_WRQ_ACT_NUM_WRITES_PENDING: Limit on the number of write-activates when doing writes. When the sequencer is serving writes, no new activates are sent out as long as at least this number of writes are pending to already-activated pages. A setting of 0 sets no cap on the number of activates.
59:63	RW	.MBA_WRQ0Q_RESERVED_59_63: Reserved.

Register Name	DDR Read Command Parameters Register
Mnemonic	MC01.PORT0.SRQ.MBA_RRQ0Q
Address	000000000701090E (SCOM)
Description	DDR read command parameters

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MBA_RRQ0Q_CFG_RRQ_SKIP_LIMIT: Number of times the bottom entry in the RRQ can be skipped before preventing the entry from being skipped
6	RW	MBA_RRQ0Q_CFG_RRQ_FIFO_MODE: RRQ FIFO mode setting. This ensures that all reads go out in the order they were received. It still allows multiple operations to be pipelined to allow for decent throughput. This needs to be set for MCBIST dgen mode.
7	RW	MBA_RRQ0Q_CFG_RRQ_SINGLE_THREAD_MODE: RRQ single thread mode. Setting this ensures that all reads are issued one at a time. With this mode set, we only issue from the bottom entry in the RRQ, and we do not issue an activate for the subsequent operation until the prior read is sent.
8:10	RW	MBA_RRQ0Q_RESERVED_8_10: Reserved.
11	RW	MBA_RRQ0Q_CFG_DISABLE_RD_PG_MODE: Disable page commands for the RRQ.
12	RW	MBA_RRQ0Q_CFG_DISABLE_FAST_PATH: Disable MBA RRQ fastpath.
13:23	RW	MBA_RRQ0Q_CFG_RD_IDLE_ALLOW_WR: Time with an empty RRQ before writes are enabled.
24:29	RW	MBA_RRQ0Q_CFG_RDBUFF_CAPACITY_LIMIT: Number of 64-byte read buffers that the sequencer is allowed to use concurrently.
30:36	RW	MBA_RRQ0Q_CFG_RMWBUFF_CAPACITY_LIMIT: Number of 64-byte read-modify-write buffers that the sequencer is allowed to use concurrently.
37:56	RW	MBA_RRQ0Q_RESERVED_37_56: Reserved.
57:60	RW	MBA_RRQ0Q_CFG_RRQ_ACT_NUM_READS_PENDING: Limit on the number of read-activates when doing reads. When the sequencer is serving reads, no new activates are sent out as long as at least this number of reads are pending to already-activated pages. A setting of 0 sets no cap on the number of activates.
61	RW	MBA_RRQ0Q_CFG_INJ_CANCEL_ACK_ERR: Inject error on cancel-ack asynchronous interface.
62	RW	MBA_RRQ0Q_CFG_RRQ_ENTRY0_ENABLE: Enable entry0 timer for RRQ.
63	RW	MBA_RRQ0Q_RESERVED_63: Reserved.

Register Name	DDR Calibration Register
Mnemonic	MC01.PORT0.SRQ.MBA_CAL0Q
Address	000000000701090F (SCOM)
Description	DDR Calibration registers

Bits	SCOM	Field Mnemonic: Description
0	RW	MBA_CAL0Q_CFG_CAL_INTERVAL_TMR0_ENABLE: Enable interval tmr0.
1:2	RW	MBA_CAL0Q_CFG_TIME_BASE_TMR0: Time base for interval tmr0 counter.
3:11	RW	MBA_CAL0Q_CFG_INTERVAL_COUNTER_TMR0: Interval timer based on time_base(time_base × interval_counter).
12	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL1_ENABLE: Enable this bit for the first calibration to perform when the timer pops. Should always be 1 if the timer is enabled.
13:16	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL1_TYPE: 10XX = Internal ZQ calibration (cal_rank ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step. 0011 = Periodic calibration: Run SysClk, DQS, and read eye all in parallel (default behavior).
17	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL1_DDR_DONE: Use the complete signal from the DDR for cal1.
18	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL2_ENABLE: Enable bit for a second calibration to perform when the timer pops.
19:22	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL2_TYPE: 10XX = Internal ZQ calibration (cal_rank ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step. 0011 = Periodic calibration: Run SysClk, DQS, and read eye all in parallel (default behavior).
23	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL2_DDR_DONE: Use the complete signal from the DDR for cal2.
24	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL3_ENABLE: Enable bit for a third calibration to perform when the timer pops.
25:28	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL3_TYPE: 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step. 0011 = Periodic calibration: Run SysClk, DQS, and read eye all in parallel (default behavior).
29	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL3_DDR_DONE: Use the complete signal from the DDR for cal3.
30:38	RW	MBA_CAL0Q_CFG_CAL_TMR0_Z_SYNC: The timer value is set to this value during z sync.
39:46	RW	MBA_CAL0Q_CFG_CAL_TMR0_DDR_RESET_TMR: Wait time for the DDR soft reset upon calibration timeout fail.
47:48	RW	MBA_CAL0Q_CFG_CAL_TMR0_DDR_RESET_TMR_TB: Timebase interval for the ddr_reset_tmr.
49	RW	MBA_CAL0Q_CFG_CAL_TMR0_DDR_RESET_ENABLE: Enable DDR soft reset upon calibration timeout fail. 0 = Do not issue a soft DDR reset upon calibration timeout. 1 = Issue a DDR soft reset upon calibration timeout.
50	RW	MBA_CAL0Q_CFG_CAL_TMR0_SINGLE_RANK: Enable single-rank mode for timer0 calibrations. Calibrations programmed in tmr0 run on one rank at a time per timer expiration. 0 = Issue calibrations for all enabled ranks per timer expiration. 1 = Issue calibrations for one rank at a time per timer expiration.
51	RW	MBA_CAL0Q_RESERVED_51: Reserved.
52	RW	MBA_CAL0Q_INJECT_1HOT_SM_ERROR: Setting to this bit to 1 injects one 1hot sm error. Must be set to 0 and then 1 again to inject another error. 0 = No error inject. 1 = Inject one 1hot sm error.

Bits	SCOM	Field Mnemonic: Description
53:55	RW	MBA_CAL0Q_CFG_CAL_SINGLE_PORT_MODE: Single port mode configuration. The default is that both ports are calibrated at the same time. The options are: • Single port calibrated at a time with both ports powered up. • Single port calibrated at a time with one port powered up. • Single port calibrated at a time with one port powered up. • Only the rank requested by the DDR PHY powered up. Only to be used in single rank mode.
56	RW	MBA_CAL0Q_DBG_BUS_BIT: Debug bus bit.
57	RW	MBA_CAL0Q_RESET_RECOVER: DDR reset recover.
58	RW	MBA_CAL0Q_CFG_RANK_SM_STALL_DISABLE: When enabled, require a minimum 1K cycle stall between all new calibration timer starts.
59	RW	MBA_CAL0Q_CFG_ENABLE_SPEC_ATTN: Allow FIR attention to cause spec attn.
60	RW	MBA_CAL0Q_CFG_ENABLE_HOST_ATTN: Allow FIR attention to cause host attn.
61:63	RW	MBA_CAL0Q_RESERVED_61_63: Reserved.

Register Name	DDR Calibration Register
Mnemonic	MC01.PORT0.SRQ.MBA_CAL1Q
Address	0000000007010910 (SCOM)
Description	DDR calibration registers

Bits	SCOM	Field Mnemonic: Description
0	RW	MBA_CAL1Q_CFG_CAL_INTERVAL_TMR1_ENABLE: Enable interval tmr1.
1:2	RW	MBA_CAL1Q_CFG_TIME_BASE_TMR1: Time base for interval tmr1 counter.
3:11	RW	MBA_CAL1Q_CFG_INTERVAL_COUNTER_TMR1: Interval timer based on time_base(time_base × interval_counter).
12	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL1_ENABLE: Enable bit for the first calibration to perform when the timer pops. It should always be 1 if the timer is enabled.
13:16	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL1_TYPE: 10XX = Internal ZQ calibration (cal_rank is ignored). 01XX = External ZQ calibration. The requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step. 0011 = Periodic calibration: Run SysClk, DQS, and read eye all in parallel (default behavior).
17	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL1_DDR_DONE: Use the complete signal from the DDR for cal1.
18	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL2_ENABLE: Enable bit for the second calibration to perform when the timer pops.
19:22	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL2_TYPE: 10XX = Internal ZQ calibration (cal_rank is ignored). 01XX = External ZQ calibration. The requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step. 0011 = Periodic calibration: Run SysClk, DQS, and read eye all in parallel (default behavior).
23	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL2_DDR_DONE: Use the complete signal from the DDR for cal2.

Bits	SCOM	Field Mnemonic: Description
24	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL3_ENABLE: Enable bit for the third calibration to perform when the timer pops.
25:28	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL3_TYPE: 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step. 0011 = Periodic calibration: Run SysClk, DQS, and read eye all in parallel (default behavior).
29	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL3_DDR_DONE: Use the complete signal from the DDR for cal3.
30:38	RW	MBA_CAL1Q_CFG_CAL_TMR1_Z_SYNC: The timer value will be set to this value during z sync.
39	RW	MBA_CAL1Q_CFG_CAL_TMR1_SINGLE_RANK: Enable single-rank mode for timer1 calibrations. Calibrations programmed in tmr1 will run on one rank at a time per timer expiration. 0 = Issue calibrations for all enabled ranks per timer expiration. 1 = Issue calibrations for one rank at a time per timer expiration.
40:47	RW	MBA_CAL1Q_CFG_CAL_RANK_ENABLE: Cal rank enable.
48:63	RW	MBA_CAL1Q_RESERVED_48_63: Reserved.

Register Name	DDR Calibration Register
Mnemonic	MC01.PORT0.SRQ.MBA_CAL2Q
Address	0000000007010911 (SCOM)
Description	DDR calibration registers

Bits	SCOM	Field Mnemonic: Description
0	RW	MBA_CAL2Q_CFG_CAL_INTERVAL_TMR2_ENABLE: Enable interval tmr2.
1:2	RW	MBA_CAL2Q_CFG_TIME_BASE_TMR2: Time base for the interval tmr2 counter.
3:11	RW	MBA_CAL2Q_CFG_INTERVAL_COUNTER_TMR2: Interval timer based on time_base(time_base × interval_counter).
12	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL1_ENABLE: Enable bit for the first calibration to perform when the timer pops. It should always be 1 if the timer is enabled.
13:16	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL1_TYPE: 10XX = Internal ZQ calibration (cal_rank ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step. 0011 = Periodic calibration: Run SysClk, DQS, and read eye all in parallel (default behavior).
17	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL1_DDR_DONE: Use the complete signal from the DDR for cal1.
18	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL2_ENABLE: Enable bit for the second calibration to perform when the timer pops.
19:22	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL2_TYPE: 10XX = Internal ZQ calibration (cal_rank ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step. 0011 = Periodic calibration: Run SysClk, DQS and read eye all in parallel (default behavior).
23	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL2_DDR_DONE: Use the complete signal from the DDR for cal2.

Bits	SCOM	Field Mnemonic: Description
24	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL3_ENABLE: Enable bit for the third calibration to perform when the timer pops.
25:28	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL3_TYPE: 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step. 0011 = Periodic calibration: Run SysClk, DQS, and read eye all in parallel (default behavior).
29	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL3_DDR_DONE: Use the complete signal from the DDR for cal3.
30:38	RW	MBA_CAL2Q_CFG_CAL_TMR2_Z_SYNC: The timer value will be set to this value during z sync.
39	RW	MBA_CAL2Q_CFG_CAL_TMR2_SINGLE_RANK: Enable single-rank mode for timer2 calibrations. Calibrations programmed in tmr2 will run on one rank at a time per timer expiration. 0 = Issue calibrations for all enabled ranks per timer expiration. 1 = Issue calibrations for one rank at a time per timer expiration.
40	RW	MBA_CAL2Q_CFG_CAL_TMR2_WAT_EVENT_ENABLE: Enable the use of tmr2 to trigger a WAT event. No other calibrations should be enabled. Must be used with the HW221617 CKSW enabled.
41:63	RW	MBA_CAL2Q_RESERVED_41_63: Reserved.

Register Name	DDR Calibration Length Register
Mnemonic	MC01.PORT0.SRQ.MBA_CAL3Q
Address	0000000007010912 (SCOM)
Description	DDR calibration length registers

Bits	SCOM	Field Mnemonic: Description
0:1	RW	MBA_CAL3Q_CFG_INTERNAL_ZQ_TB: Internal ZQ time base. Time base for the internal ZQ cal counter.
2:9	RW	MBA_CAL3Q_CFG_INTERNAL_ZQ_LENGTH: Number of internal ZQ time bases required to meet the maximum internal ZQ length.
10:11	RW	MBA_CAL3Q_CFG_EXTERNAL_ZQ_TB: External ZQ time base. Time base for the external ZQ cal counter.
12:19	RW	MBA_CAL3Q_CFG_EXTERNAL_ZQ_LENGTH: Number of external ZQ time bases required to meet the maximum external ZQ length
20:21	RW	MBA_CAL3Q_CFG_RDCLK_SYSCLK_TB: ReadclkSysclk time base. Time base for the readclksysclk cal counter.
22:29	RW	MBA_CAL3Q_CFG_RDCLK_SYSCLK_LENGTH: Number of Readclksysclk time bases required to meet the maximum rdclk length.
30:31	RW	MBA_CAL3Q_CFG_DQS_ALIGNMENT_TB: DQS alignment time base. Time base for the DQS alignment cal counter.
32:39	RW	MBA_CAL3Q_CFG_DQS_ALIGNMENT_LENGTH: Number of DQS alignment time bases required to meet maximum DQS alignment length.
40:41	RW	MBA_CAL3Q_CFG_MPR_READEYE_TB: Readeye time base. Time base for the readeye cal counter.
42:49	RW	MBA_CAL3Q_CFG_MPR_READEYE_LENGTH: Number of readeye time bases required to meet the maximum external ZQ length.
50:51	RW	MBA_CAL3Q_CFG_ALL_PERIODIC_TB: All periodics time base. Time base for all periodic cal counters.
52:59	RW	MBA_CAL3Q_CFG_ALL_PERIODIC_LENGTH: Number of all_periodic time bases required to meet the maximum calibration length for all periodic calibration (in parallel).

Bits	SCOM	Field Mnemonic: Description
60	RW	MBA_CAL3Q_CFG_FREEZE_ON_PARITY_ERROR_DIS: Disable freezing MBA execution when a parity error is detected.
61:63	RW	MBA_CAL3Q_RESERVED_61_63: Reserved.

Register Name	Final ARB Parameters Register
Mnemonic	MC01.PORT0.SRQ.MBA_FARB0Q
Address	0000000007010913 (SCOM)
Description	Final ARB parameters

Bits	SCOM	Field Mnemonic: Description
0:15	RW	MBA_FARB0Q_CFG_MISR_BLOCK: When a bit is set, an area of logic is not included in the z-sync MISR computation. Each bit independently gates (blocks) that area of logic from the MISR. Bit 0 Gate refresh pulse. Bits 1 - 3 Gate cal timers 0 - 2. bit 4 Gate nm pulse. Bits 5 - 8 Gate MCBIST tb pulses. Bits 9 - 15 Gate farb requests.
16	RW	MBA_FARB0Q_CFG_MISR_FEEDBACK_ENABLE: Allow the z-sync MISR to use circular feedback and retain the state beyond its 10-latch pipe.
17	RW	MBA_FARB0Q_CFG_2N_ADDR: Enable 2N/2T address mode.
18:19	RW	MBA_FARB0Q_RESERVED_18_19: Reserved.
20:23	RW	MBA_FARB0Q_CFG_ACT_SAME_RANK_HOLD_TIME: Time after activate to prefer subsequent activates to the same rank.
24:30	RW	MBA_FARB0Q_CFG_MAX_READS_IN_A_ROW: Limits the maximum number of reads in a row, before forcing a write. There must be a write in the WRQ for the counting to start. 0x00 = Disabled. 0x01 = 1 read before allowing a write. 0x7F = 127 reads before forcing a write.
31:37	RW	MBA_FARB0Q_CFG_MAX_WRITES_IN_A_ROW: Limits the maximum number of writes in a row, before forcing a read. There must be a read in the RRQ for the counting to start. 0x00 = Disabled. 0x01 = 1 write before allowing a read. 0x7F = 127 writes before forcing a read.
38	RW	MBA_FARB0Q_CFG_PARITY_AFTER_CMD: Determines whether OE is driven on the parity cycle. 0 = OE will not be driven on the parity cycle. 1 = OE will be driven on the parity cycle.
39	RWX	MBA_FARB0Q_CFG_INJECT_PARITY_ERR_WEN: Inject a parity error on WEN on the next CAS.
40	RWX	MBA_FARB0Q_CFG_INJECT_PARITY_ERR_ADDR5: Inject a parity error on ADDR5 on the next CAS.
41:42	RWX	MBA_FARB0Q_CFG_BW_WINDOW_SIZE: For optional size reads: 00 = Determine BW over a 1K cycle window. 01 = Determine BW over a 2K cycle window. 10 = Determine BW over a 4K cycle window. 11 = Determine BW over a 8K cycle window.
43:47	RW	MBA_FARB0Q_CFG_PARITY_DETECT_TIME: Measures the time from an injected error until when the error is detected back at the MBA.
48:53	RW	MBA_FARB0Q_CFG_RCD_PROTECTION_TIME: Time interval in which commands were sent out before an RCD parity error occurrence that should be re-issued. Should be set ≥ to cfg_parity_detect_time.
54	RW	MBA_FARB0Q_CFG_DISABLE_RCD_RECOVERY: Disable the RCD recovery procedure.

Bits	SCOM	Field Mnemonic: Description
55	RW	MBA_FARB0Q_CFG_OE_ALWAYS_ON: Force the DDR OE to always be on (never tristate the DDR address drivers).
56	RW	MBA_FARB0Q_CFG_FARB_CLOSE_ALL_PAGES: Before switching direction on the DRAM bus, require all committed accesses to be issued to any open pages. When set, no new activates can be issued for reads until all writes to open pages are sent. No new activates can be issued for writes until all reads to open pages are issued.
57	RW	MBA_FARB0Q_CFG_PORT_FAIL_DISABLE: Disable port fail after recurring RCD errors.
58	RW	MBA_FARB0Q_CFG_OE_ALL_CKE_POWERED_DOWN: Only precisely turn off cmd-addr output enable after all CKEs are powered down.
59	RW	MBA_FARB0Q_CFG_INJECT_PARITY_ERR_CONSTANT: If set, parity errors are injected continuously; otherwise, parity errors are injected only once.
60	RW	MBA_FARB0Q_CFG_FINISH_WR_BEFORE_RD: This is to prevent writes from holding up banks for a long period of time. If set, all committed writes must be issued before reads can proceed.
61:63	RW	MBA_FARB0Q_CFG_OPT_RD_SIZE: For optional size reads: 000 = Treat all 64-byte/128-byte-opt reads as 64-byte reads. 001 = Treat all 64-byte/128-byte-opt reads as 128-byte reads. 010 = If DRAM data bus utilization is greater than 50%, do optional-size reads as 64 bytes. 011 = If DRAM data bus utilization is greater than 62.5%, do optional-size reads as 64 bytes. 100 = If DRAM data bus utilization is greater than 75.0%, do optional-size reads as 64 bytes. 101 = If DRAM data bus utilization is greater than 87.5%, do optional-size reads as 64 bytes. 11X = Reserved.

Register Name	Final ARB Parameters Register
Mnemonic	MC01.PORT0.SRQ.MBA_FARB1Q
Address	0000000007010914 (SCOM)
Description	Final ARB parameters

Bits	SCOM	Field Mnemonic: Description
0:2	RW	MBA_FARB1Q_CFG_SLOT0_S0_CID: Chip ID bits for Slot 0 Master 0/1 Slave 0.
3:5	RW	MBA_FARB1Q_CFG_SLOT0_S1_CID: Chip ID bits for Slot 0 Master 0/1 Slave 1.
6:8	RW	MBA_FARB1Q_CFG_SLOT0_S2_CID: Chip ID bits for Slot 0 Master 0/1 Slave 2.
9:11	RW	MBA_FARB1Q_CFG_SLOT0_S3_CID: Chip ID bits for Slot 0 Master 0/1 Slave 3.
12:14	RW	MBA_FARB1Q_CFG_SLOT0_S4_CID: Chip ID bits for Slot 0 Master 0/1 Slave 4 or Chip ID bits for Slot 0 Master 2/3 Slave 0.
15:17	RW	MBA_FARB1Q_CFG_SLOT0_S5_CID: Chip ID bits for Slot 0 Master 0/1 Slave 5 or Chip ID bits for Slot 0 Master 2/3 Slave 1.
18:20	RW	MBA_FARB1Q_CFG_SLOT0_S6_CID: Chip ID bits for Slot 0 Master 0/1 Slave 6 or Chip ID bits for Slot 0 Master 2/3 Slave 2.
21:23	RW	MBA_FARB1Q_CFG_SLOT0_S7_CID: Chip ID bits for Slot 0 Master 0/1 Slave 7 or Chip ID bits for Slot 0 Master 2/3 Slave 3.
24:26	RW	MBA_FARB1Q_CFG_SLOT1_S0_CID: Chip ID bits for Slot 1 Master 0/1 Slave 0.
27:29	RW	MBA_FARB1Q_CFG_SLOT1_S1_CID: Chip ID bits for Slot 1 Master 0/1 Slave 1.
30:32	RW	MBA_FARB1Q_CFG_SLOT1_S2_CID: Chip ID bits for Slot 1 Master 0/1 Slave 2.
33:35	RW	MBA_FARB1Q_CFG_SLOT1_S3_CID: Chip ID bits for Slot 1 Master 0/1 Slave 3.

Bits	SCOM	Field Mnemonic: Description
36:38	RW	MBA_FARB1Q_CFG_SLOT1_S4_CID: Chip ID bits for Slot 1 Master 0/1 Slave 4 or Chip ID bits for Slot 1 Master 2/3 Slave 0.
39:41	RW	MBA_FARB1Q_CFG_SLOT1_S5_CID: Chip ID bits for Slot 1 Master 0/1 Slave 5 or Chip ID bits for Slot 1 Master 2/3 Slave 1.
42:44	RW	MBA_FARB1Q_CFG_SLOT1_S6_CID: Chip ID bits for Slot 1 Master 0/1 Slave 6 or Chip ID bits for Slot 1 Master 2/3 Slave 2.
45:47	RW	MBA_FARB1Q_CFG_SLOT1_S7_CID: Chip ID bits for Slot 1 Master 0/1 Slave 7 or Chip ID bits for Slot 1 Master 2/3 Slave 3.
48	RW	MBA_FARB1Q_CFG_DIS_SMDR: Set to 1 if using a 5D configuration. This uses the different master parameters instead of the SMDR.
49	RW	MBA_FARB1Q_CFG_DDR4_PARITY_ON_CID_DIS: Exclude CID bits in parity generation for DDR4
50:63	RW	MBA_FARB1Q_CFG_RSV0: Reserved.

Register Name	**Final ARB Parameters Register**
Mnemonic	MC01.PORT0.SRQ.MBA_FARB2Q
Address	0000000007010915 (SCOM)
Description	Final ARB parameters

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MBA_FARB2Q_CFG_RANK0_RD_ODT: ODT bits required for a read Master Rank 0.
4:7	RW	MBA_FARB2Q_CFG_RANK1_RD_ODT: ODT bits required for a read Master Rank 1.
8:11	RW	MBA_FARB2Q_CFG_RANK2_RD_ODT: ODT bits required for a read Master Rank 2.
12:15	RW	MBA_FARB2Q_CFG_RANK3_RD_ODT: ODT bits required for a read Master Rank 3.
16:19	RW	MBA_FARB2Q_CFG_RANK4_RD_ODT: ODT bits required for a read Master Rank 4.
20:23	RW	MBA_FARB2Q_CFG_RANK5_RD_ODT: ODT bits required for a read Master Rank 5.
24:27	RW	MBA_FARB2Q_CFG_RANK6_RD_ODT: ODT bits required for a read Master Rank 6.
28:31	RW	MBA_FARB2Q_CFG_RANK7_RD_ODT: ODT bits required for a read Master Rank 7.
32:35	RW	MBA_FARB2Q_CFG_RANK0_WR_ODT: ODT bits required for a write Master Rank 0.
36:39	RW	MBA_FARB2Q_CFG_RANK1_WR_ODT: ODT bits required for a write Master Rank 1.
40:43	RW	MBA_FARB2Q_CFG_RANK2_WR_ODT: ODT bits required for a write Master Rank 2.
44:47	RW	MBA_FARB2Q_CFG_RANK3_WR_ODT: ODT bits required for a write Master Rank 3.
48:51	RW	MBA_FARB2Q_CFG_RANK4_WR_ODT: ODT bits 4equired for a write Master Rank 4.
52:55	RW	MBA_FARB2Q_CFG_RANK5_WR_ODT: ODT bits required for a write Master Rank 5.
56:59	RW	MBA_FARB2Q_CFG_RANK6_WR_ODT: ODT bits required for a write Master Rank 6.
60:63	RW	MBA_FARB2Q_CFG_RANK7_WR_ODT: ODT bits required for a write Master Rank 7.

Register Name	**N/M Throttling Control Register**
Mnemonic	MC01.PORT0.SRQ.MBA_FARB3Q
Address	0000000007010916 (SCOM)
Description	N/M Throttling Control

Bits	SCOM	Field Mnemonic: Description
0:14	RW	MBA_FARB3Q_CFG_NM_N_PER_SLOT: The N value for the NM throttling across a single slot. The maximum command count that can occur over a time interval M for one slot.
15:30	RW	MBA_FARB3Q_CFG_NM_N_PER_PORT: The N value for the NM throttling across the entire port (both slots). The maximum command count that can occur over a time interval M for the entire port.
31:44	RW	MBA_FARB3Q_CFG_NM_M: The M value for the NM throttling. This counts DRAM clock cycles. Set this to 0 to disable NM throttling.
45:47	RW	MBA_FARB3Q_CFG_NM_RAS_WEIGHT: The increment to be added to the N count each time a RAS is sent.
48:50	RW	MBA_FARB3Q_CFG_NM_CAS_WEIGHT: The increment to be added to the N count each time a CAS is sent.
51	RW	MBA_FARB3Q_RESERVED_51: Reserved.
52	RW	MBA_FARB3Q_RESERVED_52: Reserved.
53	RW	MBA_FARB3Q_CFG_NM_CHANGE_AFTER_SYNC: If set, changes to cfg_nm_n_per_slot. The cfg_nm_n_per_port, cfg_nm_m, min_max_domains will only be applied after a pc_sync command is seen.
54:63	RW	MBA_FARB3Q_RESERVED_54_63: Reserved.

Register Name	Final Command Arbiter Miscellaneous Register
Mnemonic	MC01.PORT0.SRQ.MBA_FARB4Q
Address	0000000007010917 (SCOM)
Description	Final Command arbiter miscellaneous

Bits	SCOM	Field Mnemonic: Description
0:15	RW	MBA_FARB4Q_CFG_NOISE_WAIT_TIME: The time from RCD_err until the RCD error recovery procedure will start issuing precharge commands.
16:21	RW	MBA_FARB4Q_CFG_PRECHARGE_WAIT_TIME: The time from one precharge command to the next precharge command in the RCD error recovery procedure.
22	RW	MBA_FARB4Q_CFG_SIM_FAST_NOISE_WINDOW: This will skip the precharges and refreshes as part of the noise window and only observe the noise window wait time.
23:26	RW	MBA_FARB4Q_RESERVED_23_26: Reserved.
27:41	RW	MBA_FARB4Q_EMERGENCY_N: Programmable N for NM when the emergency throttle is enabled.
42:55	RW	MBA_FARB4Q_EMERGENCY_M: Programmable M for NM when the emergency throttle is enabled.
56:63	RW	MBA_FARB4Q_RESERVED_56_63: Reserved.

Register Name	DDR Interface SCOM Control Register
Mnemonic	MC01.PORT0.SRQ.MBA_FARB5Q
Address	0000000007010918 (SCOM)
Description	DDR interface SCOM control

Bits	SCOM	Field Mnemonic: Description
0:1	RW	MBA_FARB5Q_CFG_DDR_DPHY_NCLK: DDR PHY NCLK control.
2:3	RW	MBA_FARB5Q_CFG_DDR_DPHY_PCLK: DDR PHY PCLK control.
4	RW	MBA_FARB5Q_CFG_DDR_RESETN: DDR Resetn signal.

Bits	SCOM	Field Mnemonic: Description
5	RW	MBA_FARB5Q_CFG_CCS_ADDR_MUX_SEL: CCS Address Mux Sel. This bit must be turned on until all multiple CCS instructions are completed. 0 selects address data from mainline logic. 1 selects address data from CCS logic.
6	RW	MBA_FARB5Q_CFG_CCS_INST_RESET_ENABLE: When set to 1, bit 16 of the CCS_INST_ARR0 is driven out to DDR Resetn. When set to 0, cfg_ddr_resetn is driven out to DDR Resetn.
7	RW	MBA_FARB5Q_CFG_GP_BIT_3_ENABLE: When set to 1, the inverted value of GP(3) is driven on the force_mclk_low signal to the DDR PHYs. When set to 0, the inverted value of cfg_force_mclk_low_n is driven on the force_mclk_low signal to the DDR PHYs.
8	RW	MBA_FARB5Q_CFG_FORCE_MCLK_LOW_N: The inverted value of force_mclk_low_n is driven on mba_ddr_force_mclk_low when cfg_gp_bit_3_enable is 0.
9:15	RW	MBA_FARB5Q_RESERVED_56_63: Reserved.

Register Name	DDR Port Status Register
Mnemonic	MC01.PORT0.SRQ.MBA_FARB6Q
Address	0000000007010919 (SCOM)
Description	DDR Port Status Register

Bits	SCOM	Field Mnemonic: Description
0:10	ROX	MBA_FARB6Q_CFG_BW_SNAPSHOT: DRAM data bus utilization over the last 4K DDR clock window. All 1s is 100 percent utilization.
11:14	ROX	MBA_FARB6Q_CFG_CKE_PUP_STATE: Indicates which of the four CKEs are on.
15	ROX	MBA_FARB6Q_CFG_STR_STATE: Indicates whether the DRAMS on this port are in STR.
16:20	ROX	MBA_FARB6Q_CFG_RRQ_DEPTH: RRQ depth; The number of commands in the RRQ.
21:25	ROX	MBA_FARB6Q_CFG_WRQ_DEPTH: WRQ depth; The number of commands in the WRQ.
26:30	ROX	MBA_FARB6Q_CFG_RCD_PARITY_DLY: Delay from the parity error to the error being seen back in MBA. This value can then be placed back in the RCD protection time register.
31	ROX	MBA_FARB6Q_CFG_EVENTN: EventN monitor for thermal event.

Register Name	MBA Error Report Register
Mnemonic	MC01.PORT0.SRQ.MBA_ERR_REPORTQ
Address	000000000701091A (SCOM)
Description	MBA error report register

Bits	SCOM	Field Mnemonic: Description
0	ROX	MBA_ERR_REPORTQ_WRQ_HANG_ERR: WRQ hang error MBACALFIR Bit 17.
1	ROX	MBA_ERR_REPORTQ_RRQ_HANG_ERR: RRQ hang error MBACALFIR Bit 17.
2	ROX	MBA_ERR_REPORTQ_DSM_PE_ERR: Parity error in DSM configuration registers MBACALFIR Bit 1.
3	ROX	MBA_ERR_REPORTQ_TMR_PE_ERR: Parity error in TMR configuration registers MBACALFIR Bit 1.
4	ROX	MBA_ERR_REPORTQ_RRQ_PE_ERR: Parity error in RRQ configuration registers MBACALFIR Bit 0.
5	ROX	MBA_ERR_REPORTQ_WRQ_PE_ERR: Parity error in WRQ configuration registers MBACALFIR Bit 0.
6	ROX	MBA_ERR_REPORTQ_FARB_PE_ERR: Parity error in FARB configuration registers MBACALFIR Bit 1.

Bits	SCOM	Field Mnemonic: Description
7	ROX	MBA_ERR_REPORTQ_PC_PE_ERR: Parity error in PC configuration registers MBACALFIR Bit 0.
8	ROX	MBA_ERR_REPORTQ_CAL0_PE_ERR: Parity error in Cal0 configuration register MBACALFIR Bit 0.
9	ROX	MBA_ERR_REPORTQ_CAL1_PE_ERR: Parity error in Cal1 configuration register MBACALFIR Bit 0.
10	ROX	MBA_ERR_REPORTQ_CAL2_PE_ERR: Parity error in Cal2 configuration register MBACALFIR Bit 0.
11	ROX	MBA_ERR_REPORTQ_CAL3_PE_ERR: Parity error in Cal3 configuration register MBACALFIR Bit 0.
12	ROX	MBA_ERR_REPORTQ_DDR_IF_SM_1HOT_ERR: DDR state machine one hot error MBACALFIR Bit 18.
13	ROX	MBA_ERR_REPORTQ_CAL_SM_1HOT_ERR: Calibration state machine one hot error MBACALFIR Bit 18.
14	ROX	MBA_ERR_REPORTQ_RANK_SM_1HOT_ERR: Rank state machine one hot error MBACALFIR Bit 18.
15	ROX	MBA_ERR_REPORTQ_RESERVED_15: Reserved 15.
16	ROX	MBA_ERR_REPORTQ_PC_CAL_PCFSM_1HOT_ERR: Power control state machine one hot error MBACALFIR bit 18.
17	ROX	MBA_ERR_REPORTQ_FARB_CAL_RECVFSM_1HOT_ERR: Recovery state machine one hot error MBACALFIR bit 18.
18:23	ROX	MBA_ERR_REPORTQ_RESERVED_18_23: Reserved.
24	ROX	MBA_ERR_REPORTQ_RCMD_ASYNC_IF_ERR: Sequence error on rcmd asynchronous crossing. Operations received out of order.
25	ROX	MBA_ERR_REPORTQ_PF_PROMOTE_ASYNC_IF_ERR: Sequence error on prefetch promote asynchronous crossing. Operations received out of order.
26	ROX	MBA_ERR_REPORTQ_CANCEL_ACK_ASYNC_IF_ERR: Sequence error on cancel ACK asynchronous crossing. Operations received out of order.
27	ROX	MBA_ERR_REPORTQ_FARB_CMD_PE_HOLD_OUT: Parity error seen on new command to be issued by sequencer.
28	ROX	MBA_ERR_REPORTQ_DSM_CMD_PE_HOLD_OUT: Parity error seen on command as it leaves sequencer.
29:30	ROX	MBA_ERR_REPORTQ_RESERVED_29_30: Reserved.
31:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	**Emergency Throttle Register**
Mnemonic	MC01.PORT0.SRQ.MBA_FARB7Q
Address	0000000007010925 (SCOM)
Description	Emergency Throttle Register

Bits	SCOM	Field Mnemonic: Description
0	RW	MBA_FARB7Q_EMER_THROTTLE_IP: Emergency throttle in progress. This register can also be set to manually engage emergency throttle, or cleared to clear emergency throttle.

Register Name	**MBA Debug Bus Register 0**
Mnemonic	MC01.PORT0.SRQ.MBA_DBG0Q
Address	0000000007010926 (SCOM)
Description	MBA Debug Bus Register 0

Bits	SCOM	Field Mnemonic: Description
0	RW	MBA_DBG0Q_CFG_DBG_SRQ_ENABLE:
1:3	RW	MBA_DBG0Q_CFG_DBG_SRQ_SEL0:
4:6	RW	MBA_DBG0Q_CFG_DBG_SRQ_SEL1:
7:9	RW	MBA_DBG0Q_CFG_DBG_SRQ_SEL2:
10:12	RW	MBA_DBG0Q_CFG_DBG_SRQ_SEL3:
13:15	RW	MBA_DBG0Q_CFG_DBG_SRQ_SEL4:
16:18	RW	MBA_DBG0Q_CFG_DBG_SRQ_SEL5:
19:21	RW	MBA_DBG0Q_CFG_DBG_SRQ_SEL6:
22:24	RW	MBA_DBG0Q_CFG_DBG_SRQ_SEL7:
25:33	RW	MBA_DBG0Q_RESERVED_25_33:
34:41	RW	MBA_DBG0Q_CFG_DBG_SRQ_SEL_OTHER_SRQ:
42:47	RW	MBA_DBG0Q_RESERVED_42_47:
48:51	RW	MBA_DBG0Q_CFG_WAT_FARB_RRQ_GT:
52:55	RW	MBA_DBG0Q_CFG_WAT_FARB_WRQ_GT:
56:59	RW	MBA_DBG0Q_CFG_WAT_FARB_REF_GT:
60:63	RW	MBA_DBG0Q_CFG_WAT_FARB_CAL_GT:

Register Name	**MBA Debug Bus Register 1**
Mnemonic	MC01.PORT0.SRQ.MBA_DBG1Q
Address	0000000007010927 (SCOM)
Description	MBA Debug Bus Register 1

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MBA_DBG1Q_CFG_WAT_FORCE_WR_ENTRY0_HP:
4:7	RW	MBA_DBG1Q_CFG_WAT_FORCE_RD_ENTRY0_HP:
8:11	RW	MBA_DBG1Q_CFG_WAT_FP_DIS:
12:15	RW	MBA_DBG1Q_CFG_WAT_DIS_RD_PG:
16:19	RW	MBA_DBG1Q_CFG_WAT_DIS_WR_PG:
20:23	RW	MBA_DBG1Q_CFG_WAT_PUP_ALL:
24:27	RW	MBA_DBG1Q_CFG_WAT_EXIT_STR:
28:31	RW	MBA_DBG1Q_CFG_WAT_REF_HP:
32:35	RW	MBA_DBG1Q_CFG_WAT_REF_SYNC:
36:39	RW	MBA_DBG1Q_CFG_WAT_REF_SAFE:
40:43	RW	MBA_DBG1Q_CFG_WAT_CAL_SYNC:
44:47	RW	MBA_DBG1Q_CFG_WAT_RRQ_MNT_GT:
48:51	RW	MBA_DBG1Q_CFG_WAT_WRQ_MNT_GT:
52:55	RW	MBA_DBG1Q_CFG_WAT_SET_FIR:
56:59	RW	MBA_DBG1Q_CFG_WAT_EMER_TH:
60:63	RW	MBA_DBG1Q_CFG_WAT_START_RECOVERY:

Register Name	Emergency Throttle Register
Mnemonic	MC01.PORT0.SRQ.MBA_FARB8Q
Address	0000000007010928 (SCOM)
Description	Emergency Throttle Register

Bits	SCOM	Field Mnemonic: Description
0	RW	MBA_FARB8Q_SAFE_REFRESH_MODE: Safe refresh interval is being used for tREFI. This register can also be set to manually engage safe refresh or cleared to clear safe refresh.

Register Name	Timer State Machine Control Register
Mnemonic	MC01.PORT0.SRQ.MBA_TMR2Q
Address	000000000701092F (SCOM)
Description	Timer state machine control.

Bits	SCOM	Field Mnemonic: Description
0:19	RW	MBA_TMR2Q_CFG_BANK_BUSY_FSM_DIS: Disable bank busy state machines 0 - 19, one bit per FSM.
20:31	RW	MBA_TMR2Q_CFG_BANK_BUSY_OPEN_PAGE_DIS: Disable open page mode on bank busy state machines 0 - 11, one bit per FSM. Bank busy state machines 12 - 19 do not do open page mode.
32:63	RW	MBA_TMR2Q_RESERVED_32_63: Reserved.

Register Name	Refresh Register 0
Mnemonic	MC01.PORT0.SRQ.PC.MBAREF0Q
Address	0000000007010932 (SCOM)
Description	Refresh register 0

Bits	SCOM	Field Mnemonic: Description
0	RW	MBAREF0Q_CFG_REFRESH_ENABLE: Refresh enable.
1:2	RW	MBAREF0Q_CFG_REFRESH_INTERVAL_TIMEBASE_SELECT: 01 = Reserved. For 10 and 11 settings, to determine the actual refresh interval, multiply the calculated refresh interval by 8k or 2^{22} depending on which timebase was used. **Note**: Settings 10 and 11 are for characterization stress testing only.
3	RW	MBAREF0Q_CFG_PER_BANK_REFRESH: Banks are individually refreshed. Each time a new refresh to a rank pops, a refresh must be sent to each bank separately before that refresh is considered complete. DDR4E only.
4	RW	MBAREF0Q_CFG_REFRESH_DEBUG_SELECT: Refresh debug bus select. 0 selects only master ranks;. 1 selects slave ranks.
5:7	RW	MBAREF0Q_CFG_REFRESH_PRIORITY_THRESHOLD: After the number of queued refreshes to a rank reaches this threshold, that rank's refreshes become high priority. Values greater than 0x5 can potentially lead to a refresh timeout FIR.

Bits	SCOM	Field Mnemonic: Description
8:18	RW	MBAREF0Q_CFG_REFRESH_INTERVAL: This value is multiplied by 8 to represent the number of DRAM command clock cycles at which a refresh is to be sent to a rank in order to honor the refresh interval (tREFI). A refresh to a specific rank will be seen 8 × cfg_refresh_interval × num_ranks × DRAM_command_clock_cycle_time. So, program this dial to: cfg_refresh_interval = desired_tREFI_in_usnum_ranksDRAM_command_clock_cycle_in_ns.008). For example, for a system with two master ranks and four slaves per master (8 ranks total), a desired refresh interval of 7.8 µs, and DDR-1600 memory, cfg_refresh_interval = 7.881.25.008 = 97 (round down).
19:29	RW	MBAREF0Q_CFG_REFRESH_RESET_INTERVAL: This is the value to load the refresh interval counter to when a syncreset pulse is seen from the MBA. This is used to offset refreshing to the different MBAs. **Note**: The refresh reset interval should be set to a value less than the refresh interval.
30:39	RW	MBAREF0Q_CFG_TRFC: Refresh to activate rank protection timer.
40:49	RW	MBAREF0Q_CFG_REFR_TSV_STACK: Refresh-to-refresh spacing within the same TSV stack timer.
50:60	RW	MBAREF0Q_CFG_REFR_CHECK_INTERVAL: This setting is used to verify the refresh rules are upheld only (it is not the actual refresh interval). It is multiplied by 8 to represent the number of DRAM command clock cycles at which a refresh is to be seen to a given rank in order to honor the refresh interval (tREFI). A refresh to a specific rank should be seen 8 × cfg_refresh_check_interval × DRAM_command_clock_cycle_time. So, program this dial to: cfg_refr_check_interval = desired_tREFI_in_usDRAM_command_clock_cycle_in_ns.008). For example, if using DDR-1600 memory and expecting a refresh to occur every 7.8 us: cfg_refr_check_interval = 7.81.25.008 = 780=0x30C. If using DDR-1600 memory and expecting a refresh every 3.9 us: cfg_refr_check_interval = 3.91.25.008 = 390 = 0x186.
61	RW	MBAREF0Q_CFG_TRFC_STACK_GATE_ALL_REF: When set, this causes all refreshes to be spaced by cfg_refr_tsv_stack, regardless of whether they are to ranks on the same stack. This mode can be enabled as a means to reduce the power impact due to a burst of refreshes to different ranks.
62:63	RW	MBAREF0Q_RESERVED_62_63: Reserved.

Register Name	**Reserved SCOM Address Register**
Mnemonic	MC01.PORT0.SRQ.PC.MBARSVD0
Address	0000000007010933 (SCOM)
Description	Reserved SCOM Register Address

Bits	SCOM	Field Mnemonic: Description
0:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000000000000000000000

Register Name	**Power Control Register 0**
Mnemonic	MC01.PORT0.SRQ.PC.MBARPC0Q
Address	0000000007010934 (SCOM)
Description	Power control register 0

Bits	SCOM	Field Mnemonic: Description
0:1	RW	MBARPC0Q_RESERVED_0_1: Reserved.
2	RW	MBARPC0Q_CFG_MIN_MAX_DOMAINS_ENABLE: This is an overall enable for power domain control. If power control is disabled, the CKEs will always be set to a '1'.

Bits	SCOM	Field Mnemonic: Description
3:5	RW	MBARPC0Q_CFG_MIN_MAX_DOMAINS: Configures dynamic power up and power down of CKEs within specified minimum-maximum limits. Maxall_minall means power control will not limit the number of domains accessible at a given time. Power domains will not be powered down even if they go idle, unless min_domain_reduction is enabled. Maxall_minx will permit idle power down to reduce the number of domains powered up after a domain has gone idle, but it will not restrict the maximum domains powered up. Max1_minx restricts the number of domains that can be powered up at a given time to 1.
6:10	RW	MBARPC0Q_CFG_PUP_AVAIL: Specifies how many DRAM command clocks for power control to wait from CKE going high to activate.
11:15	RW	MBARPC0Q_CFG_PDN_PUP: Specifies how many DRAM command clocks for power control to wait from CKE going low to high again (enforces minimum time in power down)
16:20	RW	MBARPC0Q_CFG_PUP_PDN: Specifies how many DRAM command clocks for power control to wait from CKE going high to low again (enforces minimum time powered up).
21	RW	MBARPC0Q_RESERVED_21: Reserved.
22	RW	MBARPC0Q_CFG_MIN_DOMAIN_REDUCTION_ENABLE: This allows a dynamic reduction of the minimum domains to 0 when no memory traffic has been seen over the specified cfg_min_domain_reduction_time; minimum domains will be restored after traffic is seen; the adjusted minimum domains will not be reflected in or over-write the cfg_min_max_domains setting (adjustment made internal to logic).
23:32	RW	MBARPC0Q_CFG_MIN_DOMAIN_REDUCTION_TIME: Specifies how many DRAM command clocks the MBA must be idle before min_cke is reduced to 0.
33	RW	MBARPC0Q_CFG_PUP_AFTER_ACTIVATE_WAIT_ENABLE: After a configurable time has been met since the last activate, a subsequent domain can be powered up, even if the powering-down domain has not been powered down yet.
34:41	RW	MBARPC0Q_CFG_PUP_AFTER_ACTIVATE_WAIT_TIME: Specifies how many DRAM command clocks the MBA must be idle before minimum domains is reduced to 0.
42	RW	MBARPC0Q_CFG_FORCE_SPARE_PUP: Forces all spare CKEs to couple with their respective primary CKEs. This bit should not be toggled during run time or when calibration is enabled.
43	RW	MBARPC0Q_CFG_MIN_DOMAIN_REDUCTION_CNT_REFR_INT: If set, use refresh interval for minimum domain reduction time interval. Otherwise, use DRAM clocks as interval.
44:46	RW	MBARPC0Q_CFG_EMER_MIN_MAX_DOMAIN: This is the minmax power domain setting that power control will revert to when emergency throttling is engaged.
47	RW	MBARPC0Q_CFG_PUP_ALL_WRITES_PENDING: Enabling this allows a domain to be powered up upon a write entering the write reorder queue (provided the maximum domains is set to all). **Note**: Reads always cause a power up to their power domain upon entering the read reorder queue (when maximum domains is set to all).
48	RW	MBARPC0Q_CFG_ALWAYS_WAIT_ACT_TIME: If set, when in single domain power up mode, we will always wait the configured time between activates even when all domains are powered down already.
49:63	RW	MBARPC0Q_RESERVED_49_63: Reserved.

Register Name	STR Register 0
Mnemonic	MC01.PORT0.SRQ.PC.MBASTR0Q
Address	0000000007010935 (SCOM)
Description	STR Register 0

Bits	SCOM	Field Mnemonic: Description
0	RW	MBASTR0Q_CFG_STR_ENABLE: Enable STR Entry. **Note**: Minimum-maximum domains must also be enabled to enter STR.
1	RW	MBASTR0Q_CFG_DIS_CLK_IN_STR: Disable Memory Clocks when in STR.

Bits	SCOM	Field Mnemonic: Description
2:11	RW	MBASTR0Q_CFG_ENTER_STR_TIME: Number of cfg_min_domain_reduction intervals of idle to wait before entering STR.
12:16	RW	MBASTR0Q_CFG_TCKESR: tCKESR
17:21	RW	MBASTR0Q_CFG_TCKSRE: tCKSRE
22:26	RW	MBASTR0Q_CFG_TCKSRX: tCKSRX
27:37	RW	MBASTR0Q_CFG_TXSDLL: tXSDLL
38:45	RW	MBASTR0Q_CFG_TRFC_COUNTER_DIS: Per tRFC counter disable. This field can be used to restrict the number of outstanding refreshes.
46:56	RW	MBASTR0Q_CFG_SAFE_REFRESH_INTERVAL: This is the refresh interval used when in safe-refresh (high-temp) mode. This value is multiplied by 8 to represent the number of DRAM command clock cycles at which a refresh is to be sent to a rank in order to honor the refresh interval (tREFI). A refresh to a specific rank will be seen 8 × cfg_safe_refresh_interval × num_ranks × DRAM_command_clock_cycle_time. So, program this dial to: cfg_safe_refresh_interval=desired_tREFI_in_usnum_ranksDRAM_command_clock_cycle_in_ns.008). For example, for a system with two master ranks and four slaves per master (8 ranks total), a desired refresh interval of 7.8 µs, and DDR-1600 memory, cfg_safe_refresh_interval = 7.881.25.008 = 97 (round down).
57:60	RW	MBASTR0Q_CFG_OCC_DEADMAN_TIMER_SEL: This selects one of 8 timeout values for the OCC deadman timer. If the OCC is idle for the programmed timeout value × timebase pulse, an emergency throttle command command is issued and refresh is set to safe refresh interval. Value Time 0000 = Disabled 0001 = 16 timebase pulses 0010 = 4 timebase pulses 0011 = 8 timebase pulses 0100 = 16 timebase pulses 0101 = 32 timebase pulses 0110 = 64 timebase pulses 0111 = 128 timebase pulses 1000 = 255 timebase pulses 1001 to 1111 are unused.
61	RW	MBASTR0Q_CFG_OCC_DEADMAN_TB_SEL: This selects which timebase pulse to use for the deadman timer. 0 = 1 in 2^{22} DRAM command clocks 1 = 1 in 8K DRAM command clocks
62:63	RW	MBASTR0Q_RESERVED_62_63: Reserved.

Register Name	Refresh Avoidance Control Register
Mnemonic	MC01.PORT0.SRQ.PC.MBAREFAQ
Address	0000000007010936 (SCOM)
Description	Refresh Avoidance Control Register

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MBAREFAQ_CFG_STATIC_IDLE_DLY: This is the number of cycles that the refresh logic will wait for a rank to be idle in the RRQ before sending a low-priority refresh. **Note:** This delay counts in multiples of four DDR clocks (per default lp ref sub counter setting).
4:5	RW	MBAREFAQ_CFG_LP_SUB_CNT: Sub counter for lp refresh scheduling dials. For dials that count based on this sub-counter, a value of 00 means the counter those dials compare against increments every 1 cycle. A value of 01 in this register means the higher level count increments every 4th cycle (10 is every 8th cycle and 11 is every 16th cycle).

Bits	SCOM	Field Mnemonic: Description
6	RW	MBAREFAQ_CFG_REFRESH_HP_RANK_BLOCK_ENABLE: When enabled, the refresh logic sends a block signal when issuing a high-priority refresh. The block signal prevents new demand requests to the refreshing rank from overwhelming the read reorder queue.
7:9	RW	MBAREFAQ_RESERVED_7_9: Reserved.
10:15	RW	MBAREFAQ_CFG_REF_BLOCK_STOP_DLY: Programmable setting which is subtracted from the tRFC timer. The result is used to determine when the block signal can be deasserted leading up to the end of a tRFC period. This allows new commands targeting the refresh domain being refreshed to progress to the rrq so that they are ready to go as soon as tRFC ends. (N)

Register Name	Performance Monitor Counts0 Register
Mnemonic	MC01.PORT0.SRQ.MBA_PMU0Q
Address	0000000007010937 (SCOM)
Description	Performance monitor counts0

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MBA_PMU0Q_READ_COUNT: Read count. Increments every read; wraps.
32:63	ROX	MBA_PMU0Q_WRITE_COUNT: Write count. Increments every write; wraps.

Register Name	Performance Monitor Counts1 Register
Mnemonic	MC01.PORT0.SRQ.MBA_PMU1Q
Address	0000000007010938 (SCOM)
Description	Performance monitor counts1

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MBA_PMU1Q_ACTIVATE_COUNT: Bank activate count. Increments for every activate; wraps.
32:63	ROX	MBA_PMU1Q_PU_COUNTS: Counts the number of rising edges for a CKE; wraps.

Register Name	Performance Monitor Counts2 Register
Mnemonic	MC01.PORT0.SRQ.MBA_PMU2Q
Address	0000000007010939 (SCOM)
Description	Performance monitor counts2

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MBA_PMU2Q_FRAME_COUNT: Frame count; increments every DRAM clock(2:1) clock.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Performance Monitor Counts4 Register
Mnemonic	MC01.PORT0.SRQ.MBA_PMU3Q
Address	000000000701093A (SCOM)
Description	Performance monitor counts4

Bits	SCOM	Field Mnemonic: Description
0:15	RW	MBA_PMU3Q_LOW_IDLE_THRESHOLD: Each time the low idle (no reads or writes queued) threshold is met, the low idle count will increment; between periods of command activity, there may be multiple low-idle-threshold-width windows of command inactivity. For each of these windows, the low idle count will be incremented. (counts 2:1Dram address frequency) counts MBA idle cycles.
16:31	RW	MBA_PMU3Q_MED_IDLE_THRESHOLD: Each time the med idle (no reads or writes queued) threshold is met, the med idle count will increment; between periods of command activity, there may be multiple med-idle-threshold-width windows of command inactivity. For each of these windows, the med idle count will be incremented.
32:63	RW	MBA_PMU3Q_HIGH_IDLE_THRESHOLD: Each time the high idle (no reads or writes queued) threshold is met, the high idle count will increment; between periods of command activity, there may be multiple high-idle-threshold-width windows of command inactivity. For each of these windows, the high idle count will be incremented.

Register Name	Performance Monitor Counts Register
Mnemonic	MC01.PORT0.SRQ.MBA_PMU4Q
Address	000000000701093B (SCOM)
Description	Performance monitor counts

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MBA_PMU4Q_BASE_IDLE_COUNT: Increments every MBA idle cycle (counts 2:1Dram address frequency).
32:63	ROX	MBA_PMU4Q_LOW_IDLE_COUNT: Counts the number of times the low idle threshold was met (counts 2:1Dram address frequency).

Register Name	Performance Monitor Counts Register
Mnemonic	MC01.PORT0.SRQ.MBA_PMU5Q
Address	000000000701093C (SCOM)
Description	Performance monitor counts

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MBA_PMU5Q_MED_IDLE_COUNT: Counts the number of times the med idle threshold was met (counts 2:1Dram address frequency).
32:63	ROX	MBA_PMU5Q_HIGH_IDLE_COUNT: Counts the number of times the high idle threshold was met (counts 2:1Dram address frequency).

Register Name	Performance Monitor Counts Register
Mnemonic	MC01.PORT0.SRQ.MBA_PMU6Q
Address	000000000701093D (SCOM)
Description	Performance monitor counts

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	MBA_PMU6Q_EVENT0_COUNTER: PMU Count for Event 0.
16:31	ROX	MBA_PMU6Q_EVENT1_COUNTER: PMU Count for Event 1.
32:47	ROX	MBA_PMU6Q_EVENT2_COUNTER: PMU Count for Event 2.

Bits	SCOM	Field Mnemonic: Description
48:63	ROX	MBA_PMU6Q_EVENT3_COUNTER: PMU Count for Event 3.

Register Name	Performance Monitor Event Select Register
Mnemonic	MC01.PORT0.SRQ.MBA_PMU7Q
Address	000000000701093E (SCOM)
Description	Performance monitor event select register

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MBA_PMU7Q_CFG_EVENT0_SELECT: Event0 select. 0x00 = MBA Command clocks 0x01 = ACT all 0x02 = ACT for read 0x03 = ACT for write 0x04 = CAS all 0x05 = CAS for read 0x06 = CAS for write 0x07 = CAS for low-priority write 0x08 = CAS for high-priority write 0x09 = PRE all 0x0a = PRE for read 0x0b = PRE for write 0x0c = REF high priority 0x0d = REF low priority 0x0e = REF all 0x0f = RRQ empty 0x10 = RRQ full 0x11 = WRQ empty 0x12 = WRQ full 0x13 = WRQ above hw mark 0x14 = Reserved 0x15 = activate with direction switch (change from rd → wr or wr → rd) 0x16 = activate with mrank switch (Master rank different than previous ACT) 0x17 = activate with srank switch (Same master; slave rank different than previous ACT) 0x18 = activate with bank group switch (Same master, slave; bank group different than previous ACT) 0x19 = activate with bank switch (Same master, slave, bank group; different bank than previous ACT) 0x1a = all bank timers full 0x1b any CKE PUP transition (0 → 1) 0x1c = CKE0 cycles PUP 0x1d = CKE1 cycles PUP 0x1e = CKE2 cycles PUP 0x1f = CKE3 cycles PUP 0x20 = WDF stalled waiting on read buffer 0x21 = WDF stalled waiting on read ramp 0x22 = Command0 Compare 0x23 - 0x3f = Reserved

Bits	SCOM	Field Mnemonic: Description
6:11	RW	MBA_PMU7Q_CFG_EVENT1_SELECT: Event1 Select. 0x00 MBA Command clocks 0x01 = ACT all 0x02 = ACT for read 0x03 = ACT for write 0x04 = CAS all 0x05 = CAS for read 0x06 = CAS for write 0x07 = CAS for low-priority write 0x08 = CAS for high-priority write 0x09 = PRE all 0x0a PRE for read 0x0b = PRE for write 0x0c = REF high priority 0x0d = REF low priority 0x0e = REF all 0x0f = RRQ empty 0x10 = RRQ full 0x11 = WRQ empty 0x12 = WRQ full 0x13 = WRQ above hw mark 0x14 = Reserved 0x15 = activate with direction switch (change from rd → wr or wr → rd) 0x16 = activate with mrank switch (Master rank different than previous ACT) 0x17 = activate with srank switch (Same master; slave rank different than previous ACT) 0x18 = activate with bank group switch (Same master, slave; bank group different than previous ACT) 0x19 = activate with bank switch (Same master, slave, bank group; different bank than previous ACT) 0x1a = all bank timers full 0x1b any CKE PUP transition (0 → 1) 0x1c = CKE0 cycles PUP 0x1d = CKE1 cycles PUP 0x1e = CKE2 cycles PUP 0x1f = CKE3 cycles PUP 0 x20 = WDF stalled waiting on read buffer 0x21 = WDF stalled waiting on read ramp 0x22 = Command1 Compare 0x23 - 0x3f = Reserved

Bits	SCOM	Field Mnemonic: Description
12:17	RW	MBA_PMU7Q_CFG_EVENT2_SELECT: Event2 Select. 0x00 = MBA Command clocks 0x01 = ACT all 0x02 = ACT for read 0x03 = ACT for write 0x04 = CAS all 0x05 = CAS for read 0x06 = CAS for write 0x07 = CAS for low-priority write 0x08 = CAS for high-priority write 0x09 = PRE all 0x0a PRE for read 0x0b = PRE for write 0x0c = REF high priority 0x0d = REF low priority 0x0e = REF all 0x0f = RRQ empty 0x10 = RRQ full 0x11 = WRQ empty 0x12 = WRQ full 0x13 = WRQ above hw mark 0x14 = Reserved 0x15 = activate with direction switch (change from rd → wr or wr → rd) 0x16 = activate with mrank switch (Master rank different than previous ACT) 0x17 = activate with srank switch (Same master; slave rank different than previous ACT) 0x18 = activate with bank group switch (Same master, slave; bank group different than previous ACT) 0x19 = activate with bank switch (Same master, slave, bank group; different bank than previous ACT) 0x1a = all bank timers full 0x1b = any CKE PUP transition (0 → 1) 0x1c = CKE0 cycles PUP 0x1d = CKE1 cycles PUP 0x1e = CKE2 cycles PUP 0x1f = CKE3 cycles PUP 0 x20 = WDF stalled waiting on read buffer 0x21 = WDF stalled waiting on read ramp 0x22 = Command2 Compare 0x23 - 0x3f = Reserved

Bits	SCOM	Field Mnemonic: Description
18:23	RW	MBA_PMU7Q_CFG_EVENT3_SELECT: Event3 select. 0x00 = MBA Command clocks 0x01 = ACT all 0x02 = ACT for read 0x03 = ACT for write 0x04 = CAS all 0x05 = CAS for read 0x06 = CAS for write 0x07 = CAS for low-priority write 0x08 = CAS for high-priority write 0x09 = PRE all 0x0a PRE for read 0x0b = PRE for write 0x0c = REF high priority 0x0d = REF low priority 0x0e = REF all 0x0f = RRQ empty 0x10 = RRQ full 0x11 = WRQ empty 0x12 = WRQ full 0x13 = WRQ above hw mark 0x14 = Reserved 0x15 = activate with direction switch (change from rd → wr or wr → rd) 0x16 = activate with mrank switch (Master rank different than previous ACT) 0x17 = activate with srank switch (Same master; slave rank different than previous ACT) 0x18 = activate with bank group switch (Same master, slave; bank group different than previous ACT) 0x19 = activate with bank switch (Same master, slave, bank group; different bank than previous ACT) 0x1a = all bank timers full 0x1b = any CKE PUP transition (0 → 1) 0x1c = CKE0 cycles PUP 0x1d = CKE1 cycles PUP 0x1e = CKE2 cycles PUP 0x1f = CKE3 cycles PUP 0x20 = WDF stalled waiting on read buffer 0x21 = WDF stalled waiting on read ramp 0x22 - 0x3f = Reserved
24:25	RW	MBA_PMU7Q_CFG_PRESCALER_C0: Prescaler for event counter 0 00 = 20-bit 01 = 16-bit 10 = 8-bit 11 = 4-bit
26:27	RW	MBA_PMU7Q_CFG_PRESCALER_C1: Prescaler for event counter 1. 00 = 20-bit 01 = 16-bit 10 = 8-bit 11 = 4-bit
28:29	RW	MBA_PMU7Q_CFG_PRESCALER_C2: Prescaler for event counter 2. 00 = 20-bit 01 = 16-bit 10 = 8-bit 11 = 4-bit
30:31	RW	MBA_PMU7Q_CFG_PRESCALER_C3: Prescaler for event counter 3. 00 = 20-bit 01 = 16-bit 10 = 8-bit 11 = 4-bit

Bits	SCOM	Field Mnemonic: Description
32:34	RW	MBA_PMU7Q_CASCADE: Allows cascading of counts to make a 32-bit counter. x00 = no cascading 001 = c0 → c1 010 = c1 → c2 011 = c2 → c3 101 = c1 → c0 110 = c2 → c1 111 = c3 → c2
35	RW	MBA_PMU7Q_FREEZE: If enabled, freeze all counters when any counter reaches maximum.

Register Name	Performance Monitor Command Compare Register
Mnemonic	MC01.PORT0.SRQ.MBA_PMU8Q
Address	000000000701093F (SCOM)
Description	Performance monitor command compare register

Bits	SCOM	Field Mnemonic: Description
0:1	RW	MBA_PMU8Q_CFG_CMD0_TYPE: Command 0 compare type qualifier: 00 = read 01 = write 10 = activate 11 = read or write
2	RW	MBA_PMU8Q_CFG_CMD0_MRANK_MATCH_EN:
3	RW	MBA_PMU8Q_CFG_CMD0_SRANK_MATCH_EN:
4	RW	MBA_PMU8Q_CFG_CMD0_BG_MATCH_EN:
5	RW	MBA_PMU8Q_CFG_CMD0_BANK_MATCH_EN:
6:8	RW	MBA_PMU8Q_CFG_CMD0_MRANK:
9:11	RW	MBA_PMU8Q_CFG_CMD0_SRANK:
12:13	RW	MBA_PMU8Q_CFG_CMD0_BG:
14:16	RW	MBA_PMU8Q_CFG_CMD0_BANK:
17:18	RW	MBA_PMU8Q_CFG_CMD1_TYPE: Command 1 compare type qualifier: 00 = read 01 = write 10 = activate 11 = read or write
19	RW	MBA_PMU8Q_CFG_CMD1_MRANK_MATCH_EN:
20	RW	MBA_PMU8Q_CFG_CMD1_SRANK_MATCH_EN:
21	RW	MBA_PMU8Q_CFG_CMD1_BG_MATCH_EN:
22	RW	MBA_PMU8Q_CFG_CMD1_BANK_MATCH_EN:
23:25	RW	MBA_PMU8Q_CFG_CMD1_MRANK:
26:28	RW	MBA_PMU8Q_CFG_CMD1_SRANK:
29:30	RW	MBA_PMU8Q_CFG_CMD1_BG:
31:33	RW	MBA_PMU8Q_CFG_CMD1_BANK:

Bits	SCOM	Field Mnemonic: Description
34:35	RW	MBA_PMU8Q_CFG_CMD2_TYPE: Command 2 compare type qualifier: 00 = read 01 = write 10 = activate 11 = read or write
36	RW	MBA_PMU8Q_CFG_CMD2_MRANK_MATCH_EN:
37	RW	MBA_PMU8Q_CFG_CMD2_SRANK_MATCH_EN:
38	RW	MBA_PMU8Q_CFG_CMD2_BG_MATCH_EN:
39	RW	MBA_PMU8Q_CFG_CMD2_BANK_MATCH_EN:
40:42	RW	MBA_PMU8Q_CFG_CMD2_MRANK:
43:45	RW	MBA_PMU8Q_CFG_CMD2_SRANK:
46:47	RW	MBA_PMU8Q_CFG_CMD2_BG:
48:50	RW	MBA_PMU8Q_CFG_CMD2_BANK:
51:63	RW	MBA_PMU8Q_RESERVED_51_63:

Register Name	**MBA CAL FIR Register**
Mnemonic	MC01.PORT1.SRQ.MBACALFIRQ
Address	0000000007010940 (SCOM) 0000000007010941 (SCOM1) 0000000007010942 (SCOM2)
Description	MBA CAL FIR Register (MBACALFIR)

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	MBACALFIRQ_MBA_RECOVERABLE_ERROR: When set, an MBA recoverable error has occurred. These include cal[0:3]_cfg, rrq, wrq and power control parity errors.
1	RWX	WOX_AND	WOX_OR	MBACALFIRQ_MBA_NONRECOVERABLE_ERROR: When set, an MBA nonrecoverable error has occurred. These include dsm, tmr, farb and SIR parity errors.
2	RWX	WOX_AND	WOX_OR	MBACALFIRQ_REFRESH_OVERRUN: When set, nine (9) refreshes have been enqueued to any single rank.
3	RWX	WOX_AND	WOX_OR	MBACALFIRQ_WAT_ERROR: When set, an error has been detected in the MBA debug WAT logic.
4	RWX	WOX_AND	WOX_OR	MBACALFIRQ_RCD_PARITY_ERROR: When set, an RCD parity error has been detected on DDR port 0. If the error was seen during a Calibration, FIR 14 will fire instead.
5	RWX	WOX_AND	WOX_OR	MBACALFIRQ_DDR_CAL_TIMEOUT_ERR: When set, a calibration complete indication was not received in the calibration timeout time for ddr0.
6	RWX	WOX_AND	WOX_OR	MBACALFIRQ_EMERGENCY_THROTTLE: Emergency throttle engaged either due to OCC request or deadman timer pop.
7	RWX	WOX_AND	WOX_OR	MBACALFIRQ_DDR_CAL_RESET_TIMEOUT: When set, indicates that a soft reset issued to the DDR PHY did not clear a pending calibration update request.
8	RWX	WOX_AND	WOX_OR	MBACALFIRQ_DDR_MBA_EVENT_N: When set, indicates event_n was active on the DDR interface.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
9	RWX	WOX_AND	WOX_OR	MBACALFIRQ_WRQ_RRQ_HANG_ERR: When set, indicates that the WRQ or RRQ is in a hung state.
10	RWX	WOX_AND	WOX_OR	MBACALFIRQ_SM_1HOT_ERR: When set, indicates a state machine one hot error.
11	RWX	WOX_AND	WOX_OR	MBACALFIRQ_ASYNC_IF_ERROR: Sequencer error seen when crossing asynchronous interface from MCS.
12	RWX	WOX_AND	WOX_OR	MBACALFIRQ_CMD_PARITY_ERROR: Address parity error seen internal to the sequencer on a read or write command.
13	RWX	WOX_AND	WOX_OR	MBACALFIRQ_PORT_FAIL: The port has failed due to a persistent retry. All reads returned with RCD error so that SUE will be delivered upstream.
14	RWX	WOX_AND	WOX_OR	MBACALFIRQ_RCD_CAL_PARITY_ERROR: When set, an RCD parity error has been detected during a calibration.
15	RWX	WOX_AND	WOX_OR	MBACALFIRQ_INTERNAL_SCOM_ERROR: When set, an internal SCOM error has occurred.
16	RWX	WOX_AND	WOX_OR	MBACALFIRQ_INTERNAL_SCOM_ERROR_COPY: Copy of internal SCOM error.
17:63	RO	RO	RO	Constant = 0b00000000000000000000000000000000000000000000000000000

Register Name	MBA CAL FIR Mask Register
Mnemonic	MC01.PORT1.SRQ.MBACALFIR_MASK
Address	0000000007010943 (SCOM) 0000000007010944 (SCOM1) 0000000007010945 (SCOM2)
Description	MBA CAL FIR Mask Register (MBACALFIR_MASK)

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	MBACALFIR_MASK_MBA_RECOVERABLE_ERROR: When set, an MBA recoverable error has occurred. These include cal[0:3]_cfg, rrq, wrq and power control parity errors.
1	RW	WO_AND	WO_OR	MBACALFIR_MASK_MBA_NONRECOVERABLE_ERROR: When set, an MBA nonrecoverable error has occurred. These include DSM, TMR, FARB, and SIR parity errors.
2	RW	WO_AND	WO_OR	MBACALFIR_MASK_REFRESH_OVERRUN: When set, nine (9) refreshes have been enqueued to any single rank.
3	RW	WO_AND	WO_OR	MBACALFIR_MASK_WAT_ERROR: When set, an error has been detected in the MBA debug WAT logic.
4	RW	WO_AND	WO_OR	MBACALFIR_MASK_RCD_PARITY_ERROR: When set, an RCD parity error has been detected on DDR port 0.
5	RW	WO_AND	WO_OR	MBACALFIR_MASK_DDR_CAL_TIMEOUT_ERR: When set, a calibration complete indication was not received in the calibration timeout time for DDR0.
6	RW	WO_AND	WO_OR	MBACALFIR_MASK_EMERGENCY_THROTTLE: Emergency throttle engaged either due to an OCC request or deadman timer pop.
7	RW	WO_AND	WO_OR	MBACALFIR_MASK_DDR_CAL_RESET_TIMEOUT: When set, indicates that a soft reset issued to the DDR PHY did not clear a pending calibration update request.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
8	RW	WO_AND	WO_OR	MBACALFIR_MASK_DDR_MBA_EVENT_N: When set, indicates event_n was active on the DDR interface.
9	RW	WO_AND	WO_OR	MBACALFIR_MASK_WRQ_RRQ_HANG_ERR: When set, indicates that the WRQ or RRQ is in a hung state.
10	RW	WO_AND	WO_OR	MBACALFIR_MASK_SM_1HOT_ERR: When set, indicates a state machine one hot error.
11	RW	WO_AND	WO_OR	MBACALFIR_MASK_ASYNC_IF_ERROR: Sequencer error seen when crossing asynchronous interface from MCS.
12	RW	WO_AND	WO_OR	MBACALFIR_MASK_CMD_PARITY_ERROR: Address parity error seen internal to sequencer on read or write command.
13	RW	WO_AND	WO_OR	MBACALFIRQ_MASK_PORT_FAIL: The port has failed due to a persistent retry. All reads returned with RCD error so that SUE will be delivered upstream.
14	RW	WO_AND	WO_OR	MBACALFIRQ_MASK_RCD_CAL_PARITY_ERROR: When set, an RCD parity error has been detected during a calibration.
15	RW	WO_AND	WO_OR	MBACALFIR_MASK_INTERNAL_SCOM_ERROR: When set, and internal SCOM error has occurred.
16	RW	WO_AND	WO_OR	MBACALFIR_MASK_INTERNAL_SCOM_ERROR_COPY: Copy of internal SCOM error.
17:63	RO	RO	RO	Constant = 0b00000000000000000000000000000000000000000000000

Register Name	**MBA CAL FIR Action 0 Register**
Mnemonic	MC01.PORT1.SRQ.MBACALFIR_ACTION0
Address	0000000007010946 (SCOM)
Description	MBA CAL FIR Action 0 Register (MBACALFIR_ACTION0)

Bits	SCOM	Field Mnemonic: Description
0:16	RW	MBACALFIR_ACTION0_FIR_ACTION0: MBA action0 select for the corresponding bit in the FIR. (Action0, Action1, Mask) = Action Select: (0,0,X) = No error reported (0,1,0) = Recoverable error (1,0,0) = Checkstop error (1,1,0) = Local core checkstop freeze (X,X,1) = MASKED
17:63	RO	Constant = 0b00000000000000000000000000000000000000000000000

Register Name	**MBA CAL FIR Action 1 Register**
Mnemonic	MC01.PORT1.SRQ.MBACALFIR_ACTION1
Address	0000000007010947 (SCOM)
Description	MBA CAL FIR Action 1 Register (MBACALFIR_ACTION1)

Bits	SCOM	Field Mnemonic: Description
0:16	RW	MBACALFIR_ACTION1_FIR_ACTION1: MBA action1 select for the corresponding bit in the FIR. (Action0, Action1, Mask) = Action Select: (0,0,X) = No error reported (0,1,0) = Recoverable error (1,0,0) = Checkstop error (1,1,0) = Local core checkstop freeze (X,X,1) = Masked
17:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000

Register Name	Data State Machine Configuration Register
Mnemonic	MC01.PORT1.SRQ.MBA_DSM0Q
Address	000000000701094A (SCOM)
Description	Data state machine configurations

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MBA_DSM0Q_CFG_RODT_START_DLY: Delay from read command to ODT turn on.
6:11	RW	MBA_DSM0Q_CFG_RODT_END_DLY: Delay from read command to ODT turn off.
12:17	RW	MBA_DSM0Q_CFG_WODT_START_DLY: Delay from write command to ODT turn on.
18:23	RW	MBA_DSM0Q_CFG_WODT_END_DLY: Delay from write command to ODT turn off.
24:29	RW	MBA_DSM0Q_CFG_WRDONE_DLY: Delay from write command to write done to MBS.
30:35	RW	MBA_DSM0Q_CFG_WRDATA_DLY: Delay from write command to stating the write data flow.
36:41	RW	MBA_DSM0Q_CFG_RDTAG_DLY: Delay from read command to rd data valid back to MBS.
42	RW	MBA_DSM0Q_CFG_RDTAG_MBX_CYCLE: Determines the memory clock 1/2 cycle that the rdtag entry is released from the DSM queue. 0 = Release when MBX clock is low. 1 = Release when MBX clock is high.
43:48	RW	MBA_DSM0Q_CFG_RODT_BC4_END_DLY: Delay from read command to ODT turn off for BC4 command.
49:54	RW	MBA_DSM0Q_CFG_WODT_BC4_END_DLY: Delay from write command to ODT turn off for BC4 command.
55:63	RW	MBA_DSM0Q_RESERVED_55_63: Reserved.

Register Name	DDR Data Bus Timing Parameters Register
Mnemonic	MC01.PORT1.SRQ.MBA_TMR0Q
Address	000000000701094B (SCOM)
Description	DDR data bus timing parameters

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MBA_TMR0Q_RRDM_DLY: Read to read to different master.
4:7	RW	MBA_TMR0Q_RRSMSR_DLY: Read to read same master, same rank.
8:11	RW	MBA_TMR0Q_RRSMDR_DLY: Read to read same master, different rank.
12:15	RW	MBA_TMR0Q_RROP_DLY: Read open page to read delay.
16:19	RW	MBA_TMR0Q_WWDM_DLY: Write to write different master.
20:23	RW	MBA_TMR0Q_WWSMSR_DLY: Write to write same master, same rank.

Bits	SCOM	Field Mnemonic: Description
24:27	RW	MBA_TMR0Q_WWSMDR_DLY: Write to write same master, different rank.
28:31	RW	MBA_TMR0Q_WWOP_DLY: Write open page to write delay.
32:36	RW	MBA_TMR0Q_RWDM_DLY: Read to write different master.
37:41	RW	MBA_TMR0Q_RWSMSR_DLY: Read to write same master, same rank.
42:46	RW	MBA_TMR0Q_RWSMDR_DLY: Read to write same master, different rank.
47:50	RW	MBA_TMR0Q_WRDM_DLY: Write to read different master.
51:56	RW	MBA_TMR0Q_WRSMSR_DLY: Write to read same master ,same rank.
57:62	RW	MBA_TMR0Q_WRSMDR_DLY: Write to read same master, different rank.
63	RW	MBA_TMR0Q_RESERVED_63: Reserved.

Register Name	DDR Bank Busy Parameters Register
Mnemonic	MC01.PORT1.SRQ.MBA_TMR1Q
Address	000000000701094C (SCOM)
Description	DDR bank busy parameters

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MBA_TMR1Q_RRSBG_DLY: Read to read same bank group.
4:9	RW	MBA_TMR1Q_WRSBG_DLY: Write to read same bank group.
10:15	RW	MBA_TMR1Q_CFG_TFAW: Four activate window time.
16:20	RW	MBA_TMR1Q_CFG_TRCD: RAS to CAS delay.
21:25	RW	MBA_TMR1Q_CFG_TRP: Precharge to activate delay.
26:31	RW	MBA_TMR1Q_CFG_TRAS: Activate to precharge delay.
32:40	RW	MBA_TMR1Q_RESERVED_32_40: Reserved.
41:47	RW	MBA_TMR1Q_CFG_WR2PRE: Write to precharge delay.
48:51	RW	MBA_TMR1Q_CFG_RD2PRE: Read to precharge delay.
52:55	RW	MBA_TMR1Q_TRRD: Activate to activate delay.
56:59	RW	MBA_TMR1Q_TRRD_SBG: Activate to activate same bank group delay.
60:63	RW	MBA_TMR1Q_CFG_ACT_TO_DIFF_RANK_DLY: Activate to activate different rank delay.

Register Name	DDR Write Command Parameters Register
Mnemonic	MC01.PORT1.SRQ.MBA_WRQ0Q
Address	000000000701094D (SCOM)
Description	DDR write command parameters

Bits	SCOM	Field Mnemonic: Description
0:4	RW	MBA_WRQ0Q_CFG_WRITE_HW_MARK: Write high-water mark(force writes HPenables writes).
5	RW	MBA_WRQ0Q_CFG_WRQ_FIFO_MODE: Prevent reordering in the WRQ(only entry0 can be selected) HP Cleaner writes will not get selected until they are in entry 0.
6	RW	MBA_WRQ0Q_CFG_DISABLE_WR_PG_MODE: Disable page commands for WRQ.

Bits	SCOM	Field Mnemonic: Description
7:18	RW	MBA_WRQ0Q_CFG_WRQ_ENTRY0_HP_DLY: Time for entry0 of the WRQ before it forces HP setting this dial to a 0, will disable entry0 HP.
19	RW	MBA_WRQ0Q_CFG_WRQ_FLUSH_WR_RANK: When one write is issued to a rank, try to force more writes to that rank to avoid multiple write to read same rank penalties.
20	RW	MBA_WRQ0Q_CFG_WRQ_ENABLE_NON_HP_WR: Allow writes when they do not meet a condition such as entry0_flush or rd_idle_allow_wr.
21:32	RW	MBA_WRQ0Q_CFG_ENTRY0_MIN_FOR_RRQ_IDLE_WR: This is an added condition to allow writes when the RRQ is idle. This addition allows for multiple writes to stack up in the WRQ before starting the write burst.
33:37	RW	MBA_WRQ0Q_CFG_WRITE_LW_MARK: Write low-water mark. After write high priority has been asserted due to the writes exceeding the programmed high-water mark, write priority will remain asserted until the write low-water mark is reached. set to 8, and there are more then 8 entries in the wrq then the condition will allow writes when the rrq_idle period is met.
38:43	RW	MBA_WRQ0Q_CFG_WRQ_SKIP_LIMIT: The number of times entry0 of the WRQ can be skipped before entry0 prevents older writes from being issued until entry0 is sent.
44	RW	MBA_WRQ0Q_CFG_WRQ_SINGLE_THREAD_MODE: WRQ wrq_single Thread mode Setting this ensures all reads are issued one at a time. With this mode set we will only issue from the bottom entry in the WRQ, and we will not issue an activate for the subsequent operation until the prior write is sent.
45:52	RW	MBA_WRQ0Q_CFG_RQ_HANG_THRESHOLD: Hang detection for entry0 of reorder queue. A counter increments every mcbist_srq_hang_pulse(2048 phase hold cycles), and will set a FIR when the count = threshold and another pulse is received. Since this checks for count = threshold, a value of 0 is not valid.
53:54	RW	MBA_WRQ0Q_RESERVED_53_54: Reserved.
55:58	RW	MBA_WRQ0Q_CFG_WRQ_ACT_NUM_WRITES_PENDING: Limit on number of write-activates when doing writes. When the sequencer is serving writes, no new activates will be sent out as long as at least this number of writes are pending to already-activated pages. A setting of 0 sets no cap on the number of activates.
59:63	RW	MBA_WRQ0Q_RESERVED_59_63: Reserved.

Register Name	DDR Read Command Parameters Register
Mnemonic	MC01.PORT1.SRQ.MBA_RRQ0Q
Address	000000000701094E (SCOM)
Description	DDR read command parameters

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MBA_RRQ0Q_CFG_RRQ_SKIP_LIMIT: Number of times the bottom entry in the RRQ can be skipped before preventing the entry from being skipped.
6	RW	MBA_RRQ0Q_CFG_RRQ_FIFO_MODE: RRQ FIFO mode Setting this ensures all reads go out in the order they were received. It still allows multiple operations to be pipelined to allow for decent throughput. This needs to be set for MCBIST dgen mode.
7	RW	MBA_RRQ0Q_CFG_RRQ_SINGLE_THREAD_MODE: RRQ Single Thread mode Setting this ensures all reads are issued one at a time. With this mode set we will only issue from the bottom entry in the RRQ, and we will not issue an activate for the subsequent operation until the prior read is sent.
8:10	RW	MBA_RRQ0Q_RESERVED_8_10: Reserved.
11	RW	MBA_RRQ0Q_CFG_DISABLE_RD_PG_MODE: Disable page commands for RRQ.
12	RW	MBA_RRQ0Q_CFG_DISABLE_FAST_PATH: Disable MBA RRQ fastpath.
13:23	RW	MBA_RRQ0Q_CFG_RD_IDLE_ALLOW_WR: Time with an empty RRQ before writes will be enabled.
24:29	RW	MBA_RRQ0Q_CFG_RDBUFF_CAPACITY_LIMIT: Number of 64-byte read buffers sequencer is allowed to use concurrently.

Bits	SCOM	Field Mnemonic: Description
30:36	RW	MBA_RRQ0Q_CFG_RMWBUFF_CAPACITY_LIMIT: Number of 64-byte read-modify-write buffers sequencer is allowed to use concurrently.
37:56	RW	MBA_RRQ0Q_RESERVED_37_56: Reserved.
57:60	RW	MBA_RRQ0Q_CFG_RRQ_ACT_NUM_READS_PENDING: Limit on number of read-activates when doing reads. When the sequencer is serving reads, no new activates will be sent out as long as at least this number of reads are pending to already-activated pages. A setting of 0 sets no cap on the number of activates.
61	RW	MBA_RRQ0Q_CFG_INJ_CANCEL_ACK_ERR: Inject error on cancel-ack asynchronous interface.
62	RW	MBA_RRQ0Q_CFG_RRQ_ENTRY0_ENABLE: Enable entry0 timer for RRQ.
63	RW	MBA_RRQ0Q_RESERVED_63: Reserved.

Register Name	DDR Calibration Register
Mnemonic	MC01.PORT1.SRQ.MBA_CAL0Q
Address	000000000701094F (SCOM)
Description	DDR Calibration registers

Bits	SCOM	Field Mnemonic: Description
0	RW	MBA_CAL0Q_CFG_CAL_INTERVAL_TMR0_ENABLE: Enable interval tmr0.
1:2	RW	MBA_CAL0Q_CFG_TIME_BASE_TMR0: Time base for interval tmr0 counter.
3:11	RW	MBA_CAL0Q_CFG_INTERVAL_COUNTER_TMR0: Interval timer based on time_base(time_base × interval_counter).
12	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL1_ENABLE: Enable bit for the first calibration to perform when the timer pops. Should always be 1 if the timer is enabled.
13:16	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL1_TYPE: 10XX = Internal ZQ calibration (cal_rank ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step. 0011 = Periodic calibration: Run SysClk, DQS, and read eye all in parallel (default behavior).
17	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL1_DDR_DONE: Use the complete signal from the DDR for cal1.
18	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL2_ENABLE: Enable bit for second calibration to perform when timer pops.
19:22	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL2_TYPE: 10XX = Internal ZQ calibration (cal_rank ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step. 0011 = Periodic calibration: Run SysClk, DQS, and read eye all in parallel (default behavior).
23	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL2_DDR_DONE: Use the complete signal from the DDR for cal2.
24	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL3_ENABLE: Enable bit for third calibration to perform when timer pops.
25:28	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL3_TYPE: 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step. 0011 = Periodic calibration: Run SysClk, DQS, and read eye all in parallel (default behavior).

Bits	SCOM	Field Mnemonic: Description
29	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL3_DDR_DONE: Use the complete signal from the DDR for cal3.
30:38	RW	MBA_CAL0Q_CFG_CAL_TMR0_Z_SYNC: The timer value will be set to this value during z sync.
39:46	RW	MBA_CAL0Q_CFG_CAL_TMR0_DDR_RESET_TMR: Wait time for DDR soft reset upon calibration timeout fail.
47:48	RW	MBA_CAL0Q_CFG_CAL_TMR0_DDR_RESET_TMR_TB: Timebase interval for ddr_reset_tmr
49	RW	MBA_CAL0Q_CFG_CAL_TMR0_DDR_RESET_ENABLE: Enable DDR soft reset upon calibration timeout fail. 0 Do not issue soft DDR reset upon calibration timeout. 1 Issue DDR soft reset upon calibration timeout.
50	RW	MBA_CAL0Q_CFG_CAL_TMR0_SINGLE_RANK: Enable single-rank mode for timer0 calibrations. Calibrations programmed in tmr0 will run on one rank at a time per timer expiration. 0 = Issue calibrations for all enabled ranks per timer expiration. 1 = Issue calibrations for one rank at a time per timer expiration.
51	RW	MBA_CAL0Q_RESERVED_51: Reserved.
52	RW	MBA_CAL0Q_INJECT_1HOT_SM_ERROR: Setting to 1 will inject one 1hot sm error, must be set to 0 and then 1 again to inject another error 0 No error inject 1 Inject one 1hot sm error.
53:55	RW	MBA_CAL0Q_CFG_CAL_SINGLE_PORT_MODE: Single port mode configuration, default is both ports are calibrated at the same time, options are single port calibrated at a time with both ports powered up single port calibrated at a time with one port powered up single port calibrated at a time with one port powered up and only the rank requested by the DDR PHY powered up, only to be used in single rank mode.
56	RW	MBA_CAL0Q_DBG_BUS_BIT: Debug bus bit.
57	RW	MBA_CAL0Q_RESET_RECOVER: DDR reset recover.
58	RW	MBA_CAL0Q_CFG_RANK_SM_STALL_DISABLE: When enabled, require a minimum 1K cycle stall between all new calibration timer starts.
59	RW	MBA_CAL0Q_CFG_ENABLE_SPEC_ATTN: Allow FIR attention to cause spec attn.
60	RW	MBA_CAL0Q_CFG_ENABLE_HOST_ATTN: Allow FIR attention to cause host attn.
61:63	RW	MBA_CAL0Q_RESERVED_61_63: Reserved.

Register Name	DDR Calibration Register
Mnemonic	MC01.PORT1.SRQ.MBA_CAL1Q
Address	0000000007010950 (SCOM)
Description	DDR Calibration registers

Bits	SCOM	Field Mnemonic: Description
0	RW	MBA_CAL1Q_CFG_CAL_INTERVAL_TMR1_ENABLE: Enable interval tmr1.
1:2	RW	MBA_CAL1Q_CFG_TIME_BASE_TMR1: Time base for interval tmr1 counter.
3:11	RW	MBA_CAL1Q_CFG_INTERVAL_COUNTER_TMR1: Interval timer based on time_base(time_base × interval_counter).
12	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL1_ENABLE: Enable bit for first calibration to perform when timer pops. Should always be 1 if the timer is enabled.
13:16	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL1_TYPE: 10XX = Internal ZQ calibration (cal_rank ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step. 0011 = Periodic calibration: Run SysClk, DQS, and read eye all in parallel (default behavior).

Bits	SCOM	Field Mnemonic: Description
17	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL1_DDR_DONE: Use the complete signal from the DDR for cal1.
18	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL2_ENABLE: Enable bit for second calibration to perform when timer pops.
19:22	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL2_TYPE: 10XX = Internal ZQ calibration (cal_rank ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step. 0011 = Periodic calibration: Run SysClk, DQS, and read eye all in parallel (default behavior).
23	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL2_DDR_DONE: Use the complete signal from the DDR for cal2.
24	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL3_ENABLE: Enable bit for third calibration to perform when timer pops.
25:28	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL3_TYPE: 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step. 0011 = Periodic calibration: Run SysClk, DQS, and read eye all in parallel (default behavior).
29	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL3_DDR_DONE: Use the complete signal from the DDR for cal3.
30:38	RW	MBA_CAL1Q_CFG_CAL_TMR1_Z_SYNC: The timer value will be set to this value during z sync.
39	RW	MBA_CAL1Q_CFG_CAL_TMR1_SINGLE_RANK: Enable single-rank mode for timer1 calibrations. Calibrations programmed in tmr1 will run on one rank at a time per timer expiration. 0 = Issue calibrations for all enabled ranks per timer expiration. 1 = Issue calibrations for one rank at a time per timer expiration.
40:47	RW	MBA_CAL1Q_CFG_CAL_RANK_ENABLE: Cal Rank Enable.
48:63	RW	MBA_CAL1Q_RESERVED_48_63: Reserved.

Register Name	DDR Calibration Register
Mnemonic	MC01.PORT1.SRQ.MBA_CAL2Q
Address	0000000007010951 (SCOM)
Description	DDR Calibration registers

Bits	SCOM	Field Mnemonic: Description
0	RW	MBA_CAL2Q_CFG_CAL_INTERVAL_TMR2_ENABLE: Enable interval tmr2.
1:2	RW	MBA_CAL2Q_CFG_TIME_BASE_TMR2: Time base for interval tmr2 counter.
3:11	RW	MBA_CAL2Q_CFG_INTERVAL_COUNTER_TMR2: Interval timer based on time_base (time_base × interval_counter).
12	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL1_ENABLE: Enable bit for the first calibration to perform when the timer pops. Should always be 1 if the timer is enabled.
13:16	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL1_TYPE: 10XX = Internal ZQ calibration (cal_rank ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step. 0011 = Periodic calibration: Run SysClk, DQS, and read eye all in parallel (default behavior).
17	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL1_DDR_DONE: Use the complete signal from the DDR for cal1.

Bits	SCOM	Field Mnemonic: Description
18	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL2_ENABLE: Enable bit for the second calibration to perform when the timer pops.
19:22	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL2_TYPE: 10XX = Internal ZQ calibration (cal_rank ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step. 0011 = Periodic calibration: Run SysClk, DQS, and read eye all in parallel (default behavior).
23	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL2_DDR_DONE: Use the complete signal from the DDR for cal2.
24	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL3_ENABLE: Enable bit for the third calibration to perform when the timer pops.
25:28	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL3_TYPE: 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step. 0011 = Periodic calibration: Run SysClk, DQS, and read eye all in parallel (default behavior).
29	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL3_DDR_DONE: Use the complete signal from the DDR for cal3.
30:38	RW	MBA_CAL2Q_CFG_CAL_TMR2_Z_SYNC: The timer value will be set to this value during z sync.
39	RW	MBA_CAL2Q_CFG_CAL_TMR2_SINGLE_RANK: Enable single-rank mode for timer2 calibrations. Calibrations programmed in tmr2 will run on one rank at a time per timer expiration. 0 = Issue calibrations for all enabled ranks per timer expiration. 1 = Issue calibrations for one rank at a time per timer expiration.
40	RW	MBA_CAL2Q_CFG_CAL_TMR2_WAT_EVENT_ENABLE: Enable the use of tmr2 to trigger a WAT event. No other calibrations should be enabled. Must be used with the HW221617 CKSW enabled.
41:63	RW	MBA_CAL2Q_RESERVED_41_63: Reserved.

Register Name	DDR Calibration Length Register
Mnemonic	MC01.PORT1.SRQ.MBA_CAL3Q
Address	0000000007010952 (SCOM)
Description	DDR Calibration length registers

Bits	SCOM	Field Mnemonic: Description
0:1	RW	MBA_CAL3Q_CFG_INTERNAL_ZQ_TB: Internal ZQ time base. Time base for internal ZQ cal counter.
2:9	RW	MBA_CAL3Q_CFG_INTERNAL_ZQ_LENGTH: Number of internal ZQ time bases required to meet maximum internal ZQ length.
10:11	RW	MBA_CAL3Q_CFG_EXTERNAL_ZQ_TB: External ZQ time base. Time base for external ZQ cal counter.
12:19	RW	MBA_CAL3Q_CFG_EXTERNAL_ZQ_LENGTH: Number of external ZQ time bases required to meet maximum external ZQ length.
20:21	RW	MBA_CAL3Q_CFG_RDCLK_SYSCLK_TB: ReadclkSysclk time base. Time base for readclksysclk cal counter.
22:29	RW	MBA_CAL3Q_CFG_RDCLK_SYSCLK_LENGTH: Number of Readclksysclk time bases required to meet maximum rdclk length.
30:31	RW	MBA_CAL3Q_CFG_DQS_ALIGNMENT_TB: DQS alignment time base. Time base for DQS alignment cal counter.

Bits	SCOM	Field Mnemonic: Description
32:39	RW	MBA_CAL3Q_CFG_DQS_ALIGNMENT_LENGTH: Number of DQS alignment time bases required to meet maximum DQS alignment length.
40:41	RW	MBA_CAL3Q_CFG_MPR_READEYE_TB: Readeye time base. Time base for readeye cal counter.
42:49	RW	MBA_CAL3Q_CFG_MPR_READEYE_LENGTH: Number of readeye time bases required to meet maximum external ZQ length.
50:51	RW	MBA_CAL3Q_CFG_ALL_PERIODIC_TB: All Periodics time base. Time base for all periodic cal counter.
52:59	RW	MBA_CAL3Q_CFG_ALL_PERIODIC_LENGTH: Number of all_periodic time bases required to meet maximum calibration length for all periodic calibration (in parallel).
60	RW	MBA_CAL3Q_CFG_FREEZE_ON_PARITY_ERROR_DIS: Disable freezing MBA execution when a parity error is detected.
61:63	RW	MBA_CAL3Q_RESERVED_61_63: Reserved.

Register Name	**Final ARB Parameters Register**
Mnemonic	MC01.PORT1.SRQ.MBA_FARB0Q
Address	0000000007010953 (SCOM)
Description	Final ARB parameters

Bits	SCOM	Field Mnemonic: Description
0:15	RW	MBA_FARB0Q_CFG_MISR_BLOCK: When a bit is set, an area of logic is not included in the z-sync MISR computation. Each bit independently gates (blocks) that area of logic from the MISR. b0: gate refresh pulse b1 - 3: gate cal timers 0-2 b4: gate nm pulse b5 - 8: gate MCBIST tb pulses b9 - 15: gate farb requests
16	RW	MBA_FARB0Q_CFG_MISR_FEEDBACK_ENABLE: Allow the z-sync MISR to use circular feedback and retain state beyond its 10-latch pipe.
17	RW	MBA_FARB0Q_CFG_2N_ADDR: Enable 2N/2T address mode.
18:19	RW	MBA_FARB0Q_RESERVED_18_19: Reserved.
20:23	RW	MBA_FARB0Q_CFG_ACT_SAME_RANK_HOLD_TIME: Time after activate to prefer subsequent activates to the same rank.
24:30	RW	MBA_FARB0Q_CFG_MAX_READS_IN_A_ROW: Limits the maximum number of reads in a row, before forcing a write. There must be a write in the WRQ for the counting to start. 0x00 = Disabled. 0x01 = 1 read before allowing a write. 0x7F = 127 reads before forcing a write.
31:37	RW	MBA_FARB0Q_CFG_MAX_WRITES_IN_A_ROW: Limits the maximum number of writes in a row, before forcing a read. There must be a read in the RRQ for the counting to start. 0x00 = Disabled. 0x01 = 1 write before allowing a read. 0x7F = 127 write before forcing a read.
38	RW	MBA_FARB0Q_CFG_PARITY_AFTER_CMD: Determines whether OE is driven on the parity cycle 0 = OE will not be driven on the parity cycle. 1 = OE will be driven on the parity cycle.
39	RWX	MBA_FARB0Q_CFG_INJECT_PARITY_ERR_WEN: Inject a parity error on WEN on next CAS.
40	RWX	MBA_FARB0Q_CFG_INJECT_PARITY_ERR_ADDR5: Inject a parity error on ADDR5 on next CAS.

Bits	SCOM	Field Mnemonic: Description
41:42	RWX	MBA_FARB0Q_CFG_BW_WINDOW_SIZE: For optional size reads: 00 = Determine BW over 1K cycle window 01 = Determine BW over 2K cycle window 10 = Determine BW over 4K cycle window 11 = Determine BW over 8K cycle window
43:47	RW	MBA_FARB0Q_CFG_PARITY_DETECT_TIME: Measures the time from an injected error until when the error is detected back at the MBA.
48:53	RW	MBA_FARB0Q_CFG_RCD_PROTECTION_TIME: Time interval in which commands were sent out before an RCD parity error occurrence that should be re-issued. Should be set ≥ to cfg_parity_detect_time.
54	RW	MBA_FARB0Q_CFG_DISABLE_RCD_RECOVERY: Disable the RCD recovery procedure.
55	RW	MBA_FARB0Q_CFG_OE_ALWAYS_ON: Force DDR OE to always be on(never tristate the DDR address drivers).
56	RW	MBA_FARB0Q_CFG_FARB_CLOSE_ALL_PAGES: Before switching direction on the DRAM bus, require all committed accesses to be issued to any open pages. When set, no new activates can be issued for reads until all writes to open pages are sent. No new activates can be issued for writes until all reads to open pages are issued.
57	RW	MBA_FARB0Q_CFG_PORT_FAIL_DISABLE: Disable Port Fail after recurring RCD errors.
58	RW	MBA_FARB0Q_CFG_OE_ALL_CKE_POWERED_DOWN: Only precisely turn off cmd-addr output enable after all CKEs are powered down.
59	RW	MBA_FARB0Q_CFG_INJECT_PARITY_ERR_CONSTANT: If set, parity errors are injected continuously; otherwise, parity errors are injected only once.
60	RW	MBA_FARB0Q_CFG_FINISH_WR_BEFORE_RD: This is to prevent writes from holding up banks for a long period of time. If set, all committed writes must be issued before reads can proceed.
61:63	RW	MBA_FARB0Q_CFG_OPT_RD_SIZE: For optional size reads: 000 = Treat all 64-byte/128-byte-opt reads as 64-byte reads. 001 = Treat all 64-byte/128-byte-opt reads as 128-byte reads. 010 = If DRAM data bus utilization greater than 50%, do optional-size reads as 64 bytes. 011 = If DRAM data bus utilization greater than 62.5%, do optional-size reads as 64 bytes. 100 = If DRAM data bus utilization greater than 75.0%, do optional-size reads as 64 bytes. 101 = If DRAM data bus utilization greater than 87.5%, do optional-size reads as 64 bytes. 11X = Reserved.

Register Name	Final ARB Parameters Register
Mnemonic	MC01.PORT1.SRQ.MBA_FARB1Q
Address	0000000007010954 (SCOM)
Description	Final ARB parameters

Bits	SCOM	Field Mnemonic: Description
0:2	RW	MBA_FARB1Q_CFG_SLOT0_S0_CID: Chip ID bits for Slot 0 Master 0/1 Slave 0.
3:5	RW	MBA_FARB1Q_CFG_SLOT0_S1_CID: Chip ID bits for Slot 0 Master 0/1 Slave 1.
6:8	RW	MBA_FARB1Q_CFG_SLOT0_S2_CID: Chip ID bits for Slot 0 Master 0/1 Slave 2.
9:11	RW	MBA_FARB1Q_CFG_SLOT0_S3_CID: Chip ID bits for Slot 0 Master 0/1 Slave 3.
12:14	RW	MBA_FARB1Q_CFG_SLOT0_S4_CID: Chip ID bits for Slot 0 Master 0/1 Slave 4 or Chip ID bits for Slot 0 Master 2/3 Slave 0.
15:17	RW	MBA_FARB1Q_CFG_SLOT0_S5_CID: Chip ID bits for Slot 0 Master 0/1 Slave 5 or Chip ID bits for Slot 0 Master 2/3 Slave 1.

Bits	SCOM	Field Mnemonic: Description
18:20	RW	MBA_FARB1Q_CFG_SLOT0_S6_CID: Chip ID bits for Slot 0 Master 0/1 Slave 6 or Chip ID bits for Slot 0 Master 2/3 Slave 2.
21:23	RW	MBA_FARB1Q_CFG_SLOT0_S7_CID: Chip ID bits for Slot 0 Master 0/1 Slave 7 or Chip ID bits for Slot 0 Master 2/3 Slave 3.
24:26	RW	MBA_FARB1Q_CFG_SLOT1_S0_CID: Chip ID bits for Slot 1 Master 0/1 Slave 0.
27:29	RW	MBA_FARB1Q_CFG_SLOT1_S1_CID: Chip ID bits for Slot 1 Master 0/1 Slave 1.
30:32	RW	MBA_FARB1Q_CFG_SLOT1_S2_CID: Chip ID bits for Slot 1 Master 0/1 Slave 2.
33:35	RW	MBA_FARB1Q_CFG_SLOT1_S3_CID: Chip ID bits for Slot 1 Master 0/1 Slave 3.
36:38	RW	MBA_FARB1Q_CFG_SLOT1_S4_CID: Chip ID bits for Slot 1 Master 0/1 Slave 4 or Chip ID bits for Slot 1 Master 2/3 Slave 0.
39:41	RW	MBA_FARB1Q_CFG_SLOT1_S5_CID: Chip ID bits for Slot 1 Master 0/1 Slave 5 or Chip ID bits for Slot 1 Master 2/3 Slave 1.
42:44	RW	MBA_FARB1Q_CFG_SLOT1_S6_CID: Chip ID bits for Slot 1 Master 0/1 Slave 6 or Chip ID bits for Slot 1 Master 2/3 Slave 2.
45:47	RW	MBA_FARB1Q_CFG_SLOT1_S7_CID: Chip ID bits for Slot 1 Master 0/1 Slave 7 or Chip ID bits for Slot 1 Master 2/3 Slave 3.
48	RW	MBA_FARB1Q_CFG_DIS_SMDR: Set to 1 if using a 5D configuration. This uses the different master parameters instead of the SMDR.
49	RW	MBA_FARB1Q_CFG_DDR4_PARITY_ON_CID_DIS: Exclude CID bits in parity generation for DDR4.
50:63	RW	MBA_FARB1Q_CFG_RSV0: Reserved.

Register Name	Final ARB Parameters Register
Mnemonic	MC01.PORT1.SRQ.MBA_FARB2Q
Address	0000000007010955 (SCOM)
Description	Final ARB parameters

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MBA_FARB2Q_CFG_RANK0_RD_ODT: ODT bits required for a read Master Rank 0.
4:7	RW	MBA_FARB2Q_CFG_RANK1_RD_ODT: ODT bits required for a read Master Rank 1.
8:11	RW	MBA_FARB2Q_CFG_RANK2_RD_ODT: ODT bits required for a read Master Rank 2.
12:15	RW	MBA_FARB2Q_CFG_RANK3_RD_ODT: ODT bits required for a read Master Rank 3.
16:19	RW	MBA_FARB2Q_CFG_RANK4_RD_ODT: ODT bits required for a read Master Rank 4.
20:23	RW	MBA_FARB2Q_CFG_RANK5_RD_ODT: ODT bits required for a read Master Rank 5.
24:27	RW	MBA_FARB2Q_CFG_RANK6_RD_ODT: ODT bits required for a read Master Rank 6.
28:31	RW	MBA_FARB2Q_CFG_RANK7_RD_ODT: ODT bits required for a read Master Rank 7.
32:35	RW	MBA_FARB2Q_CFG_RANK0_WR_ODT: ODT bits required for a write Master Rank 0.
36:39	RW	MBA_FARB2Q_CFG_RANK1_WR_ODT: ODT bits required for a write Master Rank 1.
40:43	RW	MBA_FARB2Q_CFG_RANK2_WR_ODT: ODT bits required for a write Master Rank 2.
44:47	RW	MBA_FARB2Q_CFG_RANK3_WR_ODT: ODT bits required for a write Master Rank 3.
48:51	RW	MBA_FARB2Q_CFG_RANK4_WR_ODT: ODT bits 4equired for a write Master Rank 4.
52:55	RW	MBA_FARB2Q_CFG_RANK5_WR_ODT: ODT bits required for a write Master Rank 5.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	MBA_FARB2Q_CFG_RANK6_WR_ODT: ODT bits required for a write Master Rank 6.
60:63	RW	MBA_FARB2Q_CFG_RANK7_WR_ODT: ODT bits required for a write Master Rank 7.

Register Name	N/M Throttling Control Register
Mnemonic	MC01.PORT1.SRQ.MBA_FARB3Q
Address	0000000007010956 (SCOM)
Description	N/M Throttling Control

Bits	SCOM	Field Mnemonic: Description
0:14	RW	MBA_FARB3Q_CFG_NM_N_PER_SLOT: The N value for the NM throttling across a single slot. The maximum command count that can occur over a time interval M for one slot.
15:30	RW	MBA_FARB3Q_CFG_NM_N_PER_PORT: The N value for the NM throttling across the entire port (both slots). The maximum command count that can occur over a time interval M for the entire port.
31:44	RW	MBA_FARB3Q_CFG_NM_M: The M value for the NM throttling. This counts DRAM clock cycles. Set this to 0 to disable NM throttling.
45:47	RW	MBA_FARB3Q_CFG_NM_RAS_WEIGHT: The increment to be added to the N count each time a RAS is sent.
48:50	RW	MBA_FARB3Q_CFG_NM_CAS_WEIGHT: The increment to be added to the N count each time a CAS is sent.
51	RW	MBA_FARB3Q_RESERVED_51: Reserved.
52	RW	MBA_FARB3Q_RESERVED_52: Reserved.
53	RW	MBA_FARB3Q_CFG_NM_CHANGE_AFTER_SYNC: If set, changes to cfg_nm_n_per_slot, cfg_nm_n_per_port, cfg_nm_m, min_max_domains will only be applied after a pc_sync command is seen.
54:63	RW	MBA_FARB3Q_RESERVED_54_63: Reserved.

Register Name	Final Command Arbiter Miscellaneous Register
Mnemonic	MC01.PORT1.SRQ.MBA_FARB4Q
Address	0000000007010957 (SCOM)
Description	Final command arbiter miscellaneous

Bits	SCOM	Field Mnemonic: Description
0:15	RW	MBA_FARB4Q_CFG_NOISE_WAIT_TIME: The time from RCD_err until the RCD error recovery procedure will start issuing precharge commands.
16:21	RW	MBA_FARB4Q_CFG_PRECHARGE_WAIT_TIME: The time from one precharge command to the next precharge command in the RCD error recovery procedure.
22	RW	MBA_FARB4Q_CFG_SIM_FAST_NOISE_WINDOW: This will skip the precharges and refreshes as part of the noise window and only observe the noise window wait time.
23:26	RW	MBA_FARB4Q_RESERVED_23_26: Reserved.
27:41	RW	MBA_FARB4Q_EMERGENCY_N: Programmable N for NM when the emergency throttle is enabled.
42:55	RW	MBA_FARB4Q_EMERGENCY_M: Programmable M for NM when the emergency throttle is enabled.
56:63	RW	MBA_FARB4Q_RESERVED_56_63: Reserved.

Register Name	DDR Interface SCOM Control Register
Mnemonic	MC01.PORT1.SRQ.MBA_FARB5Q
Address	0000000007010958 (SCOM)
Description	DDR Interface SCOM Control

Bits	SCOM	Field Mnemonic: Description
0:1	RW	MBA_FARB5Q_CFG_DDR_DPHY_NCLK: DDR PHY nclk control.
2:3	RW	MBA_FARB5Q_CFG_DDR_DPHY_PCLK: DDR PHY pclk control.
4	RW	MBA_FARB5Q_CFG_DDR_RESETN: DDR Resetn signal.
5	RW	MBA_FARB5Q_CFG_CCS_ADDR_MUX_SEL: CCS Address Multiplexer Select. This bit should be turned on until all multiple CCS instructions are completed. 0 selects address data from the mainline logic. 1 selects address data from the CCS logic.
6	RW	MBA_FARB5Q_CFG_CCS_INST_RESET_ENABLE: When set to 1, bit 16 of the CCS_INST_ARR0 will be driven out to DDR Resetn. When set to 0, cfg_ddr_resetn will be driven out to DDR Resetn.
7	RW	MBA_FARB5Q_CFG_GP_BIT_3_ENABLE: When set to 1, the inverted value of GP(3) will be driven on the force_mclk_low signal to the DDR PHYs. When set to 0, the value of the inverted value of cfg_force_mclk_low_n will be driven on the force_mclk_low signal to the DDR PHYs.
8	RW	MBA_FARB5Q_CFG_FORCE_MCLK_LOW_N: The inverted value of force_mclk_low_n will be driven on mba_ddr_force_mclk_low when cfg_gp_bit_3_enable is 0.
9:15	RW	MBA_FARB5Q_RESERVED_56_63: Reserved.

Register Name	DDR Port Status Register
Mnemonic	MC01.PORT1.SRQ.MBA_FARB6Q
Address	0000000007010959 (SCOM)
Description	DDR Port Status Register

Bits	SCOM	Field Mnemonic: Description
0:10	ROX	MBA_FARB6Q_CFG_BW_SNAPSHOT: DRAM data bus utilization over last 4K DDR clock window. All 1s is 100 percent utilization.
11:14	ROX	MBA_FARB6Q_CFG_CKE_PUP_STATE: Indicates which of the four CKEs are on.
15	ROX	MBA_FARB6Q_CFG_STR_STATE: Indicates whether the DRAMS on this port are in STR.
16:20	ROX	MBA_FARB6Q_CFG_RRQ_DEPTH: RRQ Depth; Number of commands in RRQ.
21:25	ROX	MBA_FARB6Q_CFG_WRQ_DEPTH: WRQ Depth; Number of commands in WRQ.
26:30	ROX	MBA_FARB6Q_CFG_RCD_PARITY_DLY: Delay from parity error to error being seen back in MBA. This value can then be placed back in the RCD protection time register.
31	ROX	MBA_FARB6Q_CFG_EVENTN: EventN monitor for thermal event.

Register Name	MBA Error Report Register
Mnemonic	MC01.PORT1.SRQ.MBA_ERR_REPORTQ
Address	000000000701095A (SCOM)
Description	MBA Error report register

Bits	SCOM	Field Mnemonic: Description
0	ROX	MBA_ERR_REPORTQ_WRQ_HANG_ERR: WRQ hang error MBACALFIR Bit 17.
1	ROX	MBA_ERR_REPORTQ_RRQ_HANG_ERR: RRQ hang error MBACALFIR Bit 17.
2	ROX	MBA_ERR_REPORTQ_DSM_PE_ERR: Parity error in DSM configuration registers MBACALFIR Bit 1.
3	ROX	MBA_ERR_REPORTQ_TMR_PE_ERR: Parity error in TMR configuration registers MBACALFIR Bit 1.
4	ROX	MBA_ERR_REPORTQ_RRQ_PE_ERR: Parity error in RRQ configuration registers MBACALFIR Bit 0.
5	ROX	MBA_ERR_REPORTQ_WRQ_PE_ERR: Parity error in WRQ configuration registers MBACALFIR Bit 0.
6	ROX	MBA_ERR_REPORTQ_FARB_PE_ERR: Parity error in FARB configuration registers MBACALFIR Bit 1.
7	ROX	MBA_ERR_REPORTQ_PC_PE_ERR: Parity error in PC configuration registers MBACALFIR Bit 0.
8	ROX	MBA_ERR_REPORTQ_CAL0_PE_ERR: Parity error in Cal0 configuration register MBACALFIR Bit 0.
9	ROX	MBA_ERR_REPORTQ_CAL1_PE_ERR: Parity error in Cal1 configuration register MBACALFIR Bit 0.
10	ROX	MBA_ERR_REPORTQ_CAL2_PE_ERR: Parity error in Cal2 configuration register MBACALFIR Bit 0.
11	ROX	MBA_ERR_REPORTQ_CAL3_PE_ERR: Parity error in Cal3 configuration register MBACALFIR Bit 0.
12	ROX	MBA_ERR_REPORTQ_DDR_IF_SM_1HOT_ERR: DDR state machine one hot error MBACALFIR Bit 18.
13	ROX	MBA_ERR_REPORTQ_CAL_SM_1HOT_ERR: Calibration state machine one hot error MBACALFIR Bit 18.
14	ROX	MBA_ERR_REPORTQ_RANK_SM_1HOT_ERR: Rank state machine one hot error MBACALFIR Bit 18.
15	ROX	MBA_ERR_REPORTQ_RESERVED_15: Reserved 15.
16	ROX	MBA_ERR_REPORTQ_PC_CAL_PCFSM_1HOT_ERR: Power Control state machine 1 hot error MBACALFIR bit 18.
17	ROX	MBA_ERR_REPORTQ_FARB_CAL_RECVFSM_1HOT_ERR: Recovery state machine 1 hot error MBACALFIR bit 18.
18:23	ROX	MBA_ERR_REPORTQ_RESERVED_18_23: Reserved.
24	ROX	MBA_ERR_REPORTQ_RCMD_ASYNC_IF_ERR: Sequence error on rcmd asynchronous crossing. Operations received out of order.
25	ROX	MBA_ERR_REPORTQ_PF_PROMOTE_ASYNC_IF_ERR: Sequence error on prefetch promote asynchronous crossing. Operations received out of order.
26	ROX	MBA_ERR_REPORTQ_CANCEL_ACK_ASYNC_IF_ERR: Sequence error on cancel ACK asynchronous crossing. Operations received out of order.
27	ROX	MBA_ERR_REPORTQ_FARB_CMD_PE_HOLD_OUT: Parity error seen on new command to be issued by sequencer.
28	ROX	MBA_ERR_REPORTQ_DSM_CMD_PE_HOLD_OUT: Parity error seen on command as it leaves sequencer.
29:30	ROX	MBA_ERR_REPORTQ_RESERVED_29_30: Reserved.
31:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Emergency Throttle Register
Mnemonic	MC01.PORT1.SRQ.MBA_FARB7Q
Address	0000000007010965 (SCOM)
Description	Emergency Throttle Register

Bits	SCOM	Field Mnemonic: Description
0	RW	MBA_FARB7Q_EMER_THROTTLE_IP: Emergency Throttle in-progress. This register can also be set to manually engage emergency throttle, or cleared to clear emergency throttle.

Register Name	MBA Debug Bus Register 0
Mnemonic	MC01.PORT1.SRQ.MBA_DBG0Q
Address	0000000007010966 (SCOM)
Description	MBA Debug Bus Register 0

Bits	SCOM	Field Mnemonic: Description
0	RW	MBA_DBG0Q_CFG_DBG_SRQ_ENABLE:
1:3	RW	MBA_DBG0Q_CFG_DBG_SRQ_SEL0:
4:6	RW	MBA_DBG0Q_CFG_DBG_SRQ_SEL1:
7:9	RW	MBA_DBG0Q_CFG_DBG_SRQ_SEL2:
10:12	RW	MBA_DBG0Q_CFG_DBG_SRQ_SEL3:
13:15	RW	MBA_DBG0Q_CFG_DBG_SRQ_SEL4:
16:18	RW	MBA_DBG0Q_CFG_DBG_SRQ_SEL5:
19:21	RW	MBA_DBG0Q_CFG_DBG_SRQ_SEL6:
22:24	RW	MBA_DBG0Q_CFG_DBG_SRQ_SEL7:
25:33	RW	MBA_DBG0Q_RESERVED_25_33:
34:41	RW	MBA_DBG0Q_CFG_DBG_SRQ_SEL_OTHER_SRQ:
42:47	RW	MBA_DBG0Q_RESERVED_42_47:
48:51	RW	MBA_DBG0Q_CFG_WAT_FARB_RRQ_GT:
52:55	RW	MBA_DBG0Q_CFG_WAT_FARB_WRQ_GT:
56:59	RW	MBA_DBG0Q_CFG_WAT_FARB_REF_GT:
60:63	RW	MBA_DBG0Q_CFG_WAT_FARB_CAL_GT:

Register Name	MBA Debug Bus Register 1
Mnemonic	MC01.PORT1.SRQ.MBA_DBG1Q
Address	0000000007010967 (SCOM)
Description	MBA Debug Bus Register 1

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MBA_DBG1Q_CFG_WAT_FORCE_WR_ENTRY0_HP:
4:7	RW	MBA_DBG1Q_CFG_WAT_FORCE_RD_ENTRY0_HP:
8:11	RW	MBA_DBG1Q_CFG_WAT_FP_DIS:
12:15	RW	MBA_DBG1Q_CFG_WAT_DIS_RD_PG:
16:19	RW	MBA_DBG1Q_CFG_WAT_DIS_WR_PG:
20:23	RW	MBA_DBG1Q_CFG_WAT_PUP_ALL:
24:27	RW	MBA_DBG1Q_CFG_WAT_EXIT_STR:
28:31	RW	MBA_DBG1Q_CFG_WAT_REF_HP:
32:35	RW	MBA_DBG1Q_CFG_WAT_REF_SYNC:
36:39	RW	MBA_DBG1Q_CFG_WAT_REF_SAFE:

Bits	SCOM	Field Mnemonic: Description
40:43	RW	MBA_DBG1Q_CFG_WAT_CAL_SYNC:
44:47	RW	MBA_DBG1Q_CFG_WAT_RRQ_MNT_GT:
48:51	RW	MBA_DBG1Q_CFG_WAT_WRQ_MNT_GT:
52:55	RW	MBA_DBG1Q_CFG_WAT_SET_FIR:
56:59	RW	MBA_DBG1Q_CFG_WAT_EMER_TH:
60:63	RW	MBA_DBG1Q_CFG_WAT_START_RECOVERY:

Register Name	Emergency Throttle Register
Mnemonic	MC01.PORT1.SRQ.MBA_FARB8Q
Address	0000000007010968 (SCOM)
Description	Emergency Throttle Register

Bits	SCOM	Field Mnemonic: Description
0	RW	MBA_FARB8Q_SAFE_REFRESH_MODE: Safe refresh interval is being used for tREFI. This register can also be set to manually engage safe refresh or cleared to clear safe refresh.

Register Name	Timer State Machine Control Register
Mnemonic	MC01.PORT1.SRQ.MBA_TMR2Q
Address	000000000701096F (SCOM)
Description	Timer state machine control.

Bits	SCOM	Field Mnemonic: Description
0:19	RW	MBA_TMR2Q_CFG_BANK_BUSY_FSM_DIS: Disable bank busy state machines 0-19, one bit per FSM.
20:31	RW	MBA_TMR2Q_CFG_BANK_BUSY_OPEN_PAGE_DIS: Disable open page mode on bank busy state machines 0-11, one bit per FSM. Bank busy state machines 12-19 do not do open page mode.
32:63	RW	MBA_TMR2Q_RESERVED_32_63: Reserved.

Register Name	Refresh Register 0
Mnemonic	MC01.PORT1.SRQ.PC.MBAREF0Q
Address	0000000007010972 (SCOM)
Description	Refresh register 0

Bits	SCOM	Field Mnemonic: Description
0	RW	MBAREF0Q_CFG_REFRESH_ENABLE: Refresh enable.
1:2	RW	MBAREF0Q_CFG_REFRESH_INTERVAL_TIMEBASE_SELECT: 01 = Reserved For 10 and 11 settings, to determine the actual refresh interval, you must multiply the calculated refresh interval by 8k or 2^{22} depending on which timebase was used. **Note**: Settings 10 and 11 are for characterization stress testing only.
3	RW	MBAREF0Q_CFG_PER_BANK_REFRESH: Banks are individually refreshed each time a new refresh to a rank pops. Refresh must be sent to each bank separately before that refresh is considered complete. DDR4E only.

Bits	SCOM	Field Mnemonic: Description
4	RW	MBAREF0Q_CFG_REFRESH_DEBUG_SELECT: Refresh debug bus select. 0 selects only master ranks. 1 selects slave ranks
5:7	RW	MBAREF0Q_CFG_REFRESH_PRIORITY_THRESHOLD: After the number of queued refreshes to a rank reaches this threshold, that rank's refreshes become high priority. Values greater than 0x5 can potentially lead to a refresh timeout FIR.
8:18	RW	MBAREF0Q_CFG_REFRESH_INTERVAL: This value is multiplied by 8 to represent the number of DRAM command clock cycles at which a refresh is to be sent to a rank in order to honor the refresh interval (tREFI). A refresh to a specific rank will be seen 8 × cfg_refresh_interval × num_ranks × DRAM_command_clock_cycle_time. So, program this dial to: cfg_refresh_interval=desired_tREFI_in_usnum_ranksDRAM_command_clock_cycle_in_ns.008). For example, for a system with two master ranks and 4 slaves per master (8 ranks total), a desired refresh interval of 7.8 µs, and DDR-1600 memory, cfg_refresh_interval=7.881.25.008=97 (round down).
19:29	RW	MBAREF0Q_CFG_REFRESH_RESET_INTERVAL: This is value to load the refresh interval counter to when a syncreset pulse is seen from MBA. This is used to offset refreshing to the different MBAs. **Note**: Refresh reset interval should be set to a value less than the refresh interval.
30:39	RW	MBAREF0Q_CFG_TRFC: Refresh to activate rank protection timer.
40:49	RW	MBAREF0Q_CFG_REFR_TSV_STACK: Refresh to Refresh spacing within the same TSV stack timer.
50:60	RW	MBAREF0Q_CFG_REFR_CHECK_INTERVAL: This setting is used to verify the refresh rules are upheld only (it is not the actual refresh interval). It is multiplied by 8 to represent the number of DRAM command clock cycles at which a refresh is to be seen to a given rank in order to honor the refresh interval (tREFI). A refresh to a specific rank should be seen 8 × cfg_refresh_check_interval × DRAM_command_clock_cycle_time. So, program this dial to: cfg_refr_check_interval=desired_tREFI_in_usDRAM_command_clock_cycle_in_ns.008). For example, if using DDR-1600 memory and expecting a refresh to occur every 7.8 µs: cfg_refr_check_interval = 7.81.25.008 = 780=0x30C If using DDR-1600 memory and expecting a refresh every 3.9 µs: cfg_refr_check_interval = 3.91.25.008 = 390 = 0x186.
61	RW	MBAREF0Q_CFG_TRFC_STACK_GATE_ALL_REF: When set, this causes all refreshes to be spaced by cfg_refr_tsv_stack, regardless of whether they are to ranks on the same stack. This mode can be enabled to reduce the power impact due to a burst of refreshes to different ranks.
62:63	RW	MBAREF0Q_RESERVED_62_63: Reserved.

Register Name	Reserved SCOM Address Register
Mnemonic	MC01.PORT1.SRQ.PC.MBARSVD0
Address	0000000007010973 (SCOM)
Description	Reserved SCOM Register Address

Bits	SCOM	Field Mnemonic: Description
0:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000000000000000000000

Register Name	Power Control Register 0
Mnemonic	MC01.PORT1.SRQ.PC.MBARPC0Q
Address	0000000007010974 (SCOM)
Description	Power control register 0

Bits	SCOM	Field Mnemonic: Description
0:1	RW	MBARPC0Q_RESERVED_0_1: Reserved.

Bits	SCOM	Field Mnemonic: Description
2	RW	MBARPC0Q_CFG_MIN_MAX_DOMAINS_ENABLE: This is an overall enable for power domain control. If power control is disabled, the CKEs will always be set to a '1'.
3:5	RW	MBARPC0Q_CFG_MIN_MAX_DOMAINS: Configures dynamic power up and power down of CKEs within specified minmax limits. Maxall_minall means power control will not limit the number of domains accessible at a given time. Power domains will not be powered down even if they go idle, unless min_domain_reduction is enabled. Maxall_minx will permit idle power down to reduce the number of domains powered up after a domain has gone idle, but it will not restrict the maximum domains powered up. Max1_minx restricts the number of domains that can be powered up at a given time to 1.
6:10	RW	MBARPC0Q_CFG_PUP_AVAIL: Specifies how many DRAM command clocks for power control to wait from CKE going high to activate.
11:15	RW	MBARPC0Q_CFG_PDN_PUP: Specifies how many DRAM command clocks for power control to wait from CKE going low to high again (enforces minimum time in power down).
16:20	RW	MBARPC0Q_CFG_PUP_PDN: Specifies how many DRAM command clocks for power control to wait from CKE going high to low again (enforces minimum time powered up).
21	RW	MBARPC0Q_RESERVED_21: Reserved.
22	RW	MBARPC0Q_CFG_MIN_DOMAIN_REDUCTION_ENABLE: This allows a dynamic reduction of the minimum domains to 0 when no memory traffic has been seen over the specified cfg_min_domain_reduction_time; minimum domains will be restored after traffic is seen; the adjusted minimum domains will not be reflected in or over-write the cfg_min_max_domains setting (adjustment made internal to logic).
23:32	RW	MBARPC0Q_CFG_MIN_DOMAIN_REDUCTION_TIME: Specifies how many DRAM command clocks the MBA must be idle before min_cke is reduced to 0.
33	RW	MBARPC0Q_CFG_PUP_AFTER_ACTIVATE_WAIT_ENABLE: After a configurable time has been met since the last activate, a subsequent domain can be powered up, even if the powering-down domain has not been powered down yet.
34:41	RW	MBARPC0Q_CFG_PUP_AFTER_ACTIVATE_WAIT_TIME: Specifies how many DRAM command clocks the MBA must be idle before minimum domains is reduced to 0.
42	RW	MBARPC0Q_CFG_FORCE_SPARE_PUP: Forces all spare CKEs to couple with their respective primary CKEs. This bit should not be toggled during run time or when calibration is enabled.
43	RW	MBARPC0Q_CFG_MIN_DOMAIN_REDUCTION_CNT_REFR_INT: If set, use refresh interval for minimum domain reduction time interval. Otherwise, use DRAM clocks as interval.
44:46	RW	MBARPC0Q_CFG_EMER_MIN_MAX_DOMAIN: This is minmax power domain setting that power control will revert to when emergency throttling is engaged.
47	RW	MBARPC0Q_CFG_PUP_ALL_WRITES_PENDING: Enabling this allows a domain to be powered up upon a write entering the write reorder queue (provided the maximum domains is set to all). **Note**: Reads always cause a power up to their power domain upon entering the read reorder queue (when maximum domains is set to all).
48	RW	MBARPC0Q_CFG_ALWAYS_WAIT_ACT_TIME: If set, when in single domain power up mode, we will always wait the configured time between activates even when all domains are powered down already.
49:63	RW	MBARPC0Q_RESERVED_49_63: Reserved.

Register Name	**STR Register 0**
Mnemonic	MC01.PORT1.SRQ.PC.MBASTR0Q
Address	0000000007010975 (SCOM)
Description	STR Register 0

Bits	SCOM	Field Mnemonic: Description
0	RW	MBASTR0Q_CFG_STR_ENABLE: Enable STR Entry. **Note**: Minimum-maximum domains must also be enabled to enter STR.
1	RW	MBASTR0Q_CFG_DIS_CLK_IN_STR: Disable memory clocks when in STR.
2:11	RW	MBASTR0Q_CFG_ENTER_STR_TIME: Number of cfg_min_domain_reduction intervals of idle to wait before entering STR.
12:16	RW	MBASTR0Q_CFG_TCKESR: tCKESR
17:21	RW	MBASTR0Q_CFG_TCKSRE: tCKSRE
22:26	RW	MBASTR0Q_CFG_TCKSRX: tCKSRX
27:37	RW	MBASTR0Q_CFG_TXSDLL: tXSDLL
38:45	RW	MBASTR0Q_CFG_TRFC_COUNTER_DIS: Per tRFC counter disable; Can use this to restrict the number of outstanding refreshes.
46:56	RW	MBASTR0Q_CFG_SAFE_REFRESH_INTERVAL: This is the refresh interval used when in safe-refresh (high-temp) mode. This value is multiplied by 8 to represent the number of DRAM command clock cycles at which a refresh is to be sent to a rank in order to honor the refresh interval (tREFI). A refresh to a specific rank will be seen 8 × cfg_safe_refresh_interval × num_ranks × DRAM_command_clock_cycle_time. So, program this dial to: cfg_safe_refresh_interval = desired_tREFI_in_usnum_ranksDRAM_command_clock_cycle_in_ns.008). For example, for a system with two master ranks and four slaves per master (8 ranks total), a desired refresh interval of 7.8 µs, and DDR-1600 memory, cfg_safe_refresh_interval = 7.881.25.008 = 97 (round down).
57:60	RW	MBASTR0Q_CFG_OCC_DEADMAN_TIMER_SEL: This selects one of 8 timeout values for the OCC deadman timer. If the OCC is idle for the programmed timeout value × timebase pulse, an emergency throttle command command is issued and refresh is set to safe refresh interval. Value Time 0000 = Disabled 0001 = 16 timebase pulses 0010 = 4 timebase pulses 0011 = 8 timebase pulses 0100 = 16 timebase pulses 0101 = 32 timebase pulses 0110 = 64 timebase pulses 0111 = 128 timebase pulses 1000 = 255 timebase pulses 1001 to 1111 are unused.
61	RW	MBASTR0Q_CFG_OCC_DEADMAN_TB_SEL: This selects which timebase pulse to use for the deadman timer. 0 = 1 in 2^{22} DRAM command clocks 1 = 1 in 8K DRAM command clocks
62:63	RW	MBASTR0Q_RESERVED_62_63: Reserved.

Register Name	Refresh Avoidance Control Register
Mnemonic	MC01.PORT1.SRQ.PC.MBAREFAQ
Address	0000000007010976 (SCOM)
Description	Refresh Avoidance Control Register

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MBAREFAQ_CFG_STATIC_IDLE_DLY: This is the number of cycles that the refresh logic will wait for a rank to be idle in the RRQ before sending a low-priority refresh. **Note**: This delay counts in multiples of four DDR clocks (per default low-priority refresh subcounter setting).

Bits	SCOM	Field Mnemonic: Description
4:5	RW	MBAREFAQ_CFG_LP_SUB_CNT: Subcounter for low-priority refresh scheduling dials. For dials that count based on this subcounter, a value of 00 means the counter those dials compare against increments every one cycle. A value of 01 in this register means the higher level count increments every fourth cycle (10 is every eighth cycle and 11 is every 16th cycle).
6	RW	MBAREFAQ_CFG_REFRESH_HP_RANK_BLOCK_ENABLE: When enabled, the refresh logic sends a block signal when issuing a high-priority refresh. The block signal prevents new demand requests to the refreshing rank from overwhelming the read reorder queue.
7:9	RW	MBAREFAQ_RESERVED_7_9: Reserved.
10:15	RW	MBAREFAQ_CFG_REF_BLOCK_STOP_DLY: Programmable setting that is subtracted from the tRFC timer. The result is used to determine when the block signal can be deasserted leading up to the end of a tRFC period. This allows new commands targeting the refresh domain being refreshed to progress to the RRQ so that they are ready to go as soon as tRFC ends. (N)

Register Name	Performance Monitor Counts0 Register
Mnemonic	MC01.PORT1.SRQ.MBA_PMU0Q
Address	0000000007010977 (SCOM)
Description	Performance monitor counts0

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MBA_PMU0Q_READ_COUNT: Read count. Increments every read; wraps.
32:63	ROX	MBA_PMU0Q_WRITE_COUNT: Write count. Increments every write; wraps.

Register Name	Performance Monitor Counts1 Register
Mnemonic	MC01.PORT1.SRQ.MBA_PMU1Q
Address	0000000007010978 (SCOM)
Description	Performance monitor counts1

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MBA_PMU1Q_ACTIVATE_COUNT: Bank activate count. Increments for every activate; wraps.
32:63	ROX	MBA_PMU1Q_PU_COUNTS: Counts the number of rising edges for a CKE; wraps.

Register Name	Performance Monitor Counts2 Register
Mnemonic	MC01.PORT1.SRQ.MBA_PMU2Q
Address	0000000007010979 (SCOM)
Description	Performance monitor counts2

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MBA_PMU2Q_FRAME_COUNT: Frame count. Increments every DRAM clock(2:1) clock.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Performance Monitor Counts4 Register
Mnemonic	MC01.PORT1.SRQ.MBA_PMU3Q
Address	000000000701097A (SCOM)
Description	Performance monitor counts4

Bits	SCOM	Field Mnemonic: Description
0:15	RW	MBA_PMU3Q_LOW_IDLE_THRESHOLD: Each time the low idle (no reads or writes queued) threshold is met, the low idle count increments. Between periods of command activity, there may be multiple low-idle-threshold-width windows of command inactivity. For each of these windows, the low idle count is incremented. (counts 2:1 DRAM address frequency) counts MBA idle cycles.
16:31	RW	MBA_PMU3Q_MED_IDLE_THRESHOLD: Each time the medium idle (no reads or writes queued) threshold is met, the medium idle count increments. Between periods of command activity, there may be multiple medium-idle-threshold-width windows of command inactivity. For each of these windows, the medium idle count will be incremented.
32:63	RW	MBA_PMU3Q_HIGH_IDLE_THRESHOLD: Each time the high idle (no reads or writes queued) threshold is met, the high idle count increments. Between periods of command activity, there may be multiple high-idle-threshold-width windows of command inactivity. For each of these windows, the high idle count is incremented.

Register Name	Performance Monitor Counts Register
Mnemonic	MC01.PORT1.SRQ.MBA_PMU4Q
Address	000000000701097B (SCOM)
Description	Performance monitor counts

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MBA_PMU4Q_BASE_IDLE_COUNT: Increments every MBA idle cycle (counts 2:1 DRAM address frequency).
32:63	ROX	MBA_PMU4Q_LOW_IDLE_COUNT: Counts the number of times the low idle threshold was met (counts 2:1 DRAM address frequency).

Register Name	Performance Monitor Counts Register
Mnemonic	MC01.PORT1.SRQ.MBA_PMU5Q
Address	000000000701097C (SCOM)
Description	Performance monitor counts

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MBA_PMU5Q_MED_IDLE_COUNT: Counts the number of times the medium idle threshold was met (counts 2:1 DRAM address frequency).
32:63	ROX	MBA_PMU5Q_HIGH_IDLE_COUNT: Counts the number of times the high idle threshold was met (counts 2:1 DRAM address frequency).

Register Name	Performance Monitor Counts Register
Mnemonic	MC01.PORT1.SRQ.MBA_PMU6Q
Address	000000000701097D (SCOM)
Description	Performance monitor counts

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	MBA_PMU6Q_EVENT0_COUNTER: PMU count for event 0.
16:31	ROX	MBA_PMU6Q_EVENT1_COUNTER: PMU count for event 1.
32:47	ROX	MBA_PMU6Q_EVENT2_COUNTER: PMU count for event 2.
48:63	ROX	MBA_PMU6Q_EVENT3_COUNTER: PMU count for event 3.

Register Name	Performance Monitor Event Select Register
Mnemonic	MC01.PORT1.SRQ.MBA_PMU7Q
Address	000000000701097E (SCOM)
Description	Performance monitor event select register

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MBA_PMU7Q_CFG_EVENT0_SELECT: Event0 select. 0x00 = MBA command clocks 0x01 = ACT all 0x02 = ACT for read 0x03 = ACT for write 0x04 = CAS all 0x05 = CAS for read 0x06 = CAS for write 0x07 = CAS for low-priority write 0x08 = CAS for high-priority write 0x09 = PRE all 0x0a = PRE for read 0x0b = PRE for write 0x0c = REF high priority 0x0d = REF low priority 0x0e = REF all 0x0f = RRQ empty 0x10 = RRQ full 0x11 = WRQ empty 0x12 = WRQ full 0x13 = WRQ above hw mark 0x14 = Reserved 0x15 = activate with direction switch (change from rd→wr or wr→rd) 0x16 = activate with mrank switch (Master rank different than previous ACT) 0x17 = activate with srank switch (Same master; slave rank different than previous ACT) 0x18 = activate with bank group switch (Same master, slave; bank group different than previous ACT) 0x19 = activate with bank switch (Same master, slave, bank group; different bank than previous ACT) 0x1a = all bank timers full 0x1b any CKE PUP transition (0→1) 0x1c = CKE0 cycles PUP 0x1d = CKE1 cycles PUP 0x1e = CKE2 cycles PUP 0x1f = CKE3 cycles PUP 0x20 = WDF stalled waiting on read buffer 0x21 = WDF stalled waiting on read ramp 0x22 = Command0 Compare 0x23 - 0x3f = Reserved

Bits	SCOM	Field Mnemonic: Description
6:11	RW	MBA_PMU7Q_CFG_EVENT1_SELECT: Event1 select. 0x00 = MBA Command clocks 0x01 = ACT all 0x02 = ACT for read 0x03 = ACT for write 0x04 = CAS all 0x05 = CAS for read 0x06 = CAS for write 0x07 = CAS for low-priority write 0x08 = CAS for high-priority write 0x09 = PRE all 0x0a PRE for read 0x0b = PRE for write 0x0c = REF high priority 0x0d = REF low priority 0x0e = REF all 0x0f = RRQ empty 0x10 = RRQ full 0x11 = WRQ empty 0x12 = WRQ full 0x13 = WRQ above hw mark 0x14 = Reserved 0x15 = activate with direction switch (change from rd→wr or wr→rd) 0x16 = activate with mrank switch (Master rank different than previous ACT) 0x17 = activate with srank switch (Same master; slave rank different than previous ACT) 0x18 = activate with bank group switch (Same master, slave; bank group different than previous ACT) 0x19 = activate with bank switch (Same master, slave, bank group; different bank than previous ACT) 0x1a = all bank timers full 0x1b = any CKE PUP transition (0→1) 0x1c = CKE0 cycles PUP 0x1d = CKE1 cycles PUP 0x1e = CKE2 cycles PUP 0x1f = CKE3 cycles PUP 0x20 = WDF stalled waiting on read buffer 0x21 = WDF stalled waiting on read ramp 0x22 = Command1 Compare 0x23 - 0x3f = Reserved

Bits	SCOM	Field Mnemonic: Description
12:17	RW	MBA_PMU7Q_CFG_EVENT2_SELECT: Event2 select. 0x00 = MBA Command clocks 0x01 = ACT all 0x02 = ACT for read 0x03 = ACT for write 0x04 = CAS all 0x05 = CAS for read 0x06 = CAS for write 0x07 = CAS for low-priority write 0x08 = CAS for high-priority write 0x09 = PRE all 0x0a = PRE for read 0x0b = PRE for write 0x0c = REF high priority 0x0d = REF low-priority 0x0e = REF all 0x0f = RRQ empty 0x10 = RRQ full 0x11 = WRQ empty 0x12 = WRQ full 0x13 = WRQ above hw mark 0x14 = Reserved 0x15 = activate with direction switch (change from rd→wr or wr→rd) 0x16 = activate with mrank switch (Master rank different than previous ACT) 0x17 = activate with srank switch (Same master; slave rank different than previous ACT) 0x18 = activate with bank group switch (Same master, slave; bank group different than previous ACT) 0x19 = activate with bank switch (Same master, slave, bank group; different bank than previous ACT) 0x1a = all bank timers full 0x1b any CKE PUP transition (0→1) 0x1c = CKE0 cycles PUP 0x1d = CKE1 cycles PUP 0x1e = CKE2 cycles PUP 0x1f = CKE3 cycles PUP 0x20 = WDF stalled waiting on read buffer 0x21 = WDF stalled waiting on read ramp 0x22 = Command2 Compare 0x23 - 0x3f = Reserved

Bits	SCOM	Field Mnemonic: Description
18:23	RW	MBA_PMU7Q_CFG_EVENT3_SELECT: Event3 select. 0x00 = MBA Command clocks 0x01 = ACT all 0x02 = ACT for read 0x03 = ACT for write 0x04 = CAS all 0x05 = CAS for read 0x06 = CAS for write 0x07 = CAS for low-priority write 0x08 = CAS for high-priority write 0x09 = PRE all 0x0a = PRE for read 0x0b = PRE for write 0x0c = REF high priority 0x0d = REF low priority 0x0e = REF all 0x0f = RRQ empty 0x10 = RRQ full 0x11 = WRQ empty 0x12 = WRQ full 0x13 = WRQ above hw mark 0x14 = Reserved 0x15 = activate with direction switch (change from rd→wr or wr→rd) 0x16 = activate with mrank switch (Master rank different than previous ACT) 0x17 = activate with srank switch (Same master; slave rank different than previous ACT) 0x18 = activate with bank group switch (Same master, slave; bank group different than previous ACT) 0x19 = activate with bank switch (Same master, slave, bank group; different bank than previous ACT) 0x1a = all bank timers full 0x1b = any CKE PUP transition (0→1) 0x1c = CKE0 cycles PUP 0x1d = CKE1 cycles PUP 0x1e = CKE2 cycles PUP 0x1f = CKE3 cycles PUP 0x20 = WDF stalled waiting on read buffer 0x21 = WDF stalled waiting on read ramp 0x22 - 0x3f = Reserved
24:25	RW	MBA_PMU7Q_CFG_PRESCALER_C0: Prescaler for Event Counter 0. 00 = 20-bit 01 =16-bit 10 = 8-bit 11 = 4-bit
26:27	RW	MBA_PMU7Q_CFG_PRESCALER_C1: Prescaler for Event Counter 1. 00 = 20-bit 01 = 16-bit 10 = 8-bit 11 = 4-bit
28:29	RW	MBA_PMU7Q_CFG_PRESCALER_C2: Prescaler for Event Counter 2. 00 = 20-bit 01 =16-bit 10 = 8-bit 11 = 4-bit
30:31	RW	MBA_PMU7Q_CFG_PRESCALER_C3: Prescaler for Event Counter 3. 00 = 20-bit 01 = 16-bit 10 = 8-bit 11 = 4-bit

Bits	SCOM	Field Mnemonic: Description
32:34	RW	MBA_PMU7Q_CASCADE: Allows cascading of counts to make a 32-bit counter. x00 = no cascading 001 = c0 → c1 010 = c1 → c2 011 = c2 → c3 101 = c1 → c0 110 = c2 → c1 111 = c3 → c2
35	RW	MBA_PMU7Q_FREEZE: If enabled, freeze all counters when any counter reaches maximum.

Register Name	Performance Monitor Command Compare Register
Mnemonic	MC01.PORT1.SRQ.MBA_PMU8Q
Address	000000000701097F (SCOM)
Description	Performance monitor command compare register

Bits	SCOM	Field Mnemonic: Description
0:1	RW	MBA_PMU8Q_CFG_CMD0_TYPE: Command 0 compare type qualifier. 00 = read 01 = write 10 = activate 11 = read or write
2	RW	MBA_PMU8Q_CFG_CMD0_MRANK_MATCH_EN:
3	RW	MBA_PMU8Q_CFG_CMD0_SRANK_MATCH_EN:
4	RW	MBA_PMU8Q_CFG_CMD0_BG_MATCH_EN:
5	RW	MBA_PMU8Q_CFG_CMD0_BANK_MATCH_EN:
6:8	RW	MBA_PMU8Q_CFG_CMD0_MRANK:
9:11	RW	MBA_PMU8Q_CFG_CMD0_SRANK:
12:13	RW	MBA_PMU8Q_CFG_CMD0_BG:
14:16	RW	MBA_PMU8Q_CFG_CMD0_BANK:
17:18	RW	MBA_PMU8Q_CFG_CMD1_TYPE: Command 1 compare type qualifier. 00 = read 01 = write 10 = activate 11 = read or write
19	RW	MBA_PMU8Q_CFG_CMD1_MRANK_MATCH_EN:
20	RW	MBA_PMU8Q_CFG_CMD1_SRANK_MATCH_EN:
21	RW	MBA_PMU8Q_CFG_CMD1_BG_MATCH_EN:
22	RW	MBA_PMU8Q_CFG_CMD1_BANK_MATCH_EN:
23:25	RW	MBA_PMU8Q_CFG_CMD1_MRANK:
26:28	RW	MBA_PMU8Q_CFG_CMD1_SRANK:
29:30	RW	MBA_PMU8Q_CFG_CMD1_BG:
31:33	RW	MBA_PMU8Q_CFG_CMD1_BANK:

Bits	SCOM	Field Mnemonic: Description
34:35	RW	MBA_PMU8Q_CFG_CMD2_TYPE: Command 2 compare type qualifier. 00 = read 01 = write 10 = activate 11 = read or write
36	RW	MBA_PMU8Q_CFG_CMD2_MRANK_MATCH_EN:
37	RW	MBA_PMU8Q_CFG_CMD2_SRANK_MATCH_EN:
38	RW	MBA_PMU8Q_CFG_CMD2_BG_MATCH_EN:
39	RW	MBA_PMU8Q_CFG_CMD2_BANK_MATCH_EN:
40:42	RW	MBA_PMU8Q_CFG_CMD2_MRANK:
43:45	RW	MBA_PMU8Q_CFG_CMD2_SRANK:
46:47	RW	MBA_PMU8Q_CFG_CMD2_BG:
48:50	RW	MBA_PMU8Q_CFG_CMD2_BANK:
51:63	RW	MBA_PMU8Q_RESERVED_51_63:

Register Name	**MBA CAL FIR Register**
Mnemonic	MC01.PORT2.SRQ.MBACALFIRQ
Address	0000000007010980 (SCOM) 0000000007010981 (SCOM1) 0000000007010982 (SCOM2)
Description	MBA CAL FIR Register (MBACALFIR)

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	MBACALFIRQ_MBA_RECOVERABLE_ERROR: When set, an MBA recoverable error has occurred. These include cal[0:3]_cfg, RRQ, WRQ, and power control parity errors.
1	RWX	WOX_AND	WOX_OR	MBACALFIRQ_MBA_NONRECOVERABLE_ERROR: When set, an MBA nonrecoverable error has occurred. These include DSM, TMR, FARB, and SIR parity errors.
2	RWX	WOX_AND	WOX_OR	MBACALFIRQ_REFRESH_OVERRUN: When set, nine (9) refreshes have been enqueued to any single rank.
3	RWX	WOX_AND	WOX_OR	MBACALFIRQ_WAT_ERROR: When set, an error has been detected in the MBA debug WAT logic.
4	RWX	WOX_AND	WOX_OR	MBACALFIRQ_RCD_PARITY_ERROR: When set, an RCD parity error has been detected on DDR port 0. If the error was seen during a calibration, FIR 14 will fire instead.
5	RWX	WOX_AND	WOX_OR	MBACALFIRQ_DDR_CAL_TIMEOUT_ERR: When set, a calibration complete indication was not received in the calibration timeout time for DDR0.
6	RWX	WOX_AND	WOX_OR	MBACALFIRQ_EMERGENCY_THROTTLE: Emergency throttle engaged either due to an OCC request or a deadman timer pop.
7	RWX	WOX_AND	WOX_OR	MBACALFIRQ_DDR_CAL_RESET_TIMEOUT: When set, indicates that a soft reset issued to the DDR PHY did not clear a pending calibration update request.
8	RWX	WOX_AND	WOX_OR	MBACALFIRQ_DDR_MBA_EVENT_N: When set, indicates event_n was active on the DDR interface.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
9	RWX	WOX_AND	WOX_OR	MBACALFIRQ_WRQ_RRQ_HANG_ERR: When set, indicates that the WRQ or RRQ is in a hung state.
10	RWX	WOX_AND	WOX_OR	MBACALFIRQ_SM_1HOT_ERR: When set, indicates a state machine one hot error.
11	RWX	WOX_AND	WOX_OR	MBACALFIRQ_ASYNC_IF_ERROR: Sequencer error seen when crossing the asynchronous interface from the MCS.
12	RWX	WOX_AND	WOX_OR	MBACALFIRQ_CMD_PARITY_ERROR: Address parity error seen internal to the sequencer on a read or write command.
13	RWX	WOX_AND	WOX_OR	MBACALFIRQ_PORT_FAIL: The port has failed due to a persistent retry. All reads returned with an RCD error so that SUE will be delivered upstream.
14	RWX	WOX_AND	WOX_OR	MBACALFIRQ_RCD_CAL_PARITY_ERROR: When set, an RCD parity error has been detected during a calibration.
15	RWX	WOX_AND	WOX_OR	MBACALFIRQ_INTERNAL_SCOM_ERROR: When set, an internal SCOM error has occurred.
16	RWX	WOX_AND	WOX_OR	MBACALFIRQ_INTERNAL_SCOM_ERROR_COPY: Copy of internal SCOM error.
17:63	RO	RO	RO	Constant = 0b00000000000000000000000000000000000000000000000000000

Register Name	MBA CAL FIR Mask Register
Mnemonic	MC01.PORT2.SRQ.MBACALFIR_MASK
Address	0000000007010983 (SCOM) 0000000007010984 (SCOM1) 0000000007010985 (SCOM2)
Description	MBA CAL FIR Mask Register (MBACALFIR_MASK)

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	MBACALFIR_MASK_MBA_RECOVERABLE_ERROR: When set, an MBA recoverable error has occurred. These include cal[0:3]_cfg, RRQ, WRQ and power control parity errors.
1	RW	WO_AND	WO_OR	MBACALFIR_MASK_MBA_NONRECOVERABLE_ERROR: When set, an MBA nonrecoverable error has occurred. These include DSM, TMR, FARB, and SIR parity errors.
2	RW	WO_AND	WO_OR	MBACALFIR_MASK_REFRESH_OVERRUN: When set, nine (9) refreshes have been enqueued to any single rank.
3	RW	WO_AND	WO_OR	MBACALFIR_MASK_WAT_ERROR: When set, an error has been detected in the MBA debug WAT logic.
4	RW	WO_AND	WO_OR	MBACALFIR_MASK_RCD_PARITY_ERROR: When set, an RCD parity error has been detected on DDR port 0.
5	RW	WO_AND	WO_OR	MBACALFIR_MASK_DDR_CAL_TIMEOUT_ERR: When set, a calibration complete indication was not received in the calibration timeout time for DDR0.
6	RW	WO_AND	WO_OR	MBACALFIR_MASK_EMERGENCY_THROTTLE: Emergency throttle engaged either due to an OCC request or a deadman timer pop.
7	RW	WO_AND	WO_OR	MBACALFIR_MASK_DDR_CAL_RESET_TIMEOUT: When set, indicates that a soft reset issued to the DDR PHY did not clear a pending calibration update request.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
8	RW	WO_AND	WO_OR	MBACALFIR_MASK_DDR_MBA_EVENT_N: When set, indicates event_n was active on the DDR interface.
9	RW	WO_AND	WO_OR	MBACALFIR_MASK_WRQ_RRQ_HANG_ERR: When set, indicates that the WRQ or RRQ is in a hung state.
10	RW	WO_AND	WO_OR	MBACALFIR_MASK_SM_1HOT_ERR: When set, indicates a state machine one hot error.
11	RW	WO_AND	WO_OR	MBACALFIR_MASK_ASYNC_IF_ERROR: Sequencer error seen when crossing an asynchronous interface from the MCS.
12	RW	WO_AND	WO_OR	MBACALFIR_MASK_CMD_PARITY_ERROR: Address parity error seen internal to sequencer on a read or write command
13	RW	WO_AND	WO_OR	MBACALFIRQ_MASK_PORT_FAIL: The port has failed due to a persistent retry. All reads returned with an RCD error so that SUE will be delivered upstream.
14	RW	WO_AND	WO_OR	MBACALFIRQ_MASK_RCD_CAL_PARITY_ERROR: When set, an RCD parity error has been detected during a calibration.
15	RW	WO_AND	WO_OR	MBACALFIR_MASK_INTERNAL_SCOM_ERROR: When set, an internal SCOM error has occurred.
16	RW	WO_AND	WO_OR	MBACALFIR_MASK_INTERNAL_SCOM_ERROR_COPY: Copy of internal SCOM error.
17:63	RO	RO	RO	Constant = 0b00000000000000000000000000000000000000000000000000000

Register Name	**MBA CAL FIR Action 0 Register**
Mnemonic	MC01.PORT2.SRQ.MBACALFIR_ACTION0
Address	0000000007010986 (SCOM)
Description	MBA CAL FIR Action 0 Register (MBACALFIR_ACTION0)

Bits	SCOM	Field Mnemonic: Description
0:16	RW	MBACALFIR_ACTION0_FIR_ACTION0: MBA action0 select for the corresponding bit in the FIR. (Action0, Action1, Mask) = Action Select: (0,0,X) = No error reported (0,1,0) = Recoverable error (1,0,0) = Checkstop error (1,1,0) = Local core checkstop freeze (X,X,1) = Masked
17:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000

Register Name	**MBA CAL FIR Action 1 Register**
Mnemonic	MC01.PORT2.SRQ.MBACALFIR_ACTION1
Address	0000000007010987 (SCOM)
Description	MBA CAL FIR Action 1 Register (MBACALFIR_ACTION1)

Bits	SCOM	Field Mnemonic: Description
0:16	RW	MBACALFIR_ACTION1_FIR_ACTION1: MBA action1 select for the corresponding bit in the FIR. (Action0, Action1, Mask) = Action Select: (0,0,X) = No error reported (0,1,0) = Recoverable error (1,0,0) = Checkstop error (1,1,0) = Local core checkstop freeze (X,X,1) = Masked
17:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000

Register Name	Data State Machine Configurations Register
Mnemonic	MC01.PORT2.SRQ.MBA_DSM0Q
Address	000000000701098A (SCOM)
Description	Data State Machine Configurations

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MBA_DSM0Q_CFG_RODT_START_DLY: Delay from read command to ODT turn on.
6:11	RW	MBA_DSM0Q_CFG_RODT_END_DLY: Delay from read command to ODT turn off.
12:17	RW	MBA_DSM0Q_CFG_WODT_START_DLY: Delay from write command to ODT turn on.
18:23	RW	MBA_DSM0Q_CFG_WODT_END_DLY: Delay from write command to ODT turn off.
24:29	RW	MBA_DSM0Q_CFG_WRDONE_DLY: Delay from write command to write done to MBS.
30:35	RW	MBA_DSM0Q_CFG_WRDATA_DLY: Delay from write command to stating the write data flow.
36:41	RW	MBA_DSM0Q_CFG_RDTAG_DLY: Delay from read command to rd data valid back to MBS.
42	RW	MBA_DSM0Q_CFG_RDTAG_MBX_CYCLE: Determines the memory clock 1/2 cycle that the rdtag entry is released from the DSM queue. 0 = release when MBX clock is low 1 = release when MBX clock is high
43:48	RW	MBA_DSM0Q_CFG_RODT_BC4_END_DLY: Delay from read command to ODT turn off for BC4 command.
49:54	RW	MBA_DSM0Q_CFG_WODT_BC4_END_DLY: Delay from write command to ODT turn off for BC4 command.
55:63	RW	MBA_DSM0Q_RESERVED_55_63: Reserved.

Register Name	DDR Data Bus Timing Parameters Register
Mnemonic	MC01.PORT2.SRQ.MBA_TMR0Q
Address	000000000701098B (SCOM)
Description	DDR data bus timing parameters

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MBA_TMR0Q_RRDM_DLY: Read to read to different master.
4:7	RW	MBA_TMR0Q_RRSMSR_DLY: Read to read same master, same rank.
8:11	RW	MBA_TMR0Q_RRSMDR_DLY: Read to read same master. different rank,
12:15	RW	MBA_TMR0Q_RROP_DLY: Read open page to read delay.
16:19	RW	MBA_TMR0Q_WWDM_DLY: Write to write; different master.
20:23	RW	MBA_TMR0Q_WWSMSR_DLY: Write to write; same master, same rank.

Bits	SCOM	Field Mnemonic: Description
24:27	RW	MBA_TMR0Q_WWSMDR_DLY: Write to write; same master, different rank.
28:31	RW	MBA_TMR0Q_WWOP_DLY: Write open page to write delay.
32:36	RW	MBA_TMR0Q_RWDM_DLY: Read to write; different master.
37:41	RW	MBA_TMR0Q_RWSMSR_DLY: Read to write; same master. same rank,
42:46	RW	MBA_TMR0Q_RWSMDR_DLY: Read to write; same master. different rank,
47:50	RW	MBA_TMR0Q_WRDM_DLY: Write to read; different master.
51:56	RW	MBA_TMR0Q_WRSMSR_DLY: Write to read; same master, same rank.
57:62	RW	MBA_TMR0Q_WRSMDR_DLY: Write to read; same master, different rank.
63	RW	MBA_TMR0Q_RESERVED_63: Reserved.

Register Name	DDR Bank Busy Parameters Register
Mnemonic	MC01.PORT2.SRQ.MBA_TMR1Q
Address	000000000701098C (SCOM)
Description	DDR bank busy parameters

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MBA_TMR1Q_RRSBG_DLY: Read to read; same bank group.
4:9	RW	MBA_TMR1Q_WRSBG_DLY: Write to read; same bank group.
10:15	RW	MBA_TMR1Q_CFG_TFAW: Four activate window time.
16:20	RW	MBA_TMR1Q_CFG_TRCD: RAS to CAS delay.
21:25	RW	MBA_TMR1Q_CFG_TRP: Precharge to activate delay.
26:31	RW	MBA_TMR1Q_CFG_TRAS: Activate to precharge delay.
32:40	RW	MBA_TMR1Q_RESERVED_32_40: Reserved.
41:47	RW	MBA_TMR1Q_CFG_WR2PRE: Write to precharge delay.
48:51	RW	MBA_TMR1Q_CFG_RD2PRE: Read to precharge delay.
52:55	RW	MBA_TMR1Q_TRRD: Activate to activate delay.
56:59	RW	MBA_TMR1Q_TRRD_SBG: Activate to activate, same bank group, delay.
60:63	RW	MBA_TMR1Q_CFG_ACT_TO_DIFF_RANK_DLY: Activate to activate, different rank, delay.

Register Name	DDR Write Command Parameters Register
Mnemonic	MC01.PORT2.SRQ.MBA_WRQ0Q
Address	000000000701098D (SCOM)
Description	DDR write command parameters

Bits	SCOM	Field Mnemonic: Description
0:4	RW	MBA_WRQ0Q_CFG_WRITE_HW_MARK: Write high-water mark (force writes HPenables writes).
5	RW	MBA_WRQ0Q_CFG_WRQ_FIFO_MODE: Prevent reordering in the WRQ (only entry0 can be selected). HP cleaner writes will not get selected until they are in entry 0.
6	RW	MBA_WRQ0Q_CFG_DISABLE_WR_PG_MODE: Disable page commands for WRQ.

Bits	SCOM	Field Mnemonic: Description
7:18	RW	MBA_WRQ0Q_CFG_WRQ_ENTRY0_HP_DLY: Time for entry0 of the WRQ before it forces HP setting this dial to a 0; will disable entry0 HP.
19	RW	MBA_WRQ0Q_CFG_WRQ_FLUSH_WR_RANK: When one write is issued to a rank, try to force more writes to that rank to avoid multiple write to read same rank penalties.
20	RW	MBA_WRQ0Q_CFG_WRQ_ENABLE_NON_HP_WR: Allow writes when they do not meet a condition such as entry0_flush or rd_idle_allow_wr.
21:32	RW	MBA_WRQ0Q_CFG_ENTRY0_MIN_FOR_RRQ_IDLE_WR: This is an added condition to allow writes when the RRQ is idle. This addition allows for multiple writes to stack up in the WRQ before starting the write burst.
33:37	RW	MBA_WRQ0Q_CFG_WRITE_LW_MARK: Write low-water mark. After write high priority has been asserted due to the writes exceeding the programmed high-water mark, write priority will remain asserted until the write low-water mark is reached. If set to 8 and there are more than eight entries in the WRQ, then the condition will allow writes when the rrq_idle period is met.
38:43	RW	MBA_WRQ0Q_CFG_WRQ_SKIP_LIMIT: The number of times entry0 of the WRQ can be skipped before entry0 prevents older writes from being issued until entry0 is sent.
44	RW	MBA_WRQ0Q_CFG_WRQ_SINGLE_THREAD_MODE: WRQ wrq_single thread mode setting. This ensures all reads are issued one at a time. With this mode set, we only issue from the bottom entry in the WRQ, and do not issue an activate for the subsequent operation until the prior write is sent.
45:52	RW	MBA_WRQ0Q_CFG_RQ_HANG_THRESHOLD: Hang detection for entry0 of the reorder queue. A counter increments every mcbist_srq_hang_pulse(2048 phase hold cycles), and will set a FIR when the count = threshold and another pulse is received. Since this checks for count = threshold, a value of 0 is not valid.
53:54	RW	MBA_WRQ0Q_RESERVED_53_54: Reserved.
55:58	RW	MBA_WRQ0Q_CFG_WRQ_ACT_NUM_WRITES_PENDING: Limit on number of write activates when doing writes. When the sequencer is serving writes, no new activates will be sent out as long as at least this number of writes are pending to already-activated pages. A setting of 0 sets no cap on the number of activates.
59:63	RW	MBA_WRQ0Q_RESERVED_59_63: Reserved.

Register Name	DDR Read Command Parameters Register
Mnemonic	MC01.PORT2.SRQ.MBA_RRQ0Q
Address	000000000701098E (SCOM)
Description	DDR read command parameters

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MBA_RRQ0Q_CFG_RRQ_SKIP_LIMIT: Number of times the bottom entry in the RRQ can be skipped before preventing the entry from being skipped.
6	RW	MBA_RRQ0Q_CFG_RRQ_FIFO_MODE: RRQ FIFO mode. Setting this ensures that all reads go out in the order they were received. It still allows multiple operations to be pipelined to allow for decent throughput. This needs to be set for MCBIST dgen mode.
7	RW	MBA_RRQ0Q_CFG_RRQ_SINGLE_THREAD_MODE: RRQ single thread mode. Setting this ensures all reads are issued one at a time. With this mode set, we only issue from the bottom entry in the RRQ, and we do not issue an activate for the subsequent operation until the prior read is sent.
8:10	RW	MBA_RRQ0Q_RESERVED_8_10: Reserved.
11	RW	MBA_RRQ0Q_CFG_DISABLE_RD_PG_MODE: Disable page commands for RRQ.
12	RW	MBA_RRQ0Q_CFG_DISABLE_FAST_PATH: Disable MBA RRQ fastpath.
13:23	RW	MBA_RRQ0Q_CFG_RD_IDLE_ALLOW_WR: Time with an empty RRQ before writes will be enabled.
24:29	RW	MBA_RRQ0Q_CFG_RDBUFF_CAPACITY_LIMIT: Number of 64-byte read buffers that the sequencer is allowed to use concurrently.

Bits	SCOM	Field Mnemonic: Description
30:36	RW	MBA_RRQ0Q_CFG_RMWBUFF_CAPACITY_LIMIT: Number of 64-byte read-modify-write buffers that the sequencer is allowed to use concurrently.
37:56	RW	MBA_RRQ0Q_RESERVED_37_56: Reserved.
57:60	RW	MBA_RRQ0Q_CFG_RRQ_ACT_NUM_READS_PENDING: Limit on number of read-activates when doing reads. When the sequencer is serving reads, no new activates will be sent out as long as at least this number of reads are pending to already activated pages. A setting of 0 sets no cap on the number of activates.
61	RW	MBA_RRQ0Q_CFG_INJ_CANCEL_ACK_ERR: Inject error on cancel-ack asynchronous interface.
62	RW	MBA_RRQ0Q_CFG_RRQ_ENTRY0_ENABLE: Enable entry0 timer for RRQ.
63	RW	MBA_RRQ0Q_RESERVED_63: Reserved.

Register Name	DDR Calibration Register
Mnemonic	MC01.PORT2.SRQ.MBA_CAL0Q
Address	000000000701098F (SCOM)
Description	DDR Calibration Registers

Bits	SCOM	Field Mnemonic: Description
0	RW	MBA_CAL0Q_CFG_CAL_INTERVAL_TMR0_ENABLE: Enable interval tmr0.
1:2	RW	MBA_CAL0Q_CFG_TIME_BASE_TMR0: Time base for the interval tmr0 counter.
3:11	RW	MBA_CAL0Q_CFG_INTERVAL_COUNTER_TMR0: Interval timer based on time_base (time_base × interval_counter).
12	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL1_ENABLE: Enable bit for the first calibration to perform when the timer pops. It should always be 1 if the timer is enabled.
13:16	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL1_TYPE: 10XX Internal ZQ calibration (cal_rank ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step. 0011 = Periodic calibration: Run SysClk, DQS, and read eye all in parallel (default behavior).
17	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL1_DDR_DONE: Use the complete signal from the DDR for cal1.
18	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL2_ENABLE: Enable bit for the second calibration to perform when the timer pops.
19:22	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL2_TYPE: 10XX = Internal ZQ calibration (cal_rank ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step. 0011 = Periodic calibration: Run SysClk, DQS, and read eye all in parallel (default behavior).
23	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL2_DDR_DONE: Use the complete signal from the DDR for cal2.
24	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL3_ENABLE: Enable bit for the third calibration to perform when the timer pops.

Bits	SCOM	Field Mnemonic: Description
25:28	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL3_TYPE: 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step. 0011 = Periodic calibration: Run SysClk, DQS, and read eye all in parallel (default behavior).
29	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL3_DDR_DONE: Use the complete signal from the DDR for cal3.
30:38	RW	MBA_CAL0Q_CFG_CAL_TMR0_Z_SYNC: The timer value will be set to this value during z sync.
39:46	RW	MBA_CAL0Q_CFG_CAL_TMR0_DDR_RESET_TMR: Wait time for a DDR soft reset upon a calibration timeout fail.
47:48	RW	MBA_CAL0Q_CFG_CAL_TMR0_DDR_RESET_TMR_TB: Timebase interval for ddr_reset_tmr.
49	RW	MBA_CAL0Q_CFG_CAL_TMR0_DDR_RESET_ENABLE: Enable DDR soft reset upon calibration timeout fail. 0 = Do not issue a soft DDR reset upon calibration timeout. 1 = Issue a DDR soft reset upon calibration timeout.
50	RW	MBA_CAL0Q_CFG_CAL_TMR0_SINGLE_RANK: Enable single-rank mode for timer0 calibrations. Calibrations programmed in tmr0 will run on one rank at a time per timer expiration. 0 = Issue calibrations for all enabled ranks per timer expiration. 1 = Issue calibrations for one rank at a time per timer expiration.
51	RW	MBA_CAL0Q_RESERVED_51: Reserved.
52	RW	MBA_CAL0Q_INJECT_1HOT_SM_ERROR: Setting to 1 will inject one 1hot sm error. It must be set to 0 and then 1 again to inject another error. 0 = No error inject. 1 = Inject one 1hot sm error.
53:55	RW	MBA_CAL0Q_CFG_CAL_SINGLE_PORT_MODE: Single port mode configuration. The default is both ports are calibrated at the same time. Options are: • Single port calibrated at a time with both ports powered up. • Single port calibrated at a time with one port powered up. • Single port calibrated at a time with one port powered up and only the rank requested by the DDR PHY powered up. Only to be used in single rank mode.
56	RW	MBA_CAL0Q_DBG_BUS_BIT: Debug bus bit.
57	RW	MBA_CAL0Q_RESET_RECOVER: DDR reset recover.
58	RW	MBA_CAL0Q_CFG_RANK_SM_STALL_DISABLE: When enabled, require a minimum 1K cycle stall between all new calibration timer starts.
59	RW	MBA_CAL0Q_CFG_ENABLE_SPEC_ATTN: Allow FIR attention to cause spec attn.
60	RW	MBA_CAL0Q_CFG_ENABLE_HOST_ATTN: Allow FIR attention to cause host attn.
61:63	RW	MBA_CAL0Q_RESERVED_61_63: Reserved.

Register Name	DDR Calibration Register
Mnemonic	MC01.PORT2.SRQ.MBA_CAL1Q
Address	0000000007010990 (SCOM)
Description	DDR Calibration Registers

Bits	SCOM	Field Mnemonic: Description
0	RW	MBA_CAL1Q_CFG_CAL_INTERVAL_TMR1_ENABLE: Enable interval tmr1.
1:2	RW	MBA_CAL1Q_CFG_TIME_BASE_TMR1: Time base for the interval tmr1 counter

Bits	SCOM	Field Mnemonic: Description
3:11	RW	MBA_CAL1Q_CFG_INTERVAL_COUNTER_TMR1: Interval timer based on time_base (time_base × interval_counter).
12	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL1_ENABLE: Enable bit for the first calibration to perform when the timer pops. It should always be 1 if the timer is enabled.
13:16	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL1_TYPE: 10XX = Internal ZQ calibration (cal_rank ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step. 0011 = Periodic calibration: Run SysClk, DQS, and read eye all in parallel (default behavior).
17	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL1_DDR_DONE: Use the complete signal from the DDR for cal1.
18	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL2_ENABLE: Enable bit for the second calibration to perform when the timer pops.
19:22	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL2_TYPE: 10XX = Internal ZQ calibration (cal_rank ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step. 0011 = Periodic calibration: Run SysClk, DQS, and read eye all in parallel (default behavior).
23	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL2_DDR_DONE: Use the complete signal from the DDR for cal2.
24	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL3_ENABLE: Enable bit for the third calibration to perform when the timer pops.
25:28	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL3_TYPE: 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step. 0011 = Periodic calibration: Run SysClk, DQS, and read eye all in parallel (default behavior).
29	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL3_DDR_DONE: Use the complete signal from the DDR for cal3,
30:38	RW	MBA_CAL1Q_CFG_CAL_TMR1_Z_SYNC: The timer value will be set to this value during z sync.
39	RW	MBA_CAL1Q_CFG_CAL_TMR1_SINGLE_RANK: Enable single-rank mode for timer1 calibrations. Calibrations programmed in tmr1 will run on one rank at a time per timer expiration. 0 = Issue calibrations for all enabled ranks per timer expiration. 1 = Issue calibrations for one rank at a time per timer expiration.
40:47	RW	MBA_CAL1Q_CFG_CAL_RANK_ENABLE: Cal rank enable.
48:63	RW	MBA_CAL1Q_RESERVED_48_63: Reserved.

Register Name	DDR Calibration Register
Mnemonic	MC01.PORT2.SRQ.MBA_CAL2Q
Address	0000000007010991 (SCOM)
Description	DDR Calibration registers

Bits	SCOM	Field Mnemonic: Description
0	RW	MBA_CAL2Q_CFG_CAL_INTERVAL_TMR2_ENABLE: Enable interval tmr2.
1:2	RW	MBA_CAL2Q_CFG_TIME_BASE_TMR2: Time base for the interval tmr2 counter.

Bits	SCOM	Field Mnemonic: Description
3:11	RW	MBA_CAL2Q_CFG_INTERVAL_COUNTER_TMR2: Interval timer based on time_base (time_base × interval_counter).
12	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL1_ENABLE: Enable bit for the first calibration to perform when the timer pops. It should always be 1 if the timer is enabled.
13:16	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL1_TYPE: 10XX = Internal ZQ calibration (cal_rank ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step. 0011 = Periodic calibration: Run SysClk, DQS, and read eye all in parallel (default behavior).
17	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL1_DDR_DONE: Use the complete signal from the DDR for cal1.
18	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL2_ENABLE: Enable bit for the second calibration to perform when the timer pops.
19:22	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL2_TYPE: 10XX = Internal ZQ calibration (cal_rank ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step. 0011 = Periodic calibration: Run SysClk, DQS, and read eye all in parallel (default behavior).
23	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL2_DDR_DONE: Use the complete signal from the DDR for cal2.
24	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL3_ENABLE: Enable bit for the third calibration to perform when the timer pops.
25:28	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL3_TYPE: 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step. 0011 = Periodic calibration: Run SysClk, DQS, and read eye all in parallel (default behavior).
29	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL3_DDR_DONE: Use the complete signal from the DDR for cal3.
30:38	RW	MBA_CAL2Q_CFG_CAL_TMR2_Z_SYNC: The timer value will be set to this value during z sync.
39	RW	MBA_CAL2Q_CFG_CAL_TMR2_SINGLE_RANK: Enable single-rank mode for timer2 calibrations. Calibrations programmed in tmr2 will run on one rank at a time per timer expiration. 0 = Issue calibrations for all enabled ranks per timer expiration. 1 = Issue calibrations for one rank at a time per timer expiration.
40	RW	MBA_CAL2Q_CFG_CAL_TMR2_WAT_EVENT_ENABLE: Enable the use of tmr2 to trigger a WAT event. No other calibrations should be enabled. Must be used with the HW221617 CKSW enabled.
41:63	RW	MBA_CAL2Q_RESERVED_41_63: Reserved.

Register Name	DDR Calibration Length Register
Mnemonic	MC01.PORT2.SRQ.MBA_CAL3Q
Address	0000000007010992 (SCOM)
Description	DDR Calibration Length Registers

Bits	SCOM	Field Mnemonic: Description
0:1	RW	MBA_CAL3Q_CFG_INTERNAL_ZQ_TB: Internal ZQ time base. Time base for the internal ZQ cal counter.

Bits	SCOM	Field Mnemonic: Description
2:9	RW	MBA_CAL3Q_CFG_INTERNAL_ZQ_LENGTH: Number of internal ZQ time bases required to meet the maximum internal ZQ length.
10:11	RW	MBA_CAL3Q_CFG_EXTERNAL_ZQ_TB: External ZQ time base. Time base for the external ZQ cal counter.
12:19	RW	MBA_CAL3Q_CFG_EXTERNAL_ZQ_LENGTH: Number of external ZQ time bases required to meet the maximum external ZQ length.
20:21	RW	MBA_CAL3Q_CFG_RDCLK_SYSCLK_TB: ReadclkSysclk time base. Time base for the readclksysclk cal counter.
22:29	RW	MBA_CAL3Q_CFG_RDCLK_SYSCLK_LENGTH: Number of Readclksysclk time bases required to meet the maximum rdclk length.
30:31	RW	MBA_CAL3Q_CFG_DQS_ALIGNMENT_TB: DQS alignment time base. Time base for the DQS alignment cal counter.
32:39	RW	MBA_CAL3Q_CFG_DQS_ALIGNMENT_LENGTH: Number of DQS alignment time bases required to meet the maximum DQS alignment length.
40:41	RW	MBA_CAL3Q_CFG_MPR_READEYE_TB: Readeye time base. Time base for the readeye cal counter.
42:49	RW	MBA_CAL3Q_CFG_MPR_READEYE_LENGTH: Number of readeye time bases required to meet the maximum external ZQ length.
50:51	RW	MBA_CAL3Q_CFG_ALL_PERIODIC_TB: All Periodics time base. Time base for all periodic cal counter.
52:59	RW	MBA_CAL3Q_CFG_ALL_PERIODIC_LENGTH: Number of all_periodic time bases required to meet maximum the calibration length for all periodic calibration (in parallel).
60	RW	MBA_CAL3Q_CFG_FREEZE_ON_PARITY_ERROR_DIS: Disable freezing MBA execution when a parity error is detected.
61:63	RW	MBA_CAL3Q_RESERVED_61_63: Reserved.

Register Name	Final ARB Parameters Register
Mnemonic	MC01.PORT2.SRQ.MBA_FARB0Q
Address	0000000007010993 (SCOM)
Description	Final ARB parameters

Bits	SCOM	Field Mnemonic: Description
0:15	RW	MBA_FARB0Q_CFG_MISR_BLOCK: When a bit is set, an area of logic is not included in the z-sync MISR computation. Each bit independently gates (blocks) that area of logic from the MISR. bit 0 = gate refresh pulse bits 1 - 3 = gate cal timers 0 - 2 bit 4 = gate NM pulse bits 5 - 8 = gate MCBIST tb pulses bits 9 - 15 = gate FARB requests
16	RW	MBA_FARB0Q_CFG_MISR_FEEDBACK_ENABLE: Allow the z-sync MISR to use circular feedback and retain the state beyond its 10-latch pipe.
17	RW	MBA_FARB0Q_CFG_2N_ADDR: Enable 2N/2T address mode.
18:19	RW	MBA_FARB0Q_RESERVED_18_19: Reserved.
20:23	RW	MBA_FARB0Q_CFG_ACT_SAME_RANK_HOLD_TIME: Time after activate to prefer subsequent activates to the same rank.

Bits	SCOM	Field Mnemonic: Description
24:30	RW	MBA_FARB0Q_CFG_MAX_READS_IN_A_ROW: Limits the maximum number of reads in a row, before forcing a write. There must be a write in the WRQ for the counting to start. 0x00 = Disabled 0x01 = 1 read before allowing a write ... 0x7F = 127 reads before forcing a write
31:37	RW	MBA_FARB0Q_CFG_MAX_WRITES_IN_A_ROW: Limits the maximum number of writes in a row, before forcing a read. There must be a read in the RRQ for the counting to start. 0x00 = Disabled 0x01 = 1 write before allowing a read … 0x7F = 127 writes before forcing a read
38	RW	MBA_FARB0Q_CFG_PARITY_AFTER_CMD: Determines whether OE is driven on the parity cycle. 0 = OE will not be driven on the parity cycle. 1 = OE will be driven on the parity cycle.
39	RWX	MBA_FARB0Q_CFG_INJECT_PARITY_ERR_WEN: Inject a parity error on WEN on the next CAS.
40	RWX	MBA_FARB0Q_CFG_INJECT_PARITY_ERR_ADDR5: Inject a parity error on ADDR5 on the next CAS.
41:42	RWX	MBA_FARB0Q_CFG_BW_WINDOW_SIZE: For optional size reads: 00 = Determine BW over a 1K cycle window. 01 = Determine BW over a 2K cycle window. 10 = Determine BW over a 4K cycle window. 11 = Determine BW over an 8K cycle window.
43:47	RW	MBA_FARB0Q_CFG_PARITY_DETECT_TIME: Measures the time from an injected error until when the error is detected back at the MBA.
48:53	RW	MBA_FARB0Q_CFG_RCD_PROTECTION_TIME: Time interval in which commands were sent out before an RCD parity error occurrence that should be re-issued. Should be set ≥ to cfg_parity_detect_time.
54	RW	MBA_FARB0Q_CFG_DISABLE_RCD_RECOVERY: Disable the RCD recovery procedure.
55	RW	MBA_FARB0Q_CFG_OE_ALWAYS_ON: Force DDR OE to always be on(never tristate the DDR address drivers).
56	RW	MBA_FARB0Q_CFG_FARB_CLOSE_ALL_PAGES: Before switching direction on the DRAM bus, require all committed accesses to be issued to any open pages. When set, no new activates can be issued for reads until all writes to open pages are sent. No new activates can be issued for writes until all reads to open pages are issued.
57	RW	MBA_FARB0Q_CFG_PORT_FAIL_DISABLE: Disable Port Fail after recurring RCD errors.
58	RW	MBA_FARB0Q_CFG_OE_ALL_CKE_POWERED_DOWN: Only precisely turn off cmd-addr output enable after all CKEs are powered down.
59	RW	MBA_FARB0Q_CFG_INJECT_PARITY_ERR_CONSTANT: If set, parity errors are injected continuously; otherwise, parity errors are injected only once.
60	RW	MBA_FARB0Q_CFG_FINISH_WR_BEFORE_RD: This is to prevent writes from holding up banks for a long period of time. If set, all committed writes must be issued before reads can proceed.
61:63	RW	MBA_FARB0Q_CFG_OPT_RD_SIZE: For optional size reads: 000 = Treat all 64-byte/128-byte-opt reads as 64-byte reads. 001 = Treat all 64-byte/128-byte-opt reads as 128-byte reads. 010 = If DRAM data bus utilization is greater than 50%, do optional-size reads as 64 bytes. 011 = If DRAM data bus utilization is greater than 62.5%, do optional-size reads as 64 bytes. 100 = If DRAM data bus utilization is greater than 75.0%, do optional-size reads as 64 bytes. 101 = If DRAM data bus utilization is greater than 87.5%, do optional-size reads as 64 bytes. 11X = Reserved.

Register Name	Final ARB Parameters Register
Mnemonic	MC01.PORT2.SRQ.MBA_FARB1Q
Address	0000000007010994 (SCOM)
Description	Final ARB parameters

Bits	SCOM	Field Mnemonic: Description
0:2	RW	MBA_FARB1Q_CFG_SLOT0_S0_CID: Chip ID bits for Slot 0 Master 0/1 Slave 0.
3:5	RW	MBA_FARB1Q_CFG_SLOT0_S1_CID: Chip ID bits for Slot 0 Master 0/1 Slave 1.
6:8	RW	MBA_FARB1Q_CFG_SLOT0_S2_CID: Chip ID bits for Slot 0 Master 0/1 Slave 2.
9:11	RW	MBA_FARB1Q_CFG_SLOT0_S3_CID: Chip ID bits for Slot 0 Master 0/1 Slave 3.
12:14	RW	MBA_FARB1Q_CFG_SLOT0_S4_CID: Chip ID bits for Slot 0 Master 0/1 Slave 4 or Chip ID bits for Slot 0 Master 2/3 Slave 0.
15:17	RW	MBA_FARB1Q_CFG_SLOT0_S5_CID: Chip ID bits for Slot 0 Master 0/1 Slave 5 or Chip ID bits for Slot 0 Master 2/3 Slave 1.
18:20	RW	MBA_FARB1Q_CFG_SLOT0_S6_CID: Chip ID bits for Slot 0 Master 0/1 Slave 6 or Chip ID bits for Slot 0 Master 2/3 Slave 2.
21:23	RW	MBA_FARB1Q_CFG_SLOT0_S7_CID: Chip ID bits for Slot 0 Master 0/1 Slave 7 or Chip ID bits for Slot 0 Master 2/3 Slave 3.
24:26	RW	MBA_FARB1Q_CFG_SLOT1_S0_CID: Chip ID bits for Slot 1 Master 0/1 Slave 0.
27:29	RW	MBA_FARB1Q_CFG_SLOT1_S1_CID: Chip ID bits for Slot 1 Master 0/1 Slave 1.
30:32	RW	MBA_FARB1Q_CFG_SLOT1_S2_CID: Chip ID bits for Slot 1 Master 0/1 Slave 2.
33:35	RW	MBA_FARB1Q_CFG_SLOT1_S3_CID: Chip ID bits for Slot 1 Master 0/1 Slave 3.
36:38	RW	MBA_FARB1Q_CFG_SLOT1_S4_CID: Chip ID bits for Slot 1 Master 0/1 Slave 4 or Chip ID bits for Slot 1 Master 2/3 Slave 0.
39:41	RW	MBA_FARB1Q_CFG_SLOT1_S5_CID: Chip ID bits for Slot 1 Master 0/1 Slave 5 or Chip ID bits for Slot 1 Master 2/3 Slave 1.
42:44	RW	MBA_FARB1Q_CFG_SLOT1_S6_CID: Chip ID bits for Slot 1 Master 0/1 Slave 6 or Chip ID bits for Slot 1 Master 2/3 Slave 2.
45:47	RW	MBA_FARB1Q_CFG_SLOT1_S7_CID: Chip ID bits for Slot 1 Master 0/1 Slave 7 or Chip ID bits for Slot 1 Master 2/3 Slave 3.
48	RW	MBA_FARB1Q_CFG_DIS_SMDR: Set to 1 if using a 5D configuration. This uses the different master parameters instead of the SMDR.
49	RW	MBA_FARB1Q_CFG_DDR4_PARITY_ON_CID_DIS: Exclude CID bits in parity generation for DDR4.
50:63	RW	MBA_FARB1Q_CFG_RSV0: Reserved.

Register Name	Final ARB Parameters Register
Mnemonic	MC01.PORT2.SRQ.MBA_FARB2Q
Address	0000000007010995 (SCOM)
Description	Final ARB parameters

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MBA_FARB2Q_CFG_RANK0_RD_ODT: ODT bits required for a read Master Rank 0.
4:7	RW	MBA_FARB2Q_CFG_RANK1_RD_ODT: ODT bits required for a read Master Rank 1.

Bits	SCOM	Field Mnemonic: Description
8:11	RW	MBA_FARB2Q_CFG_RANK2_RD_ODT: ODT bits required for a read Master Rank 2.
12:15	RW	MBA_FARB2Q_CFG_RANK3_RD_ODT: ODT bits required for a read Master Rank 3.
16:19	RW	MBA_FARB2Q_CFG_RANK4_RD_ODT: ODT bits required for a read Master Rank 4.
20:23	RW	MBA_FARB2Q_CFG_RANK5_RD_ODT: ODT bits required for a read Master Rank 5.
24:27	RW	MBA_FARB2Q_CFG_RANK6_RD_ODT: ODT bits required for a read Master Rank 6.
28:31	RW	MBA_FARB2Q_CFG_RANK7_RD_ODT: ODT bits required for a read Master Rank 7.
32:35	RW	MBA_FARB2Q_CFG_RANK0_WR_ODT: ODT bits required for a write Master Rank 0.
36:39	RW	MBA_FARB2Q_CFG_RANK1_WR_ODT: ODT bits required for a write Master Rank 1.
40:43	RW	MBA_FARB2Q_CFG_RANK2_WR_ODT: ODT bits required for a write Master Rank 2.
44:47	RW	MBA_FARB2Q_CFG_RANK3_WR_ODT: ODT bits required for a write Master Rank 3.
48:51	RW	MBA_FARB2Q_CFG_RANK4_WR_ODT: ODT bits required for a write Master Rank 4.
52:55	RW	MBA_FARB2Q_CFG_RANK5_WR_ODT: ODT bits required for a write Master Rank 5.
56:59	RW	MBA_FARB2Q_CFG_RANK6_WR_ODT: ODT bits required for a write Master Rank 6.
60:63	RW	MBA_FARB2Q_CFG_RANK7_WR_ODT: ODT bits required for a write Master Rank 7.

Register Name	**N/M Throttling Control Register**
Mnemonic	MC01.PORT2.SRQ.MBA_FARB3Q
Address	0000000007010996 (SCOM)
Description	N/M Throttling Control

Bits	SCOM	Field Mnemonic: Description
0:14	RW	MBA_FARB3Q_CFG_NM_N_PER_SLOT: The N value for the NM throttling across a single slot. The maximum command count that can occur over a time interval M for one slot.
15:30	RW	MBA_FARB3Q_CFG_NM_N_PER_PORT: The N value for the NM throttling across the entire port (both slots). The maximum command count that can occur over a time interval M for the entire port.
31:44	RW	MBA_FARB3Q_CFG_NM_M: The M value for the NM throttling. This counts DRAM clock cycles. Set this to 0 to disable NM throttling.
45:47	RW	MBA_FARB3Q_CFG_NM_RAS_WEIGHT: The increment to be added to the N count each time a RAS is sent.
48:50	RW	MBA_FARB3Q_CFG_NM_CAS_WEIGHT: The increment to be added to the N count each time a CAS is sent.
51	RW	MBA_FARB3Q_RESERVED_51: Reserved.
52	RW	MBA_FARB3Q_RESERVED_52: Reserved.
53	RW	MBA_FARB3Q_CFG_NM_CHANGE_AFTER_SYNC: If set, changes to cfg_nm_n_per_slot, cfg_nm_n_per_port, cfg_nm_m, and min_max_domains will only be applied after a pc_sync command is seen.
54:63	RW	MBA_FARB3Q_RESERVED_54_63: Reserved.

Register Name	Final Command Arbiter Miscellaneous Register
Mnemonic	MC01.PORT2.SRQ.MBA_FARB4Q
Address	0000000007010997 (SCOM)
Description	Final Command Arbiter miscellaneous

Bits	SCOM	Field Mnemonic: Description
0:15	RW	MBA_FARB4Q_CFG_NOISE_WAIT_TIME: The time from RCD_err until the RCD error recovery procedure will start issuing precharge commands.
16:21	RW	MBA_FARB4Q_CFG_PRECHARGE_WAIT_TIME: The time from one precharge command to the next precharge command in the RCD error recovery procedure.
22	RW	MBA_FARB4Q_CFG_SIM_FAST_NOISE_WINDOW: This will skip the precharges and refreshes as part of the noise window and only observe the noise window wait time.
23:26	RW	MBA_FARB4Q_RESERVED_23_26: Reserved.
27:41	RW	MBA_FARB4Q_EMERGENCY_N: Programmable N for NM when the emergency throttle is enabled.
42:55	RW	MBA_FARB4Q_EMERGENCY_M: Programmable M for NM when the emergency throttle is enabled.
56:63	RW	MBA_FARB4Q_RESERVED_56_63: Reserved.

Register Name	DDR Interface SCOM Control Register
Mnemonic	MC01.PORT2.SRQ.MBA_FARB5Q
Address	0000000007010998 (SCOM)
Description	DDR Interface SCOM Control

Bits	SCOM	Field Mnemonic: Description
0:1	RW	MBA_FARB5Q_CFG_DDR_DPHY_NCLK: DDR PHY NCLK control.
2:3	RW	MBA_FARB5Q_CFG_DDR_DPHY_PCLK: DDR PHY PCLK control.
4	RW	MBA_FARB5Q_CFG_DDR_RESETN: DDR Resetn signal.
5	RW	MBA_FARB5Q_CFG_CCS_ADDR_MUX_SEL: CCS Address Mux Sel. This bit should be turned on until all multiple CCS instructions are completed. 0 selects address data from mainline logic. 1 selects address data from CCS logic.
6	RW	MBA_FARB5Q_CFG_CCS_INST_RESET_ENABLE: When set to 1, bit 16 of the CCS_INST_ARR0 will be driven out to DDR Resetn. When set to 0, cfg_ddr_resetn will be driven out to DDR Resetn.
7	RW	MBA_FARB5Q_CFG_GP_BIT_3_ENABLE: When set to 1, the inverted value of GP(3) will be driven on the force_mclk_low signal to the DDR PHYs. When set to 0, the value of the inverted value of cfg_force_mclk_low_n will be driven on the force_mclk_low signal to the DDR PHYs.
8	RW	MBA_FARB5Q_CFG_FORCE_MCLK_LOW_N: The inverted value of force_mclk_low_n will be driven on mba_ddr_force_mclk_low when cfg_gp_bit_3_enable is 0.
9:15	RW	MBA_FARB5Q_RESERVED_56_63: Reserved.

Register Name	DDR Port Status Register
Mnemonic	MC01.PORT2.SRQ.MBA_FARB6Q
Address	0000000007010999 (SCOM)
Description	DDR Port Status Register

Bits	SCOM	Field Mnemonic: Description
0:10	ROX	MBA_FARB6Q_CFG_BW_SNAPSHOT: DRAM data bus utilization over the last 4K DDR clock window. All 1s is 100 percent utilization.
11:14	ROX	MBA_FARB6Q_CFG_CKE_PUP_STATE: Indicates which of the four CKEs are on.
15	ROX	MBA_FARB6Q_CFG_STR_STATE: Indicates whether the DRAMS on this port are in STR.
16:20	ROX	MBA_FARB6Q_CFG_RRQ_DEPTH: RRQ Depth; Number of commands in the RRQ.
21:25	ROX	MBA_FARB6Q_CFG_WRQ_DEPTH: WRQ Depth; Number of commands in the WRQ.
26:30	ROX	MBA_FARB6Q_CFG_RCD_PARITY_DLY: Delay from parity error to error being seen back in the MBA. This value can then be placed back in the RCD protection time register.
31	ROX	MBA_FARB6Q_CFG_EVENTN: EventN monitor for thermal event.

Register Name	**MBA Error Report Register**
Mnemonic	MC01.PORT2.SRQ.MBA_ERR_REPORTQ
Address	000000000701099A (SCOM)
Description	MBA Error Report Register

Bits	SCOM	Field Mnemonic: Description
0	ROX	MBA_ERR_REPORTQ_WRQ_HANG_ERR: WRQ hang error; MBACALFIR bit 17.
1	ROX	MBA_ERR_REPORTQ_RRQ_HANG_ERR: RRQ hang error; MBACALFIR bit 17.
2	ROX	MBA_ERR_REPORTQ_DSM_PE_ERR: Parity error in DSM configuration registers; MBACALFIR bit 1.
3	ROX	MBA_ERR_REPORTQ_TMR_PE_ERR: Parity error in TMR configuration registers; MBACALFIR bit 1.
4	ROX	MBA_ERR_REPORTQ_RRQ_PE_ERR: Parity error in RRQ configuration registers; MBACALFIR bit 0.
5	ROX	MBA_ERR_REPORTQ_WRQ_PE_ERR: Parity error in WRQ configuration registers; MBACALFIR bit 0.
6	ROX	MBA_ERR_REPORTQ_FARB_PE_ERR: Parity error in FARB configuration registers; MBACALFIR bit 1.
7	ROX	MBA_ERR_REPORTQ_PC_PE_ERR: Parity error in PC configuration registers; MBACALFIR bit 0.
8	ROX	MBA_ERR_REPORTQ_CAL0_PE_ERR: Parity error in Cal0 configuration register; MBACALFIR bit 0.
9	ROX	MBA_ERR_REPORTQ_CAL1_PE_ERR: Parity error in Cal1 configuration register; MBACALFIR bit 0.
10	ROX	MBA_ERR_REPORTQ_CAL2_PE_ERR: Parity error in Cal2 configuration register ;MBACALFIR bit 0.
11	ROX	MBA_ERR_REPORTQ_CAL3_PE_ERR: Parity error in Cal3 configuration register; MBACALFIR bit 0.
12	ROX	MBA_ERR_REPORTQ_DDR_IF_SM_1HOT_ERR: DDR state machine one hot error; MBACALFIR bit 18.
13	ROX	MBA_ERR_REPORTQ_CAL_SM_1HOT_ERR: Calibration state machine one hot error; MBACALFIR bit 18.
14	ROX	MBA_ERR_REPORTQ_RANK_SM_1HOT_ERR: Rank state machine one hot error; MBACALFIR bit 18.
15	ROX	MBA_ERR_REPORTQ_RESERVED_15: Reserved 15.
16	ROX	MBA_ERR_REPORTQ_PC_CAL_PCFSM_1HOT_ERR: Power control state machine 1 hot error; MBACALFIR bit 18.
17	ROX	MBA_ERR_REPORTQ_FARB_CAL_RECVFSM_1HOT_ERR: Recovery state machine 1 hot error; MBACALFIR bit 18.
18:23	ROX	MBA_ERR_REPORTQ_RESERVED_18_23: Reserved.
24	ROX	MBA_ERR_REPORTQ_RCMD_ASYNC_IF_ERR: Sequence error on rcmd asynchronous crossing. Operations received out of order.
25	ROX	MBA_ERR_REPORTQ_PF_PROMOTE_ASYNC_IF_ERR: Sequence error on prefetch promote asynchronous crossing. Operations received out of order.

Bits	SCOM	Field Mnemonic: Description
26	ROX	MBA_ERR_REPORTQ_CANCEL_ACK_ASYNC_IF_ERR: Sequence error on cancel ACK asynchronous crossing. Operations received out of order.
27	ROX	MBA_ERR_REPORTQ_FARB_CMD_PE_HOLD_OUT: Parity error seen on new command to be issued by the sequencer.
28	ROX	MBA_ERR_REPORTQ_DSM_CMD_PE_HOLD_OUT: Parity error seen on command as it leaves the sequencer.
29:30	ROX	MBA_ERR_REPORTQ_RESERVED_29_30: Reserved.
31:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Emergency Throttle Register
Mnemonic	MC01.PORT2.SRQ.MBA_FARB7Q
Address	00000000070109A5 (SCOM)
Description	Emergency Throttle Register

Bits	SCOM	Field Mnemonic: Description
0	RW	MBA_FARB7Q_EMER_THROTTLE_IP: Emergency throttle in-progress. This register can also be set to manually engage an emergency throttle, or cleared to clear an emergency throttle.

Register Name	MBA Debug Bus Register 0
Mnemonic	MC01.PORT2.SRQ.MBA_DBG0Q
Address	00000000070109A6 (SCOM)
Description	MBA Debug Bus Register 0

Bits	SCOM	Field Mnemonic: Description
0	RW	MBA_DBG0Q_CFG_DBG_SRQ_ENABLE:
1:3	RW	MBA_DBG0Q_CFG_DBG_SRQ_SEL0:
4:6	RW	MBA_DBG0Q_CFG_DBG_SRQ_SEL1:
7:9	RW	MBA_DBG0Q_CFG_DBG_SRQ_SEL2:
10:12	RW	MBA_DBG0Q_CFG_DBG_SRQ_SEL3:
13:15	RW	MBA_DBG0Q_CFG_DBG_SRQ_SEL4:
16:18	RW	MBA_DBG0Q_CFG_DBG_SRQ_SEL5:
19:21	RW	MBA_DBG0Q_CFG_DBG_SRQ_SEL6:
22:24	RW	MBA_DBG0Q_CFG_DBG_SRQ_SEL7:
25:33	RW	MBA_DBG0Q_RESERVED_25_33:
34:41	RW	MBA_DBG0Q_CFG_DBG_SRQ_SEL_OTHER_SRQ:
42:47	RW	MBA_DBG0Q_RESERVED_42_47:
48:51	RW	MBA_DBG0Q_CFG_WAT_FARB_RRQ_GT:
52:55	RW	MBA_DBG0Q_CFG_WAT_FARB_WRQ_GT:
56:59	RW	MBA_DBG0Q_CFG_WAT_FARB_REF_GT:
60:63	RW	MBA_DBG0Q_CFG_WAT_FARB_CAL_GT:

Register Name	MBA Debug Bus Register 1
Mnemonic	MC01.PORT2.SRQ.MBA_DBG1Q
Address	00000000070109A7 (SCOM)
Description	MBA Debug Bus Register 1

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MBA_DBG1Q_CFG_WAT_FORCE_WR_ENTRY0_HP:
4:7	RW	MBA_DBG1Q_CFG_WAT_FORCE_RD_ENTRY0_HP:
8:11	RW	MBA_DBG1Q_CFG_WAT_FP_DIS:
12:15	RW	MBA_DBG1Q_CFG_WAT_DIS_RD_PG:
16:19	RW	MBA_DBG1Q_CFG_WAT_DIS_WR_PG:
20:23	RW	MBA_DBG1Q_CFG_WAT_PUP_ALL:
24:27	RW	MBA_DBG1Q_CFG_WAT_EXIT_STR:
28:31	RW	MBA_DBG1Q_CFG_WAT_REF_HP:
32:35	RW	MBA_DBG1Q_CFG_WAT_REF_SYNC:
36:39	RW	MBA_DBG1Q_CFG_WAT_REF_SAFE:
40:43	RW	MBA_DBG1Q_CFG_WAT_CAL_SYNC:
44:47	RW	MBA_DBG1Q_CFG_WAT_RRQ_MNT_GT:
48:51	RW	MBA_DBG1Q_CFG_WAT_WRQ_MNT_GT:
52:55	RW	MBA_DBG1Q_CFG_WAT_SET_FIR:
56:59	RW	MBA_DBG1Q_CFG_WAT_EMER_TH:
60:63	RW	MBA_DBG1Q_CFG_WAT_START_RECOVERY:

Register Name	Emergency Throttle Register
Mnemonic	MC01.PORT2.SRQ.MBA_FARB8Q
Address	00000000070109A8 (SCOM)
Description	Emergency Throttle Register

Bits	SCOM	Field Mnemonic: Description
0	RW	MBA_FARB8Q_SAFE_REFRESH_MODE: Safe refresh interval is being used for tREFI. This register can also be set to manually engage safe refresh or cleared to clear safe refresh.

Register Name	Timer State Machine Control Register
Mnemonic	MC01.PORT2.SRQ.MBA_TMR2Q
Address	00000000070109AF (SCOM)
Description	Timer state machine control.

Bits	SCOM	Field Mnemonic: Description
0:19	RW	MBA_TMR2Q_CFG_BANK_BUSY_FSM_DIS: Disable bank busy state machines 0 - 19, one bit per FSM.

Bits	SCOM	Field Mnemonic: Description
20:31	RW	MBA_TMR2Q_CFG_BANK_BUSY_OPEN_PAGE_DIS: Disable open page mode on bank busy state machines 0 - 11, one bit per FSM. Bank busy state machines 12 - 19 do not do open page mode.
32:63	RW	MBA_TMR2Q_RESERVED_32_63: Reserved.

Register Name	Refresh Register 0
Mnemonic	MC01.PORT2.SRQ.PC.MBAREF0Q
Address	00000000070109B2 (SCOM)
Description	Refresh register 0

Bits	SCOM	Field Mnemonic: Description
0	RW	MBAREF0Q_CFG_REFRESH_ENABLE: Refresh enable.
1:2	RW	MBAREF0Q_CFG_REFRESH_INTERVAL_TIMEBASE_SELECT: 01 = Reserved. For 10 and 11 settings, to determine the actual refresh interval, multiply the calculated refresh interval by 8k or 2^{22} depending on which timebase was used. **Note**: Settings 10 and 11 are for characterization stress testing only.
3	RW	MBAREF0Q_CFG_PER_BANK_REFRESH: Banks are individually refreshed each time a new refresh to a rank pops, and refresh must be sent to each bank separately before that refresh is considered complete. DDR4E only.
4	RW	MBAREF0Q_CFG_REFRESH_DEBUG_SELECT: Refresh debug bus select. 0 selects only master ranks. 1 selects slave ranks.
5:7	RW	MBAREF0Q_CFG_REFRESH_PRIORITY_THRESHOLD: After the number of queued refreshes to a rank reaches this threshold, that rank's refreshes become high priority. Values greater than 0x5 can potentially lead to a refresh timeout FIR.
8:18	RW	MBAREF0Q_CFG_REFRESH_INTERVAL: This value is multiplied by 8 to represent the number of DRAM command clock cycles at which a refresh is to be sent to a rank to honor the refresh interval (tREFI). A refresh to a specific rank will be seen 8 × cfg_refresh_interval × num_ranks × DRAM_command_clock_cycle_time. So, program this dial to: cfg_refresh_interval = desired_tREFI_in_usnum_ranksDRAM_command_clock_cycle_in_ns.008). For example, for a system with two master ranks and four slaves per master (eight ranks total), a desired refresh interval of 7.8 µs, and DDR-1600 memory, cfg_refresh_interval = 7.881.25.008 = 97 (round down).
19:29	RW	MBAREF0Q_CFG_REFRESH_RESET_INTERVAL: This is a value to load the refresh interval counter to when a syncreset pulse is seen from the MBA. This is used to offset refreshing to the different MBAs. **Note**: Refresh reset interval should be set to a value less than the refresh interval.
30:39	RW	MBAREF0Q_CFG_TRFC: Refresh to activate rank protection timer.
40:49	RW	MBAREF0Q_CFG_REFR_TSV_STACK: Refresh-to-refresh spacing within the same TSV stack timer.
50:60	RW	MBAREF0Q_CFG_REFR_CHECK_INTERVAL: This setting is used to verify that the refresh rules are upheld only (it is not the actual refresh interval). It is multiplied by 8 to represent the number of DRAM command clock cycles at which a refresh is to be seen to a given rank to honor the refresh interval (tREFI). A refresh to a specific rank should be seen 8 × cfg_refresh_check_interval × DRAM_command_clock_cycle_time. So, program this dial to: cfg_refr_check_interval = desired_tREFI_in_usDRAM_command_clock_cycle_in_ns.008). For example, if using DDR-1600 memory and expecting a refresh to occur every 7.8 µs: cfg_refr_check_interval = 7.81.25.008 = 780 = 0x30C. If using DDR-1600 memory and expecting a refresh every 3.9 µs: cfg_refr_check_interval = 3.91.25.008 = 390 = 0x186.
61	RW	MBAREF0Q_CFG_TRFC_STACK_GATE_ALL_REF: When set, this causes all refreshes to be spaced by cfg_refr_tsv_stack, regardless of whether they are to ranks on the same stack. This mode can be enabled as a means to reduce the power impact due to a burst of refreshes to different ranks.

Bits	SCOM	Field Mnemonic: Description
62:63	RW	MBAREF0Q_RESERVED_62_63: Reserved.

Register Name	Reserved SCOM Address Register
Mnemonic	MC01.PORT2.SRQ.PC.MBARSVD0
Address	00000000070109B3 (SCOM)
Description	Reserved SCOM Register Address

Bits	SCOM	Field Mnemonic: Description
0:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	Power Control Register 0
Mnemonic	MC01.PORT2.SRQ.PC.MBARPC0Q
Address	00000000070109B4 (SCOM)
Description	Power Control Register 0

Bits	SCOM	Field Mnemonic: Description
0:1	RW	MBARPC0Q_RESERVED_0_1: Reserved.
2	RW	MBARPC0Q_CFG_MIN_MAX_DOMAINS_ENABLE: This is an overall enable for power domain control. If power control is disabled, the CKEs will always be set to a '1'.
3:5	RW	MBARPC0Q_CFG_MIN_MAX_DOMAINS: Configures dynamic power up and power down of CKEs within specified minimum/maximum limits. Maxall_minall means power control will not limit the number of domains accessible at a given time. Power domains will not be powered down even if they go idle, unless min_domain_reduction is enabled. Maxall_minx will permit idle power down to reduce the number of domains powered up after a domain has gone idle, but it will not restrict the maximum domains powered up. Max1_minx restricts the number of domains that can be powered up at a given time to 1.
6:10	RW	MBARPC0Q_CFG_PUP_AVAIL: Specifies how many DRAM command clocks for power control to wait from CKE going high to activate.
11:15	RW	MBARPC0Q_CFG_PDN_PUP: Specifies how many DRAM command clocks for power control to wait from CKE going low to high again (enforces the minimum time in power down).
16:20	RW	MBARPC0Q_CFG_PUP_PDN: Specifies how many DRAM command clocks for power control to wait from CKE going high to low again (enforces the minimum time powered up).
21	RW	MBARPC0Q_RESERVED_21: Reserved.
22	RW	MBARPC0Q_CFG_MIN_DOMAIN_REDUCTION_ENABLE: This allows a dynamic reduction of the minimum domains to 0 when no memory traffic has been seen over the specified cfg_min_domain_reduction_time. Minimum domains will be restored after traffic is seen. The adjusted minimum domains will not be reflected in or overwrite the cfg_min_max_domains setting (adjustment made internal to logic).
23:32	RW	MBARPC0Q_CFG_MIN_DOMAIN_REDUCTION_TIME: Specifies how many DRAM command clocks the MBA must be idle before min_cke is reduced to 0.
33	RW	MBARPC0Q_CFG_PUP_AFTER_ACTIVATE_WAIT_ENABLE: After a configurable time has been met since the last activate, a subsequent domain can be powered up, even if the powering-down domain has not been powered down yet.
34:41	RW	MBARPC0Q_CFG_PUP_AFTER_ACTIVATE_WAIT_TIME: Specifies how many DRAM command clocks the MBA must be idle before minimum domains is reduced to 0.
42	RW	MBARPC0Q_CFG_FORCE_SPARE_PUP: Forces all spare CKEs to couple with their respective primary CKEs. This bit should not be toggled during run time or when calibration is enabled.

Bits	SCOM	Field Mnemonic: Description
43	RW	MBARPC0Q_CFG_MIN_DOMAIN_REDUCTION_CNT_REFR_INT: If set, use the refresh interval for minimum domain reduction time interval. Otherwise, use DRAM clocks as the interval.
44:46	RW	MBARPC0Q_CFG_EMER_MIN_MAX_DOMAIN: This is the minimum/maximum power domain setting that power control will revert to when emergency throttling is engaged.
47	RW	MBARPC0Q_CFG_PUP_ALL_WRITES_PENDING: Enabling this allows a domain to be powered up upon a write entering the write reorder queue (provided the maximum domains is set to all). **Note**: Reads always cause a power up to their power domain upon entering the read reorder queue (when maximum domains is set to all).
48	RW	MBARPC0Q_CFG_ALWAYS_WAIT_ACT_TIME: If set, when in single-domain power up mode, we will always wait the configured time between activates even when all domains are powered down already.
49:63	RW	MBARPC0Q_RESERVED_49_63: Reserved.

Register Name	**STR Register 0**
Mnemonic	MC01.PORT2.SRQ.PC.MBASTR0Q
Address	00000000070109B5 (SCOM)
Description	STR Register 0

Bits	SCOM	Field Mnemonic: Description
0	RW	MBASTR0Q_CFG_STR_ENABLE: Enable STR Entry. **Note**: Minimum-maximum domains must also be enabled to enter STR.
1	RW	MBASTR0Q_CFG_DIS_CLK_IN_STR: Disable memory clocks when in STR.
2:11	RW	MBASTR0Q_CFG_ENTER_STR_TIME: Number of cfg_min_domain_reduction intervals of idle to wait before entering STR.
12:16	RW	MBASTR0Q_CFG_TCKESR: tCKESR
17:21	RW	MBASTR0Q_CFG_TCKSRE: tCKSRE
22:26	RW	MBASTR0Q_CFG_TCKSRX: tCKSRX
27:37	RW	MBASTR0Q_CFG_TXSDLL: tXSDLL
38:45	RW	MBASTR0Q_CFG_TRFC_COUNTER_DIS: Per tRFC counter disable. You can use this to restrict the number of outstanding refreshes.
46:56	RW	MBASTR0Q_CFG_SAFE_REFRESH_INTERVAL: This is the refresh interval used when in safe-refresh (high-temp) mode. This value is multiplied by 8 to represent the number of DRAM command clock cycles at which a refresh is to be sent to a rank in order to honor the refresh interval (tREFI). A refresh to a specific rank will be seen 8 × cfg_safe_refresh_interval × num_ranks × DRAM_command_clock_cycle_time. So, program this dial to: cfg_safe_refresh_interval=desired_tREFI_in_usnum_ranksDRAM_command_clock_cycle_in_ns.008). For example, for a system with two master ranks and 4 slaves per master (8 ranks total), a desired refresh interval of 7.8 µs, and DDR-1600 memory, cfg_safe_refresh_interval = 7.881.25.008 = 97 (round down)

Bits	SCOM	Field Mnemonic: Description
57:60	RW	MBASTR0Q_CFG_OCC_DEADMAN_TIMER_SEL: This selects one of 8 timeout values for the OCC deadman timer. If the OCC is idle for the programmed timeout value × timebase pulse, an emergency throttle command command is issued and refresh is set to safe refresh interval. Value Time: 0000 = Disabled 0001 = 16 timebase pulses 0010 = 4 timebase pulses 0011 = 8 timebase pulses 0100 = 16 timebase pulses 0101 = 32 timebase pulses 0110 = 64 timebase pulses 0111 = 128 timebase pulses 1000 = 255 timebase pulses 1001 to 1111 are unused.
61	RW	MBASTR0Q_CFG_OCC_DEADMAN_TB_SEL: This selects which timebase pulse to use for the deadman timer. 0 = 1 in 2^{22} DRAM command clocks 1 = 1 in 8K DRAM command clocks
62:63	RW	MBASTR0Q_RESERVED_62_63: Reserved.

Register Name	**Refresh Avoidance Control Register**
Mnemonic	MC01.PORT2.SRQ.PC.MBAREFAQ
Address	00000000070109B6 (SCOM)
Description	Refresh Avoidance Control Register

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MBAREFAQ_CFG_STATIC_IDLE_DLY: This is the number of cycles that the refresh logic will wait for a rank to be idle in the RRQ before sending a low-priority refresh. **Note**: This delay counts in multiples of four DDR clocks (per default lp ref subcounter setting).
4:5	RW	MBAREFAQ_CFG_LP_SUB_CNT: Subcounter for lp refresh scheduling dials. For dials that count based on this subcounter, a value of 00 means the counter those dials compare against increments every 1 cycle. A value of 01 in this register means the higher-level count increments every 4th cycle (10 is every 8th cycle, and 11 is every 16th cycle).
6	RW	MBAREFAQ_CFG_REFRESH_HP_RANK_BLOCK_ENABLE: When enabled, the refresh logic sends a block signal when issuing a high-priority refresh. The block signal prevents new demand requests to the refreshing rank from overwhelming the read reorder queue.
7:9	RW	MBAREFAQ_RESERVED_7_9: Reserved.
10:15	RW	MBAREFAQ_CFG_REF_BLOCK_STOP_DLY: Programmable setting which is subtracted from the tRFC timer. The result is used to determine when the block signal can be deasserted leading up to the end of a tRFC period. This allows new commands targeting the refresh domain being refreshed to progress to the RRQ so that they are ready to go as soon as tRFC ends. (N)

Register Name	**Performance Monitor Counts0 Register**
Mnemonic	MC01.PORT2.SRQ.MBA_PMU0Q
Address	00000000070109B7 (SCOM)
Description	Performance monitor counts0

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MBA_PMU0Q_READ_COUNT: Read count. Increments every read; wraps.
32:63	ROX	MBA_PMU0Q_WRITE_COUNT: Write count. Increments every write; wraps.

Register Name	Performance Monitor Counts1 Register
Mnemonic	MC01.PORT2.SRQ.MBA_PMU1Q
Address	00000000070109B8 (SCOM)
Description	Performance monitor counts1

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MBA_PMU1Q_ACTIVATE_COUNT: Bank activate count. Increments for every activate; wraps.
32:63	ROX	MBA_PMU1Q_PU_COUNTS: Counts the number of rising edges for a CKE; wraps.

Register Name	Performance Monitor Counts2 Register
Mnemonic	MC01.PORT2.SRQ.MBA_PMU2Q
Address	00000000070109B9 (SCOM)
Description	Performance monitor counts2

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MBA_PMU2Q_FRAME_COUNT: Frame count. Increments every DRAM clock(2:1) clock.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Performance Monitor Counts4 Register
Mnemonic	MC01.PORT2.SRQ.MBA_PMU3Q
Address	00000000070109BA (SCOM)
Description	Performance monitor counts4

Bits	SCOM	Field Mnemonic: Description
0:15	RW	MBA_PMU3Q_LOW_IDLE_THRESHOLD: Each time the low idle (no reads or writes queued) threshold is met, the low idle count will increment. Between periods of command activity, there may be multiple low-idle-threshold-width windows of command inactivity. For each of these windows, the low idle count will be incremented. (counts 2:1Dram address frequency) counts MBA idle cycles.
16:31	RW	MBA_PMU3Q_MED_IDLE_THRESHOLD: Each time the medium idle (no reads or writes queued) threshold is met, the medium idle count will increment. Between periods of command activity, there may be multiple med-idle-threshold-width windows of command inactivity. For each of these windows, the medium idle count will be incremented.
32:63	RW	MBA_PMU3Q_HIGH_IDLE_THRESHOLD: Each time the high idle (no reads or writes queued) threshold is met, the high idle count will increment. Between periods of command activity, there may be multiple high-idle-threshold-width windows of command inactivity. For each of these windows, the high idle count will be incremented.

Register Name	Performance Monitor Counts Register
Mnemonic	MC01.PORT2.SRQ.MBA_PMU4Q
Address	00000000070109BB (SCOM)
Description	Performance monitor counts

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MBA_PMU4Q_BASE_IDLE_COUNT: Increments every MBA idle cycle (counts 2:1Dram address frequency).
32:63	ROX	MBA_PMU4Q_LOW_IDLE_COUNT: Counts the number of times the low idle threshold was met (counts 2:1Dram address frequency).

Register Name	Performance Monitor Counts Register
Mnemonic	MC01.PORT2.SRQ.MBA_PMU5Q
Address	00000000070109BC (SCOM)
Description	Performance monitor counts

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MBA_PMU5Q_MED_IDLE_COUNT: Counts the number of times the medium idle threshold was met (counts 2:1Dram address frequency).
32:63	ROX	MBA_PMU5Q_HIGH_IDLE_COUNT: Counts the number of times the high idle threshold was met (counts 2:1Dram address frequency).

Register Name	Performance Monitor Counts Register
Mnemonic	MC01.PORT2.SRQ.MBA_PMU6Q
Address	00000000070109BD (SCOM)
Description	Performance monitor counts

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	MBA_PMU6Q_EVENT0_COUNTER: PMU count for event 0.
16:31	ROX	MBA_PMU6Q_EVENT1_COUNTER: PMU count for event 1.
32:47	ROX	MBA_PMU6Q_EVENT2_COUNTER: PMU count for event 2.
48:63	ROX	MBA_PMU6Q_EVENT3_COUNTER: PMU count for event 3.

Register Name	Performance Monitor Event Select Register
Mnemonic	MC01.PORT2.SRQ.MBA_PMU7Q
Address	00000000070109BE (SCOM)
Description	Performance monitor event select register

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MBA_PMU7Q_CFG_EVENT0_SELECT: Event0 select: 0x00 = MBA command clocks 0x01 = ACT all 0x02 = ACT for read 0x03 = ACT for write 0x04 = CAS all 0x05 = CAS for read 0x06 = CAS for write 0x07 = CAS for low-priority write 0x08 = CAS for high-priority write 0x09 = PRE all 0x0a = PRE for read 0x0b = PRE for write 0x0c = REF high priority 0x0d = REF low priority 0x0e = REF all 0x0f = RRQ empty 0x10 = RRQ full 0x11 = WRQ empty 0x12 = WRQ full 0x13 = WRQ above hw mark 0x14 = Reserved 0x15 = Activate with direction switch (change from rd→wr or wr→rd) 0x16 = Activate with mrank switch (Master rank different than previous ACT) 0x17 = Activate with srank switch (Same master; slave rank different than previous ACT) 0x18 = Activate with bank group switch (Same master, slave; bank group different than previous ACT) 0x19 = Activate with bank switch (Same master, slave, bank group; different bank than previous ACT) 0x1a = All bank timers full 0x1b = Any CKE PUP transition (0→1) 0x1c = CKE0 cycles PUP 0x1d = CKE1 cycles PUP 0x1e = CKE2 cycles PUP 0x1f = CKE3 cycles PUP 0x20 = WDF stalled waiting on read buffer 0x21 = WDF stalled waiting on read ramp 0x22 = Command0 Compare 0x23 - 0x3f = Reserved

Bits	SCOM	Field Mnemonic: Description
6:11	RW	MBA_PMU7Q_CFG_EVENT1_SELECT: Event1 select: 0x00 = MBA command clocks 0x01 = ACT all 0x02 = ACT for read 0x03 = ACT for write 0x04 = CAS all 0x05 = CAS for read 0x06 = CAS for write 0x07 = CAS for low-priority write 0x08 = CAS for high-priority write 0x09 = PRE all 0x0a = PRE for read 0x0b = PRE for write 0x0c = REF high priority 0x0d = REF low priority 0x0e = REF all 0x0f = RRQ empty 0x10 = RRQ full 0x11 = WRQ empty 0x12 = WRQ full 0x13 = WRQ above hw mark 0x14 = Reserved 0x15 = Activate with direction switch (change from rd→wr or wr→rd) 0x16 = Activate with mrank switch (Master rank different than previous ACT) 0x17 = Activate with srank switch (Same master; slave rank different than previous ACT) 0x18 = Activate with bank group switch (Same master, slave; bank group different than previous ACT) 0x19 = Activate with bank switch (Same master, slave, bank group; different bank than previous ACT) 0x1a = All bank timers full 0x1b = Any CKE PUP transition (0→1) 0x1c = CKE0 cycles PUP 0x1d = CKE1 cycles PUP 0x1e = CKE2 cycles PUP 0x1f = CKE3 cycles PUP 0x20 = WDF stalled waiting on read buffer 0x21 = WDF stalled waiting on read ramp 0x22 = Command1 Compare 0x23 - 0x3f = Reserved

Bits	SCOM	Field Mnemonic: Description
12:17	RW	MBA_PMU7Q_CFG_EVENT2_SELECT: Event2 select: 0x00 = MBA command clocks 0x01 = ACT all 0x02 = ACT for read 0x03 = ACT for write 0x04 = CAS all 0x05 = CAS for read 0x06 = CAS for write 0x07 = CAS for low-priority write 0x08 = CAS for high-priority write 0x09 = PRE all 0x0a = PRE for read 0x0b = PRE for write 0x0c = REF high priority 0 x0d = REF low priority 0x0e = REF all 0x0f = RRQ empty 0x10 = RRQ full 0x11 = WRQ empty 0x12 = WRQ full 0x13 = WRQ above hw mark 0x14 = Reserved 0x15 = Activate with direction switch (change from rd→wr or wr→rd) 0x16 = Activate with mrank switch (Master rank different than previous ACT) 0x17 = Activate with srank switch (Same master; slave rank different than previous ACT) 0x18 = Activate with bank group switch (Same master, slave; bank group different than previous ACT) 0x19 = Activate with bank switch (Same master, slave, bank group; different bank than previous ACT) 0x1a = All bank timers full 0x1b = Any CKE PUP transition (0→1) 0x1c = CKE0 cycles PUP 0x1d = CKE1 cycles PUP 0x1e = CKE2 cycles PUP 0x1f = CKE3 cycles PUP 0x20 = WDF stalled waiting on read buffer 0x21 = WDF stalled waiting on read ramp 0x22 = Command2 Compare 0x23 - 0x3f = Reserved

Bits	SCOM	Field Mnemonic: Description
18:23	RW	MBA_PMU7Q_CFG_EVENT3_SELECT: Event3 select: 0x00 = MBA command clocks 0x01 = ACT all 0x02 = ACT for read 0x03 = ACT for write 0x04 = CAS all 0x05 = CAS for read 0x06 = CAS for write 0x07 = CAS for low-priority write 0x08 = CAS for high-priority write 0x09 = PRE all 0x0a = PRE for read 0x0b = PRE for write 0x0c = REF high priority 0x0d = REF low priority 0x0e = REF all 0x0f = RRQ empty 0x10 = RRQ full 0x11 = WRQ empty 0x12 = WRQ full 0x13 = WRQ above hw mark 0x14 = Reserved 0x15 = Activate with direction switch (change from rd→wr or wr→rd) 0x16 = Activate with mrank switch (Master rank different than previous ACT) 0x17 = Activate with srank switch (Same master; slave rank different than previous ACT) 0x18 = Activate with bank group switch (Same master, slave; bank group different than previous ACT) 0x19 = Activate with bank switch (Same master, slave, bank group; different bank than previous ACT) 0x1a = All bank timers full 0x1b = Any CKE PUP transition (0→1) 0x1c = CKE0 cycles PUP 0x1d = CKE1 cycles PUP 0x1e = CKE2 cycles PUP 0x1f = CKE3 cycles PUP 0x20 = WDF stalled waiting on read buffer 0x21 = WDF stalled waiting on read ramp 0x22 - 0x3f = Reserved
24:25	RW	MBA_PMU7Q_CFG_PRESCALER_C0: Prescaler for event counter 0: 00 = 20-bit 01 =16-bit 10 = 8-bit 11 = 4-bit
26:27	RW	MBA_PMU7Q_CFG_PRESCALER_C1: Prescaler for event counter 1: 00 = 20-bit 01 =16-bit 10 = 8-bit 11 = 4-bit
28:29	RW	MBA_PMU7Q_CFG_PRESCALER_C2: Prescaler for event counter 2: 00 = 20-bit 01 =16-bit 10 = 8-bit 11 = 4-bit
30:31	RW	MBA_PMU7Q_CFG_PRESCALER_C3: Prescaler for event counter 3: 00 = 20-bit 01 =16-bit 10 = 8-bit 11 = 4-bit

Bits	SCOM	Field Mnemonic: Description
32:34	RW	MBA_PMU7Q_CASCADE: Allows cascading of counts to make a 32-bit counter: X00 = no cascading 001 = c0 → c1 010 = c1 → c2 011 = c2 → c3 101 = c1 → c0 110 = c2 → c1 111 = c3 → c2
35	RW	MBA_PMU7Q_FREEZE: If enabled, freeze all counters when any counter reaches maximum.

Register Name	Performance Monitor Command Compare Register
Mnemonic	MC01.PORT2.SRQ.MBA_PMU8Q
Address	00000000070109BF (SCOM)
Description	Performance monitor command compare register

Bits	SCOM	Field Mnemonic: Description
0:1	RW	MBA_PMU8Q_CFG_CMD0_TYPE: Command 0 compare type qualifier: 00 = Read 01 = Write 10 = Activate 11 = Read Or Write
2	RW	MBA_PMU8Q_CFG_CMD0_MRANK_MATCH_EN:
3	RW	MBA_PMU8Q_CFG_CMD0_SRANK_MATCH_EN:
4	RW	MBA_PMU8Q_CFG_CMD0_BG_MATCH_EN:
5	RW	MBA_PMU8Q_CFG_CMD0_BANK_MATCH_EN:
6:8	RW	MBA_PMU8Q_CFG_CMD0_MRANK:
9:11	RW	MBA_PMU8Q_CFG_CMD0_SRANK:
12:13	RW	MBA_PMU8Q_CFG_CMD0_BG:
14:16	RW	MBA_PMU8Q_CFG_CMD0_BANK:
17:18	RW	MBA_PMU8Q_CFG_CMD1_TYPE: Command 1 compare type qualifier: 00 = Read 01 = Write 10 = Activate 11 = Read or write
19	RW	MBA_PMU8Q_CFG_CMD1_MRANK_MATCH_EN:
20	RW	MBA_PMU8Q_CFG_CMD1_SRANK_MATCH_EN:
21	RW	MBA_PMU8Q_CFG_CMD1_BG_MATCH_EN:
22	RW	MBA_PMU8Q_CFG_CMD1_BANK_MATCH_EN:
23:25	RW	MBA_PMU8Q_CFG_CMD1_MRANK:
26:28	RW	MBA_PMU8Q_CFG_CMD1_SRANK:
29:30	RW	MBA_PMU8Q_CFG_CMD1_BG:
31:33	RW	MBA_PMU8Q_CFG_CMD1_BANK:

Bits	SCOM	Field Mnemonic: Description
34:35	RW	MBA_PMU8Q_CFG_CMD2_TYPE: Command 2 compare type qualifier: 00 = Read 01 = Write 10 = Activate 11 = Read or write
36	RW	MBA_PMU8Q_CFG_CMD2_MRANK_MATCH_EN:
37	RW	MBA_PMU8Q_CFG_CMD2_SRANK_MATCH_EN:
38	RW	MBA_PMU8Q_CFG_CMD2_BG_MATCH_EN:
39	RW	MBA_PMU8Q_CFG_CMD2_BANK_MATCH_EN:
40:42	RW	MBA_PMU8Q_CFG_CMD2_MRANK:
43:45	RW	MBA_PMU8Q_CFG_CMD2_SRANK:
46:47	RW	MBA_PMU8Q_CFG_CMD2_BG:
48:50	RW	MBA_PMU8Q_CFG_CMD2_BANK:
51:63	RW	MBA_PMU8Q_RESERVED_51_63:

Register Name	**MBA CAL FIR Register**
Mnemonic	MC01.PORT3.SRQ.MBACALFIRQ
Address	00000000070109C0 (SCOM) 00000000070109C1 (SCOM1) 00000000070109C2 (SCOM2)
Description	MBA CAL FIR Register (MBACALFIR)

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	MBACALFIRQ_MBA_RECOVERABLE_ERROR: When set, an MBA recoverable error has occurred. These include cal[0:3]_cfg, RRQ, WRQ, and power control parity errors.
1	RWX	WOX_AND	WOX_OR	MBACALFIRQ_MBA_NONRECOVERABLE_ERROR: When set, an MBA nonrecoverable error has occurred. These include DSM, TMR, FARB, and SIR parity errors.
2	RWX	WOX_AND	WOX_OR	MBACALFIRQ_REFRESH_OVERRUN: When set, nine (9) refreshes have been enqueued to any single rank.
3	RWX	WOX_AND	WOX_OR	MBACALFIRQ_WAT_ERROR: When set, an error has been detected in the MBA debug WAT logic.
4	RWX	WOX_AND	WOX_OR	MBACALFIRQ_RCD_PARITY_ERROR: When set, an RCD parity error has been detected on DDR port 0. If the error was seen during a calibration, FIR 14 will fire instead.
5	RWX	WOX_AND	WOX_OR	MBACALFIRQ_DDR_CAL_TIMEOUT_ERR: When set, a calibration complete indication was not received in the calibration timeout time for DDR0.
6	RWX	WOX_AND	WOX_OR	MBACALFIRQ_EMERGENCY_THROTTLE: Emergency throttle engaged either due to an OCC request or a deadman timer pop.
7	RWX	WOX_AND	WOX_OR	MBACALFIRQ_DDR_CAL_RESET_TIMEOUT: When set, indicates that a soft reset issued to the DDR PHY did not clear a pending calibration update request.
8	RWX	WOX_AND	WOX_OR	MBACALFIRQ_DDR_MBA_EVENT_N: When set, indicates that event_n was active on the DDR interface.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
9	RWX	WOX_AND	WOX_OR	MBACALFIRQ_WRQ_RRQ_HANG_ERR: When set, indicates that the WRQ or RRQ is in a hung state.
10	RWX	WOX_AND	WOX_OR	MBACALFIRQ_SM_1HOT_ERR: When set, indicates a state machine one hot error.
11	RWX	WOX_AND	WOX_OR	MBACALFIRQ_ASYNC_IF_ERROR: Sequencer error seen when crossing the asynchronous interface from the MCS.
12	RWX	WOX_AND	WOX_OR	MBACALFIRQ_CMD_PARITY_ERROR: Address parity error seen internal to the sequencer on a read or write command
13	RWX	WOX_AND	WOX_OR	MBACALFIRQ_PORT_FAIL: The port has failed due to a persistent retry. All reads returned with an RCD error so that the SUE will be delivered upstream.
14	RWX	WOX_AND	WOX_OR	MBACALFIRQ_RCD_CAL_PARITY_ERROR: When set, an RCD parity error has been detected during a calibration.
15	RWX	WOX_AND	WOX_OR	MBACALFIRQ_INTERNAL_SCOM_ERROR: When set, an internal SCOM error has occurred.
16	RWX	WOX_AND	WOX_OR	MBACALFIRQ_INTERNAL_SCOM_ERROR_COPY: Copy of internal SCOM error.
17:63	RO	RO	RO	Constant = 0b00000000000000000000000000000000000000000000000000000

Register Name	MBA CAL FIR Mask Register
Mnemonic	MC01.PORT3.SRQ.MBACALFIR_MASK
Address	00000000070109C3 (SCOM) 00000000070109C4 (SCOM1) 00000000070109C5 (SCOM2)
Description	MBA CAL FIR Mask Register (MBACALFIR_MASK)

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	MBACALFIR_MASK_MBA_RECOVERABLE_ERROR: When set, an MBA recoverable error has occurred. These include cal[0:3]_cfg, RRQ, WRQ, and power control parity errors.
1	RW	WO_AND	WO_OR	MBACALFIR_MASK_MBA_NONRECOVERABLE_ERROR: When set, an MBA nonrecoverable error has occurred. These include DSM, TMR, FARB, and SIR parity errors.
2	RW	WO_AND	WO_OR	MBACALFIR_MASK_REFRESH_OVERRUN: When set, nine (9) refreshes have been enqueued to any single rank.
3	RW	WO_AND	WO_OR	MBACALFIR_MASK_WAT_ERROR: When set, an error has been detected in the MBA debug WAT logic
4	RW	WO_AND	WO_OR	MBACALFIR_MASK_RCD_PARITY_ERROR: When set, an RCD parity error has been detected on DDR port 0.
5	RW	WO_AND	WO_OR	MBACALFIR_MASK_DDR_CAL_TIMEOUT_ERR: When set, a calibration complete indication was not received in the calibration timeout time for DDR0.
6	RW	WO_AND	WO_OR	MBACALFIR_MASK_EMERGENCY_THROTTLE: Emergency throttle engaged either due to an OCC request or a deadman timer pop.
7	RW	WO_AND	WO_OR	MBACALFIR_MASK_DDR_CAL_RESET_TIMEOUT: When set, indicates that a soft reset issued to the DDR PHY did not clear a pending calibration update request.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
8	RW	WO_AND	WO_OR	MBACALFIR_MASK_DDR_MBA_EVENT_N: When set, indicates that event_n was active on the DDR interface.
9	RW	WO_AND	WO_OR	MBACALFIR_MASK_WRQ_RRQ_HANG_ERR: When set, indicates that the WRQ or RRQ is in a hung state.
10	RW	WO_AND	WO_OR	MBACALFIR_MASK_SM_1HOT_ERR: When set, indicates a state machine one hot error.
11	RW	WO_AND	WO_OR	MBACALFIR_MASK_ASYNC_IF_ERROR: Sequencer error seen when crossing the asynchronous interface from the MCS.
12	RW	WO_AND	WO_OR	MBACALFIR_MASK_CMD_PARITY_ERROR: Address parity error seen internal to the sequencer on a read or write command
13	RW	WO_AND	WO_OR	MBACALFIRQ_MASK_PORT_FAIL: The port has failed due to a persistent retry. All reads returned with an RCD error so that a SUE will be delivered upstream.
14	RW	WO_AND	WO_OR	MBACALFIRQ_MASK_RCD_CAL_PARITY_ERROR: When set, an RCD parity error has been detected during a calibration.
15	RW	WO_AND	WO_OR	MBACALFIR_MASK_INTERNAL_SCOM_ERROR: When set, an internal SCOM error has occurred.
16	RW	WO_AND	WO_OR	MBACALFIR_MASK_INTERNAL_SCOM_ERROR_COPY: Copy of internal SCOM error.
17:63	RO	RO	RO	Constant = 0b00000000000000000000000000000000000000000000000000000

Register Name	**MBA CAL FIR Action 0 Register**
Mnemonic	MC01.PORT3.SRQ.MBACALFIR_ACTION0
Address	00000000070109C6 (SCOM)
Description	MBA CAL FIR Action 0 Register (MBACALFIR_ACTION0)

Bits	SCOM	Field Mnemonic: Description
0:16	RW	MBACALFIR_ACTION0_FIR_ACTION0: MBA action0 select for the corresponding bit in the FIR. (Action0, Action1, Mask) = Action Select: (0,0,X) = No error reported (0,1,0) = Recoverable error (1,0,0) = Checkstop error (1,1,0) = Local core checkstop freeze (X,X,1) = Masked
17:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000

Register Name	**MBA CAL FIR Action 1 Register**
Mnemonic	MC01.PORT3.SRQ.MBACALFIR_ACTION1
Address	00000000070109C7 (SCOM)
Description	MBA CAL FIR Action 1 Register (MBACALFIR_ACTION1)

Bits	SCOM	Field Mnemonic: Description
0:16	RW	MBACALFIR_ACTION1_FIR_ACTION1: MBA action1 select for the corresponding bit in the FIR. (Action0, Action1, Mask) = Action Select: (0,0,X) = No error reported (0,1,0) = Recoverable error (1,0,0) = Checkstop error (1,1,0) = Local core checkstop freeze (X,X,1) = Masked
17:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000

Register Name	Data State Machine Configurations Register
Mnemonic	MC01.PORT3.SRQ.MBA_DSM0Q
Address	00000000070109CA (SCOM)
Description	Data State Machine Configurations

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MBA_DSM0Q_CFG_RODT_START_DLY: Delay from the read command to ODT turn on.
6:11	RW	MBA_DSM0Q_CFG_RODT_END_DLY: Delay from the read command to ODT turn off.
12:17	RW	MBA_DSM0Q_CFG_WODT_START_DLY: Delay from the write command to ODT turn on.
18:23	RW	MBA_DSM0Q_CFG_WODT_END_DLY: Delay from the write command to ODT turn off.
24:29	RW	MBA_DSM0Q_CFG_WRDONE_DLY: Delay from the write command to write done to MBS.
30:35	RW	MBA_DSM0Q_CFG_WRDATA_DLY: Delay from the write command to stating the write data flow.
36:41	RW	MBA_DSM0Q_CFG_RDTAG_DLY: Delay from the read command to rd data valid back to MBS.
42	RW	MBA_DSM0Q_CFG_RDTAG_MBX_CYCLE: Determines the memory clock 1/2 cycle that the rdtag entry is released from the DSM queue. 0 = Release when the mbx clock is low. 1 = Release when the mbx clock is high.
43:48	RW	MBA_DSM0Q_CFG_RODT_BC4_END_DLY: Delay from the read command to ODT turn off for BC4 command.
49:54	RW	MBA_DSM0Q_CFG_WODT_BC4_END_DLY: Delay from the write command to ODT turn off for BC4 command.
55:63	RW	MBA_DSM0Q_RESERVED_55_63: Reserved.

Register Name	DDR Data Bus Timing Parameters Register
Mnemonic	MC01.PORT3.SRQ.MBA_TMR0Q
Address	00000000070109CB (SCOM)
Description	DDR data bus timing parameters

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MBA_TMR0Q_RRDM_DLY: Read to Read to different master.
4:7	RW	MBA_TMR0Q_RRSMSR_DLY: Read to Read same master, same rank.
8:11	RW	MBA_TMR0Q_RRSMDR_DLY: Read to Read same master, different rank.
12:15	RW	MBA_TMR0Q_RROP_DLY: Read open page to read delay.
16:19	RW	MBA_TMR0Q_WWDM_DLY: Write to Write different master.

Bits	SCOM	Field Mnemonic: Description
20:23	RW	MBA_TMR0Q_WWSMSR_DLY: Write to Write same master, same rank.
24:27	RW	MBA_TMR0Q_WWSMDR_DLY: Write to Write same master, different rank.
28:31	RW	MBA_TMR0Q_WWOP_DLY: Write open page to write delay.
32:36	RW	MBA_TMR0Q_RWDM_DLY: Read to Write different master.
37:41	RW	MBA_TMR0Q_RWSMSR_DLY: Read to Write same master, same rank.
42:46	RW	MBA_TMR0Q_RWSMDR_DLY: Read to Write same master, different rank.
47:50	RW	MBA_TMR0Q_WRDM_DLY: Write to Read different master.
51:56	RW	MBA_TMR0Q_WRSMSR_DLY: Write to Read same master, same rank.
57:62	RW	MBA_TMR0Q_WRSMDR_DLY: Write to Read same master, different rank.
63	RW	MBA_TMR0Q_RESERVED_63: Reserved.

Register Name	DDR Bank Busy Parameters Register
Mnemonic	MC01.PORT3.SRQ.MBA_TMR1Q
Address	00000000070109CC (SCOM)
Description	DDR bank busy parameters

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MBA_TMR1Q_RRSBG_DLY: Read to Read same bank group.
4:9	RW	MBA_TMR1Q_WRSBG_DLY: Write to Read same bank group.
10:15	RW	MBA_TMR1Q_CFG_TFAW: Four activate window time.
16:20	RW	MBA_TMR1Q_CFG_TRCD: RAS to CAS delay.
21:25	RW	MBA_TMR1Q_CFG_TRP: Precharge to activate delay.
26:31	RW	MBA_TMR1Q_CFG_TRAS: Activate to precharge delay.
32:40	RW	MBA_TMR1Q_RESERVED_32_40: Reserved.
41:47	RW	MBA_TMR1Q_CFG_WR2PRE: Write to precharge delay.
48:51	RW	MBA_TMR1Q_CFG_RD2PRE: Read to precharge delay.
52:55	RW	MBA_TMR1Q_TRRD: Activate to activate delay.
56:59	RW	MBA_TMR1Q_TRRD_SBG: Activate to activate, same bank, group delay.
60:63	RW	MBA_TMR1Q_CFG_ACT_TO_DIFF_RANK_DLY: Activate to activate, different rank, delay.

Register Name	DDR Write Command Parameters Register
Mnemonic	MC01.PORT3.SRQ.MBA_WRQ0Q
Address	00000000070109CD (SCOM)
Description	DDR write command parameters

Bits	SCOM	Field Mnemonic: Description
0:4	RW	MBA_WRQ0Q_CFG_WRITE_HW_MARK: Write high-water mark (force writes HPenables writes).
5	RW	MBA_WRQ0Q_CFG_WRQ_FIFO_MODE: Prevent reordering in the WRQ (only entry0 can be selected). HP Cleaner writes will not get selected until they are in entry 0.

Bits	SCOM	Field Mnemonic: Description
6	RW	MBA_WRQ0Q_CFG_DISABLE_WR_PG_MODE: Disable page commands for the WRQ.
7:18	RW	MBA_WRQ0Q_CFG_WRQ_ENTRY0_HP_DLY: Time for entry0 of the WRQ before it forces HP. Setting this dial to a 0 will disable entry0 HP.
19	RW	MBA_WRQ0Q_CFG_WRQ_FLUSH_WR_RANK: When one write is issued to a rank, try to force more writes to that rank to avoid multiple write-to-read same rank penalties.
20	RW	MBA_WRQ0Q_CFG_WRQ_ENABLE_NON_HP_WR: Allow writes when they do not meet a condition such as entry0_flush or rd_idle_allow_wr.
21:32	RW	MBA_WRQ0Q_CFG_ENTRY0_MIN_FOR_RRQ_IDLE_WR: This is an added condition to allow writes when the RRQ is idle. This addition allows for multiple writes to stack up in the WRQ before starting the write burst.
33:37	RW	MBA_WRQ0Q_CFG_WRITE_LW_MARK: Write low-water mark. After write high priority has been asserted due to the writes exceeding the programmed high-water mark, write priority will remain asserted until the write low-water mark is reached. If set to 8 and there are more then eight entries in the WRQ, the condition will allow writes when the rrq_idle period is met.
38:43	RW	MBA_WRQ0Q_CFG_WRQ_SKIP_LIMIT: The number of times entry0 of the WRQ can be skipped before entry0 prevents older writes from being issued until entry0 is sent.
44	RW	MBA_WRQ0Q_CFG_WRQ_SINGLE_THREAD_MODE: WRQ wrq_single thread mode setting. This ensures that all reads are issued one at a time. With this mode set, we will only issue from the bottom entry in the WRQ, and we will not issue an activate for the subsequent operation until the prior write is sent.
45:52	RW	MBA_WRQ0Q_CFG_RQ_HANG_THRESHOLD: Hang detection for entry0 of the reorder queue. A counter increments every mcbist_srq_hang_pulse (2048 phase hold cycles), and will set a FIR when the count equals the threshold and another pulse is received. Since this checks for count = threshold, a value of 0 is not valid.
53:54	RW	MBA_WRQ0Q_RESERVED_53_54: Reserved.
55:58	RW	MBA_WRQ0Q_CFG_WRQ_ACT_NUM_WRITES_PENDING: Limit on the number of write-activates when doing writes. When the sequencer is serving writes, no new activates will be sent out as long as at least this number of writes are pending to already activated pages. A setting of 0 sets no cap on the number of activates.
59:63	RW	MBA_WRQ0Q_RESERVED_59_63: Reserved.

Register Name	DDR Read Command Parameters Register
Mnemonic	MC01.PORT3.SRQ.MBA_RRQ0Q
Address	00000000070109CE (SCOM)
Description	DDR read command parameters

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MBA_RRQ0Q_CFG_RRQ_SKIP_LIMIT: Number of times the bottom entry in the RRQ can be skipped before preventing the entry from being skipped.
6	RW	MBA_RRQ0Q_CFG_RRQ_FIFO_MODE: RRQ FIFO mode Setting this ensures that all reads go out in the order they were received. It still allows multiple operations to be pipelined to allow for decent throughput. This needs to be set for MCBIST DGEN mode.
7	RW	MBA_RRQ0Q_CFG_RRQ_SINGLE_THREAD_MODE: RRQ single thread mode. Setting this ensures that all reads are issued one at a time. With this mode set, we will only issue from the bottom entry in the RRQ, and we will not issue an activate for the subsequent operation until the prior read is sent.
8:10	RW	MBA_RRQ0Q_RESERVED_8_10: Reserved.
11	RW	MBA_RRQ0Q_CFG_DISABLE_RD_PG_MODE: Disable page commands for the RRQ.
12	RW	MBA_RRQ0Q_CFG_DISABLE_FAST_PATH: Disable MBA RRQ fastpath.
13:23	RW	MBA_RRQ0Q_CFG_RD_IDLE_ALLOW_WR: Time with an empty RRQ before writes will be enabled.

Bits	SCOM	Field Mnemonic: Description
24:29	RW	MBA_RRQ0Q_CFG_RDBUFF_CAPACITY_LIMIT: Number of 64-byte read buffers that the sequencer is allowed to use concurrently.
30:36	RW	MBA_RRQ0Q_CFG_RMWBUFF_CAPACITY_LIMIT: Number of 64-byte read-modify-write buffers that the sequencer is allowed to use concurrently.
37:56	RW	MBA_RRQ0Q_RESERVED_37_56: Reserved.
57:60	RW	MBA_RRQ0Q_CFG_RRQ_ACT_NUM_READS_PENDING: Limit on the number of read-activates when doing reads. When the sequencer is serving reads, no new activates will be sent out as long as at least this number of reads are pending to already activated pages. A setting of 0 sets no cap on the number of activates.
61	RW	MBA_RRQ0Q_CFG_INJ_CANCEL_ACK_ERR: Inject error on cancel-ack asynchronous interface.
62	RW	MBA_RRQ0Q_CFG_RRQ_ENTRY0_ENABLE: Enable entry0 timer for RRQ.
63	RW	MBA_RRQ0Q_RESERVED_63: Reserved.

Register Name	DDR Calibration Registers
Mnemonic	MC01.PORT3.SRQ.MBA_CAL0Q
Address	00000000070109CF (SCOM)
Description	DDR calibration registers

Bits	SCOM	Field Mnemonic: Description
0	RW	MBA_CAL0Q_CFG_CAL_INTERVAL_TMR0_ENABLE: Enable interval tmr0.
1:2	RW	MBA_CAL0Q_CFG_TIME_BASE_TMR0: Time base for interval tmr0 counter.
3:11	RW	MBA_CAL0Q_CFG_INTERVAL_COUNTER_TMR0: Interval timer based on time_base (time_base × interval_counter).
12	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL1_ENABLE: Enable bit for the first calibration to perform when the timer pops. Should always be 1 if the timer is enabled.
13:16	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL1_TYPE: 10XX = Internal ZQ calibration (cal_rank ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step. 0011 = Periodic calibration: Run SysClk, DQS, and read eye all in parallel (default behavior).
17	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL1_DDR_DONE: Use the complete signal from the DDR for cal1.
18	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL2_ENABLE: Enable bit for the second calibration to perform when the timer pops.
19:22	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL2_TYPE: 10XX = Internal ZQ calibration (cal_rank ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step. 0011 = Periodic calibration: Run SysClk, DQS, and read eye all in parallel (default behavior).
23	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL2_DDR_DONE: Use the complete signal from the DDR for cal2.
24	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL3_ENABLE: Enable bit for the third calibration to perform when the timer pops.

Bits	SCOM	Field Mnemonic: Description
25:28	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL3_TYPE: 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step. 0011 = Periodic calibration: Run SysClk, DQS, and read eye all in parallel (default behavior).
29	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL3_DDR_DONE: Use the complete signal from the DDR for cal3.
30:38	RW	MBA_CAL0Q_CFG_CAL_TMR0_Z_SYNC: The timer value will be set to this value during z sync.
39:46	RW	MBA_CAL0Q_CFG_CAL_TMR0_DDR_RESET_TMR: Wait time for the DDR soft reset upon calibration timeout fail.
47:48	RW	MBA_CAL0Q_CFG_CAL_TMR0_DDR_RESET_TMR_TB: Timebase interval for ddr_reset_tmr.
49	RW	MBA_CAL0Q_CFG_CAL_TMR0_DDR_RESET_ENABLE: Enable a DDR soft reset upon calibration timeout fail. 0 = Do not issue a soft DDR reset upon calibration timeout. 1 = Issue a DDR soft reset upon calibration timeout.
50	RW	MBA_CAL0Q_CFG_CAL_TMR0_SINGLE_RANK: Enable single-rank mode for timer0 calibrations. Calibrations programmed in tmr0 will run on one rank at a time per timer expiration. 0 = Issue calibrations for all enabled ranks per timer expiration. 1 = Issue calibrations for one rank at a time per timer expiration.
51	RW	MBA_CAL0Q_RESERVED_51: Reserved.
52	RW	MBA_CAL0Q_INJECT_1HOT_SM_ERROR: Setting to 1 will inject one 1hot sm error. must be set to 0 and then 1 again to inject another error. 0 = No error inject. 1 = Inject one 1hot sm error.
53:55	RW	MBA_CAL0Q_CFG_CAL_SINGLE_PORT_MODE: Single port mode configuration. The default is both ports are calibrated at the same time. Options are: • Single port calibrated at a time with both ports powered up. • Single port calibrated at a time with one port powered up. • Single port calibrated at a time with one port powered up and only the rank requested by the DDR PHY powered up. Only to be used in single rank mode.
56	RW	MBA_CAL0Q_DBG_BUS_BIT: Debug bus bit.
57	RW	MBA_CAL0Q_RESET_RECOVER: DDR reset recover.
58	RW	MBA_CAL0Q_CFG_RANK_SM_STALL_DISABLE: When enabled, require a minimum 1K cycle stall between all new calibration timer starts.
59	RW	MBA_CAL0Q_CFG_ENABLE_SPEC_ATTN: Allow FIR attention to cause spec attn.
60	RW	MBA_CAL0Q_CFG_ENABLE_HOST_ATTN: Allow FIR attention to cause host attn.
61:63	RW	MBA_CAL0Q_RESERVED_61_63: Reserved.

Register Name	DDR Calibration Registers
Mnemonic	MC01.PORT3.SRQ.MBA_CAL1Q
Address	00000000070109D0 (SCOM)
Description	DDR calibration registers

Bits	SCOM	Field Mnemonic: Description
0	RW	MBA_CAL1Q_CFG_CAL_INTERVAL_TMR1_ENABLE: Enable interval tmr1.

Bits	SCOM	Field Mnemonic: Description
1:2	RW	MBA_CAL1Q_CFG_TIME_BASE_TMR1: Time base for the interval tmr1 counter.
3:11	RW	MBA_CAL1Q_CFG_INTERVAL_COUNTER_TMR1: Interval timer based on time_base (time_base × interval_counter).
12	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL1_ENABLE: Enable bit for the first calibration to perform when the timer pops. Should always be 1 if the timer is enabled.
13:16	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL1_TYPE: 10XX = Internal ZQ calibration (cal_rank ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step. 0011 = Periodic calibration: Run SysClk, DQS, and read eye all in parallel (default behavior).
17	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL1_DDR_DONE: Use the complete signal from the DDR for cal1.
18	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL2_ENABLE: Enable bit for the second calibration to perform when the timer pops.
19:22	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL2_TYPE: 10XX = Internal ZQ calibration (cal_rank ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step. 0011 = Periodic calibration: Run SysClk, DQS, and read eye all in parallel (default behavior).
23	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL2_DDR_DONE: Use the complete signal from the DDR for cal2.
24	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL3_ENABLE: Enable bit for the third calibration to perform when the timer pops.
25:28	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL3_TYPE: 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step. 0011 = Periodic calibration: Run SysClk, DQS, and read eye all in parallel (default behavior).
29	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL3_DDR_DONE: Use the complete signal from the DDR for cal3.
30:38	RW	MBA_CAL1Q_CFG_CAL_TMR1_Z_SYNC: The timer value will be set to this value during z sync.
39	RW	MBA_CAL1Q_CFG_CAL_TMR1_SINGLE_RANK: Enable single-rank mode for timer1 calibrations. Calibrations programmed in tmr1 will run on one rank at a time per timer expiration. 0 = Issue calibrations for all enabled ranks per timer expiration. 1 = Issue calibrations for one rank at a time per timer expiration.
40:47	RW	MBA_CAL1Q_CFG_CAL_RANK_ENABLE: Cal rank enable.
48:63	RW	MBA_CAL1Q_RESERVED_48_63: Reserved.

Register Name	DDR Calibration Registers
Mnemonic	MC01.PORT3.SRQ.MBA_CAL2Q
Address	00000000070109D1 (SCOM)
Description	DDR calibration registers

Bits	SCOM	Field Mnemonic: Description
0	RW	MBA_CAL2Q_CFG_CAL_INTERVAL_TMR2_ENABLE: Enable interval tmr2.

Bits	SCOM	Field Mnemonic: Description
1:2	RW	MBA_CAL2Q_CFG_TIME_BASE_TMR2: Time base for the interval tmr2 counter.
3:11	RW	MBA_CAL2Q_CFG_INTERVAL_COUNTER_TMR2: Interval timer based on time_base (time_base × interval_counter).
12	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL1_ENABLE: Enable bit for the first calibration to perform when the timer pops. Should always be 1 if the timer is enabled.
13:16	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL1_TYPE: 10XX = Internal ZQ calibration (cal_rank ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step. 0011 = Periodic calibration: Run SysClk, DQS, and read eye all in parallel (default behavior).
17	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL1_DDR_DONE: Use the complete signal from the DDR for cal1.
18	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL2_ENABLE: Enable bit for the second calibration to perform when the timer pops.
19:22	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL2_TYPE: 10XX = Internal ZQ calibration (cal_rank ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step. 0011 = Periodic calibration: Run SysClk, DQS, and read eye all in parallel (default behavior).
23	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL2_DDR_DONE: Use the complete signal from the DDR for cal2.
24	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL3_ENABLE: Enable bit for the third calibration to perform when the timer pops.
25:28	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL3_TYPE: 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step. 0011 = Periodic calibration: Run SysClk, DQS, and read eye all in parallel (default behavior).
29	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL3_DDR_DONE: Use the complete signal from the DDR for cal3.
30:38	RW	MBA_CAL2Q_CFG_CAL_TMR2_Z_SYNC: The timer value will be set to this value during z sync.
39	RW	MBA_CAL2Q_CFG_CAL_TMR2_SINGLE_RANK: Enable single-rank mode for timer2 calibrations. Calibrations programmed in tmr2 will run on one rank at a time per timer expiration. 0 = Issue calibrations for all enabled ranks per timer expiration. 1 = Issue calibrations for one rank at a time per timer expiration.
40	RW	MBA_CAL2Q_CFG_CAL_TMR2_WAT_EVENT_ENABLE: Enable the use of tmr2 to trigger a WAT event. No other calibrations should be enabled. Must be used with the HW221617 CKSW enabled.
41:63	RW	MBA_CAL2Q_RESERVED_41_63: Reserved.

Register Name	DDR Calibration Length Registers
Mnemonic	MC01.PORT3.SRQ.MBA_CAL3Q
Address	00000000070109D2 (SCOM)
Description	DDR calibration length registers

Bits	SCOM	Field Mnemonic: Description
0:1	RW	MBA_CAL3Q_CFG_INTERNAL_ZQ_TB: Internal ZQ time base Time base for the internal ZQ cal counter.

Bits	SCOM	Field Mnemonic: Description
2:9	RW	MBA_CAL3Q_CFG_INTERNAL_ZQ_LENGTH: Number of internal ZQ time bases required to meet the maximum internal ZQ length.
10:11	RW	MBA_CAL3Q_CFG_EXTERNAL_ZQ_TB: External ZQ time base. Time base for the external ZQ cal counter.
12:19	RW	MBA_CAL3Q_CFG_EXTERNAL_ZQ_LENGTH: Number of external ZQ time bases required to meet the maximum external ZQ length.
20:21	RW	MBA_CAL3Q_CFG_RDCLK_SYSCLK_TB: ReadclkSysclk time base. Time base for the readclksysclk cal counter.
22:29	RW	MBA_CAL3Q_CFG_RDCLK_SYSCLK_LENGTH: Number of Readclksysclk time bases required to meet the maximum rdclk length.
30:31	RW	MBA_CAL3Q_CFG_DQS_ALIGNMENT_TB: DQS alignment time base. Time base for the DQS alignment cal counter.
32:39	RW	MBA_CAL3Q_CFG_DQS_ALIGNMENT_LENGTH: Number of DQS alignment time bases required to meet the maximum DQS alignment length.
40:41	RW	MBA_CAL3Q_CFG_MPR_READEYE_TB: Readeye time base. Time base for the readeye cal counter.
42:49	RW	MBA_CAL3Q_CFG_MPR_READEYE_LENGTH: Number of readeye time bases required to meet the maximum external ZQ length.
50:51	RW	MBA_CAL3Q_CFG_ALL_PERIODIC_TB: All periodics time base. Time base for the all periodic cal counter.
52:59	RW	MBA_CAL3Q_CFG_ALL_PERIODIC_LENGTH: Number of all_periodic time bases required to meet the maximum calibration length for all periodic calibration (in parallel).
60	RW	MBA_CAL3Q_CFG_FREEZE_ON_PARITY_ERROR_DIS: Disable freezing MBA execution when a parity error is detected.
61:63	RW	MBA_CAL3Q_RESERVED_61_63: Reserved.

Register Name	Final ARB Parameters Register
Mnemonic	MC01.PORT3.SRQ.MBA_FARB0Q
Address	00000000070109D3 (SCOM)
Description	Final ARB parameters

Bits	SCOM	Field Mnemonic: Description
0:15	RW	MBA_FARB0Q_CFG_MISR_BLOCK: When a bit is set, an area of logic is not included in the z-sync MISR computation. Each bit independently gates (blocks) that area of logic from the MISR. b0 = Gate refresh pulse. b1 - 3 = Gate cal timers 0 - 2. b4 = Gate nm pulse. b5 - 8 = Gate MCBIST tb pulses. b9 - b15 = Gate FARB requests.
16	RW	MBA_FARB0Q_CFG_MISR_FEEDBACK_ENABLE: Allow the z-sync MISR to use circular feedback and retain the state beyond its 10-latch pipe.
17	RW	MBA_FARB0Q_CFG_2N_ADDR: Enable 2N/2T address mode.
18:19	RW	MBA_FARB0Q_RESERVED_18_19: Reserved.
20:23	RW	MBA_FARB0Q_CFG_ACT_SAME_RANK_HOLD_TIME: Time after activate to prefer subsequent activates to the same rank.

Bits	SCOM	Field Mnemonic: Description
24:30	RW	MBA_FARB0Q_CFG_MAX_READS_IN_A_ROW: Limits the maximum number of reads in a row, before forcing a write. There must be a write in the WRQ for the counting to start. 0x00 = Disabled 0x01 = 1 read before allowing a write ... 0x7F = 127 reads before forcing a write
31:37	RW	MBA_FARB0Q_CFG_MAX_WRITES_IN_A_ROW: Limits the maximum number of writes in a row before forcing a read. There must be a read in the RRQ for the counting to start. 0x00 = Disabled 0x01 = 1 write before allowing a read ... 0x7F = 127 write before forcing a read
38	RW	MBA_FARB0Q_CFG_PARITY_AFTER_CMD: Determines whether OE is driven on the parity cycle. 0 = OE will not be driven on the parity cycle. 1 = OE will be driven on the parity cycle.
39	RWX	MBA_FARB0Q_CFG_INJECT_PARITY_ERR_WEN: Inject a parity error on WEN on the next CAS.
40	RWX	MBA_FARB0Q_CFG_INJECT_PARITY_ERR_ADDR5: Inject a parity error on ADDR5 on the next CAS.
41:42	RWX	MBA_FARB0Q_CFG_BW_WINDOW_SIZE: For optional size reads: 00 = Determine the BW over a 1K cycle window. 01 = Determine the BW over a 2K cycle window. 10 = Determine the BW over a 4K cycle window. 11 = Determine the BW over a 8K cycle window.
43:47	RW	MBA_FARB0Q_CFG_PARITY_DETECT_TIME: Measures the time from an injected error until when the error is detected back at the MBA.
48:53	RW	MBA_FARB0Q_CFG_RCD_PROTECTION_TIME: Time interval in which commands were sent out before an RCD parity error occurrence that should be re-issued. Should be set ≥ to cfg_parity_detect_time.
54	RW	MBA_FARB0Q_CFG_DISABLE_RCD_RECOVERY: Disable the RCD recovery procedure.
55	RW	MBA_FARB0Q_CFG_OE_ALWAYS_ON: Force DDR OE to always be on (never tristate the DDR address drivers).
56	RW	MBA_FARB0Q_CFG_FARB_CLOSE_ALL_PAGES: Before switching direction on the DRAM bus, require all committed accesses to be issued to any open pages. When set, no new activates can be issued for reads until all writes to open pages are sent. No new activates can be issued for writes until all reads to open pages are issued.
57	RW	MBA_FARB0Q_CFG_PORT_FAIL_DISABLE: Disable Port Fail after recurring RCD errors.
58	RW	MBA_FARB0Q_CFG_OE_ALL_CKE_POWERED_DOWN: Only precisely turn off cmd-addr output enable after all CKEs are powered down.
59	RW	MBA_FARB0Q_CFG_INJECT_PARITY_ERR_CONSTANT: If set, parity errors are injected continuously; otherwise, parity errors are injected only once.
60	RW	MBA_FARB0Q_CFG_FINISH_WR_BEFORE_RD: This is to prevent writes from holding up banks for a long period of time. If set, all committed writes must be issued before reads can proceed.
61:63	RW	MBA_FARB0Q_CFG_OPT_RD_SIZE: For optional size reads: 000 = Treat all 64-byte/128-byte-opt reads as 64-byte reads. 001 = Treat all 64-byte/128-byte-opt reads as 128-byte reads. 010 = If DRAM data bus utilization is greater than 50%, do optional-size reads as 64 bytes. 011 = If DRAM data bus utilization is greater than 62.5%, do optional-size reads as 64 bytes. 100 = If DRAM data bus utilization is greater than 75.0%, do optional-size reads as 64 bytes. 101 = If DRAM data bus utilization is greater than 87.5%, do optional-size reads as 64 bytes. 11X = Reserved.

Register Name	Final ARB Parameters Register
Mnemonic	MC01.PORT3.SRQ.MBA_FARB1Q
Address	00000000070109D4 (SCOM)
Description	Final ARB parameters

Bits	SCOM	Field Mnemonic: Description
0:2	RW	MBA_FARB1Q_CFG_SLOT0_S0_CID: Chip ID bits for Slot 0, Master 0/1, Slave 0.
3:5	RW	MBA_FARB1Q_CFG_SLOT0_S1_CID: Chip ID bits for Slot 0, Master 0/1, Slave 1.
6:8	RW	MBA_FARB1Q_CFG_SLOT0_S2_CID: Chip ID bits for Slot 0, Master 0/1, Slave 2.
9:11	RW	MBA_FARB1Q_CFG_SLOT0_S3_CID: Chip ID bits for Slot 0, Master 0/1, Slave 3.
12:14	RW	MBA_FARB1Q_CFG_SLOT0_S4_CID: Chip ID bits for Slot 0, Master 0/1, Slave 4 or Chip ID bits for Slot 0, Master 2/3, Slave 0.
15:17	RW	MBA_FARB1Q_CFG_SLOT0_S5_CID: Chip ID bits for Slot 0, Master 0/1, Slave 5 or Chip ID bits for Slot 0, Master 2/3, Slave 1.
18:20	RW	MBA_FARB1Q_CFG_SLOT0_S6_CID: Chip ID bits for Slot 0, Master 0/1, Slave 6 or Chip ID bits for Slot 0, Master 2/3, Slave 2.
21:23	RW	MBA_FARB1Q_CFG_SLOT0_S7_CID: Chip ID bits for Slot 0, Master 0/1, Slave 7 or Chip ID bits for Slot 0, Master 2/3, Slave 3.
24:26	RW	MBA_FARB1Q_CFG_SLOT1_S0_CID: Chip ID bits for Slot 1, Master 0/1, Slave 0.
27:29	RW	MBA_FARB1Q_CFG_SLOT1_S1_CID: Chip ID bits for Slot 1, Master 0/1, Slave 1.
30:32	RW	MBA_FARB1Q_CFG_SLOT1_S2_CID: Chip ID bits for Slot 1, Master 0/1, Slave 2.
33:35	RW	MBA_FARB1Q_CFG_SLOT1_S3_CID: Chip ID bits for Slot 1, Master 0/1, Slave 3.
36:38	RW	MBA_FARB1Q_CFG_SLOT1_S4_CID: Chip ID bits for Slot 1, Master 0/1, Slave 4 or Chip ID bits for Slot 1, Master 2/3, Slave 0.
39:41	RW	MBA_FARB1Q_CFG_SLOT1_S5_CID: Chip ID bits for Slot 1, Master 0/1, Slave 5 or Chip ID bits for Slot 1, Master 2/3, Slave 1.
42:44	RW	MBA_FARB1Q_CFG_SLOT1_S6_CID: Chip ID bits for Slot 1, Master 0/1, Slave 6 or Chip ID bits for Slot 1, Master 2/3, Slave 2.
45:47	RW	MBA_FARB1Q_CFG_SLOT1_S7_CID: Chip ID bits for Slot 1, Master 0/1, Slave 7 or Chip ID bits for Slot 1, Master 2/3, Slave 3.
48	RW	MBA_FARB1Q_CFG_DIS_SMDR: Set to 1 if using a 5D configuration. This uses the different master parameters instead of the SMDR.
49	RW	MBA_FARB1Q_CFG_DDR4_PARITY_ON_CID_DIS: Exclude CID bits in parity generation for DDR4.
50:63	RW	MBA_FARB1Q_CFG_RSV0: Reserved.

Register Name	Final ARB Parameters Register
Mnemonic	MC01.PORT3.SRQ.MBA_FARB2Q
Address	00000000070109D5 (SCOM)
Description	Final ARB parameters

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MBA_FARB2Q_CFG_RANK0_RD_ODT: ODT bits required for a read Master Rank 0.
4:7	RW	MBA_FARB2Q_CFG_RANK1_RD_ODT: ODT bits required for a read Master Rank 1.

Bits	SCOM	Field Mnemonic: Description
8:11	RW	MBA_FARB2Q_CFG_RANK2_RD_ODT: ODT bits required for a read Master Rank 2.
12:15	RW	MBA_FARB2Q_CFG_RANK3_RD_ODT: ODT bits required for a read Master Rank 3.
16:19	RW	MBA_FARB2Q_CFG_RANK4_RD_ODT: ODT bits required for a read Master Rank 4.
20:23	RW	MBA_FARB2Q_CFG_RANK5_RD_ODT: ODT bits required for a read Master Rank 5.
24:27	RW	MBA_FARB2Q_CFG_RANK6_RD_ODT: ODT bits required for a read Master Rank 6.
28:31	RW	MBA_FARB2Q_CFG_RANK7_RD_ODT: ODT bits required for a read Master Rank 7.
32:35	RW	MBA_FARB2Q_CFG_RANK0_WR_ODT: ODT bits required for a write Master Rank 0.
36:39	RW	MBA_FARB2Q_CFG_RANK1_WR_ODT: ODT bits required for a write Master Rank 1.
40:43	RW	MBA_FARB2Q_CFG_RANK2_WR_ODT: ODT bits required for a write Master Rank 2.
44:47	RW	MBA_FARB2Q_CFG_RANK3_WR_ODT: ODT bits required for a write Master Rank 3.
48:51	RW	MBA_FARB2Q_CFG_RANK4_WR_ODT: ODT bits 4equired for a write Master Rank 4.
52:55	RW	MBA_FARB2Q_CFG_RANK5_WR_ODT: ODT bits required for a write Master Rank 5.
56:59	RW	MBA_FARB2Q_CFG_RANK6_WR_ODT: ODT bits required for a write Master Rank 6.
60:63	RW	MBA_FARB2Q_CFG_RANK7_WR_ODT: ODT bits required for a write Master Rank 7.

Register Name	**N/M Throttling Control Register**
Mnemonic	MC01.PORT3.SRQ.MBA_FARB3Q
Address	00000000070109D6 (SCOM)
Description	N/M throttling control

Bits	SCOM	Field Mnemonic: Description
0:14	RW	MBA_FARB3Q_CFG_NM_N_PER_SLOT: The N value for the NM throttling across a single slot. The maximum command count that can occur over a time interval M for one slot.
15:30	RW	MBA_FARB3Q_CFG_NM_N_PER_PORT: The N value for the NM throttling across the entire port (both slots). The maximum command count that can occur over a time interval M for the entire port.
31:44	RW	MBA_FARB3Q_CFG_NM_M: The M value for the NM throttling. This counts DRAM clock cycles. Set this to 0 to disable NM throttling.
45:47	RW	MBA_FARB3Q_CFG_NM_RAS_WEIGHT: The increment to be added to the N count each time a RAS is sent.
48:50	RW	MBA_FARB3Q_CFG_NM_CAS_WEIGHT: The increment to be added to the N count each time a CAS is sent.
51	RW	MBA_FARB3Q_RESERVED_51: Reserved.
52	RW	MBA_FARB3Q_RESERVED_52: Reserved.
53	RW	MBA_FARB3Q_CFG_NM_CHANGE_AFTER_SYNC: If set, changes to cfg_nm_n_per_slot, cfg_nm_n_per_port, cfg_nm_m, and min_max_domains will only be applied after a pc_sync command is seen.
54:63	RW	MBA_FARB3Q_RESERVED_54_63: Reserved.

Register Name	Final Command Arbiter Miscellaneous Register
Mnemonic	MC01.PORT3.SRQ.MBA_FARB4Q
Address	00000000070109D7 (SCOM)
Description	Final command arbiter miscellaneous

Bits	SCOM	Field Mnemonic: Description
0:15	RW	MBA_FARB4Q_CFG_NOISE_WAIT_TIME: The time from RCD_err until the RCD error recovery procedure will start issuing precharge commands.
16:21	RW	MBA_FARB4Q_CFG_PRECHARGE_WAIT_TIME: The time from one precharge command to the next precharge command in the RCD error recovery procedure.
22	RW	MBA_FARB4Q_CFG_SIM_FAST_NOISE_WINDOW: This will skip the precharges and refreshes as part of the noise window and only observe the noise window wait time.
23:26	RW	MBA_FARB4Q_RESERVED_23_26: Reserved.
27:41	RW	MBA_FARB4Q_EMERGENCY_N: Programmable N for NM when the emergency throttle is enabled.
42:55	RW	MBA_FARB4Q_EMERGENCY_M: Programmable M for NM when the emergency throttle is enabled.
56:63	RW	MBA_FARB4Q_RESERVED_56_63: Reserved.

Register Name	DDR Interface SCOM Control Register
Mnemonic	MC01.PORT3.SRQ.MBA_FARB5Q
Address	00000000070109D8 (SCOM)
Description	DDR interface SCOM control

Bits	SCOM	Field Mnemonic: Description
0:1	RW	MBA_FARB5Q_CFG_DDR_DPHY_NCLK: DDR PHY NCLK control.
2:3	RW	MBA_FARB5Q_CFG_DDR_DPHY_PCLK: DDR PHY PCLK control.
4	RW	MBA_FARB5Q_CFG_DDR_RESETN: DDR Resetn signal.
5	RW	MBA_FARB5Q_CFG_CCS_ADDR_MUX_SEL: CCS address mux select. This bit should be turned on until all multiple CCS instructions are completed. 0 selects address data from the mainline logic. 1 selects address data from the CCS logic.
6	RW	MBA_FARB5Q_CFG_CCS_INST_RESET_ENABLE: When set to 1, bit 16 of the CCS_INST_ARR0 will be driven out to DDR Resetn. When set to 0, cfg_ddr_resetn will be driven out to DDR Resetn.
7	RW	MBA_FARB5Q_CFG_GP_BIT_3_ENABLE: When set to 1, the inverted value of GP(3) will be driven on the force_mclk_low signal to the DDR PHYs. When set to 0, the inverted value of cfg_force_mclk_low_n will be driven on the force_mclk_low signal to the DDR PHYs.
8	RW	MBA_FARB5Q_CFG_FORCE_MCLK_LOW_N: The inverted value of force_mclk_low_n will be driven on mba_ddr_force_mclk_low when cfg_gp_bit_3_enable is 0.
9:15	RW	MBA_FARB5Q_RESERVED_56_63: Reserved.

Register Name	DDR Port Status Register
Mnemonic	MC01.PORT3.SRQ.MBA_FARB6Q
Address	00000000070109D9 (SCOM)
Description	DDR port status register

Bits	SCOM	Field Mnemonic: Description
0:10	ROX	MBA_FARB6Q_CFG_BW_SNAPSHOT: DRAM data bus utilization over the last 4K DDR clock window. All 1s is 100 percent utilization.
11:14	ROX	MBA_FARB6Q_CFG_CKE_PUP_STATE: Indicates which of the 4 CKEs are on.
15	ROX	MBA_FARB6Q_CFG_STR_STATE: Indicates whether the DRAMS on this port are in STR.
16:20	ROX	MBA_FARB6Q_CFG_RRQ_DEPTH: RRQ Depth; Number of commands in the RRQ.
21:25	ROX	MBA_FARB6Q_CFG_WRQ_DEPTH: WRQ Depth; Number of commands in the WRQ.
26:30	ROX	MBA_FARB6Q_CFG_RCD_PARITY_DLY: Delay from the parity error to the error being seen back in the MBA. This value can then be placed back in the RCD protection time register.
31	ROX	MBA_FARB6Q_CFG_EVENTN: EventN monitor for the thermal event.

Register Name	MBA Error Report Register
Mnemonic	MC01.PORT3.SRQ.MBA_ERR_REPORTQ
Address	00000000070109DA (SCOM)
Description	MBA error report register

Bits	SCOM	Field Mnemonic: Description
0	ROX	MBA_ERR_REPORTQ_WRQ_HANG_ERR: WRQ hang error. MBACALFIR Bit 17.
1	ROX	MBA_ERR_REPORTQ_RRQ_HANG_ERR: RRQ hang error. MBACALFIR Bit 17.
2	ROX	MBA_ERR_REPORTQ_DSM_PE_ERR: Parity error in the DSM configuration registers. MBACALFIR Bit 1.
3	ROX	MBA_ERR_REPORTQ_TMR_PE_ERR: Parity error in the TMR configuration registers. MBACALFIR Bit 1.
4	ROX	MBA_ERR_REPORTQ_RRQ_PE_ERR: Parity error in the RRQ configuration registers. MBACALFIR Bit 0.
5	ROX	MBA_ERR_REPORTQ_WRQ_PE_ERR: Parity error in the WRQ configuration registers. MBACALFIR Bit 0.
6	ROX	MBA_ERR_REPORTQ_FARB_PE_ERR: Parity error in the FARB configuration registers. MBACALFIR Bit 1.
7	ROX	MBA_ERR_REPORTQ_PC_PE_ERR: Parity error in the PC configuration registers. MBACALFIR Bit 0.
8	ROX	MBA_ERR_REPORTQ_CAL0_PE_ERR: Parity error in the Cal0 configuration register. MBACALFIR Bit 0.
9	ROX	MBA_ERR_REPORTQ_CAL1_PE_ERR: Parity error in the Cal1 configuration register. MBACALFIR Bit 0.
10	ROX	MBA_ERR_REPORTQ_CAL2_PE_ERR: Parity error in the Cal2 configuration register. MBACALFIR Bit 0.
11	ROX	MBA_ERR_REPORTQ_CAL3_PE_ERR: Parity error in the Cal3 configuration register. MBACALFIR Bit 0.
12	ROX	MBA_ERR_REPORTQ_DDR_IF_SM_1HOT_ERR: DDR state machine one hot error. MBACALFIR Bit 18.
13	ROX	MBA_ERR_REPORTQ_CAL_SM_1HOT_ERR: Calibration state machine one hot error. MBACALFIR Bit 18.
14	ROX	MBA_ERR_REPORTQ_RANK_SM_1HOT_ERR: Rank state machine one hot error. MBACALFIR Bit 18.
15	ROX	MBA_ERR_REPORTQ_RESERVED_15: Reserved 15.
16	ROX	MBA_ERR_REPORTQ_PC_CAL_PCFSM_1HOT_ERR: Power Control state machine 1 hot error. MBACALFIR bit 18.
17	ROX	MBA_ERR_REPORTQ_FARB_CAL_RECVFSM_1HOT_ERR: Recovery state machine 1 hot error. MBACALFIR bit 18.
18:23	ROX	MBA_ERR_REPORTQ_RESERVED_18_23: Reserved.
24	ROX	MBA_ERR_REPORTQ_RCMD_ASYNC_IF_ERR: Sequence error on rcmd asynchronous crossing. Operations received out of order.
25	ROX	MBA_ERR_REPORTQ_PF_PROMOTE_ASYNC_IF_ERR: Sequence error on prefetch promote asynchronous crossing. Operations received out of order.

Bits	SCOM	Field Mnemonic: Description
26	ROX	MBA_ERR_REPORTQ_CANCEL_ACK_ASYNC_IF_ERR: Sequence error on cancel ACK asynchronous crossing. Operations received out of order.
27	ROX	MBA_ERR_REPORTQ_FARB_CMD_PE_HOLD_OUT: Parity error seen on a new command to be issued by the sequencer.
28	ROX	MBA_ERR_REPORTQ_DSM_CMD_PE_HOLD_OUT: Parity error seen on the command as it leaves the sequencer.
29:30	ROX	MBA_ERR_REPORTQ_RESERVED_29_30: Reserved.
31:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Emergency Throttle Register
Mnemonic	MC01.PORT3.SRQ.MBA_FARB7Q
Address	00000000070109E5 (SCOM)
Description	Emergency throttle register

Bits	SCOM	Field Mnemonic: Description
0	RW	MBA_FARB7Q_EMER_THROTTLE_IP: Emergency throttle in-progress. This register can also be set to manually engage emergency throttle, or cleared to clear emergency throttle.

Register Name	MBA Debug Bus Register 0
Mnemonic	MC01.PORT3.SRQ.MBA_DBG0Q
Address	00000000070109E6 (SCOM)
Description	MBA Debug Bus Register 0

Bits	SCOM	Field Mnemonic: Description
0	RW	MBA_DBG0Q_CFG_DBG_SRQ_ENABLE:
1:3	RW	MBA_DBG0Q_CFG_DBG_SRQ_SEL0:
4:6	RW	MBA_DBG0Q_CFG_DBG_SRQ_SEL1:
7:9	RW	MBA_DBG0Q_CFG_DBG_SRQ_SEL2:
10:12	RW	MBA_DBG0Q_CFG_DBG_SRQ_SEL3:
13:15	RW	MBA_DBG0Q_CFG_DBG_SRQ_SEL4:
16:18	RW	MBA_DBG0Q_CFG_DBG_SRQ_SEL5:
19:21	RW	MBA_DBG0Q_CFG_DBG_SRQ_SEL6:
22:24	RW	MBA_DBG0Q_CFG_DBG_SRQ_SEL7:
25:33	RW	MBA_DBG0Q_RESERVED_25_33:
34:41	RW	MBA_DBG0Q_CFG_DBG_SRQ_SEL_OTHER_SRQ:
42:47	RW	MBA_DBG0Q_RESERVED_42_47:
48:51	RW	MBA_DBG0Q_CFG_WAT_FARB_RRQ_GT:
52:55	RW	MBA_DBG0Q_CFG_WAT_FARB_WRQ_GT:
56:59	RW	MBA_DBG0Q_CFG_WAT_FARB_REF_GT:
60:63	RW	MBA_DBG0Q_CFG_WAT_FARB_CAL_GT:

Register Name	MBA Debug Bus Register 1
Mnemonic	MC01.PORT3.SRQ.MBA_DBG1Q
Address	00000000070109E7 (SCOM)
Description	MBA debug bus register 1

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MBA_DBG1Q_CFG_WAT_FORCE_WR_ENTRY0_HP:
4:7	RW	MBA_DBG1Q_CFG_WAT_FORCE_RD_ENTRY0_HP:
8:11	RW	MBA_DBG1Q_CFG_WAT_FP_DIS:
12:15	RW	MBA_DBG1Q_CFG_WAT_DIS_RD_PG:
16:19	RW	MBA_DBG1Q_CFG_WAT_DIS_WR_PG:
20:23	RW	MBA_DBG1Q_CFG_WAT_PUP_ALL:
24:27	RW	MBA_DBG1Q_CFG_WAT_EXIT_STR:
28:31	RW	MBA_DBG1Q_CFG_WAT_REF_HP:
32:35	RW	MBA_DBG1Q_CFG_WAT_REF_SYNC:
36:39	RW	MBA_DBG1Q_CFG_WAT_REF_SAFE:
40:43	RW	MBA_DBG1Q_CFG_WAT_CAL_SYNC:
44:47	RW	MBA_DBG1Q_CFG_WAT_RRQ_MNT_GT:
48:51	RW	MBA_DBG1Q_CFG_WAT_WRQ_MNT_GT:
52:55	RW	MBA_DBG1Q_CFG_WAT_SET_FIR:
56:59	RW	MBA_DBG1Q_CFG_WAT_EMER_TH:
60:63	RW	MBA_DBG1Q_CFG_WAT_START_RECOVERY:

Register Name	Emergency Throttle Register
Mnemonic	MC01.PORT3.SRQ.MBA_FARB8Q
Address	00000000070109E8 (SCOM)
Description	Emergency throttle register

Bits	SCOM	Field Mnemonic: Description
0	RW	MBA_FARB8Q_SAFE_REFRESH_MODE: Safe refresh interval is being used for tREFI. This register can also be set to manually engage safe refresh or cleared to clear safe refresh.

Register Name	Timer State Machine Control Register
Mnemonic	MC01.PORT3.SRQ.MBA_TMR2Q
Address	00000000070109EF (SCOM)
Description	Timer state machine control

Bits	SCOM	Field Mnemonic: Description
0:19	RW	MBA_TMR2Q_CFG_BANK_BUSY_FSM_DIS: Disable bank busy state machines 0 - 19, one bit per FSM.

Bits	SCOM	Field Mnemonic: Description
20:31	RW	MBA_TMR2Q_CFG_BANK_BUSY_OPEN_PAGE_DIS: Disable open page mode on bank busy state machines 0 - 11, one bit per FSM. Bank busy state machines 12 - 19 do not do open page mode.
32:63	RW	MBA_TMR2Q_RESERVED_32_63: Reserved.

Register Name	Refresh Register 0
Mnemonic	MC01.PORT3.SRQ.PC.MBAREF0Q
Address	00000000070109F2 (SCOM)
Description	Refresh register 0

Bits	SCOM	Field Mnemonic: Description
0	RW	MBAREF0Q_CFG_REFRESH_ENABLE: Refresh enable.
1:2	RW	MBAREF0Q_CFG_REFRESH_INTERVAL_TIMEBASE_SELECT: 01 = Reserved. For 10 and 11 settings, to determine the actual refresh interval, you must multiply the calculated refresh interval by 8k or 2^{22} depending on which timebase was used. **Note**: Settings 10 and 11 are for characterization stress testing only.
3	RW	MBAREF0Q_CFG_PER_BANK_REFRESH: Banks are individually refreshed each time a new refresh to a rank pops. The refresh must be sent to each bank separately before that refresh is considered complete. DDR4E only.
4	RW	MBAREF0Q_CFG_REFRESH_DEBUG_SELECT: Refresh debug bus select. 0 selects only master ranks. 1 selects slave ranks.
5:7	RW	MBAREF0Q_CFG_REFRESH_PRIORITY_THRESHOLD: After the number of queued refreshes to a rank reaches this threshold, that rank's refreshes become high priority. Values greater than 0x5 can potentially lead to a refresh timeout FIR.
8:18	RW	MBAREF0Q_CFG_REFRESH_INTERVAL: This value is multiplied by 8 to represent the number of DRAM command clock cycles at which a refresh is to be sent to a rank to honor the refresh interval (tREFI). A refresh to a specific rank will be seen 8 × cfg_refresh_interval × num_ranks × DRAM_command_clock_cycle_time. So, program this dial to: cfg_refresh_interval = desired_tREFI_in_usnum_ranksDRAM_command_clock_cycle_in_ns.008). For example, for a system with two master ranks and four slaves per master (8 ranks total), a desired refresh interval of 7.8 µs, and DDR-1600 memory, cfg_refresh_interval = 7.881.25.008 = 97 (round down)
19:29	RW	MBAREF0Q_CFG_REFRESH_RESET_INTERVAL: This is the value to load the refresh interval counter to when a syncreset pulse is seen from the MBA. This is used to offset refreshing to the different MBAs. **Note**: The refresh reset interval should be set to a value less than the refresh interval.
30:39	RW	MBAREF0Q_CFG_TRFC: Refresh to activate the rank protection timer.
40:49	RW	MBAREF0Q_CFG_REFR_TSV_STACK: Refresh-to-refresh spacing within the same TSV stack timer.
50:60	RW	MBAREF0Q_CFG_REFR_CHECK_INTERVAL: This setting is used to verify that the refresh rules are upheld only (it is not the actual refresh interval). It is multiplied by 8 to represent the number of DRAM command clock cycles at which a refresh is to be seen to a given rank to honor the refresh interval (tREFI). A refresh to a specific rank should be seen 8 × cfg_refresh_check_interval × DRAM_command_clock_cycle_time. So, program this dial to: cfg_refr_check_interval = desired_tREFI_in_usDRAM_command_clock_cycle_in_ns.008). For example, if using DDR-1600 memory and expecting a refresh to occur every 7.8 µs: cfg_refr_check_interval = 7.81.25.008 = 780 = 0x30C If using DDR-1600 memory and expecting a refresh every 3.9 µs: cfg_refr_check_interval = 3.91.25.008 = 390 = 0x186
61	RW	MBAREF0Q_CFG_TRFC_STACK_GATE_ALL_REF: When set, this causes all refreshes to be spaced by cfg_refr_tsv_stack, regardless of whether they are to ranks on the same stack. This mode can be enabled to reduce the power impact due to a burst of refreshes to different ranks.

Bits	SCOM	Field Mnemonic: Description
62:63	RW	MBAREF0Q_RESERVED_62_63: Reserved.

Register Name	Reserved SCOM Address Register
Mnemonic	MC01.PORT3.SRQ.PC.MBARSVD0
Address	00000000070109F3 (SCOM)
Description	Reserved SCOM register address

Bits	SCOM	Field Mnemonic: Description
0:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	Power Control Register 0
Mnemonic	MC01.PORT3.SRQ.PC.MBARPC0Q
Address	00000000070109F4 (SCOM)
Description	Power control register 0

Bits	SCOM	Field Mnemonic: Description
0:1	RW	MBARPC0Q_RESERVED_0_1: Reserved.
2	RW	MBARPC0Q_CFG_MIN_MAX_DOMAINS_ENABLE: This is an overall enable for power domain control. If power control is disabled, the CKEs will always be set to a '1'.
3:5	RW	MBARPC0Q_CFG_MIN_MAX_DOMAINS: Configures dynamic power up and power down of CKEs within specified minmax limits. Maxall_minall means power control will not limit the number of domains accessible at a given time. Power domains will not be powered down even if they go idle, unless min_domain_reduction is enabled. Maxall_minx will permit idle power down to reduce the number of domains powered up after a domain has gone idle, but it will not restrict the maximum domains powered up. Max1_minx restricts the number of domains that can be powered up at a given time to 1.
6:10	RW	MBARPC0Q_CFG_PUP_AVAIL: Specifies how many DRAM command clocks for power control to wait from CKE going high to activate.
11:15	RW	MBARPC0Q_CFG_PDN_PUP: Specifies how many DRAM command clocks for power control to wait from CKE going low to high again (enforces the minimum time in power down).
16:20	RW	MBARPC0Q_CFG_PUP_PDN: Specifies how many DRAM command clocks for power control to wait from CKE going high to low again (enforces the minimum time powered up).
21	RW	MBARPC0Q_RESERVED_21: Reserved.
22	RW	MBARPC0Q_CFG_MIN_DOMAIN_REDUCTION_ENABLE: This allows a dynamic reduction of the minimum domains to 0 when no memory traffic has been seen over the specified cfg_min_domain_reduction_time. Minimum domains will be restored after traffic is seen. The adjusted minimum domains will not be reflected in or overwrite the cfg_min_max_domains setting (adjustment made internal to logic).
23:32	RW	MBARPC0Q_CFG_MIN_DOMAIN_REDUCTION_TIME: Specifies how many DRAM command clocks the MBA must be idle before min_cke is reduced to 0.
33	RW	MBARPC0Q_CFG_PUP_AFTER_ACTIVATE_WAIT_ENABLE: After a configurable time has been met since the last activate, a subsequent domain can be powered up, even if the powering-down domain has not been powered down yet.
34:41	RW	MBARPC0Q_CFG_PUP_AFTER_ACTIVATE_WAIT_TIME: Specifies how many DRAM command clocks the MBA must be idle before the minimum domain is reduced to 0.
42	RW	MBARPC0Q_CFG_FORCE_SPARE_PUP: Forces all spare CKEs to couple with their respective primary CKEs. This bit should not be toggled during run time or when calibration is enabled.

Bits	SCOM	Field Mnemonic: Description
43	RW	MBARPC0Q_CFG_MIN_DOMAIN_REDUCTION_CNT_REFR_INT: If set, use the refresh interval for the minimum domain reduction time interval. Otherwise, use DRAM clocks as the interval.
44:46	RW	MBARPC0Q_CFG_EMER_MIN_MAX_DOMAIN: This is the minmax power domain setting that power control will revert to when emergency throttling is engaged.
47	RW	MBARPC0Q_CFG_PUP_ALL_WRITES_PENDING: Enabling this allows a domain to be powered up upon a write entering the write reorder queue (provided the maximum domains is set to all). **Note**: Reads always cause a power up to their power domain upon entering the read reorder queue (when maximum domains is set to all).
48	RW	MBARPC0Q_CFG_ALWAYS_WAIT_ACT_TIME: If set, when in single domain power up mode, we will always wait the configured time between activates even when all domains are powered down already.
49:63	RW	MBARPC0Q_RESERVED_49_63: Reserved.

Register Name	**STR Register 0**
Mnemonic	MC01.PORT3.SRQ.PC.MBASTR0Q
Address	00000000070109F5 (SCOM)
Description	STR register 0

Bits	SCOM	Field Mnemonic: Description
0	RW	MBASTR0Q_CFG_STR_ENABLE: Enable STR entry. **Note**: Minimum-maximum domains must also be enabled to enter STR.
1	RW	MBASTR0Q_CFG_DIS_CLK_IN_STR: Disable memory clocks when in STR.
2:11	RW	MBASTR0Q_CFG_ENTER_STR_TIME: Number of cfg_min_domain_reduction intervals of idle to wait before entering STR.
12:16	RW	MBASTR0Q_CFG_TCKESR: tCKESR
17:21	RW	MBASTR0Q_CFG_TCKSRE: tCKSRE
22:26	RW	MBASTR0Q_CFG_TCKSRX: tCKSRX
27:37	RW	MBASTR0Q_CFG_TXSDLL: tXSDLL
38:45	RW	MBASTR0Q_CFG_TRFC_COUNTER_DIS: Per tRFC counter disable; Can use this to restrict the number of outstanding refreshes.
46:56	RW	MBASTR0Q_CFG_SAFE_REFRESH_INTERVAL: This is the refresh interval used when in safe-refresh (high-temp) mode. This value is multiplied by 8 to represent the number of DRAM command clock cycles at which a refresh is to be sent to a rank to honor the refresh interval (tREFI). A refresh to a specific rank will be seen 8 × cfg_safe_refresh_interval × num_ranks × DRAM_command_clock_cycle_time. So, program this dial to: cfg_safe_refresh_interval = desired_tREFI_in_usnum_ranksDRAM_command_clock_cycle_in_ns.008). For example, for a system with two master ranks and four slaves per master (8 ranks total), a desired refresh interval of 7.8 µs, and DDR-1600 memory, cfg_safe_refresh_interval = 7.881.25.008 = 97 (round down).

Bits	SCOM	Field Mnemonic: Description
57:60	RW	MBASTR0Q_CFG_OCC_DEADMAN_TIMER_SEL: This selects one of eight timeout values for the OCC deadman timer. If the OCC is idle for the programmed timeout value × timebase pulse, an emergency throttle command is issued and refresh is set to a safe refresh interval. Value Time 0000 = Disabled 0001 = 16 timebase pulses 0010 = 4 timebase pulses 0011 = 8 timebase pulses 0100 = 16 timebase pulses 0101 = 32 timebase pulses 0110 = 64 timebase pulses 0111 = 128 timebase pulses 1000 = 255 timebase pulses 1001 to 1111 are unused.
61	RW	MBASTR0Q_CFG_OCC_DEADMAN_TB_SEL: This selects which timebase pulse to use for the deadman timer. 0 = 1 in 2^{22} DRAM command clocks 1 = 1 in 8K DRAM command clocks
62:63	RW	MBASTR0Q_RESERVED_62_63: Reserved.

Register Name	Refresh Avoidance Control Register
Mnemonic	MC01.PORT3.SRQ.PC.MBAREFAQ
Address	00000000070109F6 (SCOM)
Description	Refresh avoidance control register

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MBAREFAQ_CFG_STATIC_IDLE_DLY: This is the number of cycles that the refresh logic will wait for a rank to be idle in the RRQ before sending a low-priority refresh. **Note**: This delay counts in multiples of four DDR clocks (per default low-priority refresh subcounter setting).
4:5	RW	MBAREFAQ_CFG_LP_SUB_CNT: Subcounter for low-priority refresh scheduling dials. For dials that count based on this subcounter, a value of 00 means that the counter those dials compare against increments every 1 cycle. A value of 01 in this register means that the higher-level count increments every 4th cycle (10 is every 8th cycle, and 11 is every 16th cycle).
6	RW	MBAREFAQ_CFG_REFRESH_HP_RANK_BLOCK_ENABLE: When enabled, the refresh logic sends a block signal when issuing a high-priority refresh. The block signal prevents new demand requests to the refreshing rank from overwhelming the read reorder queue.
7:9	RW	MBAREFAQ_RESERVED_7_9: Reserved.
10:15	RW	MBAREFAQ_CFG_REF_BLOCK_STOP_DLY: Programmable setting that is subtracted from the tRFC timer. The result is used to determine when the block signal can be deasserted leading up to the end of a tRFC period. This allows new commands targeting the refresh domain being refreshed to progress to the RRQ so that they are ready to go as soon as tRFC ends. (N)

Register Name	Performance Monitor Counts0 Register
Mnemonic	MC01.PORT3.SRQ.MBA_PMU0Q
Address	00000000070109F7 (SCOM)
Description	Performance monitor counts0

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MBA_PMU0Q_READ_COUNT: Read count. Increments every read; wraps.
32:63	ROX	MBA_PMU0Q_WRITE_COUNT: Write count. Increments every write; wraps.

Register Name	Performance Monitor Counts1 Register
Mnemonic	MC01.PORT3.SRQ.MBA_PMU1Q
Address	00000000070109F8 (SCOM)
Description	Performance monitor counts1

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MBA_PMU1Q_ACTIVATE_COUNT: Bank activate count. Increments for every activate; wraps.
32:63	ROX	MBA_PMU1Q_PU_COUNTS: Counts the number of rising edges for a CKE; wraps.

Register Name	Performance Monitor Counts2 Register
Mnemonic	MC01.PORT3.SRQ.MBA_PMU2Q
Address	00000000070109F9 (SCOM)
Description	Performance monitor counts2

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MBA_PMU2Q_FRAME_COUNT: Frame count. Increments every DRAM clock(2:1) clock.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Performance Monitor Counts4 Register
Mnemonic	MC01.PORT3.SRQ.MBA_PMU3Q
Address	00000000070109FA (SCOM)
Description	Performance monitor counts4

Bits	SCOM	Field Mnemonic: Description
0:15	RW	MBA_PMU3Q_LOW_IDLE_THRESHOLD: Each time the low idle (no reads or writes queued) threshold is met, the low idle count will increment. Between periods of command activity, there may be multiple low-idle-threshold-width windows of command inactivity. For each of these windows, the low idle count will be incremented. (counts 2:1Dram address frequency) counts MBA idle cycles.
16:31	RW	MBA_PMU3Q_MED_IDLE_THRESHOLD: Each time the medium idle (no reads or writes queued) threshold is met, the medium idle count will increment. Between periods of command activity, there may be multiple medium-idle-threshold-width windows of command inactivity. For each of these windows, the medium idle count will be incremented.
32:63	RW	MBA_PMU3Q_HIGH_IDLE_THRESHOLD: Each time the high idle (no reads or writes queued) threshold is met, the high idle count will increment. Between periods of command activity, there may be multiple high-idle-threshold-width windows of command inactivity. For each of these windows, the high idle count will be incremented.

Register Name	Performance Monitor Counts Register
Mnemonic	MC01.PORT3.SRQ.MBA_PMU4Q
Address	00000000070109FB (SCOM)
Description	Performance monitor counts

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MBA_PMU4Q_BASE_IDLE_COUNT: Increments every MBA idle cycle (counts 2:1Dram address frequency).
32:63	ROX	MBA_PMU4Q_LOW_IDLE_COUNT: Counts the number of times the low idle threshold was met (counts 2:1Dram address frequency).

Register Name	Performance Monitor Counts Register
Mnemonic	MC01.PORT3.SRQ.MBA_PMU5Q
Address	00000000070109FC (SCOM)
Description	Performance monitor counts

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MBA_PMU5Q_MED_IDLE_COUNT: Counts the number of times the medium idle threshold was met (counts 2:1Dram address frequency).
32:63	ROX	MBA_PMU5Q_HIGH_IDLE_COUNT: Counts the number of times the high idle threshold was met (counts 2:1Dram address frequency).

Register Name	Performance Monitor Counts Register
Mnemonic	MC01.PORT3.SRQ.MBA_PMU6Q
Address	00000000070109FD (SCOM)
Description	Performance monitor counts

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	MBA_PMU6Q_EVENT0_COUNTER: PMU count for event 0.
16:31	ROX	MBA_PMU6Q_EVENT1_COUNTER: PMU count for event 1.
32:47	ROX	MBA_PMU6Q_EVENT2_COUNTER: PMU count for event 2.
48:63	ROX	MBA_PMU6Q_EVENT3_COUNTER: PMU count for event 3.

Register Name	Performance Monitor Event Select Register
Mnemonic	MC01.PORT3.SRQ.MBA_PMU7Q
Address	00000000070109FE (SCOM)
Description	Performance monitor event select register

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MBA_PMU7Q_CFG_EVENT0_SELECT: Event0 select. 0x00 = MBA command clocks 0x01 = ACT all 0x02 = ACT for read 0x03 = ACT for write 0x04 = CAS all 0x05 = CAS for read 0x06 = CAS for write 0x07 = CAS for low-priority write 0x08 = CAS for high-priority write 0x09 = PRE all 0x0a = PRE for read 0x0b = PRE for write 0x0c = REF high priority 0x0d = REF low priority 0x0e = REF all 0x0f = RRQ empty 0x10 = RRQ full 0x11 = WRQ empty 0x12 = WRQ full 0x13 = WRQ above hw mark 0x14 = Reserved 0x15 = Activate with direction switch (change from rd→wr or wr→rd) 0x16 = Activate with mrank switch (Master rank different than previous ACT) 0x17 = Activate with srank switch (Same master; slave rank different than previous ACT) 0x18 = Activate with bank group switch (Same master, slave; bank group different than previous ACT) 0x19 = Activate with bank switch (Same master, slave, bank group; different bank than previous ACT) 0x1a = All bank timers full 0x1b = Any CKE PUP transition (0→1) 0x1c = CKE0 cycles PUP 0x1d = CKE1 cycles PUP 0x1e = CKE2 cycles PUP 0x1f = CKE3 cycles PUP 0x20 = WDF stalled waiting on read buffer 0x21 = WDF stalled waiting on read ramp 0x22 = Command0 compare 0x23 - 0x3f = Reserved

Bits	SCOM	Field Mnemonic: Description
6:11	RW	MBA_PMU7Q_CFG_EVENT1_SELECT: Event1 select. 0x00 = MBA command clocks 0x01 = ACT all 0x02 = ACT for read 0x03 = ACT for write 0x04 = CAS all 0x05 = CAS for read 0x06 = CAS for write 0x07 = CAS for low-priority write 0x08 = CAS for high-priority write 0x09 = PRE all 0x0a = PRE for read 0x0b = PRE for write 0x0c = REF high priority 0x0d = REF low priority 0x0e = REF all 0x0f = RRQ empty 0x10 = RRQ full 0x11 = WRQ empty 0x12 = WRQ full 0x13 = WRQ above hw mark 0x14 = Reserved 0x15 = Activate with direction switch (change from rd→wr or wr→rd) 0x16 = Activate with mrank switch (Master rank different than previous ACT) 0x17 = Activate with srank switch (Same master; slave rank different than previous ACT) 0x18 = Activate with bank group switch (Same master, slave; bank group different than previous ACT) 0x19 = Activate with bank switch (Same master, slave, bank group; different bank than previous ACT) 0x1a = All bank timers full 0x1b = Any CKE PUP transition (0→1) 0x1c = CKE0 cycles PUP 0x1d = CKE1 cycles PUP 0x1e = CKE2 cycles PUP 0x1f = CKE3 cycles PUP 0x20 = WDF stalled waiting on read buffer 0x21 = WDF stalled waiting on read ramp 0x22 = Command1 compare 0x23 - 0x3f = Reserved

Bits	SCOM	Field Mnemonic: Description
12:17	RW	MBA_PMU7Q_CFG_EVENT2_SELECT: Event2 select. 0x00 = MBA command clocks 0x01 = ACT all 0x02 = ACT for read 0x03 = ACT for write 0x04 = CAS all 0x05 = CAS for read 0x06 = CAS for write 0x07 = CAS for low-priority write 0x08 = CAS for high-priority write 0x09 = PRE all 0x0a = PRE for read 0x0b = PRE for write 0x0c = REF high priority 0x0d = REF low priority 0x0e = REF all 0x0f = RRQ empty 0x10 = RRQ full 0x11 = WRQ empty 0x12 = WRQ full 0x13 = WRQ above hw mark 0x14 = Reserved 0x15 = Activate with direction switch (change from rd→wr or wr→rd) 0x16 = Activate with mrank switch (Master rank different than previous ACT) 0x17 = Activate with srank switch (Same master; slave rank different than previous ACT) 0x18 = Activate with bank group switch (Same master, slave; bank group different than previous ACT) 0x19 = Activate with bank switch (Same master, slave, bank group; different bank than previous ACT) 0x1a = All bank timers full 0x1b = Any CKE PUP transition (0→1) 0x1c = CKE0 cycles PUP 0x1d = CKE1 cycles PUP 0x1e = CKE2 cycles PUP 0x1f = CKE3 cycles PUP 0x20 = WDF stalled waiting on read buffer 0x21 = WDF stalled waiting on read ramp 0x22 = Command2 Compare 0x23 - 0x3f = Reserved

Bits	SCOM	Field Mnemonic: Description
18:23	RW	MBA_PMU7Q_CFG_EVENT3_SELECT: Event3 select. 0x00 = MBA command clocks 0x01 = ACT all 0x02 = ACT for read 0x03 = ACT for write 0x04 = CAS all 0x05 = CAS for read 0x06 = CAS for write 0x07 = CAS for low-priority write 0x08 = CAS for high-priority write 0x09 = PRE all 0x0a = PRE for read 0x0b = PRE for write 0x0c = REF high priority 0x0d = REF low priority 0x0e = REF all 0x0f = RRQ empty 0x10 = RRQ full 0x11 = WRQ empty 0x12 = WRQ full 0x13 = WRQ above hw mark 0x14 = Reserved 0x15 = Activate with direction switch (change from rd→wr or wr→rd) 0x16 = Activate with mrank switch (Master rank different than previous ACT) 0x17 = Activate with srank switch (Same master; slave rank different than previous ACT) 0x18 = Activate with bank group switch (Same master, slave; bank group different than previous ACT) 0x19 = Activate with bank switch (Same master, slave, bank group; different bank than previous ACT) 0x1a = All bank timers full 0x1b any CKE PUP transition (0→1) 0x1c = CKE0 cycles PUP 0x1d = CKE1 cycles PUP 0x1e = CKE2 cycles PUP 0x1f = CKE3 cycles PUP 0x20 = WDF stalled waiting on read buffer 0x21 = WDF stalled waiting on read ramp 0x22 - 0x3f = Reserved
24:25	RW	MBA_PMU7Q_CFG_PRESCALER_C0: Prescaler for event counter 0. 00 = 20-bit 01 = 16-bit 10 = 8-bit 11 = 4-bit
26:27	RW	MBA_PMU7Q_CFG_PRESCALER_C1: Prescaler for event counter 1. 00 = 20-bit 01 = 16-bit 10 = 8-bit 11 = 4-bit
28:29	RW	MBA_PMU7Q_CFG_PRESCALER_C2: Prescaler for event counter 2. 00 = 20-bit 01 = 16-bit 10 = 8-bit 11 = 4-bit
30:31	RW	MBA_PMU7Q_CFG_PRESCALER_C3: Prescaler for event counter r 3. 00 = 20-bit 01 = 16-bit 10 = 8-bit 11 = 4-bit

Bits	SCOM	Field Mnemonic: Description
32:34	RW	MBA_PMU7Q_CASCADE: Allows cascading of counts to make a 32-bit counter. X00 = no cascading 001 = c0 → c1 010 = c1 → c2 011 = c2 → c3 101 = c1 → c0 110 = c2 → c1 111 = c3 → c2
35	RW	MBA_PMU7Q_FREEZE: If enabled, freeze all counters when any counter reaches maximum.

Register Name	Performance Monitor Command Compare Register
Mnemonic	MC01.PORT3.SRQ.MBA_PMU8Q
Address	00000000070109FF (SCOM)
Description	Performance monitor command compare register

Bits	SCOM	Field Mnemonic: Description
0:1	RW	MBA_PMU8Q_CFG_CMD0_TYPE: Command 0 compare type qualifier. 00 = Read 01 = Write 10 = Activate 11 = Read or write
2	RW	MBA_PMU8Q_CFG_CMD0_MRANK_MATCH_EN:
3	RW	MBA_PMU8Q_CFG_CMD0_SRANK_MATCH_EN:
4	RW	MBA_PMU8Q_CFG_CMD0_BG_MATCH_EN:
5	RW	MBA_PMU8Q_CFG_CMD0_BANK_MATCH_EN:
6:8	RW	MBA_PMU8Q_CFG_CMD0_MRANK:
9:11	RW	MBA_PMU8Q_CFG_CMD0_SRANK:
12:13	RW	MBA_PMU8Q_CFG_CMD0_BG:
14:16	RW	MBA_PMU8Q_CFG_CMD0_BANK:
17:18	RW	MBA_PMU8Q_CFG_CMD1_TYPE: Command 1 compare type qualifier. 00 = Read 01 = Write 10 = Activate 11 = Read or write
19	RW	MBA_PMU8Q_CFG_CMD1_MRANK_MATCH_EN:
20	RW	MBA_PMU8Q_CFG_CMD1_SRANK_MATCH_EN:
21	RW	MBA_PMU8Q_CFG_CMD1_BG_MATCH_EN:
22	RW	MBA_PMU8Q_CFG_CMD1_BANK_MATCH_EN:
23:25	RW	MBA_PMU8Q_CFG_CMD1_MRANK:
26:28	RW	MBA_PMU8Q_CFG_CMD1_SRANK:
29:30	RW	MBA_PMU8Q_CFG_CMD1_BG:
31:33	RW	MBA_PMU8Q_CFG_CMD1_BANK:

Bits	SCOM	Field Mnemonic: Description
34:35	RW	MBA_PMU8Q_CFG_CMD2_TYPE: Command 2 compare type qualifier. 00 = Read 01 = Write 10 = Activate 11 = Read or write
36	RW	MBA_PMU8Q_CFG_CMD2_MRANK_MATCH_EN:
37	RW	MBA_PMU8Q_CFG_CMD2_SRANK_MATCH_EN:
38	RW	MBA_PMU8Q_CFG_CMD2_BG_MATCH_EN:
39	RW	MBA_PMU8Q_CFG_CMD2_BANK_MATCH_EN:
40:42	RW	MBA_PMU8Q_CFG_CMD2_MRANK:
43:45	RW	MBA_PMU8Q_CFG_CMD2_SRANK:
46:47	RW	MBA_PMU8Q_CFG_CMD2_BG:
48:50	RW	MBA_PMU8Q_CFG_CMD2_BANK:
51:63	RW	MBA_PMU8Q_RESERVED_51_63:

Register Name	Datapath Fault Isolation Register
Mnemonic	MC01.PORT0.ECC64.SCOM.FIR
Address	0000000007010A00 (SCOM) 0000000007010A01 (SCOM1) 0000000007010A02 (SCOM2)
Description	Datapath fault isolation register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:7	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_MPE_RANK_0_TO_7: Mark placed error (MPE) detected on a mainline read. The corresponding Hardware Mark Store Register (HWMSx [x = 0..7]) is updated with a chipmark for the associated master rank.
8	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_NCE: New correctable error (NCE) detected on a mainline read.
9	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_TCE: Two-symbol correctable error (TCE) detected on a mainline read.
10	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_SCE: Symbol mark corrected error (SCE) detected on a mainline read.
11	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_MCE: Chip mark corrected error (MCE) detected on a mainline read.
12	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_SUE: Special uncorrectable error (SUE) detected on a mainline read.
13	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_AUE: Address uncorrectable error (AUE) detected on a mainline read.
14	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_UE: Uncorrectable error (UE) detected on a mainline read.
15	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_RCD: Parity error detected by registering clock driver (RCD) detected on a mainline read.
16	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_IAUE: Intermittent AUE (IAUE) detected on a mainline read.
17	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_IUE: Intermittent UE (IUE) detected on a mainline read.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
18	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_IRCD: Intermittent RCD (IRCD) detected on a mainline read.
19	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_IMPE: Intermittent MPE (IMPE) detected on a mainline read.
20:27	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_MPE_RANK_0_TO_7: Mark placed error (MPE) detected on a maintenance read. The corresponding Hardware Mark Store Register (HWMSx [x = 0..7]) is updated with a chipmark for the associated master rank.
28	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_NCE: New correctable error (NCE) detected on a maintenance read.
29	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_TCE: Two-symbol correctable error (TCE) detected on a maintenance read.
30	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_SCE: Symbol mark corrected error (SCE) detected on a maintenance read.
31	RWX	WOX_AND	WOX_OR	Fir_maintenance_mce: Chip mark corrected error (MCE) detected on a maintenance read.
32	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_SUE: Special uncorrectable error (SUE) detected on a maintenance read.
33	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_AUE: Address uncorrectable error (AUE) detected on a maintenance read.
34	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_UE: Uncorrectable error (UE) detected on a maintenance read.
35	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_RCD: Parity error detected by registering clock driver (RCD) detected on a maintenance read.
36	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_IAUE: Intermittent AUE (IAUE) detected on a maintenance read.
37	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_IUE: Intermittent UE (IUE) detected on a maintenance read.
38	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_IRCD: Intermittent RCD (IRCD) detected on a maintenance read.
39	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_IMPE: Intermittent MPE (IMPE) detected on a maintenance read.
40	RWX	WOX_AND	WOX_OR	FIR_RESERVED_40: Reserved.
41	RWX	WOX_AND	WOX_OR	FIR_SCOM_PARITY_CLASS_STATUS: SCOM register parity error, for registers in the “status” class (no data integrity risk). For more information, see the CERR0 register.
42	RWX	WOX_AND	WOX_OR	FIR_SCOM_PARITY_CLASS_RECOVERABLE: SCOM register parity error, for registers in 'recoverable' class (no data integrity risk; register must be reloaded). For more information, see the CERR0 register (page 214).
43	RWX	WOX_AND	WOX_OR	FIR_SCOM_PARITY_CLASS_UNRECOVERABLE: SCOM register parity error, for registers in the “unrecoverable” class (data integrity risk). For more information, see the CERR0 register (page 214).
44	RWX	WOX_AND	WOX_OR	FIR_ECC_CORRECTOR_INTERNAL_PARITY_ERROR: ECC corrector internal parity error. Data Integrity risk. For more information, see the CERR1 register (page 215).
45	RWX	WOX_AND	WOX_OR	FIR_WRITE_RMW_CE: CE detected at Write or RMW buffer read port. For more information, see the CERR1 and WRT_ECC registers (pages 215 and 224).

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
46	RWX	WOX_AND	WOX_OR	FIR_WRITE_RMW_UE: UE detected at Write or RMW buffer read port. For more information, see the CERR1 and WRT_ECC registers (pages 215 and 224).
47	RWX	WOX_AND	WOX_OR	FIR_WRITE_RMW_SUE: SUE detected at Write or RMW buffer read port. For more information, see the CERR1 and WRT_ECC registers (pages 215 and 224).
48	RWX	WOX_AND	WOX_OR	FIR_WDF_OVERRUN_ERROR_0: WDF logic detected a buffer overrun error (class 0).
49	RWX	WOX_AND	WOX_OR	FIR_WDF_OVERRUN_ERROR_1: WDF logic detected a buffer overrun error (class 1).
50	RWX	WOX_AND	WOX_OR	FIR_WDF_SCOM_SEQUENCE_ERROR: WDF logic detected a SCOM sequence error.
51	RWX	WOX_AND	WOX_OR	FIR_WDF_STATE_MACHINE_ERROR: WDF logic detected a state machine error.
52	RWX	WOX_AND	WOX_OR	FIR_WDF_MISC_REGISTER_PARITY_ERROR: WDF logic detected a miscellaneous register parity error.
53	RWX	WOX_AND	WOX_OR	FIR_WRT_SCOM_SEQUENCE_ERROR: WRT logic detected a SCOM sequence error.
54	RWX	WOX_AND	WOX_OR	FIR_WRT_MISC_REGISTER_PARITY_ERROR: WRT logic detected a miscellaneous register parity error.
55	RWX	WOX_AND	WOX_OR	FIR_ECC_GENERATOR_INTERNAL_PARITY_ERROR: ECC generator internal parity error (data integrity risk).
56	RWX	WOX_AND	WOX_OR	FIR_READ_BUFFER_OVERFLOW_ERROR: Read buffer overflow error (data integrity risk).
57	RWX	WOX_AND	WOX_OR	FIR_WDF_ASYNC_INTERFACE_ERROR: WDF asynchronous interface error.
58	RWX	WOX_AND	WOX_OR	FIR_READ_ASYNC_INTERFACE_PARITY_ERROR: READ asynchronous interface parity error.
59	RWX	WOX_AND	WOX_OR	FIR_READ_ASYNC_INTERFACE_SEQUENCE_ERROR: READ asynchronous interface sequence error.
60:61	RWX	WOX_AND	WOX_OR	FIR_RESERVED: Reserved.
62	RWX	WOX_AND	WOX_OR	FIR_INTERNAL_SCOM_ERROR: A SCOM/FIR internal error has occurred.
63	RWX	WOX_AND	WOX_OR	FIR_INTERNAL_SCOM_ERROR_COPY: A SCOM/FIR internal error has occurred (redundant copy).

Register Name	**Datapath FIR Mask Register**
Mnemonic	MC01.PORT0.ECC64.SCOM.MASK
Address	0000000007010A03 (SCOM) 0000000007010A04 (SCOM1) 0000000007010A05 (SCOM2)
Description	Datapath FIR mask

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:63	RW	WO_AND	WO_OR	MASK_FIR_MASK: MASK for FIR bits 0:63.

Register Name	Datapath FIR Action 0 Register
Mnemonic	MC01.PORT0.ECC64.SCOM.ACTION0
Address	0000000007010A06 (SCOM)
Description	Datapath FIR action 0

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ACTION0_FIR_ACTION0: Action0 select for corresponding bits in the FIR. (Action0, Action1, Mask) selects: (0,0,0) = Checkstop error (0,1,0) = Recoverable error (1,0,0) = Attention (1,1,0) = Local checkstop error (X,X,1) = Masked

Register Name	Datapath FIR Action 1 Register
Mnemonic	MC01.PORT0.ECC64.SCOM.ACTION1
Address	0000000007010A07 (SCOM)
Description	Datapath FIR action 1

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ACTION1_FIR_ACTION1: Action1 select for corresponding bits in FIR. (Action0, Action1, Mask) selects: (0,0,0) = Checkstop error (0,1,0) = Recoverable error (1,0,0) = Attention (1,1,0) = Local checkstop error (X,X,1) = Masked

Register Name	Datapath FIR “Who is On First”’ Register
Mnemonic	MC01.PORT0.ECC64.SCOM.WOF
Address	0000000007010A08 (SCOM)
Description	Datapath FIR “Who is On First”

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	WOF_FIR_WOF: The WOF register locks on the first error. Writing zeros the register.

Register Name	Read ECC Control Register
Mnemonic	MC01.PORT0.ECC64.SCOM.RECR
Address	0000000007010A0A (SCOM)
Description	Read ECC control register

Bits	SCOM	Field Mnemonic: Description
0	RW	MBSECCQ_DISABLE_MEMORY_ECC_CHECK_CORRECT: When set, memory ECC check and correct is disabled. When memory ECC checking is disabled, the SUE injecting into the 8-byte data bus ECC is also disabled.
1	RW	MBSECCQ_DISABLE_MEMORY_ECC_CORRECT: When set, memory ECC correct is disabled (memory ECC checking is not disabled).
2	RW	MBSECCQ_DISABLE_MARK_STORE_WRITE: Disables update of the Hardware Mark Store Register (HWMSx [x = 0..7]) registers on an MPE.
3	RW	MBSECCQ_DISABLE_UE_RETRY: When off, a read diagnosed as an exit-point-2 uncorrectable error (UE, AUE, or RCD) is retried. The FIR is set if the problem reoccurs on the retry. If the problem does not reoccur, the IUE/IAUE/IRCD FIR is set. When on, the UE/AUE/RCD FIRs are set immediately, and the IUE/IAUE/IRCD FIRS are not set.
4	RW	MBSECCQ_ITAG_METADATA_ENABLE: Enables I-series tag bits in the metadata symbols. When this dial is not set, the tag bits are used as four additional check bits.
5	RW	MBSECCQ_SLOW_EXIT_REDUCTION: When set, exit selection is modified to prevent the pileup of output data beats by choosing a later exit than would normally be used. Latency is increased. This mode is intended as a workaround to potential read_mac asynchronous interface issues.
6:8	RW	MBSECCQ_READ_POINTER_DELAY: Read pointer delay (mba_mbx_rdtag_val to mbr_ddr_clock_en) is (dial value + 2) MEMx2 cycles. This field interacts with MBSECCQ_ECC_SCHEDULER_DELAY according to the following formula: rdptrdly + 3 + (staging latches to PHY on mbr_ddr_* and from PHY on ddr_mbr_rdata) = scheddly + 7 Both rdptrdly and scheddly must be in the range 0 - 7.
9:10	RW	MBSECCQ_EXIT_OVERRIDE: Non-zero settings are for debug operation only.
11	RW	MBSECCQ_HWMARK_EXIT1: Selects the value to which HWMSx(9) [exit_1] is set when hardware sets a chipmark.
12	RW	MBSECCQ_DATA_GENERATOR_OVERRIDE: Also known as “wrap mode.” When set, overrides ECC corrector data output with an address-based data pattern. In each doubleword: bits 0:15 = 0xdead bits 16:19 = port index (0..7) bits 20:22 = 0 bit 23 = DIMM bits 24:25 = master rank bits 26:28 = slave rank bits 29:30 = bank group bits 31:33 = bank bits 34:51 = row(0:17) bits 52:59 = col(2:9) bits 60:63 = doubleword index (0 to 3) Metadata (I-series tags and MDI bit) will be zero. **Note**: Wrap mode also requires Exit_Override set to 0b01 (force_exit_0).
13:15	RW	MBSECCQ_ECC_SCHEDULER_DELAY: ECC scheduler delay (mba_mbx_rdtag_val to scheduler start). See MBSECCQ_Read_Pointer_Delay (6:8).
16:18	RW	MBSECCQ_VAL_TO_DATA_DELAY: Asynchronous side 2x cycle delay from ecc_tag_valid_rd to data valid. Affects the asynchronous interface.
19	RW	MBSECCQ_DELAY_VALID_1X: When set, read control delays ecc_tag_valid_rd by one MCA 1x cycle. In effect, subtracts 0.5 from val_to_data_delay.
20:21	RW	MBSECCQ_NEST_VAL_TO_DATA_DELAY: Number of extra nest cycles of delay from tag to data. The valid range is 0 - 2. Affects the asynchronous interface.
22	RW	MBSECCQ_DELAY_NONBYPASS: When set, adds one extra nest cycle delay for nonbypass data (needed for null_xfer/retry signal).
23	RW	MBSECCQ_ENABLE_SPECIAL_ATTENTION: When set, FIRs with action set to 10 assert special_attention.

Bits	SCOM	Field Mnemonic: Description
24	RW	MBSECCQ_ENABLE_HOST_ATTENTION: When set, FIRs with action set to 10 assert host_attention.
25	RW	MBSECCQ_DISABLE_MPE_CONFIRM: When set, hardware marks are placed in the confirmed state.
26	RW	MBSECCQ_ENABLE_UE_NOISE_WINDOW: Enables noise window processing whenever a UE (or an AUE) is detected.
27	RW	MBSECCQ_ENABLE_TCE_CORRECTION: Enables two-symbol error correction.
28	RW	MBSECCQ_ENABLE_CHIPMARKED_SCE_NCE: Enables correction of a marked symbol, and one unmarked symbol, when there is a chip mark (but no error in the marked chip).
29	RW	MBSECCQ_USE_ADDRESS_HASH: Enables use of an address hash in the ECC.
30:31	RW	MBSECCQ_DATA_INVERSION: Controls inversion of data to or from the PHY. Data and checks (including metadata) can be inverted for data beats where col(2) = 1. Alternatively, data can be set to always invert, while checks invert where col(2) = 1.
32	RW	MBSECCQ_DISABLE_PIPE_NOERR_CLOCK_GATING: Disables these no-err/no-change clock gating features in the ECC pipe: 1) Mark precomputation is normally held while marks remain the same (for example, all-0). 2) Post-syndrome ECC computation stages are held while there is no new error.
33	RW	MBSECCQ_MAINT_NO_RETRY_UE: Maintenance equivalent of DISABLE_UE_RETRY (bit 3).
34	RW	MBSECCQ_MAINT_NO_RETRY_MPE: Maintenance equivalent of DISABLE_MPE_CONFIRM (bit 25).
35	RW	MBSECCQ_DISABLE_BYPASS_TEMPLATE_A: Disables least-latency mode for 128-byte bypass reads, so that beat 1 has an SUE in case of a bypass error on beat 0.
36:43	RW	MBSECCQ_RESERVED_36_43: Reserved.

Register Name	ECC Debug/WAT Control Register
Mnemonic	MC01.PORT0.ECC64.SCOM.DBGR
Address	0000000007010A0B (SCOM)
Description	ECC debug/WAT control register

Bits	SCOM	Field Mnemonic: Description
0	RW	DBGR_ECC_DEBUG_ENABLE: Enable the debug bus in the ECC64 macro. Required for debug of ECC64 or SRQ.
1:2	RW	DBGR_ECC_DEBUG_CHUNK_SELECT: Select 0, 1, 2, or 4 22-bit data chunks from ECC debug sources. ECC data is inserted in the debug bus as follows: 00 = inp inp inp inp 01 = inp inp inp ecc 10 = inp inp ecc ecc 11 = ecc ecc ecc ecc Other fields of the debug bus output propagate the input (inp).
3:5	RW	DBGR_ECC_DEBUG_PRIMARY_SELECT: Primary select for the ECC debug source. 000 = sch1 sch2 ep21 ep22 / - - ep21 ep22 / - - - ep22 001 = sch1 sch2 ep22 ep21 / - - ep22 ep21 / - - - ep21 010 = ep21 ep22 wrd1 wrd2 / - - wrd1 wrd2 / - - - wrd2 011 = ep21 ep22 wrd2 wrd1 / - - wrd2 wrd1 / - - - wrd1 100 = wrd1 wrd2 sch1 sch2 / - - sch1 sch2 / - - - sch2 101 = wrd1 wrd2 sch2 sch1 / - - sch2 sch1 / - - - sch1 where: sch1 and sch2 are collections of debug information for the ECC corrector's scheduler logic. ep21 and ep22 are collections of debug information related to the exit-point-2 state logic. wrd1 and wrd2 are collections of debug information related to the write data logic.

Bits	SCOM	Field Mnemonic: Description
6:7	RW	DBGR_ECC_DEBUG_SECONDARY_SELECT: Secondary select for the ECC debug data. Action varies by the primary source bus.
8	RW	DBGR_ECC_WAT_ENABLE: Enable workaround logic in the ECC corrector.
9	RW	DBGR_ECC_WAT_ACTION_SELECT: Select the workaround action: 0 = Bypass disable (while the selected WAT event is 1). 1 = Force exit 2 (while the selected WAT event is 1).
10:11	RW	DBGR_ECC_WAT_SOURCE: Select the WAT event (bit 0 to 3).
12:14	RW	DBGR_READ_DEBUG_SELECT: Select the debug source data in the read macro.

Register Name	Mark Shadow Register
Mnemonic	MC01.PORT0.ECC64.SCOM.MSR
Address	0000000007010A0C (SCOM)
Description	Mark shadow register

Bits	SCOM	Field Mnemonic: Description
0:7	RO	Constant = 0b00000000
8:15	ROX	MSR_CHIPMARK: Mark the location (Galois field code) of the last mark placed (includes unconfirmed marks).
16:18	ROX	MSR_RANK: Rank of the last mark placed (includes unconfirmed marks).
19:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000

Register Name	Error Inject Control Register
Mnemonic	MC01.PORT0.ECC64.SCOM.EICR
Address	0000000007010A0D (SCOM)
Description	Error inject control register

Bits	SCOM	Field Mnemonic: Description
0:36	RW	EICR_ADDRESS: An error is injected when the read address matches the EICR address, up to the fields masked by the EICR region. bit 0 = DIMM select bits 1:2 = mrank(0:1) bits 3:5 = srank(0:2) bits 6:7 = bank_group(0:1) bits 8:10 = bank(0:2) bits 11:28 = row(0:17) bits 29:36 = col(2:9)
37	RW	EICR_RESERVED: Reserved.
38:39	RW	EICR_PERSIST: Persistence of injected error. Set to disabled (00) to disable error injection. Affects the memory ECC error injection selected via the type field, or the miscellaneous injection via the MISC field.
40:42	RW	EICR_REGION: Address region size for error inject.

Bits	SCOM	Field Mnemonic: Description
43:47	RW	EICR_TYPE: Bitmask for the error type to inject. bit 43 = Inject address UE. bit 44 = Inject DQ 0 (symbol 71, Galois code 0x38). bit 45 = Inject DQ 1 (symbol 70, Galois code 0xa2). bit 46 = Inject DQ 4 (symbol 39, Galois code 0x46). bit 47 = Inject DQ 5,6 (symbols 38,37, Galois codes 0x1d, x0f4).
48:51	RW	EICR_MISC: Selects miscellaneous error injections: • 8-byte ECC error injection at the output of the memory ECC checker. Inject a CE in bit 0 or bit 1, or a UE in both bits. Any data read from memory into either the RMW buffer or READ buffer will be injected. Errors should be visible in RMW ECC checkers or in the read master's ECC checkers. • Inject FIR(44) = ecc_corrector_internal_parity_error. • Inject read path asynchronous interface errors (parity or sequence_check). Miscellaneous errors are not affected by the address or region, but are affected by persistence (both soft_error and hard_error persistence act as a continuous inject). Undefined codes inject no error.

Register Name	Error Report Hold Register 0 (SCOM Register Parity Errors)
Mnemonic	MC01.PORT0.ECC64.SCOM.CERR0
Address	0000000007010A0E (SCOM)
Description	Each register parity error is reported in the bit location corresponding to the least 6 bits of the register's SCOM address. Writing the CERR0 register clears all hold bits in CERR0 and CERR1.

Bits	SCOM	Field Mnemonic: Description
0:9	RO	Constant = 0b0000000000
10	RWX_WCLRREG	CERR0_RECR_PE: RECR parity error (FIR 43).
11	RO	Constant = 0b0
12	RWX_WCLRREG	CERR0_MSR_PE: MSR parity error (FIR 41).
13	RWX_WCLRREG	CERR0_EICR_PE: EICR parity error (FIR 42).
14:15	RO	Constant = 0b00
16:23	RWX_WCLRREG	CERR0_HWMSX_PE: Hardware Mark Store Register **x (**HWMSx [x = 0..7]) parity error (FIR 42).
24:31	RWX_WCLRREG	CERR0_FWMSX_PE: Firmware Mark Store Register x (FWMSx) parity error (FIR 42).
32:39	RO	Constant = 0b00000000
40	RWX_WCLRREG	CERR0_WECR_PE: WECR parity error (FIR 43).
41	RWX_WCLRREG	CERR0_AACR_PE: AACR parity error (FIR 42).
42	RWX_WCLRREG	CERR0_AADR_PE: AADR parity error (FIR 42).
43	RWX_WCLRREG	CERR0_AAER_PE: AAER parity error (FIR 42).

Bits	SCOM	Field Mnemonic: Description
44	RWX_WCLRREG	CERR0_MCBCM_PE: MCBCM parity error (FIR 42).
45:47	RO	Constant = 0b000
48	RWX_WCLRREG	CERR0_WDFCFG_PE: WDFCFG parity error (FIR 52).
49:55	RO	Constant = 0b0000000
56	RWX_WCLRREG	CERR0_WRTCFG_PE: WRTCFG parity error (FIR 54).
57:63	RO	Constant = 0b0000000

Register Name	Error Report Hold Register 1
Mnemonic	MC01.PORT0.ECC64.SCOM.CERR1
Address	0000000007010A0F (SCOM)
Description	Contains error hold bits for errors other than SCOM register parity errors. Writing the CERR0 register clears all hold bits in CERR0 and CERR1. CERR1 makes various internal error detections visible.

Bits	SCOM	Field Mnemonic: Description
0	ROX	CERR1_ECC_CTL_AF_PERR: Sticky bit for a read ECC control-logic address FIFO parity error (FIR 44).
1	ROX	CERR1_ECC_CTL_RPTR_PERR: Sticky bit for a read ECC control-logic read-pointer timer parity error (FIR 44).
2	ROX	CERR1_ECC_CTL_TCHN_PERR: Sticky bit for a read ECC control-logic main timer parity error (FIR 44).
3	ROX	CERR1_ECC_CTL_CMPMODE_ERR: Sticky bit for a read ECC control-logic compare-mode error (FIR 44).
4	ROX	CERR1_ECC_CTL_SCHCTL_PERR: Sticky bit for a read ECC control-logic scheduler control parity error (FIR 44).
5	ROX	CERR1_ECC_CTL_PCTL_PERR: Sticky bit for a read ECC control-logic pipe control parity error (FIR 44).
6	ROX	CERR1_ECC_CTL_TGST_PERR: Sticky bit for a read ECC control-logic retry state parity error (FIR 44).
7	ROX	CERR1_ECC_CTL_SCHTAB_PERR: Sticky bit for a read ECC control-logic schedule table parity error (FIR 44).
8	ROX	CERR1_ECC_PIPE_PCX_PERR: Sticky bit for a read ECC mark precomputation parity error (FIR 44).
9	ROX	CERR1_ECC_PIPE_SYND_PERR: Sticky bit for a read ECC syndrome parity error (FIR 44).
10	ROX	CERR1_ECC_PIPE_2SYM_PERR: Sticky bit for a read ECC 2-symbol corrector parity error (FIR 44).
11	ROX	CERR1_ECC_PIPE_CPLX_PERR: Sticky bit for a read ECC complex corrector parity error (FIR 44).
12	ROX	CERR1_ECC_PIPE_EP2_PERR: Sticky bit for a read ECC exit-2 parity error (FIR 44).
13	ROX	CERR1_READ_ECC_DATAPATH_PARITY_ERROR: Sticky bit for a read ECC datapath parity error (FIR 44).
14	ROX	CERR1_PHY_RPTR_PARITY_ERROR: Sticky bit for a DDR PHY read-pointer parity error (FIR 44).
15	ROX	CERR1_ECC_CTL_RPD_PERR: Sticky bit for a read ECC control-logic pointer delay logic parity error (FIR 44).
16	ROX	CERR1_WDF_ASYNC_ERROR: Sticky bit for a WDF asynchronous interface error (FIR 57).
17	ROX	CERR1_WDF_BUFFER_CE: Sticky bit for a WDF buffer CE (FIR 45).
18	ROX	CERR1_WDF_BUFFER_UE: Sticky bit for a WDF buffer UE (FIR 46).
19	ROX	CERR1_WDF_BUFFER_SUE: Sticky bit for a WDF buffer SUE (FIR 47).
20:24	RO	Constant = 0b00000

Bits	SCOM	Field Mnemonic: Description
25	ROX	CERR1_WRT_BUFFER_CE: Sticky bit for a write buffer CE (FIR 45).
26	ROX	CERR1_WRT_BUFFER_UE: Sticky bit for a write buffer UE (FIR 46).
27	ROX	CERR1_WRT_BUFFER_SUE: Sticky bit for a write buffer SUE (FIR 47).
28:31	RO	Constant = 0b0000
32	ROX	CERR1_READ_CONTROL_OVERFLOW_ERROR: Sticky bit for a read buffer overflow error (FIR 56).
33:39	RO	Constant = 0b0000000
40	ROX	CERR1_WRITE_ECC_DATAPATH_ERROR: Sticky bit for a write ECC datapath parity error (FIR 55).
41:63	RO	Constant = 0b00000000000000000000000

Register Name	Hardware Mark Store Rank 0 Register
Mnemonic	MC01.PORT0.ECC64.SCOM.HWMS0
Address	0000000007010A10 (SCOM)
Description	Hardware mark store rank 0

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	HWMS0_CHIPMARK: Hardware chipmark (Galois field code) for rank 0.
8	RWX	HWMS0_CONFIRMED: Chipmark confirmed.
9	RW	HWMS0_EXIT_1: When set, bypass-enabled reads using this mark use exit 1; otherwise, they use exit 0.

Register Name	Hardware Mark Store Rank 1 Register
Mnemonic	MC01.PORT0.ECC64.SCOM.HWMS1
Address	0000000007010A11 (SCOM)
Description	Hardware mark store rank 1

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	HWMS1_CHIPMARK: Hardware chipmark (Galois field code) for rank 1.
8	RWX	HWMS1_CONFIRMED: Chipmark confirmed.
9	RW	HWMS1_EXIT_1: When set, bypass-enabled reads using this mark use exit 1; otherwise, they use exit 0.

Register Name	Hardware Mark Store Rank 2 Register
Mnemonic	MC01.PORT0.ECC64.SCOM.HWMS2
Address	0000000007010A12 (SCOM)
Description	Hardware mark store rank 2

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	HWMS2_CHIPMARK: Hardware chipmark (Galois field code) for rank 2.
8	RWX	HWMS2_CONFIRMED: Chipmark confirmed.
9	RW	HWMS2_EXIT_1: When set, bypass-enabled reads using this mark use exit 1; otherwise, they use exit 0.

Register Name	Hardware Mark Store Rank 3 Register
Mnemonic	MC01.PORT0.ECC64.SCOM.HWMS3
Address	0000000007010A13 (SCOM)
Description	Hardware mark store rank 3

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	HWMS3_CHIPMARK: Hardware chipmark (Galois field code) for rank 3.
8	RWX	HWMS3_CONFIRMED: Chipmark confirmed.
9	RW	HWMS3_EXIT_1: When set, bypass-enabled reads using this mark use exit 1; otherwise, they use exit 0.

Register Name	Hardware Mark Store Rank 4 Register
Mnemonic	MC01.PORT0.ECC64.SCOM.HWMS4
Address	0000000007010A14 (SCOM)
Description	Hardware mark store rank 4

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	HWMS4_CHIPMARK: Hardware chipmark (Galois field code) for rank 4.
8	RWX	HWMS4_CONFIRMED: Chipmark confirmed.
9	RW	HWMS4_EXIT_1: When set, bypass-enabled reads using this mark use exit 1; otherwise, they use exit 0.

Register Name	Hardware Mark Store Rank 5 Register
Mnemonic	MC01.PORT0.ECC64.SCOM.HWMS5
Address	0000000007010A15 (SCOM)
Description	Hardware mark store rank 5

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	HWMS5_CHIPMARK: Hardware chipmark (Galois field code) for rank 5.
8	RWX	HWMS5_CONFIRMED: Chipmark confirmed.
9	RW	HWMS5_EXIT_1: When set, bypass-enabled reads using this mark use exit 1; otherwise, they use exit 0.

Register Name	Hardware Mark Store Rank 6 Register
Mnemonic	MC01.PORT0.ECC64.SCOM.HWMS6
Address	0000000007010A16 (SCOM)
Description	Hardware mark store rank 6

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	HWMS6_CHIPMARK: Hardware chipmark (Galois field code) for rank 6.
8	RWX	HWMS6_CONFIRMED: Chipmark confirmed.
9	RW	HWMS6_EXIT_1: When set, bypass-enabled reads using this mark use exit 1; otherwise, they use exit 0.

Register Name	**Hardware Mark Store Rank 7 Register**
Mnemonic	MC01.PORT0.ECC64.SCOM.HWMS7
Address	0000000007010A17 (SCOM)
Description	Hardware mark store rank 7

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	HWMS7_CHIPMARK: Hardware chipmark (Galois field code) for rank 7.
8	RWX	HWMS7_CONFIRMED: Chipmark confirmed.
9	RW	HWMS7_EXIT_1: When set, bypass-enabled reads using this mark use exit 1; otherwise, they use exit 0.

Register Name	**Firmware Mark Store 0 Register**
Mnemonic	MC01.PORT0.ECC64.SCOM.FWMS0
Address	0000000007010A18 (SCOM)
Description	Firmware mark store 0

Bits	SCOM	Field Mnemonic: Description
0:7	RW	FWMS0_MARK: Mark (Galois field code).
8	RW	FWMS0_TYPE: Mark type.
9:11	RW	FWMS0_REGION: Selects the mark region (address range to which the mark applies).
12:22	RW	FWMS0_ADDRESS: Mark region address. bit 12 = DIMM bits 13:14 = mrank bits 15:17 = srank bits 18:19 = bank group bits 20:22 = bank (reserving space for 32 total banks)
23	RW	FWMS0_EXIT_1: When set, bypass-enabled reads using this mark use exit 1.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	**Firmware Mark Store 1 Register**
Mnemonic	MC01.PORT0.ECC64.SCOM.FWMS1
Address	0000000007010A19 (SCOM)
Description	Firmware mark store 1

Bits	SCOM	Field Mnemonic: Description
0:7	RW	FWMS1_MARK: Mark (Galois field code).
8	RW	FWMS1_TYPE: Mark type.
9:11	RW	FWMS1_REGION: Selects the mark region (address range to which the mark applies).
12:22	RW	FWMS1_ADDRESS: Mark region address. bit 12 = DIMM bits 13:14 = mrank bits 15:17 = srank bits 18:19 = bank group bits 20:22 = bank (reserving space for 32 total banks)
23	RW	FWMS1_EXIT_1: When set, bypass-enabled reads using this mark use exit 1.

Bits	SCOM	Field Mnemonic: Description
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Firmware Mark Store 2 Register
Mnemonic	MC01.PORT0.ECC64.SCOM.FWMS2
Address	0000000007010A1A (SCOM)
Description	Firmware mark store 2

Bits	SCOM	Field Mnemonic: Description
0:7	RW	FWMS2_MARK: Mark (Galois field code).
8	RW	FWMS2_TYPE: Mark type.
9:11	RW	FWMS2_REGION: Selects the mark region (address range to which the mark applies).
12:22	RW	FWMS2_ADDRESS: Mark region address. bit 12 = DIMM bits 13:14 = mrank bits 15:17 = srank bits 18:19 = bank group bits 20:22 = bank (reserving space for 32 total banks)
23	RW	FWMS2_EXIT_1: When set, bypass-enabled reads using this mark use exit 1.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Firmware Mark Store 3 Register
Mnemonic	MC01.PORT0.ECC64.SCOM.FWMS3
Address	0000000007010A1B (SCOM)
Description	Firmware mark store 3

Bits	SCOM	Field Mnemonic: Description
0:7	RW	FWMS3_MARK: Mark (Galois field code).
8	RW	FWMS3_TYPE: Mark type.
9:11	RW	FWMS3_REGION: Selects the mark region (address range to which the mark applies).
12:22	RW	FWMS3_ADDRESS: Mark region address. bit 12 = DIMM bits 13:14 = mrank bits 15:17 = srank bits 18:19 = bank group bits 20:22 = bank (reserving space for 32 total banks)
23	RW	FWMS3_EXIT_1: When set, bypass-enabled reads using this mark use exit 1.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Firmware Mark Store 4 Register
Mnemonic	MC01.PORT0.ECC64.SCOM.FWMS4
Address	0000000007010A1C (SCOM)
Description	Firmware mark store 4

Bits	SCOM	Field Mnemonic: Description
0:7	RW	FWMS4_MARK: Mark (Galois field code).
8	RW	FWMS4_TYPE: Mark type.
9:11	RW	FWMS4_REGION: Selects the mark region (address range to which the mark applies).
12:22	RW	FWMS4_ADDRESS: Mark region address. bit 12 = DIMM bits 13:14 = mrank bits 15:17 = srank bits 18:19 = bank group bits 20:22 = bank (reserving space for 32 total banks)
23	RW	FWMS4_EXIT_1: When set, bypass-enabled reads using this mark use exit 1.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Firmware Mark Store 5 Register
Mnemonic	MC01.PORT0.ECC64.SCOM.FWMS5
Address	0000000007010A1D (SCOM)
Description	Firmware mark store 5

Bits	SCOM	Field Mnemonic: Description
0:7	RW	FWMS5_MARK: Mark (Galois field code).
8	RW	FWMS5_TYPE: Mark type.
9:11	RW	FWMS5_REGION: Selects the mark region (address range to which the mark applies).
12:22	RW	FWMS5_ADDRESS: Mark region address. bit 12 = DIMM bits 13:14 = mrank bits 15:17 = srank bits 18:19 = bank group bits 20:22 = bank (reserving space for 32 total banks)
23	RW	FWMS5_EXIT_1: When set, bypass-enabled reads using this mark use exit 1.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Firmware Mark Store 6 Register
Mnemonic	MC01.PORT0.ECC64.SCOM.FWMS6
Address	0000000007010A1E (SCOM)
Description	Firmware mark store 6

Bits	SCOM	Field Mnemonic: Description
0:7	RW	FWMS6_MARK: Mark (Galois field code).
8	RW	FWMS6_TYPE: Mark type.
9:11	RW	FWMS6_REGION: Selects the mark region (address range to which the mark applies).

Bits	SCOM	Field Mnemonic: Description
12:22	RW	FWMS6_ADDRESS: Mark region address. bit 12 = DIMM bits 13:14 = mrank bits 15:17 = srank bits 18:19 = bank group bits 20:22 = bank (reserving space for 32 total banks)
23	RW	FWMS6_EXIT_1: When set, bypass-enabled reads using this mark use exit 1.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Firmware Mark Store 7 Register
Mnemonic	MC01.PORT0.ECC64.SCOM.FWMS7
Address	0000000007010A1F (SCOM)
Description	Firmware mark store 7

Bits	SCOM	Field Mnemonic: Description
0:7	RW	FWMS7_MARK: Mark (Galois field code).
8	RW	FWMS7_TYPE: Mark type.
9:11	RW	FWMS7_REGION: Selects the mark region (address range to which the mark applies).
12:22	RW	FWMS7_ADDRESS: Mark region address. bit 12 = DIMM bits 13:14 = mrank bits 15:17 = srank bits 18:19 = bank group bits 20:22 = bank (reserving space for 32 total banks)
23	RW	FWMS7_EXIT_1: When set, bypass-enabled reads using this mark use exit 1.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Write ECC Control Register
Mnemonic	MC01.PORT0.ECC64.SCOM.WECR
Address	0000000007010A28 (SCOM)
Description	Write ECC control register

Bits	SCOM	Field Mnemonic: Description
0	RW	MBA_WRD_MODE_CFG_WRD_ECC_CHK_DISABLE: Set to disable 8-byte ECC checking on the WRD data bus.
1	RW	MBA_WRD_MODE_CFG_WRD_ECC_COR_DISABLE: Set to disable 8-byte ECC correction on the WRD data bus.
2	RW	MBA_WRD_MODE_CFG_CRC_MODE_EN: Set to enable CRC generation on write data.
3	RW	MBA_WRD_MODE_CFG_CRC_MODE_X8: Only applies if cfg_crc_mode_en = 1. Set to generate a x8 CRC. Clear to generate a x4 CRC.
4	RW	MBA_WRD_MODE_RESERVED_4: Reserved.
5	RW	MBA_WRD_MODE_CFG_CAW2_CE_UE_ERR_DETECT_EN: Set to disable the internal error check of the memory ECC generator.
6:56	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000

Register Name	Array Access Control Register
Mnemonic	MC01.PORT0.ECC64.SCOM.AACR
Address	0000000007010A29 (SCOM)
Description	Array access control register

Bits	SCOM	Field Mnemonic: Description
0	RW	AACR_BUFFER: Buffer select.
1:9	RWX	AACR_ADDRESS: Array doubleword address.
10	RW	AACR_AUTOINC: When set, the AACR address field is incremented after each access to AAER.
11	RW	AACR_ECCGEN: When set, an 8-byte ECC is generated automatically when writing the AAER (for more information, see 3Array Access ECC Register on page 222) and an 8-byte ECC is checked when reading the array (when reading AADR). When not set, an ECC is not generated or checked.
12:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	Array Access Data Register
Mnemonic	MC01.PORT0.ECC64.SCOM.AADR
Address	0000000007010A2A (SCOM)
Description	Array access data register

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	AADR_DATA: Array data (0:63).

Register Name	Array Access ECC Register
Mnemonic	MC01.PORT0.ECC64.SCOM.AAER
Address	0000000007010A2B (SCOM)
Description	Array access ECC register

Bits	SCOM	Field Mnemonic: Description
0:8	RWX	AAER_TAG_ECC: Array data(64:72). The contents of this register can be in either of two formats: • BUS format: Bit 0 is an I-series tag bit. Bits 1:8 are an 8-byte ECC. • MEM format: Bits 0:7 are memory ECC bits (the “metadata” is in bit 0). Bit 8 is unused (write as 0). Hardware generation of ECC bits for the BUS format is enabled when AACR_ECCGEN = 1. In this mode, the ECC bits 1:8 should be written as 0.

Register Name	MCBIST Compare Mask Register
Mnemonic	MC01.PORT0.ECC64.SCOM.MCBCM
Address	0000000007010A2C (SCOM)
Description	MCBIST compare mask register. This register clears with an MCBIST global reset.

Bits	SCOM	Field Mnemonic: Description
0:39	RWX	MCBCM_MCBIST_HALF_COMPARE_MASK: Specifies data bits to ignore for MCBIST comparison. This mask covers either bits 0:39 or 40:79, configurable by mask_coverage_selector dial.
40	RWX	MCBCM_MCBIST_MASK_COVERAGE_SELECTOR: Specifies the bits covered by the compare mask. If '0', the mask covers bits 0:39; otherwise, bits 40:79.
41	RWX	MCBCM_MCBIST_TRAP_NONSTOP: if '1', MCBIST continues to trap new errors even when storage is full, *overwriting* older errors. If '0', MCBIST stops trapping when storage is full.
42	RWX	MCBCM_MCBIST_TRAP_CE_ENABLE: Enables capturing information for CEs.
43	RWX	MCBCM_MCBIST_TRAP_MPE_ENABLE: Enables capturing information for MPEs.
44	RWX	MCBCM_MCBIST_TRAP_UE_ENABLE: Enables capturing information for UEs.

Register Name	**Maintenance Buffer MDI/SUE State Register**
Mnemonic	MC01.PORT0.ECC64.SCOM.MBMDI
Address	0000000007010A2D (SCOM)
Description	Maintenance Buffer MDI/SUE state

Bits	SCOM	Field Mnemonic: Description
0	RWX	MBMDI_MDI_0: MDI state for the first 64 bytes of the maintenance buffer. Maintenance reads set this bit to '1' if either in-memory MDI bit is '1'. Maintenance writes use this bit and the SUE_0 bit to compute the in-memory MDI bits, unless the ECC override is '1' where the undecoded maintenance buffer content is used.
1	RWX	MBMDI_SUE_0: SUE state for the first 64 bytes of the maintenance buffer. Maintenance reads set this bit to '1' if the in-memory MDI bits differ. Maintenance writes use this bit and the MDI_0 bit to compute the in-memory MDI bits, unless the ECC override is '1' where the undecoded maintenance buffer content is used.
2	RWX	MBMDI_MDI_1: MDI state for the second 64 bytes of the maintenance buffer. Maintenance reads set this bit to '1' if either in-memory MDI bit is '1'. Maintenance writes use this bit and the SUE_0 bit to compute the in-memory MDI bits, unless the ECC override is '1' where the undecoded maintenance buffer content is used.
3	RWX	MBMDI_SUE_1: SUE state for the second 64 bytes of the maintenance buffer. Maintenance reads set this bit to '1' if the in-memory MDI bits differ. Maintenance writes use this bit and the MDI_1 bit to compute the in-memory MDI bits, unless the ECC override is '1' where the undecoded maintenance buffer content is used.

Register Name	**Write ECC Syndrome Register**
Mnemonic	MC01.PORT0.ECC64.SCOM.WESR
Address	0000000007010A2E (SCOM)
Description	The Write ECC Syndrome Register (WESR) contains additional hardware debug information.

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	WESR_SYNDROME: Traps an 8-byte ECC syndrome on the last WRD CAW2 errors.
8:9	ROX	WESR_WHICH_8BECK: Indicates which 8-byte ECC checker's syndrome was trapped. 00 = Doubleword 04 checker 01 = Doubleword 15 checker 10 = Doubleword 26 checker 11 = Doubleword 37 checker For multiple fails, trap priority goes to 00 first, 11 last.
10	ROX	WESR_PAR_ERR_ONLY: Indicates that no 8-byte ECC error was detected and this CAW2 error was triggered by parity on non-data bits.

Register Name	Error Log Pointer Register
Mnemonic	MC01.PORT0.ECC64.CNTL.ELPR
Address	0000000007010A2F (SCOM)
Description	Provides a readout of the current error-log write pointer and a full/wrap indicator bit. The ELPR is not writable, but is cleared when MCB_CNTLQ[7] = 1 (dial MCB_CNTLQ_MCB_RESET_ERROR_LOGS).

Bits	SCOM	Field Mnemonic: Description
0	ROX	ELPR_LOG_FULL: The log is full. Distinguishes empty from exactly 64 entries.
1	RO	Constant = 0b0
2:7	ROX	ELPR_LOG_POINTER: Log pointer to the next entry to be written.

Register Name	WDF Buffer Miscellaneous Configuration Register
Mnemonic	MC01.PORT0.WDF.WDFCFG
Address	0000000007010A30 (SCOM)
Description	WDF buffer miscellaneous configuration

Bits	SCOM	Field Mnemonic: Description
0	RW	CFG_WRITE_MODE_ECC_CHK_DIS: Disables 8-byte ECC checking on WDF-buffer read ports.
1	RW	CFG_WRITE_MODE_ECC_COR_DIS: Disables 8-byte ECC correction on WDF-buffer read ports.
2	RW	CFG_WDF_SERIAL_SEQ_MODE: Puts the six PW sequencers into a serial mode of operation; no overlap.
3	RW	RESET_KEEPER: Reset miscellaneous c_err_rpt keepers in the write buffer logic.
4:7	RW	MERGE_CAPACITY_LIMIT: Sets the capacity limit for the merge asynchronous buffer. Valid values are 0 - 8.
8:11	RW	WDFCFG_8_11_SPARE: Spare bits.
12:17	RW	ASYNC_INJ: asynchronous Error inject.
18:31	RW	WDFCFG_18_31_SPARE: Spare bits.
32:35	RW	ECC_WDF_HCA_TIMEBASE_SELECT: HCA time base select.
36:63	RW	ECC_WDF_HCA_TIMEBASE: HCA time base.

Register Name	Write Buffer WRQ Register
Mnemonic	MC01.PORT0.WDF.WRT_ECC
Address	0000000007010A31 (SCOM)
Description	Port ECC error information register

Bits	SCOM	Field Mnemonic: Description
0:2	RWX_WCLRPART	WRT_ECC_DW0_ERR_TYPE: The ECC checker detected the following types of errors in write buffer WRQ read-port doubleword 0: bit 0 = CE bit 1 = UE bit 2 = SUE
3:7	RO	Constant = 0b00000
8:15	RWX_WCLRPART	WRT_ECC_DW0_SYNDROME: Write buffer WRQ read port doubleword 0 ECC checker syndrome.

Bits	SCOM	Field Mnemonic: Description
16:18	RWX_WCLRPART	WRT_ECC_DW1_ERR_TYPE: The ECC checker detected the following types of errors in write buffer WRQ read port doubleword 1: bit 0 = CE bit 1 = UE bit 2 = SUE
19:23	RO	Constant = 0b00000
24:31	RWX_WCLRPART	WRT_ECC_DW1_SYNDROME: Write buffer WRQ read port doubleword 1 ECC checker syndrome.
32:34	RWX_WCLRPART	WRT_ECC_DW2_ERR_TYPE: The ECC checker detected the following types of errors in write buffer WRQ read port doubleword 2: bit 0 = CE bit 1 = UE bit 2 = SUE
35:39	RO	Constant = 0b00000
40:47	RWX_WCLRPART	WRT_ECC_DW2_SYNDROME: Write buffer WRQ read port doubleword 2 ECC checker syndrome.
48:50	RWX_WCLRPART	WRT_ECC_DW3_ERR_TYPE: The ECC checker detected the following types of errors in write buffer WRQ read port doubleword 3: bit 0 = CE bit 1 = UE bit 2 = SUE
51:55	RO	Constant = 0b00000
56:63	RWX_WCLRPART	WRT_ECC_DW3_SYNDROME: Write buffer WRQ read port doubleword 3 ECC checker syndrome.

Register Name	WDF HCA Accumulator Register
Mnemonic	MC01.PORT0.WDF.HCA_ACCUM_REG
Address	0000000007010A32 (SCOM)
Description	WDF HCA accumulator register

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	ACCUM_REG: WDF HCA accumulator data.

Register Name	WDF Tag Overrun Information Register
Mnemonic	MC01.PORT0.WDF.WBMGR_TAG_INFO
Address	0000000007010A33 (SCOM)
Description	WDF tag overrun information

Bits	SCOM	Field Mnemonic: Description
0	RWX	BUFFER_OVERRUN: WDF buffer overrun indicator.
1	RWX	TAG_OVERRUN: WDF tag overrun indicator.
2	RWX	REL_TAG_ASYNC_PARITY_ERROR: WDF ERL tag parity error indicator.
3	RWX	REL_TAG_ASYNC_SEQUENCE_ERROR: WDF ERL tag sequence error indicator.
4	RWX	REL_MERGE_TAG_ASYNC_PARITY_ERROR: WDF ERL tag parity error indicator.

Bits	SCOM	Field Mnemonic: Description
5	RWX	REL_MERGE_TAG_ASYNC_SEQUENCE_ERROR: WDF ERL tag sequence error indicator.
6:12	RWX	TAG_INFORMATION: WDF tag overrun information.
13:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000

Register Name	WDF Debug Control Register
Mnemonic	MC01.PORT0.WDF.WDFDBG
Address	0000000007010A34 (SCOM)
Description	WDF debug control

Bits	SCOM	Field Mnemonic: Description
0	RW	DBG_SEL_IN: Indicates that wdf_a_debug_in should be driven to wdf_a_debug_out.
1	RW	DBG_SEL_WDF: Indicates that internal debug data should be driven to wdf_a_debug_out.
2	RW	DBG_SEL_PWSEQ0_DEBUG_0: Indicates that internal debug data pwseq0_debug_0 should be driven to wdf_a_debug_out.
3	RW	DBG_SEL_PWSEQ0_DEBUG_1: Indicates that internal debug data pwseq0_debug_1 should be driven to wdf_a_debug_out.
4	RW	DBG_SEL_PWSEQ1_DEBUG_0: Indicates that internal debug data pwseq1_debug_0 should be driven to wdf_a_debug_out.
5	RW	DBG_SEL_PWSEQ1_DEBUG_1: Indicates that internal debug data pwseq1_debug_1 should be driven to wdf_a_debug_out.
6	RW	DBG_SEL_PWSEQ2_DEBUG_0: Indicates that internal debug data pwseq2_debug_0 should be driven to wdf_a_debug_out.
7	RW	DBG_SEL_PWSEQ2_DEBUG_1: Indicates that internal debug data pwseq2_debug_1 should be driven to wdf_a_debug_out.
8	RW	DBG_SEL_PWSEQ3_DEBUG_0: Indicates that internal debug data pwseq3_debug_0 should be driven to wdf_a_debug_out.
9	RW	DBG_SEL_PWSEQ3_DEBUG_1: Indicates that internal debug data pwseq3_debug_1 should be driven to wdf_a_debug_out.
10	RW	DBG_SEL_PWSEQ4_DEBUG_0: Indicates that internal debug data pwseq4_debug_0 should be driven to wdf_a_debug_out.
11	RW	DBG_SEL_PWSEQ4_DEBUG_1: Indicates that internal debug data pwseq4_debug_1 should be driven to wdf_a_debug_out.
12	RW	DBG_SEL_PWSEQ5_DEBUG_0: Indicates that internal debug data pwseq5_debug_0 should be driven to wdf_a_debug_out.
13	RW	DBG_SEL_PWSEQ5_DEBUG_1: Indicates that internal debug data pwseq5_debug_1 should be driven to wdf_a_debug_out.
14	RW	DBG_SEL_PWCTL_DEBUG: Indicates that internal debug data pwctl_debug should be driven to wdf_a_debug_out.
15	RW	DBG_SEL_WDFMGR_DEBUG: Indicates that internal debug data wdfmgr_debug should be driven to wdf_a_debug_out.
16	RW	DBG_SEL_WDFRD_DEBUG_0: Indicates that internal debug data wdfrd_debug_0 should be driven to wdf_a_debug_out.
17	RW	DBG_SEL_WDFRD_DEBUG_1: Indicates that internal debug data wdfrd_debug_1 should be driven to wdf_a_debug_out.

Bits	SCOM	Field Mnemonic: Description
18	RW	DBG_SEL_WDFWR_DEBUG_0: Indicates that internal debug data wdfwr_debug_0 should be driven to wdf_a_debug_out.
19	RW	DBG_SEL_WDFWR_DEBUG_1: Indicates that internal debug data wdfwr_debug_1 should be driven to wdf_a_debug_out.
20	RW	DBG_SEL_SEC_WDFRD_DEBUG_0: Indicates that internal debug data sec_wdfrd_debug_0 should be driven to wdf_a_debug_out.
21	RW	DBG_SEL_SEC_WDFRD_DEBUG_1: Indicates that internal debug data sec_wdfrd_debug_1 should be driven to wdf_a_debug_out.
22:31	RW	DBG_SPARE: Spare bits.
32	RW	WAT_EVENT_ENABLE: Enable latching of wat_event_in.
33:35	RW	WAT_SPARE1: WAT spare.
36:39	RW	WAT0_EVENT_SELECT: Select for wat_action(0).
40:43	RW	WAT1_EVENT_SELECT: Select for wat_action(1).
44:63	RO	Constant = 0b00000000000000000000

Register Name	Write Buffer Miscellaneous Configuration Register
Mnemonic	MC01.PORT0.WRITE.WRTCFG
Address	0000000007010A38 (SCOM)
Description	Write buffer miscellaneous configuration

Bits	SCOM	Field Mnemonic: Description
0	RW	CFG_WRITE_MODE_ECC_CHK_DIS: Disables 8-byte ECC checking on write-buffer read ports.
1	RW	CFG_WRITE_MODE_ECC_COR_DIS: Disables 8-byte ECC correction on write-buffer read ports.
2	RW	RESET_KEEPER: Reset miscellaneous c_err_rpt keepers in the write buffer logic.
3	RW	MPIPL: mpipl
4:7	RW	ASYNC_INJ: Asynchronous error inject.
8:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	Write Buffer WRQ Register
Mnemonic	MC01.PORT0.WRITE.WRT_ECC
Address	0000000007010A39 (SCOM)
Description	Port ECC error information register

Bits	SCOM	Field Mnemonic: Description
0:2	RWX_WCLRPART	WRT_ECC_DW0_ERR_TYPE: The ECC checker detected the following types of errors in write buffer WRQ read port doubleword 0: bit 0 = CE bit 1 = UE bit 2 = SUE
3:7	RO	Constant = 0b00000
8:15	RWX_WCLRPART	WRT_ECC_DW0_SYNDROME: Write buffer WRQ read port doubleword 0 ECC checker syndrome.

Bits	SCOM	Field Mnemonic: Description
16:18	RWX_WCLRPART	WRT_ECC_DW1_ERR_TYPE: The ECC checker detected the following types of errors in write buffer WRQ read port doubleword 1: bit 0 = CE bit 1 = UE bit 2 = SUE
19:23	RO	Constant = 0b00000
24:31	RWX_WCLRPART	WRT_ECC_DW1_SYNDROME: Write buffer WRQ read port doubleword 1 ECC checker syndrome.
32:34	RWX_WCLRPART	WRT_ECC_DW2_ERR_TYPE: The ECC checker detected the following types of errors in write buffer WRQ read port doubleword 2: bit 0 = CE bit 1 = UE bit 2 = SUE
35:39	RO	Constant = 0b00000
40:47	RWX_WCLRPART	WRT_ECC_DW2_SYNDROME: Write buffer WRQ read port doubleword 2 ECC checker syndrome.
48:50	RWX_WCLRPART	WRT_ECC_DW3_ERR_TYPE: The ECC checker detected the following types of errors in write buffer WRQ read port doubleword 3: bit 0 = CE bit 1 = UE bit 2 = SUE
51:55	RO	Constant = 0b00000
56:63	RWX_WCLRPART	WRT_ECC_DW3_SYNDROME: Write buffer WRQ read port doubleword 3 ECC checker syndrome.

Register Name	WRT MCA Debug Control Register
Mnemonic	MC01.PORT0.WRITE.WRTDBGMCA
Address	0000000007010A3A (SCOM)
Description	WRT MCA Debug Control

Bits	SCOM	Field Mnemonic: Description
0	RW	MCA_DBG_SEL_IN: Indicates that write_a_debug_in should be driven to write_a_debug_out.
1	RW	MCA_DBG_SEL_WRT: Indicates that internal debug data should be driven to write_a_debug_out.
2	RW	WBRD_DEBUG_0_SELECT: Indicates that internal debug data wbrd_debug_0 should be driven to write_a_debug_out.
3	RW	WBRD_DEBUG_1_SELECT: Indicates that internal debug data wbrd_debug_1 should be driven to write_a_debug_out.
4	RW	SEC_WBRD_DEBUG_0_SELECT: Indicates that internal debug data sec_wbrd_debug_0 should be driven to write_a_debug_out.
5	RW	SEC_WBRD_DEBUG_1_SELECT: Indicates that internal debug data sec_wbrd_debug_1 should be driven to write_a_debug_out.
6:15	RW	DBG_SPARE_MCA: Spare bits.
16	RW	WAT_EVENT_ENABLE_MCA: Enable latching of wat_event_in.
17:19	RW	WAT_SPARE1_MCA: WAT spare.
20:23	RW	WAT0_EVENT_SELECT_MCA: Select for wat_action(0).

Bits	SCOM	Field Mnemonic: Description
24:27	RW	WAT1_EVENT_SELECT_MCA: Select for wat_action(1).
28:63	RO	Constant = 0b00000000000000000000000000000000000000

Register Name	WRT Nest Debug Control Register
Mnemonic	MC01.PORT0.WRITE.WRTDBGNEST
Address	0000000007010A3B (SCOM)
Description	WRT nest debug control

Bits	SCOM	Field Mnemonic: Description
0	RW	NEST_DBG_SEL_IN: Indicates that write_s_debug_in should be driven to write_s_debug_out.
1	RW	NEST_DBG_SEL_WRT: Indicates that internal debug data should be driven to write_s_debug_out.
2	RW	WBMGR_DBG_0_SELECT: Indicates that internal debug data wbmgr_0_debug should be driven to write_s_debug_out.
3	RW	WBMGR_DBG_1_SELECT: Indicates that internal debug data wbmgr_1_debug should be driven to write_s_debug_out.
4	RW	WRCNTL_DBG_SELECT: Indicates that internal debug data wrcntl_debug should be driven to write_s_debug_out.
5:15	RW	DBG_SPARE_NEST: Spare bits.
16	RW	WAT_EVENT_ENABLE_NEST: Enable latching of wat_event_in.
17:19	RW	WAT_SPARE1_NEST: WAT spare.
20:23	RW	WAT0_EVENT_SELECT_NEST: Select for wat_action(0).
24:27	RW	WAT1_EVENT_SELECT_NEST: Select for wat_action(1).
28:63	RO	Constant = 0b00000000000000000000000000000000000000

Register Name	Datapath Fault Isolation Register
Mnemonic	MC01.PORT1.ECC64.SCOM.FIR
Address	0000000007010A40 (SCOM) 0000000007010A41 (SCOM1) 0000000007010A42 (SCOM2)
Description	Datapath fault isolation register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:7	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_MPE_RANK_0_TO_7: Mark placed error (MPE) detected on a mainline read. The corresponding Hardware Mark Store Register (HWMSx [x = 0..7]) is updated with a chipmark for the associated master rank.
8	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_NCE: New correctable error (NCE) detected on a mainline read.
9	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_TCE: Two-symbol correctable error (TCE) detected on a mainline read.
10	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_SCE: Symbol mark corrected error (SCE) detected on a mainline read.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
11	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_MCE: Chip mark corrected error (MCE) detected on a mainline read.
12	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_SUE: Special uncorrectable error (SUE) detected on a mainline read.
13	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_AUE: Address uncorrectable error (AUE) detected on a mainline read.
14	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_UE: Uncorrectable error (UE) detected on a mainline read.
15	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_RCD: Parity error detected by registering clock driver (RCD) detected on a mainline read.
16	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_IAUE: Intermittent AUE (IAUE) detected on a mainline read.
17	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_IUE: Intermittent UE (IUE) detected on a mainline read.
18	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_IRCD: Intermittent RCD (IRCD) detected on a mainline read.
19	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_IMPE: Intermittent MPE (IMPE) detected on a mainline read.
20:27	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_MPE_RANK_0_TO_7: Mark placed error (MPE) detected on a maintenance read. The corresponding Hardware Mark Store Register (HWMSx [x = 0..7]) is updated with a chipmark for the associated master rank.
28	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_NCE: New correctable error (NCE) detected on a maintenance read.
29	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_TCE: Two-symbol correctable error (TCE) detected on a maintenance read.
30	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_SCE: Symbol mark corrected error (SCE) detected on a maintenance read.
31	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_MCE: Chip mark corrected error (MCE) detected on a maintenance read.
32	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_SUE: Special uncorrectable error (SUE) detected on a maintenance read.
33	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_AUE: Address uncorrectable error (AUE) detected on a maintenance read.
34	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_UE: Uncorrectable error (UE) detected on a maintenance read.
35	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_RCD: Parity error detected by registering clock driver (RCD) detected on a maintenance read.
36	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_IAUE: Intermittent AUE (IAUE) detected on a maintenance read.
37	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_IUE: Intermittent UE (IUE) detected on a maintenance read.
38	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_IRCD: Intermittent RCD (IRCD) detected on a maintenance read.
39	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_IMPE: Intermittent MPE (IMPE) detected on a maintenance read.
40	RWX	WOX_AND	WOX_OR	FIR_RESERVED_40: Reserved.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
41	RWX	WOX_AND	WOX_OR	FIR_SCOM_PARITY_CLASS_STATUS: SCOM register parity error, for registers in the “status” class (no data integrity risk). For more information, see the CERR0 register (page 214.)
42	RWX	WOX_AND	WOX_OR	FIR_SCOM_PARITY_CLASS_RECOVERABLE: SCOM register parity error, for registers in the “recoverable” class (no data integrity risk; register must be reloaded). For more information, see the CERR0 register (page 214.)
43	RWX	WOX_AND	WOX_OR	FIR_SCOM_PARITY_CLASS_UNRECOVERABLE: SCOM register parity error, for registers in the “unrecoverable” class (data integrity risk). For more information, see the CERR0 register (page 214.)
44	RWX	WOX_AND	WOX_OR	FIR_ECC_CORRECTOR_INTERNAL_PARITY_ERROR: ECC corrector internal parity error (data integrity risk). For more information, see the CERR1 register (page 215).
45	RWX	WOX_AND	WOX_OR	FIR_WRITE_RMW_CE: CE detected at the write or RMW buffer read port. For more information, see the CERR1 and WRT_ECC registers (pages 215 and 227).
46	RWX	WOX_AND	WOX_OR	FIR_WRITE_RMW_UE: UE detected at the write or RMW buffer read port. For more information, see the CERR1 and WRT_ECC registers (pages 215 and 227).
47	RWX	WOX_AND	WOX_OR	FIR_WRITE_RMW_SUE: SUE detected at the write or RMW buffer read port. For more information, see the CERR1 and WRT_ECC registers (pages 215 and 227).
48	RWX	WOX_AND	WOX_OR	FIR_WDF_OVERRUN_ERROR_0: WDF logic detected a buffer overrun error (class 0).
49	RWX	WOX_AND	WOX_OR	FIR_WDF_OVERRUN_ERROR_1: WDF logic detected a buffer overrun error (class 1).
50	RWX	WOX_AND	WOX_OR	FIR_WDF_SCOM_SEQUENCE_ERROR: WDF logic detected a SCOM sequence error.
51	RWX	WOX_AND	WOX_OR	FIR_WDF_STATE_MACHINE_ERROR: WDF logic detected a state machine error.
52	RWX	WOX_AND	WOX_OR	FIR_WDF_MISC_REGISTER_PARITY_ERROR: WDF logic detected a miscellaneous register parity error.
53	RWX	WOX_AND	WOX_OR	FIR_WRT_SCOM_SEQUENCE_ERROR: WRT logic detected a SCOM sequence error.
54	RWX	WOX_AND	WOX_OR	FIR_WRT_MISC_REGISTER_PARITY_ERROR: WRT logic detected a miscellaneous register parity error.
55	RWX	WOX_AND	WOX_OR	FIR_ECC_GENERATOR_INTERNAL_PARITY_ERROR: ECC generator internal parity error (data integrity risk).
56	RWX	WOX_AND	WOX_OR	FIR_READ_BUFFER_OVERFLOW_ERROR: Read buffer overflow error (data integrity risk).
57	RWX	WOX_AND	WOX_OR	FIR_WDF_ASYNC_INTERFACE_ERROR: WDF asynchronous interface error.
58	RWX	WOX_AND	WOX_OR	FIR_READ_ASYNC_INTERFACE_PARITY_ERROR: READ asynchronous interface parity error.
59	RWX	WOX_AND	WOX_OR	FIR_READ_ASYNC_INTERFACE_SEQUENCE_ERROR: READ asynchronous interface sequence error.
60:61	RWX	WOX_AND	WOX_OR	FIR_RESERVED: Reserved.
62	RWX	WOX_AND	WOX_OR	FIR_INTERNAL_SCOM_ERROR: A SCOM/FIR internal error has occurred.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
63	RWX	WOX_AND	WOX_OR	FIR_INTERNAL_SCOM_ERROR_COPY: A SCOM/FIR internal error has occurred (redundant copy).

Register Name	Datapath FIR Mask Register
Mnemonic	MC01.PORT1.ECC64.SCOM.MASK
Address	0000000007010A43 (SCOM) 0000000007010A44 (SCOM1) 0000000007010A45 (SCOM2)
Description	Datapath FIR mask

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:63	RW	WO_AND	WO_OR	MASK_FIR_MASK: MASK for FIR bits 0:63.

Register Name	Datapath FIR Action 0 Register
Mnemonic	MC01.PORT1.ECC64.SCOM.ACTION0
Address	0000000007010A46 (SCOM)
Description	Datapath FIR action 0

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ACTION0_FIR_ACTION0: Action0 select for the corresponding bits in the FIR. (Action0, Action1, Mask) selects: (0,0,0) = Checkstop error (0,1,0) = Recoverable error (1,0,0) = Attention (1,1,0) = Local checkstop error (X,X,1) = Masked

Register Name	Datapath FIR Action 1 Register
Mnemonic	MC01.PORT1.ECC64.SCOM.ACTION1
Address	0000000007010A47 (SCOM)
Description	Datapath FIR action 1

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ACTION1_FIR_ACTION1: Action1 select for the corresponding bits in the FIR. (Action0, Action1, Mask) selects: (0,0,0) = Checkstop error (0,1,0) = Recoverable error (1,0,0) = Attention (1,1,0) = Local checkstop error (X,X,1) = Masked

Register Name	Datapath FIR “Who is On First” Register
Mnemonic	MC01.PORT1.ECC64.SCOM.WOF
Address	0000000007010A48 (SCOM)
Description	Datapath FIR 'Who is On First'

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	WOF_FIR_WOF: The WOF register locks on the first error. Writing zeros the register.

Register Name	Read ECC Control Register
Mnemonic	MC01.PORT1.ECC64.SCOM.RECR
Address	0000000007010A4A (SCOM)
Description	Read ECC control register

Bits	SCOM	Field Mnemonic: Description
0	RW	MBSECCQ_DISABLE_MEMORY_ECC_CHECK_CORRECT: When set, memory ECC check and correct is disabled. When memory ECC checking is disabled, the SUE injecting into the 8-byte data bus ECC is also disabled.
1	RW	MBSECCQ_DISABLE_MEMORY_ECC_CORRECT: When set, memory ECC correct is disabled (memory ECC checking is not disabled).
2	RW	MBSECCQ_DISABLE_MARK_STORE_WRITE: Disables update of the HWMSx registers on an MPE.
3	RW	MBSECCQ_DISABLE_UE_RETRY: When off, a read diagnosed as an exit-point-2 uncorrectable error (UE, AUE, or RCD) is retried. The FIR is set if the problem reoccurs on the retry. If the problem does not reoccur, the IUE/IAUE/IRCD FIR is set. When on, the UE/AUE/RCD FIRs are set immediately, and the IUE/IAUE/IRCD FIRs are not set.
4	RW	MBSECCQ_ITAG_METADATA_ENABLE: Enables I-series tag bits in the metadata symbols. When this dial is not set, the tag bits are used as four additional check bits.
5	RW	MBSECCQ_SLOW_EXIT_REDUCTION: When set, exit selection is modified to prevent the pileup of output data beats by choosing a later exit than would normally be used. Latency is increased. This mode is intended as a workaround to potential read_mac asynchronous interface issues.
6:8	RW	MBSECCQ_READ_POINTER_DELAY: Read pointer delay (mba_mbx_rdtag_val to mbr_ddr_clock_en) is (dial value + 2) MEMx2 cycles. This field interacts with MBSECCQ_ECC_SCHEDULER_DELAY according to the following formula: rdptrdly + 3 + (staging latches to PHY on mbr_ddr_* and from PHY on ddr_mbr_rdata) = scheddly + 7 Both rdptrdly and scheddly must be in the range 0 - 7.
9:10	RW	MBSECCQ_EXIT_OVERRIDE: Non-zero settings are for debug operation only.
11	RW	MBSECCQ_HWMARK_EXIT1: Selects the value to which HWMSx(9) [exit_1] is set when hardware sets a chipmark.

Bits	SCOM	Field Mnemonic: Description
12	RW	MBSECCQ_DATA_GENERATOR_OVERRIDE: Also known as “wrap mode.” When set, overrides ECC corrector data output with an address-based data pattern. In each doubleword: bits (0:15) = 0xdead bits (16:19) = port index (0..7) bits (20:22) = 0 bit (23) = DIMM bits (24:25) = master rank bits (26:28) = slave rank bits (29:30) = bank group bits (31:33) = bank bits (34:51) = row (0:17) bits (52:59) = col (2:9) bits (60:63) = doubleword index (0 to 3) Metadata (I-series tags and MDI bit) will be zero. **Note**: Wrap mode also requires Exit_Override set to 0b01 (force_exit_0).
13:15	RW	MBSECCQ_ECC_SCHEDULER_DELAY: ECC scheduler delay (mba_mbx_rdtag_val to scheduler start). See MBSECCQ_Read_Pointer_Delay (6:8).
16:18	RW	MBSECCQ_VAL_TO_DATA_DELAY: Asynchronous side 2x cycle delay from ecc_tag_valid_rd to data valid. Affects the asynchronous interface.
19	RW	MBSECCQ_DELAY_VALID_1X: When set, read control delays ecc_tag_valid_rd by one MCA 1x cycle. In effect, it subtracts 0.5 from val_to_data_delay.
20:21	RW	MBSECCQ_NEST_VAL_TO_DATA_DELAY: Number of extra nest cycles of delay from tag to data. The valid range is 0 - 2. Affects the asynchronous interface.
22	RW	MBSECCQ_DELAY_NONBYPASS: When set, adds one extra nest cycle delay for nonbypass data (needed for the null_xfer/retry signal).
23	RW	MBSECCQ_ENABLE_SPECIAL_ATTENTION: When set, FIRs with action set to 10 assert special_attention.
24	RW	MBSECCQ_ENABLE_HOST_ATTENTION: When set, FIRs with action set to 10 assert host_attention.
25	RW	MBSECCQ_DISABLE_MPE_CONFIRM: When set, hardware marks are placed in the confirmed state.
26	RW	MBSECCQ_ENABLE_UE_NOISE_WINDOW: Enables noise window processing whenever a UE (or AUE) is detected.
27	RW	MBSECCQ_ENABLE_TCE_CORRECTION: Enables two-symbol error correction.
28	RW	MBSECCQ_ENABLE_CHIPMARKED_SCE_NCE: Enables correction of a marked symbol, and one unmarked symbol, when there is a chip mark (but no error in the marked chip).
29	RW	MBSECCQ_USE_ADDRESS_HASH: Enables use of an address hash in the ECC.
30:31	RW	MBSECCQ_DATA_INVERSION: Controls inversion of data to or from the PHY. Data and checks (including metadata) can be inverted for data beats where col(2) = 1. Alternatively, data can be set to always invert, while checks invert where col(2) = 1.
32	RW	MBSECCQ_DISABLE_PIPE_NOERR_CLOCK_GATING: Disables these no-err/no-change clock gating features in the ECC pipe: 1. Mark precomputation is normally held while marks remain the same (for example, all-0). 2. Post-syndrome ECC computation stages are held while there is no new error.
33	RW	MBSECCQ_MAINT_NO_RETRY_UE: Maintenance equivalent of Disable_ue_retry (bit 3).
34	RW	MBSECCQ_MAINT_NO_RETRY_MPE: Maintenance equivalent of disable_MPE_confirm (bit 25).
35	RW	MBSECCQ_DISABLE_BYPASS_TEMPLATE_A: Disables least-latency mode for 128-byte bypass reads, so that beat 1 will have an SUE in case of a bypass error on beat 0.
36:43	RW	MBSECCQ_RESERVED_36_43: Reserved.

Register Name	ECC Debug/WAT Control Register
Mnemonic	MC01.PORT1.ECC64.SCOM.DBGR
Address	0000000007010A4B (SCOM)
Description	ECC Debug/WAT control register

Bits	SCOM	Field Mnemonic: Description
0	RW	DBGR_ECC_DEBUG_ENABLE: Enable the debug bus in the ecc64 macro. Required for debug of ECC64 or SRQ.
1:2	RW	DBGR_ECC_DEBUG_CHUNK_SELECT: Select 0, 1, 2, or 4 22-bit data chunks from ECC debug sources. ECC data is inserted in the debug bus as follows: 00 = inp inp inp inp 01 = inp inp inp ecc 10 = inp inp ecc ecc 11 = ecc ecc ecc ecc Other fields of the debug bus output propagate the input (inp).
3:5	RW	DBGR_ECC_DEBUG_PRIMARY_SELECT: Primary select for the ECC debug source. 000 = sch1 sch2 ep21 ep22 / - - ep21 ep22 / - - - ep22 001 = sch1 sch2 ep22 ep21 / - - ep22 ep21 / - - - ep21 010 = ep21 ep22 wrd1 wrd2 / - - wrd1 wrd2 / - - - wrd2 011 = ep21 ep22 wrd2 wrd1 / - - wrd2 wrd1 / - - - wrd1 100 = wrd1 wrd2 sch1 sch2 / - - sch1 sch2 / - - - sch2 101 = wrd1 wrd2 sch2 sch1 / - - sch2 sch1 / - - - sch1 where: sch1 and sch2 are collections of debug information for the ECC corrector's scheduler logic. ep21 and ep22 are collections of debug information related to the exit-point-2 state logic. wrd1 and wrd2 are collections of debug information related to the write data logic.
6:7	RW	DBGR_ECC_DEBUG_SECONDARY_SELECT: Secondary select for the ECC debug data. Action varies by the primary source bus.
8	RW	DBGR_ECC_WAT_ENABLE: Enable workaround logic in the ECC corrector.
9	RW	DBGR_ECC_WAT_ACTION_SELECT: Select the workaround action: 0 = Bypass disable (while the selected WAT event is 1). 1 = Force exit 2 (while the selected WAT event is 1).
10:11	RW	DBGR_ECC_WAT_SOURCE: Select the WAT event (bit 0 to 3).
12:14	RW	DBGR_READ_DEBUG_SELECT: Select the debug source data in the read macro.

Register Name	Mark Shadow Register
Mnemonic	MC01.PORT1.ECC64.SCOM.MSR
Address	0000000007010A4C (SCOM)
Description	Mark Shadow Register

Bits	SCOM	Field Mnemonic: Description
0:7	RO	Constant = 0b00000000
8:15	ROX	MSR_CHIPMARK: Mark the location (Galois field code) of the last mark placed (includes unconfirmed marks).
16:18	ROX	MSR_RANK: Rank of the last mark placed (includes unconfirmed marks).
19:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000

Register Name	Error Inject Control Register
Mnemonic	MC01.PORT1.ECC64.SCOM.EICR
Address	0000000007010A4D (SCOM)
Description	Error Inject Control Register

Bits	SCOM	Field Mnemonic: Description
0:36	RW	EICR_ADDRESS: An error is injected when the read address matches the EICR address, up to the fields masked by the EICR region. bit 0 = DIMM select bits 1:2 = mrank(0:1) bits 3:5 = srank(0:2) bits 6:7 = bank_group(0:1) bits 8:10 = bank(0:2) bits 11:28 = row(0:17) bits 29:36 = col(2:9)
37	RW	EICR_RESERVED: Reserved.
38:39	RW	EICR_PERSIST: Persistence of the injected error. Set to disabled (00) to disable error injection. It affects the memory ECC error injection selected via the type field, or miscellaneous injection via the MISC field.
40:42	RW	EICR_REGION: Address region size for error inject.
43:47	RW	EICR_TYPE: Bit mask for the error type to inject. bit 43 = Inject address UE bit 44 = Inject DQ 0 (symbol 71, Galois code 0x38) bit 45 = Inject DQ 1 (symbol 70, Galois code 0xa2) bit 46 = Inject DQ 4 (symbol 39, Galois code 0x46) bit 47 = Inject DQ 5,6 (symbols 38,37, Galois codes 0x1d, x0f4)
48:51	RW	EICR_MISC: Selects miscellaneous error injections: • 8-byte ECC error injection at the output of the memory ECC checker. Inject a CE in bit 0 or bit 1, or a UE in both bits. Any data read from memory into either the RMW buffer or READ buffer will be injected. Errors should be visible in RMW ECC checkers or in the read master's ECC checkers. • Inject FIR(44) = ecc_corrector_internal_parity_error. • Inject read path asynchronous interface errors (parity or sequence_check). Miscellaneous errors are not affected by the address or region, but are affected by persistence (both soft_error and hard_error persistence act as a continuous inject). Undefined codes inject no error.

Register Name	Error Report Hold Register 0 (SCOM Register Parity Errors)
Mnemonic	MC01.PORT1.ECC64.SCOM.CERR0
Address	0000000007010A4E (SCOM)
Description	Each register parity error is reported in the bit location corresponding to the least-significant 6 bits of the register's SCOM address. Writing the CERR0 register clears all hold bits in CERR0 and CERR1.

Bits	SCOM	Field Mnemonic: Description
0:9	RO	Constant = 0b0000000000
10	RWX_WCLRREG	CERR0_RECR_PE: RECR parity error (FIR 43).
11	RO	Constant = 0b0

Bits	SCOM	Field Mnemonic: Description
12	RWX_WCLRREG	CERR0_MSR_PE: MSR parity error (FIR 41).
13	RWX_WCLRREG	CERR0_EICR_PE: EICR parity error (FIR 42).
14:15	RO	Constant = 0b00
16:23	RWX_WCLRREG	CERR0_HWMSX_PE: Hardware Mark Store Register (HWMSx [x = 0..7]) parity error (FIR 42).
24:31	RWX_WCLRREG	CERR0_FWMSX_PE: Firmware Mark Store Register x (FWMSx) parity error (FIR 42).
32:39	RO	Constant = 0b00000000
40	RWX_WCLRREG	CERR0_WECR_PE: WECR parity error (FIR 43).
41	RWX_WCLRREG	CERR0_AACR_PE: AACR parity error (FIR 42).
42	RWX_WCLRREG	CERR0_AADR_PE: AADR parity error (FIR 42).
43	RWX_WCLRREG	CERR0_AAER_PE: AAER parity error (FIR 42).
44	RWX_WCLRREG	CERR0_MCBCM_PE: MCBCM parity error (FIR 42).
45:47	RO	Constant = 0b000
48	RWX_WCLRREG	CERR0_WDFCFG_PE: WDFCFG parity error (FIR 52).
49:55	RO	Constant = 0b0000000
56	RWX_WCLRREG	CERR0_WRTCFG_PE: WRTCFG parity error (FIR 54).
57:63	RO	Constant = 0b0000000

Register Name	Error Report Hold Register 1
Mnemonic	MC01.PORT1.ECC64.SCOM.CERR1
Address	0000000007010A4F (SCOM)
Description	Contains error hold bits for errors other than SCOM register parity errors. Writing the CERR0 register clears all hold bits in CERR0 and CERR1. CERR1 makes various internal error detections visible.

Bits	SCOM	Field Mnemonic: Description
0	ROX	CERR1_ECC_CTL_AF_PERR: Sticky bit for a read ECC control-logic address FIFO parity error (FIR 44).
1	ROX	CERR1_ECC_CTL_RPTR_PERR: Sticky bit for a read ECC control-logic read-pointer timer parity error (FIR 44).
2	ROX	CERR1_ECC_CTL_TCHN_PERR: Sticky bit for a read ECC control-logic main timer parity error (FIR 44).
3	ROX	CERR1_ECC_CTL_CMPMODE_ERR: Sticky bit for a read ECC control-logic compare-mode error (FIR 44).
4	ROX	CERR1_ECC_CTL_SCHCTL_PERR: Sticky bit for a read ECC control-logic scheduler control parity error (FIR 44).
5	ROX	CERR1_ECC_CTL_PCTL_PERR: Sticky bit for a read ECC control-logic pipe control parity error (FIR 44).
6	ROX	CERR1_ECC_CTL_TGST_PERR: Sticky bit for a read ECC control-logic retry state parity error (FIR 44).

Bits	SCOM	Field Mnemonic: Description
7	ROX	CERR1_ECC_CTL_SCHTAB_PERR: Sticky bit for a read ECC control-logic schedule table parity error (FIR 44).
8	ROX	CERR1_ECC_PIPE_PCX_PERR: Sticky bit for a read ECC mark precomputation parity error (FIR 44).
9	ROX	CERR1_ECC_PIPE_SYND_PERR: Sticky bit for a read ECC syndrome parity error (FIR 44).
10	ROX	CERR1_ECC_PIPE_2SYM_PERR: Sticky bit for a read ECC 2-symbol corrector parity error (FIR 44).
11	ROX	CERR1_ECC_PIPE_CPLX_PERR: Sticky bit for a read ECC complex corrector parity error (FIR 44).
12	ROX	CERR1_ECC_PIPE_EP2_PERR: Sticky bit for a read ECC exit-2 parity error (FIR 44).
13	ROX	CERR1_READ_ECC_DATAPATH_PARITY_ERROR: Sticky bit for a read ECC datapath parity error (FIR 44).
14	ROX	CERR1_PHY_RPTR_PARITY_ERROR: Sticky bit for a DDR PHY read pointer parity error (FIR 44).
15	ROX	CERR1_ECC_CTL_RPD_PERR: Sticky bit for a read ECC control-logic pointer delay logic parity error (FIR 44).
16	ROX	CERR1_WDF_ASYNC_ERROR: Sticky bit for a WDF asynchronous interface error (FIR 57).
17	ROX	CERR1_WDF_BUFFER_CE: Sticky bit for a WDF buffer CE (FIR 45).
18	ROX	CERR1_WDF_BUFFER_UE: Sticky bit for a WDF buffer UE (FIR 46).
19	ROX	CERR1_WDF_BUFFER_SUE: Sticky bit for a WDF buffer SUE (FIR 47).
20:24	RO	Constant = 0b00000
25	ROX	CERR1_WRT_BUFFER_CE: Sticky bit for a write buffer CE (FIR 45).
26	ROX	CERR1_WRT_BUFFER_UE: Sticky bit for a write buffer UE (FIR 46).
27	ROX	CERR1_WRT_BUFFER_SUE: Sticky bit for a write buffer SUE (FIR 47).
28:31	RO	Constant = 0b0000
32	ROX	CERR1_READ_CONTROL_OVERFLOW_ERROR: Sticky bit for a read buffer overflow error (FIR 56).
33:39	RO	Constant = 0b0000000
40	ROX	CERR1_WRITE_ECC_DATAPATH_ERROR: Sticky bit for a write ECC datapath parity error (FIR 55).
41:63	RO	Constant = 0b00000000000000000000000

Register Name	**Hardware Mark Store Rank 0 Register**
Mnemonic	MC01.PORT1.ECC64.SCOM.HWMS0
Address	0000000007010A50 (SCOM)
Description	Hardware mark store rank 0

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	HWMS0_CHIPMARK: Hardware chipmark (Galois field code) for rank 0.
8	RWX	HWMS0_CONFIRMED: Chipmark confirmed.
9	RW	HWMS0_EXIT_1: When set, bypass-enabled reads using this mark use exit 1; otherwise, they use exit 0.

Register Name	**Hardware Mark Store Rank 1 Register**
Mnemonic	MC01.PORT1.ECC64.SCOM.HWMS1
Address	0000000007010A51 (SCOM)
Description	Hardware mark store rank 1

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	HWMS1_CHIPMARK: Hardware chipmark (Galois field code) for rank 1.
8	RWX	HWMS1_CONFIRMED: Chipmark confirmed.
9	RW	HWMS1_EXIT_1: When set, bypass-enabled reads using this mark use exit 1; otherwise, they use exit 0.

Register Name	Hardware Mark Store Rank 2 Register
Mnemonic	MC01.PORT1.ECC64.SCOM.HWMS2
Address	0000000007010A52 (SCOM)
Description	Hardware mark store rank 2

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	HWMS2_CHIPMARK: Hardware chipmark (Galois field code) for rank 2.
8	RWX	HWMS2_CONFIRMED: Chipmark confirmed.
9	RW	HWMS2_EXIT_1: When set, bypass-enabled reads using this mark use exit 1; otherwise, they use exit 0.

Register Name	Hardware Mark Store Rank 3 Register
Mnemonic	MC01.PORT1.ECC64.SCOM.HWMS3
Address	0000000007010A53 (SCOM)
Description	Hardware mark store rank 3

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	HWMS3_CHIPMARK: Hardware chipmark (Galois field code) for rank 3.
8	RWX	HWMS3_CONFIRMED: Chipmark confirmed.
9	RW	HWMS3_EXIT_1: When set, bypass-enabled reads using this mark use exit 1; otherwise, they use exit 0.

Register Name	Hardware Mark Store Rank 4 Register
Mnemonic	MC01.PORT1.ECC64.SCOM.HWMS4
Address	0000000007010A54 (SCOM)
Description	Hardware mark store rank 4

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	HWMS4_CHIPMARK: Hardware chipmark (Galois field code) for rank 4.
8	RWX	HWMS4_CONFIRMED: Chipmark confirmed.
9	RW	HWMS4_EXIT_1: When set, bypass-enabled reads using this mark use exit 1; otherwise, they use exit 0.

Register Name	Hardware Mark Store Rank 5 Register
Mnemonic	MC01.PORT1.ECC64.SCOM.HWMS5
Address	0000000007010A55 (SCOM)
Description	Hardware mark store rank 5

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	HWMS5_CHIPMARK: Hardware chipmark (Galois field code) for rank 5.
8	RWX	HWMS5_CONFIRMED: Chipmark confirmed.
9	RW	HWMS5_EXIT_1: When set, bypass-enabled reads using this mark use exit 1; otherwise, they use exit 0.

Register Name	Hardware Mark Store Rank 6 Register
Mnemonic	MC01.PORT1.ECC64.SCOM.HWMS6
Address	0000000007010A56 (SCOM)
Description	Hardware mark store rank 6

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	HWMS6_CHIPMARK: Hardware chipmark (Galois field code) for rank 6.
8	RWX	HWMS6_CONFIRMED: Chipmark confirmed.
9	RW	HWMS6_EXIT_1: When set, bypass-enabled reads using this mark use exit 1; otherwise, they use exit 0.

Register Name	Hardware Mark Store Rank 7 Register
Mnemonic	MC01.PORT1.ECC64.SCOM.HWMS7
Address	0000000007010A57 (SCOM)
Description	Hardware mark store rank 7

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	HWMS7_CHIPMARK: Hardware chipmark (Galois field code) for rank 7.
8	RWX	HWMS7_CONFIRMED: Chipmark confirmed.
9	RW	HWMS7_EXIT_1: When set, bypass-enabled reads using this mark use exit 1; otherwise, they use exit 0.

Register Name	Firmware Mark Store 0 Register
Mnemonic	MC01.PORT1.ECC64.SCOM.FWMS0
Address	0000000007010A58 (SCOM)
Description	Firmware mark store 0

Bits	SCOM	Field Mnemonic: Description
0:7	RW	FWMS0_MARK: Mark (Galois field code).
8	RW	FWMS0_TYPE: Mark type.
9:11	RW	FWMS0_REGION: Selects the mark region (the address range to which the mark applies).
12:22	RW	FWMS0_ADDRESS: Mark region address. bit 12 = DIMM bits 13:14 = mrank bits 15:17 = srank bits 18:19 = bank group bits 20:22 = bank (reserving space for 32 total banks)
23	RW	FWMS0_EXIT_1: When set, bypass-enabled reads using this mark use exit 1.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Firmware Mark Store 1 Register
Mnemonic	MC01.PORT1.ECC64.SCOM.FWMS1
Address	0000000007010A59 (SCOM)
Description	Firmware Mark Store 1

Bits	SCOM	Field Mnemonic: Description
0:7	RW	FWMS1_MARK: Mark (Galois field code).
8	RW	FWMS1_TYPE: Mark type.
9:11	RW	FWMS1_REGION: Selects the mark region (the address range to which the mark applies).
12:22	RW	FWMS1_ADDRESS: Mark region address. bit 12 = DIMM bits 13:14 = mrank bits 15:17 = srank bits 18:19 = bank group bits 20:22 = bank (reserving space for 32 total banks)
23	RW	FWMS1_EXIT_1: When set, bypass-enabled reads using this mark use exit 1.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Firmware Mark Store 2 Register
Mnemonic	MC01.PORT1.ECC64.SCOM.FWMS2
Address	0000000007010A5A (SCOM)
Description	Firmware mark store 2

Bits	SCOM	Field Mnemonic: Description
0:7	RW	FWMS2_MARK: Mark (Galois field code).
8	RW	FWMS2_TYPE: Mark type.
9:11	RW	FWMS2_REGION: Selects the mark region (the address range to which the mark applies).
12:22	RW	FWMS2_ADDRESS: Mark region address. bit 12 = DIMM bits 13:14 = mrank bits 15:17 = srank bits 18:19 = bank group bits 20:22 = bank (reserving space for 32 total banks)
23	RW	FWMS2_EXIT_1: When set, bypass-enabled reads using this mark use exit 1.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Firmware Mark Store 3 Register
Mnemonic	MC01.PORT1.ECC64.SCOM.FWMS3
Address	0000000007010A5B (SCOM)
Description	Firmware mark store 3

Bits	SCOM	Field Mnemonic: Description
0:7	RW	FWMS3_MARK: Mark (Galois field code).
8	RW	FWMS3_TYPE: Mark type.
9:11	RW	FWMS3_REGION: Selects the mark region (the address range to which the mark applies).
12:22	RW	FWMS3_ADDRESS: Mark region address. bit 12 = DIMM bits 13:14 = mrank bits 15:17 = srank bits 18:19 = bank group bits 20:22 = bank (reserving space for 32 total banks)
23	RW	FWMS3_EXIT_1: When set, bypass-enabled reads using this mark use exit 1.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Firmware Mark Store 4 Register
Mnemonic	MC01.PORT1.ECC64.SCOM.FWMS4
Address	0000000007010A5C (SCOM)
Description	Firmware mark store 4

Bits	SCOM	Field Mnemonic: Description
0:7	RW	FWMS4_MARK: Mark (Galois field code).
8	RW	FWMS4_TYPE: Mark type.
9:11	RW	FWMS4_REGION: Selects the mark region (the address range to which the mark applies).
12:22	RW	FWMS4_ADDRESS: Mark region address. bit 12 = DIMM bits 13:14 = mrank bits 15:17 = srank bits 18:19 = bank group bits 20:22 = bank (reserving space for 32 total banks)
23	RW	FWMS4_EXIT_1: When set, bypass-enabled reads using this mark use exit 1.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Firmware Mark Store 5 Register
Mnemonic	MC01.PORT1.ECC64.SCOM.FWMS5
Address	0000000007010A5D (SCOM)
Description	Firmware mark store 5

Bits	SCOM	Field Mnemonic: Description
0:7	RW	FWMS5_MARK: Mark (Galois field code).
8	RW	FWMS5_TYPE: Mark type.
9:11	RW	FWMS5_REGION: Selects the mark region (the address range to which the mark applies).

Bits	SCOM	Field Mnemonic: Description
12:22	RW	FWMS5_ADDRESS: Mark region address. bit 12 = DIMM bits 13:14 = mrank bits 15:17 = srank bits 18:19 = bank group bits 20:22 = bank (reserving space for 32 total banks)
23	RW	FWMS5_EXIT_1: When set, bypass-enabled reads using this mark use exit 1.
24:63	RO	Constant = 0b0000000000000000000000000000000000000000

Register Name	Firmware Mark Store 6 Register
Mnemonic	MC01.PORT1.ECC64.SCOM.FWMS6
Address	0000000007010A5E (SCOM)
Description	Firmware mark store 6

Bits	SCOM	Field Mnemonic: Description
0:7	RW	FWMS6_MARK: Mark (Galois field code).
8	RW	FWMS6_TYPE: Mark type.
9:11	RW	FWMS6_REGION: Selects the mark region (the address range to which the mark applies).
12:22	RW	FWMS6_ADDRESS: Mark region address. bit 12 = DIMM bits 13:14 = mrank bits 15:17 = srank bits 18:19 = bank group bits 20:22 = bank (reserving space for 32 total banks)
23	RW	FWMS6_EXIT_1: When set, bypass-enabled reads using this mark use exit 1.
24:63	RO	Constant = 0b0000000000000000000000000000000000000000

Register Name	Firmware Mark Store 7 Register
Mnemonic	MC01.PORT1.ECC64.SCOM.FWMS7
Address	0000000007010A5F (SCOM)
Description	Firmware mark store 7

Bits	SCOM	Field Mnemonic: Description
0:7	RW	FWMS7_MARK: Mark (Galois field code).
8	RW	FWMS7_TYPE: Mark type.
9:11	RW	FWMS7_REGION: Selects the mark region (the address range to which the mark applies).
12:22	RW	FWMS7_ADDRESS: Mark region address. bit 12 = DIMM bits 13:14 = mrank bits 15:17 = srank bits 18:19 = bank group bits 20:22 = bank (reserving space for 32 total banks)
23	RW	FWMS7_EXIT_1: When set, bypass-enabled reads using this mark use exit 1.
24:63	RO	Constant = 0b0000000000000000000000000000000000000000

Register Name	Write ECC Control Register
Mnemonic	MC01.PORT1.ECC64.SCOM.WECR
Address	0000000007010A68 (SCOM)
Description	Write ECC control register

Bits	SCOM	Field Mnemonic: Description
0	RW	MBA_WRD_MODE_CFG_WRD_ECC_CHK_DISABLE: Set to disable 8-byte ECC checking on the WRD data bus.
1	RW	MBA_WRD_MODE_CFG_WRD_ECC_COR_DISABLE: Set to disable 8-byte ECC correction on the WRD data bus.
2	RW	MBA_WRD_MODE_CFG_CRC_MODE_EN: Set to enable CRC generation on write data.
3	RW	MBA_WRD_MODE_CFG_CRC_MODE_X8: Only applies if cfg_crc_mode_en = 1. Set to generate a x8 CRC. Clear to generate a x4 CRC.
4	RW	MBA_WRD_MODE_RESERVED_4: Reserved.
5	RW	MBA_WRD_MODE_CFG_CAW2_CE_UE_ERR_DETECT_EN: Set to disable the internal error check of the memory ECC generator.
6:56	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	Array Access Control Register
Mnemonic	MC01.PORT1.ECC64.SCOM.AACR
Address	0000000007010A69 (SCOM)
Description	Array access control register

Bits	SCOM	Field Mnemonic: Description
0	RW	AACR_BUFFER: Buffer select.
1:9	RWX	AACR_ADDRESS: Array doubleword address.
10	RW	AACR_AUTOINC: When set, the AACR address field is incremented after each access to AAER.
11	RW	AACR_ECCGEN: When set, an 8-byte ECC is generated automatically when writing AAER (for more information, see Array Access ECC Register on page 222) and the 8-byte ECC is checked when reading the array (when reading AADR). When not set, an ECC is not generated or checked.
12:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	Array Access Data Register
Mnemonic	MC01.PORT1.ECC64.SCOM.AADR
Address	0000000007010A6A (SCOM)
Description	Array access data register

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	AADR_DATA: Array data (0:63).

Register Name	**Array Access ECC Register**
Mnemonic	MC01.PORT1.ECC64.SCOM.AAER
Address	0000000007010A6B (SCOM)
Description	Array access ECC register

Bits	SCOM	Field Mnemonic: Description
0:8	RWX	AAER_TAG_ECC: Array data(64:72). The contents of this register can be in either of two formats: • BUS format: Bit 0 is an I-series tag bit. Bits 1:8 are an 8-byte ECC. • MEM format: Bits 0:7 are memory ECC bits (the “metadata” is in bit 0). Bit 8 is unused (write as 0). Hardware generation of ECC bits for the BUS format is enabled when AACR_eccgen = 1. In this mode, ECC bits 1:8 should be written as 0.

Register Name	**MCBIST Compare Mask Register**
Mnemonic	MC01.PORT1.ECC64.SCOM.MCBCM
Address	0000000007010A6C (SCOM)
Description	MCBIST compare mask register. This register clears with an MCBIST global reset.

Bits	SCOM	Field Mnemonic: Description
0:39	RWX	MCBCM_MCBIST_HALF_COMPARE_MASK: Specifies the data bits to ignore for an MCBIST comparison. This mask covers either bits 0:39 or 40:79, configurable by the MASK_COVERAGE_SELECTOR dial.
40	RWX	MCBCM_MCBIST_MASK_COVERAGE_SELECTOR: Specifies the bits covered by the compare mask. If '0', the mask covers bits 0:39; otherwise, it covers bits 40:79.
41	RWX	MCBCM_MCBIST_TRAP_NONSTOP: If '1', MCBIST continues to trap new errors even when storage is full, *overwriting* older errors. If '0', MCBIST stops trapping when storage is full.
42	RWX	MCBCM_MCBIST_TRAP_CE_ENABLE: Enables capturing information for CEs.
43	RWX	MCBCM_MCBIST_TRAP_MPE_ENABLE: Enables capturing information for MPEs.
44	RWX	MCBCM_MCBIST_TRAP_UE_ENABLE: Enables capturing information for UEs.

Register Name	**Maintenance Buffer MDI/SUE State Register**
Mnemonic	MC01.PORT1.ECC64.SCOM.MBMDI
Address	0000000007010A6D (SCOM)
Description	Maintenance buffer MDI/SUE state

Bits	SCOM	Field Mnemonic: Description
0	RWX	MBMDI_MDI_0: MDI state for the first 64 bytes of the maintenance buffer. Maintenance reads set this bit to '1' if either in-memory MDI bit is '1'. Maintenance writes use this bit and the SUE_0 bit to compute the in-memory MDI bits, unless the ECC override is '1' where the undecoded maintenance buffer content is used.
1	RWX	MBMDI_SUE_0: SUE state for the first 64 bytes of the maintenance buffer. Maintenance reads set this bit to '1' if the in-memory MDI bits differ. Maintenance writes use this bit and the MDI_0 bit to compute the in-memory MDI bits, unless the ECC override is '1' where the undecoded maintenance buffer content is used.
2	RWX	MBMDI_MDI_1: MDI state for the second 64 bytes of the maintenance buffer. Maintenance reads set this bit to '1' if either in-memory MDI bit is '1'. Maintenance writes use this bit and the SUE_0 bit to compute the in-memory MDI bits, unless the ECC override is '1' where the undecoded maintenance buffer content is used.

Bits	SCOM	Field Mnemonic: Description
3	RWX	MBMDI_SUE_1: SUE state for the second 64 bytes of the maintenance buffer. Maintenance reads set this bit to '1' if the in-memory MDI bits differ. Maintenance writes use this bit and the MDI_1 bit to compute the in-memory MDI bits, unless the ECC override is '1' where the undecoded maintenance buffer content is used.

Register Name	Write ECC Syndrome Register
Mnemonic	MC01.PORT1.ECC64.SCOM.WESR
Address	0000000007010A6E (SCOM)
Description	The Write ECC Syndrome Register (WESR) contains additional hardware debug information.

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	WESR_SYNDROME: Traps an 8-byte ECC syndrome on the last WRD CAW2 errors.
8:9	ROX	WESR_WHICH_8BECK: Indicates which 8-byte ECC checker's syndrome was trapped. 00 = Doubleword 04 checker 01 = Doubleword 15 checker 10 = Doubleword 26 checker 11 = Doubleword 37 checker For multiple fails, trap priority goes to 00 first, 11 last.
10	ROX	WESR_PAR_ERR_ONLY: Indicates that no 8-byte ECC error was detected, and this CAW2 error was triggered by parity on non-data bits.

Register Name	Error Log Pointer Register
Mnemonic	MC01.PORT1.ECC64.CNTL.ELPR
Address	0000000007010A6F (SCOM)
Description	Provides a readout of the current error-log write pointer and a full/wrap indicator bit. The ELPR is not writable, but is cleared when MCB_CNTLQ[7] = 1 (dial MCB_CNTLQ_MCB_RESET_ERROR_LOGS).

Bits	SCOM	Field Mnemonic: Description
0	ROX	ELPR_LOG_FULL: The log is full. Distinguishes empty from exactly 64 entries.
1	RO	Constant = 0b0
2:7	ROX	ELPR_LOG_POINTER: Log pointer to the next entry to be written.

Register Name	WDF Buffer Miscellaneous Configuration Register
Mnemonic	MC01.PORT1.WDF.WDFCFG
Address	0000000007010A70 (SCOM)
Description	WDF buffer miscellaneous configuration

Bits	SCOM	Field Mnemonic: Description
0	RW	CFG_WRITE_MODE_ECC_CHK_DIS: Disables 8-byte ECC checking on WDF-buffer read ports.
1	RW	CFG_WRITE_MODE_ECC_COR_DIS: Disables 8-byte ECC correction on WDF-buffer read ports.
2	RW	CFG_WDF_SERIAL_SEQ_MODE: Puts the six PW sequencers into a serial mode of operation. No overlap.
3	RW	RESET_KEEPER: Reset the miscellaneous c_err_rpt keepers in the write buffer logic.
4:7	RW	MERGE_CAPACITY_LIMIT: Sets the capacity limit for the merge asynchronous buffer. Valid values are 0 - 8.

Bits	SCOM	Field Mnemonic: Description
8:11	RW	WDFCFG_8_11_SPARE: Spare bits.
12:17	RW	ASYNC_INJ: Asynchronous error inject.
18:31	RW	WDFCFG_18_31_SPARE: Spare bits.
32:35	RW	ECC_WDF_HCA_TIMEBASE_SELECT: HCA time base select.
36:63	RW	ECC_WDF_HCA_TIMEBASE: HCA time base.

Register Name	Write Buffer WRQ Register
Mnemonic	MC01.PORT1.WDF.WRT_ECC
Address	0000000007010A71 (SCOM)
Description	Port ECC error information register

Bits	SCOM	Field Mnemonic: Description
0:2	RWX_WCLRPART	WRT_ECC_DW0_ERR_TYPE: The ECC checker detected the following types of errors in write buffer WRQ read port, doubleword 0: bit 0 = CE bit 1 = UE bit 2 = SUE
3:7	RO	Constant = 0b00000
8:15	RWX_WCLRPART	WRT_ECC_DW0_SYNDROME: Write buffer WRQ read port, doubleword 0 ECC checker syndrome.
16:18	RWX_WCLRPART	WRT_ECC_DW1_ERR_TYPE: The ECC checker detected the following types of errors in write buffer WRQ read port, doubleword 1: bit 0 = CE bit 1 = UE bit 2 = SUE
19:23	RO	Constant = 0b00000
24:31	RWX_WCLRPART	WRT_ECC_DW1_SYNDROME: Write buffer WRQ read port, doubleword 1 ECC checker syndrome.
32:34	RWX_WCLRPART	WRT_ECC_DW2_ERR_TYPE: The ECC checker detected the following types of errors in write buffer WRQ read port, doubleword 2: bit 0 = CE bit 1 = UE bit 2 = SUE
35:39	RO	Constant = 0b00000
40:47	RWX_WCLRPART	WRT_ECC_DW2_SYNDROME: Write buffer WRQ read port, doubleword 2 ECC checker syndrome.
48:50	RWX_WCLRPART	WRT_ECC_DW3_ERR_TYPE: The ECC checker detected the following types of errors in write buffer WRQ read port, doubleword 3: bit 0 = CE bit 1 = UE bit 2 = SUE
51:55	RO	Constant = 0b00000
56:63	RWX_WCLRPART	WRT_ECC_DW3_SYNDROME: Write buffer WRQ read port, doubleword 3 ECC checker syndrome.

Register Name	WDF HCA Accumulator Register
Mnemonic	MC01.PORT1.WDF.HCA_ACCUM_REG
Address	0000000007010A72 (SCOM)
Description	WDF HCA accumulator register

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	ACCUM_REG: WDF HCA accumulator data.

Register Name	WDF Tag Overrun Information Register
Mnemonic	MC01.PORT1.WDF.WBMGR_TAG_INFO
Address	0000000007010A73 (SCOM)
Description	WDF tag overrun information

Bits	SCOM	Field Mnemonic: Description
0	RWX	BUFFER_OVERRUN: WDF buffer overrun indicator.
1	RWX	TAG_OVERRUN: WDF tag overrun indicator.
2	RWX	REL_TAG_ASYNC_PARITY_ERROR: WDF ERL tag parity error indicator.
3	RWX	REL_TAG_ASYNC_SEQUENCE_ERROR: WDF ERL tag sequence error indicator.
4	RWX	REL_MERGE_TAG_ASYNC_PARITY_ERROR: WDF ERL tag parity error indicator.
5	RWX	REL_MERGE_TAG_ASYNC_SEQUENCE_ERROR: WDF ERL tag sequence error indicator.
6:12	RWX	TAG_INFORMATION: WDF tag overrun information.
13:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000

Register Name	WDF Debug Control Register
Mnemonic	MC01.PORT1.WDF.WDFDBG
Address	0000000007010A74 (SCOM)
Description	WDF debug control

Bits	SCOM	Field Mnemonic: Description
0	RW	DBG_SEL_IN: Indicates that wdf_a_debug_in should be driven to wdf_a_debug_out.
1	RW	DBG_SEL_WDF: Indicates that internal debug data should be driven to wdf_a_debug_out.
2	RW	DBG_SEL_PWSEQ0_DEBUG_0: Indicates that internal debug data pwseq0_debug_0 should be driven to wdf_a_debug_out.
3	RW	DBG_SEL_PWSEQ0_DEBUG_1: Indicates that internal debug data pwseq0_debug_1 should be driven to wdf_a_debug_out.
4	RW	DBG_SEL_PWSEQ1_DEBUG_0: Indicates that internal debug data pwseq1_debug_0 should be driven to wdf_a_debug_out.
5	RW	DBG_SEL_PWSEQ1_DEBUG_1: Indicates that internal debug data pwseq1_debug_1 should be driven to wdf_a_debug_out.
6	RW	DBG_SEL_PWSEQ2_DEBUG_0: Indicates that internal debug data pwseq2_debug_0 should be driven to wdf_a_debug_out.

Bits	SCOM	Field Mnemonic: Description
7	RW	DBG_SEL_PWSEQ2_DEBUG_1: Indicates that internal debug data pwseq2_debug_1 should be driven to wdf_a_debug_out.
8	RW	DBG_SEL_PWSEQ3_DEBUG_0: Indicates that internal debug data pwseq3_debug_0 should be driven to wdf_a_debug_out.
9	RW	DBG_SEL_PWSEQ3_DEBUG_1: Indicates that internal debug data pwseq3_debug_1 should be driven to wdf_a_debug_out.
10	RW	DBG_SEL_PWSEQ4_DEBUG_0: Indicates that internal debug data pwseq4_debug_0 should be driven to wdf_a_debug_out.
11	RW	DBG_SEL_PWSEQ4_DEBUG_1: Indicates that internal debug data pwseq4_debug_1 should be driven to wdf_a_debug_out.
12	RW	DBG_SEL_PWSEQ5_DEBUG_0: Indicates that internal debug data pwseq5_debug_0 should be driven to wdf_a_debug_out.
13	RW	DBG_SEL_PWSEQ5_DEBUG_1: Indicates that internal debug data pwseq5_debug_1 should be driven to wdf_a_debug_out.
14	RW	DBG_SEL_PWCTL_DEBUG: Indicates that internal debug data pwctl_debug should be driven to wdf_a_debug_out.
15	RW	DBG_SEL_WDFMGR_DEBUG: Indicates that internal debug data wdfmgr_debug should be driven to wdf_a_debug_out.
16	RW	DBG_SEL_WDFRD_DEBUG_0: Indicates that internal debug data wdfrd_debug_0 should be driven to wdf_a_debug_out.
17	RW	DBG_SEL_WDFRD_DEBUG_1: Indicates that internal debug data wdfrd_debug_1 should be driven to wdf_a_debug_out.
18	RW	DBG_SEL_WDFWR_DEBUG_0: Indicates that internal debug data wdfwr_debug_0 should be driven to wdf_a_debug_out.
19	RW	DBG_SEL_WDFWR_DEBUG_1: Indicates that internal debug data wdfwr_debug_1 should be driven to wdf_a_debug_out.
20	RW	DBG_SEL_SEC_WDFRD_DEBUG_0: Indicates that internal debug data sec_wdfrd_debug_0 should be driven to wdf_a_debug_out.
21	RW	DBG_SEL_SEC_WDFRD_DEBUG_1: Indicates that internal debug data sec_wdfrd_debug_1 should be driven to wdf_a_debug_out.
22:31	RW	DBG_SPARE: Spare bits.
32	RW	WAT_EVENT_ENABLE: Enable latching of wat_event_in.
33:35	RW	WAT_SPARE1: WAT spare.
36:39	RW	WAT0_EVENT_SELECT: Select for wat_action(0).
40:43	RW	WAT1_EVENT_SELECT: Select for wat_action(1).
44:63	RO	Constant = 0b00000000000000000000

Register Name	Write Buffer Miscellaneous Configuration Register
Mnemonic	MC01.PORT1.WRITE.WRTCFG
Address	0000000007010A78 (SCOM)
Description	Write buffer miscellaneous configuration

Bits	SCOM	Field Mnemonic: Description
0	RW	CFG_WRITE_MODE_ECC_CHK_DIS: Disables 8-byte ECC checking on write-buffer read ports.

Bits	SCOM	Field Mnemonic: Description
1	RW	CFG_WRITE_MODE_ECC_COR_DIS: Disables 8-byte ECC correction on write-buffer read ports.
2	RW	RESET_KEEPER: Reset miscellaneous c_err_rpt keepers in the write buffer logic.
3	RW	MPIPL: mpipl.
4:7	RW	ASYNC_INJ: Asynchronous error inject.
8:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	Write Buffer WRQ Register
Mnemonic	MC01.PORT1.WRITE.WRT_ECC
Address	0000000007010A79 (SCOM)
Description	Port ECC error information register.

Bits	SCOM	Field Mnemonic: Description
0:2	RWX_WCLRPART	WRT_ECC_DW0_ERR_TYPE: The ECC checker detected the following types of errors in write buffer WRQ read port, doubleword 0: bit 0 = CE bit 1 = UE bit 2 = SUE
3:7	RO	Constant = 0b00000
8:15	RWX_WCLRPART	WRT_ECC_DW0_SYNDROME: Write buffer WRQ read port, doubleword 0 ECC checker syndrome.
16:18	RWX_WCLRPART	WRT_ECC_DW1_ERR_TYPE: The ECC checker detected the following types of errors in write buffer WRQ read port, doubleword 1: bit 0 = CE bit 1 = UE bit 2 = SUE
19:23	RO	Constant = 0b00000
24:31	RWX_WCLRPART	WRT_ECC_DW1_SYNDROME: Write buffer WRQ read port, doubleword 1 ECC checker syndrome.
32:34	RWX_WCLRPART	WRT_ECC_DW2_ERR_TYPE: The ECC checker detected the following types of errors in write buffer WRQ read port, doubleword 2: bit 0 = CE bit 1 = UE bit 2 = SUE
35:39	RO	Constant = 0b00000
40:47	RWX_WCLRPART	WRT_ECC_DW2_SYNDROME: Write buffer WRQ read port, doubleword 2 ECC checker syndrome.
48:50	RWX_WCLRPART	WRT_ECC_DW3_ERR_TYPE: The ECC checker detected the following types of errors in write buffer WRQ read port, doubleword 3: bit 0 = CE bit 1 = UE bit 2 = SUE
51:55	RO	Constant = 0b00000
56:63	RWX_WCLRPART	WRT_ECC_DW3_SYNDROME: Write buffer WRQ read port, doubleword 3 ECC checker syndrome.

Register Name	WRT MCA Debug Control Register
Mnemonic	MC01.PORT1.WRITE.WRTDBGMCA
Address	0000000007010A7A (SCOM)
Description	WRT MCA debug control

Bits	SCOM	Field Mnemonic: Description
0	RW	MCA_DBG_SEL_IN: Indicates that write_a_debug_in should be driven to write_a_debug_out.
1	RW	MCA_DBG_SEL_WRT: Indicates that internal debug data should be driven to write_a_debug_out.
2	RW	WBRD_DEBUG_0_SELECT: Indicates that internal debug data wbrd_debug_0 should be driven to write_a_debug_out.
3	RW	WBRD_DEBUG_1_SELECT: Indicates that internal debug data wbrd_debug_1 should be driven to write_a_debug_out.
4	RW	SEC_WBRD_DEBUG_0_SELECT: Indicates that internal debug data sec_wbrd_debug_0 should be driven to write_a_debug_out.
5	RW	SEC_WBRD_DEBUG_1_SELECT: Indicates that internal debug data sec_wbrd_debug_1 should be driven to write_a_debug_out.
6:15	RW	DBG_SPARE_MCA: Spare bits.
16	RW	WAT_EVENT_ENABLE_MCA: Enable latching of wat_event_in.
17:19	RW	WAT_SPARE1_MCA: WAT spare.
20:23	RW	WAT0_EVENT_SELECT_MCA: Select for wat_action(0).
24:27	RW	WAT1_EVENT_SELECT_MCA: Select for wat_action(1).
28:63	RO	Constant = 0b00000000000000000000000000000000000000

Register Name	WRT Nest Debug Control Register
Mnemonic	MC01.PORT1.WRITE.WRTDBGNEST
Address	0000000007010A7B (SCOM)
Description	WRT nest debug control

Bits	SCOM	Field Mnemonic: Description
0	RW	NEST_DBG_SEL_IN: Indicates that write_s_debug_in should be driven to write_s_debug_out.
1	RW	NEST_DBG_SEL_WRT: Indicates that internal debug data should be driven to write_s_debug_out.
2	RW	WBMGR_DBG_0_SELECT: Indicates that internal debug data wbmgr_0_debug should be driven to write_s_debug_out.
3	RW	WBMGR_DBG_1_SELECT: Indicates that internal debug data wbmgr_1_debug should be driven to write_s_debug_out.
4	RW	WRCNTL_DBG_SELECT: Indicates that internal debug data wrcntl_debug should be driven to write_s_debug_out.
5:15	RW	DBG_SPARE_NEST: Spare bits.
16	RW	WAT_EVENT_ENABLE_NEST: Enable latching of wat_event_in.
17:19	RW	WAT_SPARE1_NEST: WAT spare.
20:23	RW	WAT0_EVENT_SELECT_NEST: Select for wat_action(0).
24:27	RW	WAT1_EVENT_SELECT_NEST: Select for wat_action(1).

Bits	SCOM	Field Mnemonic: Description
28:63	RO	Constant = 0b00000000000000000000000000000000000000

Register Name	Datapath Fault Isolation Register
Mnemonic	MC01.PORT2.ECC64.SCOM.FIR
Address	0000000007010A80 (SCOM) 0000000007010A81 (SCOM1) 0000000007010A82 (SCOM2)
Description	Datapath fault isolation register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:7	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_MPE_RANK_0_TO_7: Mark placed error (MPE) detected on a mainline read. The corresponding Hardware Mark Store Register (HWMSx [x = 0..7]) is updated with a chipmark for the associated master rank.
8	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_NCE: New correctable error (NCE) detected on a mainline read.
9	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_TCE: Two-symbol correctable error (TCE) detected on a mainline read.
10	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_SCE: Symbol mark corrected error (SCE) detected on a mainline read.
11	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_MCE: Chip mark corrected error (MCE) detected on a mainline read.
12	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_SUE: Special uncorrectable error (SUE) detected on a mainline read.
13	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_AUE: Address uncorrectable error (AUE) detected on a mainline read.
14	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_UE: Uncorrectable error (UE) detected on a mainline read.
15	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_RCD: Parity error detected by the registering clock driver (RCD) detected on a mainline read.
16	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_IAUE: Intermittent AUE (IAUE) detected on a mainline read.
17	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_IUE: Intermittent UE (IUE) detected on a mainline read.
18	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_IRCD: Intermittent RCD (IRCD) detected on a mainline read.
19	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_IMPE: Intermittent MPE (IMPE) detected on a mainline read.
20:27	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_MPE_RANK_0_TO_7: Mark placed error (MPE) detected on a maintenance read. The corresponding Hardware Mark Store Register (HWMSx [x = 0..7]) is updated with a chipmark for the associated master rank.
28	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_NCE: New correctable error (NCE) detected on a maintenance read.
29	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_TCE: Two-symbol correctable error (TCE) detected on a maintenance read.
30	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_SCE: Symbol mark corrected error (SCE) detected on a maintenance read.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
31	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_MCE: Chip mark corrected error (MCE) detected on a maintenance read.
32	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_SUE: Special uncorrectable error (SUE) detected on a maintenance read.
33	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_AUE: Address uncorrectable error (AUE) detected on a maintenance read.
34	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_UE: Uncorrectable error (UE) detected on a maintenance read.
35	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_RCD: Parity error detected by the registering clock driver (RCD) detected on a maintenance read.
36	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_IAUE: Intermittent AUE (IAUE) detected on a maintenance read.
37	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_IUE: Intermittent UE (IUE) detected on a maintenance read.
38	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_IRCD: Intermittent RCD (IRCD) detected on a maintenance read.
39	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_IMPE: Intermittent MPE (IMPE) detected on a maintenance read.
40	RWX	WOX_AND	WOX_OR	FIR_RESERVED_40: Reserved.
41	RWX	WOX_AND	WOX_OR	FIR_SCOM_PARITY_CLASS_STATUS: SCOM register parity error, for registers in the “status” class (no data integrity risk). For additional information, see Error Report Hold Register 0 (SCOM Register Parity Errors) on page 214.
42	RWX	WOX_AND	WOX_OR	FIR_SCOM_PARITY_CLASS_RECOVERABLE: SCOM register parity error, for registers in the “recoverable” class (no data integrity risk; register must be reloaded). For additional information, see Error Report Hold Register 0 (SCOM Register Parity Errors)I on page 214.
43	RWX	WOX_AND	WOX_OR	FIR_SCOM_PARITY_CLASS_UNRECOVERABLE: SCOM register parity error, for registers in the “unrecoverable” class (data integrity risk). For additional information, see Error Report Hold Register 0 (SCOM Register Parity Errors)I on page 214.
44	RWX	WOX_AND	WOX_OR	FIR_ECC_CORRECTOR_INTERNAL_PARITY_ERROR: ECC corrector internal parity error (data integrity risk). For additional information, see Error Report Hold Register 1 on page 215.
45	RWX	WOX_AND	WOX_OR	FIR_WRITE_RMW_CE: CE detected at the write or RMW buffer read port. For additional information, see Error Report Hold Register 1 on page 215 and Write Buffer WRQ Register on page 224.
46	RWX	WOX_AND	WOX_OR	FIR_WRITE_RMW_UE: UE detected at the write or RMW buffer read port. For additional information, see Error Report Hold Register 1 on page 215 and Write Buffer WRQ Register on page 224.
47	RWX	WOX_AND	WOX_OR	FIR_WRITE_RMW_SUE: SUE detected at the write or RMW buffer read port. For additional information, see Error Report Hold Register 1 on page 215 and Write Buffer WRQ Register on page 224.
48	RWX	WOX_AND	WOX_OR	FIR_WDF_OVERRUN_ERROR_0: WDF logic detected a buffer overrun error (class 0).
49	RWX	WOX_AND	WOX_OR	FIR_WDF_OVERRUN_ERROR_1: WDF logic detected a buffer overrun error (class 1).
50	RWX	WOX_AND	WOX_OR	FIR_WDF_SCOM_SEQUENCE_ERROR: WDF logic detected a SCOM sequence error.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
51	RWX	WOX_AND	WOX_OR	FIR_WDF_STATE_MACHINE_ERROR: WDF logic detected a state machine error.
52	RWX	WOX_AND	WOX_OR	FIR_WDF_MISC_REGISTER_PARITY_ERROR: WDF logic detected a miscellaneous register parity error.
53	RWX	WOX_AND	WOX_OR	FIR_WRT_SCOM_SEQUENCE_ERROR: WRT logic detected a SCOM sequence error.
54	RWX	WOX_AND	WOX_OR	FIR_WRT_MISC_REGISTER_PARITY_ERROR: WRT logic detected a miscellaneous register parity error.
55	RWX	WOX_AND	WOX_OR	FIR_ECC_GENERATOR_INTERNAL_PARITY_ERROR: ECC generator internal parity error (data integrity risk).
56	RWX	WOX_AND	WOX_OR	FIR_READ_BUFFER_OVERFLOW_ERROR: Read buffer overflow error (data integrity risk).
57	RWX	WOX_AND	WOX_OR	FIR_WDF_ASYNC_INTERFACE_ERROR: WDF asynchronous interface error.
58	RWX	WOX_AND	WOX_OR	FIR_READ_ASYNC_INTERFACE_PARITY_ERROR: Read asynchronous interface parity error.
59	RWX	WOX_AND	WOX_OR	FIR_READ_ASYNC_INTERFACE_SEQUENCE_ERROR: Read asynchronous interface sequence error.
60:61	RWX	WOX_AND	WOX_OR	FIR_RESERVED: Reserved.
62	RWX	WOX_AND	WOX_OR	FIR_INTERNAL_SCOM_ERROR: A SCOM/FIR internal error has occurred.
63	RWX	WOX_AND	WOX_OR	FIR_INTERNAL_SCOM_ERROR_COPY: A SCOM/FIR internal error has occurred (redundant copy).

Register Name	**Datapath FIR Mask Register**
Mnemonic	MC01.PORT2.ECC64.SCOM.MASK
Address	0000000007010A83 (SCOM) 0000000007010A84 (SCOM1) 0000000007010A85 (SCOM2)
Description	Datapath FIR mask

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:63	RW	WO_AND	WO_OR	MASK_FIR_MASK: Mask for FIR bits 0:63.

Register Name	**Datapath FIR Action 0 Register**
Mnemonic	MC01.PORT2.ECC64.SCOM.ACTION0
Address	0000000007010A86 (SCOM)
Description	Datapath FIR Action 0

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ACTION0_FIR_ACTION0: Action0 select for the corresponding bits in the FIR. (Action0, Action1, Mask) selects: (0,0,0) = Checkstop error (0,1,0) = Recoverable error (1,0,0) = Attention (1,1,0) = Local checkstop error (X,X,1) = Masked

Register Name	Datapath FIR Action 1 Register
Mnemonic	MC01.PORT2.ECC64.SCOM.ACTION1
Address	0000000007010A87 (SCOM)
Description	Datapath FIR action 1

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ACTION1_FIR_ACTION1: Action1 select for the corresponding bits in the FIR. (Action0, Action1, Mask) selects: (0,0,0) = Checkstop error (0,1,0) = Recoverable error (1,0,0) = Attention (1,1,0) = Local checkstop error (X,X,1) = Masked

Register Name	Datapath FIR “Who is On First” Register
Mnemonic	MC01.PORT2.ECC64.SCOM.WOF
Address	0000000007010A88 (SCOM)
Description	Datapath FIR “Who is On First”

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	WOF_FIR_WOF: The WOF register locks on the first error. Writing zeros the register.

Register Name	Read ECC Control Register
Mnemonic	MC01.PORT2.ECC64.SCOM.RECR
Address	0000000007010A8A (SCOM)
Description	Read ECC control register

Bits	SCOM	Field Mnemonic: Description
0	RW	MBSECCQ_DISABLE_MEMORY_ECC_CHECK_CORRECT: When set, memory ECC check and correct is disabled. When memory ECC checking is disabled, SUE injecting into the 8-byte data bus ECC is also disabled.
1	RW	MBSECCQ_DISABLE_MEMORY_ECC_CORRECT: When set, memory ECC correct is disabled (memory ECC checking is not disabled).
2	RW	MBSECCQ_DISABLE_MARK_STORE_WRITE: Disables update of the HWMSx registers on an MPE.

Bits	SCOM	Field Mnemonic: Description
3	RW	MBSECCQ_DISABLE_UE_RETRY: When off, a read diagnosed as an exit-point-2 uncorrectable error (UE, AUE, or RCD) is retried. The FIR is set if the problem reoccurs on the retry. If the problem does not reoccur, the IUE/IAUE/IRCD FIR is set. When on, the UE/AUE/RCD FIRs are set immediately, and the IUE/IAUE/IRCD FIRs are not set.
4	RW	MBSECCQ_ITAG_METADATA_ENABLE: Enables I-series tag bits in the metadata symbols. When this dial is not set, the tag bits are used as four additional check bits.
5	RW	MBSECCQ_SLOW_EXIT_REDUCTION: When set, exit selection is modified to prevent the pileup of output data beats by choosing a later exit than would normally be used. Latency is increased. This mode is intended as a workaround to potential read_mac asynchronous interface issues.
6:8	RW	MBSECCQ_READ_POINTER_DELAY: Read pointer delay (mba_mbx_rdtag_val to mbr_ddr_clock_en) is (dial value + 2) MEMx2 cycles. This field interacts with MBSECCQ_ECC_SCHEDULER_DELAY according to the following formula: rdptrdly + 3 + (staging latches to PHY on mbr_ddr_* and from PHY on ddr_mbr_rdata) = scheddly + 7 Both rdptrdly and scheddly must be in the range 0 - 7.
9:10	RW	MBSECCQ_EXIT_OVERRIDE: Non-zero settings are for debug operation only.
11	RW	MBSECCQ_HWMARK_EXIT1: Selects the value to which HWMSx(9) [exit_1] is set when hardware sets a chipmark.
12	RW	MBSECCQ_DATA_GENERATOR_OVERRIDE: Also known as “wrap mode.” When set, overrides ECC corrector data output with an address-based data pattern. In each doubleword: bits(0:15) = 0xdead bits(16:19) = port index (0..7) bits(20:22) = 0 bit(23) = DIMM bits(24:25) = master rank bits(26:28) = slave rank bits(29:30) = bank group bits(31:33) = bank bits(34:51) = row(0:17) bits(52:59) = col(2:9) bits(60:63) = doubleword index (0 to 3) Metadata (I-series tags and MDI bit) will be zero. **Note**: Wrap mode also requires Exit_Override set to 0b01 (force_exit_0).
13:15	RW	MBSECCQ_ECC_SCHEDULER_DELAY: ECC scheduler delay (mba_mbx_rdtag_val to scheduler start). See MBSECCQ_Read_Pointer_Delay (6:8).
16:18	RW	MBSECCQ_VAL_TO_DATA_DELAY: Asynchronous side 2x cycle delay from ecc_tag_valid_rd to data valid. Affects the asynchronous interface.
19	RW	MBSECCQ_DELAY_VALID_1X: When set, read control delays ecc_tag_valid_rd by one MCA 1x cycle. In effect, it subtracts 0.5 from val_to_data_delay.
20:21	RW	MBSECCQ_NEST_VAL_TO_DATA_DELAY: The number of extra nest cycles of delay from tag to data. The valid range is 0 - 2. Affects the asynchronous interface.
22	RW	MBSECCQ_DELAY_NONBYPASS: When set, adds one extra nest cycle delay for nonbypass data (needed for the null_xfer/retry signal).
23	RW	MBSECCQ_ENABLE_SPECIAL_ATTENTION: When set, FIRs with action set to 10 assert special_attention.
24	RW	MBSECCQ_ENABLE_HOST_ATTENTION: When set, FIRs with action set to 10 assert host_attention.
25	RW	MBSECCQ_DISABLE_MPE_CONFIRM: When set, hardware marks are placed in the confirmed state.
26	RW	MBSECCQ_ENABLE_UE_NOISE_WINDOW: Enables noise window processing whenever a UE (or AUE) is detected.
27	RW	MBSECCQ_ENABLE_TCE_CORRECTION: Enables two-symbol error correction.

Bits	SCOM	Field Mnemonic: Description
28	RW	MBSECCQ_ENABLE_CHIPMARKED_SCE_NCE: Enables correction of a marked symbol and one unmarked symbol, when there is a chip mark (but no error in the marked chip).
29	RW	MBSECCQ_USE_ADDRESS_HASH: Enables use of an address hash in the ECC.
30:31	RW	MBSECCQ_DATA_INVERSION: Controls inversion of data to or from the PHY. Data and checks (including metadata) can be inverted for data beats where col(2) = 1. Or, data can be set to always invert, while checks invert where col(2) = 1.
32	RW	MBSECCQ_DISABLE_PIPE_NOERR_CLOCK_GATING: Disables these no-err/no-change clock gating features in the ECC pipe: 1. Mark precomputation is normally held while marks remain the same (for example, all-0). 2. Post-syndrome ECC computation stages are held while there is no new error.
33	RW	MBSECCQ_MAINT_NO_RETRY_UE: Maintenance equivalent of Disable_ue_retry (bit 3).
34	RW	MBSECCQ_MAINT_NO_RETRY_MPE: Maintenance equivalent of disable_MPE_confirm (bit 25).
35	RW	MBSECCQ_DISABLE_BYPASS_TEMPLATE_A: Disables least-latency mode for 128-byte bypass reads, so that beat 1 has an SUE in case of a bypass error on beat 0.
36:43	RW	MBSECCQ_RESERVED_36_43: Reserved.

Register Name	ECC Debug/WAT Control Register
Mnemonic	MC01.PORT2.ECC64.SCOM.DBGR
Address	0000000007010A8B (SCOM)
Description	ECC debug/WAT control register

Bits	SCOM	Field Mnemonic: Description
0	RW	DBGR_ECC_DEBUG_ENABLE: Enable the debug bus in the ECC64 macro. Required for the debug of ECC64 or SRQ.
1:2	RW	DBGR_ECC_DEBUG_CHUNK_SELECT: Select 0,1, 2, or 4 22-bit data chunks from the ECC debug sources. ECC data is inserted in the debug bus as follows: 00 = inp inp inp inp 01 = inp inp inp ecc 10 = inp inp ecc ecc 11 = ecc ecc ecc ecc Other fields of the debug bus output propagate the input (inp).
3:5	RW	DBGR_ECC_DEBUG_PRIMARY_SELECT: Primary select for the ECC debug source. 000 = sch1 sch2 ep21 ep22 / - - ep21 ep22 / - - - ep22 001 = sch1 sch2 ep22 ep21 / - - ep22 ep21 / - - - ep21 010 = ep21 ep22 wrd1 wrd2 / - - wrd1 wrd2 / - - - wrd2 011 = ep21 ep22 wrd2 wrd1 / - - wrd2 wrd1 / - - - wrd1 100 = wrd1 wrd2 sch1 sch2 / - - sch1 sch2 / - - - sch2 101 = wrd1 wrd2 sch2 sch1 / - - sch2 sch1 / - - - sch1 where: sch1 and sch2 are collections of debug information for the ECC corrector's scheduler logic. ep21 and ep22 are collections of debug information related to the exit-point-2 state logic. wrd1 and wrd2 are collections of debug information related to the write data logic.
6:7	RW	DBGR_ECC_DEBUG_SECONDARY_SELECT: Secondary select for the ECC debug data. The action varies by the primary source bus.
8	RW	DBGR_ECC_WAT_ENABLE: Enable workaround logic in the ECC corrector.

Bits	SCOM	Field Mnemonic: Description
9	RW	DBGR_ECC_WAT_ACTION_SELECT: Select the workaround action: 0 = Bypass disable (while selected, the WAT event is 1). 1 = Force exit 2 (while selected, the WAT event is 1).
10:11	RW	DBGR_ECC_WAT_SOURCE: Select the WAT event (bit 0 to 3).
12:14	RW	DBGR_READ_DEBUG_SELECT: Select debug source data in the read macro.

Register Name	Mark Shadow Register
Mnemonic	MC01.PORT2.ECC64.SCOM.MSR
Address	0000000007010A8C (SCOM)
Description	Mark Shadow Register

Bits	SCOM	Field Mnemonic: Description
0:7	RO	Constant = 0b00000000
8:15	ROX	MSR_CHIPMARK: Mark location (Galois field code) of the last mark placed (includes unconfirmed marks).
16:18	ROX	MSR_RANK: Rank of the last mark placed (includes unconfirmed marks).
19:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000

Register Name	Error Inject Control Register
Mnemonic	MC01.PORT2.ECC64.SCOM.EICR
Address	0000000007010A8D (SCOM)
Description	Error Inject Control Register

Bits	SCOM	Field Mnemonic: Description
0:36	RW	EICR_ADDRESS: An error is injected when the read address matches the EICR address, up to the fields masked by the EICR region. bit 0 = DIMM select bits 1:2 = mrank(0:1) bits 3:5 = srank(0:2) bits 6:7 = bank_group(0:1) bits 8:10 = bank(0:2) bits 11:28 = row(0:17) bits 29:36 = col(2:9)
37	RW	EICR_RESERVED: Reserved.
38:39	RW	EICR_PERSIST: Persistence of the injected error. Set to disabled (00) to disable error injection. Affects memory ECC error injection selected via the type field, or miscellaneous injection via the MISC field.
40:42	RW	EICR_REGION: Address region size for the error inject.
43:47	RW	EICR_TYPE: Bitmask for the error type to inject. bit 43: Inject address UE. bit 44: Inject DQ 0 (symbol 71, Galois code 0x38). bit 45: Inject DQ 1 (symbol 70, Galois code 0xa2). bit 46: Inject DQ 4 (symbol 39, Galois code 0x46). bit 47: Inject DQ 5,6 (symbols 38,37, Galois codes 0x1d, x0f4).

Bits	SCOM	Field Mnemonic: Description
48:51	RW	EICR_MISC: Selects miscellaneous error injections: • 8-byte ECC error injection at the output of the memory ECC checker. Inject a CE in bit 0 or bit 1, or a UE in both bits. Any data read from memory into either the RMW buffer or READ buffer will be injected. Errors should be visible in RMW ECC checkers or in the read master's ECC checkers. • Inject FIR(44) = ecc_corrector_internal_parity_error. • Inject read path asynchronous interface errors (parity or sequence_check). Miscellaneous errors are not affected by the address or region, but are affected by persistence (both soft_error and hard_error persistence act as a continuous inject). Undefined codes inject no error.

Register Name	Error Report Hold Register 0 (SCOM Register Parity Errors)
Mnemonic	MC01.PORT2.ECC64.SCOM.CERR0
Address	0000000007010A8E (SCOM)
Description	Each register parity error is reported in the bit location corresponding to the least 6 bits of the register's SCOM address. Writing the CERR0 register clears all hold bits in CERR0 and CERR1.

Bits	SCOM	Field Mnemonic: Description
0:9	RO	Constant = 0b0000000000
10	RWX_WCLRREG	CERR0_RECR_PE: RECR parity error (FIR 43).
11	RO	Constant = 0b0
12	RWX_WCLRREG	CERR0_MSR_PE: MSR parity error (FIR 41).
13	RWX_WCLRREG	CERR0_EICR_PE: EICR parity error (FIR 42).
14:15	RO	Constant = 0b00
16:23	RWX_WCLRREG	CERR0_HWMSX_PE: HWMSx parity error (FIR 42).
24:31	RWX_WCLRREG	CERR0_FWMSX_PE: FWMSx parity error (FIR 42).
32:39	RO	Constant = 0b00000000
40	RWX_WCLRREG	CERR0_WECR_PE: WECR parity error (FIR 43).
41	RWX_WCLRREG	CERR0_AACR_PE: AACR parity error (FIR 42).
42	RWX_WCLRREG	CERR0_AADR_PE: AADR parity error (FIR 42).
43	RWX_WCLRREG	CERR0_AAER_PE: AAER parity error (FIR 42).
44	RWX_WCLRREG	CERR0_MCBCM_PE: MCBCM parity error (FIR 42).
45:47	RO	Constant = 0b000
48	RWX_WCLRREG	CERR0_WDFCFG_PE: WDFCFG parity error (FIR 52).

Bits	SCOM	Field Mnemonic: Description
49:55	RO	Constant = 0b0000000
56	RWX_WCLRREG	CERR0_WRTCFG_PE: WRTCFG parity error (FIR 54).
57:63	RO	Constant = 0b0000000

Register Name	**Error Report Hold Register 1**
Mnemonic	MC01.PORT2.ECC64.SCOM.CERR1
Address	0000000007010A8F (SCOM)
Description	Contains error hold bits for errors other than SCOM register parity errors. Writing the CERR0 register clears all hold bits in CERR0 and CERR1. CERR1 makes various internal error detections visible.

Bits	SCOM	Field Mnemonic: Description
0	ROX	CERR1_ECC_CTL_AF_PERR: Sticky bit for a read ECC control-logic address FIFO parity error (FIR 44).
1	ROX	CERR1_ECC_CTL_RPTR_PERR: Sticky bit for a read ECC control-logic read-pointer timer parity error (FIR 44).
2	ROX	CERR1_ECC_CTL_TCHN_PERR: Sticky bit for a read ECC control-logic main timer parity error (FIR 44).
3	ROX	CERR1_ECC_CTL_CMPMODE_ERR: Sticky bit for a read ECC control-logic compare-mode error (FIR 44).
4	ROX	CERR1_ECC_CTL_SCHCTL_PERR: Sticky bit for a read ECC control-logic scheduler control parity error (FIR 44).
5	ROX	CERR1_ECC_CTL_PCTL_PERR: Sticky bit for a read ECC control-logic pipe control parity error (FIR 44).
6	ROX	CERR1_ECC_CTL_TGST_PERR: Sticky bit for a read ECC control-logic retry state parity error (FIR 44).
7	ROX	CERR1_ECC_CTL_SCHTAB_PERR: Sticky bit for a read ECC control-logic schedule table parity error (FIR 44).
8	ROX	CERR1_ECC_PIPE_PCX_PERR: Sticky bit for a read ECC mark precomputation parity error (FIR 44).
9	ROX	CERR1_ECC_PIPE_SYND_PERR: Sticky bit for a read ECC syndrome parity error (FIR 44).
10	ROX	CERR1_ECC_PIPE_2SYM_PERR: Sticky bit for a read ECC 2-symbol corrector parity error (FIR 44).
11	ROX	CERR1_ECC_PIPE_CPLX_PERR: Sticky bit for a read ECC complex corrector parity error (FIR 44).
12	ROX	CERR1_ECC_PIPE_EP2_PERR: Sticky bit for a read ECC exit-2 parity error (FIR 44).
13	ROX	CERR1_READ_ECC_DATAPATH_PARITY_ERROR: Sticky bit for a read ECC datapath parity error (FIR 44).
14	ROX	CERR1_PHY_RPTR_PARITY_ERROR: Sticky bit for DDR PHY a read pointer parity error (FIR 44).
15	ROX	CERR1_ECC_CTL_RPD_PERR: Sticky bit for a read ECC control-logic pointer delay logic parity error (FIR 44).
16	ROX	CERR1_WDF_ASYNC_ERROR: Sticky bit for a WDF asynchronous interface error (FIR 57).
17	ROX	CERR1_WDF_BUFFER_CE: Sticky bit for a WDF buffer CE (FIR 45).
18	ROX	CERR1_WDF_BUFFER_UE: Sticky bit for a WDF buffer UE (FIR 46).
19	ROX	CERR1_WDF_BUFFER_SUE: Sticky bit for a WDF buffer SUE (FIR 47).
20:24	RO	Constant = 0b00000
25	ROX	CERR1_WRT_BUFFER_CE: Sticky bit for a write buffer CE (FIR 45).
26	ROX	CERR1_WRT_BUFFER_UE: Sticky bit for a write buffer UE (FIR 46).
27	ROX	CERR1_WRT_BUFFER_SUE: Sticky bit for a write buffer SUE (FIR 47).
28:31	RO	Constant = 0b0000

Bits	SCOM	Field Mnemonic: Description
32	ROX	CERR1_READ_CONTROL_OVERFLOW_ERROR: Sticky bit for a read buffer overflow error (FIR 56).
33:39	RO	Constant = 0b0000000
40	ROX	CERR1_WRITE_ECC_DATAPATH_ERROR: Sticky bit for a write ECC datapath parity error (FIR 55).
41:63	RO	Constant = 0b00000000000000000000000

Register Name	Hardware Mark Store Rank 0 Register
Mnemonic	MC01.PORT2.ECC64.SCOM.HWMS0
Address	0000000007010A90 (SCOM)
Description	Hardware mark store rank 0

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	HWMS0_CHIPMARK: Hardware chipmark (Galois field code) for rank 0.
8	RWX	HWMS0_CONFIRMED: Chipmark confirmed.
9	RW	HWMS0_EXIT_1: When set, bypass-enabled reads using this mark use exit 1; otherwise, they use exit 0.

Register Name	Hardware Mark Store Rank 1 Register
Mnemonic	MC01.PORT2.ECC64.SCOM.HWMS1
Address	0000000007010A91 (SCOM)
Description	Hardware mark store rank 1

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	HWMS1_CHIPMARK: Hardware chipmark (Galois field code) for rank 1.
8	RWX	HWMS1_CONFIRMED: Chipmark confirmed.
9	RW	HWMS1_EXIT_1: When set, bypass-enabled reads using this mark use exit 1; otherwise, they use exit 0.

Register Name	Hardware Mark Store Rank 2 Register
Mnemonic	MC01.PORT2.ECC64.SCOM.HWMS2
Address	0000000007010A92 (SCOM)
Description	Hardware mark store rank 2

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	HWMS2_CHIPMARK: Hardware chipmark (Galois field code) for rank 2.
8	RWX	HWMS2_CONFIRMED: Chipmark confirmed.
9	RW	HWMS2_EXIT_1: When set, bypass-enabled reads using this mark use exit 1; otherwise, they use exit 0.

Register Name	Hardware Mark Store Rank 3 Register
Mnemonic	MC01.PORT2.ECC64.SCOM.HWMS3
Address	0000000007010A93 (SCOM)
Description	Hardware mark store rank 3

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	HWMS3_CHIPMARK: Hardware chipmark (Galois field code) for rank 3.
8	RWX	HWMS3_CONFIRMED: Chipmark confirmed.
9	RW	HWMS3_EXIT_1: When set, bypass-enabled reads using this mark use exit 1; otherwise, they use exit 0.

Register Name	Hardware Mark Store Rank 4 Register
Mnemonic	MC01.PORT2.ECC64.SCOM.HWMS4
Address	0000000007010A94 (SCOM)
Description	Hardware mark store rank 4

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	HWMS4_CHIPMARK: Hardware chipmark (Galois field code) for rank 4.
8	RWX	HWMS4_CONFIRMED: Chipmark confirmed.
9	RW	HWMS4_EXIT_1: When set, bypass-enabled reads using this mark use exit 1; otherwise, they use exit 0.

Register Name	Hardware Mark Store Rank 5 Register
Mnemonic	MC01.PORT2.ECC64.SCOM.HWMS5
Address	0000000007010A95 (SCOM)
Description	Hardware mark store rank 5

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	HWMS5_CHIPMARK: Hardware chipmark (Galois field code) for rank 5.
8	RWX	HWMS5_CONFIRMED: Chipmark confirmed.
9	RW	HWMS5_EXIT_1: When set, bypass-enabled reads using this mark use exit 1; otherwise, they use exit 0.

Register Name	Hardware Mark Store Rank 6 Register
Mnemonic	MC01.PORT2.ECC64.SCOM.HWMS6
Address	0000000007010A96 (SCOM)
Description	Hardware mark store rank 6

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	HWMS6_CHIPMARK: Hardware chipmark (Galois field code) for rank 6.
8	RWX	HWMS6_CONFIRMED: Chipmark confirmed.
9	RW	HWMS6_EXIT_1: When set, bypass-enabled reads using this mark use exit 1; otherwise, they use exit 0.

Register Name	Hardware Mark Store Rank 7 Register
Mnemonic	MC01.PORT2.ECC64.SCOM.HWMS7
Address	0000000007010A97 (SCOM)
Description	Hardware mark store rank 7

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	HWMS7_CHIPMARK: Hardware chipmark (Galois field code) for rank 7.
8	RWX	HWMS7_CONFIRMED: Chipmark confirmed.
9	RW	HWMS7_EXIT_1: When set, bypass-enabled reads using this mark use exit 1; otherwise, they use exit 0.

Register Name	Firmware Mark Store 0 Register
Mnemonic	MC01.PORT2.ECC64.SCOM.FWMS0
Address	0000000007010A98 (SCOM)
Description	Firmware mark store 0

Bits	SCOM	Field Mnemonic: Description
0:7	RW	FWMS0_MARK: Mark (Galois field code).
8	RW	FWMS0_TYPE: Mark type.
9:11	RW	FWMS0_REGION: Selects the mark region (address range to which the mark applies).
12:22	RW	FWMS0_ADDRESS: Mark region address. bit 12 = DIMM bits 13:14 = mrank bits 15:17 = srank bits 18:19 = bank group bits 20:22 = bank (reserving space for 32 total banks)
23	RW	FWMS0_EXIT_1: When set, bypass-enabled reads using this mark use exit 1.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Firmware Mark Store 1 Register
Mnemonic	MC01.PORT2.ECC64.SCOM.FWMS1
Address	0000000007010A99 (SCOM)
Description	Firmware mark store 1

Bits	SCOM	Field Mnemonic: Description
0:7	RW	FWMS1_MARK: Mark (Galois field code).
8	RW	FWMS1_TYPE: Mark type.
9:11	RW	FWMS1_REGION: Selects the mark region (address range to which the mark applies).
12:22	RW	FWMS1_ADDRESS: Mark region address. bit 12 = DIMM bits 13:14 = mrank bits 15:17 = srank bits 18:19 = bank group bits 20:22 = bank (reserving space for 32 total banks)
23	RW	FWMS1_EXIT_1: When set, bypass-enabled reads using this mark use exit 1.

Bits	SCOM	Field Mnemonic: Description
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Firmware Mark Store 2 Register
Mnemonic	MC01.PORT2.ECC64.SCOM.FWMS2
Address	0000000007010A9A (SCOM)
Description	Firmware Mark Store 2

Bits	SCOM	Field Mnemonic: Description
0:7	RW	FWMS2_MARK: Mark (Galois field code).
8	RW	FWMS2_TYPE: Mark type.
9:11	RW	FWMS2_REGION: Selects the mark region (address range to which the mark applies).
12:22	RW	FWMS2_ADDRESS: Mark region address. bit 12 = DIMM bits 13:14 = mrank bits 15:17 = srank bits 18:19 = bank group bits 20:22 = bank (reserving space for 32 total banks)
23	RW	FWMS2_EXIT_1: When set, bypass-enabled reads using this mark use exit 1.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Firmware Mark Store 3 Register
Mnemonic	MC01.PORT2.ECC64.SCOM.FWMS3
Address	0000000007010A9B (SCOM)
Description	Firmware mark store 3

Bits	SCOM	Field Mnemonic: Description
0:7	RW	FWMS3_MARK: Mark (Galois field code).
8	RW	FWMS3_TYPE: Mark type.
9:11	RW	FWMS3_REGION: Selects the mark region (address range to which the mark applies).
12:22	RW	FWMS3_ADDRESS: Mark region address. bit 12 = DIMM bits 13:14 = mrank bits 15:17 = srank bits 18:19 = bank group bits 20:22 = bank (reserving space for 32 total banks)
23	RW	FWMS3_EXIT_1: When set, bypass-enabled reads using this mark use exit 1.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Firmware Mark Store 4 Register
Mnemonic	MC01.PORT2.ECC64.SCOM.FWMS4
Address	0000000007010A9C (SCOM)
Description	Firmware mark store 4

Bits	SCOM	Field Mnemonic: Description
0:7	RW	FWMS4_MARK: Mark (Galois field code).
8	RW	FWMS4_TYPE: Mark type.
9:11	RW	FWMS4_REGION: Selects the mark region (address range to which the mark applies).
12:22	RW	FWMS4_ADDRESS: Mark region address. bit 12 = DIMM bits 13:14 = mrank bits 15:17 = srank bits 18:19 = bank group bits 20:22 = bank (reserving space for 32 total banks)
23	RW	FWMS4_EXIT_1: When set, bypass-enabled reads using this mark use exit 1.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Firmware Mark Store 5 Register
Mnemonic	MC01.PORT2.ECC64.SCOM.FWMS5
Address	0000000007010A9D (SCOM)
Description	Firmware mark store 5

Bits	SCOM	Field Mnemonic: Description
0:7	RW	FWMS5_MARK: Mark (Galois field code).
8	RW	FWMS5_TYPE: Mark type.
9:11	RW	FWMS5_REGION: Selects the mark region (address range to which the mark applies).
12:22	RW	FWMS5_ADDRESS: Mark region address. bit 12 = DIMM bits 13:14 = mrank bits 15:17 = srank bits 18:19 = bank group bits 20:22 = bank (reserving space for 32 total banks)
23	RW	FWMS5_EXIT_1: When set, bypass-enabled reads using this mark use exit 1.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Firmware Mark Store 6 Register
Mnemonic	MC01.PORT2.ECC64.SCOM.FWMS6
Address	0000000007010A9E (SCOM)
Description	Firmware mark store 6

Bits	SCOM	Field Mnemonic: Description
0:7	RW	FWMS6_MARK: Mark (Galois field code).
8	RW	FWMS6_TYPE: Mark type.
9:11	RW	FWMS6_REGION: Selects the mark region (address range to which the mark applies).

Bits	SCOM	Field Mnemonic: Description
12:22	RW	FWMS6_ADDRESS: Mark region address. bit 12 = DIMM bits 13:14 = mrank bits 15:17 = srank bits 18:19 = bank group bits 20:22 = bank (reserving space for 32 total banks)
23	RW	FWMS6_EXIT_1: When set, bypass-enabled reads using this mark use exit 1
24:63	RO	Constant = 0b0000000000000000000000000000000000000000

Register Name	Firmware Mark Store 7 Register
Mnemonic	MC01.PORT2.ECC64.SCOM.FWMS7
Address	0000000007010A9F (SCOM)
Description	Firmware mark store 7

Bits	SCOM	Field Mnemonic: Description
0:7	RW	FWMS7_MARK: Mark (Galois field code).
8	RW	FWMS7_TYPE: Mark type.
9:11	RW	FWMS7_REGION: Selects the mark region (address range to which the mark applies).
12:22	RW	FWMS7_ADDRESS: Mark region address. bit 12 = DIMM bits 13:14 = mrank bits 15:17 = srank bits 18:19 = bank group bits 20:22 = bank (reserving space for 32 total banks)
23	RW	FWMS7_EXIT_1: When set, bypass-enabled reads using this mark use exit 1.
24:63	RO	Constant = 0b0000000000000000000000000000000000000000

Register Name	Write ECC Control Register
Mnemonic	MC01.PORT2.ECC64.SCOM.WECR
Address	0000000007010AA8 (SCOM)
Description	Write ECC control register

Bits	SCOM	Field Mnemonic: Description
0	RW	MBA_WRD_MODE_CFG_WRD_ECC_CHK_DISABLE: Set to disable 8-byte ECC checking on the WRD data bus.
1	RW	MBA_WRD_MODE_CFG_WRD_ECC_COR_DISABLE: Set to disable 8-byte ECC correction on the WRD data bus.
2	RW	MBA_WRD_MODE_CFG_CRC_MODE_EN: Set to enable CRC generation on write data.
3	RW	MBA_WRD_MODE_CFG_CRC_MODE_X8: Only applies if cfg_crc_mode_en = 1. Set to generate x8 CRC. Clear to generate x4 CRC.
4	RW	MBA_WRD_MODE_RESERVED_4: Reserved.
5	RW	MBA_WRD_MODE_CFG_CAW2_CE_UE_ERR_DETECT_EN: Set to disable the internal error check of the memory ECC generator.
6:56	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	Array Access Control Register
Mnemonic	MC01.PORT2.ECC64.SCOM.AACR
Address	0000000007010AA9 (SCOM)
Description	Array Access Control Register

Bits	SCOM	Field Mnemonic: Description
0	RW	AACR_BUFFER: Buffer select.
1:9	RWX	AACR_ADDRESS: Array doubleword address.
10	RW	AACR_AUTOINC: When set, the AACR address field is incremented after each access to the AAER.
11	RW	AACR_ECCGEN: When set, an 8-byte ECC is generated automatically when writing the AAER (for more information, see 3Array Access ECC Register on page 222) and an 8-byte ECC is checked when reading the array (when reading AADR). When not set, ECC is not generated or checked.
12:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	Array Access Data Register
Mnemonic	MC01.PORT2.ECC64.SCOM.AADR
Address	0000000007010AAA (SCOM)
Description	Array Access Data Register

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	AADR_DATA: Array data(0:63).

Register Name	Array Access ECC Register
Mnemonic	MC01.PORT2.ECC64.SCOM.AAER
Address	0000000007010AAB (SCOM)
Description	Array Access ECC Register

Bits	SCOM	Field Mnemonic: Description
0:8	RWX	AAER_TAG_ECC: Array data(64:72). The contents of this register can be in either of two formats: • BUS format: Bit 0 is an I-series tag bit. Bits 1:8 are an 8-byte ECC. • MEM format: Bits 0:7 are memory ECC bits (the “metadata” is in bit 0). Bit 8 is unused (write as 0). Hardware generation of ECC bits for the BUS format is enabled when AACR_eccgen = 1. In this mode, the ECC bits 1:8 should be written as 0.

Register Name	MCBIST Compare Mask Register
Mnemonic	MC01.PORT2.ECC64.SCOM.MCBCM
Address	0000000007010AAC (SCOM)
Description	MCBIST Compare Mask Register (register clears with MCBIST global reset)

Bits	SCOM	Field Mnemonic: Description
0:39	RWX	MCBCM_MCBIST_HALF_COMPARE_MASK: Specifies data bits to ignore for MCBIST comparison. This mask covers either bits 0:39 or 40:79, configurable by the MASK_COVERAGE_SELECTOR dial.
40	RWX	MCBCM_MCBIST_MASK_COVERAGE_SELECTOR: Specifies the bits covered by the compare mask. If '0', the mask covers bits 0:39; otherwise, they cover bits 40:79.
41	RWX	MCBCM_MCBIST_TRAP_NONSTOP: If '1', MCBIST continues to trap new errors even when storage is full, *overwriting* older errors. If '0', MCBIST stops trapping when storage is full.
42	RWX	MCBCM_MCBIST_TRAP_CE_ENABLE: Enables capturing information for CEs.
43	RWX	MCBCM_MCBIST_TRAP_MPE_ENABLE: Enables capturing information for MPEs.
44	RWX	MCBCM_MCBIST_TRAP_UE_ENABLE: Enables capturing information for UEs.

Register Name	**Maintenance Buffer MDI/SUE State Register**
Mnemonic	MC01.PORT2.ECC64.SCOM.MBMDI
Address	0000000007010AAD (SCOM)
Description	Maintenance buffer MDI/SUE state

Bits	SCOM	Field Mnemonic: Description
0	RWX	MBMDI_MDI_0: MDI state for the first 64 bytes of the maintenance buffer. Maintenance reads set this bit to '1' if either in-memory MDI bit is '1'. Maintenance writes use this bit and the SUE_0 bit to compute the in-memory MDI bits, unless the ECC override is '1' where the undecoded maintenance buffer content is used.
1	RWX	MBMDI_SUE_0: SUE state for the first 64 bytes of the maintenance buffer. Maintenance reads set this bit to '1' if the in-memory MDI bits differ. Maintenance writes use this bit and the MDI_0 bit to compute the in-memory MDI bits, unless the ECC override is '1' where the undecoded maintenance buffer content is used.
2	RWX	MBMDI_MDI_1: MDI state for the second 64 bytes of the maintenance buffer. Maintenance reads set this bit to '1' if either in-memory MDI bit is '1'. Maintenance writes use this bit and the SUE_0 bit to compute the in-memory MDI bits, unless the ECC override is '1' where the undecoded maintenance buffer content is used.
3	RWX	MBMDI_SUE_1: SUE state for the second 64 bytes of the maintenance buffer. Maintenance reads set this bit to '1' if the in-memory MDI bits differ. Maintenance writes use this bit and the MDI_1 bit to compute the in-memory MDI bits, unless the ECC override is '1' where the undecoded maintenance buffer content is used.

Register Name	**Write ECC Syndrome Register**
Mnemonic	MC01.PORT2.ECC64.SCOM.WESR
Address	0000000007010AAE (SCOM)
Description	The Write ECC Syndrome Register (WESR) contains additional hardware debug information.

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	WESR_SYNDROME: Traps an 8-byte ECC syndrome on the last WRD CAW2 errors.
8:9	ROX	WESR_WHICH_8BECK: Indicates which 8-byte ECC checker's syndrome was trapped. 00 = Doubleword 04 checker 01 = Doubleword 15 checker 10 = Doubleword 26 checker 11 = Doubleword 37 checker For multiple fails, trap priority goes to 00 first, 11 last.
10	ROX	WESR_PAR_ERR_ONLY: Indicates that no 8-byte ECC error was detected and this CAW2 error was triggered by parity on non-data bits.

Register Name	Error Log Pointer Register
Mnemonic	MC01.PORT2.ECC64.CNTL.ELPR
Address	0000000007010AAF (SCOM)
Description	Provides a readout of the current error-log write pointer and the full/wrap indicator bit. The ELPR is not writable, but is cleared when MCB_CNTLQ[7] = 1 (dial MCB_CNTLQ_MCB_RESET_ERROR_LOGS).

Bits	SCOM	Field Mnemonic: Description
0	ROX	ELPR_LOG_FULL: The log is full. Distinguishes empty from exactly 64 entries.
1	RO	Constant = 0b0
2:7	ROX	ELPR_LOG_POINTER: Log pointer to the next entry to be written.

Register Name	WDF Buffer Miscellaneous Configuration Register
Mnemonic	MC01.PORT2.WDF.WDFCFG
Address	0000000007010AB0 (SCOM)
Description	WDF buffer miscellaneous configuration

Bits	SCOM	Field Mnemonic: Description
0	RW	CFG_WRITE_MODE_ECC_CHK_DIS: Disables 8-byte ECC checking on WDF-buffer read ports.
1	RW	CFG_WRITE_MODE_ECC_COR_DIS: Disables 8-byte ECC correction on WDF-buffer read ports.
2	RW	CFG_WDF_SERIAL_SEQ_MODE: Puts the six PW sequencers into a serial mode of operation; no overlap.
3	RW	RESET_KEEPER: Reset miscellaneous c_err_rpt keepers in the write buffer logic.
4:7	RW	MERGE_CAPACITY_LIMIT: Sets the capacity limit for the merge asynchronous buffer. Valid values are 0 - 8.
8:11	RW	WDFCFG_8_11_SPARE: Spare bits.
12:17	RW	ASYNC_INJ: Asynchronous error inject.
18:31	RW	WDFCFG_18_31_SPARE: Spare bits.
32:35	RW	ECC_WDF_HCA_TIMEBASE_SELECT: HCA time base select.
36:63	RW	ECC_WDF_HCA_TIMEBASE: HCA time base.

Register Name	Write Buffer WRQ Register
Mnemonic	MC01.PORT2.WDF.WRT_ECC
Address	0000000007010AB1 (SCOM)
Description	Port ECC error information register

Bits	SCOM	Field Mnemonic: Description
0:2	RWX_WCLRPART	WRT_ECC_DW0_ERR_TYPE: The ECC checker detected the following types of errors in write buffer WRQ read port doubleword 0: bit 0 = CE bit 1 = UE bit 2 = SUE
3:7	RO	Constant = 0b00000
8:15	RWX_WCLRPART	WRT_ECC_DW0_SYNDROME: Write buffer WRQ read port doubleword 0 ECC checker syndrome.

Bits	SCOM	Field Mnemonic: Description
16:18	RWX_WCLRPART	WRT_ECC_DW1_ERR_TYPE: The ECC checker detected the following types of errors in write buffer WRQ read port doubleword 1: bit 0 = CE bit 1 = UE bit 2 = SUE
19:23	RO	Constant = 0b00000
24:31	RWX_WCLRPART	WRT_ECC_DW1_SYNDROME: Write buffer WRQ read port doubleword 1 ECC checker syndrome.
32:34	RWX_WCLRPART	WRT_ECC_DW2_ERR_TYPE: The ECC checker detected the following types of errors in write buffer WRQ read port doubleword 2: bit 0 = CE bit 1 = UE bit 2 = SUE
35:39	RO	Constant = 0b00000
40:47	RWX_WCLRPART	WRT_ECC_DW2_SYNDROME: Write buffer WRQ read port doubleword 2 ECC checker syndrome.
48:50	RWX_WCLRPART	WRT_ECC_DW3_ERR_TYPE: The ECC checker detected the following types of errors in write buffer WRQ read port doubleword 3: bit 0 = CE bit 1 = UE bit 2 = SUE
51:55	RO	Constant = 0b00000
56:63	RWX_WCLRPART	WRT_ECC_DW3_SYNDROME: Write buffer WRQ read port doubleword 3 ECC checker syndrome.

Register Name	WDF HCA Accumulator Register
Mnemonic	MC01.PORT2.WDF.HCA_ACCUM_REG
Address	0000000007010AB2 (SCOM)
Description	WDF HCA accumulator register

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	ACCUM_REG: WDF HCA accumulator data.

Register Name	WDF Tag Overrun Information Register
Mnemonic	MC01.PORT2.WDF.WBMGR_TAG_INFO
Address	0000000007010AB3 (SCOM)
Description	WDF tag overrun information

Bits	SCOM	Field Mnemonic: Description
0	RWX	BUFFER_OVERRUN: WDF buffer overrun indicator.
1	RWX	TAG_OVERRUN: WDF tag overrun indicator.
2	RWX	REL_TAG_ASYNC_PARITY_ERROR: WDF ERL tag parity error indicator.
3	RWX	REL_TAG_ASYNC_SEQUENCE_ERROR: WDF ERL tag sequence error indicator.
4	RWX	REL_MERGE_TAG_ASYNC_PARITY_ERROR: WDF ERL tag parity error indicator.

Bits	SCOM	Field Mnemonic: Description
5	RWX	REL_MERGE_TAG_ASYNC_SEQUENCE_ERROR: WDF ERL tag sequence error indicator.
6:12	RWX	TAG_INFORMATION: WDF tag overrun information.
13:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000

Register Name	WDF Debug Control Register
Mnemonic	MC01.PORT2.WDF.WDFDBG
Address	0000000007010AB4 (SCOM)
Description	WDF debug control

Bits	SCOM	Field Mnemonic: Description
0	RW	DBG_SEL_IN: Indicates that wdf_a_debug_in should be driven to wdf_a_debug_out.
1	RW	DBG_SEL_WDF: Indicates that internal debug data should be driven to wdf_a_debug_out.
2	RW	DBG_SEL_PWSEQ0_DEBUG_0: Indicates that internal debug data pwseq0_debug_0 should be driven to wdf_a_debug_out.
3	RW	DBG_SEL_PWSEQ0_DEBUG_1: Indicates that internal debug data pwseq0_debug_1 should be driven to wdf_a_debug_out.
4	RW	DBG_SEL_PWSEQ1_DEBUG_0: Indicates that internal debug data pwseq1_debug_0 should be driven to wdf_a_debug_out.
5	RW	DBG_SEL_PWSEQ1_DEBUG_1: Indicates that internal debug data pwseq1_debug_1 should be driven to wdf_a_debug_out.
6	RW	DBG_SEL_PWSEQ2_DEBUG_0: Indicates that internal debug data pwseq2_debug_0 should be driven to wdf_a_debug_out.
7	RW	DBG_SEL_PWSEQ2_DEBUG_1: Indicates that internal debug data pwseq2_debug_1 should be driven to wdf_a_debug_out.
8	RW	DBG_SEL_PWSEQ3_DEBUG_0: Indicates that internal debug data pwseq3_debug_0 should be driven to wdf_a_debug_out.
9	RW	DBG_SEL_PWSEQ3_DEBUG_1: Indicates that internal debug data pwseq3_debug_1 should be driven to wdf_a_debug_out.
10	RW	DBG_SEL_PWSEQ4_DEBUG_0: Indicates that internal debug data pwseq4_debug_0 should be driven to wdf_a_debug_out.
11	RW	DBG_SEL_PWSEQ4_DEBUG_1: Indicates that internal debug data pwseq4_debug_1 should be driven to wdf_a_debug_out.
12	RW	DBG_SEL_PWSEQ5_DEBUG_0: Indicates that internal debug data pwseq5_debug_0 should be driven to wdf_a_debug_out.
13	RW	DBG_SEL_PWSEQ5_DEBUG_1: Indicates that internal debug data pwseq5_debug_1 should be driven to wdf_a_debug_out.
14	RW	DBG_SEL_PWCTL_DEBUG: Indicates that internal debug data pwctl_debug should be driven to wdf_a_debug_out.
15	RW	DBG_SEL_WDFMGR_DEBUG: Indicates that internal debug data wdfmgr_debug should be driven to wdf_a_debug_out.
16	RW	DBG_SEL_WDFRD_DEBUG_0: Indicates that internal debug data wdfrd_debug_0 should be driven to wdf_a_debug_out.
17	RW	DBG_SEL_WDFRD_DEBUG_1: Indicates that internal debug data wdfrd_debug_1 should be driven to wdf_a_debug_out.

Bits	SCOM	Field Mnemonic: Description
18	RW	DBG_SEL_WDFWR_DEBUG_0: Indicates that internal debug data wdfwr_debug_0 should be driven to wdf_a_debug_out.
19	RW	DBG_SEL_WDFWR_DEBUG_1: Indicates that internal debug data wdfwr_debug_1 should be driven to wdf_a_debug_out.
20	RW	DBG_SEL_SEC_WDFRD_DEBUG_0: Indicates that internal debug data sec_wdfrd_debug_0 should be driven to wdf_a_debug_out.
21	RW	DBG_SEL_SEC_WDFRD_DEBUG_1: Indicates that internal debug data sec_wdfrd_debug_1 should be driven to wdf_a_debug_out.
22:31	RW	DBG_SPARE: Spare bits.
32	RW	WAT_EVENT_ENABLE: Enable latching of wat_event_in.
33:35	RW	WAT_SPARE1: WAT spare.
36:39	RW	WAT0_EVENT_SELECT: Select for wat_action(0).
40:43	RW	WAT1_EVENT_SELECT: Select for wat_action(1).
44:63	RO	Constant = 0b00000000000000000000

Register Name	**Write Buffer Miscellaneous Configuration Register**
Mnemonic	MC01.PORT2.WRITE.WRTCFG
Address	0000000007010AB8 (SCOM)
Description	Write buffer miscellaneous configuration

Bits	SCOM	Field Mnemonic: Description
0	RW	CFG_WRITE_MODE_ECC_CHK_DIS: Disables 8-byte ECC checking on write-buffer read ports.
1	RW	CFG_WRITE_MODE_ECC_COR_DIS: Disables 8-byte ECC correction on write-buffer read ports.
2	RW	RESET_KEEPER: Reset miscellaneous c_err_rpt keepers in write buffer logic.
3	RW	MPIPL: mpipl.
4:7	RW	ASYNC_INJ: Asynchronous error inject.
8:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	**Write Buffer WRQ Register**
Mnemonic	MC01.PORT2.WRITE.WRT_ECC
Address	0000000007010AB9 (SCOM)
Description	Port ECC error information register

Bits	SCOM	Field Mnemonic: Description
0:2	RWX_WCLRPART	WRT_ECC_DW0_ERR_TYPE: The ECC checker detected the following types of errors in write buffer WRQ read port doubleword 0: bit 0 = CE bit 1 = UE bit 2 = SUE
3:7	RO	Constant = 0b00000
8:15	RWX_WCLRPART	WRT_ECC_DW0_SYNDROME: Write buffer WRQ read port doubleword 0 ECC checker syndrome.

Bits	SCOM	Field Mnemonic: Description
16:18	RWX_WCLRPART	WRT_ECC_DW1_ERR_TYPE: The ECC checker detected the following types of errors in write buffer WRQ read port doubleword 1: bit 0 = CE bit 1 = UE bit 2 = SUE
19:23	RO	Constant = 0b00000
24:31	RWX_WCLRPART	WRT_ECC_DW1_SYNDROME: Write buffer WRQ read port doubleword 1 ECC checker syndrome.
32:34	RWX_WCLRPART	WRT_ECC_DW2_ERR_TYPE: The ECC checker detected the following types of errors in write buffer WRQ read port doubleword 2: bit 0 = CE bit 1 = UE bit 2 = SUE
35:39	RO	Constant = 0b00000
40:47	RWX_WCLRPART	WRT_ECC_DW2_SYNDROME: Write buffer WRQ read port doubleword 2 ECC checker syndrome.
48:50	RWX_WCLRPART	WRT_ECC_DW3_ERR_TYPE: The ECC checker detected the following types of errors in write buffer WRQ read port doubleword 3: bit 0 = CE bit 1 = UE bit 2 = SUE
51:55	RO	Constant = 0b00000
56:63	RWX_WCLRPART	WRT_ECC_DW3_SYNDROME: Write buffer WRQ read port doubleword 3 ECC checker syndrome.

Register Name	WRT MCA Debug Control Register
Mnemonic	MC01.PORT2.WRITE.WRTDBGMCA
Address	0000000007010ABA (SCOM)
Description	WRT MCA debug control

Bits	SCOM	Field Mnemonic: Description
0	RW	MCA_DBG_SEL_IN: Indicates that write_a_debug_in should be driven to write_a_debug_out.
1	RW	MCA_DBG_SEL_WRT: Indicates that internal debug data should be driven to write_a_debug_out.
2	RW	WBRD_DEBUG_0_SELECT: Indicates that internal debug data wbrd_debug_0 should be driven to write_a_debug_out.
3	RW	WBRD_DEBUG_1_SELECT: Indicates that internal debug data wbrd_debug_1 should be driven to write_a_debug_out.
4	RW	SEC_WBRD_DEBUG_0_SELECT: Indicates that internal debug data sec_wbrd_debug_0 should be driven to write_a_debug_out.
5	RW	SEC_WBRD_DEBUG_1_SELECT: Indicates that internal debug data sec_wbrd_debug_1 should be driven to write_a_debug_out.
6:15	RW	DBG_SPARE_MCA: Spare bits.
16	RW	WAT_EVENT_ENABLE_MCA: Enable latching of wat_event_in.
17:19	RW	WAT_SPARE1_MCA: WAT spare.
20:23	RW	WAT0_EVENT_SELECT_MCA: Select for wat_action(0).

Bits	SCOM	Field Mnemonic: Description
24:27	RW	WAT1_EVENT_SELECT_MCA: Select for wat_action(1).
28:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	WRT Nest Debug Control Register
Mnemonic	MC01.PORT2.WRITE.WRTDBGNEST
Address	0000000007010ABB (SCOM)
Description	WRT nest debug control

Bits	SCOM	Field Mnemonic: Description
0	RW	NEST_DBG_SEL_IN: Indicates that write_s_debug_in should be driven to write_s_debug_out.
1	RW	NEST_DBG_SEL_WRT: Indicates that internal debug data should be driven to write_s_debug_out.
2	RW	WBMGR_DBG_0_SELECT: Indicates that internal debug data wbmgr_0_debug should be driven to write_s_debug_out.
3	RW	WBMGR_DBG_1_SELECT: Indicates that internal debug data wbmgr_1_debug should be driven to write_s_debug_out.
4	RW	WRCNTL_DBG_SELECT: Indicates that internal debug data wrcntl_debug should be driven to write_s_debug_out.
5:15	RW	DBG_SPARE_NEST: Spare bits.
16	RW	WAT_EVENT_ENABLE_NEST: Enable latching of wat_event_in.
17:19	RW	WAT_SPARE1_NEST: WAT spare.
20:23	RW	WAT0_EVENT_SELECT_NEST: Select for wat_action(0).
24:27	RW	WAT1_EVENT_SELECT_NEST: Select for wat_action(1).
28:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Datapath Fault Isolation Register
Mnemonic	MC01.PORT3.ECC64.SCOM.FIR
Address	0000000007010AC0 (SCOM) 0000000007010AC1 (SCOM1) 0000000007010AC2 (SCOM2)
Description	Datapath Fault Isolation Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:7	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_MPE_RANK_0_TO_7: Mark placed error (MPE) detected on a mainline read. The corresponding Hardware Mark Store Register (HWMSx [x = 0..7]) is updated with a chipmark for the associated master rank.
8	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_NCE: New correctable error (NCE) detected on a mainline read.
9	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_TCE: Two-symbol correctable error (TCE) detected on a mainline read.
10	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_SCE: Symbol mark corrected error (SCE) detected on a mainline read.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
11	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_MCE: Chip mark corrected error (MCE) detected on a mainline read.
12	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_SUE: Special uncorrectable error (SUE) detected on a mainline read.
13	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_AUE: Address uncorrectable error (AUE) detected on a mainline read.
14	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_UE: Uncorrectable error (UE) detected on a mainline read.
15	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_RCD: Parity error detected by registering clock driver (RCD) detected on a mainline read.
16	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_IAUE: Intermittent AUE (IAUE) detected on a mainline read.
17	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_IUE: Intermittent UE (IUE) detected on a mainline read.
18	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_IRCD: Intermittent RCD (IRCD) detected on a mainline read.
19	RWX	WOX_AND	WOX_OR	FIR_MAINLINE_IMPE: Intermittent MPE (IMPE) detected on a mainline read.
20:27	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_MPE_RANK_0_TO_7: Mark placed error (MPE) detected on a maintenance read. The corresponding Hardware Mark Store Register (HWMSx [x = 0..7]) is updated with a chipmark for the associated master rank.
28	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_NCE: New correctable error (NCE) detected on a maintenance read.
29	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_TCE: Two-symbol correctable error (TCE) detected on a maintenance read.
30	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_SCE: Symbol mark corrected error (SCE) detected on a maintenance read.
31	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_MCE: Chip mark corrected error (MCE) detected on a maintenance read.
32	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_SUE: Special uncorrectable error (SUE) detected on a maintenance read.
33	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_AUE: Address uncorrectable error (AUE) detected on a maintenance read.
34	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_UE: Uncorrectable error (UE) detected on a maintenance read.
35	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_RCD: Parity error detected by registering clock driver (RCD) detected on a maintenance read.
36	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_IAUE: Intermittent AUE (IAUE) detected on a maintenance read.
37	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_IUE: Intermittent UE (IUE) detected on a maintenance read.
38	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_IRCD: Intermittent RCD (IRCD) detected on a maintenance read.
39	RWX	WOX_AND	WOX_OR	FIR_MAINTENANCE_IMPE: Intermittent MPE (IMPE) detected on a maintenance read.
40	RWX	WOX_AND	WOX_OR	FIR_RESERVED_40: Reserved.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
41	RWX	WOX_AND	WOX_OR	FIR_SCOM_PARITY_CLASS_STATUS: SCOM register parity error, for registers in the “status”’class (no data integrity risk). For additional information, see Error Report Hold Register 0 (SCOM Register Parity Errors) on page 214.
42	RWX	WOX_AND	WOX_OR	FIR_SCOM_PARITY_CLASS_RECOVERABLE: SCOM register parity error, for registers in the “recoverable” class (no data integrity risk; register must be reloaded). For additional information, see Error Report Hold Register 0 (SCOM Register Parity Errors) on page 214.
43	RWX	WOX_AND	WOX_OR	FIR_SCOM_PARITY_CLASS_UNRECOVERABLE: SCOM register parity error, for registers in the “unrecoverable” class (data integrity risk). For additional information, see Error Report Hold Register 0 (SCOM Register Parity Errors) on page 214.
44	RWX	WOX_AND	WOX_OR	FIR_ECC_CORRECTOR_INTERNAL_PARITY_ERROR: ECC corrector internal parity error. Data Integrity risk. For additional information, see Error Report Hold Register 1 on page 215.
45	RWX	WOX_AND	WOX_OR	FIR_WRITE_RMW_CE: CE detected at Write or RMW buffer read port. For additional information, see Error Report Hold Register 1 on page 215 and Write Buffer WRQ Register on page 224.
46	RWX	WOX_AND	WOX_OR	FIR_WRITE_RMW_UE: UE detected at Write or RMW buffer read port. For additional information, see Error Report Hold Register 1 on page 215 and Write Buffer WRQ Register on page 224.
47	RWX	WOX_AND	WOX_OR	FIR_WRITE_RMW_SUE: SUE detected at Write or RMW buffer read port. For additional information, see Error Report Hold Register 1 on page 215 and Write Buffer WRQ Register on page 224.
48	RWX	WOX_AND	WOX_OR	FIR_WDF_OVERRUN_ERROR_0: WDF logic detected a buffer overrun error (class 0).
49	RWX	WOX_AND	WOX_OR	FIR_WDF_OVERRUN_ERROR_1: WDF logic detected a buffer overrun error (class 1).
50	RWX	WOX_AND	WOX_OR	FIR_WDF_SCOM_SEQUENCE_ERROR: WDF logic detected a SCOM sequence error.
51	RWX	WOX_AND	WOX_OR	FIR_WDF_STATE_MACHINE_ERROR: WDF logic detected a state machine error.
52	RWX	WOX_AND	WOX_OR	FIR_WDF_MISC_REGISTER_PARITY_ERROR: WDF logic detected a miscellaneous register parity error.
53	RWX	WOX_AND	WOX_OR	FIR_WRT_SCOM_SEQUENCE_ERROR: WRT logic detected a SCOM sequence error.
54	RWX	WOX_AND	WOX_OR	FIR_WRT_MISC_REGISTER_PARITY_ERROR: WRT logic detected a miscellaneous register parity error.
55	RWX	WOX_AND	WOX_OR	FIR_ECC_GENERATOR_INTERNAL_PARITY_ERROR: ECC generator internal parity error (data integrity risk).
56	RWX	WOX_AND	WOX_OR	FIR_READ_BUFFER_OVERFLOW_ERROR: Read buffer overflow error (data integrity risk).
57	RWX	WOX_AND	WOX_OR	FIR_WDF_ASYNC_INTERFACE_ERROR: WDF asynchronous interface error.
58	RWX	WOX_AND	WOX_OR	FIR_READ_ASYNC_INTERFACE_PARITY_ERROR: Read asynchronous interface parity error.
59	RWX	WOX_AND	WOX_OR	FIR_READ_ASYNC_INTERFACE_SEQUENCE_ERROR: Read asynchronous interface sequence error.
60:61	RWX	WOX_AND	WOX_OR	FIR_RESERVED: Reserved.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
62	RWX	WOX_AND	WOX_OR	FIR_INTERNAL_SCOM_ERROR: A SCOM/FIR internal error has occurred.
63	RWX	WOX_AND	WOX_OR	FIR_INTERNAL_SCOM_ERROR_COPY: A SCOM/FIR internal error has occurred (redundant copy).

Register Name	Datapath FIR Mask Register
Mnemonic	MC01.PORT3.ECC64.SCOM.MASK
Address	0000000007010AC3 (SCOM) 0000000007010AC4 (SCOM1) 0000000007010AC5 (SCOM2)
Description	Datapath FIR mask

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:63	RW	WO_AND	WO_OR	MASK_FIR_MASK: MASK for FIR bits 0:63.

Register Name	Datapath FIR Action 0 Register
Mnemonic	MC01.PORT3.ECC64.SCOM.ACTION0
Address	0000000007010AC6 (SCOM)
Description	Datapath FIR action 0

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ACTION0_FIR_ACTION0: Action0 select for the corresponding bits in the FIR. (Action0, Action1, Mask) selects: (0,0,0) = Checkstop error (0,1,0) = Recoverable error (1,0,0) = Attention (1,1,0) = Local checkstop error (X,X,1) = Masked

Register Name	Datapath FIR Action 1 Register
Mnemonic	MC01.PORT3.ECC64.SCOM.ACTION1
Address	0000000007010AC7 (SCOM)
Description	Datapath FIR action 1

Bits	SCOM	Field Mnemonic: Description
0:63	RW	ACTION1_FIR_ACTION1: Action1 select for the corresponding bits in the FIR. (Action0, Action1, Mask) selects: (0,0,0) = Checkstop error (0,1,0) = Recoverable error (1,0,0) = Attention (1,1,0) = Local checkstop error (X,X,1) = Masked

Register Name	Datapath FIR “Who is On First” Register
Mnemonic	MC01.PORT3.ECC64.SCOM.WOF
Address	0000000007010AC8 (SCOM)
Description	Datapath FIR 'Who is On First'

Bits	SCOM	Field Mnemonic: Description
0:63	RWX_WCLRREG	WOF_FIR_WOF: WOF register locks on the first error. Writing zeros the register.

Register Name	Read ECC Control Register
Mnemonic	MC01.PORT3.ECC64.SCOM.RECR
Address	0000000007010ACA (SCOM)
Description	Read ECC Control Register

Bits	SCOM	Field Mnemonic: Description
0	RW	MBSECCQ_DISABLE_MEMORY_ECC_CHECK_CORRECT: When set, memory ECC check and correct is disabled. When memory ECC checking is disabled, the SUE injecting into the 8-byte data bus ECC is also disabled.
1	RW	MBSECCQ_DISABLE_MEMORY_ECC_CORRECT: When set, memory ECC correct is disabled (memory ECC checking is not disabled).
2	RW	MBSECCQ_DISABLE_MARK_STORE_WRITE: Disables update of the HWMSx registers on an MPE.
3	RW	MBSECCQ_DISABLE_UE_RETRY: When off, a read diagnosed as an exit-point-2 uncorrectable error (UE, AUE, or RCD) is retried. The FIR set if the problem reoccurs on the retry. If the problem does not reoccur, the IUE/IAUE/IRCD FIR is set. When on, the UE/AUE/RCD FIRs are set immediately, and the IUE/IAUE/IRCD FIRs are not set.
4	RW	MBSECCQ_ITAG_METADATA_ENABLE: Enables I-series tag bits in the metadata symbols. When this dial is not set, the tag bits are used as four additional check bits.
5	RW	MBSECCQ_SLOW_EXIT_REDUCTION: When set, exit selection is modified to prevent the pileup of output data beats by choosing a later exit than would normally be used. Latency is increased. This mode is intended as a workaround to potential read_mac asynchronous interface issues.
6:8	RW	MBSECCQ_READ_POINTER_DELAY: Read pointer delay (mba_mbx_rdtag_val to mbr_ddr_clock_en) is (dial value + 2) MEMx2 cycles. Interacts with the MBSECCQ_ECC_SCHEDULER_DELAY according to the following formula: rdptrdly + 3 + (staging latches to PHY on mbr_ddr_* and from PHY on ddr_mbr_rdata) = scheddly + 7 Both rdptrdly and scheddly must be in the range 0 - 7.
9:10	RW	MBSECCQ_EXIT_OVERRIDE: Non-zero settings are for debug operation only.
11	RW	MBSECCQ_HWMARK_EXIT1: Selects the value to which HWMSx(9) [exit_1] is set when hardware sets a chipmark.

Bits	SCOM	Field Mnemonic: Description
12	RW	MBSECCQ_DATA_GENERATOR_OVERRIDE: Also known as “wrap mode.” When set, it overrides ECC corrector data output with an address-based data pattern. In each doubleword: bits(0:15) = 0xdead bits(16:19) = port index (0..7) bits(20:22) = 0 bit(23) = DIMM bits(24:25) = master rank bits(26:28) = slave rank bits(29:30) = bank group bits(31:33) = bank bits(34:51) = row(0:17) bits(52:59) = col(2:9) bits(60:63) = doubleword index (0 to 3) Metadata (I-series tags and MDI bit) will be zero. **Note**: Wrap mode also requires Exit_Override set to 0b01 (force_exit_0).
13:15	RW	MBSECCQ_ECC_SCHEDULER_DELAY: ECC scheduler delay (mba_mbx_rdtag_val to scheduler start). See MBSECCQ_Read_Pointer_Delay.
16:18	RW	MBSECCQ_VAL_TO_DATA_DELAY: Asynchronous side 2x cycle delay from ecc_tag_valid_rd to data valid. It affects the the asynchronous interface.
19	RW	MBSECCQ_DELAY_VALID_1X: When set, read control delays ecc_tag_valid_rd by one mca 1x cycle. In effect, it subtracts 0.5 from val_to_data_delay.
20:21	RW	MBSECCQ_NEST_VAL_TO_DATA_DELAY: Number of extra nest cycles of delay from tag to data. The valid range is 0 - 2. It affects the asynchronous interface.
22	RW	MBSECCQ_DELAY_NONBYPASS: When set, adds one extra nest cycle delay for nonbypass data (needed for null_xfer/retry signal).
23	RW	MBSECCQ_ENABLE_SPECIAL_ATTENTION: When set, FIRs with action set to 10 assert special_attention.
24	RW	MBSECCQ_ENABLE_HOST_ATTENTION: When set, FIRs with action set to 10 assert host_attention.
25	RW	MBSECCQ_DISABLE_MPE_CONFIRM: When set, hardware marks are placed in the confirmed state.
26	RW	MBSECCQ_ENABLE_UE_NOISE_WINDOW: Enables noise window processing whenever a UE (or AUE) is detected.
27	RW	MBSECCQ_ENABLE_TCE_CORRECTION: Enables two-symbol error correction.
28	RW	MBSECCQ_ENABLE_CHIPMARKED_SCE_NCE: Enables correction of a marked symbol, and one unmarked symbol, when there is a chip mark (but no error in the marked chip).
29	RW	MBSECCQ_USE_ADDRESS_HASH: Enables use of an address hash in the ECC.
30:31	RW	MBSECCQ_DATA_INVERSION: Controls inversion of data to or from the PHY. Data and checks (including metadata) can be inverted for data beats where col(2) = 1. Or, data can be set to always invert, while checks invert where col(2) = 1.
32	RW	MBSECCQ_DISABLE_PIPE_NOERR_CLOCK_GATING: Disables these no-err/no-change clock gating features in ECC pipe: 1. Mark precomputation is normally held while marks remain the same (for example, all-0). 2. Post-syndrome ECC computation stages are held while there is no new error.
33	RW	MBSECCQ_MAINT_NO_RETRY_UE: Maintenance equivalent of Disable_ue_retry (bit 3).
34	RW	MBSECCQ_MAINT_NO_RETRY_MPE: Maintenance equivalent of disable_MPE_confirm (bit 25).
35	RW	MBSECCQ_DISABLE_BYPASS_TEMPLATE_A: Disables least-latency mode for 128-byte bypass reads, so that beat 1 will have an SUE in case of a bypass error on beat 0.
36:43	RW	MBSECCQ_RESERVED_36_43: Reserved.

Register Name	**ECC Debug/WAT Control Register**
Mnemonic	MC01.PORT3.ECC64.SCOM.DBGR
Address	0000000007010ACB (SCOM)
Description	ECC Debug/WAT Control Register

Bits	SCOM	Field Mnemonic: Description
0	RW	DBGR_ECC_DEBUG_ENABLE: Enable a debug bus in the ecc64 macro. Required for the debug of ecc64 or SRQ.
1:2	RW	DBGR_ECC_DEBUG_CHUNK_SELECT: Select 0,1, 2, or 4 22-bit data chunks from ECC debug sources. ECC data is inserted in the debug bus as follows: 00 = inp inp inp inp 01 = inp inp inp ecc 10 = inp inp ecc ecc 11 = ecc ecc ecc ecc Other fields of the debug bus output propagate the input (inp).
3:5	RW	DBGR_ECC_DEBUG_PRIMARY_SELECT: Primary select for the ECC debug source. 000 = sch1 sch2 ep21 ep22 / - - ep21 ep22 / - - - ep22 001 = sch1 sch2 ep22 ep21 / - - ep22 ep21 / - - - ep21 010 = ep21 ep22 wrd1 wrd2 / - - wrd1 wrd2 / - - - wrd2 011 = ep21 ep22 wrd2 wrd1 / - - wrd2 wrd1 / - - - wrd1 100 = wrd1 wrd2 sch1 sch2 / - - sch1 sch2 / - - - sch2 101 = wrd1 wrd2 sch2 sch1 / - - sch2 sch1 / - - - sch1 where: sch1 and sch2 are collections of debug information for the ECC corrector's scheduler logic. ep21 and ep22 are collections of debug information related to the exit-point-2 state logic. wrd1 and wrd2 are collections of debug information related to the write data logic.
6:7	RW	DBGR_ECC_DEBUG_SECONDARY_SELECT: Secondary select for the ECC debug data. Action varies by the primary source bus.
8	RW	DBGR_ECC_WAT_ENABLE: Enable workaround logic in the ECC corrector.
9	RW	DBGR_ECC_WAT_ACTION_SELECT: Select workaround action: 0 = Bypass disable (while the selected WAT event is 1). 1 = Force exit 2 (while the selected WAT event is 1).
10:11	RW	DBGR_ECC_WAT_SOURCE: Select the WAT event (bit 0 to 3).
12:14	RW	DBGR_READ_DEBUG_SELECT: Select the debug source data in the read macro.

Register Name	**Mark Shadow Register**
Mnemonic	MC01.PORT3.ECC64.SCOM.MSR
Address	0000000007010ACC (SCOM)
Description	Mark Shadow Register

Bits	SCOM	Field Mnemonic: Description
0:7	RO	Constant = 0b00000000
8:15	ROX	MSR_CHIPMARK: Mark location (Galois field code) of the last mark placed (includes unconfirmed marks).
16:18	ROX	MSR_RANK: Rank of the last mark placed (includes unconfirmed marks).
19:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000

Register Name	Error Inject Control Register
Mnemonic	MC01.PORT3.ECC64.SCOM.EICR
Address	0000000007010ACD (SCOM)
Description	Error Inject Control Register

Bits	SCOM	Field Mnemonic: Description
0:36	RW	EICR_ADDRESS: An error is injected when the read address matches the EICR address, up to fields masked by the EICR region. bit 0 = DIMM select bits 1:2 = mrank(0:1) bits 3:5 = srank(0:2) bits 6:7 = bank_group(0:1) bits 8:10 = bank(0:2) bits 11:28 = row(0:17) bits 29:36 = col(2:9)
37	RW	EICR_RESERVED: Reserved.
38:39	RW	EICR_PERSIST: Persistence of the injected error. Set to disabled (00) to disable error injection. It affects the memory ECC error injection selected via the type field, or miscellaneous injection via the MISC field.
40:42	RW	EICR_REGION: Address region size for the error inject.
43:47	RW	EICR_TYPE: Bitmask for the error type to inject. bit 43: Inject address UE bit 44: Inject DQ 0 (symbol 71, Galois code 0x38) bit 45: Inject DQ 1 (symbol 70, Galois code 0xa2) bit 46: Inject DQ 4 (symbol 39, Galois code 0x46) bit 47: Inject DQ 5,6 (symbols 38,37, Galois codes 0x1d, x0f4)
48:51	RW	EICR_MISC: Selects miscellaneous error injections: • 8-byte ECC error injection at the output of the memory ECC checker. Inject a CE in bit 0 or bit 1, or a UE in both bits. Any data read from memory into either the RMW buffer or READ buffer will be injected. Errors should be visible in RMW ECC checkers or in the read master's ECC checkers. • Inject FIR(44) = ecc_corrector_internal_parity_error. • Inject read path asynchronous interface errors (parity or sequence_check). Miscellaneous errors are not affected by the address or region, but are affected by persistence (both soft_error and hard_error persistence act as a continuous inject). Undefined codes inject no error.

Register Name	Error Report Hold Register 0 (SCOM Register Parity Errors)
Mnemonic	MC01.PORT3.ECC64.SCOM.CERR0
Address	0000000007010ACE (SCOM)
Description	Each register parity error is reported in the bit location corresponding to the least-significant 6 bits of the register's SCOM address. Writing the CERR0 register clears all hold bits in CERR0 and CERR1.

Bits	SCOM	Field Mnemonic: Description
0:9	RO	Constant = 0b0000000000
10	RWX_WCLRREG	CERR0_RECR_PE: RECR parity error (FIR 43).
11	RO	Constant = 0b0

Bits	SCOM	Field Mnemonic: Description
12	RWX_WCLRREG	CERR0_MSR_PE: MSR parity error (FIR 41).
13	RWX_WCLRREG	CERR0_EICR_PE: EICR parity error (FIR 42).
14:15	RO	Constant = 0b00
16:23	RWX_WCLRREG	CERR0_HWMSX_PE: HWMSx parity error (FIR 42).
24:31	RWX_WCLRREG	CERR0_FWMSX_PE: FWMSx parity error (FIR 42).
32:39	RO	Constant = 0b00000000
40	RWX_WCLRREG	CERR0_WECR_PE: WECR parity error (FIR 43).
41	RWX_WCLRREG	CERR0_AACR_PE: AACR parity error (FIR 42).
42	RWX_WCLRREG	CERR0_AADR_PE: AADR parity error (FIR 42).
43	RWX_WCLRREG	CERR0_AAER_PE: AAER parity error (FIR 42).
44	RWX_WCLRREG	CERR0_MCBCM_PE: MCBCM parity error (FIR 42).
45:47	RO	Constant = 0b000
48	RWX_WCLRREG	CERR0_WDFCFG_PE: WDFCFG parity error (FIR 52).
49:55	RO	Constant = 0b0000000
56	RWX_WCLRREG	CERR0_WRTCFG_PE: WRTCFG parity error (FIR 54).
57:63	RO	Constant = 0b0000000

Register Name	Error Report Hold Register 1
Mnemonic	MC01.PORT3.ECC64.SCOM.CERR1
Address	0000000007010ACF (SCOM)
Description	Contains error hold bits for errors other than SCOM register parity errors. Writing the CERR0 register clears all hold bits in CERR0 and CERR1. CERR1 makes various internal error detections visible.

Bits	SCOM	Field Mnemonic: Description
0	ROX	CERR1_ECC_CTL_AF_PERR: Sticky bit for a read ECC control-logic address FIFO parity error (FIR 44).
1	ROX	CERR1_ECC_CTL_RPTR_PERR: Sticky bit for a read ECC control-logic read-pointer timer parity error (FIR 44).
2	ROX	CERR1_ECC_CTL_TCHN_PERR: Sticky bit for a read ECC control-logic main timer parity error (FIR 44).
3	ROX	CERR1_ECC_CTL_CMPMODE_ERR: Sticky bit for a read ECC control-logic compare-mode error (FIR 44).
4	ROX	CERR1_ECC_CTL_SCHCTL_PERR: Sticky bit for a read ECC control-logic scheduler control parity error (FIR 44).
5	ROX	CERR1_ECC_CTL_PCTL_PERR: Sticky bit for a read ECC control-logic pipe control parity error (FIR 44).
6	ROX	CERR1_ECC_CTL_TGST_PERR: Sticky bit for a read ECC control-logic retry state parity error (FIR 44).

Bits	SCOM	Field Mnemonic: Description
7	ROX	CERR1_ECC_CTL_SCHTAB_PERR: Sticky bit for a read ECC control-logic schedule table parity error (FIR 44).
8	ROX	CERR1_ECC_PIPE_PCX_PERR: Sticky bit for a read ECC mark precomputation parity error (FIR 44).
9	ROX	CERR1_ECC_PIPE_SYND_PERR: Sticky bit for a read ECC syndrome parity error (FIR 44).
10	ROX	CERR1_ECC_PIPE_2SYM_PERR: Sticky bit for a read ECC 2-symbol corrector parity error (FIR 44).
11	ROX	CERR1_ECC_PIPE_CPLX_PERR: Sticky bit for a read ECC complex corrector parity error (FIR 44).
12	ROX	CERR1_ECC_PIPE_EP2_PERR: Sticky bit for a read ECC exit-2 parity error (FIR 44).
13	ROX	CERR1_READ_ECC_DATAPATH_PARITY_ERROR: Sticky bit for a read ECC datapath parity error (FIR 44).
14	ROX	CERR1_PHY_RPTR_PARITY_ERROR: Sticky bit for a DDR PHY read pointer parity error (FIR 44).
15	ROX	CERR1_ECC_CTL_RPD_PERR: Sticky bit for a read ECC control-logic pointer delay logic parity error (FIR 44).
16	ROX	CERR1_WDF_ASYNC_ERROR: Sticky bit for a WDF asynchronous interface error (FIR 57).
17	ROX	CERR1_WDF_BUFFER_CE: Sticky bit for a WDF buffer CE (FIR 45).
18	ROX	CERR1_WDF_BUFFER_UE: Sticky bit for a WDF buffer UE (FIR 46).
19	ROX	CERR1_WDF_BUFFER_SUE: Sticky bit for a WDF buffer SUE (FIR 47).
20:24	RO	Constant = 0b00000
25	ROX	CERR1_WRT_BUFFER_CE: Sticky bit for a write buffer CE (FIR 45).
26	ROX	CERR1_WRT_BUFFER_UE: Sticky bit for a write buffer UE (FIR 46).
27	ROX	CERR1_WRT_BUFFER_SUE: Sticky bit for a write buffer SUE (FIR 47).
28:31	RO	Constant = 0b0000
32	ROX	CERR1_READ_CONTROL_OVERFLOW_ERROR: Sticky bit for a read buffer overflow error (FIR 56).
33:39	RO	Constant = 0b0000000
40	ROX	CERR1_WRITE_ECC_DATAPATH_ERROR: Sticky bit for a write ECC datapath parity error (FIR 55).
41:63	RO	Constant = 0b00000000000000000000000

Register Name	**Hardware Mark Store Rank 0 Register**
Mnemonic	MC01.PORT3.ECC64.SCOM.HWMS0
Address	0000000007010AD0 (SCOM)
Description	Hardware mark store rank 0

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	HWMS0_CHIPMARK: Hardware chipmark (Galois field code) for rank 0.
8	RWX	HWMS0_CONFIRMED: Chipmark confirmed.
9	RW	HWMS0_EXIT_1: When set, bypass-enabled reads using this mark use exit 1; otherwise, they use exit 0.

Register Name	**Hardware Mark Store Rank 1 Register**
Mnemonic	MC01.PORT3.ECC64.SCOM.HWMS1
Address	0000000007010AD1 (SCOM)
Description	Hardware mark store rank 1

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	HWMS1_CHIPMARK: Hardware chipmark (Galois field code) for rank 1.
8	RWX	HWMS1_CONFIRMED: Chipmark confirmed.
9	RW	HWMS1_EXIT_1: When set, bypass-enabled reads using this mark use exit 1; otherwise, they use exit 0.

Register Name	Hardware Mark Store Rank 2 Register
Mnemonic	MC01.PORT3.ECC64.SCOM.HWMS2
Address	0000000007010AD2 (SCOM)
Description	Hardware mark store rank 2

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	HWMS2_CHIPMARK: Hardware chipmark (Galois field code) for rank 2.
8	RWX	HWMS2_CONFIRMED: Chipmark confirmed.
9	RW	HWMS2_EXIT_1: When set, bypass-enabled reads using this mark use exit 1; otherwise, they use exit 0.

Register Name	Hardware Mark Store Rank 3 Register
Mnemonic	MC01.PORT3.ECC64.SCOM.HWMS3
Address	0000000007010AD3 (SCOM)
Description	Hardware mark store rank 3

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	HWMS3_CHIPMARK: Hardware chipmark (Galois field code) for rank 3.
8	RWX	HWMS3_CONFIRMED: Chipmark confirmed.
9	RW	HWMS3_EXIT_1: When set, bypass-enabled reads using this mark use exit 1; otherwise, they use exit 0.

Register Name	Hardware Mark Store Rank 4 Register
Mnemonic	MC01.PORT3.ECC64.SCOM.HWMS4
Address	0000000007010AD4 (SCOM)
Description	Hardware mark store rank 4

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	HWMS4_CHIPMARK: Hardware chipmark (Galois field code) for rank 4.
8	RWX	HWMS4_CONFIRMED: Chipmark confirmed.
9	RW	HWMS4_EXIT_1: When set, bypass-enabled reads using this mark use exit 1; otherwise, they use exit 0.

Register Name	Hardware Mark Store Rank 5 Register
Mnemonic	MC01.PORT3.ECC64.SCOM.HWMS5
Address	0000000007010AD5 (SCOM)
Description	Hardware mark store rank 5

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	HWMS5_CHIPMARK: Hardware chipmark (Galois field code) for rank 5.
8	RWX	HWMS5_CONFIRMED: Chipmark confirmed.
9	RW	HWMS5_EXIT_1: When set, bypass-enabled reads using this mark use exit 1; otherwise, they use exit 0.

Register Name	Hardware Mark Store Rank 6 Register
Mnemonic	MC01.PORT3.ECC64.SCOM.HWMS6
Address	0000000007010AD6 (SCOM)
Description	Hardware mark store rank 6

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	HWMS6_CHIPMARK: Hardware chipmark (Galois field code) for rank 6.
8	RWX	HWMS6_CONFIRMED: Chipmark confirmed.
9	RW	HWMS6_EXIT_1: When set, bypass-enabled reads using this mark use exit 1; otherwise, they use exit 0.

Register Name	Hardware Mark Store Rank 7 Register
Mnemonic	MC01.PORT3.ECC64.SCOM.HWMS7
Address	0000000007010AD7 (SCOM)
Description	Hardware mark store rank 7

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	HWMS7_CHIPMARK: Hardware chipmark (Galois field code) for rank 7.
8	RWX	HWMS7_CONFIRMED: Chipmark confirmed.
9	RW	HWMS7_EXIT_1: When set, bypass-enabled reads using this mark use exit 1; otherwise, they use exit 0.

Register Name	Firmware Mark Store 0 Register
Mnemonic	MC01.PORT3.ECC64.SCOM.FWMS0
Address	0000000007010AD8 (SCOM)
Description	Firmware mark store 0

Bits	SCOM	Field Mnemonic: Description
0:7	RW	FWMS0_MARK: Mark (Galois field code).
8	RW	FWMS0_TYPE: Mark type.
9:11	RW	FWMS0_REGION: Selects the mark region (address range to which the mark applies).
12:22	RW	FWMS0_ADDRESS: Mark region address. bit 12 = DIMM bits 13:14 = mrank bits 15:17 = srank bits 18:19 = bank group bits 20:22 = bank (reserving space for 32 total banks)
23	RW	FWMS0_EXIT_1: When set, bypass-enabled reads using this mark use exit 1.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000

Register Name	Firmware Mark Store 1 Register
Mnemonic	MC01.PORT3.ECC64.SCOM.FWMS1
Address	0000000007010AD9 (SCOM)
Description	Firmware mark store 1

Bits	SCOM	Field Mnemonic: Description
0:7	RW	FWMS1_MARK: Mark (Galois field code).
8	RW	FWMS1_TYPE: Mark type.
9:11	RW	FWMS1_REGION: Selects the mark region (address range to which the mark applies).
12:22	RW	FWMS1_ADDRESS: Mark region address. bit 12 = DIMM bits 13:14 = mrank bits 15:17 = srank bits 18:19 = bank group bits 20:22 = bank (reserving space for 32 total banks)
23	RW	FWMS1_EXIT_1: When set, bypass-enabled reads using this mark use exit 1.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Firmware Mark Store 2 Register
Mnemonic	MC01.PORT3.ECC64.SCOM.FWMS2
Address	0000000007010ADA (SCOM)
Description	Firmware mark store 2

Bits	SCOM	Field Mnemonic: Description
0:7	RW	FWMS2_MARK: Mark (Galois field code).
8	RW	FWMS2_TYPE: Mark type.
9:11	RW	FWMS2_REGION: Selects the mark region (address range to which the mark applies).
12:22	RW	FWMS2_ADDRESS: Mark region address. bit 12 = DIMM bits 13:14 = mrank bits 15:17 = srank bits 18:19 = bank group bits 20:22 = bank (reserving space for 32 total banks)
23	RW	FWMS2_EXIT_1: When set, bypass-enabled reads using this mark use exit 1.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Firmware Mark Store 3 Register
Mnemonic	MC01.PORT3.ECC64.SCOM.FWMS3
Address	0000000007010ADB (SCOM)
Description	Firmware mark store 3

Bits	SCOM	Field Mnemonic: Description
0:7	RW	FWMS3_MARK: Mark (Galois field code).
8	RW	FWMS3_TYPE: Mark type.
9:11	RW	FWMS3_REGION: Selects the mark region (address range to which the mark applies).
12:22	RW	FWMS3_ADDRESS: Mark region address. bit 12 = DIMM bits 13:14 = mrank bits 15:17 = srank bits 18:19 = bank group bits 20:22 = bank (reserving space for 32 total banks)
23	RW	FWMS3_EXIT_1: When set, bypass-enabled reads using this mark use exit 1.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Firmware Mark Store 4 Register
Mnemonic	MC01.PORT3.ECC64.SCOM.FWMS4
Address	0000000007010ADC (SCOM)
Description	Firmware mark store 4

Bits	SCOM	Field Mnemonic: Description
0:7	RW	FWMS4_MARK: Mark (Galois field code).
8	RW	FWMS4_TYPE: Mark type.
9:11	RW	FWMS4_REGION: Selects the mark region (address range to which the mark applies).
12:22	RW	FWMS4_ADDRESS: Mark region address. bit 12 = DIMM bits 13:14 = mrank bits 15:17 = srank bits 18:19 = bank group bits 20:22 = bank (reserving space for 32 total banks)
23	RW	FWMS4_EXIT_1: When set, bypass-enabled reads using this mark use exit 1.
24:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	Firmware Mark Store 5 Register
Mnemonic	MC01.PORT3.ECC64.SCOM.FWMS5
Address	0000000007010ADD (SCOM)
Description	Firmware mark store 5

Bits	SCOM	Field Mnemonic: Description
0:7	RW	FWMS5_MARK: Mark (Galois field code).
8	RW	FWMS5_TYPE: Mark type.
9:11	RW	FWMS5_REGION: Selects the mark region (address range to which the mark applies).

Bits	SCOM	Field Mnemonic: Description
12:22	RW	FWMS5_ADDRESS: Mark region address. bit 12 = DIMM bits 13:14 = mrank bits 15:17 = srank bits 18:19 = bank group bits 20:22 = bank (reserving space for 32 total banks)
23	RW	FWMS5_EXIT_1: When set, bypass-enabled reads using this mark use exit 1.
24:63	RO	Constant = 0b0000000000000000000000000000000000000000

Register Name	Firmware Mark Store 6 Register
Mnemonic	MC01.PORT3.ECC64.SCOM.FWMS6
Address	0000000007010ADE (SCOM)
Description	Firmware mark store 6

Bits	SCOM	Field Mnemonic: Description
0:7	RW	FWMS6_MARK: Mark (Galois field code).
8	RW	FWMS6_TYPE: Mark type.
9:11	RW	FWMS6_REGION: Selects the mark region (address range to which the mark applies).
12:22	RW	FWMS6_ADDRESS: Mark region address. bit 12 = DIMM bits 13:14 = mrank bits 15:17 = srank bits 18:19 = bank group bits 20:22 = bank (reserving space for 32 total banks)
23	RW	FWMS6_EXIT_1: When set, bypass-enabled reads using this mark use exit 1.
24:63	RO	Constant = 0b0000000000000000000000000000000000000000

Register Name	Firmware Mark Store 7 Register
Mnemonic	MC01.PORT3.ECC64.SCOM.FWMS7
Address	0000000007010ADF (SCOM)
Description	Firmware mark store 7

Bits	SCOM	Field Mnemonic: Description
0:7	RW	FWMS7_MARK: Mark (Galois field code).
8	RW	FWMS7_TYPE: Mark type.
9:11	RW	FWMS7_REGION: Selects the mark region (address range to which the mark applies).
12:22	RW	FWMS7_ADDRESS: Mark region address. bit 12 = DIMM bits 13:14 = mrank bits 15:17 = srank bits 18:19 = bank group bits 20:22 = bank (reserving space for 32 total banks)
23	RW	FWMS7_EXIT_1: When set, bypass-enabled reads using this mark use exit 1.
24:63	RO	Constant = 0b0000000000000000000000000000000000000000

Register Name	Write ECC Control Register
Mnemonic	MC01.PORT3.ECC64.SCOM.WECR
Address	0000000007010AE8 (SCOM)
Description	Write ECC Control Register

Bits	SCOM	Field Mnemonic: Description
0	RW	MBA_WRD_MODE_CFG_WRD_ECC_CHK_DISABLE: Set to disable 8-byte ECC checking on the WRD data bus.
1	RW	MBA_WRD_MODE_CFG_WRD_ECC_COR_DISABLE: Set to disable 8-byte ECC correction on the WRD data bus.
2	RW	MBA_WRD_MODE_CFG_CRC_MODE_EN: Set to enable CRC generation on write data.
3	RW	MBA_WRD_MODE_CFG_CRC_MODE_X8: Only applies if cfg_crc_mode_en = 1. Set to generate x8 CRC. Clear to generate x4 CRC.
4	RW	MBA_WRD_MODE_RESERVED_4: Reserved.
5	RW	MBA_WRD_MODE_CFG_CAW2_CE_UE_ERR_DETECT_EN: Set to disable the internal error check of the memory ECC generator.
6:56	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	Array Access Control Register
Mnemonic	MC01.PORT3.ECC64.SCOM.AACR
Address	0000000007010AE9 (SCOM)
Description	Array Access Control Register

Bits	SCOM	Field Mnemonic: Description
0	RW	AACR_BUFFER: Buffer select.
1:9	RWX	AACR_ADDRESS: Array doubleword address.
10	RW	AACR_AUTOINC: When set, the AACR address field is incremented after each access to the AAER.
11	RW	AACR_ECCGEN: When set, an 8-byte ECC is generated automatically when writing the AAER (for more information, see 3Array Access ECC Register on page 222) and an 8-byte ECC is checked when reading the array (when reading AADR). When not set, the ECC is not generated or checked.
12:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Register Name	Array Access Data Register
Mnemonic	MC01.PORT3.ECC64.SCOM.AADR
Address	0000000007010AEA (SCOM)
Description	Array Access Data Register

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	AADR_DATA: Array data (0:63).

Register Name	Array Access ECC Register
Mnemonic	MC01.PORT3.ECC64.SCOM.AAER
Address	0000000007010AEB (SCOM)
Description	Array Access ECC Register

Bits	SCOM	Field Mnemonic: Description
0:8	RWX	AAER_TAG_ECC: Array data(64:72). The contents of this register can be in either of two formats: • BUS format: Bit 0 is an I-series tag bit. Bits 1:8 are an 8-byte ECC. • MEM format: Bits 0:7 are memory ECC bits (the “metadata” is in bit 0). Bit 8 is unused (write as 0). Hardware generation of ECC bits for the BUS format is enabled when AACR_eccgen = 1. In this mode, the ECC bits 1:8 should be written as 0.

Register Name	MCBIST Compare Mask Register
Mnemonic	MC01.PORT3.ECC64.SCOM.MCBCM
Address	0000000007010AEC (SCOM)
Description	MCBIST Compare Mask Register. The register clears with an MCBIST global reset.

Bits	SCOM	Field Mnemonic: Description
0:39	RWX	MCBCM_MCBIST_HALF_COMPARE_MASK: Specifies the data bits to ignore for MCBIST comparison. This mask covers either bits 0:39 or 40:79, configurable by mask_coverage_selector dial.
40	RWX	MCBCM_MCBIST_MASK_COVERAGE_SELECTOR: Specifies the bits covered by the compare mask. If '0', the mask covers bits 0:39; otherwise, it covers bits 40:79.
41	RWX	MCBCM_MCBIST_TRAP_NONSTOP: If '1', MCBIST continues to trap new errors even when storage is full, *overwriting* older errors. If '0', MCBIST stops trapping when storage is full.
42	RWX	MCBCM_MCBIST_TRAP_CE_ENABLE: Enables capturing information for CEs.
43	RWX	MCBCM_MCBIST_TRAP_MPE_ENABLE: Enables capturing information for MPEs.
44	RWX	MCBCM_MCBIST_TRAP_UE_ENABLE: Enables capturing information for UEs.

Register Name	Maintenance Buffer MDI/SUE State Register
Mnemonic	MC01.PORT3.ECC64.SCOM.MBMDI
Address	0000000007010AED (SCOM)
Description	Maintenance Buffer MDI/SUE state

Bits	SCOM	Field Mnemonic: Description
0	RWX	MBMDI_MDI_0: MDI state for the first 64 bytes of the maintenance buffer. Maintenance reads set this bit to '1' if either in-memory MDI bit is '1'. Maintenance writes use this bit and the SUE_0 bit to compute the in-memory MDI bits, unless the ECC override is '1' where the undecoded maintenance buffer content is used.
1	RWX	MBMDI_SUE_0: SUE state for the first 64 bytes of the maintenance buffer. Maintenance reads set this bit to '1' if the in-memory MDI bits differ. Maintenance writes use this bit and the MDI_0 bit to compute the in-memory MDI bits, unless the ECC override is '1' where the undecoded maintenance buffer content is used.
2	RWX	MBMDI_MDI_1: MDI state for the second 64 bytes of the maintenance buffer. Maintenance reads set this bit to '1' if either in-memory MDI bit is '1'. Maintenance writes use this bit and the SUE_0 bit to compute the in-memory MDI bits, unless the ECC override is '1' where the undecoded maintenance buffer content is used.

Bits	SCOM	Field Mnemonic: Description
3	RWX	MBMDI_SUE_1: SUE state for the second 64 bytes of the maintenance buffer. Maintenance reads set this bit to '1' if the in-memory MDI bits differ. Maintenance writes use this bit and the MDI_1 bit to compute the in-memory MDI bits, unless the ECC override is '1' where the undecoded maintenance buffer content is used.

Register Name	Write ECC Syndrome Register
Mnemonic	MC01.PORT3.ECC64.SCOM.WESR
Address	0000000007010AEE (SCOM)
Description	The Write ECC Syndrome Register (WESR) contains additional hardware debug information.

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	WESR_SYNDROME: Traps an 8-byte ECC syndrome on the last WRD CAW2 errors.
8:9	ROX	WESR_WHICH_8BECK: Indicates which 8-byte ECC checker's syndrome was trapped. 00 = Doubleword 04 checker 01 = Doubleword 15 checker 10 = Doubleword 26 checker 11 = Doubleword 37 checker For multiple fails, trap priority goes to 00 first, 11 last.
10	ROX	WESR_PAR_ERR_ONLY: Indicates that no 8-byte ECC error was detected, and this CAW2 error was triggered by parity on non-data bits.

Register Name	Error Log Pointer Register
Mnemonic	MC01.PORT3.ECC64.CNTL.ELPR
Address	0000000007010AEF (SCOM)
Description	Provides the readout of the current error-log write pointer and the full/wrap indicator bit. The ELPR is not writable, but is cleared when MCB_CNTLQ[7] = 1 (dial MCB_CNTLQ_MCB_RESET_ERROR_LOGS).

Bits	SCOM	Field Mnemonic: Description
0	ROX	ELPR_LOG_FULL: Log is full. Distinguishes empty from exactly 64 entries.
1	RO	Constant = 0b0
2:7	ROX	ELPR_LOG_POINTER: Log pointer to the next entry to be written.

Register Name	WDF Buffer Miscellaneous Configuration Register
Mnemonic	MC01.PORT3.WDF.WDFCFG
Address	0000000007010AF0 (SCOM)
Description	WDF buffer miscellaneous configuration

Bits	SCOM	Field Mnemonic: Description
0	RW	CFG_WRITE_MODE_ECC_CHK_DIS: Disables 8-byte ECC checking on WDF-buffer read ports.
1	RW	CFG_WRITE_MODE_ECC_COR_DIS: Disables 8-byte ECC correction on WDF-buffer read ports.
2	RW	CFG_WDF_SERIAL_SEQ_MODE: Puts the six PW sequencers into a serial mode of operation; no overlap.
3	RW	RESET_KEEPER: Reset miscellaneous c_err_rpt keepers in the write buffer logic.
4:7	RW	MERGE_CAPACITY_LIMIT: Sets the capacity limit for the merge asynchronous buffer. Valid values are 0 - 8.

Bits	SCOM	Field Mnemonic: Description
8:11	RW	WDFCFG_8_11_SPARE: Spare bits.
12:17	RW	ASYNC_INJ: Asynchronous error inject.
18:31	RW	WDFCFG_18_31_SPARE: Spare bits.
32:35	RW	ECC_WDF_HCA_TIMEBASE_SELECT: HCA time base select.
36:63	RW	ECC_WDF_HCA_TIMEBASE: HCA time base.

Register Name	**Write Buffer WRQ Register**
Mnemonic	MC01.PORT3.WDF.WRT_ECC
Address	0000000007010AF1 (SCOM)
Description	Port ECC error information register

Bits	SCOM	Field Mnemonic: Description
0:2	RWX_WCLRPART	WRT_ECC_DW0_ERR_TYPE: The ECC checker detected the following types of errors in write buffer WRQ read port doubleword 0: bit 0 = CE bit 1 = UE bit 2 = SUE
3:7	RO	Constant = 0b00000
8:15	RWX_WCLRPART	WRT_ECC_DW0_SYNDROME: Write buffer WRQ read port doubleword 0 ECC checker syndrome.
16:18	RWX_WCLRPART	WRT_ECC_DW1_ERR_TYPE: The ECC checker detected the following types of errors in write buffer WRQ read port doubleword 1: bit 0 = CE bit 1 = UE bit 2 = SUE
19:23	RO	Constant = 0b00000
24:31	RWX_WCLRPART	WRT_ECC_DW1_SYNDROME: Write buffer WRQ read port doubleword 1 ECC checker syndrome.
32:34	RWX_WCLRPART	WRT_ECC_DW2_ERR_TYPE: The ECC checker detected the following types of errors in write buffer WRQ read port doubleword 2: bit 0 = CE bit 1 = UE bit 2 = SUE
35:39	RO	Constant = 0b00000
40:47	RWX_WCLRPART	WRT_ECC_DW2_SYNDROME: Write buffer WRQ read port doubleword 2 ECC checker syndrome.
48:50	RWX_WCLRPART	WRT_ECC_DW3_ERR_TYPE: The ECC checker detected the following types of errors in write buffer WRQ read port doubleword 3: bit 0 = CE bit 1 = UE bit 2 = SUE
51:55	RO	Constant = 0b00000
56:63	RWX_WCLRPART	WRT_ECC_DW3_SYNDROME: Write buffer WRQ read port doubleword 3 ECC checker syndrome.

Register Name	WDF HCA Accumulator Register
Mnemonic	MC01.PORT3.WDF.HCA_ACCUM_REG
Address	0000000007010AF2 (SCOM)
Description	WDF HCA accumulator register

Bits	SCOM	Field Mnemonic: Description
0:63	RWX	ACCUM_REG: WDF HCA accumulator data.

Register Name	WDF Tag Overrun Information Register
Mnemonic	MC01.PORT3.WDF.WBMGR_TAG_INFO
Address	0000000007010AF3 (SCOM)
Description	WDF tag overrun information

Bits	SCOM	Field Mnemonic: Description
0	RWX	BUFFER_OVERRUN: WDF buffer overrun indicator.
1	RWX	TAG_OVERRUN: WDF tag overrun indicator.
2	RWX	REL_TAG_ASYNC_PARITY_ERROR: WDF ERL tag parity error indicator.
3	RWX	REL_TAG_ASYNC_SEQUENCE_ERROR: WDF ERL tag sequence error indicator.
4	RWX	REL_MERGE_TAG_ASYNC_PARITY_ERROR: WDF ERL tag parity error indicator.
5	RWX	REL_MERGE_TAG_ASYNC_SEQUENCE_ERROR: WDF ERL tag sequence error indicator.
6:12	RWX	TAG_INFORMATION: WDF tag overrun information.
13:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000

Register Name	WDF Debug Control Register
Mnemonic	MC01.PORT3.WDF.WDFDBG
Address	0000000007010AF4 (SCOM)
Description	WDF debug control

Bits	SCOM	Field Mnemonic: Description
0	RW	DBG_SEL_IN: Indicates that wdf_a_debug_in should be driven to wdf_a_debug_out.
1	RW	DBG_SEL_WDF: Indicates that internal debug data should be driven to wdf_a_debug_out.
2	RW	DBG_SEL_PWSEQ0_DEBUG_0: Indicates that internal debug data pwseq0_debug_0 should be driven to wdf_a_debug_out.
3	RW	DBG_SEL_PWSEQ0_DEBUG_1: Indicates that internal debug data pwseq0_debug_1 should be driven to wdf_a_debug_out.
4	RW	DBG_SEL_PWSEQ1_DEBUG_0: Indicates that internal debug data pwseq1_debug_0 should be driven to wdf_a_debug_out.
5	RW	DBG_SEL_PWSEQ1_DEBUG_1: Indicates that internal debug data pwseq1_debug_1 should be driven to wdf_a_debug_out.
6	RW	DBG_SEL_PWSEQ2_DEBUG_0: Indicates that internal debug data pwseq2_debug_0 should be driven to wdf_a_debug_out.

Bits	SCOM	Field Mnemonic: Description
7	RW	DBG_SEL_PWSEQ2_DEBUG_1: Indicates that internal debug data pwseq2_debug_1 should be driven to wdf_a_debug_out.
8	RW	DBG_SEL_PWSEQ3_DEBUG_0: Indicates that internal debug data pwseq3_debug_0 should be driven to wdf_a_debug_out.
9	RW	DBG_SEL_PWSEQ3_DEBUG_1: Indicates that internal debug data pwseq3_debug_1 should be driven to wdf_a_debug_out.
10	RW	DBG_SEL_PWSEQ4_DEBUG_0: Indicates that internal debug data pwseq4_debug_0 should be driven to wdf_a_debug_out.
11	RW	DBG_SEL_PWSEQ4_DEBUG_1: Indicates that internal debug data pwseq4_debug_1 should be driven to wdf_a_debug_out.
12	RW	DBG_SEL_PWSEQ5_DEBUG_0: Indicates that internal debug data pwseq5_debug_0 should be driven to wdf_a_debug_out.
13	RW	DBG_SEL_PWSEQ5_DEBUG_1: Indicates that internal debug data pwseq5_debug_1 should be driven to wdf_a_debug_out.
14	RW	DBG_SEL_PWCTL_DEBUG: Indicates that internal debug data pwctl_debug should be driven to wdf_a_debug_out
15	RW	DBG_SEL_WDFMGR_DEBUG: Indicates that internal debug data wdfmgr_debug should be driven to wdf_a_debug_out.
16	RW	DBG_SEL_WDFRD_DEBUG_0: Indicates that internal debug data wdfrd_debug_0 should be driven to wdf_a_debug_out.
17	RW	DBG_SEL_WDFRD_DEBUG_1: Indicates that internal debug data wdfrd_debug_1 should be driven to wdf_a_debug_out.
18	RW	DBG_SEL_WDFWR_DEBUG_0: Indicates that internal debug data wdfwr_debug_0 should be driven to wdf_a_debug_out.
19	RW	DBG_SEL_WDFWR_DEBUG_1: Indicates that internal debug data wdfwr_debug_1 should be driven to wdf_a_debug_out.
20	RW	DBG_SEL_SEC_WDFRD_DEBUG_0: Indicates that internal debug data sec_wdfrd_debug_0 should be driven to wdf_a_debug_out.
21	RW	DBG_SEL_SEC_WDFRD_DEBUG_1: Indicates that internal debug data sec_wdfrd_debug_1 should be driven to wdf_a_debug_out.
22:31	RW	DBG_SPARE: Spare bits.
32	RW	WAT_EVENT_ENABLE: Enable latching of wat_event_in.
33:35	RW	WAT_SPARE1: WAT spare.
36:39	RW	WAT0_EVENT_SELECT: Select for wat_action(0).
40:43	RW	WAT1_EVENT_SELECT: Select for wat_action(1).
44:63	RO	Constant = 0b0000000000000000000

Register Name	Write Buffer Miscellaneous Configuration Register
Mnemonic	MC01.PORT3.WRITE.WRTCFG
Address	0000000007010AF8 (SCOM)
Description	Write buffer miscellaneous configuration

Bits	SCOM	Field Mnemonic: Description
0	RW	CFG_WRITE_MODE_ECC_CHK_DIS: Disables 8-byte ECC checking on write-buffer read ports.

Bits	SCOM	Field Mnemonic: Description
1	RW	CFG_WRITE_MODE_ECC_COR_DIS: Disables 8-byte ECC correction on write-buffer read ports.
2	RW	RESET_KEEPER: Reset miscellaneous c_err_rpt keepers in the write buffer logic.
3	RW	MPIPL: mpipl
4:7	RW	ASYNC_INJ: Asynchronous error inject.
8:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	Write Buffer WRQ Register
Mnemonic	MC01.PORT3.WRITE.WRT_ECC
Address	0000000007010AF9 (SCOM)
Description	Port ECC error information register

Bits	SCOM	Field Mnemonic: Description
0:2	RWX_WCLRPART	WRT_ECC_DW0_ERR_TYPE: The ECC checker detected the following types of errors in write buffer WRQ read port doubleword 0: bit 0 = CE bit 1 = UE bit 2 = SUE
3:7	RO	Constant = 0b00000
8:15	RWX_WCLRPART	WRT_ECC_DW0_SYNDROME: Write buffer WRQ read port doubleword 0 ECC checker syndrome.
16:18	RWX_WCLRPART	WRT_ECC_DW1_ERR_TYPE: The ECC checker detected the following types of errors in write buffer WRQ read port doubleword 1: bit 0 = CE bit 1 = UE bit 2 = SUE
19:23	RO	Constant = 0b00000
24:31	RWX_WCLRPART	WRT_ECC_DW1_SYNDROME: Write buffer WRQ read port doubleword 1 ECC checker syndrome.
32:34	RWX_WCLRPART	WRT_ECC_DW2_ERR_TYPE: The ECC checker detected the following types of errors in write buffer WRQ read port doubleword 2: bit 0 = CE bit 1 = UE bit 2 = SUE
35:39	RO	Constant = 0b00000
40:47	RWX_WCLRPART	WRT_ECC_DW2_SYNDROME: Write buffer WRQ read port doubleword 2 ECC checker syndrome.
48:50	RWX_WCLRPART	WRT_ECC_DW3_ERR_TYPE: The ECC checker detected the following types of errors in write buffer WRQ read port doubleword 3: bit 0 = CE bit 1 = UE bit 2 = SUE
51:55	RO	Constant = 0b00000
56:63	RWX_WCLRPART	WRT_ECC_DW3_SYNDROME: Write buffer WRQ read port doubleword 3 ECC checker syndrome.

Register Name	WRT MCA Debug Control Register
Mnemonic	MC01.PORT3.WRITE.WRTDBGMCA
Address	0000000007010AFA (SCOM)
Description	WRT MCA debug control

Bits	SCOM	Field Mnemonic: Description
0	RW	MCA_DBG_SEL_IN: Indicates that write_a_debug_in should be driven to write_a_debug_out.
1	RW	MCA_DBG_SEL_WRT: Indicates that internal debug data should be driven to write_a_debug_out.
2	RW	WBRD_DEBUG_0_SELECT: Indicates that internal debug data wbrd_debug_0 should be driven to write_a_debug_out.
3	RW	WBRD_DEBUG_1_SELECT: Indicates that internal debug data wbrd_debug_1 should be driven to write_a_debug_out.
4	RW	SEC_WBRD_DEBUG_0_SELECT: Indicates that internal debug data sec_wbrd_debug_0 should be driven to write_a_debug_out.
5	RW	SEC_WBRD_DEBUG_1_SELECT: Indicates that internal debug data sec_wbrd_debug_1 should be driven to write_a_debug_out.
6:15	RW	DBG_SPARE_MCA: Spare bits.
16	RW	WAT_EVENT_ENABLE_MCA: Enable latching of wat_event_in.
17:19	RW	WAT_SPARE1_MCA: WAT spare.
20:23	RW	WAT0_EVENT_SELECT_MCA: Select for wat_action(0).
24:27	RW	WAT1_EVENT_SELECT_MCA: Select for wat_action(1).
28:63	RO	Constant = 0b00000000000000000000000000000000000000

Register Name	WRT Nest Debug Control Register
Mnemonic	MC01.PORT3.WRITE.WRTDBGNEST
Address	0000000007010AFB (SCOM)
Description	WRT nest debug control

Bits	SCOM	Field Mnemonic: Description
0	RW	NEST_DBG_SEL_IN: Indicates that write_s_debug_in should be driven to write_s_debug_out.
1	RW	NEST_DBG_SEL_WRT: Indicates that internal debug data should be driven to write_s_debug_out.
2	RW	WBMGR_DBG_0_SELECT: Indicates that internal debug data wbmgr_0_debug should be driven to write_s_debug_out.
3	RW	WBMGR_DBG_1_SELECT: Indicates that internal debug data wbmgr_1_debug should be driven to write_s_debug_out.
4	RW	WRCNTL_DBG_SELECT: Indicates that internal debug data wrcntl_debug should be driven to write_s_debug_out.
5:15	RW	DBG_SPARE_NEST: Spare bits.
16	RW	WAT_EVENT_ENABLE_NEST: Enable latching of wat_event_in.
17:19	RW	WAT_SPARE1_NEST: WAT spare.
20:23	RW	WAT0_EVENT_SELECT_NEST: Select for wat_action(0).
24:27	RW	WAT1_EVENT_SELECT_NEST: Select for wat_action(1).

Bits	SCOM	Field Mnemonic: Description
28:63	RO	Constant = 0b00000000000000000000000000000000000000

Register Name	Trace Array High Data Register
Mnemonic	TP.TCMC01.MCFAST.TRA0.TR0.TRACE_HI_DATA_REG
Address	0000000007010C00 (SCOM)
Description	This register provides the high trace-array data.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: This field contains trace array data 0:63.

Register Name	Trace Array Low Data Register
Mnemonic	TP.TCMC01.MCFAST.TRA0.TR0.TRACE_LO_DATA_REG
Address	0000000007010C01 (SCOM)
Description	This register provides the low trace array data.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace array data 64:95.
32:41	ROX	TRACE_ADDRESS: Trace address.
42:50	ROX	TRACE_LAST_BANK: Trace last bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace last bank valid.
52	ROX	TRACE_WRITE_ON_RUN: Trace write-on-run indicator.
53	ROX	TRACE_RUNNING: Trace run indicator.
54:63	ROX	TRACE_HOLD_ADDRESS: Trace hold address (pointing to last entry).

Register Name	Trace Control Configuration Register
Mnemonic	TP.TCMC01.MCFAST.TRA0.TR0.TRACE_TRCTRL_CONFIG
Address	0000000007010C02 (SCOM)
Description	This register contains trace control configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	STORE_ON_TRIG_MODE: This bit enables store on trigger mode.
1	RW	WRITE_ON_RUN_MODE: This bit enables an unconditional forced write when a trace runs.
2:9	RW	EXTEND_TRIG_MODE: This field contains the counter value for extended trigger mode.
10	RW	BANK_MODE: This bit enables bank mode.
11	RW	ENH_TRACE_MODE: This bit enables enhanced trace mode.
12	RW	LOCAL_CLOCK_GATE_CONTROL: When this bit is set, internal clock gating is disabled. The trace control logic and the trace data pipeline are always clocked.
13	RW	UNUSED_13B. Unused.

Bits	SCOM	Field Mnemonic: Description
14:17	RW	TRACE_SELCT_CONTROL: This field is a selector for two sets of external trace bus multiplexers: tra_mux0_sel(0:1) and tra_mux1_sel(0:1).
18:21	RW	SPARE_CONTROL: This field contains spare control bits.

Register Name	Trace Data Configuration Register 0
Mnemonic	TP.TCMC01.MCFAST.TRA0.TR0.TRACE_TRDATA_CONFIG_0
Address	0000000007010C03 (SCOM)
Description	This register contains a trace data compare mask for bits 0 - 63.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: This field contains a trace data compare mask for bits 0 - 63.

Register Name	Trace Data Configuration Register 1
Mnemonic	TP.TCMC01.MCFAST.TRA0.TR0.TRACE_TRDATA_CONFIG_1
Address	0000000007010C04 (SCOM)
Description	This register contains a trace data compare mask for bits 64 - 87.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: This field contains a trace data compare mask for bits 64 - 87.

Register Name	Trace Data Configuration Register 2
Mnemonic	TP.TCMC01.MCFAST.TRA0.TR0.TRACE_TRDATA_CONFIG_2
Address	0000000007010C05 (SCOM)
Description	This register contains patterns A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: Pattern match pattern A 0 - 23. Pattern A is used to perform a data compare on the trace data. When the data compare matches, a trigger is generated that can be used for a "store on trigger" function or as a trace trigger to the debug macro.
24:47	RW	PATTERNB: Pattern match pattern B 0 - 23. Pattern B is used to perform a data compare on the trace data. When the data compare matches, a trigger is generated that can be used for a "store on trigger" function or as a trace trigger to the debug macro.

Register Name	Trace Data Configuration Register 3
Mnemonic	TP.TCMC01.MCFAST.TRA0.TR0.TRACE_TRDATA_CONFIG_3
Address	0000000007010C06 (SCOM)
Description	This register contains patterns C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNC: Pattern match pattern C 0 - 23. Pattern C is used to perform a data compare on the trace data. When the data compare matches, a trigger is generated that can be used for a "store on trigger" function or as a trace trigger to the debug macro.
24:47	RW	PATTERND: Pattern match pattern D 0 - 23. Pattern D is used to perform a data compare on the trace data. When the data compare matches, a trigger is generated that can be used for a "store on trigger" function or as a trace trigger to the debug macro.

Register Name	Trace Data Configuration Register 4
Mnemonic	TP.TCMC01.MCFAST.TRA0.TR0.TRACE_TRDATA_CONFIG_4
Address	0000000007010C07 (SCOM)
Description	This register contains masks A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: Mask A. When set to '1', masks off bits from Pattern A. This field is used to mask off individual bits of Pattern A so that they are "don't care" for the data compare match function.
24:47	RW	MASKB: Mask B. When set to '1', masks off bits from Pattern B. This field is used to mask off individual bits of Pattern B so that they are "don't care" for the data compare match function.

Register Name	Trace Data Configuration Register 5
Mnemonic	TP.TCMC01.MCFAST.TRA0.TR0.TRACE_TRDATA_CONFIG_5
Address	0000000007010C08 (SCOM)
Description	This register contains masks C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: Mask C. When set to '1', masks off bits from Pattern C. This field is used to mask off individual bits of Pattern C so that they are "don't care" for the data compare match function.
24:47	RW	MASKD: Mask D. When set to '1', masks off bits from Pattern D. This field is used to mask off individual bits of Pattern D so that they are "don't care" for the data compare match function.

Register Name	Trace Data Configuration Register 9
Mnemonic	TP.TCMC01.MCFAST.TRA0.TR0.TRACE_TRDATA_CONFIG_9
Address	0000000007010C09 (SCOM)
Description	This register contains trace data configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disable trace data compression (store data every cycle).
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Take into account (care about) changes in the error bit for trace data compression (default = 0)
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 00 = Debug bus bits(00:23) 01 = Debug bus bits(24:47) 10 = Debug bus bits(48:71) 11 = Debug bus bits(72:87) | 8 zeros

Bits	SCOM	Field Mnemonic: Description
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 00 = Debug bus bits(00:23) 01 = Debug bus bits(24:47) 10 = Debug bus bits(48:71) 11 = Debug bus bits(72:87) | 8 zeros
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 00 = Debug bus bits(00:23) 01 = Debug bus bits(24:47) 10 = Debug bus bits(48:71) 11 = Debug bus bits(72:87) | 8 zeros
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 00 = Debug bus bits(00:23) 01 = Debug bus bits(24:47) 10 = Debug bus bits(48:71) 11 = Debug bus bits(72:87) | 8 zeros
10:13	RW	TRIG0_OR_MASK: **Note**: The OR of all selected MATCHes is ORed with the result of TRIG0_AND. 1XXX selects MATCHA OR X1XX selects MATCHB OR XX1X selects MATCHC OR XXX1 selects MATCHD OR 0000 selects to not OR any MATCHes
14:17	RW	TRIG0_AND_MASK: **Note**: The AND of the following selected MATCHes is ORed with the result of TRIG0_OR. 1XXX selects MATCHA AND X1XX selects MATCHB AND XX1X selects MATCHC AND XXX1 selects MATCHD AND 0000 selects to not AND any MATCHes together to form TRIG0
18:21	RW	TRIG1_OR_MASK: **Note**: The OR of all selected MATCHes is ORed with the result of TRIG1_AND. 1XXX selects MATCHA OR X1XX selects MATCHB OR XX1X selects MATCHC OR XXX1 selects MATCHD OR 0000 selects to not OR any MATCHes to form TRIG1
22:25	RW	TRIG1_AND_MASK: **Note**: The AND of the following selected MATCHes is ORed with the result of TRIG1_OR. 1XXX selects MATCHA AND X1XX selects MATCHB AND XX1X selects MATCHC AND XXX1 selects MATCHD AND 0000 selects to not AND any MATCHes together to form TRIG1
26	RW	TRIG0_NOT_MODE: Invert TRIG0 before using it.
27	RW	TRIG1_NOT_MODE: Invert TRIG1 before using it.
28:31	RW	MATCH_NOT_MODE: Invert the match polarity before using it to form a TRIGger. 1000 inverts MATCHA 0100 inverts MATCHB 0010 inverts MATCHC 0001 inverts MATCHD
32:35	RW	Reserved.
36	RW	DD1_STRETCH_TRIGGER_PULSES: (DD1 workaround) Stretch trigger output pulses to two clocks. This bit must be enabled for MCFAST and L2FAST traces.

Bits	SCOM	Field Mnemonic: Description
37	RW	Reserved.

Register Name	Trace Array High Data Register
Mnemonic	TP.TCMC01.MCFAST.TRA1.TR0.TRACE_HI_DATA_REG
Address	0000000007010C40 (SCOM)
Description	This register provides the high trace array data.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: This field contains trace array data 0:63.

Register Name	Trace Array Low Data Register
Mnemonic	TP.TCMC01.MCFAST.TRA1.TR0.TRACE_LO_DATA_REG
Address	0000000007010C41 (SCOM)
Description	This register provides the low trace array data.

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace array data 64:95.
32:41	ROX	TRACE_ADDRESS: Trace address.
42:50	ROX	TRACE_LAST_BANK: Trace last bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace last bank valid.
52	ROX	TRACE_WRITE_ON_RUN: Trace write-on-run indicator.
53	ROX	TRACE_RUNNING: Trace run indicator.
54:63	ROX	TRACE_HOLD_ADDRESS: Trace hold address (pointing to last entry).

Register Name	Trace Control Configuration Register
Mnemonic	TP.TCMC01.MCFAST.TRA1.TR0.TRACE_TRCTRL_CONFIG
Address	0000000007010C42 (SCOM)
Description	This register contains trace control configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	STORE_ON_TRIG_MODE: This bit enables store on trigger mode.
1	RW	WRITE_ON_RUN_MODE: This bit enables an unconditional forced write when a trace runs.
2:9	RW	EXTEND_TRIG_MODE: This field contains the counter value for extended trigger mode.
10	RW	BANK_MODE: This bit enables bank mode.
11	RW	ENH_TRACE_MODE: This bit enables enhanced trace mode.
12	RW	LOCAL_CLOCK_GATE_CONTROL: When this bit is set, internal clock gating is disabled. The trace control logic and the trace data pipeline are always clocked.
13	RW	UNUSED_13B. Unused.

Bits	SCOM	Field Mnemonic: Description
14:17	RW	TRACE_SELCT_CONTROL: This field is a selector for two sets of external trace bus multiplexers: tra_mux0_sel(0:1) and tra_mux1_sel(0:1).
18:21	RW	SPARE_CONTROL: This field contains spare control bits.

Register Name	Trace Data Configuration Register 0
Mnemonic	TP.TCMC01.MCFAST.TRA1.TR0.TRACE_TRDATA_CONFIG_0
Address	0000000007010C43 (SCOM)
Description	This register contains a trace data compare mask for bits 0 - 63.

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CMP_MSK_LT_B_0_TO_63: This field contains a trace data compare mask for bits 0 - 63.

Register Name	Trace Data Configuration Register 1
Mnemonic	TP.TCMC01.MCFAST.TRA1.TR0.TRACE_TRDATA_CONFIG_1
Address	0000000007010C44 (SCOM)
Description	This register contains a trace data compare mask for bits 64 - 87.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	CMP_MSK_LT_B_64_TO_87: This field contains a trace data compare mask for bits 64 - 87.

Register Name	Trace Data Configuration Register 2
Mnemonic	TP.TCMC01.MCFAST.TRA1.TR0.TRACE_TRDATA_CONFIG_2
Address	0000000007010C45 (SCOM)
Description	This register contains patterns A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNA: Pattern match pattern A 0 - 23. Pattern A is used to perform a data compare on the trace data. When the data compare matches, a trigger is generated that can be used for a "store on trigger" function or as a trace trigger to the debug macro.
24:47	RW	PATTERNB: Pattern match pattern B 0 - 23. Pattern B is used to perform a data compare on the trace data. When the data compare matches, a trigger is generated that can be used for a "store on trigger" function or as a trace trigger to the debug macro.

Register Name	Trace Data Configuration Register 3
Mnemonic	TP.TCMC01.MCFAST.TRA1.TR0.TRACE_TRDATA_CONFIG_3
Address	0000000007010C46 (SCOM)
Description	This register contains patterns C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	PATTERNC: Pattern match pattern C 0 - 23. Pattern C is used to perform a data compare on the trace data. When the data compare matches, a trigger is generated that can be used for a "store on trigger" function or as a trace trigger to the debug macro.
24:47	RW	PATTERND: Pattern match pattern D 0 - 23. Pattern D is used to perform a data compare on the trace data. When the data compare matches, a trigger is generated that can be used for a "store on trigger" function or as a trace trigger to the debug macro.

Register Name	Trace Data Configuration Register 4
Mnemonic	TP.TCMC01.MCFAST.TRA1.TR0.TRACE_TRDATA_CONFIG_4
Address	0000000007010C47 (SCOM)
Description	This register contains masks A and B.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKA: Mask A. When set to '1', masks off bits from Pattern A. This field is used to mask off individual bits of Pattern A so that they are "don't care" for the data compare match function.
24:47	RW	MASKB: Mask B. When set to '1', masks off bits from Pattern B. This field is used to mask off individual bits of Pattern B so that they are "don't care" for the data compare match function.

Register Name	Trace Data Configuration Register 5
Mnemonic	TP.TCMC01.MCFAST.TRA1.TR0.TRACE_TRDATA_CONFIG_5
Address	0000000007010C48 (SCOM)
Description	This register contains masks C and D.

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MASKC: Mask C. When set to '1', masks off bits from Pattern C. This field is used to mask off individual bits of Pattern C so that they are "don't care" for the data compare match function.
24:47	RW	MASKD: Mask D. When set to '1', masks off bits from Pattern D. This field is used to mask off individual bits of Pattern D so that they are "don't care" for the data compare match function.

Register Name	Trace Data Configuration Register 9
Mnemonic	TP.TCMC01.MCFAST.TRA1.TR0.TRACE_TRDATA_CONFIG_9
Address	0000000007010C49 (SCOM)
Description	This register contains trace data configuration fields.

Bits	SCOM	Field Mnemonic: Description
0	RW	DISABLE_COMPRESSION: Disable trace data compression (store data every cycle).
1	RW	ERROR_BIT_COMPRESSION_CARE_MASK: Take into account (care about) changes in the error bit for trace data compression (default = 0).
2:3	RW	MATCHA_MUXSEL: Match PATTERNA against: 00 = Debug bus bits(00:23) 01 = Debug bus bits(24:47) 10 = Debug bus bits(48:71) 11 = Debug bus bits(72:87) | 8 zeros

Bits	SCOM	Field Mnemonic: Description
4:5	RW	MATCHB_MUXSEL: Match PATTERNB against: 00 = Debug bus bits(00:23) 01 = Debug bus bits(24:47) 10 = Debug bus bits(48:71) 11 = Debug bus bits(72:87) | 8 zeros
6:7	RW	MATCHC_MUXSEL: Match PATTERNC against: 00 = Debug bus bits(00:23) 01 = Debug bus bits(24:47) 10 = Debug bus bits(48:71) 11 = Debug bus bits(72:87) | 8 zeros
8:9	RW	MATCHD_MUXSEL: Match PATTERND against: 00 = Debug bus bits(00:23) 01 = Debug bus bits(24:47) 10 = Debug bus bits(48:71) 11 = Debug bus bits(72:87) | 8 zeros
10:13	RW	TRIG0_OR_MASK: **Note**: The OR of all selected MATCHes is ORed with the result of TRIG0_AND. 1XXX selects MATCHA OR X1XX selects MATCHB OR XX1X selects MATCHC OR XXX1 selects MATCHD OR 0000 selects to not OR any MATCHes
14:17	RW	TRIG0_AND_MASK: **Note**: The AND of the following selected MATCHes is ORed with the result of TRIG0_OR. 1XXX selects MATCHA AND X1XX selects MATCHB AND XX1X selects MATCHC AND XXX1 selects MATCHD AND 0000 selects to not AND any MATCHes together to form TRIG0
18:21	RW	TRIG1_OR_MASK: **Note**: The OR of all selected MATCHes is ORed with the result of TRIG1_AND. 1XXX selects MATCHA OR X1XX selects MATCHB OR XX1X selects MATCHC OR XXX1 selects MATCHD OR 0000 selects to not OR any MATCHes to form TRIG1
22:25	RW	TRIG1_AND_MASK: **Note**: The AND of the following selected MATCHes is ORed with the result of TRIG1_OR. 1XXX selects MATCHA AND X1XX selects MATCHB AND XX1X selects MATCHC AND XXX1 selects MATCHD AND 0000 selects to not AND any MATCHes together to form TRIG1
26	RW	TRIG0_NOT_MODE: Invert TRIG0 before using it.
27	RW	TRIG1_NOT_MODE: Invert TRIG1 before using it.
28:31	RW	MATCH_NOT_MODE: Invert the match polarity before using it to form a TRIGger. 1000 inverts MATCHA 0100 inverts MATCHB 0010 inverts MATCHC 0001 inverts MATCHD
32:35	RW	Reserved.
36	RW	DD1_STRETCH_TRIGGER_PULSES: (DD1 workaround) Stretch trigger output pulses to two clocks. This bit must be enabled for MCFAST and L2FAST traces.

Bits	SCOM	Field Mnemonic: Description
37	RW	Reserved.

Register Name	IOM_PHY0 Pervasive FIR Register
Mnemonic	IOM0.IOM_PHY0_DDRPHY_FIR_REG
Address	0000000007011000 (SCOM) 0000000007011001 (SCOM1) 0000000007011002 (SCOM2)
Description	Local FIR register for the chip pervasive logic

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:53	RO	RO	RO	Constant = 0b00000000000000000000000000000000000000000000000000000
54	RWX	WOX_AND	WOX_OR	IOM_PHY0_DDRPHY_FIR_REG_DDR_FIR_ERROR_0: PHYTOP non-recoverable state machine errors.
55	RWX	WOX_AND	WOX_OR	IOM_PHY0_DDRPHY_FIR_REG_DDR_FIR_ERROR_1: PHYTOP and ADR parity errors affect the entire bus.
56	RWX	WOX_AND	WOX_OR	IOM_PHY0_DDRPHY_FIR_REG_DDR_FIR_ERROR_2: DP8/DP16 parity errors affecting initial calibration, initial calibration errors, and DLL errors during initial calibration.
57	RWX	WOX_AND	WOX_OR	IOM_PHY0_DDRPHY_FIR_REG_DDR_FIR_ERROR_3: PHYTOP and DP8/DP16 possibly recoverable state machine errors.
58	RWX	WOX_AND	WOX_OR	IOM_PHY0_DDRPHY_FIR_REG_DDR_FIR_ERROR_4: DP8/DP16 parity errors affecting up to 16 bits. DLL errors during traffic are included.
59	RWX	WOX_AND	WOX_OR	IOM_PHY0_DDRPHY_FIR_REG_DDR_FIR_ERROR_5: DP8/DP16 parity errors affecting up to 8 bits.
60	RWX	WOX_AND	WOX_OR	IOM_PHY0_DDRPHY_FIR_REG_DDR_FIR_ERROR_6: DP8/DP16 parity errors affecting up to 4 bits.
61	RWX	WOX_AND	WOX_OR	IOM_PHY0_DDRPHY_FIR_REG_DDR_FIR_ERROR_7: DP8/DP16 parity errors affecting up to 1 bit.
62:63	RO	RO	RO	Constant = 0b00

Register Name	IOM_PHY0 Pervasive FIR Mask Register
Mnemonic	IOM0.IOM_PHY0_DDRPHY_FIR_MASK_REG
Address	0000000007011003 (SCOM) 0000000007011004 (SCOM1) 0000000007011005 (SCOM2)
Description	This register contains the FIR mask bits for all errors detected in the DDRPHY.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:53	RO	RO	RO	Constant = 0b00000000000000000000000000000000000000000000000000000
54	RW	WO_AND	WO_OR	IOM_PHY0_DDRPHY_FIR_MASK_REG_DDR_FIR_ERROR_0_MASK: Mask PHYTOP non-recoverable state machine errors.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
55	RW	WO_AND	WO_OR	IOM_PHY0_DDRPHY_FIR_MASK_REG_DDR_FIR_ERROR_1_MASK: Mask PHYTOP (both non-recoverable and recoverable) and ADR parity errors (affect entire bus).
56	RW	WO_AND	WO_OR	IOM_PHY0_DDRPHY_FIR_MASK_REG_DDR_FIR_ERROR_2_MASK: Mask DP8/DP16 parity errors affecting initcal, initcal errors, DLL errors during initcal.
57	RW	WO_AND	WO_OR	IOM_PHY0_DDRPHY_FIR_MASK_REG_DDR_FIR_ERROR_3_MASK: Mask PHYTOP and DP8/DP16 possibly recoverable state machine errors.
58	RW	WO_AND	WO_OR	IOM_PHY0_DDRPHY_FIR_MASK_REG_DDR_FIR_ERROR_4_MASK: Mask DP8/DP16 parity errors affecting up to 16 bits, DLL errors during traffic included.
59	RW	WO_AND	WO_OR	IOM_PHY0_DDRPHY_FIR_MASK_REG_DDR_FIR_ERROR_5_MASK: Mask DP8/DP16 parity errors affecting up to 8 bit.
60	RW	WO_AND	WO_OR	IOM_PHY0_DDRPHY_FIR_MASK_REG_DDR_FIR_ERROR_6_MASK: Mask DP8/DP16 parity errors affecting up to 4 bit.
61	RW	WO_AND	WO_OR	IOM_PHY0_DDRPHY_FIR_MASK_REG_DDR_FIR_ERROR_7_MASK: Mask DP8/DP16 parity errors affecting up to 1 bit.
62:63	RO	RO	RO	Constant = 0b00

Register Name	**IOM_PHY0 Pervasive FIR Action 0 Register**
Mnemonic	IOM0.IOM_PHY0_DDRPHY_FIR_ACTION0_REG
Address	0000000007011006 (SCOM)
Description	This register contains the sction select for the FIR bits. FIR action register decodes. (Action0,Action1,Mask) = Action Select (0,0,0) = Checkstop (0,1,0) = Recoverable (1,0,0) = Unused/recov_int (1,1,0) = Local core checkstop/freeze (X,X,1) = Masked

Bits	SCOM	Field Mnemonic: Description
0:53	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000
54:61	RW	IOM_PHY0_DDRPHY_FIR_ACTION0_REG_DDR_FIR_ACTION0: See the corresponding FIR bit decodes in the register description.
62:63	RO	Constant = 0b00

Register Name	IOM_PHY0 Pervasive FIR Action 1 Register
Mnemonic	IOM0.IOM_PHY0_DDRPHY_FIR_ACTION1_REG
Address	0000000007011007 (SCOM)
Description	This register contains the second action select. FIR action register decodes. (Action0,Action1,Mask) = Action Select (0,0,0) = Checkstop (0,1,0) = Recoverable (1,0,0) = Unused/recov_int (1,1,0) = Local core checkstop/freeze (X,X,1) = Masked

Bits	SCOM	Field Mnemonic: Description
0:53	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
54:61	RW	IOM_PHY0_DDRPHY_FIR_ACTION1_REG_DDR_FIR_ACTION1: See the corresponding FIR bit decodes in the register description.
62:63	RO	Constant = 0b00

Register Name	IOM_PHY0 Pervasive FIR WOF Register
Mnemonic	IOM0.IOM_PHY0_DDRPHY_FIR_WOF_REG
Address	0000000007011008 (SCOM)
Description	The Who Is on First Register indicates which error occurred first.

Bits	SCOM	Field Mnemonic: Description
0:53	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
54:61	RWX_WCLRREG	IOM_PHY0_DDRPHY_FIR_WOF_REG_DDR_FIR_WOF: The WOF Register locks on the first error.
62:63	RO	Constant = 0b00

Register Name	IOM_PHY1 Pervasive FIR Register
Mnemonic	IOM0.IOM_PHY1_DDRPHY_FIR_REG
Address	0000000007011400 (SCOM) 0000000007011401 (SCOM1) 0000000007011402 (SCOM2)
Description	Local FIR register for the chip pervasive logic

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:53	RO	RO	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
54	RWX	WOX_AND	WOX_OR	IOM_PHY1_DDRPHY_FIR_REG_DDR_FIR_ERROR_0: PHYTOP Non-recoverable state machine errors.
55	RWX	WOX_AND	WOX_OR	IOM_PHY1_DDRPHY_FIR_REG_DDR_FIR_ERROR_1: PHYTOP and ADR parity errors affect the entire bus.
56	RWX	WOX_AND	WOX_OR	IOM_PHY1_DDRPHY_FIR_REG_DDR_FIR_ERROR_2: DP8/DP16 parity errors affecting initial calibration, initial calibration errors, and DLL errors during initial calibration.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
57	RWX	WOX_AND	WOX_OR	IOM_PHY1_DDRPHY_FIR_REG_DDR_FIR_ERROR_3: PHYTOP and DP8/DP16 possibly recoverable state machine errors.
58	RWX	WOX_AND	WOX_OR	IOM_PHY1_DDRPHY_FIR_REG_DDR_FIR_ERROR_4: DP8/DP16 parity errors affecting up to 16 bits. DLL errors during traffic are included.
59	RWX	WOX_AND	WOX_OR	IOM_PHY1_DDRPHY_FIR_REG_DDR_FIR_ERROR_5: DP8/DP16 parity errors affecting up to 8 bits.
60	RWX	WOX_AND	WOX_OR	IOM_PHY1_DDRPHY_FIR_REG_DDR_FIR_ERROR_6: DP8/DP16 parity errors affecting up to 4 bits.
61	RWX	WOX_AND	WOX_OR	IOM_PHY1_DDRPHY_FIR_REG_DDR_FIR_ERROR_7: DP8/DP16 parity errors affecting up to 1 bit.
62:63	RO	RO	RO	Constant = 0b00

Register Name	**IOM_PHY1 Pervasive FIR Mask Register**
Mnemonic	IOM0.IOM_PHY1_DDRPHY_FIR_MASK_REG
Address	0000000007011403 (SCOM) 0000000007011404 (SCOM1) 0000000007011405 (SCOM2)
Description	This register contains the FIR mask bits for all the errors detected in the DDRPHY.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:53	RO	RO	RO	Constant = 0b00000000000000000000000000000000000000000000000000000
54	RW	WO_AND	WO_OR	IOM_PHY1_DDRPHY_FIR_MASK_REG_DDR_FIR_ERROR_0_MASK: Mask PHYTOP non-recoverable state machine errors.
55	RW	WO_AND	WO_OR	IOM_PHY1_DDRPHY_FIR_MASK_REG_DDR_FIR_ERROR_1_MASK: Mask PHYTOP (both non-recoverable and recoverable) and ADR parity errors (affect entire bus).
56	RW	WO_AND	WO_OR	IOM_PHY1_DDRPHY_FIR_MASK_REG_DDR_FIR_ERROR_2_MASK: Mask DP8/DP16 parity errors affecting initcal, initcal errors,DLL errors during initcal.
57	RW	WO_AND	WO_OR	IOM_PHY1_DDRPHY_FIR_MASK_REG_DDR_FIR_ERROR_3_MASK: Mask PHYTOP and DP8/DP16 possibly recoverable state machine errors.
58	RW	WO_AND	WO_OR	IOM_PHY1_DDRPHY_FIR_MASK_REG_DDR_FIR_ERROR_4_MASK: Mask DP8/DP16 parity errors affecting up to 16 bits, DLL errors during traffic included.
59	RW	WO_AND	WO_OR	IOM_PHY1_DDRPHY_FIR_MASK_REG_DDR_FIR_ERROR_5_MASK: Mask DP8/DP16 parity errors affecting up to 8 bit.
60	RW	WO_AND	WO_OR	IOM_PHY1_DDRPHY_FIR_MASK_REG_DDR_FIR_ERROR_6_MASK: Mask DP8/DP16 parity errors affecting up to 4 bit.
61	RW	WO_AND	WO_OR	IOM_PHY1_DDRPHY_FIR_MASK_REG_DDR_FIR_ERROR_7_MASK: Mask DP8/DP16 parity errors affecting up to 1 bit.
62:63	RO	RO	RO	Constant = 0b00

Register Name	IOM_PHY1 Pervasive FIR Action 0 Register
Mnemonic	IOM0.IOM_PHY1_DDRPHY_FIR_ACTION0_REG
Address	0000000007011406 (SCOM)
Description	FIR Action Register Decodes. (Action0, Action1, Mask) (0,0,0) = Checkstop (0,1,0) = Recoverable (1,0,0) = Unused/recov_int (1,1,0) = Local core checkstop/freeze (X,X,1) = Masked

Bits	SCOM	Field Mnemonic: Description
0:53	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000
54:61	RW	IOM_PHY1_DDRPHY_FIR_ACTION0_REG_DDR_FIR_ACTION0: See the corresponding FIR bit decodes in the register description.
62:63	RO	Constant = 0b00

Register Name	IOM_PHY1 Pervasive FIR Action 1 Register
Mnemonic	IOM0.IOM_PHY1_DDRPHY_FIR_ACTION1_REG
Address	0000000007011407 (SCOM)
Description	FIR Action Register Decodes (Action0, Action1, Mask) (0,0,0) = Checkstop (0,1,0) = Recoverable (1,0,0) = Unused/recov_int (1,1,0) = Local core checkstop/freeze (X,X,1) = Masked

Bits	SCOM	Field Mnemonic: Description
0:53	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000
54:61	RW	IOM_PHY1_DDRPHY_FIR_ACTION1_REG_DDR_FIR_ACTION1: See the corresponding FIR bit decodes in the register description.
62:63	RO	Constant = 0b00

Register Name	IOM_PHY1 Pervasive FIR WOF Register
Mnemonic	IOM0.IOM_PHY1_DDRPHY_FIR_WOF_REG
Address	0000000007011408 (SCOM)
Description	The Who Is on First Register indicates which error occurred first.

Bits	SCOM	Field Mnemonic: Description
0:53	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000
54:61	RWX_WCLRREG	IOM_PHY1_DDRPHY_FIR_WOF_REG_DDR_FIR_WOF: The WOF Register locks on the first error.
62:63	RO	Constant = 0b00

Register Name	**IOM_PHY2 Pervasive FIR Register**
Mnemonic	IOM0.IOM_PHY2_DDRPHY_FIR_REG
Address	0000000007011800 (SCOM) 0000000007011801 (SCOM1) 0000000007011802 (SCOM2)
Description	Local FIR register for the chip pervasive logic

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:53	RO	RO	RO	Constant = 0b00000000000000000000000000000000000000000000000000000
54	RWX	WOX_AND	WOX_OR	IOM_PHY2_DDRPHY_FIR_REG_DDR_FIR_ERROR_0: PHYTOP Non-recoverable state machine errors.
55	RWX	WOX_AND	WOX_OR	IOM_PHY2_DDRPHY_FIR_REG_DDR_FIR_ERROR_1: PHYTOP and ADR parity errors affect the entire bus.
56	RWX	WOX_AND	WOX_OR	IOM_PHY2_DDRPHY_FIR_REG_DDR_FIR_ERROR_2: DP8/DP16 parity errors affecting initial calibration, initial calibration errors, and DLL errors during initial calibration.
57	RWX	WOX_AND	WOX_OR	IOM_PHY2_DDRPHY_FIR_REG_DDR_FIR_ERROR_3: PHYTOP and DP8/DP16 possibly recoverable state machine errors.
58	RWX	WOX_AND	WOX_OR	IOM_PHY2_DDRPHY_FIR_REG_DDR_FIR_ERROR_4: DP8/DP16 Parity errors affecting up to 16 bits. DLL errors during traffic are included.
59	RWX	WOX_AND	WOX_OR	IOM_PHY2_DDRPHY_FIR_REG_DDR_FIR_ERROR_5: DP8/DP16 parity errors affecting up to 8 bits.
60	RWX	WOX_AND	WOX_OR	IOM_PHY2_DDRPHY_FIR_REG_DDR_FIR_ERROR_6: DP8/DP16 parity errors affecting up to 4 bits.
61	RWX	WOX_AND	WOX_OR	IOM_PHY2_DDRPHY_FIR_REG_DDR_FIR_ERROR_7: DP8/DP16 parity errors affecting up to 1 bit.
62:63	RO	RO	RO	Constant = 0b00

Register Name	**IOM_PHY2 Pervasive FIR Mask Register**
Mnemonic	IOM0.IOM_PHY2_DDRPHY_FIR_MASK_REG
Address	0000000007011803 (SCOM) 0000000007011804 (SCOM1) 0000000007011805 (SCOM2)
Description	This register contains the FIR mask bits for all the errors detected in the DDRPHY.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:53	RO	RO	RO	Constant = 0b00000000000000000000000000000000000000000000000000000
54	RW	WO_AND	WO_OR	IOM_PHY2_DDRPHY_FIR_MASK_REG_DDR_FIR_ERROR_0_MASK: Mask PHYTOP non-recoverable state machine errors.
55	RW	WO_AND	WO_OR	IOM_PHY2_DDRPHY_FIR_MASK_REG_DDR_FIR_ERROR_1_MASK: Mask PHYTOP (both non-recoverable and recoverable) and ADR parity errors (affect entire bus).
56	RW	WO_AND	WO_OR	IOM_PHY2_DDRPHY_FIR_MASK_REG_DDR_FIR_ERROR_2_MASK: Mask DP8/DP16 parity errors affecting initcal, initcal errors, DLL errors during initcal.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
57	RW	WO_AND	WO_OR	IOM_PHY2_DDRPHY_FIR_MASK_REG_DDR_FIR_ERROR_3_MASK: Mask PHYTOP and DP8/DP16 possibly recoverable state machine errors.
58	RW	WO_AND	WO_OR	IOM_PHY3_DDRPHY_FIR_MASK_REG_DDR_FIR_ERROR_4_MASK: Mask DP8/DP16 parity errors affecting up to 16 bits, DLL errors during traffic included.
59	RW	WO_AND	WO_OR	IOM_PHY2_DDRPHY_FIR_MASK_REG_DDR_FIR_ERROR_5_MASK: Mask DP8/DP16 parity errors affecting up to 8 bit.
60	RW	WO_AND	WO_OR	IOM_PHY2_DDRPHY_FIR_MASK_REG_DDR_FIR_ERROR_6_MASK: Mask DP8/DP16 parity errors affecting up to 4 bit.
61	RW	WO_AND	WO_OR	IOM_PHY2_DDRPHY_FIR_MASK_REG_DDR_FIR_ERROR_7_MASK: Mask DP8/DP16 parity errors affecting up to 1 bit.
62:63	RO	RO	RO	Constant = 0b00

Register Name	**IOM_PHY2 Pervasive FIR Action 0 Register**
Mnemonic	IOM0.IOM_PHY2_DDRPHY_FIR_ACTION0_REG
Address	0000000007011806 (SCOM)
Description	FIR Action Register Decodes. (Action0, Action1, Mask) (0,0,0) = Checkstop (0,1,0) = Recoverable (1,0,0) = Unused/recov_int (1,1,0) = Local core checkstop/freeze (X,X,1) = Masked

Bits	SCOM	Field Mnemonic: Description
0:53	RO	Constant = 0b00000000000000000000000000000000000000000000000000000
54:61	RW	IOM_PHY2_DDRPHY_FIR_ACTION0_REG_DDR_FIR_ACTION0: See the corresponding FIR bit decodes in the register description.
62:63	RO	Constant = 0b00

Register Name	**IOM_PHY2 Pervasive FIR Action 1 Register**
Mnemonic	IOM0.IOM_PHY2_DDRPHY_FIR_ACTION1_REG
Address	0000000007011807 (SCOM)
Description	FIR Action Register Decodes. (Action0, Action1, Mask) (0,0,0) = Checkstop (0,1,0) = Recoverable (1,0,0) = Unused/recov_int (1,1,0) = Local core checkstop/freeze (X,X,1) = Masked

Bits	SCOM	Constant = 0b00000000000000000000000000000000000000000000000000000
0:53	RO	
54:61	RW	IOM_PHY2_DDRPHY_FIR_ACTION1_REG_DDR_FIR_ACTION1: See the corresponding FIR bit decodes in the register description.
62:63	RO	Constant = 0b00

Register Name	IOM_PHY2 Pervasive FIR WOF Register
Mnemonic	IOM0.IOM_PHY2_DDRPHY_FIR_WOF_REG
Address	0000000007011808 (SCOM)
Description	The Who Is on First Register indicates which error occurred first.

Bits	SCOM	Field Mnemonic: Description
0:53	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000
54:61	RWX_WCLRREG	IOM_PHY2_DDRPHY_FIR_WOF_REG_DDR_FIR_WOF: The WOF Register locks on the first error.
62:63	RO	Constant = 0b00

Register Name	IOM_PHY3 Pervasive FIR Register
Mnemonic	IOM0.IOM_PHY3_DDRPHY_FIR_REG
Address	0000000007011C00 (SCOM) 0000000007011C01 (SCOM1) 0000000007011C02 (SCOM2)
Description	Local FIR register for the chip pervasive logic

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:53	RO	RO	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000
54	RWX	WOX_AND	WOX_OR	IOM_PHY3_DDRPHY_FIR_REG_DDR_FIR_ERROR_0: PHYTOP Non-recoverable state machine errors.
55	RWX	WOX_AND	WOX_OR	IOM_PHY3_DDRPHY_FIR_REG_DDR_FIR_ERROR_1: PHYTOP and ADR parity errors affect the entire bus.
56	RWX	WOX_AND	WOX_OR	IOM_PHY3_DDRPHY_FIR_REG_DDR_FIR_ERROR_2: DP8/DP16 parity errors affecting initial calibration, initial calibration errors, and DLL errors during initial calibration.
57	RWX	WOX_AND	WOX_OR	IOM_PHY3_DDRPHY_FIR_REG_DDR_FIR_ERROR_3: PHYTOP and DP8/DP16 possibly recoverable state machine errors.
58	RWX	WOX_AND	WOX_OR	IOM_PHY3_DDRPHY_FIR_REG_DDR_FIR_ERROR_4: DP8/DP16 Parity errors affecting up to 16 bits. DLL errors during traffic are included.
59	RWX	WOX_AND	WOX_OR	IOM_PHY3_DDRPHY_FIR_REG_DDR_FIR_ERROR_5: DP8/DP16 parity errors affecting up to 8 bits.
60	RWX	WOX_AND	WOX_OR	IOM_PHY3_DDRPHY_FIR_REG_DDR_FIR_ERROR_6: DP8/DP16 parity errors affecting up to 4 bits.
61	RWX	WOX_AND	WOX_OR	IOM_PHY3_DDRPHY_FIR_REG_DDR_FIR_ERROR_7: DP8/DP16 parity errors affecting up to 1 bit.
62:63	RO	RO	RO	Constant = 0b00

Register Name	**IOM_PHY3 Pervasive FIR Mask Register**
Mnemonic	IOM0.IOM_PHY3_DDRPHY_FIR_MASK_REG
Address	0000000007011C03 (SCOM) 0000000007011C04 (SCOM1) 0000000007011C05 (SCOM2)
Description	This register contains the FIR mask bits for all the errors detected in the DDRPHY.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:53	RO	RO	RO	Constant = 0b00000000000000000000000000000000000000000000000000000
54	RW	WO_AND	WO_OR	IOM_PHY3_DDRPHY_FIR_MASK_REG_DDR_FIR_ERROR_0_MASK: Mask PHYTOP non-recoverable state machine errors.
55	RW	WO_AND	WO_OR	IOM_PHY3_DDRPHY_FIR_MASK_REG_DDR_FIR_ERROR_1_MASK: Mask PHYTOP (both non-recoverable and recoverable) and ADR parity errors (affect entire bus).
56	RW	WO_AND	WO_OR	IOM_PHY3_DDRPHY_FIR_MASK_REG_DDR_FIR_ERROR_2_MASK: Mask DP8/DP16 parity errors affecting initcal, initcal errors,DLL errors during initcal.
57	RW	WO_AND	WO_OR	IOM_PHY3_DDRPHY_FIR_MASK_REG_DDR_FIR_ERROR_3_MASK: Mask PHYTOP and DP8/DP16 possibly recoverable state machine errors.
58	RW	WO_AND	WO_OR	IOM_PHY3_DDRPHY_FIR_MASK_REG_DDR_FIR_ERROR_4_MASK: Mask DP8/DP16 parity errors affecting up to 16 bits, DLL errors during traffic included.
59	RW	WO_AND	WO_OR	IOM_PHY3_DDRPHY_FIR_MASK_REG_DDR_FIR_ERROR_5_MASK: Mask DP8/DP16 parity errors affecting up to 8 bit.
60	RW	WO_AND	WO_OR	IOM_PHY3_DDRPHY_FIR_MASK_REG_DDR_FIR_ERROR_6_MASK: Mask DP8/DP16 parity errors affecting up to 4 bit.
61	RW	WO_AND	WO_OR	IOM_PHY3_DDRPHY_FIR_MASK_REG_DDR_FIR_ERROR_7_MASK: Mask DP8/DP16 parity errors affecting up to 1 bit.
62:63	RO	RO	RO	Constant = 0b00

Register Name	**IOM_PHY3 Pervasive FIR Action 0 Register**
Mnemonic	IOM0.IOM_PHY3_DDRPHY_FIR_ACTION0_REG
Address	0000000007011C06 (SCOM)
Description	FIR Action Register Decodes. (Action0, Action1, Mask) (0,0,0) = Checkstop (0,1,0) = Recoverable (1,0,0) = Unused/recov_int (1,1,0) = Local core checkstop/freeze (X,X,1) = Masked

Bits	SCOM	Field Mnemonic: Description
0:53	RO	Constant = 0b00000000000000000000000000000000000000000000000000000
54:61	RW	IOM_PHY3_DDRPHY_FIR_ACTION0_REG_DDR_FIR_ACTION0: See the corresponding FIR bit decodes in the register description.
62:63	RO	Constant = 0b00

Register Name	IOM_PHY3 Pervasive FIR Action 1 Register
Mnemonic	IOM0.IOM_PHY3_DDRPHY_FIR_ACTION1_REG
Address	0000000007011C07 (SCOM)
Description	FIR Action Register Decodes. (Action0, Action1, Mask) (0,0,0) = Checkstop (0,1,0) = Recoverable (1,0,0) = Unused/recov_int (1,1,0) = Local core checkstop/freeze (X,X,1) = Masked

Bits	SCOM	Field Mnemonic: Description
0:53	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000
54:61	RW	IOM_PHY3_DDRPHY_FIR_ACTION1_REG_DDR_FIR_ACTION1: See the corresponding FIR bit decodes in the register description.
62:63	RO	Constant = 0b00

Register Name	IOM_PHY3 Pervasive FIR WOF Register
Mnemonic	IOM0.IOM_PHY3_DDRPHY_FIR_WOF_REG
Address	0000000007011C08 (SCOM)
Description	The Who Is on First Register indicates which error occurred first.

Bits	SCOM	Field Mnemonic: Description
0:53	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000
54:61	RWX_WCLRREG	IOM_PHY3_DDRPHY_FIR_WOF_REG_DDR_FIR_WOF: The WOF Register locks on the first error.
62:63	RO	Constant = 0b00

Register Name	MCBIST Fault Isolation Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBISTFIRQ
Address	0000000007012300 (SCOM) 0000000007012301 (SCOM1) 0000000007012302 (SCOM2)
Description	MCBIST Fault Isolation Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	MCBISTFIRQ_INVALID_MAINT_ADDRESS: Invalid maintenance address. Only in maintenance address mode, checks the start or end address for non-existent DIMM select, mrank, and srank bits that are high. Set at the beginning of the subtest that uses the invalid address.
1	RWX	WOX_AND	WOX_OR	MCBISTFIRQ_COMMAND_ADDRESS_TIMEOUT: Command address timeout. Timeout while waiting for an ACK to be received after a command request to the SRQ. The timeout threshold is determined by the cfg_cmd_timeout_mode in MCBCFG.
2	RWX	WOX_AND	WOX_OR	MCBISTFIRQ_INTERNAL_FSM_ERROR: Internal FSM error. Parity error on the MCBIST or CCS state machine.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
3	RWX	WOX_AND	WOX_OR	MCBISTFIRQ_MCBIST_BRODCAST_OUT_OF_SYNC: MCBIST broadcast out of sync. This bit is set when we detect that ports are out of sync that the MCBIST is broadcasting commands to. Specifically, this can possibly indicate one of the following: 1. MCBIST saw a response from some MCBIST-active ports but not all. 2. MCBIST saw a response from non MCBIST-active ports. Detection logic is based on req, ACK, valid, and done signals from ports.
4	RWX	WOX_AND	WOX_OR	MCBISTFIRQ_MCBIST_DATA_ERROR: MCBIST data error. This bit is set when the MCBIST has detected an error that is configured to be trapped.
5	RWX	WOX_AND	WOX_OR	MCBISTFIRQ_HARD_NCE_ETE_ATTN: Hard NCE ETE attention. This bit is set when the hard NCE error threshold has been triggered.
6	RWX	WOX_AND	WOX_OR	MCBISTFIRQ_SOFT_NCE_ETE_ATTN: Soft NCE ETE Attention. This bit is set when the soft NCE error threshold has been triggered.
7	RWX	WOX_AND	WOX_OR	MCBISTFIRQ_INT_NCE_ETE_ATTN: Intermittent NCE ETE attention. This bit is set when the intermittent NCE error threshold has been triggered.
8	RWX	WOX_AND	WOX_OR	MCBISTFIRQ_RCE_ETE_ATTN: RCE ETE attention. This bit is set when the RCE error threshold has been triggered.
9	RWX	WOX_AND	WOX_OR	MCBISTFIRQ_ICE_ETE_ATTN: ICE (IMPE) ETE attention. This bit is set when the ICE error threshold has been triggered.
10	RWX	WOX_AND	WOX_OR	MCBISTFIRQ_MCBIST_PROGRAM_COMPLETE: MCBIST program complete. This bit is set whenever the MCBIST pauses or stops. If MCB_CNTLSTATQ(0) MCB_IP is also set, this is a pause. If MCB_CNTLSTATQ(0) MCB_IP is not also set, this is a stop.
11	RWX	WOX_AND	WOX_OR	MCBISTFIRQ_MCBIST_CCS_SUBTEST_DONE: MCBIST CCS subtest done. This bit is set when an MCBIST-initiated CCS subtest completes.
12	RWX	WOX_AND	WOX_OR	MCBISTFIRQ_WAT_DEBUG_ATTN: WAT debug bus attention. This is a way for the WAT debug bus to trigger an attention.
13	RWX	WOX_AND	WOX_OR	MCBISTFIRQ_SCOM_RECOVERABLE_REG_PE: SCOM recoverable register parity error. This bit is set when a recoverable parity error on a SCOM register takes place. These register errors are configuration-related. They are unable to corrupt data or mainline, and they can be contained by simply not using the MCBIST.
14	RWX	WOX_AND	WOX_OR	MCBISTFIRQ_SCOM_FATAL_REG_PE: SCOM fatal register parity error. This bit is set when a fatal parity error on a SCOM register takes place. These register errors are control-related. They are able to corrupt data or mainline, and they cannot be contained by simply not using MCBIST.
15	RWX	WOX_AND	WOX_OR	MCBISTFIRQ_WAT_DEBUG_REG_PE: SCOM WAT and debug register parity error. Indicates that control registers for WAT and debug logic have taken a parity error.
16	RWX	WOX_AND	WOX_OR	MCBISTFIRQ_RESERVED_16: Reserved.
17	RWX	WOX_AND	WOX_OR	MCBISTFIRQ_RESERVED_17: Reserved.
18	RWX	WOX_AND	WOX_OR	MCBISTFIRQ_INTERNAL_SCOM_ERROR: Internal SCOM error.
19	RWX	WOX_AND	WOX_OR	MCBISTFIRQ_INTERNAL_SCOM_ERROR_CLONE: Internal SCOM error clone.
20:63	RO	RO	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	MCBIST Fault Isolation Mask Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBISTFIRMASK
Address	0000000007012303 (SCOM) 0000000007012304 (SCOM1) 0000000007012305 (SCOM2)
Description	MCBIST Fault Isolation Mask Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:19	RW	WO_AND	WO_OR	MCBISTFIRMASK_FIR_MASK: Mask for FIR bits 0:63.
20:63	RO	RO	RO	Constant = 0b00000000000000000000000000000000000000000000000

Register Name	MCBIST Fault Isolation Action 0 Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBISTFIRACT0
Address	0000000007012306 (SCOM)
Description	MCBIST Fault Isolation Action 0 Register

Bits	SCOM	Field Mnemonic: Description
0:19	RW	MCBISTFIRACT0_FIR_ACTION0: Action0 select for the corresponding bits in the FIR. (Action0, Action1, Mask) selects: (0,0,0) = Checkstop error (0,1,0) = Recoverable error (1,0,0) = Attention (1,1,0) = Local checkstop error (X,X,1) = Masked
20:63	RO	Constant = 0b00000000000000000000000000000000000000000000000

Register Name	MCBIST Fault Isolation Action 1 Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBISTFIRACT1
Address	0000000007012307 (SCOM)
Description	MCBIST Fault Isolation Action 1 Register

Bits	SCOM	Field Mnemonic: Description
0:19	RW	MCBISTFIRACT1_FIR_ACTION1: Action1 select for the corresponding bits in the FIR. (Action0, Action1, Mask) selects: (0,0,0) = Checkstop error (0,1,0) = Recoverable error (1,0,0) = Attention (1,1,0) = Local checkstop error (X,X,1) = Masked
20:63	RO	Constant = 0b00000000000000000000000000000000000000000000000

Register Name	MCBIST Fault Isolation WOF Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBISTFIRWOF
Address	0000000007012308 (SCOM)
Description	MCBIST Fault Isolation WOF Register

Bits	SCOM	Field Mnemonic: Description
0:19	RWX_WCLRREG	MCBISTFIRWOF_INVALID_MAINT_ADDRESS: The WOF Register locks on the first error. Writing zeros the register.
20:63	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	MBA Error Control Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MBECTLQ
Address	0000000007012310 (SCOM)
Description	MBA Error Control Register

Bits	SCOM	Field Mnemonic: Description
0	RW	MBECTLQ_ATOMIC_ALT_CE_INJ: Atomic Alter CE inject. This bit is used with the Atomic Alter Error Inject command to inject a CE. When set, MBECTL[4:10] are used to select the symbol to be modified.
1	RW	MBECTLQ_ATOMIC_ALT_CHIP_KILL_INJ: Atomic Alter Chip Kill inject. This bit is used with the Atomic Alter Error Inject command to inject a Mark Place Error (MPE), or a Mark Correct Error (MCE), if a mark is already in place for the chip kill error being injected. When set, MBECTL[4:10] are used to select the mark to be modified.
2	RW	MBECTLQ_ATOMIC_ALT_UE_INJ: Atomic Alter UE inject. This bit is used with the Atomic Alter Error Inject command to inject an uncorrectable error. When set, symbols 66 - 71 are inverted to create a UE.
3	RW	MBECTLQ_ATOMIC_ALT_SUE_INJ: Atomic Alter SUE inject. This bit is used with the Atomic Alter Error Inject command to inject an SUE. It turns on the SUE bit in the 65th byte.
4:10	RW	MBECTLQ_ATOMIC_ALT_INJ_SYM_SEL: The atomic alter inject symbol select has three modes: • CE inject • Chip kill (x4 mode) • Chip kill (x8 mode)
11	RW	MBECTLQ_RESERVE_11: Reserved.
12	RW	MBECTLQ_SCOM_CMD_REG_INJ_MODE: 0 = Single shot inject error 1 = Continuous inject error
13	RW	MBECTLQ_SCOM_CMD_REG_INJ: Parity error inject mode into the CCS Control Register; detected by the MCBISTFIR[14].
14	RW	MBECTLQ_MCBIST_FSM_INJ_MODE: Parity error inject mode for injecting a parity error into the MCBIST state machine; detected by MCBISTFIR[2].
15	RW	MBECTLQ_MCBIST_FSM_INJ_REG: Parity error inject for injecting a parity error into the MCBIST state machine; detected by MCBISTFIR[2].
16	RW	MBECTLQ_CCS_FSM_INJ_MODE: Parity error inject mode for injecting a parity error into the CCS state machine; detected by MCBISTFIR[2]. **Note**: CCS must be enabled first.
17	RW	MBECTLQ_CCS_FSM_INJ_REG: Parity error inject for injecting a parity error into the CCS state machine; detected by MCBISTFIR[2]. **Note**: CCS must be enabled first.

Bits	SCOM	Field Mnemonic: Description
18:31	RW	MBECTLQ_RESERVED_18_31: Reserved.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	CCS INST ARR0 00 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR0_00
Address	0000000007012315 (SCOM)
Description	CCS INST ARR0 00

Bits	SCOM	Field Mnemonic: Description
0:13	RW	CCS_INST_ARR0_00_CCS_DDR_ADDRESS_0_13: DDR Address Row Column; bits 0:13.
14	RW	CCS_INST_ARR0_00_CCS_DDR_ADDRESS_17: DDR Address Row Column; bit 17 (formerly labeled address(14) for IBM POWER8®).
15	RW	CCS_INST_ARR0_00_CCS_DDR_BANK_GROUP_1: DDR Address Bank Group; bit 1 (formerly labeled address(15) for POWER8).
16	RW	CCS_INST_ARR0_00_CCS_DDR_RESETN: DDR Resetn. Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) controls the value of DDR Resetn.
17:18	RW	CCS_INST_ARR0_00_CCS_DDR_BANK_0_1: DDR Address Bank; bits 0:1.
19	RW	CCS_INST_ARR0_00_CCS_DDR_BANK_GROUP_0: DDR Address Bank Group; bit 0 (formerly labeled bank(2) for POWER8).
20	RW	CCS_INST_ARR0_00_CCS_DDR_ACTN: DDR Activate Not (formerly labeled Active although functionally equivalent for POWER8).
21	RW	CCS_INST_ARR0_00_CCS_DDR_ADDRESS_16: DDR Address Row Column; bit 16 (formerly labeled rasn for POWER8).
22	RW	CCS_INST_ARR0_00_CCS_DDR_ADDRESS_15: DDR Address Row Column; bit 15 (formerly labeled casn for POWER8).
23	RW	CCS_INST_ARR0_00_CCS_DDR_ADDRESS_14: DDR Address Row Column; bit 14 (formerly labeled wen for POWER8).
24:27	RW	CCS_INST_ARR0_00_CCS_DDR_CKE: DDR CKE. ccs_ddr_cke[0:1] → CKE[0:1] (also CKE[2:3] when CKEs copied enabled). ccs_ddr_cke[2:3] → CKE[4:5] (also CKE[6:7] when CKEs copied enabled).
28:31	RW	CCS_INST_ARR0_00_RESERVED_28_31: Reserved.
32:33	RW	CCS_INST_ARR0_00_CCS_DDR_CSN_0_1: DDR CSN Chip Select Not; bits 0:1.
34:35	RW	CCS_INST_ARR0_00_CCS_DDR_CID_0_1: DDR CID Chip ID; bits 0:1.
36:37	RW	CCS_INST_ARR0_00_CCS_DDR_CSN_2_3: DDR CSN Chip Select Not; bits 2:3.
38	RW	CCS_INST_ARR0_00_CCS_DDR_CID_2: DDR CID Chip ID; bit 2.
39:47	RW	CCS_INST_ARR0_00_RESERVED_39_47: Reserved.
48:51	RW	CCS_INST_ARR0_00_CCS_DDR_ODT: DDR ODT.
52:55	RW	CCS_INST_ARR0_00_RESERVED_52_55: Reserved.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	CCS_INST_ARR0_00_CCS_DDR_CAL_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the subtype. 0123 11XX = Initial calibration. Performs all of the following steps that are enabled via the configuration register: • SysclkRdclk alignment • DQS alignment • Read eye MPR centering • Write leveling • Write centering • Coarse rdwr alignment • Read eye custom pattern centering 10XX = Internal ZQ calibration (cal_rank is ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step.
60	RW	CCS_INST_ARR0_00_CCS_DDR_PARITY: DDR Parity. Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61	RW	CCS_INST_ARR0_00_CCS_DDR_BANK_2: DDR Address Bank; bit 2 (new for POWER9 DDR4E).
62:63	RW	CCS_INST_ARR0_00_CCS_LOOP_BREAK_MODE: Selects which programmable iteration value to compare to in order to break out of the loop. 00 = Never break out of the loop. 01 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare0. 10 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare1. 11 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare2. **Note**: This is now held in local latches instead of the array for earlier access.

Register Name	CCS INST ARR0 01 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR0_01
Address	0000000007012316 (SCOM)
Description	CCS INST ARR0 01

Bits	SCOM	Field Mnemonic: Description
0:13	RW	CCS_INST_ARR0_01_CCS_DDR_ADDRESS_0_13: DDR Address Row Column; bits 0:13.
14	RW	CCS_INST_ARR0_01_CCS_DDR_ADDRESS_17: DDR Address Row Column; bit 17 (formerly labeled address(14) for POWER8).
15	RW	CCS_INST_ARR0_01_CCS_DDR_BANK_GROUP_1: DDR Address Bank Group; bit 1 (formerly labeled address(15) for POWER8).
16	RW	CCS_INST_ARR0_01_CCS_DDR_RESETN: DDR Resetn. Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) controls the value of DDR Resetn.
17:18	RW	CCS_INST_ARR0_01_CCS_DDR_BANK_0_1: DDR Address Bank; bits 0:1.
19	RW	CCS_INST_ARR0_01_CCS_DDR_BANK_GROUP_0: DDR Address Bank Group; bit 0 (formerly labeled bank(2) for POWER8).
20	RW	CCS_INST_ARR0_01_CCS_DDR_ACTN: DDR Activate Not (formerly labeled Active although functionally equivalent for POWER8).
21	RW	CCS_INST_ARR0_01_CCS_DDR_ADDRESS_16: DDR Address Row Column; bit 16 (formerly labeled rasn for POWER8).

Bits	SCOM	Field Mnemonic: Description
22	RW	CCS_INST_ARR0_01_CCS_DDR_ADDRESS_15: DDR Address Row Column; bit 15 (formerly labeled casn for POWER8).
23	RW	CCS_INST_ARR0_01_CCS_DDR_ADDRESS_14: DDR Address Row Column; bit 14 (formerly labeled wen for POWER8).
24:27	RW	CCS_INST_ARR0_01_CCS_DDR_CKE: DDR CKE. ccs_ddr_cke[0:1] → CKE[0:1] (also CKE[2:3] when CKEs copied enabled). ccs_ddr_cke[2:3] → CKE[4:5] (also CKE[6:7] when CKEs copied enabled).
28:31	RW	CCS_INST_ARR0_01_RESERVED_28_31: Reserved.
32:33	RW	CCS_INST_ARR0_01_CCS_DDR_CSN_0_1: DDR CSN Chip Select Not; bits 0:1.
34:35	RW	CCS_INST_ARR0_01_CCS_DDR_CID_0_1: DDR CID Chip ID; bits 0:1.
36:37	RW	CCS_INST_ARR0_01_CCS_DDR_CSN_2_3: DDR CSN Chip Select Not; bits 2:3.
38	RW	CCS_INST_ARR0_01_CCS_DDR_CID_2: DDR CID Chip ID; bit 2.
39:47	RW	CCS_INST_ARR0_01_RESERVED_39_47: Reserved.
48:51	RW	CCS_INST_ARR0_01_CCS_DDR_ODT: DDR ODT.
52:55	RW	CCS_INST_ARR0_01_RESERVED_52_55: Reserved.
56:59	RW	CCS_INST_ARR0_01_CCS_DDR_CAL_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the subtype. 0123 11XX = Initial calibration. Performs all of the following steps that are enabled via the configuration register: • SysclkRdclk alignment • DQS alignment • Read eye MPR centering • Write leveling • Write centering • Coarse rdwr alignment • Read eye custom pattern centering 10XX = Internal ZQ calibration (cal_rank is ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step.
60	RW	CCS_INST_ARR0_01_CCS_DDR_PARITY: DDR Parity. Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61	RW	CCS_INST_ARR0_01_CCS_DDR_BANK_2: DDR Address Bank; bit 2 (new for POWER9 DDR4E).
62:63	RW	CCS_INST_ARR0_01_CCS_LOOP_BREAK_MODE: Selects which programmable iteration value to compare to in order to break out of the loop. 00 = Never break out of the loop. 01 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare0. 10 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare1. 11 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare2. **Note**: This is now held in local latches instead of the array for earlier access.

Register Name	CCS INST ARR0 02 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR0_02
Address	0000000007012317 (SCOM)
Description	CCS INST ARR0 02

Bits	SCOM	Field Mnemonic: Description
0:13	RW	CCS_INST_ARR0_02_CCS_DDR_ADDRESS_0_13: DDR Address Row Column; bits 0:13.
14	RW	CCS_INST_ARR0_02_CCS_DDR_ADDRESS_17: DDR Address Row Column; bit 17 (formerly labeled address(14) for POWER8).
15	RW	CCS_INST_ARR0_02_CCS_DDR_BANK_GROUP_1: DDR Address Bank Group; bit 1 (formerly labeled address(15) for POWER8).
16	RW	CCS_INST_ARR0_02_CCS_DDR_RESETN: DDR Resetn. Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq[24] controls the value of DDR Resetn.
17:18	RW	CCS_INST_ARR0_02_CCS_DDR_BANK_0_1: DDR Address Bank; bits 0:1.
19	RW	CCS_INST_ARR0_02_CCS_DDR_BANK_GROUP_0: DDR Address Bank Group; bit 0 (formerly labeled bank(2) for POWER8).
20	RW	CCS_INST_ARR0_02_CCS_DDR_ACTN: DDR Activate Not (formerly labeled Active although functionally equivalent for POWER8).
21	RW	CCS_INST_ARR0_02_CCS_DDR_ADDRESS_16: DDR Address Row Column; bit 16 (formerly labeled rasn for POWER8).
22	RW	CCS_INST_ARR0_02_CCS_DDR_ADDRESS_15: DDR Address Row Column; bit 15 (formerly labeled casn for POWER8).
23	RW	CCS_INST_ARR0_02_CCS_DDR_ADDRESS_14: DDR Address Row Column; bit 14 (formerly labeled wen for POWER8).
24:27	RW	CCS_INST_ARR0_02_CCS_DDR_CKE: DDR CKE. ccs_ddr_cke[0:1] → CKE[0:1] (also CKE[2:3] when CKEs copied enabled). ccs_ddr_cke[2:3] → CKE[4:5] (also CKE[6:7] when CKEs copied enabled).
28:31	RW	CCS_INST_ARR0_02_RESERVED_28_31: Reserved.
32:33	RW	CCS_INST_ARR0_02_CCS_DDR_CSN_0_1: DDR CSN Chip Select Not; bits 0:1.
34:35	RW	CCS_INST_ARR0_02_CCS_DDR_CID_0_1: DDR CID Chip ID; bits 0:1.
36:37	RW	CCS_INST_ARR0_02_CCS_DDR_CSN_2_3: DDR CSN Chip Select Not; bits 2:3.
38	RW	CCS_INST_ARR0_02_CCS_DDR_CID_2: DDR CID Chip ID; bit 2.
39:47	RW	CCS_INST_ARR0_02_RESERVED_39_47: Reserved.
48:51	RW	CCS_INST_ARR0_02_CCS_DDR_ODT: DDR ODT.
52:55	RW	CCS_INST_ARR0_02_RESERVED_52_55: Reserved.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	CCS_INST_ARR0_02_CCS_DDR_CAL_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the subtype. 0123 11XX = Initial calibration. Performs all of the following steps that are enabled via the configuration register: • SysclkRdclk alignment • DQS alignment • Read eye MPR centering • Write leveling • Write centering • Coarse rdwr alignment • Read eye custom pattern centering 10XX = Internal ZQ calibration (cal_rank is ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step.
60	RW	CCS_INST_ARR0_02_CCS_DDR_PARITY: DDR Parity. Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61	RW	CCS_INST_ARR0_02_CCS_DDR_BANK_2: DDR Address Bank; bit 2 (new for POWER9 DDR4E).
62:63	RW	CCS_INST_ARR0_02_CCS_LOOP_BREAK_MODE: Selects which programmable iteration value to compare to in order to break out of the loop. 00 = Never break out of the loop. 01 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare0. 10 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare1. 11 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare2. **Note**: This is now held in local latches instead of the array for earlier access.

Register Name	CCS INST ARR0 03 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR0_03
Address	0000000007012318 (SCOM)
Description	CCS INST ARR0 03

Bits	SCOM	Field Mnemonic: Description
0:13	RW	CCS_INST_ARR0_03_CCS_DDR_ADDRESS_0_13: DDR Address Row Column; bits 0:13.
14	RW	CCS_INST_ARR0_03_CCS_DDR_ADDRESS_17: DDR Address Row Column; bit 17 (formerly labeled address(14) for POWER8).
15	RW	CCS_INST_ARR0_03_CCS_DDR_BANK_GROUP_1: DDR Address Bank Group; bit 1 (formerly labeled address(15) for POWER8).
16	RW	CCS_INST_ARR0_03_CCS_DDR_RESETN: DDR Resetn. Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq[24] controls the value of DDR Resetn.
17:18	RW	CCS_INST_ARR0_03_CCS_DDR_BANK_0_1: DDR Address Bank; bits 0:1.
19	RW	CCS_INST_ARR0_03_CCS_DDR_BANK_GROUP_0: DDR Address Bank Group; bit 0 (formerly labeled bank(2) for POWER8).
20	RW	CCS_INST_ARR0_03_CCS_DDR_ACTN: DDR Activate Not (formerly labeled Active although functionally equivalent for POWER8).
21	RW	CCS_INST_ARR0_03_CCS_DDR_ADDRESS_16: DDR Address Row Column; bit 16 (formerly labeled rasn for POWER8).

Bits	SCOM	Field Mnemonic: Description
22	RW	CCS_INST_ARR0_03_CCS_DDR_ADDRESS_15: DDR Address Row Column; bit 15 (formerly labeled casn for POWER8).
23	RW	CCS_INST_ARR0_03_CCS_DDR_ADDRESS_14: DDR Address Row Column; bit 14 (formerly labeled wen for POWER8).
24:27	RW	CCS_INST_ARR0_03_CCS_DDR_CKE: DDR CKE. ccs_ddr_cke[0:1] → CKE[0:1] (also CKE[2:3] when CKEs copied enabled). ccs_ddr_cke[2:3] → CKE[4:5] (also CKE[6:7] when CKEs copied enabled).
28:31	RW	CCS_INST_ARR0_03_RESERVED_28_31: Reserved.
32:33	RW	CCS_INST_ARR0_03_CCS_DDR_CSN_0_1: DDR CSN Chip Select Not; bits 0:1.
34:35	RW	CCS_INST_ARR0_03_CCS_DDR_CID_0_1: DDR CID Chip ID; bits 0:1.
36:37	RW	CCS_INST_ARR0_03_CCS_DDR_CSN_2_3: DDR CSN Chip Select Not; bits 2:3.
38	RW	CCS_INST_ARR0_03_CCS_DDR_CID_2: DDR CID Chip ID; bit 2.
39:47	RW	CCS_INST_ARR0_03_RESERVED_39_47: Reserved.
48:51	RW	CCS_INST_ARR0_03_CCS_DDR_ODT: DDR ODT.
52:55	RW	CCS_INST_ARR0_03_RESERVED_52_55: Reserved.
56:59	RW	CCS_INST_ARR0_03_CCS_DDR_CAL_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the subtype. 0123 11XX = Initial calibration. Performs all of the following steps that are enabled via the configuration register: • SysclkRdclk alignment • DQS alignment • Read eye MPR centering • Write leveling • Write centering • Coarse rdwr alignment • Read eye custom pattern centering 10XX = Internal ZQ calibration (cal_rank is ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step.
60	RW	CCS_INST_ARR0_03_CCS_DDR_PARITY: DDR Parity. Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61	RW	CCS_INST_ARR0_03_CCS_DDR_BANK_2: DDR Address Bank; bit 2 (new for POWER9 DDR4E).
62:63	RW	CCS_INST_ARR0_03_CCS_LOOP_BREAK_MODE: Selects which programmable iteration value to compare to in order to break out of the loop. 00 = Never break out of the loop. 01 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare0. 10 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare1. 11 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare2. **Note**: This is now held in local latches instead of the array for earlier access.

Register Name	CCS INST ARR0 04 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR0_04
Address	0000000007012319 (SCOM)
Description	CCS INST ARR0 04

Bits	SCOM	Field Mnemonic: Description
0:13	RW	CCS_INST_ARR0_04_CCS_DDR_ADDRESS_0_13: DDR Address Row Column; bits 0:13.
14	RW	CCS_INST_ARR0_04_CCS_DDR_ADDRESS_17: DDR Address Row Column; bit 17 (formerly labeled address(14) for POWER8).
15	RW	CCS_INST_ARR0_04_CCS_DDR_BANK_GROUP_1: DDR Address Bank Group; bit 1 (formerly labeled address(15) for POWER8).
16	RW	CCS_INST_ARR0_04_CCS_DDR_RESETN: DDR Resetn. Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq[24] controls the value of DDR Resetn.
17:18	RW	CCS_INST_ARR0_04_CCS_DDR_BANK_0_1: DDR Address Bank; bits 0:1.
19	RW	CCS_INST_ARR0_04_CCS_DDR_BANK_GROUP_0: DDR Address Bank Group; bit 0 (formerly labeled bank(2) for POWER8).
20	RW	CCS_INST_ARR0_04_CCS_DDR_ACTN: DDR Activate Not (formerly labeled Active although functionally equivalent for POWER8).
21	RW	CCS_INST_ARR0_04_CCS_DDR_ADDRESS_16: DDR Address Row Column; bit 16 (formerly labeled rasn for POWER8).
22	RW	CCS_INST_ARR0_04_CCS_DDR_ADDRESS_15: DDR Address Row Column; bit 15 (formerly labeled casn for POWER8).
23	RW	CCS_INST_ARR0_04_CCS_DDR_ADDRESS_14: DDR Address Row Column; bit 14 (formerly labeled wen for POWER8).
24:27	RW	CCS_INST_ARR0_04_CCS_DDR_CKE: DDR CKE. ccs_ddr_cke[0:1] → CKE[0:1] (also CKE[2:3] when CKEs copied enabled). ccs_ddr_cke[2:3] → CKE[4:5] (also CKE[6:7] when CKEs copied enabled).
28:31	RW	CCS_INST_ARR0_04_RESERVED_28_31: Reserved.
32:33	RW	CCS_INST_ARR0_04_CCS_DDR_CSN_0_1: DDR CSN Chip Select Not; bits 0:1.
34:35	RW	CCS_INST_ARR0_04_CCS_DDR_CID_0_1: DDR CID Chip ID; bits 0:1.
36:37	RW	CCS_INST_ARR0_04_CCS_DDR_CSN_2_3: DDR CSN Chip Select Not; bits 2:3.
38	RW	CCS_INST_ARR0_04_CCS_DDR_CID_2: DDR CID Chip ID; bit 2.
39:47	RW	CCS_INST_ARR0_04_RESERVED_39_47: Reserved.
48:51	RW	CCS_INST_ARR0_04_CCS_DDR_ODT: DDR ODT.
52:55	RW	CCS_INST_ARR0_04_RESERVED_52_55: Reserved.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	CCS_INST_ARR0_04_CCS_DDR_CAL_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the subtype. 0123 11XX = Initial calibration. Performs all of the following steps that are enabled via the configuration register: • SysclkRdclk alignment • DQS alignment • Read eye MPR centering • Write leveling • Write centering • Coarse rdwr alignment • Read eye custom pattern centering 10XX = Internal ZQ calibration (cal_rank is ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step.
60	RW	CCS_INST_ARR0_04_CCS_DDR_PARITY: DDR Parity. Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61	RW	CCS_INST_ARR0_04_CCS_DDR_BANK_2: DDR Address Bank; bit 2 (new for POWER9 DDR4E).
62:63	RW	CCS_INST_ARR0_04_CCS_LOOP_BREAK_MODE: Selects which programmable iteration value to compare to in order to break out of the loop. 00 = Never break out of the loop. 01 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare0. 10 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare1. 11 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare2. **Note**: This is now held in local latches instead of the array for earlier access.

Register Name	CCS INST ARR0 05 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR0_05
Address	000000000701231A (SCOM)
Description	CCS INST ARR0 05

Bits	SCOM	Field Mnemonic: Description
0:13	RW	CCS_INST_ARR0_05_CCS_DDR_ADDRESS_0_13: DDR Address Row Column; bits 0:13.
14	RW	CCS_INST_ARR0_05_CCS_DDR_ADDRESS_17: DDR Address Row Column; bit 17 (formerly labeled address(14) for POWER8).
15	RW	CCS_INST_ARR0_05_CCS_DDR_BANK_GROUP_1: DDR Address Bank Group; bit 1 (formerly labeled address(15) for POWER8).
16	RW	CCS_INST_ARR0_05_CCS_DDR_RESETN: DDR Resetn. Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq[24] controls the value of DDR Resetn.
17:18	RW	CCS_INST_ARR0_05_CCS_DDR_BANK_0_1: DDR Address Bank; bits 0:1.
19	RW	CCS_INST_ARR0_05_CCS_DDR_BANK_GROUP_0: DDR Address Bank Group; bit 0 (formerly labeled bank(2) for POWER8).
20	RW	CCS_INST_ARR0_05_CCS_DDR_ACTN: DDR Activate Not (formerly labeled Active although functionally equivalent for POWER8).
21	RW	CCS_INST_ARR0_05_CCS_DDR_ADDRESS_16: DDR Address Row Column; bit 16 (formerly labeled rasn for POWER8).

Bits	SCOM	Field Mnemonic: Description
22	RW	CCS_INST_ARR0_05_CCS_DDR_ADDRESS_15: DDR Address Row Column; bit 15 (formerly labeled casn for POWER8).
23	RW	CCS_INST_ARR0_05_CCS_DDR_ADDRESS_14: DDR Address Row Column; bit 14 (formerly labeled wen for POWER8).
24:27	RW	CCS_INST_ARR0_05_CCS_DDR_CKE: DDR CKE. ccs_ddr_cke[0:1] → CKE[0:1] (also CKE[2:3] when CKEs copied enabled). ccs_ddr_cke[2:3] → CKE[4:5] (also CKE[6:7] when CKEs copied enabled).
28:31	RW	CCS_INST_ARR0_05_RESERVED_28_31: Reserved.
32:33	RW	CCS_INST_ARR0_05_CCS_DDR_CSN_0_1: DDR CSN Chip Select Not; bits 0:1.
34:35	RW	CCS_INST_ARR0_05_CCS_DDR_CID_0_1: DDR CID Chip ID; bits 0:1.
36:37	RW	CCS_INST_ARR0_05_CCS_DDR_CSN_2_3: DDR CSN Chip Select Not; bits 2:3.
38	RW	CCS_INST_ARR0_05_CCS_DDR_CID_2: DDR CID Chip ID; bit 2.
39:47	RW	CCS_INST_ARR0_05_RESERVED_39_47: Reserved.
48:51	RW	CCS_INST_ARR0_05_CCS_DDR_ODT: DDR ODT.
52:55	RW	CCS_INST_ARR0_05_RESERVED_52_55: Reserved.
56:59	RW	CCS_INST_ARR0_05_CCS_DDR_CAL_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the subtype. 0123 11XX = Initial calibration. Performs all of the following steps that are enabled via the configuration register: • SysclkRdclk alignment • DQS alignment • Read eye MPR centering • Write leveling • Write centering • Coarse rdwr alignment • Read eye custom pattern centering 10XX = Internal ZQ calibration (cal_rank is ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step.
60	RW	CCS_INST_ARR0_05_CCS_DDR_PARITY: DDR Parity. Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61	RW	CCS_INST_ARR0_05_CCS_DDR_BANK_2: DDR Address Bank; bit 2 (new for POWER9 DDR4E)
62:63	RW	CCS_INST_ARR0_05_CCS_LOOP_BREAK_MODE: Selects which programmable iteration value to compare to in order to break out of the loop. 00 = Never break out of the loop. 01 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare0. 10 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare1. 11 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare2. **Note**: This is now held in local latches instead of the array for earlier access.

Register Name	CCS INST ARR0 06 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR0_06
Address	000000000701231B (SCOM)
Description	CCS INST ARR0 06

Bits	SCOM	Field Mnemonic: Description
0:13	RW	CCS_INST_ARR0_06_CCS_DDR_ADDRESS_0_13: DDR Address Row Column; bits 0:13.
14	RW	CCS_INST_ARR0_06_CCS_DDR_ADDRESS_17: DDR Address Row Column; bit 17 (formerly labeled address(14) for POWER8).
15	RW	CCS_INST_ARR0_06_CCS_DDR_BANK_GROUP_1: DDR Address Bank Group; bit 1 (formerly labeled address(15) for POWER8).
16	RW	CCS_INST_ARR0_06_CCS_DDR_RESETN: DDR Resetn. Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq[24] controls the value of DDR Resetn.
17:18	RW	CCS_INST_ARR0_06_CCS_DDR_BANK_0_1: DDR Address Bank; bits 0:1.
19	RW	CCS_INST_ARR0_06_CCS_DDR_BANK_GROUP_0: DDR Address Bank Group; bit 0 (formerly labeled bank(2) for POWER8).
20	RW	CCS_INST_ARR0_06_CCS_DDR_ACTN: DDR Activate Not (formerly labeled Active although functionally equivalent for POWER8).
21	RW	CCS_INST_ARR0_06_CCS_DDR_ADDRESS_16: DDR Address Row Column; bit 16 (formerly labeled rasn for POWER8).
22	RW	CCS_INST_ARR0_06_CCS_DDR_ADDRESS_15: DDR Address Row Column; bit 15 (formerly labeled casn for POWER8).
23	RW	CCS_INST_ARR0_06_CCS_DDR_ADDRESS_14: DDR Address Row Column; bit 14 (formerly labeled wen for POWER8).
24:27	RW	CCS_INST_ARR0_06_CCS_DDR_CKE: DDR CKE. ccs_ddr_cke[0:1] → CKE[0:1] (also CKE[2:3] when CKEs copied enabled). ccs_ddr_cke[2:3] → CKE[4:5] (also CKE[6:7] when CKEs copied enabled).
28:31	RW	CCS_INST_ARR0_06_RESERVED_28_31: Reserved.
32:33	RW	CCS_INST_ARR0_06_CCS_DDR_CSN_0_1: DDR CSN Chip Select Not; bits 0:1.
34:35	RW	CCS_INST_ARR0_06_CCS_DDR_CID_0_1: DDR CID Chip ID; bits 0:1.
36:37	RW	CCS_INST_ARR0_06_CCS_DDR_CSN_2_3: DDR CSN Chip Select Not; bits 2:3.
38	RW	CCS_INST_ARR0_06_CCS_DDR_CID_2: DDR CID Chip ID; bit 2.
39:47	RW	CCS_INST_ARR0_06_RESERVED_39_47: Reserved.
48:51	RW	CCS_INST_ARR0_06_CCS_DDR_ODT: DDR ODT.
52:55	RW	CCS_INST_ARR0_06_RESERVED_52_55: Reserved.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	CCS_INST_ARR0_06_CCS_DDR_CAL_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the subtype. 0123 11XX = Initial calibration. Performs all of the following steps that are enabled via the configuration register: • SysclkRdclk alignment • DQS alignment • Read eye MPR centering • Write leveling • Write centering • Coarse rdwr alignment • Read eye custom pattern centering 10XX = Internal ZQ calibration (cal_rank is ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step.
60	RW	CCS_INST_ARR0_06_CCS_DDR_PARITY: DDR Parity. Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61	RW	CCS_INST_ARR0_06_CCS_DDR_BANK_2: DDR Address Bank; bit 2 (new for POWER9 DDR4E).
62:63	RW	CCS_INST_ARR0_06_CCS_LOOP_BREAK_MODE: Selects which programmable iteration value to compare to in order to break out of the loop. 00 = Never break out of the loop. 01 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare0. 10 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare1. 11 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare2. **Note**: This is now held in local latches instead of the array for earlier access.

Register Name	CCS INST ARR0 07 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR0_07
Address	000000000701231C (SCOM)
Description	CCS INST ARR0 07

Bits	SCOM	Field Mnemonic: Description
0:13	RW	CCS_INST_ARR0_07_CCS_DDR_ADDRESS_0_13: DDR Address Row Column; bits 0:13.
14	RW	CCS_INST_ARR0_07_CCS_DDR_ADDRESS_17: DDR Address Row Column; bit 17 (formerly labeled address(14) for POWER8).
15	RW	CCS_INST_ARR0_07_CCS_DDR_BANK_GROUP_1: DDR Address Bank Group; bit 1 (formerly labeled address(15) for POWER8).
16	RW	CCS_INST_ARR0_07_CCS_DDR_RESETN: DDR Resetn. Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq[24] controls the value of DDR Resetn.
17:18	RW	CCS_INST_ARR0_07_CCS_DDR_BANK_0_1: DDR Address Bank; bits 0:1.
19	RW	CCS_INST_ARR0_07_CCS_DDR_BANK_GROUP_0: DDR Address Bank Group; bit 0 (formerly labeled bank(2) for POWER8).
20	RW	CCS_INST_ARR0_07_CCS_DDR_ACTN: DDR Activate Not (formerly labeled Active although functionally equivalent for POWER8).
21	RW	CCS_INST_ARR0_07_CCS_DDR_ADDRESS_16: DDR Address Row Column; bit 16 (formerly labeled rasn for POWER8).

Bits	SCOM	Field Mnemonic: Description
22	RW	CCS_INST_ARR0_07_CCS_DDR_ADDRESS_15: DDR Address Row Column; bit 15 (formerly labeled casn for POWER8).
23	RW	CCS_INST_ARR0_07_CCS_DDR_ADDRESS_14: DDR Address Row Column; bit 14 (formerly labeled wen for POWER8).
24:27	RW	CCS_INST_ARR0_07_CCS_DDR_CKE: DDR CKE. ccs_ddr_cke[0:1] → CKE[0:1] (also CKE[2:3] when CKEs copied enabled). ccs_ddr_cke[2:3] → CKE[4:5] (also CKE[6:7] when CKEs copied enabled).
28:31	RW	CCS_INST_ARR0_07_RESERVED_28_31: Reserved.
32:33	RW	CCS_INST_ARR0_07_CCS_DDR_CSN_0_1: DDR CSN Chip Select Not; bits 0:1.
34:35	RW	CCS_INST_ARR0_07_CCS_DDR_CID_0_1: DDR CID Chip ID; bits 0:1.
36:37	RW	CCS_INST_ARR0_07_CCS_DDR_CSN_2_3: DDR CSN Chip Select Not; bits 2:3.
38	RW	CCS_INST_ARR0_07_CCS_DDR_CID_2: DDR CID Chip ID; bit 2.
39:47	RW	CCS_INST_ARR0_07_RESERVED_39_47: Reserved.
48:51	RW	CCS_INST_ARR0_07_CCS_DDR_ODT: DDR ODT.
52:55	RW	CCS_INST_ARR0_07_RESERVED_52_55: Reserved.
56:59	RW	CCS_INST_ARR0_07_CCS_DDR_CAL_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the subtype. 0123 11XX = Initial calibration. Performs all of the following steps that are enabled via the configuration register: • SysclkRdclk alignment • DQS alignment • Read eye MPR centering • Write leveling • Write centering • Coarse rdwr alignment • Read eye custom pattern centering 10XX = Internal ZQ calibration (cal_rank is ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step.
60	RW	CCS_INST_ARR0_07_CCS_DDR_PARITY: DDR Parity. Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61	RW	CCS_INST_ARR0_07_CCS_DDR_BANK_2: DDR Address Bank; bit 2 (new for POWER9 DDR4E).
62:63	RW	CCS_INST_ARR0_07_CCS_LOOP_BREAK_MODE: Selects which programmable iteration value to compare to in order to break out of the loop. 00 = Never break out of the loop. 01 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare0. 10 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare1. 11 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare2. **Note**: This is now held in local latches instead of the array for earlier access.

Register Name	CCS INST ARR0 08 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR0_08
Address	000000000701231D (SCOM)
Description	CCS INST ARR0 08

Bits	SCOM	Field Mnemonic: Description
0:13	RW	CCS_INST_ARR0_08_CCS_DDR_ADDRESS_0_13: DDR Address Row Column; bits 0:13.
14	RW	CCS_INST_ARR0_08_CCS_DDR_ADDRESS_17: DDR Address Row Column; bit 17 (formerly labeled address(14) for POWER8).
15	RW	CCS_INST_ARR0_08_CCS_DDR_BANK_GROUP_1: DDR Address Bank Group; bit 1 (formerly labeled address(15) for POWER8).
16	RW	CCS_INST_ARR0_08_CCS_DDR_RESETN: DDR Resetn. Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq[24] controls the value of DDR Resetn.
17:18	RW	CCS_INST_ARR0_08_CCS_DDR_BANK_0_1: DDR Address Bank; bits 0:1.
19	RW	CCS_INST_ARR0_08_CCS_DDR_BANK_GROUP_0: DDR Address Bank Group; bit 0 (formerly labeled bank(2) for POWER8).
20	RW	CCS_INST_ARR0_08_CCS_DDR_ACTN: DDR Activate Not (formerly labeled Active although functionally equivalent for POWER8).
21	RW	CCS_INST_ARR0_08_CCS_DDR_ADDRESS_16: DDR Address Row Column; bit 16 (formerly labeled rasn for POWER8).
22	RW	CCS_INST_ARR0_08_CCS_DDR_ADDRESS_15: DDR Address Row Column; bit 15 (formerly labeled casn for POWER8).
23	RW	CCS_INST_ARR0_08_CCS_DDR_ADDRESS_14: DDR Address Row Column; bit 14 (formerly labeled wen for POWER8).
24:27	RW	CCS_INST_ARR0_08_CCS_DDR_CKE: DDR CKE. ccs_ddr_cke[0:1] → CKE[0:1] (also CKE[2:3] when CKEs copied enabled). ccs_ddr_cke[2:3] → CKE[4:5] (also CKE[6:7] when CKEs copied enabled).
28:31	RW	CCS_INST_ARR0_08_RESERVED_28_31: Reserved.
32:33	RW	CCS_INST_ARR0_08_CCS_DDR_CSN_0_1: DDR CSN Chip Select Not; bits 0:1.
34:35	RW	CCS_INST_ARR0_08_CCS_DDR_CID_0_1: DDR CID Chip ID; bits 0:1.
36:37	RW	CCS_INST_ARR0_08_CCS_DDR_CSN_2_3: DDR CSN Chip Select Not; bits 2:3.
38	RW	CCS_INST_ARR0_08_CCS_DDR_CID_2: DDR CID Chip ID; bit 2.
39:47	RW	CCS_INST_ARR0_08_RESERVED_39_47: Reserved.
48:51	RW	CCS_INST_ARR0_08_CCS_DDR_ODT: DDR ODT.
52:55	RW	CCS_INST_ARR0_08_RESERVED_52_55: Reserved.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	CCS_INST_ARR0_08_CCS_DDR_CAL_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the subtype. 0123 11XX = Initial calibration. Performs all of the following steps that are enabled via the configuration register: • SysclkRdclk alignment • DQS alignment • Read eye MPR centering • Write leveling • Write centering • Coarse rdwr alignment • Read eye custom pattern centering 10XX = Internal ZQ calibration (cal_rank is ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step.
60	RW	CCS_INST_ARR0_08_CCS_DDR_PARITY: DDR Parity. Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61	RW	CCS_INST_ARR0_08_CCS_DDR_BANK_2: DDR Address Bank; bit 2 (new for POWER9 DDR4E).
62:63	RW	CCS_INST_ARR0_08_CCS_LOOP_BREAK_MODE: Selects which programmable iteration value to compare to in order to break out of the loop. 00 = Never break out of the loop. 01 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare0. 10 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare1. 11 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare2. **Note**: This is now held in local latches instead of the array for earlier access.

Register Name	CCS INST ARR0 09 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR0_09
Address	000000000701231E (SCOM)
Description	CCS INST ARR0 09

Bits	SCOM	Field Mnemonic: Description
0:13	RW	CCS_INST_ARR0_09_CCS_DDR_ADDRESS_0_13: DDR Address Row Column; bits 0:13.
14	RW	CCS_INST_ARR0_09_CCS_DDR_ADDRESS_17: DDR Address Row Column; bit 17 (formerly labeled address(14) for POWER8).
15	RW	CCS_INST_ARR0_09_CCS_DDR_BANK_GROUP_1: DDR Address Bank Group; bit 1 (formerly labeled address(15) for POWER8).
16	RW	CCS_INST_ARR0_09_CCS_DDR_RESETN: DDR Resetn. Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq[24] controls the value of DDR Resetn.
17:18	RW	CCS_INST_ARR0_09_CCS_DDR_BANK_0_1: DDR Address Bank; bits 0:1.
19	RW	CCS_INST_ARR0_09_CCS_DDR_BANK_GROUP_0: DDR Address Bank Group; bit 0 (formerly labeled bank(2) for POWER8).
20	RW	CCS_INST_ARR0_09_CCS_DDR_ACTN: DDR Activate Not (formerly labeled Active although functionally equivalent for POWER8).
21	RW	CCS_INST_ARR0_09_CCS_DDR_ADDRESS_16: DDR Address Row Column; bit 16 (formerly labeled rasn for POWER8).

Bits	SCOM	Field Mnemonic: Description
22	RW	CCS_INST_ARR0_09_CCS_DDR_ADDRESS_15: DDR Address Row Column; bit 15 (formerly labeled casn for POWER8).
23	RW	CCS_INST_ARR0_09_CCS_DDR_ADDRESS_14: DDR Address Row Column; bit 14 (formerly labeled wen for POWER8).
24:27	RW	CCS_INST_ARR0_09_CCS_DDR_CKE: DDR CKE. ccs_ddr_cke[0:1] → CKE[0:1] (also CKE[2:3] when CKEs copied enabled). ccs_ddr_cke[2:3] → CKE[4:5] (also CKE[6:7] when CKEs copied enabled).
28:31	RW	CCS_INST_ARR0_09_RESERVED_28_31: Reserved.
32:33	RW	CCS_INST_ARR0_09_CCS_DDR_CSN_0_1: DDR CSN Chip Select Not; bits 0:1.
34:35	RW	CCS_INST_ARR0_09_CCS_DDR_CID_0_1: DDR CID Chip ID; bits 0:1.
36:37	RW	CCS_INST_ARR0_09_CCS_DDR_CSN_2_3: DDR CSN Chip Select Not; bits 2:3.
38	RW	CCS_INST_ARR0_09_CCS_DDR_CID_2: DDR CID Chip ID; bit 2.
39:47	RW	CCS_INST_ARR0_09_RESERVED_39_47: Reserved.
48:51	RW	CCS_INST_ARR0_09_CCS_DDR_ODT: DDR ODT.
52:55	RW	CCS_INST_ARR0_09_RESERVED_52_55: Reserved.
56:59	RW	CCS_INST_ARR0_09_CCS_DDR_CAL_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the subtype. 0123 11XX = Initial calibration. Performs all of the following steps that are enabled via the configuration register: • SysclkRdclk alignment • DQS alignment • Read eye MPR centering • Write leveling • Write centering • Coarse rdwr alignment • Read eye custom pattern centering 10XX = Internal ZQ calibration (cal_rank is ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step.
60	RW	CCS_INST_ARR0_09_CCS_DDR_PARITY: DDR Parity. Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61	RW	CCS_INST_ARR0_09_CCS_DDR_BANK_2: DDR Address Bank; bit 2 (new for POWER9 DDR4E).
62:63	RW	CCS_INST_ARR0_09_CCS_LOOP_BREAK_MODE: Selects which programmable iteration value to compare to in order to break out of the loop. 00 = Never break out of the loop. 01 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare0. 10 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare1. 11 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare2. **Note**: This is now held in local latches instead of the array for earlier access.

Register Name	CCS INST ARR0 10 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR0_10
Address	000000000701231F (SCOM)
Description	CCS INST ARR0 10

Bits	SCOM	Field Mnemonic: Description
0:13	RW	CCS_INST_ARR0_10_CCS_DDR_ADDRESS_0_13: DDR Address Row Column; bits 0:13.
14	RW	CCS_INST_ARR0_10_CCS_DDR_ADDRESS_17: DDR Address Row Column; bit 17 (formerly labeled address(14) for POWER8).
15	RW	CCS_INST_ARR0_10_CCS_DDR_BANK_GROUP_1: DDR Address Bank Group; bit 1 (formerly labeled address(15) for POWER8).
16	RW	CCS_INST_ARR0_10_CCS_DDR_RESETN: DDR Resetn. Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq[24] controls the value of DDR Resetn.
17:18	RW	CCS_INST_ARR0_10_CCS_DDR_BANK_0_1: DDR Address Bank; bits 0:1.
19	RW	CCS_INST_ARR0_10_CCS_DDR_BANK_GROUP_0: DDR Address Bank Group; bit 0 (formerly labeled bank(2) for POWER8).
20	RW	CCS_INST_ARR0_10_CCS_DDR_ACTN: DDR Activate Not (formerly labeled Active although functionally equivalent for POWER8).
21	RW	CCS_INST_ARR0_10_CCS_DDR_ADDRESS_16: DDR Address Row Column; bit 16 (formerly labeled rasn for POWER8).
22	RW	CCS_INST_ARR0_10_CCS_DDR_ADDRESS_15: DDR Address Row Column; bit 15 (formerly labeled casn for POWER8).
23	RW	CCS_INST_ARR0_10_CCS_DDR_ADDRESS_14: DDR Address Row Column; bit 14 (formerly labeled wen for POWER8).
24:27	RW	CCS_INST_ARR0_10_CCS_DDR_CKE: DDR CKE. ccs_ddr_cke[0:1] → CKE[0:1] (also CKE[2:3] when CKEs copied enabled). ccs_ddr_cke[2:3] → CKE[4:5] (also CKE[6:7] when CKEs copied enabled).
28:31	RW	CCS_INST_ARR0_10_RESERVED_28_31: Reserved.
32:33	RW	CCS_INST_ARR0_10_CCS_DDR_CSN_0_1: DDR CSN Chip Select Not; bits 0:1.
34:35	RW	CCS_INST_ARR0_10_CCS_DDR_CID_0_1: DDR CID Chip ID; bits 0:1.
36:37	RW	CCS_INST_ARR0_10_CCS_DDR_CSN_2_3: DDR CSN Chip Select Not; bits 2:3.
38	RW	CCS_INST_ARR0_10_CCS_DDR_CID_2: DDR CID Chip ID; bit 2.
39:47	RW	CCS_INST_ARR0_10_RESERVED_39_47: Reserved.
48:51	RW	CCS_INST_ARR0_10_CCS_DDR_ODT: DDR ODT.
52:55	RW	CCS_INST_ARR0_10_RESERVED_52_55: Reserved.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	CCS_INST_ARR0_10_CCS_DDR_CAL_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the subtype. 0123 11XX = Initial calibration. Performs all of the following steps that are enabled via the configuration register: • SysclkRdclk alignment • DQS alignment • Read eye MPR centering • Write leveling • Write centering • Coarse rdwr alignment • Read eye custom pattern centering 10XX = Internal ZQ calibration (cal_rank is ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step.
60	RW	CCS_INST_ARR0_10_CCS_DDR_PARITY: DDR Parity. Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61	RW	CCS_INST_ARR0_10_CCS_DDR_BANK_2: DDR Address Bank; bit 2 (new for POWER9 DDR4E).
62:63	RW	CCS_INST_ARR0_10_CCS_LOOP_BREAK_MODE: Selects which programmable iteration value to compare to in order to break out of the loop. 00 = Never break out of the loop. 01 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare0. 10 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare1. 11 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare2. **Note**: This is now held in local latches instead of the array for earlier access.

Register Name	CCS INST ARR0 11 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR0_11
Address	0000000007012320 (SCOM)
Description	CCS INST ARR0 11

Bits	SCOM	Field Mnemonic: Description
0:13	RW	CCS_INST_ARR0_11_CCS_DDR_ADDRESS_0_13: DDR Address Row Column; bits 0:13.
14	RW	CCS_INST_ARR0_11_CCS_DDR_ADDRESS_17: DDR Address Row Column; bit 17 (formerly labeled address(14) for POWER8).
15	RW	CCS_INST_ARR0_11_CCS_DDR_BANK_GROUP_1: DDR Address Bank Group; bit 1 (formerly labeled address(15) for POWER8).
16	RW	CCS_INST_ARR0_11_CCS_DDR_RESETN: DDR Resetn. Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq[24] controls the value of DDR Resetn.
17:18	RW	CCS_INST_ARR0_11_CCS_DDR_BANK_0_1: DDR Address Bank; bits 0:1.
19	RW	CCS_INST_ARR0_11_CCS_DDR_BANK_GROUP_0: DDR Address Bank Group; bit 0 (formerly labeled bank(2) for POWER8).
20	RW	CCS_INST_ARR0_11_CCS_DDR_ACTN: DDR Activate Not (formerly labeled Active although functionally equivalent for POWER8).
21	RW	CCS_INST_ARR0_11_CCS_DDR_ADDRESS_16: DDR Address Row Column; bit 16 (formerly labeled rasn for POWER8).

Bits	SCOM	Field Mnemonic: Description
22	RW	CCS_INST_ARR0_11_CCS_DDR_ADDRESS_15: DDR Address Row Column; bit 15 (formerly labeled casn for POWER8).
23	RW	CCS_INST_ARR0_11_CCS_DDR_ADDRESS_14: DDR Address Row Column; bit 14 (formerly labeled wen for POWER8).
24:27	RW	CCS_INST_ARR0_11_CCS_DDR_CKE: DDR CKE. ccs_ddr_cke[0:1] → CKE[0:1] (also CKE[2:3] when CKEs copied enabled). ccs_ddr_cke[2:3] → CKE[4:5] (also CKE[6:7] when CKEs copied enabled).
28:31	RW	CCS_INST_ARR0_11_RESERVED_28_31: Reserved.
32:33	RW	CCS_INST_ARR0_11_CCS_DDR_CSN_0_1: DDR CSN Chip Select Not; bits 0:1.
34:35	RW	CCS_INST_ARR0_11_CCS_DDR_CID_0_1: DDR CID Chip ID; bits 0:1.
36:37	RW	CCS_INST_ARR0_11_CCS_DDR_CSN_2_3: DDR CSN Chip Select Not; bits 2:3.
38	RW	CCS_INST_ARR0_11_CCS_DDR_CID_2: DDR CID Chip ID; bit 2.
39:47	RW	CCS_INST_ARR0_11_RESERVED_39_47: Reserved.
48:51	RW	CCS_INST_ARR0_11_CCS_DDR_ODT: DDR ODT.
52:55	RW	CCS_INST_ARR0_11_RESERVED_52_55: Reserved.
56:59	RW	CCS_INST_ARR0_11_CCS_DDR_CAL_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the subtype. 0123 11XX = Initial calibration. Performs all of the following steps that are enabled via the configuration register: • SysclkRdclk alignment • DQS alignment • Read eye MPR centering • Write leveling • Write centering • Coarse rdwr alignment • Read eye custom pattern centering 10XX = Internal ZQ calibration (cal_rank is ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step.
60	RW	CCS_INST_ARR0_11_CCS_DDR_PARITY: DDR Parity. Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61	RW	CCS_INST_ARR0_11_CCS_DDR_BANK_2: DDR Address Bank; bit 2 (new for POWER9 DDR4E).
62:63	RW	CCS_INST_ARR0_11_CCS_LOOP_BREAK_MODE: Selects which programmable iteration value to compare to in order to break out of the loop. 00 = Never break out of the loop. 01 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare0. 10 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare1. 11 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare2. **Note**: This is now held in local latches instead of the array for earlier access.

Register Name	CCS INST ARR0 12 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR0_12
Address	0000000007012321 (SCOM)
Description	CCS INST ARR0 12

Bits	SCOM	Field Mnemonic: Description
0:13	RW	CCS_INST_ARR0_12_CCS_DDR_ADDRESS_0_13: DDR Address Row Column; bits 0:13.
14	RW	CCS_INST_ARR0_12_CCS_DDR_ADDRESS_17: DDR Address Row Column; bit 17 (formerly labeled address(14) for POWER8).
15	RW	CCS_INST_ARR0_12_CCS_DDR_BANK_GROUP_1: DDR Address Bank Group; bit 1 (formerly labeled address(15) for POWER8).
16	RW	CCS_INST_ARR0_12_CCS_DDR_RESETN: DDR Resetn. Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq[24] controls the value of DDR Resetn.
17:18	RW	CCS_INST_ARR0_12_CCS_DDR_BANK_0_1: DDR Address Bank; bits 0:1.
19	RW	CCS_INST_ARR0_12_CCS_DDR_BANK_GROUP_0: DDR Address Bank Group; bit 0 (formerly labeled bank(2) for POWER8).
20	RW	CCS_INST_ARR0_12_CCS_DDR_ACTN: DDR Activate Not (formerly labeled Active although functionally equivalent for POWER8).
21	RW	CCS_INST_ARR0_12_CCS_DDR_ADDRESS_16: DDR Address Row Column; bit 16 (formerly labeled rasn for POWER8).
22	RW	CCS_INST_ARR0_12_CCS_DDR_ADDRESS_15: DDR Address Row Column; bit 15 (formerly labeled casn for POWER8).
23	RW	CCS_INST_ARR0_12_CCS_DDR_ADDRESS_14: DDR Address Row Column; bit 14 (formerly labeled wen for POWER8).
24:27	RW	CCS_INST_ARR0_12_CCS_DDR_CKE: DDR CKE. ccs_ddr_cke[0:1] → CKE[0:1] (also CKE[2:3] when CKEs copied enabled). ccs_ddr_cke[2:3] → CKE[4:5] (also CKE[6:7] when CKEs copied enabled).
28:31	RW	CCS_INST_ARR0_12_RESERVED_28_31: Reserved.
32:33	RW	CCS_INST_ARR0_12_CCS_DDR_CSN_0_1: DDR CSN Chip Select Not; bits 0:1.
34:35	RW	CCS_INST_ARR0_12_CCS_DDR_CID_0_1: DDR CID Chip ID; bits 0:1.
36:37	RW	CCS_INST_ARR0_12_CCS_DDR_CSN_2_3: DDR CSN Chip Select Not; bits 2:3.
38	RW	CCS_INST_ARR0_12_CCS_DDR_CID_2: DDR CID Chip ID; bit 2.
39:47	RW	CCS_INST_ARR0_12_RESERVED_39_47: Reserved.
48:51	RW	CCS_INST_ARR0_12_CCS_DDR_ODT: DDR ODT.
52:55	RW	CCS_INST_ARR0_12_RESERVED_52_55: Reserved.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	CCS_INST_ARR0_12_CCS_DDR_CAL_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the subtype. 0123 11XX = Initial calibration. Performs all of the following steps that are enabled via the configuration register: • SysclkRdclk alignment • DQS alignment • Read eye MPR centering • Write leveling • Write centering • Coarse rdwr alignment • Read eye custom pattern centering 10XX = Internal ZQ calibration (cal_rank is ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step.
60	RW	CCS_INST_ARR0_12_CCS_DDR_PARITY: DDR Parity. Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61	RW	CCS_INST_ARR0_12_CCS_DDR_BANK_2: DDR Address Bank; bit 2 (new for POWER9 DDR4E).
62:63	RW	CCS_INST_ARR0_12_CCS_LOOP_BREAK_MODE: Selects which programmable iteration value to compare to in order to break out of the loop. 00 = Never break out of the loop. 01 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare0. 10 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare1. 11 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare2. **Note**: This is now held in local latches instead of the array for earlier access.

Register Name	CCS INST ARR0 13 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR0_13
Address	0000000007012322 (SCOM)
Description	ccs inst arr0 13

Bits	SCOM	Field Mnemonic: Description
0:13	RW	CCS_INST_ARR0_13_CCS_DDR_ADDRESS_0_13: DDR Address Row Column; bits 0:13.
14	RW	CCS_INST_ARR0_13_CCS_DDR_ADDRESS_17: DDR Address Row Column; bit 17 (formerly labeled address(14) for POWER8).
15	RW	CCS_INST_ARR0_13_CCS_DDR_BANK_GROUP_1: DDR Address Bank Group; bit 1 (formerly labeled address(15) for POWER8).
16	RW	CCS_INST_ARR0_13_CCS_DDR_RESETN: DDR Resetn. Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq[24] controls the value of DDR Resetn.
17:18	RW	CCS_INST_ARR0_13_CCS_DDR_BANK_0_1: DDR Address Bank; bits 0:1.
19	RW	CCS_INST_ARR0_13_CCS_DDR_BANK_GROUP_0: DDR Address Bank Group; bit 0 (formerly labeled bank(2) for POWER8).
20	RW	CCS_INST_ARR0_13_CCS_DDR_ACTN: DDR Activate Not (formerly labeled Active although functionally equivalent for POWER8).
21	RW	CCS_INST_ARR0_13_CCS_DDR_ADDRESS_16: DDR Address Row Column; bit 16 (formerly labeled rasn for POWER8).

Bits	SCOM	Field Mnemonic: Description
22	RW	CCS_INST_ARR0_13_CCS_DDR_ADDRESS_15: DDR Address Row Column; bit 15 (formerly labeled casn for POWER8).
23	RW	CCS_INST_ARR0_13_CCS_DDR_ADDRESS_14: DDR Address Row Column; bit 14 (formerly labeled wen for POWER8).
24:27	RW	CCS_INST_ARR0_13_CCS_DDR_CKE: DDR CKE. ccs_ddr_cke[0:1] → CKE[0:1] (also CKE[2:3] when CKEs copied enabled). ccs_ddr_cke[2:3] → CKE[4:5] (also CKE[6:7] when CKEs copied enabled).
28:31	RW	CCS_INST_ARR0_13_RESERVED_28_31: Reserved.
32:33	RW	CCS_INST_ARR0_13_CCS_DDR_CSN_0_1: DDR CSN Chip Select Not; bits 0:1.
34:35	RW	CCS_INST_ARR0_13_CCS_DDR_CID_0_1: DDR CID Chip ID; bits 0:1.
36:37	RW	CCS_INST_ARR0_13_CCS_DDR_CSN_2_3: DDR CSN Chip Select Not; bits 2:3.
38	RW	CCS_INST_ARR0_13_CCS_DDR_CID_2: DDR CID Chip ID; bit 2.
39:47	RW	CCS_INST_ARR0_13_RESERVED_39_47: Reserved.
48:51	RW	CCS_INST_ARR0_13_CCS_DDR_ODT: DDR ODT.
52:55	RW	CCS_INST_ARR0_13_RESERVED_52_55: Reserved.
56:59	RW	CCS_INST_ARR0_13_CCS_DDR_CAL_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the subtype. 0123 11XX = Initial calibration. Performs all of the following steps that are enabled via the configuration register: • SysclkRdclk alignment • DQS alignment • Read eye MPR centering • Write leveling • Write centering • Coarse rdwr alignment • Read eye custom pattern centering 10XX = Internal ZQ calibration (cal_rank is ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step.
60	RW	CCS_INST_ARR0_13_CCS_DDR_PARITY: DDR Parity. Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61	RW	CCS_INST_ARR0_13_CCS_DDR_BANK_2: DDR Address Bank; bit 2 (new for POWER9 DDR4E).
62:63	RW	CCS_INST_ARR0_13_CCS_LOOP_BREAK_MODE: Selects which programmable iteration value to compare to in order to break out of the loop. 00 = Never break out of the loop. 01 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare0. 10 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare1. 11 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare2. **Note**: This is now held in local latches instead of the array for earlier access.

Register Name	CCS INST ARR0 14 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR0_14
Address	0000000007012323 (SCOM)
Description	CCS INST ARR0 14

Bits	SCOM	Field Mnemonic: Description
0:13	RW	CCS_INST_ARR0_14_CCS_DDR_ADDRESS_0_13: DDR Address Row Column; bits 0:13.
14	RW	CCS_INST_ARR0_14_CCS_DDR_ADDRESS_17: DDR Address Row Column; bit 17 (formerly labeled address(14) for POWER8).
15	RW	CCS_INST_ARR0_14_CCS_DDR_BANK_GROUP_1: DDR Address Bank Group; bit 1 (formerly labeled address(15) for POWER8).
16	RW	CCS_INST_ARR0_14_CCS_DDR_RESETN: DDR Resetn. Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq[24] controls the value of DDR Resetn.
17:18	RW	CCS_INST_ARR0_14_CCS_DDR_BANK_0_1: DDR Address Bank; bits 0:1.
19	RW	CCS_INST_ARR0_14_CCS_DDR_BANK_GROUP_0: DDR Address Bank Group; bit 0 (formerly labeled bank(2) for POWER8).
20	RW	CCS_INST_ARR0_14_CCS_DDR_ACTN: DDR Activate Not (formerly labeled Active although functionally equivalent for POWER8).
21	RW	CCS_INST_ARR0_14_CCS_DDR_ADDRESS_16: DDR Address Row Column; bit 16 (formerly labeled rasn for POWER8).
22	RW	CCS_INST_ARR0_14_CCS_DDR_ADDRESS_15: DDR Address Row Column; bit 15 (formerly labeled casn for POWER8).
23	RW	CCS_INST_ARR0_14_CCS_DDR_ADDRESS_14: DDR Address Row Column; bit 14 (formerly labeled wen for POWER8).
24:27	RW	CCS_INST_ARR0_14_CCS_DDR_CKE: DDR CKE. ccs_ddr_cke[0:1] → CKE[0:1] (also CKE[2:3] when CKEs copied enabled). ccs_ddr_cke[2:3] → CKE[4:5] (also CKE[6:7] when CKEs copied enabled).
28:31	RW	CCS_INST_ARR0_14_RESERVED_28_31: Reserved.
32:33	RW	CCS_INST_ARR0_14_CCS_DDR_CSN_0_1: DDR CSN Chip Select Not; bits 0:1.
34:35	RW	CCS_INST_ARR0_14_CCS_DDR_CID_0_1: DDR CID Chip ID; bits 0:1.
36:37	RW	CCS_INST_ARR0_14_CCS_DDR_CSN_2_3: DDR CSN Chip Select Not; bits 2:3.
38	RW	CCS_INST_ARR0_14_CCS_DDR_CID_2: DDR CID Chip ID; bit 2.
39:47	RW	CCS_INST_ARR0_14_RESERVED_39_47: Reserved.
48:51	RW	CCS_INST_ARR0_14_CCS_DDR_ODT: DDR ODT.
52:55	RW	CCS_INST_ARR0_14_RESERVED_52_55: Reserved.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	CCS_INST_ARR0_14_CCS_DDR_CAL_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the subtype. 0123 11XX = Initial calibration. Performs all of the following steps that are enabled via the configuration register: • SysclkRdclk alignment • DQS alignment • Read eye MPR centering • Write leveling • Write centering • Coarse rdwr alignment • Read eye custom pattern centering 10XX = Internal ZQ calibration (cal_rank is ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step.
60	RW	CCS_INST_ARR0_14_CCS_DDR_PARITY: DDR Parity. Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61	RW	CCS_INST_ARR0_14_CCS_DDR_BANK_2: DDR Address Bank; bit 2 (new for POWER9 DDR4E)
62:63	RW	CCS_INST_ARR0_14_CCS_LOOP_BREAK_MODE: Selects which programmable iteration value to compare to in order to break out of the loop. 00 = Never break out of the loop. 01 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare0. 10 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare1. 11 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare2. **Note**: This is now held in local latches instead of the array for earlier access.

Register Name	CCS INST ARR0 15 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR0_15
Address	0000000007012324 (SCOM)
Description	CCS INST ARR0 15

Bits	SCOM	Field Mnemonic: Description
0:13	RW	CCS_INST_ARR0_15_CCS_DDR_ADDRESS_0_13: DDR Address Row Column; bits 0:13.
14	RW	CCS_INST_ARR0_15_CCS_DDR_ADDRESS_17: DDR Address Row Column; bit 17 (formerly labeled address(14) for POWER8).
15	RW	CCS_INST_ARR0_15_CCS_DDR_BANK_GROUP_1: DDR Address Bank Group; bit 1 (formerly labeled address(15) for POWER8).
16	RW	CCS_INST_ARR0_15_CCS_DDR_RESETN: DDR Resetn. Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq[24] controls the value of DDR Resetn.
17:18	RW	CCS_INST_ARR0_15_CCS_DDR_BANK_0_1: DDR Address Bank; bits 0:1.
19	RW	CCS_INST_ARR0_15_CCS_DDR_BANK_GROUP_0: DDR Address Bank Group; bit 0 (formerly labeled bank(2) for POWER8).
20	RW	CCS_INST_ARR0_15_CCS_DDR_ACTN: DDR Activate Not (formerly labeled Active although functionally equivalent for POWER8).
21	RW	CCS_INST_ARR0_15_CCS_DDR_ADDRESS_16: DDR Address Row Column; bit 16 (formerly labeled rasn for POWER8).

Bits	SCOM	Field Mnemonic: Description
22	RW	CCS_INST_ARR0_15_CCS_DDR_ADDRESS_15: DDR Address Row Column; bit 15 (formerly labeled casn for POWER8).
23	RW	CCS_INST_ARR0_15_CCS_DDR_ADDRESS_14: DDR Address Row Column; bit 14 (formerly labeled wen for POWER8).
24:27	RW	CCS_INST_ARR0_15_CCS_DDR_CKE: DDR CKE. ccs_ddr_cke[0:1] → CKE[0:1] (also CKE[2:3] when CKEs copied enabled). ccs_ddr_cke[2:3] → CKE[4:5] (also CKE[6:7] when CKEs copied enabled).
28:31	RW	CCS_INST_ARR0_15_RESERVED_28_31: Reserved.
32:33	RW	CCS_INST_ARR0_15_CCS_DDR_CSN_0_1: DDR CSN Chip Select Not; bits 0:1.
34:35	RW	CCS_INST_ARR0_15_CCS_DDR_CID_0_1: DDR CID Chip ID; bits 0:1.
36:37	RW	CCS_INST_ARR0_15_CCS_DDR_CSN_2_3: DDR CSN Chip Select Not; bits 2:3.
38	RW	CCS_INST_ARR0_15_CCS_DDR_CID_2: DDR CID Chip ID; bit 2.
39:47	RW	CCS_INST_ARR0_15_RESERVED_39_47: Reserved.
48:51	RW	CCS_INST_ARR0_15_CCS_DDR_ODT: DDR ODT.
52:55	RW	CCS_INST_ARR0_15_RESERVED_52_55: Reserved.
56:59	RW	CCS_INST_ARR0_15_CCS_DDR_CAL_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the subtype. 0123 11XX = Initial calibration. Performs all of the following steps that are enabled via the configuration register: • SysclkRdclk alignment • DQS alignment • Read eye MPR centering • Write leveling • Write centering • Coarse rdwr alignment • Read eye custom pattern centering 10XX = Internal ZQ calibration (cal_rank is ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step.
60	RW	CCS_INST_ARR0_15_CCS_DDR_PARITY: DDR Parity. Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61	RW	CCS_INST_ARR0_15_CCS_DDR_BANK_2: DDR Address Bank; bit 2 (new for POWER9 DDR4E).
62:63	RW	CCS_INST_ARR0_15_CCS_LOOP_BREAK_MODE: Selects which programmable iteration value to compare to in order to break out of the loop. 00 = Never break out of the loop. 01 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare0. 10 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare1. 11 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare2. **Note**: This is now held in local latches instead of the array for earlier access.

Register Name	CCS INST ARR0 16 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR0_16
Address	0000000007012325 (SCOM)
Description	ccs inst arr0 16

Bits	SCOM	Field Mnemonic: Description
0:13	RW	CCS_INST_ARR0_16_CCS_DDR_ADDRESS_0_13: DDR Address Row Column; bits 0:13.
14	RW	CCS_INST_ARR0_16_CCS_DDR_ADDRESS_17: DDR Address Row Column; bit 17 (formerly labeled address(14) for POWER8).
15	RW	CCS_INST_ARR0_16_CCS_DDR_BANK_GROUP_1: DDR Address Bank Group; bit 1 (formerly labeled address(15) for POWER8).
16	RW	CCS_INST_ARR0_16_CCS_DDR_RESETN: DDR Resetn. Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq[24] controls the value of DDR Resetn.
17:18	RW	CCS_INST_ARR0_16_CCS_DDR_BANK_0_1: DDR Address Bank; bits 0:1.
19	RW	CCS_INST_ARR0_16_CCS_DDR_BANK_GROUP_0: DDR Address Bank Group; bit 0 (formerly labeled bank(2) for POWER8).
20	RW	CCS_INST_ARR0_16_CCS_DDR_ACTN: DDR Activate Not (formerly labeled Active although functionally equivalent for POWER8).
21	RW	CCS_INST_ARR0_16_CCS_DDR_ADDRESS_16: DDR Address Row Column; bit 16 (formerly labeled rasn for POWER8).
22	RW	CCS_INST_ARR0_16_CCS_DDR_ADDRESS_15: DDR Address Row Column; bit 15 (formerly labeled casn for POWER8).
23	RW	CCS_INST_ARR0_16_CCS_DDR_ADDRESS_14: DDR Address Row Column; bit 14 (formerly labeled wen for POWER8).
24:27	RW	CCS_INST_ARR0_16_CCS_DDR_CKE: DDR CKE. ccs_ddr_cke[0:1] → CKE[0:1] (also CKE[2:3] when CKEs copied enabled). ccs_ddr_cke[2:3] → CKE[4:5] (also CKE[6:7] when CKEs copied enabled).
28:31	RW	CCS_INST_ARR0_16_RESERVED_28_31: Reserved.
32:33	RW	CCS_INST_ARR0_16_CCS_DDR_CSN_0_1: DDR CSN Chip Select Not; bits 0:1.
34:35	RW	CCS_INST_ARR0_16_CCS_DDR_CID_0_1: DDR CID Chip ID; bits 0:1.
36:37	RW	CCS_INST_ARR0_16_CCS_DDR_CSN_2_3: DDR CSN Chip Select Not; bits 2:3.
38	RW	CCS_INST_ARR0_16_CCS_DDR_CID_2: DDR CID Chip ID; bit 2.
39:47	RW	CCS_INST_ARR0_16_RESERVED_39_47: Reserved.
48:51	RW	CCS_INST_ARR0_16_CCS_DDR_ODT: DDR ODT.
52:55	RW	CCS_INST_ARR0_16_RESERVED_52_55: Reserved.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	CCS_INST_ARR0_16_CCS_DDR_CAL_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the subtype. 0123 11XX = Initial calibration. Performs all of the following steps that are enabled via the configuration register: • SysclkRdclk alignment • DQS alignment • Read eye MPR centering • Write leveling • Write centering • Coarse rdwr alignment • Read eye custom pattern centering 10XX = Internal ZQ calibration (cal_rank is ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step.
60	RW	CCS_INST_ARR0_16_CCS_DDR_PARITY: DDR Parity. Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61	RW	CCS_INST_ARR0_16_CCS_DDR_BANK_2: DDR Address Bank; bit 2 (new for POWER9 DDR4E).
62:63	RW	CCS_INST_ARR0_16_CCS_LOOP_BREAK_MODE: Selects which programmable iteration value to compare to in order to break out of the loop. 00 = Never break out of the loop. 01 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare0. 10 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare1. 11 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare2. **Note**: This is now held in local latches instead of the array for earlier access.

Register Name	CCS INST ARR0 17 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR0_17
Address	0000000007012326 (SCOM)
Description	ccs inst arr0 17

Bits	SCOM	Field Mnemonic: Description
0:13	RW	CCS_INST_ARR0_17_CCS_DDR_ADDRESS_0_13: DDR Address Row Column; bits 0:13.
14	RW	CCS_INST_ARR0_17_CCS_DDR_ADDRESS_17: DDR Address Row Column; bit 17 (formerly labeled address(14) for POWER8).
15	RW	CCS_INST_ARR0_17_CCS_DDR_BANK_GROUP_1: DDR Address Bank Group; bit 1 (formerly labeled address(15) for POWER8).
16	RW	CCS_INST_ARR0_17_CCS_DDR_RESETN: DDR Resetn. Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq[24] controls the value of DDR Resetn.
17:18	RW	CCS_INST_ARR0_17_CCS_DDR_BANK_0_1: DDR Address Bank; bits 0:1.
19	RW	CCS_INST_ARR0_17_CCS_DDR_BANK_GROUP_0: DDR Address Bank Group; bit 0 (formerly labeled bank(2) for POWER8).
20	RW	CCS_INST_ARR0_17_CCS_DDR_ACTN: DDR Activate Not (formerly labeled Active although functionally equivalent for POWER8).
21	RW	CCS_INST_ARR0_17_CCS_DDR_ADDRESS_16: DDR Address Row Column; bit 16 (formerly labeled rasn for POWER8).

Bits	SCOM	Field Mnemonic: Description
22	RW	CCS_INST_ARR0_17_CCS_DDR_ADDRESS_15: DDR Address Row Column; bit 15 (formerly labeled casn for POWER8).
23	RW	CCS_INST_ARR0_17_CCS_DDR_ADDRESS_14: DDR Address Row Column; bit 14 (formerly labeled wen for POWER8).
24:27	RW	CCS_INST_ARR0_17_CCS_DDR_CKE: DDR CKE. ccs_ddr_cke[0:1] → CKE[0:1] (also CKE[2:3] when CKEs copied enabled). ccs_ddr_cke[2:3] → CKE[4:5] (also CKE[6:7] when CKEs copied enabled).
28:31	RW	CCS_INST_ARR0_17_RESERVED_28_31: Reserved.
32:33	RW	CCS_INST_ARR0_17_CCS_DDR_CSN_0_1: DDR CSN Chip Select Not; bits 0:1.
34:35	RW	CCS_INST_ARR0_17_CCS_DDR_CID_0_1: DDR CID Chip ID; bits 0:1.
36:37	RW	CCS_INST_ARR0_17_CCS_DDR_CSN_2_3: DDR CSN Chip Select Not; bits 2:3.
38	RW	CCS_INST_ARR0_17_CCS_DDR_CID_2: DDR CID Chip ID; bit 2.
39:47	RW	CCS_INST_ARR0_17_RESERVED_39_47: Reserved.
48:51	RW	CCS_INST_ARR0_17_CCS_DDR_ODT: DDR ODT.
52:55	RW	CCS_INST_ARR0_17_RESERVED_52_55: Reserved.
56:59	RW	CCS_INST_ARR0_17_CCS_DDR_CAL_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the subtype. 0123 11XX = Initial calibration. Performs all of the following steps that are enabled via the configuration register: • SysclkRdclk alignment • DQS alignment • Read eye MPR centering • Write leveling • Write centering • Coarse rdwr alignment • Read eye custom pattern centering 10XX = Internal ZQ calibration (cal_rank is ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step.
60	RW	CCS_INST_ARR0_17_CCS_DDR_PARITY: DDR Parity. Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61	RW	CCS_INST_ARR0_17_CCS_DDR_BANK_2: DDR Address Bank; bit 2 (new for POWER9 DDR4E).
62:63	RW	CCS_INST_ARR0_17_CCS_LOOP_BREAK_MODE: Selects which programmable iteration value to compare to in order to break out of the loop. 00 = Never break out of the loop. 01 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare0. 10 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare1. 11 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare2. **Note**: This is now held in local latches instead of the array for earlier access.

Register Name	CCS INST ARR0 18 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR0_18
Address	0000000007012327 (SCOM)
Description	CCS INST ARR0 18

Bits	SCOM	Field Mnemonic: Description
0:13	RW	CCS_INST_ARR0_18_CCS_DDR_ADDRESS_0_13: DDR Address Row Column; bits 0:13.
14	RW	CCS_INST_ARR0_18_CCS_DDR_ADDRESS_17: DDR Address Row Column; bit 17 (formerly labeled address(14) for POWER8).
15	RW	CCS_INST_ARR0_18_CCS_DDR_BANK_GROUP_1: DDR Address Bank Group; bit 1 (formerly labeled address(15) for POWER8).
16	RW	CCS_INST_ARR0_18_CCS_DDR_RESETN: DDR Resetn. Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq[24] controls the value of DDR Resetn.
17:18	RW	CCS_INST_ARR0_18_CCS_DDR_BANK_0_1: DDR Address Bank; bits 0:1.
19	RW	CCS_INST_ARR0_18_CCS_DDR_BANK_GROUP_0: DDR Address Bank Group; bit 0 (formerly labeled bank(2) for POWER8).
20	RW	CCS_INST_ARR0_18_CCS_DDR_ACTN: DDR Activate Not (formerly labeled Active although functionally equivalent for POWER8).
21	RW	CCS_INST_ARR0_18_CCS_DDR_ADDRESS_16: DDR Address Row Column; bit 16 (formerly labeled rasn for POWER8).
22	RW	CCS_INST_ARR0_18_CCS_DDR_ADDRESS_15: DDR Address Row Column; bit 15 (formerly labeled casn for POWER8).
23	RW	CCS_INST_ARR0_18_CCS_DDR_ADDRESS_14: DDR Address Row Column; bit 14 (formerly labeled wen for POWER8).
24:27	RW	CCS_INST_ARR0_18_CCS_DDR_CKE: DDR CKE. ccs_ddr_cke[0:1] → CKE[0:1] (also CKE[2:3] when CKEs copied enabled). ccs_ddr_cke[2:3] → CKE[4:5] (also CKE[6:7] when CKEs copied enabled).
28:31	RW	CCS_INST_ARR0_18_RESERVED_28_31: Reserved.
32:33	RW	CCS_INST_ARR0_18_CCS_DDR_CSN_0_1: DDR CSN Chip Select Not; bits 0:1.
34:35	RW	CCS_INST_ARR0_18_CCS_DDR_CID_0_1: DDR CID Chip ID; bits 0:1.
36:37	RW	CCS_INST_ARR0_18_CCS_DDR_CSN_2_3: DDR CSN Chip Select Not; bits 2:3.
38	RW	CCS_INST_ARR0_18_CCS_DDR_CID_2: DDR CID Chip ID; bit 2.
39:47	RW	CCS_INST_ARR0_18_RESERVED_39_47: Reserved.
48:51	RW	CCS_INST_ARR0_18_CCS_DDR_ODT: DDR ODT.
52:55	RW	CCS_INST_ARR0_18_RESERVED_52_55: Reserved.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	CCS_INST_ARR0_18_CCS_DDR_CAL_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the subtype. 0123 11XX = Initial calibration. Performs all of the following steps that are enabled via the configuration register: • SysclkRdclk alignment • DQS alignment • Read eye MPR centering • Write leveling • Write centering • Coarse rdwr alignment • Read eye custom pattern centering 10XX = Internal ZQ calibration (cal_rank is ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step.
60	RW	CCS_INST_ARR0_18_CCS_DDR_PARITY: DDR Parity. Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61	RW	CCS_INST_ARR0_18_CCS_DDR_BANK_2: DDR Address Bank; bit 2 (new for POWER9 DDR4E).
62:63	RW	CCS_INST_ARR0_18_CCS_LOOP_BREAK_MODE: Selects which programmable iteration value to compare to in order to break out of the loop. 00 = Never break out of the loop. 01 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare0. 10 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare1. 11 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare2. **Note**: This is now held in local latches instead of the array for earlier access.

Register Name	CCS INST ARR0 19 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR0_19
Address	0000000007012328 (SCOM)
Description	CCS INST ARR0 19

Bits	SCOM	Field Mnemonic: Description
0:13	RW	CCS_INST_ARR0_19_CCS_DDR_ADDRESS_0_13: DDR Address Row Column; bits 0:13.
14	RW	CCS_INST_ARR0_19_CCS_DDR_ADDRESS_17: DDR Address Row Column; bit 17 (formerly labeled address(14) for POWER8).
15	RW	CCS_INST_ARR0_19_CCS_DDR_BANK_GROUP_1: DDR Address Bank Group; bit 1 (formerly labeled address(15) for POWER8).
16	RW	CCS_INST_ARR0_19_CCS_DDR_RESETN: DDR Resetn. Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq[24] controls the value of DDR Resetn.
17:18	RW	CCS_INST_ARR0_19_CCS_DDR_BANK_0_1: DDR Address Bank; bits 0:1.
19	RW	CCS_INST_ARR0_19_CCS_DDR_BANK_GROUP_0: DDR Address Bank Group; bit 0 (formerly labeled bank(2) for POWER8).
20	RW	CCS_INST_ARR0_19_CCS_DDR_ACTN: DDR Activate Not (formerly labeled Active although functionally equivalent for POWER8).
21	RW	CCS_INST_ARR0_19_CCS_DDR_ADDRESS_16: DDR Address Row Column; bit 16 (formerly labeled rasn for POWER8).

Bits	SCOM	Field Mnemonic: Description
22	RW	CCS_INST_ARR0_19_CCS_DDR_ADDRESS_15: DDR Address Row Column; bit 15 (formerly labeled casn for POWER8).
23	RW	CCS_INST_ARR0_19_CCS_DDR_ADDRESS_14: DDR Address Row Column; bit 14 (formerly labeled wen for POWER8).
24:27	RW	CCS_INST_ARR0_19_CCS_DDR_CKE: DDR CKE. ccs_ddr_cke[0:1] → CKE[0:1] (also CKE[2:3] when CKEs copied enabled). ccs_ddr_cke[2:3] → CKE[4:5] (also CKE[6:7] when CKEs copied enabled).
28:31	RW	CCS_INST_ARR0_19_RESERVED_28_31: Reserved.
32:33	RW	CCS_INST_ARR0_19_CCS_DDR_CSN_0_1: DDR CSN Chip Select Not; bits 0:1.
34:35	RW	CCS_INST_ARR0_19_CCS_DDR_CID_0_1: DDR CID Chip ID; bits 0:1.
36:37	RW	CCS_INST_ARR0_19_CCS_DDR_CSN_2_3: DDR CSN Chip Select Not; bits 2:3.
38	RW	CCS_INST_ARR0_19_CCS_DDR_CID_2: DDR CID Chip ID; bit 2.
39:47	RW	CCS_INST_ARR0_19_RESERVED_39_47: Reserved.
48:51	RW	CCS_INST_ARR0_19_CCS_DDR_ODT: DDR ODT.
52:55	RW	CCS_INST_ARR0_19_RESERVED_52_55: Reserved.
56:59	RW	CCS_INST_ARR0_19_CCS_DDR_CAL_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the subtype. 0123 11XX = Initial calibration. Performs all of the following steps that are enabled via the configuration register: • SysclkRdclk alignment • DQS alignment • Read eye MPR centering • Write leveling • Write centering • Coarse rdwr alignment • Read eye custom pattern centering 10XX = Internal ZQ calibration (cal_rank is ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step.
60	RW	CCS_INST_ARR0_19_CCS_DDR_PARITY: DDR Parity. Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61	RW	CCS_INST_ARR0_19_CCS_DDR_BANK_2: DDR Address Bank; bit 2 (new for POWER9 DDR4E).
62:63	RW	CCS_INST_ARR0_19_CCS_LOOP_BREAK_MODE: Selects which programmable iteration value to compare to in order to break out of the loop. 00 = Never break out of the loop. 01 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare0. 10 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare1. 11 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare2. **Note**: This is now held in local latches instead of the array for earlier access.

Register Name	CCS INST ARR0 20 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR0_20
Address	0000000007012329 (SCOM)
Description	CCS INST ARR0 20

Bits	SCOM	Field Mnemonic: Description
0:13	RW	CCS_INST_ARR0_20_CCS_DDR_ADDRESS_0_13: DDR Address Row Column; bits 0:13.
14	RW	CCS_INST_ARR0_20_CCS_DDR_ADDRESS_17: DDR Address Row Column; bit 17 (formerly labeled address(14) for POWER8).
15	RW	CCS_INST_ARR0_20_CCS_DDR_BANK_GROUP_1: DDR Address Bank Group; bit 1 (formerly labeled address(15) for POWER8).
16	RW	CCS_INST_ARR0_20_CCS_DDR_RESETN: DDR Resetn. Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq[24] controls the value of DDR Resetn.
17:18	RW	CCS_INST_ARR0_20_CCS_DDR_BANK_0_1: DDR Address Bank; bits 0:1.
19	RW	CCS_INST_ARR0_20_CCS_DDR_BANK_GROUP_0: DDR Address Bank Group; bit 0 (formerly labeled bank(2) for POWER8).
20	RW	CCS_INST_ARR0_20_CCS_DDR_ACTN: DDR Activate Not (formerly labeled Active although functionally equivalent for POWER8).
21	RW	CCS_INST_ARR0_20_CCS_DDR_ADDRESS_16: DDR Address Row Column; bit 16 (formerly labeled rasn for POWER8).
22	RW	CCS_INST_ARR0_20_CCS_DDR_ADDRESS_15: DDR Address Row Column; bit 15 (formerly labeled casn for POWER8).
23	RW	CCS_INST_ARR0_20_CCS_DDR_ADDRESS_14: DDR Address Row Column; bit 14 (formerly labeled wen for POWER8).
24:27	RW	CCS_INST_ARR0_20_CCS_DDR_CKE: DDR CKE. ccs_ddr_cke[0:1] → CKE[0:1] (also CKE[2:3] when CKEs copied enabled). ccs_ddr_cke[2:3] → CKE[4:5] (also CKE[6:7] when CKEs copied enabled).
28:31	RW	CCS_INST_ARR0_20_RESERVED_28_31: Reserved.
32:33	RW	CCS_INST_ARR0_20_CCS_DDR_CSN_0_1: DDR CSN Chip Select Not; bits 0:1.
34:35	RW	CCS_INST_ARR0_20_CCS_DDR_CID_0_1: DDR CID Chip ID; bits 0:1.
36:37	RW	CCS_INST_ARR0_20_CCS_DDR_CSN_2_3: DDR CSN Chip Select Not; bits 2:3.
38	RW	CCS_INST_ARR0_20_CCS_DDR_CID_2: DDR CID Chip ID; bit 2.
39:47	RW	CCS_INST_ARR0_20_RESERVED_39_47: Reserved.
48:51	RW	CCS_INST_ARR0_20_CCS_DDR_ODT: DDR ODT.
52:55	RW	CCS_INST_ARR0_20_RESERVED_52_55: Reserved.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	CCS_INST_ARR0_20_CCS_DDR_CAL_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the subtype. 0123 11XX = Initial calibration. Performs all of the following steps that are enabled via the configuration register: • SysclkRdclk alignment • DQS alignment • Read eye MPR centering • Write leveling • Write centering • Coarse rdwr alignment • Read eye custom pattern centering 10XX = Internal ZQ calibration (cal_rank is ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step 0001 = Periodic calibration: DQS alignment step 0010 = Periodic calibration: Read eye MPR centering step
60	RW	CCS_INST_ARR0_20_CCS_DDR_PARITY: DDR Parity. Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61	RW	CCS_INST_ARR0_20_CCS_DDR_BANK_2: DDR Address Bank; bit 2 (new for POWER9 DDR4E).
62:63	RW	CCS_INST_ARR0_20_CCS_LOOP_BREAK_MODE: Selects which programmable iteration value to compare to in order to break out of the loop. 00 = Never break out of the loop. 01 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare0. 10 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare1. 11 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare2. **Note**: This is now held in local latches instead of the array for earlier access.

Register Name	CCS INST ARR0 21 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR0_21
Address	000000000701232A (SCOM)
Description	CCS INST ARR0 21

Bits	SCOM	Field Mnemonic: Description
0:13	RW	CCS_INST_ARR0_21_CCS_DDR_ADDRESS_0_13: DDR Address Row Column; bits 0:13.
14	RW	CCS_INST_ARR0_21_CCS_DDR_ADDRESS_17: DDR Address Row Column; bit 17 (formerly labeled address(14) for POWER8).
15	RW	CCS_INST_ARR0_21_CCS_DDR_BANK_GROUP_1: DDR Address Bank Group; bit 1 (formerly labeled address(15) for POWER8).
16	RW	CCS_INST_ARR0_21_CCS_DDR_RESETN: DDR Resetn. Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq[24] controls the value of DDR Resetn.
17:18	RW	CCS_INST_ARR0_21_CCS_DDR_BANK_0_1: DDR Address Bank; bits 0:1.
19	RW	CCS_INST_ARR0_21_CCS_DDR_BANK_GROUP_0: DDR Address Bank Group; bit 0 (formerly labeled bank(2) for POWER8).
20	RW	CCS_INST_ARR0_21_CCS_DDR_ACTN: DDR Activate Not (formerly labeled Active although functionally equivalent for POWER8).
21	RW	CCS_INST_ARR0_21_CCS_DDR_ADDRESS_16: DDR Address Row Column; bit 16 (formerly labeled rasn for POWER8).

Bits	SCOM	Field Mnemonic: Description
22	RW	CCS_INST_ARR0_21_CCS_DDR_ADDRESS_15: DDR Address Row Column; bit 15 (formerly labeled casn for POWER8).
23	RW	CCS_INST_ARR0_21_CCS_DDR_ADDRESS_14: DDR Address Row Column; bit 14 (formerly labeled wen for POWER8).
24:27	RW	CCS_INST_ARR0_21_CCS_DDR_CKE: DDR CKE. ccs_ddr_cke[0:1] → CKE[0:1] (also CKE[2:3] when CKEs copied enabled). ccs_ddr_cke[2:3] → CKE[4:5] (also CKE[6:7] when CKEs copied enabled).
28:31	RW	CCS_INST_ARR0_21_RESERVED_28_31: Reserved.
32:33	RW	CCS_INST_ARR0_21_CCS_DDR_CSN_0_1: DDR CSN Chip Select Not; bits 0:1.
34:35	RW	CCS_INST_ARR0_21_CCS_DDR_CID_0_1: DDR CID Chip ID; bits 0:1.
36:37	RW	CCS_INST_ARR0_21_CCS_DDR_CSN_2_3: DDR CSN Chip Select Not; bits 2:3.
38	RW	CCS_INST_ARR0_21_CCS_DDR_CID_2: DDR CID Chip ID; bit 2.
39:47	RW	CCS_INST_ARR0_21_RESERVED_39_47: Reserved.
48:51	RW	CCS_INST_ARR0_21_CCS_DDR_ODT: DDR ODT.
52:55	RW	CCS_INST_ARR0_21_RESERVED_52_55: Reserved.
56:59	RW	CCS_INST_ARR0_21_CCS_DDR_CAL_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the subtype. 0123 11XX = Initial calibration. Performs all of the following steps that are enabled via the configuration register: • SysclkRdclk alignment • DQS alignment • Read eye MPR centering • Write leveling • Write centering • Coarse rdwr alignment • Read eye custom pattern centering 10XX = Internal ZQ calibration (cal_rank is ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step.
60	RW	CCS_INST_ARR0_21_CCS_DDR_PARITY: DDR Parity. Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61	RW	CCS_INST_ARR0_21_CCS_DDR_BANK_2: DDR Address Bank; bit 2 (new for POWER9 DDR4E).
62:63	RW	CCS_INST_ARR0_21_CCS_LOOP_BREAK_MODE: Selects which programmable iteration value to compare to in order to break out of the loop. 00 = Never break out of the loop. 01 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare0. 10 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare1. 11 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare2. **Note**: This is now held in local latches instead of the array for earlier access.

Register Name	CCS INST ARR0 22 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR0_22
Address	000000000701232B (SCOM)
Description	CCS INST ARR0 22

Bits	SCOM	Field Mnemonic: Description
0:13	RW	CCS_INST_ARR0_22_CCS_DDR_ADDRESS_0_13: DDR Address Row Column; bits 0:13.
14	RW	CCS_INST_ARR0_22_CCS_DDR_ADDRESS_17: DDR Address Row Column; bit 17 (formerly labeled address(14) for POWER8).
15	RW	CCS_INST_ARR0_22_CCS_DDR_BANK_GROUP_1: DDR Address Bank Group; bit 1 (formerly labeled address(15) for POWER8).
16	RW	CCS_INST_ARR0_22_CCS_DDR_RESETN: DDR Resetn. Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq[24] controls the value of DDR Resetn.
17:18	RW	CCS_INST_ARR0_22_CCS_DDR_BANK_0_1: DDR Address Bank; bits 0:1.
19	RW	CCS_INST_ARR0_22_CCS_DDR_BANK_GROUP_0: DDR Address Bank Group; bit 0 (formerly labeled bank(2) for POWER8).
20	RW	CCS_INST_ARR0_22_CCS_DDR_ACTN: DDR Activate Not (formerly labeled Active although functionally equivalent for POWER8).
21	RW	CCS_INST_ARR0_22_CCS_DDR_ADDRESS_16: DDR Address Row Column; bit 16 (formerly labeled rasn for POWER8).
22	RW	CCS_INST_ARR0_22_CCS_DDR_ADDRESS_15: DDR Address Row Column; bit 15 (formerly labeled casn for POWER8).
23	RW	CCS_INST_ARR0_22_CCS_DDR_ADDRESS_14: DDR Address Row Column; bit 14 (formerly labeled wen for POWER8).
24:27	RW	CCS_INST_ARR0_22_CCS_DDR_CKE: DDR CKE. ccs_ddr_cke[0:1] → CKE[0:1] (also CKE[2:3] when CKEs copied enabled). ccs_ddr_cke[2:3] → CKE[4:5] (also CKE[6:7] when CKEs copied enabled).
28:31	RW	CCS_INST_ARR0_22_RESERVED_28_31: Reserved.
32:33	RW	CCS_INST_ARR0_22_CCS_DDR_CSN_0_1: DDR CSN Chip Select Not; bits 0:1.
34:35	RW	CCS_INST_ARR0_22_CCS_DDR_CID_0_1: DDR CID Chip ID; bits 0:1.
36:37	RW	CCS_INST_ARR0_22_CCS_DDR_CSN_2_3: DDR CSN Chip Select Not; bits 2:3.
38	RW	CCS_INST_ARR0_22_CCS_DDR_CID_2: DDR CID Chip ID; bit 2.
39:47	RW	CCS_INST_ARR0_22_RESERVED_39_47: Reserved.
48:51	RW	CCS_INST_ARR0_22_CCS_DDR_ODT: DDR ODT.
52:55	RW	CCS_INST_ARR0_22_RESERVED_52_55: Reserved.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	CCS_INST_ARR0_22_CCS_DDR_CAL_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the subtype. 0123 11XX = Initial calibration. Performs all of the following steps that are enabled via the configuration register: • SysclkRdclk alignment • DQS alignment • Read eye MPR centering • Write leveling • Write centering • Coarse rdwr alignment • Read eye custom pattern centering 10XX = Internal ZQ calibration (cal_rank is ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step.
60	RW	CCS_INST_ARR0_22_CCS_DDR_PARITY: DDR Parity. Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61	RW	CCS_INST_ARR0_22_CCS_DDR_BANK_2: DDR Address Bank; bit 2 (new for POWER9 DDR4E).
62:63	RW	CCS_INST_ARR0_22_CCS_LOOP_BREAK_MODE: Selects which programmable iteration value to compare to in order to break out of the loop. 00 = Never break out of the loop. 01 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare0. 10 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare1. 11 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare2. **Note**: This is now held in local latches instead of the array for earlier access.

Register Name	CCS INST ARR0 23 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR0_23
Address	000000000701232C (SCOM)
Description	CCS INST ARR0 23

Bits	SCOM	Field Mnemonic: Description
0:13	RW	CCS_INST_ARR0_23_CCS_DDR_ADDRESS_0_13: DDR Address Row Column; bits 0:13.
14	RW	CCS_INST_ARR0_23_CCS_DDR_ADDRESS_17: DDR Address Row Column; bit 17 (formerly labeled address(14) for POWER8).
15	RW	CCS_INST_ARR0_23_CCS_DDR_BANK_GROUP_1: DDR Address Bank Group; bit 1 (formerly labeled address(15) for POWER8).
16	RW	CCS_INST_ARR0_23_CCS_DDR_RESETN: DDR Resetn. Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq[24] controls the value of DDR Resetn.
17:18	RW	CCS_INST_ARR0_23_CCS_DDR_BANK_0_1: DDR Address Bank; bits 0:1.
19	RW	CCS_INST_ARR0_23_CCS_DDR_BANK_GROUP_0: DDR Address Bank Group; bit 0 (formerly labeled bank(2) for POWER8).
20	RW	CCS_INST_ARR0_23_CCS_DDR_ACTN: DDR Activate Not (formerly labeled Active although functionally equivalent for POWER8).
21	RW	CCS_INST_ARR0_23_CCS_DDR_ADDRESS_16: DDR Address Row Column; bit 16 (formerly labeled rasn for POWER8).

Bits	SCOM	Field Mnemonic: Description
22	RW	CCS_INST_ARR0_23_CCS_DDR_ADDRESS_15: DDR Address Row Column; bit 15 (formerly labeled casn for POWER8).
23	RW	CCS_INST_ARR0_23_CCS_DDR_ADDRESS_14: DDR Address Row Column; bit 14 (formerly labeled wen for POWER8).
24:27	RW	CCS_INST_ARR0_23_CCS_DDR_CKE: DDR CKE. ccs_ddr_cke[0:1] → CKE[0:1] (also CKE[2:3] when CKEs copied enabled). ccs_ddr_cke[2:3] → CKE[4:5] (also CKE[6:7] when CKEs copied enabled).
28:31	RW	CCS_INST_ARR0_23_RESERVED_28_31: Reserved.
32:33	RW	CCS_INST_ARR0_23_CCS_DDR_CSN_0_1: DDR CSN Chip Select Not; bits 0:1.
34:35	RW	CCS_INST_ARR0_23_CCS_DDR_CID_0_1: DDR CID Chip ID; bits 0:1.
36:37	RW	CCS_INST_ARR0_23_CCS_DDR_CSN_2_3: DDR CSN Chip Select Not; bits 2:3.
38	RW	CCS_INST_ARR0_23_CCS_DDR_CID_2: DDR CID Chip ID; bit 2.
39:47	RW	CCS_INST_ARR0_23_RESERVED_39_47: Reserved.
48:51	RW	CCS_INST_ARR0_23_CCS_DDR_ODT: DDR ODT.
52:55	RW	CCS_INST_ARR0_23_RESERVED_52_55: Reserved.
56:59	RW	CCS_INST_ARR0_23_CCS_DDR_CAL_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the subtype. 0123 11XX = Initial calibration. Performs all of the following steps that are enabled via the configuration register: • SysclkRdclk alignment • DQS alignment • Read eye MPR centering • Write leveling • Write centering • Coarse rdwr alignment • Read eye custom pattern centering 10XX = Internal ZQ calibration (cal_rank is ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step.
60	RW	CCS_INST_ARR0_23_CCS_DDR_PARITY: DDR Parity. Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61	RW	CCS_INST_ARR0_23_CCS_DDR_BANK_2: DDR Address Bank; bit 2 (new for POWER9 DDR4E).
62:63	RW	CCS_INST_ARR0_23_CCS_LOOP_BREAK_MODE: Selects which programmable iteration value to compare to in order to break out of the loop. 00 = Never break out of the loop. 01 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare0. 10 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare1. 11 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare2. **Note**: This is now held in local latches instead of the array for earlier access.

Register Name	CCS INST ARR0 24 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR0_24
Address	000000000701232D (SCOM)
Description	CCS INST ARR0 24

Bits	SCOM	Field Mnemonic: Description
0:13	RW	CCS_INST_ARR0_24_CCS_DDR_ADDRESS_0_13: DDR Address Row Column; bits 0:13.
14	RW	CCS_INST_ARR0_24_CCS_DDR_ADDRESS_17: DDR Address Row Column; bit 17 (formerly labeled address(14) for POWER8).
15	RW	CCS_INST_ARR0_24_CCS_DDR_BANK_GROUP_1: DDR Address Bank Group; bit 1 (formerly labeled address(15) for POWER8).
16	RW	CCS_INST_ARR0_24_CCS_DDR_RESETN: DDR Resetn. Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq[24] controls the value of DDR Resetn.
17:18	RW	CCS_INST_ARR0_24_CCS_DDR_BANK_0_1: DDR Address Bank; bits 0:1.
19	RW	CCS_INST_ARR0_24_CCS_DDR_BANK_GROUP_0: DDR Address Bank Group; bit 0 (formerly labeled bank(2) for POWER8).
20	RW	CCS_INST_ARR0_24_CCS_DDR_ACTN: DDR Activate Not (formerly labeled Active although functionally equivalent for POWER8).
21	RW	CCS_INST_ARR0_24_CCS_DDR_ADDRESS_16: DDR Address Row Column; bit 16 (formerly labeled rasn for POWER8).
22	RW	CCS_INST_ARR0_24_CCS_DDR_ADDRESS_15: DDR Address Row Column; bit 15 (formerly labeled casn for POWER8).
23	RW	CCS_INST_ARR0_24_CCS_DDR_ADDRESS_14: DDR Address Row Column; bit 14 (formerly labeled wen for POWER8).
24:27	RW	CCS_INST_ARR0_24_CCS_DDR_CKE: DDR CKE. ccs_ddr_cke[0:1] → CKE[0:1] (also CKE[2:3] when CKEs copied enabled). ccs_ddr_cke[2:3] → CKE[4:5] (also CKE[6:7] when CKEs copied enabled).
28:31	RW	CCS_INST_ARR0_24_RESERVED_28_31: Reserved.
32:33	RW	CCS_INST_ARR0_24_CCS_DDR_CSN_0_1: DDR CSN Chip Select Not; bits 0:1.
34:35	RW	CCS_INST_ARR0_24_CCS_DDR_CID_0_1: DDR CID Chip ID; bits 0:1.
36:37	RW	CCS_INST_ARR0_24_CCS_DDR_CSN_2_3: DDR CSN Chip Select Not; bits 2:3.
38	RW	CCS_INST_ARR0_24_CCS_DDR_CID_2: DDR CID Chip ID; bit 2.
39:47	RW	CCS_INST_ARR0_24_RESERVED_39_47: Reserved.
48:51	RW	CCS_INST_ARR0_24_CCS_DDR_ODT: DDR ODT.
52:55	RW	CCS_INST_ARR0_24_RESERVED_52_55: Reserved.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	CCS_INST_ARR0_24_CCS_DDR_CAL_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the subtype. 0123 11XX = Initial calibration. Performs all of the following steps that are enabled via the configuration register: • SysclkRdclk alignment • DQS alignment • Read eye MPR centering • Write leveling • Write centering • Coarse rdwr alignment • Read eye custom pattern centering 10XX = Internal ZQ calibration (cal_rank is ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step.
60	RW	CCS_INST_ARR0_24_CCS_DDR_PARITY: DDR Parity. Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61	RW	CCS_INST_ARR0_24_CCS_DDR_BANK_2: DDR Address Bank; bit 2 (new for POWER9 DDR4E).
62:63	RW	CCS_INST_ARR0_24_CCS_LOOP_BREAK_MODE: Selects which programmable iteration value to compare to in order to break out of the loop. 00 = Never break out of the loop. 01 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare0. 10 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare1. 11 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare2. **Note**: This is now held in local latches instead of the array for earlier access.

Register Name	CCS INST ARR0 25 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR0_25
Address	000000000701232E (SCOM)
Description	CCS INST ARR0 25

Bits	SCOM	Field Mnemonic: Description
0:13	RW	CCS_INST_ARR0_25_CCS_DDR_ADDRESS_0_13: DDR Address Row Column; bits 0:13.
14	RW	CCS_INST_ARR0_25_CCS_DDR_ADDRESS_17: DDR Address Row Column; bit 17 (formerly labeled address(14) for POWER8).
15	RW	CCS_INST_ARR0_25_CCS_DDR_BANK_GROUP_1: DDR Address Bank Group; bit 1 (formerly labeled address(15) for POWER8).
16	RW	CCS_INST_ARR0_25_CCS_DDR_RESETN: DDR Resetn. Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq[24] controls the value of DDR Resetn.
17:18	RW	CCS_INST_ARR0_25_CCS_DDR_BANK_0_1: DDR Address Bank; bits 0:1.
19	RW	CCS_INST_ARR0_25_CCS_DDR_BANK_GROUP_0: DDR Address Bank Group; bit 0 (formerly labeled bank(2) for POWER8).
20	RW	CCS_INST_ARR0_25_CCS_DDR_ACTN: DDR Activate Not (formerly labeled Active although functionally equivalent for POWER8).
21	RW	CCS_INST_ARR0_25_CCS_DDR_ADDRESS_16: DDR Address Row Column; bit 16 (formerly labeled rasn for POWER8).

Bits	SCOM	Field Mnemonic: Description
22	RW	CCS_INST_ARR0_25_CCS_DDR_ADDRESS_15: DDR Address Row Column; bit 15 (formerly labeled casn for POWER8).
23	RW	CCS_INST_ARR0_25_CCS_DDR_ADDRESS_14: DDR Address Row Column; bit 14 (formerly labeled wen for POWER8).
24:27	RW	CCS_INST_ARR0_25_CCS_DDR_CKE: DDR CKE. ccs_ddr_cke[0:1] → CKE[0:1] (also CKE[2:3] when CKEs copied enabled). ccs_ddr_cke[2:3] → CKE[4:5] (also CKE[6:7] when CKEs copied enabled).
28:31	RW	CCS_INST_ARR0_25_RESERVED_28_31: Reserved.
32:33	RW	CCS_INST_ARR0_25_CCS_DDR_CSN_0_1: DDR CSN Chip Select Not; bits 0:1.
34:35	RW	CCS_INST_ARR0_25_CCS_DDR_CID_0_1: DDR CID Chip ID; bits 0:1.
36:37	RW	CCS_INST_ARR0_25_CCS_DDR_CSN_2_3: DDR CSN Chip Select Not; bits 2:3.
38	RW	CCS_INST_ARR0_25_CCS_DDR_CID_2: DDR CID Chip ID; bit 2.
39:47	RW	CCS_INST_ARR0_25_RESERVED_39_47: Reserved.
48:51	RW	CCS_INST_ARR0_25_CCS_DDR_ODT: DDR ODT.
52:55	RW	CCS_INST_ARR0_25_RESERVED_52_55: Reserved.
56:59	RW	CCS_INST_ARR0_25_CCS_DDR_CAL_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the subtype. 0123 11XX = Initial calibration. Performs all of the following steps that are enabled via the configuration register: • SysclkRdclk alignment • DQS alignment • Read eye MPR centering • Write leveling • Write centering • Coarse rdwr alignment • Read eye custom pattern centering 10XX = Internal ZQ calibration (cal_rank is ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step.
60	RW	CCS_INST_ARR0_25_CCS_DDR_PARITY: DDR Parity. Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61	RW	CCS_INST_ARR0_25_CCS_DDR_BANK_2: DDR Address Bank; bit 2 (new for POWER9 DDR4E).
62:63	RW	CCS_INST_ARR0_25_CCS_LOOP_BREAK_MODE: Selects which programmable iteration value to compare to in order to break out of the loop. 00 = Never break out of the loop. 01 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare0. 10 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare1. 11 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare2. **Note**: This is now held in local latches instead of the array for earlier access.

Register Name	CCS INST ARR0 26 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR0_26
Address	000000000701232F (SCOM)
Description	ccs inst arr0 26

Bits	SCOM	Field Mnemonic: Description
0:13	RW	CCS_INST_ARR0_26_CCS_DDR_ADDRESS_0_13: DDR Address Row Column; bits 0:13.
14	RW	CCS_INST_ARR0_26_CCS_DDR_ADDRESS_17: DDR Address Row Column; bit 17 (formerly labeled address(14) for POWER8).
15	RW	CCS_INST_ARR0_26_CCS_DDR_BANK_GROUP_1: DDR Address Bank Group; bit 1 (formerly labeled address(15) for POWER8).
16	RW	CCS_INST_ARR0_26_CCS_DDR_RESETN: DDR Resetn. Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq[24] controls the value of DDR Resetn.
17:18	RW	CCS_INST_ARR0_26_CCS_DDR_BANK_0_1: DDR Address Bank; bits 0:1.
19	RW	CCS_INST_ARR0_26_CCS_DDR_BANK_GROUP_0: DDR Address Bank Group; bit 0 (formerly labeled bank(2) for POWER8).
20	RW	CCS_INST_ARR0_26_CCS_DDR_ACTN: DDR Activate Not (formerly labeled Active although functionally equivalent for POWER8).
21	RW	CCS_INST_ARR0_26_CCS_DDR_ADDRESS_16: DDR Address Row Column; bit 16 (formerly labeled rasn for POWER8).
22	RW	CCS_INST_ARR0_26_CCS_DDR_ADDRESS_15: DDR Address Row Column; bit 15 (formerly labeled casn for POWER8).
23	RW	CCS_INST_ARR0_26_CCS_DDR_ADDRESS_14: DDR Address Row Column; bit 14 (formerly labeled wen for POWER8).
24:27	RW	CCS_INST_ARR0_26_CCS_DDR_CKE: DDR CKE. ccs_ddr_cke[0:1] → CKE[0:1] (also CKE[2:3] when CKEs copied enabled). ccs_ddr_cke[2:3] → CKE[4:5] (also CKE[6:7] when CKEs copied enabled).
28:31	RW	CCS_INST_ARR0_26_RESERVED_28_31: Reserved.
32:33	RW	CCS_INST_ARR0_26_CCS_DDR_CSN_0_1: DDR CSN Chip Select Not; bits 0:1.
34:35	RW	CCS_INST_ARR0_26_CCS_DDR_CID_0_1: DDR CID Chip ID; bits 0:1.
36:37	RW	CCS_INST_ARR0_26_CCS_DDR_CSN_2_3: DDR CSN Chip Select Not; bits 2:3.
38	RW	CCS_INST_ARR0_26_CCS_DDR_CID_2: DDR CID Chip ID; bit 2.
39:47	RW	CCS_INST_ARR0_26_RESERVED_39_47: Reserved.
48:51	RW	CCS_INST_ARR0_26_CCS_DDR_ODT: DDR ODT.
52:55	RW	CCS_INST_ARR0_26_RESERVED_52_55: Reserved.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	CCS_INST_ARR0_26_CCS_DDR_CAL_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the subtype. 0123 11XX = Initial calibration. Performs all of the following steps that are enabled via the configuration register: • SysclkRdclk alignment • DQS alignment • Read eye MPR centering • Write leveling • Write centering • Coarse rdwr alignment • Read eye custom pattern centering 10XX = Internal ZQ calibration (cal_rank is ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step.
60	RW	CCS_INST_ARR0_26_CCS_DDR_PARITY: DDR Parity. Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61	RW	CCS_INST_ARR0_26_CCS_DDR_BANK_2: DDR Address Bank; bit 2 (new for POWER9 DDR4E).
62:63	RW	CCS_INST_ARR0_26_CCS_LOOP_BREAK_MODE: Selects which programmable iteration value to compare to in order to break out of the loop. 00 = Never break out of the loop. 01 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare0. 10 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare1. 11 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare2. **Note**: This is now held in local latches instead of the array for earlier access.

Register Name	CCS INST ARR0 27 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR0_27
Address	0000000007012330 (SCOM)
Description	CCS INST ARR0 27

Bits	SCOM	Field Mnemonic: Description
0:13	RW	CCS_INST_ARR0_27_CCS_DDR_ADDRESS_0_13: DDR Address Row Column; bits 0:13.
14	RW	CCS_INST_ARR0_27_CCS_DDR_ADDRESS_17: DDR Address Row Column; bit 17 (formerly labeled address(14) for POWER8).
15	RW	CCS_INST_ARR0_27_CCS_DDR_BANK_GROUP_1: DDR Address Bank Group; bit 1 (formerly labeled address(15) for POWER8).
16	RW	CCS_INST_ARR0_27_CCS_DDR_RESETN: DDR Resetn. Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq[24] controls the value of DDR Resetn.
17:18	RW	CCS_INST_ARR0_27_CCS_DDR_BANK_0_1: DDR Address Bank; bits 0:1.
19	RW	CCS_INST_ARR0_27_CCS_DDR_BANK_GROUP_0: DDR Address Bank Group; bit 0 (formerly labeled bank(2) for POWER8).
20	RW	CCS_INST_ARR0_27_CCS_DDR_ACTN: DDR Activate Not (formerly labeled Active although functionally equivalent for POWER8).
21	RW	CCS_INST_ARR0_27_CCS_DDR_ADDRESS_16: DDR Address Row Column; bit 16 (formerly labeled rasn for POWER8).

Bits	SCOM	Field Mnemonic: Description
22	RW	CCS_INST_ARR0_27_CCS_DDR_ADDRESS_15: DDR Address Row Column; bit 15 (formerly labeled casn for POWER8).
23	RW	CCS_INST_ARR0_27_CCS_DDR_ADDRESS_14: DDR Address Row Column; bit 14 (formerly labeled wen for POWER8).
24:27	RW	CCS_INST_ARR0_27_CCS_DDR_CKE: DDR CKE. ccs_ddr_cke[0:1] → CKE[0:1] (also CKE[2:3] when CKEs copied enabled). ccs_ddr_cke[2:3] → CKE[4:5] (also CKE[6:7] when CKEs copied enabled).
28:31	RW	CCS_INST_ARR0_27_RESERVED_28_31: Reserved.
32:33	RW	CCS_INST_ARR0_27_CCS_DDR_CSN_0_1: DDR CSN Chip Select Not; bits 0:1.
34:35	RW	CCS_INST_ARR0_27_CCS_DDR_CID_0_1: DDR CID Chip ID; bits 0:1.
36:37	RW	CCS_INST_ARR0_27_CCS_DDR_CSN_2_3: DDR CSN Chip Select Not; bits 2:3.
38	RW	CCS_INST_ARR0_27_CCS_DDR_CID_2: DDR CID Chip ID; bit 2.
39:47	RW	CCS_INST_ARR0_27_RESERVED_39_47: Reserved.
48:51	RW	CCS_INST_ARR0_27_CCS_DDR_ODT: DDR ODT.
52:55	RW	CCS_INST_ARR0_27_RESERVED_52_55: Reserved.
56:59	RW	CCS_INST_ARR0_27_CCS_DDR_CAL_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the subtype. 0123 11XX = Initial calibration. Performs all of the following steps that are enabled via the configuration register: • SysclkRdclk alignment • DQS alignment • Read eye MPR centering • Write leveling • Write centering • Coarse rdwr alignment • Read eye custom pattern centering 10XX = Internal ZQ calibration (cal_rank is ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step.
60	RW	CCS_INST_ARR0_27_CCS_DDR_PARITY: DDR Parity. Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61	RW	CCS_INST_ARR0_27_CCS_DDR_BANK_2: DDR Address Bank; bit 2 (new for POWER9 DDR4E).
62:63	RW	CCS_INST_ARR0_27_CCS_LOOP_BREAK_MODE: Selects which programmable iteration value to compare to in order to break out of the loop. 00 = Never break out of the loop. 01 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare0. 10 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare1. 11 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare2. **Note**: This is now held in local latches instead of the array for earlier access.

Register Name	CCS INST ARR0 28 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR0_28
Address	0000000007012331 (SCOM)
Description	CCS INST ARR0 28

Bits	SCOM	Field Mnemonic: Description
0:13	RW	CCS_INST_ARR0_28_CCS_DDR_ADDRESS_0_13: DDR Address Row Column; bits 0:13.
14	RW	CCS_INST_ARR0_28_CCS_DDR_ADDRESS_17: DDR Address Row Column; bit 17 (formerly labeled address(14) for POWER8).
15	RW	CCS_INST_ARR0_28_CCS_DDR_BANK_GROUP_1: DDR Address Bank Group; bit 1 (formerly labeled address(15) for POWER8).
16	RW	CCS_INST_ARR0_28_CCS_DDR_RESETN: DDR Resetn. Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq[24] controls the value of DDR Resetn.
17:18	RW	CCS_INST_ARR0_28_CCS_DDR_BANK_0_1: DDR Address Bank; bits 0:1.
19	RW	CCS_INST_ARR0_28_CCS_DDR_BANK_GROUP_0: DDR Address Bank Group; bit 0 (formerly labeled bank(2) for POWER8).
20	RW	CCS_INST_ARR0_28_CCS_DDR_ACTN: DDR Activate Not (formerly labeled Active although functionally equivalent for POWER8).
21	RW	CCS_INST_ARR0_28_CCS_DDR_ADDRESS_16: DDR Address Row Column; bit 16 (formerly labeled rasn for POWER8).
22	RW	CCS_INST_ARR0_28_CCS_DDR_ADDRESS_15: DDR Address Row Column; bit 15 (formerly labeled casn for POWER8).
23	RW	CCS_INST_ARR0_28_CCS_DDR_ADDRESS_14: DDR Address Row Column; bit 14 (formerly labeled wen for POWER8).
24:27	RW	CCS_INST_ARR0_28_CCS_DDR_CKE: DDR CKE. ccs_ddr_cke[0:1] → CKE[0:1] (also CKE[2:3] when CKEs copied enabled). ccs_ddr_cke[2:3] → CKE[4:5] (also CKE[6:7] when CKEs copied enabled).
28:31	RW	CCS_INST_ARR0_28_RESERVED_28_31: Reserved.
32:33	RW	CCS_INST_ARR0_28_CCS_DDR_CSN_0_1: DDR CSN Chip Select Not; bits 0:1.
34:35	RW	CCS_INST_ARR0_28_CCS_DDR_CID_0_1: DDR CID Chip ID; bits 0:1.
36:37	RW	CCS_INST_ARR0_28_CCS_DDR_CSN_2_3: DDR CSN Chip Select Not; bits 2:3.
38	RW	CCS_INST_ARR0_28_CCS_DDR_CID_2: DDR CID Chip ID; bit 2.
39:47	RW	CCS_INST_ARR0_28_RESERVED_39_47: Reserved.
48:51	RW	CCS_INST_ARR0_28_CCS_DDR_ODT: DDR ODT.
52:55	RW	CCS_INST_ARR0_28_RESERVED_52_55: Reserved.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	CCS_INST_ARR0_28_CCS_DDR_CAL_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the subtype. 0123 11XX = Initial calibration. Performs all of the following steps that are enabled via the configuration register: • SysclkRdclk alignment • DQS alignment • Read eye MPR centering • Write leveling • Write centering • Coarse rdwr alignment • Read eye custom pattern centering 10XX = Internal ZQ calibration (cal_rank is ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step.
60	RW	CCS_INST_ARR0_28_CCS_DDR_PARITY: DDR Parity. Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61	RW	CCS_INST_ARR0_28_CCS_DDR_BANK_2: DDR Address Bank; bit 2 (new for POWER9 DDR4E).
62:63	RW	CCS_INST_ARR0_28_CCS_LOOP_BREAK_MODE: Selects which programmable iteration value to compare to in order to break out of the loop. 00 = Never break out of the loop. 01 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare0. 10 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare1. 11 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare2. **Note**: This is now held in local latches instead of the array for earlier access.

Register Name	CCS INST ARR0 29 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR0_29
Address	0000000007012332 (SCOM)
Description	CCS INST ARR0 29

Bits	SCOM	Field Mnemonic: Description
0:13	RW	CCS_INST_ARR0_29_CCS_DDR_ADDRESS_0_13: DDR Address Row Column; bits 0:13.
14	RW	CCS_INST_ARR0_29_CCS_DDR_ADDRESS_17: DDR Address Row Column; bit 17 (formerly labeled address(14) for POWER8).
15	RW	CCS_INST_ARR0_29_CCS_DDR_BANK_GROUP_1: DDR Address Bank Group; bit 1 (formerly labeled address(15) for POWER8).
16	RW	CCS_INST_ARR0_29_CCS_DDR_RESETN: DDR Resetn. Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq[24] controls the value of DDR Resetn.
17:18	RW	CCS_INST_ARR0_29_CCS_DDR_BANK_0_1: DDR Address Bank; bits 0:1.
19	RW	CCS_INST_ARR0_29_CCS_DDR_BANK_GROUP_0: DDR Address Bank Group; bit 0 (formerly labeled bank(2) for POWER8).
20	RW	CCS_INST_ARR0_29_CCS_DDR_ACTN: DDR Activate Not (formerly labeled Active although functionally equivalent for POWER8).
21	RW	CCS_INST_ARR0_29_CCS_DDR_ADDRESS_16: DDR Address Row Column; bit 16 (formerly labeled rasn for POWER8).

Bits	SCOM	Field Mnemonic: Description
22	RW	CCS_INST_ARR0_29_CCS_DDR_ADDRESS_15: DDR Address Row Column; bit 15 (formerly labeled casn for POWER8).
23	RW	CCS_INST_ARR0_29_CCS_DDR_ADDRESS_14: DDR Address Row Column; bit 14 (formerly labeled wen for POWER8).
24:27	RW	CCS_INST_ARR0_29_CCS_DDR_CKE: DDR CKE. ccs_ddr_cke[0:1] → CKE[0:1] (also CKE[2:3] when CKEs copied enabled). ccs_ddr_cke[2:3] → CKE[4:5] (also CKE[6:7] when CKEs copied enabled).
28:31	RW	CCS_INST_ARR0_29_RESERVED_28_31: Reserved.
32:33	RW	CCS_INST_ARR0_29_CCS_DDR_CSN_0_1: DDR CSN Chip Select Not; bits 0:1.
34:35	RW	CCS_INST_ARR0_29_CCS_DDR_CID_0_1: DDR CID Chip ID; bits 0:1.
36:37	RW	CCS_INST_ARR0_29_CCS_DDR_CSN_2_3: DDR CSN Chip Select Not; bits 2:3.
38	RW	CCS_INST_ARR0_29_CCS_DDR_CID_2: DDR CID Chip ID; bit 2.
39:47	RW	CCS_INST_ARR0_29_RESERVED_39_47: Reserved.
48:51	RW	CCS_INST_ARR0_29_CCS_DDR_ODT: DDR ODT.
52:55	RW	CCS_INST_ARR0_29_RESERVED_52_55: Reserved.
56:59	RW	CCS_INST_ARR0_29_CCS_DDR_CAL_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the subtype. 0123 11XX = Initial calibration. Performs all of the following steps that are enabled via the configuration register: • SysclkRdclk alignment • DQS alignment • Read eye MPR centering • Write leveling • Write centering • Coarse rdwr alignment • Read eye custom pattern centering 10XX = Internal ZQ calibration (cal_rank is ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step.
60	RW	CCS_INST_ARR0_29_CCS_DDR_PARITY: DDR Parity. Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61	RW	CCS_INST_ARR0_29_CCS_DDR_BANK_2: DDR Address Bank; bit 2 (new for POWER9 DDR4E).
62:63	RW	CCS_INST_ARR0_29_CCS_LOOP_BREAK_MODE: Selects which programmable iteration value to compare to in order to break out of the loop. 00 = Never break out of the loop. 01 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare0. 10 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare1. 11 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare2. **Note**: This is now held in local latches instead of the array for earlier access.

Register Name	CCS INST ARR0 30 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR0_30
Address	0000000007012333 (SCOM)
Description	CCS INST ARR0 30

Bits	SCOM	Field Mnemonic: Description
0:13	RW	CCS_INST_ARR0_30_CCS_DDR_ADDRESS_0_13: DDR Address Row Column; bits 0:13.
14	RW	CCS_INST_ARR0_30_CCS_DDR_ADDRESS_17: DDR Address Row Column; bit 17 (formerly labeled address(14) for POWER8).
15	RW	CCS_INST_ARR0_30_CCS_DDR_BANK_GROUP_1: DDR Address Bank Group; bit 1 (formerly labeled address(15) for POWER8).
16	RW	CCS_INST_ARR0_30_CCS_DDR_RESETN: DDR Resetn. Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq[24] controls the value of DDR Resetn.
17:18	RW	CCS_INST_ARR0_30_CCS_DDR_BANK_0_1: DDR Address Bank; bits 0:1.
19	RW	CCS_INST_ARR0_30_CCS_DDR_BANK_GROUP_0: DDR Address Bank Group; bit 0 (formerly labeled bank(2) for POWER8).
20	RW	CCS_INST_ARR0_30_CCS_DDR_ACTN: DDR Activate Not (formerly labeled Active although functionally equivalent for POWER8).
21	RW	CCS_INST_ARR0_30_CCS_DDR_ADDRESS_16: DDR Address Row Column; bit 16 (formerly labeled rasn for POWER8).
22	RW	CCS_INST_ARR0_30_CCS_DDR_ADDRESS_15: DDR Address Row Column; bit 15 (formerly labeled casn for POWER8).
23	RW	CCS_INST_ARR0_30_CCS_DDR_ADDRESS_14: DDR Address Row Column; bit 14 (formerly labeled wen for POWER8).
24:27	RW	CCS_INST_ARR0_30_CCS_DDR_CKE: DDR CKE. ccs_ddr_cke[0:1] → CKE[0:1] (also CKE[2:3] when CKEs copied enabled). ccs_ddr_cke[2:3] → CKE[4:5] (also CKE[6:7] when CKEs copied enabled).
28:31	RW	CCS_INST_ARR0_30_RESERVED_28_31: Reserved.
32:33	RW	CCS_INST_ARR0_30_CCS_DDR_CSN_0_1: DDR CSN Chip Select Not; bits 0:1.
34:35	RW	CCS_INST_ARR0_30_CCS_DDR_CID_0_1: DDR CID Chip ID; bits 0:1.
36:37	RW	CCS_INST_ARR0_30_CCS_DDR_CSN_2_3: DDR CSN Chip Select Not; bits 2:3.
38	RW	CCS_INST_ARR0_30_CCS_DDR_CID_2: DDR CID Chip ID; bit 2.
39:47	RW	CCS_INST_ARR0_30_RESERVED_39_47: Reserved.
48:51	RW	CCS_INST_ARR0_30_CCS_DDR_ODT: DDR ODT.
52:55	RW	CCS_INST_ARR0_30_RESERVED_52_55: Reserved.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	CCS_INST_ARR0_30_CCS_DDR_CAL_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the subtype. 0123 11XX = Initial calibration. Performs all of the following steps that are enabled via the configuration register: • SysclkRdclk alignment • DQS alignment • Read eye MPR centering • Write leveling • Write centering • Coarse rdwr alignment • Read eye custom pattern centering 10XX = Internal ZQ calibration (cal_rank is ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step.
60	RW	CCS_INST_ARR0_30_CCS_DDR_PARITY: DDR Parity. Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61	RW	CCS_INST_ARR0_30_CCS_DDR_BANK_2: DDR Address Bank; bit 2 (new for POWER9 DDR4E).
62:63	RW	CCS_INST_ARR0_30_CCS_LOOP_BREAK_MODE: Selects which programmable iteration value to compare to in order to break out of the loop. 00 = Never break out of the loop. 01 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare0. 10 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare1. 11 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare2. **Note**: This is now held in local latches instead of the array for earlier access.

Register Name	CCS INST ARR0 31 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR0_31
Address	0000000007012334 (SCOM)
Description	CCS INST ARR0 31

Bits	SCOM	Field Mnemonic: Description
0:13	RW	CCS_INST_ARR0_31_CCS_DDR_ADDRESS_0_13: DDR Address Row Column; bits 0:13.
14	RW	CCS_INST_ARR0_31_CCS_DDR_ADDRESS_17: DDR Address Row Column; bit 17 (formerly labeled address(14) for POWER8).
15	RW	CCS_INST_ARR0_31_CCS_DDR_BANK_GROUP_1: DDR Address Bank Group; bit 1 (formerly labeled address(15) for POWER8).
16	RW	CCS_INST_ARR0_31_CCS_DDR_RESETN: DDR Resetn. Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq[24] controls the value of DDR Resetn.
17:18	RW	CCS_INST_ARR0_31_CCS_DDR_BANK_0_1: DDR Address Bank; bits 0:1.
19	RW	CCS_INST_ARR0_31_CCS_DDR_BANK_GROUP_0: DDR Address Bank Group; bit 0 (formerly labeled bank(2) for POWER8).
20	RW	CCS_INST_ARR0_31_CCS_DDR_ACTN: DDR Activate Not (formerly labeled Active although functionally equivalent for POWER8).
21	RW	CCS_INST_ARR0_31_CCS_DDR_ADDRESS_16: DDR Address Row Column; bit 16 (formerly labeled rasn for POWER8).

Bits	SCOM	Field Mnemonic: Description
22	RW	CCS_INST_ARR0_31_CCS_DDR_ADDRESS_15: DDR Address Row Column; bit 15 (formerly labeled casn for POWER8).
23	RW	CCS_INST_ARR0_31_CCS_DDR_ADDRESS_14: DDR Address Row Column; bit 14 (formerly labeled wen for POWER8).
24:27	RW	CCS_INST_ARR0_31_CCS_DDR_CKE: DDR CKE. ccs_ddr_cke[0:1] → CKE[0:1] (also CKE[2:3] when CKEs copied enabled). ccs_ddr_cke[2:3] → CKE[4:5] (also CKE[6:7] when CKEs copied enabled).
28:31	RW	CCS_INST_ARR0_31_RESERVED_28_31: Reserved.
32:33	RW	CCS_INST_ARR0_31_CCS_DDR_CSN_0_1: DDR CSN Chip Select Not; bits 0:1.
34:35	RW	CCS_INST_ARR0_31_CCS_DDR_CID_0_1: DDR CID Chip ID; bits 0:1.
36:37	RW	CCS_INST_ARR0_31_CCS_DDR_CSN_2_3: DDR CSN Chip Select Not; bits 2:3.
38	RW	CCS_INST_ARR0_31_CCS_DDR_CID_2: DDR CID Chip ID; bit 2.
39:47	RW	CCS_INST_ARR0_31_RESERVED_39_47: Reserved.
48:51	RW	CCS_INST_ARR0_31_CCS_DDR_ODT: DDR ODT.
52:55	RW	CCS_INST_ARR0_31_RESERVED_52_55: Reserved.
56:59	RW	CCS_INST_ARR0_31_CCS_DDR_CAL_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the subtype. 0123 11XX = Initial calibration. Performs all of the following steps that are enabled via the configuration register: • SysclkRdclk alignment • DQS alignment • Read eye MPR centering • Write leveling • Write centering • Coarse rdwr alignment • Read eye custom pattern centering 10XX = Internal ZQ calibration (cal_rank is ignored). 01XX = External ZQ calibration. Requested rank is ZQ calibrated. 0000 = Periodic calibration: SysClkRdClk alignment step. 0001 = Periodic calibration: DQS alignment step. 0010 = Periodic calibration: Read eye MPR centering step.
60	RW	CCS_INST_ARR0_31_CCS_DDR_PARITY: DDR Parity. Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61	RW	CCS_INST_ARR0_31_CCS_DDR_BANK_2: DDR Address Bank; bit 2 (new for POWER9 DDR4E).
62:63	RW	CCS_INST_ARR0_31_CCS_LOOP_BREAK_MODE: Selects which programmable iteration value to compare to in order to break out of the loop. 00 = Never break out of the loop. 01 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare0. 10 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare1. 11 = Breaks out of the loop when equal to CCSARRERRINJQ_ccs_loop_counter_compare2. **Note**: This is now held in local latches instead of the array for earlier access.

Register Name	CCS INST ARR1 00 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR1_00
Address	0000000007012335 (SCOM)
Description	CCS INST ARR1 00

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_00_IDLES: The number of idle cycles before issuing the next command.
16:31	RW	CCS_INST_ARR1_00_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_00_READ_OR_WRITE_DATA: This is write data [0:19] if a write command is coded up, or a read compare byte if a read command is coded up. (Each bit represents a nibble of data.)
52	RW	CCS_INST_ARR1_00_READ_COMPARE_REQUIRED: Set to 1b if this command is a read, and requires a data compare.
53:56	RW	CCS_INST_ARR1_00_DDR_CAL_RANK: DDR rank address[0:3] to calibrate.
57	RW	CCS_INST_ARR1_00_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0.
58	RW	CCS_INST_ARR1_00_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_00_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, go to this command number next (after the repeat count has expired).

Register Name	CCS INST ARR1 01 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR1_01
Address	0000000007012336 (SCOM)
Description	CCS INST ARR1 01

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_01_IDLES: The number of idle cycles before issuing the next command.
16:31	RW	CCS_INST_ARR1_01_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_01_READ_OR_WRITE_DATA: This is write data [0:19] if a write command is coded up, or a read compare byte if a read command is coded up. (Each bit represents a nibble of data.)
52	RW	CCS_INST_ARR1_01_READ_COMPARE_REQUIRED: Set to 1b if this command is a read and requires a data compare.
53:56	RW	CCS_INST_ARR1_01_DDR_CAL_RANK: DDR rank address [0:3] to calibrate.
57	RW	CCS_INST_ARR1_01_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0.
58	RW	CCS_INST_ARR1_01_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_01_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, go to this command number next (after the repeat count has expired).

Register Name	CCS INST ARR1 02 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR1_02
Address	0000000007012337 (SCOM)
Description	CCS INST ARR1 02

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_02_IDLES: The number of idle cycles before issuing the next command.
16:31	RW	CCS_INST_ARR1_02_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_02_READ_OR_WRITE_DATA: This is write data [0:19] if a write command is coded up, or a read compare byte if a read command is coded up. (Each bit represents a nibble of data.)
52	RW	CCS_INST_ARR1_02_READ_COMPARE_REQUIRED: Set to 1b if this command is a read and requires a data compare.
53:56	RW	CCS_INST_ARR1_02_DDR_CAL_RANK: DDR rank address [0:3] to calibrate.
57	RW	CCS_INST_ARR1_02_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0.
58	RW	CCS_INST_ARR1_02_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_02_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, go to this command number next (after the repeat count has expired).

Register Name	**CCS INST ARR1 03 Register**
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR1_03
Address	0000000007012338 (SCOM)
Description	CCS INST ARR1 03

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_03_IDLES: The number of idle cycles before issuing the next command.
16:31	RW	CCS_INST_ARR1_03_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_03_READ_OR_WRITE_DATA: This is write data [0:19] if a write command is coded up, or a read compare byte if a read command is coded up. (Each bit represents a nibble of data.)
52	RW	CCS_INST_ARR1_03_READ_COMPARE_REQUIRED: Set to 1b if this command is a read and requires a data compare.
53:56	RW	CCS_INST_ARR1_03_DDR_CAL_RANK:DDR rank address [0:3] to calibrate.
57	RW	CCS_INST_ARR1_03_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0.
58	RW	CCS_INST_ARR1_03_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_03_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, go to this command number next (after the repeat count has expired).

Register Name	**CCS INST ARR1 04 Register**
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR1_04
Address	0000000007012339 (SCOM)
Description	CCS INST ARR1 04

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_04_IDLES: The number of idle cycles before issuing the next command.
16:31	RW	CCS_INST_ARR1_04_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_04_READ_OR_WRITE_DATA: This is write data [0:19] if a write command is coded up, or a read compare byte if a read command is coded up. (Each bit represents a nibble of data.)

Bits	SCOM	Field Mnemonic: Description
52	RW	CCS_INST_ARR1_04_READ_COMPARE_REQUIRED: Set to 1b if this command is a read and requires a data compare.
53:56	RW	CCS_INST_ARR1_04_DDR_CAL_RANK:DDR rank address [0:3] to calibrate.
57	RW	CCS_INST_ARR1_04_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0.
58	RW	CCS_INST_ARR1_04_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_04_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, go to this command number next (after the repeat count has expired).

Register Name	CCS INST ARR1 05 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR1_05
Address	000000000701233A (SCOM)
Description	CCS INST ARR1 05

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_05_IDLES: The number of idle cycles before issuing the next command.
16:31	RW	CCS_INST_ARR1_05_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_05_READ_OR_WRITE_DATA: This is write data [0:19] if a write command is coded up, or a read compare byte if a read command is coded up. (Each bit represents a nibble of data.)
52	RW	CCS_INST_ARR1_05_READ_COMPARE_REQUIRED: Set to 1b if this command is a read and requires a data compare.
53:56	RW	CCS_INST_ARR1_05_DDR_CAL_RANK:DDR rank address [0:3] to calibrate.
57	RW	CCS_INST_ARR1_05_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0.
58	RW	CCS_INST_ARR1_05_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_05_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, go to this command number next (after the repeat count has expired).

Register Name	CCS INST ARR1 06 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR1_06
Address	000000000701233B (SCOM)
Description	CCS INST ARR1 06

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_06_IDLES: The number of idle cycles before issuing the next command.
16:31	RW	CCS_INST_ARR1_06_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_06_READ_OR_WRITE_DATA: This is write data [0:19] if a write command is coded up, or a read compare byte if a read command is coded up. (Each bit represents a nibble of data.)
52	RW	CCS_INST_ARR1_06_READ_COMPARE_REQUIRED: Set to 1b if this command is a read and requires a data compare.
53:56	RW	CCS_INST_ARR1_06_DDR_CAL_RANK:DDR rank address [0:3] to calibrate.

Bits	SCOM	Field Mnemonic: Description
57	RW	CCS_INST_ARR1_06_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0.
58	RW	CCS_INST_ARR1_06_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_06_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, go to this command number next (after the repeat count has expired).

Register Name	CCS INST ARR1 07 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR1_07
Address	000000000701233C (SCOM)
Description	CCS INST ARR1 07

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_07_IDLES: The number of idle cycles before issuing the next command.
16:31	RW	CCS_INST_ARR1_07_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_07_READ_OR_WRITE_DATA: This is write data [0:19] if a write command is coded up, or a read compare byte if a read command is coded up. (Each bit represents a nibble of data.)
52	RW	CCS_INST_ARR1_07_READ_COMPARE_REQUIRED: Set to 1b if this command is a read and requires a data compare.
53:56	RW	CCS_INST_ARR1_07_DDR_CAL_RANK:DDR rank address [0:3] to calibrate.
57	RW	CCS_INST_ARR1_07_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0.
58	RW	CCS_INST_ARR1_07_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_07_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, go to this command number next (after the repeat count has expired).

Register Name	CCS INST ARR1 08 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR1_08
Address	000000000701233D (SCOM)
Description	CCS INST ARR1 08

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_08_IDLES: The number of idle cycles before issuing the next command.
16:31	RW	CCS_INST_ARR1_08_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_08_READ_OR_WRITE_DATA: This is write data [0:19] if a write command is coded up, or a read compare byte if a read command is coded up. (Each bit represents a nibble of data.)
52	RW	CCS_INST_ARR1_08_READ_COMPARE_REQUIRED: Set to 1b if this command is a read and requires a data compare.
53:56	RW	CCS_INST_ARR1_08_DDR_CAL_RANK:DDR rank address [0:3] to calibrate.
57	RW	CCS_INST_ARR1_08_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0.
58	RW	CCS_INST_ARR1_08_CCS_END: Set to 1b if this is the last CCS command.

Bits	SCOM	Field Mnemonic: Description
59:63	RW	CCS_INST_ARR1_08_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, go to this command number next (after the repeat count has expired).

Register Name	CCS INST ARR1 09 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR1_09
Address	000000000701233E (SCOM)
Description	CCS INST ARR1 09

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_09_IDLES: The number of idle cycles before issuing the next command.
16:31	RW	CCS_INST_ARR1_09_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_09_READ_OR_WRITE_DATA: This is write data [0:19] if a write command is coded up, or a read compare byte if a read command is coded up. (Each bit represents a nibble of data.)
52	RW	CCS_INST_ARR1_09_READ_COMPARE_REQUIRED: Set to 1b if this command is a read and requires a data compare.
53:56	RW	CCS_INST_ARR1_09_DDR_CAL_RANK:DDR rank address [0:3] to calibrate.
57	RW	CCS_INST_ARR1_09_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0.
58	RW	CCS_INST_ARR1_09_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_09_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, go to this command number next (after the repeat count has expired).

Register Name	CCS INST ARR1 10 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR1_10
Address	000000000701233F (SCOM)
Description	CCS INST ARR1 10

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_10_IDLES: The number of idle cycles before issuing the next command.
16:31	RW	CCS_INST_ARR1_10_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_10_READ_OR_WRITE_DATA: This is write data [0:19] if a write command is coded up, or a read compare byte if a read command is coded up. (Each bit represents a nibble of data.)
52	RW	CCS_INST_ARR1_10_READ_COMPARE_REQUIRED: Set to 1b if this command is a read and requires a data compare.
53:56	RW	CCS_INST_ARR1_10_DDR_CAL_RANK:DDR rank address [0:3] to calibrate.
57	RW	CCS_INST_ARR1_10_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0.
58	RW	CCS_INST_ARR1_10_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_10_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, go to this command number next (after the repeat count has expired).

Register Name	CCS INST ARR1 11 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR1_11
Address	0000000007012340 (SCOM)
Description	CCS INST ARR1 11

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_11_IDLES: The number of idle cycles before issuing the next command.
16:31	RW	CCS_INST_ARR1_11_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_11_READ_OR_WRITE_DATA: This is write data [0:19] if a write command is coded up, or a read compare byte if a read command is coded up. (Each bit represents a nibble of data.)
52	RW	CCS_INST_ARR1_11_READ_COMPARE_REQUIRED: Set to 1b if this command is a read and requires a data compare.
53:56	RW	CCS_INST_ARR1_11_DDR_CAL_RANK:DDR rank address [0:3] to calibrate.
57	RW	CCS_INST_ARR1_11_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0.
58	RW	CCS_INST_ARR1_11_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_11_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, go to this command number next (after the repeat count has expired).

Register Name	CCS INST ARR1 12 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR1_12
Address	0000000007012341 (SCOM)
Description	CCS INST ARR1 12

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_12_IDLES: The number of idle cycles before issuing the next command.
16:31	RW	CCS_INST_ARR1_12_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_12_READ_OR_WRITE_DATA: This is write data [0:19] if a write command is coded up, or a read compare byte if a read command is coded up. (Each bit represents a nibble of data.)
52	RW	CCS_INST_ARR1_12_READ_COMPARE_REQUIRED: Set to 1b if this command is a read and requires a data compare.
53:56	RW	CCS_INST_ARR1_12_DDR_CAL_RANK:DDR rank address [0:3] to calibrate.
57	RW	CCS_INST_ARR1_12_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0.
58	RW	CCS_INST_ARR1_12_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_12_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, go to this command number next (after the repeat count has expired).

Register Name	CCS INST ARR1 13 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR1_13
Address	0000000007012342 (SCOM)
Description	CCS INST ARR1 13

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_13_IDLES: The number of idle cycles before issuing the next command.
16:31	RW	CCS_INST_ARR1_13_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_13_READ_OR_WRITE_DATA: This is write data [0:19] if a write command is coded up, or a read compare byte if a read command is coded up. (Each bit represents a nibble of data.)
52	RW	CCS_INST_ARR1_13_READ_COMPARE_REQUIRED: Set to 1b if this command is a read and requires a data compare.
53:56	RW	CCS_INST_ARR1_13_DDR_CAL_RANK:DDR rank address [0:3] to calibrate.
57	RW	CCS_INST_ARR1_13_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0.
58	RW	CCS_INST_ARR1_13_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_13_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, go to this command number next (after the repeat count has expired).

Register Name	**CCS INST ARR1 14 Register**
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR1_14
Address	0000000007012343 (SCOM)
Description	CCS INST ARR1 14

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_14_IDLES: The number of idle cycles before issuing the next command.
16:31	RW	CCS_INST_ARR1_14_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_14_READ_OR_WRITE_DATA: This is write data [0:19] if a write command is coded up, or a read compare byte if a read command is coded up. (Each bit represents a nibble of data.)
52	RW	CCS_INST_ARR1_14_READ_COMPARE_REQUIRED: Set to 1b if this command is a read and requires a data compare.
53:56	RW	CCS_INST_ARR1_14_DDR_CAL_RANK:DDR rank address [0:3] to calibrate.
57	RW	CCS_INST_ARR1_14_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0.
58	RW	CCS_INST_ARR1_14_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_14_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, go to this command number next (after the repeat count has expired).

Register Name	**CCS INST ARR1 15 Register**
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR1_15
Address	0000000007012344 (SCOM)
Description	CCS INST ARR1 15

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_15_IDLES: The number of idle cycles before issuing the next command.
16:31	RW	CCS_INST_ARR1_15_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_15_READ_OR_WRITE_DATA: This is write data [0:19] if a write command is coded up, or a read compare byte if a read command is coded up. (Each bit represents a nibble of data.)

Bits	SCOM	Field Mnemonic: Description
52	RW	CCS_INST_ARR1_15_READ_COMPARE_REQUIRED: Set to 1b if this command is a read and requires a data compare.
53:56	RW	CCS_INST_ARR1_15_DDR_CAL_RANK:DDR rank address [0:3] to calibrate.
57	RW	CCS_INST_ARR1_15_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0.
58	RW	CCS_INST_ARR1_15_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_15_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, go to this command number next (after the repeat count has expired).

Register Name	CCS INST ARR1 16 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR1_16
Address	0000000007012345 (SCOM)
Description	CCS INST ARR1 16

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_16_IDLES: The number of idle cycles before issuing the next command.
16:31	RW	CCS_INST_ARR1_16_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_16_READ_OR_WRITE_DATA: This is write data [0:19] if a write command is coded up, or a read compare byte if a read command is coded up. (Each bit represents a nibble of data.)
52	RW	CCS_INST_ARR1_16_READ_COMPARE_REQUIRED: Set to 1b if this command is a read and requires a data compare.
53:56	RW	CCS_INST_ARR1_16_DDR_CAL_RANK:DDR rank address [0:3] to calibrate.
57	RW	CCS_INST_ARR1_16_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0.
58	RW	CCS_INST_ARR1_16_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_16_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, go to this command number next (after the repeat count has expired).

Register Name	CCS INST ARR1 17 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR1_17
Address	0000000007012346 (SCOM)
Description	CCS INST ARR1 17

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_17_IDLES: The number of idle cycles before issuing the next command.
16:31	RW	CCS_INST_ARR1_17_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_17_READ_OR_WRITE_DATA: This is write data [0:19] if a write command is coded up, or a read compare byte if a read command is coded up. (Each bit represents a nibble of data.)
52	RW	CCS_INST_ARR1_17_READ_COMPARE_REQUIRED: Set to 1b if this command is a read and requires a data compare.
53:56	RW	CCS_INST_ARR1_17_DDR_CAL_RANK:DDR rank address [0:3] to calibrate.

Bits	SCOM	Field Mnemonic: Description
57	RW	CCS_INST_ARR1_17_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0.
58	RW	CCS_INST_ARR1_17_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_17_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, go to this command number next (after the repeat count has expired).

Register Name	CCS INST ARR1 18 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR1_18
Address	0000000007012347 (SCOM)
Description	CCS INST ARR1 18

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_18_IDLES: The number of idle cycles before issuing the next command.
16:31	RW	CCS_INST_ARR1_18_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_18_READ_OR_WRITE_DATA: This is write data [0:19] if a write command is coded up, or a read compare byte if a read command is coded up. (Each bit represents a nibble of data.)
52	RW	CCS_INST_ARR1_18_READ_COMPARE_REQUIRED: Set to 1b if this command is a read and requires a data compare.
53:56	RW	CCS_INST_ARR1_18_DDR_CAL_RANK:DDR rank address [0:3] to calibrate.
57	RW	CCS_INST_ARR1_18_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0.
58	RW	CCS_INST_ARR1_18_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_18_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, go to this command number next (after the repeat count has expired).

Register Name	CCS INST ARR1 19 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR1_19
Address	0000000007012348 (SCOM)
Description	CCS INST ARR1 19

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_19_IDLES: The number of idle cycles before issuing the next command.
16:31	RW	CCS_INST_ARR1_19_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_19_READ_OR_WRITE_DATA: This is write data [0:19] if a write command is coded up, or a read compare byte if a read command is coded up. (Each bit represents a nibble of data.)
52	RW	CCS_INST_ARR1_19_READ_COMPARE_REQUIRED: Set to 1b if this command is a read and requires a data compare.
53:56	RW	CCS_INST_ARR1_19_DDR_CAL_RANK:DDR rank address [0:3] to calibrate.
57	RW	CCS_INST_ARR1_19_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0.
58	RW	CCS_INST_ARR1_19_CCS_END: Set to 1b if this is the last CCS command.

Bits	SCOM	Field Mnemonic: Description
59:63	RW	CCS_INST_ARR1_19_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, go to this command number next (after the repeat count has expired).

Register Name	CCS INST ARR1 20 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR1_20
Address	0000000007012349 (SCOM)
Description	CCS INST ARR1 20

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_20_IDLES: The number of idle cycles before issuing the next command.
16:31	RW	CCS_INST_ARR1_20_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_20_READ_OR_WRITE_DATA: This is write data [0:19] if a write command is coded up, or a read compare byte if a read command is coded up. (Each bit represents a nibble of data.)
52	RW	CCS_INST_ARR1_20_READ_COMPARE_REQUIRED: Set to 1b if this command is a read and requires a data compare.
53:56	RW	CCS_INST_ARR1_20_DDR_CAL_RANK:DDR rank address [0:3] to calibrate.
57	RW	CCS_INST_ARR1_20_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0.
58	RW	CCS_INST_ARR1_20_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_20_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, go to this command number next (after the repeat count has expired).

Register Name	CCS INST ARR1 21 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR1_21
Address	000000000701234A (SCOM)
Description	CCS INST ARR1 21

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_21_IDLES: The number of idle cycles before issuing the next command.
16:31	RW	CCS_INST_ARR1_21_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_21_READ_OR_WRITE_DATA: This is write data [0:19] if a write command is coded up, or a read compare byte if a read command is coded up. (Each bit represents a nibble of data.)
52	RW	CCS_INST_ARR1_21_READ_COMPARE_REQUIRED: Set to 1b if this command is a read and requires a data compare.
53:56	RW	CCS_INST_ARR1_21_DDR_CAL_RANK:DDR rank address [0:3] to calibrate.
57	RW	CCS_INST_ARR1_21_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0.
58	RW	CCS_INST_ARR1_21_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_21_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, go to this command number next (after the repeat count has expired).

Register Name	CCS INST ARR1 22 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR1_22
Address	000000000701234B (SCOM)
Description	CCS INST ARR1 22

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_22_IDLES: The number of idle cycles before issuing the next command.
16:31	RW	CCS_INST_ARR1_22_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_22_READ_OR_WRITE_DATA: This is write data [0:19] if a write command is coded up, or a read compare byte if a read command is coded up. (Each bit represents a nibble of data.)
52	RW	CCS_INST_ARR1_22_READ_COMPARE_REQUIRED: Set to 1b if this command is a read and requires a data compare.
53:56	RW	CCS_INST_ARR1_22_DDR_CAL_RANK:DDR rank address [0:3] to calibrate.
57	RW	CCS_INST_ARR1_22_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0.
58	RW	CCS_INST_ARR1_22_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_22_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, go to this command number next (after the repeat count has expired).

Register Name	CCS INST ARR1 23 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR1_23
Address	000000000701234C (SCOM)
Description	CCS INST ARR1 23

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_23_IDLES: The number of idle cycles before issuing the next command.
16:31	RW	CCS_INST_ARR1_23_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_23_READ_OR_WRITE_DATA: This is write data [0:19] if a write command is coded up, or a read compare byte if a read command is coded up. (Each bit represents a nibble of data.)
52	RW	CCS_INST_ARR1_23_READ_COMPARE_REQUIRED: Set to 1b if this command is a read and requires a data compare.
53:56	RW	CCS_INST_ARR1_23_DDR_CAL_RANK:DDR rank address [0:3] to calibrate.
57	RW	CCS_INST_ARR1_23_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0.
58	RW	CCS_INST_ARR1_23_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_23_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, go to this command number next (after the repeat count has expired).

Register Name	CCS INST ARR1 24 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR1_24
Address	000000000701234D (SCOM)
Description	CCS INST ARR1 24

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_24_IDLES: The number of idle cycles before issuing the next command.
16:31	RW	CCS_INST_ARR1_24_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_24_READ_OR_WRITE_DATA: This is write data [0:19] if a write command is coded up, or a read compare byte if a read command is coded up. (Each bit represents a nibble of data.)
52	RW	CCS_INST_ARR1_24_READ_COMPARE_REQUIRED: Set to 1b if this command is a read and requires a data compare.
53:56	RW	CCS_INST_ARR1_24_DDR_CAL_RANK:DDR rank address [0:3] to calibrate.
57	RW	CCS_INST_ARR1_24_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0.
58	RW	CCS_INST_ARR1_24_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_24_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, go to this command number next (after the repeat count has expired).

Register Name	CCS INST ARR1 25 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR1_25
Address	000000000701234E (SCOM)
Description	CCS INST ARR1 25

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_25_IDLES: The number of idle cycles before issuing the next command.
16:31	RW	CCS_INST_ARR1_25_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_25_READ_OR_WRITE_DATA: This is write data [0:19] if a write command is coded up, or a read compare byte if a read command is coded up. (Each bit represents a nibble of data.)
52	RW	CCS_INST_ARR1_25_READ_COMPARE_REQUIRED: Set to 1b if this command is a read and requires a data compare.
53:56	RW	CCS_INST_ARR1_25_DDR_CAL_RANK:DDR rank address [0:3] to calibrate.
57	RW	CCS_INST_ARR1_25_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0.
58	RW	CCS_INST_ARR1_25_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_25_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, go to this command number next (after the repeat count has expired).

Register Name	CCS INST ARR1 26 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR1_26
Address	000000000701234F (SCOM)
Description	CCS INST ARR1 26

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_26_IDLES: The number of idle cycles before issuing the next command.
16:31	RW	CCS_INST_ARR1_26_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_26_READ_OR_WRITE_DATA: This is write data [0:19] if a write command is coded up, or a read compare byte if a read command is coded up. (Each bit represents a nibble of data.)

Bits	SCOM	Field Mnemonic: Description
52	RW	CCS_INST_ARR1_26_READ_COMPARE_REQUIRED: Set to 1b if this command is a read and requires a data compare.
53:56	RW	CCS_INST_ARR1_26_DDR_CAL_RANK:DDR rank address [0:3] to calibrate.
57	RW	CCS_INST_ARR1_26_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0.
58	RW	CCS_INST_ARR1_26_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_26_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, go to this command number next (after the repeat count has expired).

Register Name	CCS INST ARR1 27 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR1_27
Address	0000000007012350 (SCOM)
Description	CCS INST ARR1 27

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_27_IDLES: The number of idle cycles before issuing the next command.
16:31	RW	CCS_INST_ARR1_27_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_27_READ_OR_WRITE_DATA: This is write data [0:19] if a write command is coded up, or a read compare byte if a read command is coded up. (Each bit represents a nibble of data.)
52	RW	CCS_INST_ARR1_27_READ_COMPARE_REQUIRED: Set to 1b if this command is a read and requires a data compare.
53:56	RW	CCS_INST_ARR1_27_DDR_CAL_RANK:DDR rank address [0:3] to calibrate.
57	RW	CCS_INST_ARR1_27_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0.
58	RW	CCS_INST_ARR1_27_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_27_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, go to this command number next (after the repeat count has expired).

Register Name	CCS INST ARR1 28 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR1_28
Address	0000000007012351 (SCOM)
Description	CCS INST ARR1 28

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_28_IDLES: The number of idle cycles before issuing the next command.
16:31	RW	CCS_INST_ARR1_28_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_28_READ_OR_WRITE_DATA: This is write data [0:19] if a write command is coded up, or a read compare byte if a read command is coded up. (Each bit represents a nibble of data.)
52	RW	CCS_INST_ARR1_28_READ_COMPARE_REQUIRED: Set to 1b if this command is a read and requires a data compare.
53:56	RW	CCS_INST_ARR1_28_DDR_CAL_RANK:DDR rank address [0:3] to calibrate.

Bits	SCOM	Field Mnemonic: Description
57	RW	CCS_INST_ARR1_28_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0.
58	RW	CCS_INST_ARR1_28_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_28_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, go to this command number next (after the repeat count has expired).

Register Name	CCS INST ARR1 29 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR1_29
Address	0000000007012352 (SCOM)
Description	CCS INST ARR1 29

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_29_IDLES: The number of idle cycles before issuing the next command.
16:31	RW	CCS_INST_ARR1_29_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_29_READ_OR_WRITE_DATA: This is write data [0:19] if a write command is coded up, or a read compare byte if a read command is coded up. (Each bit represents a nibble of data.)
52	RW	CCS_INST_ARR1_29_READ_COMPARE_REQUIRED: Set to 1b if this command is a read and requires a data compare.
53:56	RW	CCS_INST_ARR1_29_DDR_CAL_RANK:DDR rank address [0:3] to calibrate.
57	RW	CCS_INST_ARR1_29_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0.
58	RW	CCS_INST_ARR1_29_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_29_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, go to this command number next (after the repeat count has expired).

Register Name	CCS INST ARR1 30 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR1_30
Address	0000000007012353 (SCOM)
Description	CCS INST ARR1 30

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_30_IDLES: The number of idle cycles before issuing the next command.
16:31	RW	CCS_INST_ARR1_30_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_30_READ_OR_WRITE_DATA: This is write data [0:19] if a write command is coded up, or a read compare byte if a read command is coded up. (Each bit represents a nibble of data.)
52	RW	CCS_INST_ARR1_30_READ_COMPARE_REQUIRED: Set to 1b if this command is a read and requires a data compare.
53:56	RW	CCS_INST_ARR1_30_DDR_CAL_RANK:DDR rank address [0:3] to calibrate.
57	RW	CCS_INST_ARR1_30_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0.
58	RW	CCS_INST_ARR1_30_CCS_END: Set to 1b if this is the last CCS command.

Bits	SCOM	Field Mnemonic: Description
59:63	RW	CCS_INST_ARR1_30_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, go to this command number next (after the repeat count has expired).

Register Name	CCS INST ARR1 31 Register
Mnemonic	MC01.MCBIST.CCS.CCS_INST_ARR1_31
Address	0000000007012354 (SCOM)
Description	CCS INST ARR1 31

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_31_IDLES: The number of idle cycles before issuing the next command.
16:31	RW	CCS_INST_ARR1_31_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_31_READ_OR_WRITE_DATA: This is write data [0:19] if a write command is coded up, or a read compare byte if a read command is coded up. (Each bit represents a nibble of data.)
52	RW	CCS_INST_ARR1_31_READ_COMPARE_REQUIRED: Set to 1b if this command is a read and requires a data compare.
53:56	RW	CCS_INST_ARR1_31_DDR_CAL_RANK:DDR rank address [0:3] to calibrate.
57	RW	CCS_INST_ARR1_31_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0.
58	RW	CCS_INST_ARR1_31_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_31_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, go to this command number next (after the repeat count has expired).

Register Name	MBS Memory Scrub/Read Error Count Register 0
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MBSEC0Q
Address	0000000007012355 (SCOM)
Description	MBS Memory Scrub/Read Error Count Register 0

Bits	SCOM	Field Mnemonic: Description
0:11	RWX	MBSEC0Q_INTERMITTENT_CE_COUNT: Intermittent CE count. This is a 12-bit count of intermittent CE events. It freezes its value upon incrementing to the maximum value until reset.
12:23	RWX	MBSEC0Q_SOFT_CE_COUNT: Soft CE count. This is a 12-bit count of soft CE events. It freezes its value upon incrementing to the maximum value until reset.
24:35	RWX	MBSEC0Q_HARD_CE_COUNT: Hard CE count. This is a 12-bit count of hard CE events. It freezes its value upon incrementing to the maximum value until reset.
36:47	RWX	MBSEC0Q_INTERMITTENT_MCE_COUNT: Intermittent MCE count. This is a 12-bit count of Intermittent Marked Chip Correctable Error events. It freezes its value upon incrementing to the maximum value until reset.
48:59	RWX	MBSEC0Q_SOFT_MCE_COUNT: Soft MCE Count This is a 12-bit count of Soft Marked Chip Correctable Error events. It freezes its value upon incrementing to the maximum value until reset.
60:63	RO	Constant = 0b0000

Register Name	MBS Memory Scrub/Read Error Count Register 1
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MBSEC1Q
Address	0000000007012356 (SCOM)
Description	MBS Memory Scrub/Read Error Count Register 1

Bits	SCOM	Field Mnemonic: Description
0:11	RWX	MBSEC1Q_HARD_MCE_COUNT: Hard MCE count. This is a 12-bit count of Hard Marked Chip Correctable Error events. It freezes its value upon incrementing to the maximum value until reset.
12:23	RWX	MBSEC1Q_ICE_COUNT: ICE (IMPE) count. This is a 12-bit count of Intermittent Marked-Placed Chip Error events. It freezes its value upon incrementing to the maximum value until reset.
24:35	RWX	MBSEC1Q_UE_COUNT: UE count. This is a 12-bit count of Uncorrectable Error events. It freezes its value upon incrementing to the maximum value until reset.
36:47	RWX	MBSEC1Q_AUE: AUE count. This is a 12-bit count of AUE Parity Error events. It freezes its value upon incrementing to the maximum value until reset.
48:59	RWX	MBSEC1Q_RCE_COUNT: RCE count. This is a 12-bit count of Retried Correctable Error events. It freezes its value upon incrementing to the maximum value until reset.
60:63	RO	Constant = 0b0000

Register Name	MBS Memory Scrub/Read Error Threshold Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MBSTRQ
Address	0000000007012357 (SCOM)
Description	MBS Memory Scrub/Read Error Threshold Register

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MBSTRQ_CFG_THRESH_MAG_NCE_INT: NCE intermittent error threshold magnitude that triggers a pause. If 1111, the pause is never triggered (disabled). Otherwise, the MCBIST pauses if it sees $2^{[\text{this value}]}$ number of errors of this type.
4:7	RW	MBSTRQ_CFG_THRESH_MAG_NCE_SOFT: NCE soft error threshold magnitude that triggers a pause. If 1111, the pause is never triggered (disabled). Otherwise, the MCBIST pauses if it sees $2^{[\text{this value}]}$ number of errors of this type.
8:11	RW	MBSTRQ_CFG_THRESH_MAG_NCE_HARD: NCE hard error threshold magnitude that triggers a pause. If 1111, the pause is never triggered (disabled). Otherwise, the MCBIST pauses if it sees $2^{[\text{this value}]}$ number of errors of this type.
12:15	RW	MBSTRQ_CFG_THRESH_MAG_RCE: RCE error threshold magnitude that triggers a pause. If 1111, the pause is never triggered (disabled). Otherwise, the MCBIST pauses if it sees $2^{[\text{this value}]}$ number of errors of this type.
16:19	RW	MBSTRQ_CFG_THRESH_MAG_ICE: ICE (IMPE) error threshold magnitude that triggers a pause. If 1111, the pause is never triggered (disabled). Otherwise, the MCBIST pauses if it sees $2^{[\text{this value}]}$ number of errors of this type.
20:23	RW	MBSTRQ_CFG_THRESH_MAG_MCE_INT: MCE intermittent error threshold magnitude that triggers a pause. If 1111, the pause is never triggered (disabled). Otherwise, the MCBIST pauses if it sees $2^{[\text{this value}]}$ number of errors of this type.
24:27	RW	MBSTRQ_CFG_THRESH_MAG_MCE_SOFT: MCE soft error threshold magnitude that triggers a pause. If 1111, the pause is never triggered (disabled). Otherwise, the MCBIST pauses if it sees $2^{[\text{this value}]}$ number of errors of this type.

Bits	SCOM	Field Mnemonic: Description
28:31	RW	MBSTRQ_CFG_THRESH_MAG_MCE_HARD: MCE hard error threshold magnitude that triggers a pause. If 1111, the pause is never triggered (disabled). Otherwise, the MCBIST pauses if it sees $2^{[\text{this value}]}$ number of errors of this type.
32	RW	MBSTRQ_CFG_PAUSE_ON_SCE: Enable pause on an SCE error. When enabled, the MCBIST pauses at the boundary configured if this error is seen.
33	RW	MBSTRQ_RESERVED_33: Reserved.
34	RW	MBSTRQ_CFG_PAUSE_ON_MPE: Enable a pause on an MPE error. When enabled, the MCBIST pauses at the boundary configured if this error is seen.
35	RW	MBSTRQ_CFG_PAUSE_ON_UE: Enable a pause on a UE. When enabled, the MCBIST pauses at the boundary configured if this error is seen.
36	RW	MBSTRQ_CFG_PAUSE_ON_SUE: Enable a pause on an SUE. When enabled, the MCBIST pauses at the boundary configured if this error is seen.
37	RW	MBSTRQ_CFG_PAUSE_ON_AUE: Enable a pause on an AUE. When enabled, the MCBIST pauses at the boundary configured if this error is seen.
38	RW	MBSTRQ_CFG_PAUSE_ON_RCD: Enable a pause on an RCD error. When enabled, the MCBIST pauses at the boundary configured if this error is seen.
39:52	RW	MBSTRQ_RESERVE_39_52: Reserved.
53:54	RW	MBSTRQ_CFG_SYMBOL_COUNTER_MODE: Selects which mode to use symbol counter latches: Mode 0: Maintenance 8-bit error counters for of 72 symbols Mode 1: MCBIST 4-bit error counters for 18 nibbles x 8 ranks (port agnostic) Mode 2: MCBIST 4-bit error counters for 18 nibbles x 4 ports (rank agnostic) and 1-bit error rank map for 18 nibbles x 4 ports
55	RW	MBSTRQ_CFG_NCE_SOFT_SYMBOL_COUNT_ENABLE: Enables soft NCEs to trigger per-symbol NCE error counting. Only applies to scrub where we have different types of NCE. Nonscrub counts all NCE.
56	RW	MBSTRQ_CFG_NCE_INTER_SYMBOL_COUNT_ENABLE: Enables intermittent NCEs to trigger per-symbol NCE error counting. Only applies to scrub where we have different types of NCE. Nonscrub counts all NCE.
57	RW	MBSTRQ_CFG_NCE_HARD_SYMBOL_COUNT_ENABLE: Enables hard NCEs to trigger per-symbol NCE error counting. Only applies to scrub where we have different types of NCE. Nonscrub counts all NCE.
58	RW	MBSTRQ_CFG_PAUSE_MCB_ERROR: Enable a pause when an MCBIST error is logged. When enabled, the MCBIST pauses at the boundary configured if this error is seen.
59	RW	MBSTRQ_CFG_PAUSE_MCB_LOG_FULL: Enable a pause when the MCBIST log is full. When enabled, the MCBIST pauses at the boundary configured if this error is seen.
60	RW	MBSTRQ_CFG_MAINT_RCE_WITH_CE: cfg_maint_rce_with_ce. Not implemented.
61	RW	MBSTRQ_CFG_MCE_SOFT_SYMBOL_COUNT_ENABLE: Enables soft MCEs to trigger per-symbol MCE error counting. Only applies to scrub where we have different types of MCE. Nonscrub counts all MCE.
62	RW	MBSTRQ_CFG_MCE_INTER_SYMBOL_COUNT_ENABLE: Enables intermittent MCEs to trigger per-symbol MCE error counting. Only applies to scrub where we have different types of MCE. Nonscrub counts all MCE.
63	RW	MBSTRQ_CFG_MCE_HARD_SYMBOL_COUNT_ENABLE: Enables hard MCEs to trigger per-symbol MCE error counting. Only applies to scrub where we have different types of MCE. Nonscrub counts all MCE.

Register Name	**MCBIST Modal Symbol Counter Register 0**
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MBSSYMEC0Q
Address	0000000007012358 (SCOM)
Description	MCBIST Modal Symbol Counter Register 0

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBSSYMEC0Q_MODAL_SYMBOL_COUNTER_00: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 00 if 01, 0:3 = MCBIST error counter for nibble 00 and rank 0 4:7 = MCBIST error counter for nibble 00 and rank 1 if 10, 0:3 = MCBIST error counter for port 0 and nibble 00 4:7 = MCBIST error rank map for port 0 and nibble 00
8:15	RWX	MBSSYMEC0Q_MODAL_SYMBOL_COUNTER_01: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 01 if 01, 0:3 = MCBIST error counter for nibble 00 and rank 2 4:7 = MCBIST error counter for nibble 00 and rank 3 if 10, 0:3 = MCBIST error counter for port 0 and nibble 01 4:7 = MCBIST error rank map for port 0 and nibble 01
16:23	RWX	MBSSYMEC0Q_MODAL_SYMBOL_COUNTER_02: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 02 if 01, 0:3 = MCBIST error counter for nibble 00 and rank 4 4:7 = MCBIST error counter for nibble 00 and rank 5 if 10, 0:3 = MCBIST error counter for port 0 and nibble 02 4:7 = MCBIST error rank map for port 0 and nibble 02
24:31	RWX	MBSSYMEC0Q_MODAL_SYMBOL_COUNTER_03: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 03 if 01, 0:3 = MCBIST error counter for nibble 00 and rank 6 4:7 = MCBIST error counter for nibble 00 and rank 7 if 10, 0:3 = MCBIST error counter for port 0 and nibble 03 4:7 = MCBIST error rank map for port 0 and nibble 03
32:39	RWX	MBSSYMEC0Q_MODAL_SYMBOL_COUNTER_04: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 04 if 01, 0:3 = MCBIST error counter for nibble 01 and rank 0 4:7 = MCBIST error counter for nibble 01 and rank 1 if 10, 0:3 = MCBIST error counter for port 0 and nibble 04 4:7 = MCBIST error rank map for port 0 and nibble 04
40:47	RWX	MBSSYMEC0Q_MODAL_SYMBOL_COUNTER_05: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 05 if 01, 0:3 = MCBIST error counter for nibble 01 and rank 2 4:7 = MCBIST error counter for nibble 01 and rank 3 if 10, 0:3 = MCBIST error counter for port 0 and nibble 05 4:7 = MCBIST error rank map for port 0 and nibble 05
48:55	RWX	MBSSYMEC0Q_MODAL_SYMBOL_COUNTER_06: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 06 if 01, 0:3 = MCBIST error counter for nibble 01 and rank 4 4:7 = MCBIST error counter for nibble 01 and rank 5 if 10, 0:3 = MCBIST error counter for port 0 and nibble 06 4:7 = MCBIST error rank map for port 0 and nibble 06
56:63	RWX	MBSSYMEC0Q_MODAL_SYMBOL_COUNTER_07: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 07 if 01, 0:3 = MCBIST error counter for nibble 01 and rank 6 4:7 = MCBIST error counter for nibble 01 and rank 7 if 10, 0:3 = MCBIST error counter for port 0 and nibble 07 4:7 = MCBIST error rank map for port 0 and nibble 07

Register Name	MCBIST Modal Symbol Counter Register 1
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MBSSYMEC1Q
Address	0000000007012359 (SCOM)
Description	MCBIST Modal Symbol Counter Register 1

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBSSYMEC1Q_MODAL_SYMBOL_COUNTER_08: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 08 if 01, 0:3 = MCBIST error counter for nibble 02 and rank 0 4:7 = MCBIST error counter for nibble 02 and rank 1 if 10, 0:3 = MCBIST error counter for port 0 and nibble 08 4:7 = MCBIST error rank map for port 0 and nibble 08
8:15	RWX	MBSSYMEC1Q_MODAL_SYMBOL_COUNTER_09: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 09 if 01, 0:3 = MCBIST error counter for nibble 02 and rank 2 4:7 = MCBIST error counter for nibble 02 and rank 3 if 10, 0:3 = MCBIST error counter for port 0 and nibble 09 4:7 = MCBIST error rank map for port 0 and nibble 09
16:23	RWX	MBSSYMEC1Q_MODAL_SYMBOL_COUNTER_10: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 10 if 01, 0:3 = MCBIST error counter for nibble 02 and rank 4 4:7 = MCBIST error counter for nibble 02 and rank 5 if 10, 0:3 = MCBIST error counter for port 0 and nibble 10 4:7 = MCBIST error rank map for port 0 and nibble 10
24:31	RWX	MBSSYMEC1Q_MODAL_SYMBOL_COUNTER_11: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 11 if 01, 0:3 = MCBIST error counter for nibble 02 and rank 6 4:7 = MCBIST error counter for nibble 02 and rank 7 if 10, 0:3 = MCBIST error counter for port 0 and nibble 11 4:7 = MCBIST error rank map for port 0 and nibble 11
32:39	RWX	MBSSYMEC1Q_MODAL_SYMBOL_COUNTER_12: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 12 if 01, 0:3 = MCBIST error counter for nibble 03 and rank 0 4:7 = MCBIST error counter for nibble 03 and rank 1 if 10, 0:3 = MCBIST error counter for port 0 and nibble 12 4:7 = MCBIST error rank map for port 0 and nibble 12
40:47	RWX	MBSSYMEC1Q_MODAL_SYMBOL_COUNTER_13: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 13 if 01, 0:3 = MCBIST error counter for nibble 03 and rank 2 4:7 = MCBIST error counter for nibble 03 and rank 3 if 10, 0:3 = MCBIST error counter for port 0 and nibble 13 4:7 = MCBIST error rank map for port 0 and nibble 13

Bits	SCOM	Field Mnemonic: Description
48:55	RWX	MBSSYMEC1Q_MODAL_SYMBOL_COUNTER_14: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 14 if 01, 0:3 = MCBIST error counter for nibble 03 and rank 4 4:7 = MCBIST error counter for nibble 03 and rank 5 if 10, 0:3 = MCBIST error counter for port 0 and nibble 14 4:7 = MCBIST error rank map for port 0 and nibble 14
56:63	RWX	MBSSYMEC1Q_MODAL_SYMBOL_COUNTER_15: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 15 if 01, 0:3 = MCBIST error counter for nibble 03 and rank 6 4:7 = MCBIST error counter for nibble 03 and rank 7 if 10, 0:3 = MCBIST error counter for port 0 and nibble 15 4:7 = MCBIST error rank map for port 0 and nibble 15

Register Name	MCBIST Modal Symbol Counter Register 2
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MBSSYMEC2Q
Address	000000000701235A (SCOM)
Description	MCBIST Modal Symbol Counter Register 2

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBSSYMEC2Q_MODAL_SYMBOL_COUNTER_16: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 16 if 01, 0:3 = MCBIST error counter for nibble 04 and rank 0 4:7 = MCBIST error counter for nibble 04 and rank 1 if 10, 0:3 = MCBIST error counter for port 0 and nibble 16 4:7 = MCBIST error rank map for port 0 and nibble 16
8:15	RWX	MBSSYMEC2Q_MODAL_SYMBOL_COUNTER_17: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 17 if 01, 0:3 = MCBIST error counter for nibble 04 and rank 2 4:7 = MCBIST error counter for nibble 04 and rank 3 if 10, 0:3 = MCBIST error counter for port 0 and nibble 17 4:7 = MCBIST error rank map for port 0 and nibble 17
16:23	RWX	MBSSYMEC2Q_MODAL_SYMBOL_COUNTER_18: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 18 if 01, 0:3 = MCBIST error counter for nibble 04 and rank 4 4:7 = MCBIST error counter for nibble 04 and rank 5 if 10, 0:3 = MCBIST error counter for port 1 and nibble 00 4:7 = MCBIST error rank map for port 1 and nibble 00
24:31	RWX	MBSSYMEC2Q_MODAL_SYMBOL_COUNTER_19: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 19 if 01, 0:3 = MCBIST error counter for nibble 04 and rank 6 4:7 = MCBIST error counter for nibble 04 and rank 7 if 10, 0:3 = MCBIST error counter for port 1 and nibble 01 4:7 = MCBIST error rank map for port 1 and nibble 01

Bits	SCOM	Field Mnemonic: Description
32:39	RWX	MBSSYMEC2Q_MODAL_SYMBOL_COUNTER_20: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 20 if 01, 0:3 = MCBIST error counter for nibble 05 and rank 0 4:7 = MCBIST error counter for nibble 05 and rank 1 if 10, 0:3 = MCBIST error counter for port 1 and nibble 02 4:7 = MCBIST error rank map for port 1 and nibble 02
40:47	RWX	MBSSYMEC2Q_MODAL_SYMBOL_COUNTER_21: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 21 if 01, 0:3 = MCBIST error counter for nibble 05 and rank 2 4:7 = MCBIST error counter for nibble 05 and rank 3 if 10, 0:3 = MCBIST error counter for port 1 and nibble 03 4:7 = MCBIST error rank map for port 1 and nibble 03
48:55	RWX	MBSSYMEC2Q_MODAL_SYMBOL_COUNTER_22: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 22 if 01, 0:3 = MCBIST error counter for nibble 05 and rank 4 4:7 = MCBIST error counter for nibble 05 and rank 5 if 10, 0:3 = MCBIST error counter for port 1 and nibble 04 4:7 = MCBIST error rank map for port 1 and nibble 04
56:63	RWX	MBSSYMEC2Q_MODAL_SYMBOL_COUNTER_23: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 23 if 01, 0:3 = MCBIST error counter for nibble 05 and rank 6 4:7 = MCBIST error counter for nibble 05 and rank 7 if 10, 0:3 = MCBIST error counter for port 1 and nibble 05 4:7 = MCBIST error rank map for port 1 and nibble 05

Register Name	**MCBIST Modal Symbol Counter Register 3**
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MBSSYMEC3Q
Address	000000000701235B (SCOM)
Description	MCBIST Modal Symbol Counter Register 3

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBSSYMEC3Q_MODAL_SYMBOL_COUNTER_24: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 24 if 01, 0:3 = MCBIST error counter for nibble 06 and rank 0 4:7 = MCBIST error counter for nibble 06 and rank 1 if 10, 0:3 = MCBIST error counter for port 1 and nibble 06 4:7 = MCBIST error rank map for port 1 and nibble 06
8:15	RWX	MBSSYMEC3Q_MODAL_SYMBOL_COUNTER_25: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 25 if 01, 0:3 = MCBIST error counter for nibble 06 and rank 2 4:7 = MCBIST error counter for nibble 06 and rank 3 if 10, 0:3 = MCBIST error counter for port 1 and nibble 07 4:7 = MCBIST error rank map for port 1 and nibble 07

Bits	SCOM	Field Mnemonic: Description
16:23	RWX	MBSSYMEC3Q_MODAL_SYMBOL_COUNTER_26: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 26 if 01, 0:3 = MCBIST error counter for nibble 06 and rank 4 4:7 = MCBIST error counter for nibble 06 and rank 5 if 10, 0:3 = MCBIST error counter for port 1 and nibble 08 4:7 = MCBIST error rank map for port 1 and nibble 08
24:31	RWX	MBSSYMEC3Q_MODAL_SYMBOL_COUNTER_27: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 27 if 01, 0:3 = MCBIST error counter for nibble 06 and rank 6 4:7 = MCBIST error counter for nibble 06 and rank 7 if 10, 0:3 = MCBIST error counter for port 1 and nibble 09 4:7 = MCBIST error rank map for port 1 and nibble 09
32:39	RWX	MBSSYMEC3Q_MODAL_SYMBOL_COUNTER_28: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 28 if 01, 0:3 = MCBIST error counter for nibble 07 and rank 0 4:7 = MCBIST error counter for nibble 07 and rank 1 if 10, 0:3 = MCBIST error counter for port 1 and nibble 10 4:7 = MCBIST error rank map for port 1 and nibble 10
40:47	RWX	MBSSYMEC3Q_MODAL_SYMBOL_COUNTER_29: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 29 if 01, 0:3 = MCBIST error counter for nibble 07 and rank 2 4:7 = MCBIST error counter for nibble 07 and rank 3 if 10, 0:3 = MCBIST error counter for port 1 and nibble 11 4:7 = MCBIST error rank map for port 1 and nibble 11
48:55	RWX	MBSSYMEC3Q_MODAL_SYMBOL_COUNTER_30: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 30 if 01, 0:3 = MCBIST error counter for nibble 07 and rank 4 4:7 = MCBIST error counter for nibble 07 and rank 5 if 10, 0:3 = MCBIST error counter for port 1 and nibble 12 4:7 = MCBIST error rank map for port 1 and nibble 12
56:63	RWX	MBSSYMEC3Q_MODAL_SYMBOL_COUNTER_31: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 31 if 01, 0:3 = MCBIST error counter for nibble 07 and rank 6 4:7 = MCBIST error counter for nibble 07 and rank 7 if 10, 0:3 = MCBIST error counter for port 1 and nibble 13 4:7 = MCBIST error rank map for port 1 and nibble 13

Register Name	**MCBIST Modal Symbol Counter Register 4**
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MBSSYMEC4Q
Address	000000000701235C (SCOM)
Description	MCBIST Modal Symbol Counter Register 4

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBSSYMEC4Q_MODAL_SYMBOL_COUNTER_32: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 32 if 01, 0:3 = MCBIST error counter for nibble 08 and rank 0 4:7 = MCBIST error counter for nibble 08 and rank 1 if 10, 0:3 = MCBIST error counter for port 1 and nibble 14 4:7 = MCBIST error rank map for port 1 and nibble 14
8:15	RWX	MBSSYMEC4Q_MODAL_SYMBOL_COUNTER_33: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 33 if 01, 0:3 = MCBIST error counter for nibble 08 and rank 2 4:7 = MCBIST error counter for nibble 08 and rank 3 if 10, 0:3 = MCBIST error counter for port 1 and nibble 15 4:7 = MCBIST error rank map for port 1 and nibble 15
16:23	RWX	MBSSYMEC4Q_MODAL_SYMBOL_COUNTER_34: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 34 if 01, 0:3 = MCBIST error counter for nibble 08 and rank 4 4:7 = MCBIST error counter for nibble 08 and rank 5 if 10, 0:3 = MCBIST error counter for port 1 and nibble 16 4:7 = MCBIST error rank map for port 1 and nibble 16
24:31	RWX	MBSSYMEC4Q_MODAL_SYMBOL_COUNTER_35: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 35 if 01, 0:3 = MCBIST error counter for nibble 08 and rank 6 4:7 = MCBIST error counter for nibble 08 and rank 7 if 10, 0:3 = MCBIST error counter for port 1 and nibble 17 4:7 = MCBIST error rank map for port 1 and nibble 17
32:39	RWX	MBSSYMEC4Q_MODAL_SYMBOL_COUNTER_36: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 36 if 01, 0:3 = MCBIST error counter for nibble 09 and rank 0 4:7 = MCBIST error counter for nibble 09 and rank 1 if 10, 0:3 = MCBIST error counter for port 2 and nibble 00 4:7 = MCBIST error rank map for port 2 and nibble 00
40:47	RWX	MBSSYMEC4Q_MODAL_SYMBOL_COUNTER_37: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 37 if 01, 0:3 = MCBIST error counter for nibble 09 and rank 2 4:7 = MCBIST error counter for nibble 09 and rank 3 if 10, 0:3 = MCBIST error counter for port 2 and nibble 01 4:7 = MCBIST error rank map for port 2 and nibble 01
48:55	RWX	MBSSYMEC4Q_MODAL_SYMBOL_COUNTER_38: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 38 if 01, 0:3 = MCBIST error counter for nibble 09 and rank 4 4:7 = MCBIST error counter for nibble 09 and rank 5 if 10, 0:3 = MCBIST error counter for port 2 and nibble 02 4:7 = MCBIST error rank map for port 2 and nibble 02
56:63	RWX	MBSSYMEC4Q_MODAL_SYMBOL_COUNTER_39: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 39 if 01, 0:3 = MCBIST error counter for nibble 09 and rank 6 4:7 = MCBIST error counter for nibble 09 and rank 7 if 10, 0:3 = MCBIST error counter for port 2 and nibble 03 4:7 = MCBIST error rank map for port 2 and nibble 03

Register Name	**MCBIST Modal Symbol Counter Register 5**
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MBSSYMEC5Q
Address	000000000701235D (SCOM)
Description	MCBIST Modal Symbol Counter Register 5

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBSSYMEC5Q_MODAL_SYMBOL_COUNTER_40: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 40 if 01, 0:3 = MCBIST error counter for nibble 10 and rank 0 4:7 = MCBIST error counter for nibble 10 and rank 1 if 10, 0:3 = MCBIST error counter for port 2 and nibble 04 4:7 = MCBIST error rank map for port 2 and nibble 04
8:15	RWX	MBSSYMEC5Q_MODAL_SYMBOL_COUNTER_41: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 41 if 01, 0:3 = MCBIST error counter for nibble 10 and rank 2 4:7 = MCBIST error counter for nibble 10 and rank 3 if 10, 0:3 = MCBIST error counter for port 2 and nibble 05 4:7 = MCBIST error rank map for port 2 and nibble 05
16:23	RWX	MBSSYMEC5Q_MODAL_SYMBOL_COUNTER_42: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 42 if 01, 0:3 = MCBIST error counter for nibble 10 and rank 4 4:7 = MCBIST error counter for nibble 10 and rank 5 if 10, 0:3 = MCBIST error counter for port 2 and nibble 06 4:7 = MCBIST error rank map for port 2 and nibble 06
24:31	RWX	MBSSYMEC5Q_MODAL_SYMBOL_COUNTER_43: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 43 if 01, 0:3 = MCBIST error counter for nibble 10 and rank 6 4:7 = MCBIST error counter for nibble 10 and rank 7 if 10, 0:3 = MCBIST error counter for port 2 and nibble 07 4:7 = MCBIST error rank map for port 2 and nibble 07
32:39	RWX	MBSSYMEC5Q_MODAL_SYMBOL_COUNTER_44: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 44 if 01, 0:3 = MCBIST error counter for nibble 11 and rank 0 4:7 = MCBIST error counter for nibble 11 and rank 1 if 10, 0:3 = MCBIST error counter for port 2 and nibble 08 4:7 = MCBIST error rank map for port 2 and nibble 08
40:47	RWX	MBSSYMEC5Q_MODAL_SYMBOL_COUNTER_45: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 45 if 01, 0:3 = MCBIST error counter for nibble 11 and rank 2 4:7 = MCBIST error counter for nibble 11 and rank 3 if 10, 0:3 = MCBIST error counter for port 2 and nibble 09 4:7 = MCBIST error rank map for port 2 and nibble 09

Bits	SCOM	Field Mnemonic: Description
48:55	RWX	MBSSYMEC5Q_MODAL_SYMBOL_COUNTER_46: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 46 if 01, 0:3 = MCBIST error counter for nibble 11 and rank 4 4:7 = MCBIST error counter for nibble 11 and rank 5 if 10, 0:3 = MCBIST error counter for port 2 and nibble 10 4:7 = MCBIST error rank map for port 2 and nibble 10
56:63	RWX	MBSSYMEC5Q_MODAL_SYMBOL_COUNTER_47: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 47 if 01, 0:3 = MCBIST error counter for nibble 11 and rank 6 4:7 = MCBIST error counter for nibble 11 and rank 7 if 10, 0:3 = MCBIST error counter for port 2 and nibble 11 4:7 = MCBIST error rank map for port 2 and nibble 11

Register Name	MCBIST Modal Symbol Counter Register 6
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MBSSYMEC6Q
Address	000000000701235E (SCOM)
Description	MCBIST Modal Symbol Counter Register 6

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBSSYMEC6Q_MODAL_SYMBOL_COUNTER_48: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 48 if 01, 0:3 = MCBIST error counter for nibble 12 and rank 0 4:7 = MCBIST error counter for nibble 12 and rank 1 if 10, 0:3 = MCBIST error counter for port 2 and nibble 12 4:7 = MCBIST error rank map for port 2 and nibble 12
8:15	RWX	MBSSYMEC6Q_MODAL_SYMBOL_COUNTER_49: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 49 if 01, 0:3 = MCBIST error counter for nibble 12 and rank 2 4:7 = MCBIST error counter for nibble 12 and rank 3 if 10, 0:3 = MCBIST error counter for port 2 and nibble 13 4:7 = MCBIST error rank map for port 2 and nibble 13
16:23	RWX	MBSSYMEC6Q_MODAL_SYMBOL_COUNTER_50: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 50 if 01, 0:3 = MCBIST error counter for nibble 12 and rank 4 4:7 = MCBIST error counter for nibble 12 and rank 5 if 10, 0:3 = MCBIST error counter for port 2 and nibble 14 4:7 = MCBIST error rank map for port 2 and nibble 14
24:31	RWX	MBSSYMEC6Q_MODAL_SYMBOL_COUNTER_51: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 51 if 01, 0:3 = MCBIST error counter for nibble 12 and rank 6 4:7 = MCBIST error counter for nibble 12 and rank 7 if 10, 0:3 = MCBIST error counter for port 2 and nibble 15 4:7 = MCBIST error rank map for port 2 and nibble 15

Bits	SCOM	Field Mnemonic: Description
32:39	RWX	MBSSYMEC6Q_MODAL_SYMBOL_COUNTER_52: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 52 if 01, 0:3 = MCBIST error counter for nibble 13 and rank 0 4:7 = MCBIST error counter for nibble 13 and rank 1 if 10, 0:3 = MCBIST error counter for port 2 and nibble 16 4:7 = MCBIST error rank map for port 2 and nibble 16
40:47	RWX	MBSSYMEC6Q_MODAL_SYMBOL_COUNTER_53: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 53 if 01, 0:3 = MCBIST error counter for nibble 13 and rank 2 4:7 = MCBIST error counter for nibble 13 and rank 3 if 10, 0:3 = MCBIST error counter for port 2 and nibble 17 4:7 = MCBIST error rank map for port 2 and nibble 17
48:55	RWX	MBSSYMEC6Q_MODAL_SYMBOL_COUNTER_54: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 54 if 01, 0:3 = MCBIST error counter for nibble 13 and rank 4 4:7 = MCBIST error counter for nibble 13 and rank 5 if 10, 0:3 = MCBIST error counter for port 3 and nibble 00 4:7 = MCBIST error rank map for port 3 and nibble 00
56:63	RWX	MBSSYMEC6Q_MODAL_SYMBOL_COUNTER_55: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 55 if 01, 0:3 = MCBIST error counter for nibble 13 and rank 6 4:7 = MCBIST error counter for nibble 13 and rank 7 if 10, 0:3 = MCBIST error counter for port 3 and nibble 01 4:7 = MCBIST error rank map for port 3 and nibble 01

Register Name	MCBIST Modal Symbol Counter Register 7
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MBSSYMEC7Q
Address	000000000701235F (SCOM)
Description	MCBIST Modal Symbol Counter Register 7

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBSSYMEC7Q_MODAL_SYMBOL_COUNTER_56: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 56 if 01, 0:3 = MCBIST error counter for nibble 14 and rank 0 4:7 = MCBIST error counter for nibble 14 and rank 1 if 10, 0:3 = MCBIST error counter for port 3 and nibble 02 4:7 = MCBIST error rank map for port 3 and nibble 02
8:15	RWX	MBSSYMEC7Q_MODAL_SYMBOL_COUNTER_57: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 57 if 01, 0:3 = MCBIST error counter for nibble 14 and rank 2 4:7 = MCBIST error counter for nibble 14 and rank 3 if 10, 0:3 = MCBIST error counter for port 3 and nibble 03 4:7 = MCBIST error rank map for port 3 and nibble 03

Bits	SCOM	Field Mnemonic: Description
16:23	RWX	MBSSYMEC7Q_MODAL_SYMBOL_COUNTER_58: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 58 if 01, 0:3 = MCBIST error counter for nibble 14 and rank 4 4:7 = MCBIST error counter for nibble 14 and rank 5 if 10, 0:3 = MCBIST error counter for port 3 and nibble 04 4:7 = MCBIST error rank map for port 3 and nibble 04
24:31	RWX	MBSSYMEC7Q_MODAL_SYMBOL_COUNTER_59: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 59 if 01, 0:3 = MCBIST error counter for nibble 14 and rank 6 4:7 = MCBIST error counter for nibble 14 and rank 7 if 10, 0:3 = MCBIST error counter for port 3 and nibble 05 4:7 = MCBIST error rank map for port 3 and nibble 05
32:39	RWX	MBSSYMEC7Q_MODAL_SYMBOL_COUNTER_60: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 60 if 01, 0:3 = MCBIST error counter for nibble 15 and rank 0 4:7 = MCBIST error counter for nibble 15 and rank 1 if 10, 0:3 = MCBIST error counter for port 3 and nibble 06 4:7 = MCBIST error rank map for port 3 and nibble 06
40:47	RWX	MBSSYMEC7Q_MODAL_SYMBOL_COUNTER_61: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 61 if 01, 0:3 = MCBIST error counter for nibble 15 and rank 2 4:7 = MCBIST error counter for nibble 15 and rank 3 if 10, 0:3 = MCBIST error counter for port 3 and nibble 07 4:7 = MCBIST error rank map for port 3 and nibble 07
48:55	RWX	MBSSYMEC7Q_MODAL_SYMBOL_COUNTER_62: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 62 if 01, 0:3 = MCBIST error counter for nibble 15 and rank 4 4:7 = MCBIST error counter for nibble 15 and rank 5 if 10, 0:3 = MCBIST error counter for port 3 and nibble 08 4:7 = MCBIST error rank map for port 3 and nibble 08
56:63	RWX	MBSSYMEC7Q_MODAL_SYMBOL_COUNTER_63: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 63 if 01, 0:3 = MCBIST error counter for nibble 15 and rank 6 4:7 = MCBIST error counter for nibble 15 and rank 7 if 10, 0:3 = MCBIST error counter for port 3 and nibble 09 4:7 = MCBIST error rank map for port 3 and nibble 09

Register Name	**MCBIST Modal Symbol Counter Register 8**
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MBSSYMEC8Q
Address	0000000007012360 (SCOM)
Description	MCBIST Modal Symbol Counter Register 8

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBSSYMEC8Q_MODAL_SYMBOL_COUNTER_64: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 64 if 01, 0:3 = MCBIST error counter for nibble 16 and rank 0 4:7 = MCBIST error counter for nibble 16 and rank 1 if 10, 0:3 = MCBIST error counter for port 3 and nibble 10 4:7 = MCBIST error rank map for port 3 and nibble 10
8:15	RWX	MBSSYMEC8Q_MODAL_SYMBOL_COUNTER_65: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 65 if 01, 0:3 = MCBIST error counter for nibble 16 and rank 2 4:7 = MCBIST error counter for nibble 16 and rank 3 if 10, 0:3 = MCBIST error counter for port 3 and nibble 11 4:7 = MCBIST error rank map for port 3 and nibble 11
16:23	RWX	MBSSYMEC8Q_MODAL_SYMBOL_COUNTER_66: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 66 if 01, 0:3 = MCBIST error counter for nibble 16 and rank 4 4:7 = MCBIST error counter for nibble 16 and rank 5 if 10, 0:3 = MCBIST error counter for port 3 and nibble 12 4:7 = MCBIST error rank map for port 3 and nibble 12
24:31	RWX	MBSSYMEC8Q_MODAL_SYMBOL_COUNTER_67: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 67 if 01, 0:3 = MCBIST error counter for nibble 16 and rank 6 4:7 = MCBIST error counter for nibble 16 and rank 7 if 10, 0:3 = MCBIST error counter for port 3 and nibble 13 4:7 = MCBIST error rank map for port 3 and nibble 13
32:39	RWX	MBSSYMEC8Q_MODAL_SYMBOL_COUNTER_68: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 68 if 01, 0:3 = MCBIST error counter for nibble 17 and rank 0 4:7 = MCBIST error counter for nibble 17 and rank 1 if 10, 0:3 = MCBIST error counter for port 3 and nibble 14 4:7 = MCBIST error rank map for port 3 and nibble 14
40:47	RWX	MBSSYMEC8Q_MODAL_SYMBOL_COUNTER_69: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 69 if 01, 0:3 = MCBIST error counter for nibble 17 and rank 2 4:7 = MCBIST error counter for nibble 17 and rank 3 if 10, 0:3 = MCBIST error counter for port 3 and nibble 15 4:7 = MCBIST error rank map for port 3 and nibble 15
48:55	RWX	MBSSYMEC8Q_MODAL_SYMBOL_COUNTER_70: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 70 if 01, 0:3 = MCBIST error counter for nibble 17 and rank 4 4:7 = MCBIST error counter for nibble 17 and rank 5 if 10, 0:3 = MCBIST error counter for port 3 and nibble 16 4:7 = MCBIST error rank map for port 3 and nibble 16
56:63	RWX	MBSSYMEC8Q_MODAL_SYMBOL_COUNTER_71: Functional mode determined by MBSTRQ_Symbol_counter_mode: if 00, 0:7 = Maintenance NCE counter for symbol 71 if 01, 0:3 = MCBIST error counter for nibble 17 and rank 6 4:7 = MCBIST error counter for nibble 17 and rank 7 if 10, 0:3 = MCBIST error counter for port 3 and nibble 17 4:7 = MCBIST error rank map for port 3 and nibble 17

Register Name	MBS MCBIST Mode Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MBSMODESQ
Address	0000000007012362 (SCOM)
Description	MBS MCBIST Mode Register

Bits	SCOM	Field Mnemonic: Description
0	RW	MBSMODESQ_CFG_DDR4E_BLIND_STEER_MODE: When high and performing a Steer command: • In ECC64, maintenance FIRs and mark placement are suppressed. • In MCBIST, suppresses steer write back for MPEs and error counting, and uses a secondary command timebase (cfg_min_cmd_gap_blind_steer).
1:4	RW	MBSMODESQ_CFG_MCB_NIB_CNT_PORT_AGNOSTIC_MASK_DIS: Only applies when MBSTRQ_Symbol_counter_mode = 01 (port agnostic mode). When doing MCBIST nibble counts for a single port or port agnostic, this option allows you to mask or disable particular ports from affecting the results. For example, if value = 0101, errors from ports 1 and 3 are ignored and only errors from port 0 and 2 affect counts.
5:15	RW	MBSMODESQ_RESERVE_5_15: Reserved.

Register Name	MCBIST Error Status Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBSTATQ
Address	0000000007012366 (SCOM)
Description	MCBIST Error Status Register

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	MCBSTATQ_MCBIST_LOGGED_ERROR_ON_PORT_INDICATOR: MCBIST logged error on port indicator. In MCB mode, these are sticky bits to indicate that an error has been logged on this port.
4:8	ROX	MCBSTATQ_MCBIST_SUBTEST_NUM_INDICATOR: MCBIST subtest number indicator. Indicates which subtest number the MCBIST is currently on.
9:15	ROX	MCBSTATQ_RESERVED_9_15: Reserved.
16:55	RO	Constant = 0b00000000000000000000000000000000000000000000

Register Name	MBS Memory Scrub/Read Error Count Register 0
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MBSMSECQ
Address	0000000007012369 (SCOM)
Description	MBS Memory Scrub/Read Error Count Register 0

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBSMSECQ_MCE_SYMBOL0_COUNT: MCE symbol 0 error count. This is an 8-bit count that increments on MCE when symbol 0 under the chip mark takes an error. It freezes its value upon incrementing to the maximum value until reset.
8:15	RWX	MBSMSECQ_MCE_SYMBOL1_COUNT: MCE symbol 1 error count. This is an 8-bit count that increments on MCE when symbol 1 under the chip mark takes an error. It freezes its value upon incrementing to the maximum value until reset.

Bits	SCOM	Field Mnemonic: Description
16:23	RWX	MBSMSECQ_MCE_SYMBOL2_COUNT: MCE symbol 2 error count. This is an 8-bit count that increments on MCE when symbol 2 under the chip mark takes an error. It freezes its value upon incrementing to the maximum value until reset.
24:31	RWX	MBSMSECQ_MCE_SYMBOL3_COUNT: MCE symbol 3 error count. This is an 8-bit count that increments on MCE when symbol 3 under chip mark takes an error. It freezes its value upon incrementing to the maximum value until reset.

Register Name	**MBS Port 0 Mainline NCE Address Trap Register**
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MBNCER0Q
Address	000000000701236A (SCOM)
Description	MBS Port 0 Mainline NCE Address Trap Register

Bits	SCOM	Field Mnemonic: Description
0:37	RWX	MBNCER0Q_PORT_0_MAINLINE_NCE_ADDR_TRAP: The trap address for the last mainline NCE on port 0. 0:1 = Reserve 2 = DIMM select 3:4 = Master rank 5:7 = Slave rank 8:25 = Row 26:32 = Column 33:35 = Bank 36:37 = Bank group
38	RWX	MBNCER0Q_PORT_0_MAINLINE_NCE_ON_RCE: Indicates if this NCE came on the retry of a UE, an RCD, or an AUE as part of an RCE.
39	RWX	MBNCER0Q_PORT_0_MAINLINE_NCE_IS_TCE: Indicates if this NCE is actually a two-symbol error (TCE).

Register Name	**MBS Port 0 Mainline RCE Address Trap Register**
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MBRCER0Q
Address	000000000701236B (SCOM)
Description	MBS Port 0 Mainline RCE Address Trap Register

Bits	SCOM	Field Mnemonic: Description
0:37	RWX	MBRCER0Q_PORT_0_MAINLINE_RCE_ADDR_TRAP: The trap address for the last mainline RCE on port 0. 0:1 = Reserve 2 = DIMM select 3:4 = Master rank 5:7 = Slave rank 8:25 = Row 26:32 = Column 33:35 = Bank 36:37 = Bank group
38:39	RWX	MBRCER0Q_RESERVED_38_39: Reserved.

Register Name	**MBS Port 0 Mainline MPE Address Trap Register**
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MBMPER0Q
Address	000000000701236C (SCOM)
Description	MBS Port 0 Mainline MPE Address Trap Register

Bits	SCOM	Field Mnemonic: Description
0:37	RWX	MBMPER0Q_PORT_0_MAINLINE_MPE_ADDR_TRAP: The trap address for the last mainline MPE on port 0. 0:1 = Reserve 2 = DIMM select 3:4 = Master rank 5:7 = Slave rank 8:25 = Row 26:32 = Column 33:35 = Bank 36:37 = Bank group
38	RWX	MBMPER0Q_PORT_0_MAINLINE_MPE_ON_RCE: Indicates if this error came on the retry of a UE, an RCD, or an AUE as part of an RCE.
39	RWX	MBMPER0Q_RESERVED_39: Reserved.

Register Name	**MBS Port 0 Mainline UE Address Trap Register**
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MBUER0Q
Address	000000000701236D (SCOM)
Description	MBS Port 0 Mainline UE Address Trap Register

Bits	SCOM	Field Mnemonic: Description
0:37	RWX	MBUER0Q_PORT_0_MAINLINE_UE_ADDR_TRAP: The trap address for the last mainline UE on port 0. 0:1 = Reserve 2 = DIMM select 3:4 = Master rank 5:7 = Slave rank 8:25 = Row 26:32 = Column 33:35 = Bank 36:37 = Bank group
38:39	RWX	MBUER0Q_RESERVED_38_39: Reserved.

Register Name	**MBS Port 0 Mainline AUE Address Trap Register**
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MBAUER0Q
Address	000000000701236E (SCOM)
Description	MBS Port 0 Mainline AUE Address Trap Register

Bits	SCOM	Field Mnemonic: Description
0:37	RWX	MBAUER0Q_PORT_0_MAINLINE_AUE_ADDR_TRAP: The trap address for the last mainline AUE on port 0. 0:1 = Reserve 2 = DIMM select 3:4 = Master rank 5:7 = Slave rank 8:25 = Row 26:32 = Column 33:35 = Bank 36:37 = Bank group
38:39	RWX	MBAUER0Q_RESERVED_38_39: Reserved.

Register Name	MBS Port 1 Mainline NCE Address Trap Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MBNCER1Q
Address	000000000701236F (SCOM)
Description	MBS Port 1 Mainline NCE Address Trap Register

Bits	SCOM	Field Mnemonic: Description
0:37	RWX	MBNCER1Q_PORT_1_MAINLINE_NCE_ADDR_TRAP: The trap address for the last mainline NCE on port 1. 0:1 = Reserve 2 = DIMM select 3:4 = Master rank 5:7 = Slave rank 8:25 = Row 26:32 = Column 33:35 = Bank 36:37 = Bank group
38	RWX	MBNCER1Q_PORT_1_MAINLINE_NCE_ON_RCE: Indicates if this NCE came on the retry of a UE, an RCD, or an AUE as part of an RCE.
39	RWX	MBNCER1Q_PORT_1_MAINLINE_NCE_IS_TCE: Indicates if this NCE is actually a two-symbol error (TCE).

Register Name	MBS Port 1 Mainline RCE Address Trap Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MBRCER1Q
Address	0000000007012370 (SCOM)
Description	MBS Port 1 Mainline RCE Address Trap Register

Bits	SCOM	Field Mnemonic: Description
0:37	RWX	MBRCER1Q_PORT_1_MAINLINE_RCE_ADDR_TRAP: The trap address for the last mainline RCE on port 1. 0:1 = Reserve 2 = DIMM select 3:4 = Master rank 5:7 = Slave rank 8:25 = Row 26:32 = Column 33:35 = Bank 36:37 = Bank group
38:39	RWX	MBRCER1Q_RESERVED_38_39: Reserved.

Register Name	**MBS Port 1 Mainline MPE Address Trap Register**
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MBMPER1Q
Address	0000000007012371 (SCOM)
Description	MBS Port 1 Mainline MPE Address Trap Register

Bits	SCOM	Field Mnemonic: Description
0:37	RWX	MBMPER1Q_PORT_1_MAINLINE_MPE_ADDR_TRAP: The trap address for the last mainline MPE on port 1. 0:1 = Reserve 2 = DIMM select 3:4 = Master rank 5:7 = Slave rank 8:25 = Row 26:32 = Column 33:35 = Bank 36:37 = Bank group
38	RWX	MBMPER1Q_PORT_1_MAINLINE_MPE_ON_RCE: Indicates if this error came on the retry of a UE, an RCD, or an AUE as part of an RCE.
39	RWX	MBMPER1Q_RESERVED_39: Reserved.

Register Name	**MBS Port 1 Mainline UE Address Trap Register**
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MBUER1Q
Address	0000000007012372 (SCOM)
Description	MBS Port 1 Mainline UE Address Trap Register

Bits	SCOM	Field Mnemonic: Description
0:37	RWX	MBUER1Q_PORT_1_MAINLINE_UE_ADDR_TRAP: The trap address for the last mainline UE on port 1. 0:1 = Reserve 2 = DIMM select 3:4 = Master rank 5:7 = Slave rank 8:25 = Row 26:32 = Column 33:35 = Bank 36:37 = Bank group
38:39	RWX	MBUER1Q_RESERVED_38_39: Reserved.

Register Name	**MBS Port 1 Mainline AUE Address Trap Register**
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MBAUER1Q
Address	0000000007012373 (SCOM)
Description	MBS Port 1 Mainline AUE Address Trap Register

Bits	SCOM	Field Mnemonic: Description
0:37	RWX	MBAUER1Q_PORT_1_MAINLINE_AUE_ADDR_TRAP: The trap address for the last mainline AUE on port 1. 0:1 = Reserve 2 = DIMM select 3:4 = Master rank 5:7 = Slave rank 8:25 = Row 26:32 = Column 33:35 = Bank 36:37 = Bank group
38:39	RWX	MBAUER1Q_RESERVED_38_39: Reserved.

Register Name	**MBS Port 2 Mainline NCE Address Trap Register**
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MBNCER2Q
Address	0000000007012374 (SCOM)
Description	MBS Port 2 Mainline NCE Address Trap Register

Bits	SCOM	Field Mnemonic: Description
0:37	RWX	MBNCER2Q_PORT_2_MAINLINE_NCE_ADDR_TRAP: The trap address for the last mainline NCE on port 2. 0:1 = Reserve 2 = DIMM select 3:4 = Master rank 5:7 = Slave rank 8:25 = Row 26:32 = Column 33:35 = Bank 36:37 = Bank group
38	RWX	MBNCER2Q_PORT_2_MAINLINE_NCE_ON_RCE: Indicates if this NCE came on the retry of a UE, an RCD, or an AUE as part of an RCE.
39	RWX	MBNCER2Q_PORT_2_MAINLINE_NCE_IS_TCE: Indicates if the NCE is actually a two-symbol error (TCE).

Register Name	**MBS Port 2 Mainline RCE Address Trap Register**
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MBRCER2Q
Address	0000000007012375 (SCOM)
Description	MBS Port 2 Mainline RCE Address Trap Register

Bits	SCOM	Field Mnemonic: Description
0:37	RWX	MBRCER2Q_PORT_2_MAINLINE_RCE_ADDR_TRAP: The trap address for the last mainline RCE on port 2. 0:1 = Reserve 2 = DIMM select 3:4 = Master rank 5:7 = Slave rank 8:25 = Row 26:32 = Column 33:35 = Bank 36:37 = Bank group
38:39	RWX	MBRCER2Q_RESERVED_38_39: Reserved.

Register Name	MBS Port 2 Mainline MPE Address Trap Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MBMPER2Q
Address	0000000007012376 (SCOM)
Description	MBS Port 2 Mainline MPE Address Trap Register

Bits	SCOM	Field Mnemonic: Description
0:37	RWX	MBMPER2Q_PORT_2_MAINLINE_MPE_ADDR_TRAP: The trap address for the last mainline MPE on port 2. 0:1 = Reserve 2 = DIMM select 3:4 = Master rank 5:7 = Slave rank 8:25 = Row 26:32 = Column 33:35 = Bank 36:37 = Bank group
38	RWX	MBMPER2Q_PORT_2_MAINLINE_MPE_ON_RCE: Indicates if this error came on the retry of a UE, an RCD, or an AUE as part of an RCE.
39	RWX	MBMPER2Q_RESERVED_39: Reserved.

Register Name	MBS Port 2 Mainline UE Address Trap Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MBUER2Q
Address	0000000007012377 (SCOM)
Description	MBS Port 2 Mainline UE Address Trap Register

Bits	SCOM	Field Mnemonic: Description
0:37	RWX	MBUER2Q_PORT_2_MAINLINE_UE_ADDR_TRAP: The trap address for the last mainline UE on port 2. 0:1 = Reserve 2 = DIMM select 3:4 = Master rank 5:7 = Slave rank 8:25 = Row 26:32 = Column 33:35 = Bank 36:37 = Bank group
38:39	RWX	MBUER2Q_RESERVED_38_39: Reserved.

Register Name	MBS Port 2 Mainline AUE Address Trap Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MBAUER2Q
Address	0000000007012378 (SCOM)
Description	MBS Port 2 Mainline AUE Address Trap Register

Bits	SCOM	Field Mnemonic: Description
0:37	RWX	MBAUER2Q_PORT_2_MAINLINE_AUE_ADDR_TRAP: The trap address for the last mainline AUE on port 2. 0:1 = Reserve 2 = DIMM select 3:4 = Master rank 5:7 = Slave rank 8:25 = Row 26:32 = Column 33:35 = Bank 36:37 = Bank group
38:39	RWX	MBAUER2Q_RESERVED_38_39: Reserved.

Register Name	MBS Port 3 Mainline NCE Address Trap Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MBNCER3Q
Address	0000000007012379 (SCOM)
Description	MBS Port 3 Mainline NCE Address Trap Register

Bits	SCOM	Field Mnemonic: Description
0:37	RWX	MBNCER3Q_PORT_3_MAINLINE_NCE_ADDR_TRAP: The trap address for the last mainline NCE on port 3. 0:1 = Reserve 2 = DIMM select 3:4 = Master rank 5:7 = Slave rank 8:25 = Row 26:32 = Column 33:35 = Bank 36:37 = Bank group
38	RWX	MBNCER3Q_PORT_3_MAINLINE_NCE_ON_RCE: Indicates if this NCE came on the retry of a UE, an RCD, or an AUE as part of an RCE.
39	RWX	MBNCER3Q_PORT_3_MAINLINE_NCE_IS_TCE: Indicates if this NCE is actually a two-symbol error (TCE).

Register Name	MBS Port 3 Mainline RCE Address Trap Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MBRCER3Q
Address	000000000701237A (SCOM)
Description	MBS Port 3 Mainline RCE Address Trap Register

Bits	SCOM	Field Mnemonic: Description
0:37	RWX	MBRCER3Q_PORT_3_MAINLINE_RCE_ADDR_TRAP: The trap address for the last mainline RCE on port 3. 0:1 = Reserve 2 = DIMM select 3:4 = Master rank 5:7 = Slave rank 8:25 = Row 26:32 = Column 33:35 = Bank 36:37 = Bank group
38:39	RWX	MBRCER3Q_RESERVED_38_39: Reserved.

Register Name	MBS Port 3 Mainline MPE Address Trap Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MBMPER3Q
Address	000000000701237B (SCOM)
Description	MBS Port 3 Mainline MPE Address Trap Register

Bits	SCOM	Field Mnemonic: Description
0:37	RWX	MBMPER3Q_PORT_3_MAINLINE_MPE_ADDR_TRAP: The trap address for the last mainline MPE on port 3. 0:1 = Reserve 2 = DIMM select 3:4 = Master rank 5:7 = Slave rank 8:25 = Row 26:32 = Column 33:35 = Bank 36:37 = Bank group
38	RWX	MBMPER3Q_PORT_3_MAINLINE_MPE_ON_RCE: Indicates if this error came on the retry of a UE, an RCD, or an AUE as part of an RCE.
39	RWX	MBMPER3Q_RESERVED_39: Reserved.

Register Name	MBS Port 3 Mainline UE Address Trap Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MBUER3Q
Address	000000000701237C (SCOM)
Description	MBS Port 3 Mainline UE Address Trap Register

Bits	SCOM	Field Mnemonic: Description
0:37	RWX	MBUER3Q_PORT_3_MAINLINE_UE_ADDR_TRAP: The trap address for the last mainline UE on port 3. 0:1 = Reserve 2 = DIMM select 3:4 = Master rank 5:7 = Slave rank 8:25 = Row 26:32 = Column 33:35 = Bank 36:37 = Bank group
38:39	RWX	MBUER3Q_RESERVED_38_39: Reserved.

Register Name	MBS Port 3 Mainline AUE Address Trap Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MBAUER3Q
Address	000000000701237D (SCOM)
Description	MBS Port 3 Mainline AUE Address Trap Register

Bits	SCOM	Field Mnemonic: Description
0:37	RWX	MBAUER3Q_PORT_3_MAINLINE_AUE_ADDR_TRAP: The trap address for the last mainline AUE on port 3. 0:1 = Reserve 2 = DIMM select 3:4 = Master rank 5:7 = Slave rank 8:25 = Row 26:32 = Column 33:35 = Bank 36:37 = Bank group
38:39	RWX	MBAUER3Q_RESERVED_38_39: Reserved.

Register Name	**MBS Error Vector Trap Register 0 (Port 0 and 1 Mainline)**
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MBSEVR0Q
Address	000000000701237E (SCOM)
Description	MBS Error Vector Trap Register 0 (Port 0 and 1 mainline)

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBSEVR0Q_PORT_0_MAINLINE_NCE_GALOIS_FIELD: Port 0 mainline NCE Galois field.
8:15	RWX	MBSEVR0Q_PORT_0_MAINLINE_NCE_MAGNITUDE_FIELD: Port 0 mainline NCE magnitude field.
16:23	RWX	MBSEVR0Q_PORT_0_MAINLINE_TCE_GALOIS_FIELD: Port 0 mainline TCE Galois field.
24:31	RWX	MBSEVR0Q_PORT_0_MAINLINE_TCE_MAGNITUDE_FIELD: Port 0 mainline TCE magnitude field.
32:39	RWX	MBSEVR0Q_PORT_1_MAINLINE_NCE_GALOIS_FIELD: Port 1 mainline NCE Galois field.
40:47	RWX	MBSEVR0Q_PORT_1_MAINLINE_NCE_MAGNITUDE_FIELD: Port 1 mainline NCE magnitude field.
48:55	RWX	MBSEVR0Q_PORT_1_MAINLINE_TCE_GALOIS_FIELD: Port 1 mainline TCE Galois field.
56:63	RWX	MBSEVR0Q_PORT_1_MAINLINE_TCE_MAGNITUDE_FIELD: Port 1 mainline TCE magnitude field.

Register Name	**MBS Error Vector Trap Register 1 (Port 2 and 3 Mainline)**
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MBSEVR1Q
Address	000000000701237F (SCOM)
Description	MBS Error Vector Trap Register 1 (Port 2 and 3 mainline)

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBSEVR1Q_PORT_2_MAINLINE_NCE_GALOIS_FIELD: Port 2 mainline NCE Galois field.
8:15	RWX	MBSEVR1Q_PORT_2_MAINLINE_NCE_MAGNITUDE_FIELD: Port 2 mainline NCE magnitude field.
16:23	RWX	MBSEVR1Q_PORT_2_MAINLINE_TCE_GALOIS_FIELD: Port 2 mainline TCE Galois field.
24:31	RWX	MBSEVR1Q_PORT_2_MAINLINE_TCE_MAGNITUDE_FIELD: Port 2 mainline TCE magnitude field.
32:39	RWX	MBSEVR1Q_PORT_3_MAINLINE_NCE_GALOIS_FIELD: Port 3 mainline NCE Galois field.
40:47	RWX	MBSEVR1Q_PORT_3_MAINLINE_NCE_MAGNITUDE_FIELD: Port 3 mainline NCE magnitude field.
48:55	RWX	MBSEVR1Q_PORT_3_MAINLINE_TCE_GALOIS_FIELD: Port 3 mainline TCE Galois field.
56:63	RWX	MBSEVR1Q_PORT_3_MAINLINE_TCE_MAGNITUDE_FIELD: Port 3 mainline TCE magnitude field.

Register Name	MCBIST WAT 0 Configuration Register 0A (WAT Event Sel)
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.WATCFG0AQ
Address	0000000007012380 (SCOM)
Description	MCBIST WAT 0 Configuration Register 0A (WAT event sel)

Bits	SCOM	Field Mnemonic: Description
0:47	RW	WATCFG0AQ_CFG_WAT_EVENT_SEL: cfg_wat_event_sel.

Register Name	MCBIST WAT 0 Configuration Register 0B (Mask a and Cntl)
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.WATCFG0BQ
Address	0000000007012381 (SCOM)
Description	MCBIST WAT 0 Configuration Register 0B (Mask a and cntl)

Bits	SCOM	Field Mnemonic: Description
0:43	RW	WATCFG0BQ_CFG_WAT_MSKA: cfg_wat_mska.
44:60	RW	WATCFG0BQ_CFG_WAT_CNTL: cfg_wat_cntl.

Register Name	MCBIST WAT 0 Configuration Register 0C (Mask b)
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.WATCFG0CQ
Address	0000000007012382 (SCOM)
Description	MCBIST WAT 0 Configuration Register 0C (Mask b)

Bits	SCOM	Field Mnemonic: Description
0:43	RW	WATCFG0CQ_CFG_WAT_MSKB: cfg_wat_mskb.

Register Name	MCBIST WAT 0 Configuration Register 0D (Pattern a)
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.WATCFG0DQ
Address	0000000007012383 (SCOM)
Description	MCBIST WAT 0 Configuration Register 0D (Pattern a)

Bits	SCOM	Field Mnemonic: Description
0:43	RW	WATCFG0DQ_CFG_WAT_PATA: cfg_wat_pata.

Register Name	MCBIST WAT 0 Configuration Register 0E (Pattern b)
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.WATCFG0EQ
Address	0000000007012384 (SCOM)
Description	MCBIST WAT 0 Configuration Register 0E (Pattern b)

Bits	SCOM	Field Mnemonic: Description
0:43	RW	WATCFG0EQ_CFG_WAT_PATB: cfg_wat_patb.

Register Name	MCBIST WAT 1 Configuration Register 1A (WAT Event Sel)
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.WATCFG1AQ
Address	0000000007012385 (SCOM)
Description	MCBIST WAT 1 Configuration Register 1A (WAT event sel)

Bits	SCOM	Field Mnemonic: Description
0:47	RW	WATCFG1AQ_CFG_WAT_EVENT_SEL: cfg_wat_event_sel.

Register Name	MCBIST WAT 1 Configuration Register 1B (Mask a and Cntl)
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.WATCFG1BQ
Address	0000000007012386 (SCOM)
Description	MCBIST WAT 1 Configuration Register 1B (Mask a and cntl)

Bits	SCOM	Field Mnemonic: Description
0:43	RW	WATCFG1BQ_CFG_WAT_MSKA: cfg_wat_mska.
44:60	RW	WATCFG1BQ_CFG_WAT_CNTL: cfg_wat_cntl.

Register Name	MCBIST WAT 1 Configuration Register 1C (Mask b)
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.WATCFG1CQ
Address	0000000007012387 (SCOM)
Description	MCBIST WAT 1 Configuration Register 1C (Mask b)

Bits	SCOM	Field Mnemonic: Description
0:43	RW	WATCFG1CQ_CFG_WAT_MSKB: cfg_wat_mskb.

Register Name	MCBIST WAT 1 Configuration Register 1D (Pattern a)
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.WATCFG1DQ
Address	0000000007012388 (SCOM)
Description	MCBIST WAT 1 Configuration Register 1D (Pattern a)

Bits	SCOM	Field Mnemonic: Description
0:43	RW	WATCFG1DQ_CFG_WAT_PATA: cfg_wat_pata.

Register Name	MCBIST WAT 1 Configuration Register 1E (Pattern b)
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.WATCFG1EQ
Address	0000000007012389 (SCOM)
Description	MCBIST WAT 1 Configuration Register 1E (Pattern b)

Bits	SCOM	Field Mnemonic: Description
0:43	RW	WATCFG1EQ_CFG_WAT_PATB: cfg_wat_patb.

Register Name	MCBIST WAT 2 Configuration Register 2A (WAT Event Sel)
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.WATCFG2AQ
Address	000000000701238A (SCOM)
Description	MCBIST WAT 2 Configuration Register 2A (WAT event sel)

Bits	SCOM	Field Mnemonic: Description
0:47	RW	WATCFG2AQ_CFG_WAT_EVENT_SEL: cfg_wat_event_sel.

Register Name	MCBIST WAT 2 Configuration Register 2B (Mask a and Cntl)
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.WATCFG2BQ
Address	000000000701238B (SCOM)
Description	MCBIST WAT 2 Configuration Register 2B (Mask a and cntl)

Bits	SCOM	Field Mnemonic: Description
0:43	RW	WATCFG2BQ_CFG_WAT_MSKA: cfg_wat_mska.
44:60	RW	WATCFG2BQ_CFG_WAT_CNTL: cfg_wat_cntl.

Register Name	MCBIST WAT 2 Configuration Register 2C (Mask b)
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.WATCFG2CQ
Address	000000000701238C (SCOM)
Description	MCBIST WAT 2 Configuration Register 2C (Mask b)

Bits	SCOM	Field Mnemonic: Description
0:43	RW	WATCFG2CQ_CFG_WAT_MSKB: cfg_wat_mskb.

Register Name	MCBIST WAT 2 Configuration Register 2D (Pattern a)
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.WATCFG2DQ
Address	000000000701238D (SCOM)
Description	MCBIST WAT 2 Configuration Register 2D (Pattern a)

Bits	SCOM	Field Mnemonic: Description
0:43	RW	WATCFG2DQ_CFG_WAT_PATA: cfg_wat_pata.

Register Name	MCBIST WAT 2 Configuration Register 2E (Pattern b)
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.WATCFG2EQ
Address	000000000701238E (SCOM)
Description	MCBIST WAT 2 Configuration Register 2E (Pattern b)

Bits	SCOM	Field Mnemonic: Description
0:43	RW	WATCFG2EQ_CFG_WAT_PATB: cfg_wat_patb.

Register Name	MCBIST WAT 3 Configuration Register 3A (WAT Event Sel)
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.WATCFG3AQ
Address	000000000701238F (SCOM)
Description	MCBIST WAT 3 Configuration Register 3A (WAT event sel)

Bits	SCOM	Field Mnemonic: Description
0:47	RW	WATCFG3AQ_CFG_WAT_EVENT_SEL: cfg_wat_event_sel.

Register Name	MCBIST WAT 3 Configuration Register 3B (Mask a and Cntl)
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.WATCFG3BQ
Address	0000000007012390 (SCOM)
Description	MCBIST WAT 3 Configuration Register 3B (Mask a and cntl)

Bits	SCOM	Field Mnemonic: Description
0:43	RW	WATCFG3BQ_CFG_WAT_MSKA: cfg_wat_mska.
44:60	RW	WATCFG3BQ_CFG_WAT_CNTL: cfg_wat_cntl.

Register Name	MCBIST WAT 3 Configuration Register 3C (Mask b)
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.WATCFG3CQ
Address	0000000007012391 (SCOM)
Description	MCBIST WAT 3 Configuration Register 3C (Mask b)

Bits	SCOM	Field Mnemonic: Description
0:43	RW	WATCFG3CQ_CFG_WAT_MSKB: cfg_wat_mskb.

Register Name	MCBIST WAT 3 Configuration Register 3D (Pattern a)
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.WATCFG3DQ
Address	0000000007012392 (SCOM)
Description	MCBIST WAT 3 Configuration Register 3D (Pattern a)

Bits	SCOM	Field Mnemonic: Description
0:43	RW	WATCFG3DQ_CFG_WAT_PATA: cfg_wat_pata.

Register Name	MCBIST WAT 3 Configuration Register 3E (Pattern b)
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.WATCFG3EQ
Address	0000000007012393 (SCOM)
Description	MCBIST WAT 3 Configuration Register 3E (Pattern b)

Bits	SCOM	Field Mnemonic: Description
0:43	RW	WATCFG3EQ_CFG_WAT_PATB: cfg_wat_patb.

Register Name	Configured Command Sequence Control Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.CCS_CNTLQ
Address	00000000070123A5 (SCOM)
Description	Configured Command Sequence Control Register

Bits	SCOM	Field Mnemonic: Description
0	RWX	CCS_CNTLQ_CCS_START: Start bit. This self-resetting bit kicks off the CCS operation.
1	RWX	CCS_CNTLQ_CCS_STOP: Stop bit. This self-resetting bit stops the current CCS operation.
2:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	Configured Command Sequence Status Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.CCS_STATQ
Address	00000000070123A6 (SCOM)
Description	Configured Command Sequence Status Register

Bits	SCOM	Field Mnemonic: Description
0	RWX	CCS_STATQ_CCS_IP: IP bit. Hardware sets this bit to a '1'b when a CCS run is in progress.
1	RWX	CCS_STATQ_CCS_DONE: Done bit. Hardware sets this bit to a '1'b when a CCS run is complete.
2	RWX	CCS_STATQ_CCS_FAIL: Fail bit. Hardware sets this bit to a '1'b when a CCS run failed.
3:5	RWX	CCS_STATQ_CCS_FAIL_TYPE: Fail type. Indicates the type of CCS failure: 0 = Read miscompare 1 = Instruction array UE or SUE 2 = Calibration operation times out
6	RWX	CCS_STATQ_MCBIST_CCS_SUBTEST_IP: Indicates that the current CCS run was initiated as a MCBIST subtest.
7	RWX	CCS_STATQ_CCS_FAIL_RCD: Indicates that an RCD fail occurred during a CCS.
8:14	RO	Constant = 0b0000000

Register Name	Configured Command Sequence Mode Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.CCS_MODEQ
Address	00000000070123A7 (SCOM)
Description	Configured Command Sequence Mode Register

Bits	SCOM	Field Mnemonic: Description
0	RW	CCS_MODEQ_CCS_STOP_ON_ERR: The user sets this bit to a '1'b to tell the hardware to stop the CCS whenever a failure occurs. When '0'b, hardware will continue the CCS even if a failure occurs.
1	RW	CCS_MODEQ_CCS_UE_DISABLE: The user sets this bit to a '1'b to force the hardware to ignore any array UE or SUE errors during CCS command fetching.
2:3	RW	CCS_MODEQ_CCS_DATA_COMPARE_BURST_SEL: Reserved.
4:7	RW	CCS_MODEQ_RESERVED_4_7: Reserved.
8:23	RW	CCS_MODEQ_DDR_CAL_TIMEOUT_CNT: DDR calibration time counter. Indicates the amount of time to wait for DDR calibration to complete. This value is multiplied by the factor in bits 30:31 to get the total timeout wait time.
24	RW	CCS_MODEQ_CFG_CCS_PARITY_AFTER_CMD: Determines whether OE is driven on the parity cycle. 0 = OE is not driven on the parity cycle. 1 = OE is driven on the parity cycle.
25	RW	CCS_MODEQ_RESERVED_25: Reserved.
26	RW	CCS_MODEQ_COPY_CKE_TO_SPARE_CKE: Copy CKE signals to CKE spare on both ports. **Note**: *Does not apply for POWER9. No spare chips to copy to.* 0 = Spare CKEs are not copied with values from CKE(0:1) and CKE(4:5). 1 = Port A CKE(0:1) is copied to port A CKE(2:3), port A CKE(4:5) is copied to port A CKE(6:7), port B CKE(0:1) is copied to port B CKE(2:3), and port B CKE(4:5) is copied to port B CKE(6:7).
27	RW	CCS_MODEQ_DISABLE_ECC_ARRAY_CHK: Disable ECC checking on the CCS arrays. 0 = ECC checking on. 1 = ECC checking off.
28	RW	CCS_MODEQ_DISABLE_ECC_ARRAY_CORRECTION: Disable ECC correction on the CCS arrays. 0 = ECC correction on. 1 = ECC correction off.
29	RW	CCS_MODEQ_CFG_CCS_DGEN_FIXED_MODE: When enabled and a CCS is in progress, the CCS uses MCBIST DGEN fixed data mode for its write data. This mode allows varying data per burst and bit. For CCS DGEN, ECC is disabled.
30:31	RW	CCS_MODEQ_DDR_CAL_TIMEOUT_CNT_MULT: DDR calibration time counter multiplication factor. This value is multiplied by the counter in bits 8:23 to get the total timeout wait time.
32:45	RW	CCS_MODEQ_CCS_IDLE_PAT_ADDRESS_0_13: Idle pattern for CCS DDR Address Row Column; bits 0:13.
46	RW	CCS_MODEQ_CCS_IDLE_PAT_ADDRESS_17: Idle pattern for CCS DDR Address Row Column; bit 17 (formerly labeled address(14) for POWER8).
47	RW	CCS_MODEQ_CCS_IDLE_PAT_BANK_GROUP_1: Idle pattern for CCS DDR Address Bank Group; bit 1 (formerly labeled address(15) for POWER8).
48:49	RW	CCS_MODEQ_CCS_IDLE_PAT_BANK_0_1: Idle pattern for CCS DDR Address Bank; bits 0:1.
50	RW	CCS_MODEQ_CCS_IDLE_PAT_BANK_GROUP_0: Idle pattern for CCS DDR Address Bank Group; bit 0 (formerly labeled bank(2) for POWER8).
51	RW	CCS_MODEQ_CCS_IDLE_PAT_ACTN: Idle pattern for CCS DDR Activate Not.
52	RW	CCS_MODEQ_CCS_IDLE_PAT_ADDRESS_16: Idle pattern for CCS DDR Address Row Column; bit 16 (formerly labeled RASN for POWER8).
53	RW	CCS_MODEQ_CCS_IDLE_PAT_ADDRESS_15: Idle pattern for CCS DDR Address Row Column; bit 15 (formerly labeled CASN for POWER8).
54	RW	CCS_MODEQ_CCS_IDLE_PAT_ADDRESS_14: Idle pattern for CCS DDR Address Row Column; bit 14 (formerly labeled WEN for POWER8).
55	RW	CCS_MODEQ_NTTM_MODE: Nontraditional transparent mode. When set to 1, limited nontraditional read and write operations can be done.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	CCS_MODEQ_NTTM_RW_DATA_DLY: Nontraditional transparent read/write delay. Use to delay the write data start pulse or read data capture pulse to the DDR PHYs. A maximum delay of 15 cycles is possible.
60	RW	CCS_MODEQ_CCS_IDLE_PAT_BANK_2: Idle pattern for CCS DDR Address Bank; bit 2.
61	RW	CCS_MODEQ_DDR_PARITY_ENABLE: DDR Parity enabled. When set to 1, the value of CCS_INST_ARR0_[00-31]_ccs_ddr_parity or arra0(60) is driven out to DDR parity. When set to 0, the hardware calculates the parity.
62	RW	CCS_MODEQ_CCS_IDLE_PAT_PARITY: If CCS_MODEQ_DDR_parity_enable = 1, the CCS drives this value for parity on idle cycles.
63	RW	CCS_MODEQ_RESERVED_63: Reserved_63.

Register Name	**MCBIST Memory Register 0**
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBMR0Q
Address	00000000070123A8 (SCOM)
Description	MCBIST Memory Register 0

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MCBIST_CFG_TEST00_OP_TYPE: Operation type. • If Subtest(0:3) = 0111 and 9:11(Data mode) = 000 (goto command), Subtest Addr 4:8 specifies which subtest address to change to (used for looping). • If Subtest(0:3) = 0111 and 9:11(Data mode) not = 000 (refresh only command), Subtest Addr 4:8 is a don't care.
4	RW	MCBIST_CFG_TEST00_COMPL_1ST_CMD: Complement the data for the first subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
5	RW	MCBIST_CFG_TEST00_COMPL_2ND_CMD: Complement the data for the second subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
6	RW	MCBIST_CFG_TEST00_COMPL_3RD_CMD: Complement the data for the third subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
7	RW	MCBIST_CFG_TEST00_ADDR_REV_MODE: Generate addresses in reverse order.
8	RW	MCBIST_CFG_TEST00_ADDR_RAND_MODE: Generate addresses in random order.
9:11	RW	MCBIST_CFG_TEST00_DATA_MODE: Data mode.
12	RW	MCBIST_CFG_TEST00_ECC_MODE: Generate and check data with the ECC.
13	RW	MCBIST_CFG_TEST00_DONE: Done bit.
14:15	RW	MCBIST_CFG_TEST00_ADDR_SEL: Address select mode.
16:19	RW	MCBIST_CFG_TEST01_OP_TYPE: Operation type. • If Subtest(16:19) = 0111 and 25:27(Data mode) = 000 (goto command), Subtest Addr 20:24 specifies which subtest address to change to (used for looping). • If Subtest(16:19) = 0111 and 25:27(Data mode) not = 000 (refresh only command), Subtest Addr 20:24 is a don't care.
20	RW	MCBIST_CFG_TEST01_COMPL_1ST_CMD: Complement the data for the first subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
21	RW	MCBIST_CFG_TEST01_COMPL_2ND_CMD: Complement the data for the second subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
22	RW	MCBIST_CFG_TEST01_COMPL_3RD_CMD: Complement the data for the third subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.

Bits	SCOM	Field Mnemonic: Description
23	RW	MCBIST_CFG_TEST01_ADDR_REV_MODE: Generate addresses in reverse order.
24	RW	MCBIST_CFG_TEST01_ADDR_RAND_MODE: Generate addresses in random order.
25:27	RW	MCBIST_CFG_TEST01_DATA_MODE: Data mode.
28	RW	MCBIST_CFG_TEST01_ECC_MODE: Generate and check data with the ECC.
29	RW	MCBIST_CFG_TEST01_DONE: Done bit.
30:31	RW	MCBIST_CFG_TEST01_ADDR_SEL: Address select mode.
32:35	RW	MCBIST_CFG_TEST02_OP_TYPE: Operation type. • If Subtest(32:35) = 0111 and 41:43(Data mode) = 000 (goto command), Subtest Addr 36:40 specifies which subtest address to change to (used for looping). • If Subtest(32:35) = 0111 and 41:43(Data mode) not = 000 (refresh only command), Subtest Addr 36:40 is a don't care.
36	RW	MCBIST_CFG_TEST02_COMPL_1ST_CMD: Complement the data for the first subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
37	RW	MCBIST_CFG_TEST02_COMPL_2ND_CMD: Complement the data for the second subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
38	RW	MCBIST_CFG_TEST02_COMPL_3RD_CMD: Complement the data for the third subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
39	RW	MCBIST_CFG_TEST02_ADDR_REV_MODE: Generate addresses in reverse order.
40	RW	MCBIST_CFG_TEST02_ADDR_RAND_MODE: Generate addresses in random order.
41:43	RW	MCBIST_CFG_TEST02_DATA_MODE: Data mode.
44	RW	MCBIST_CFG_TEST02_ECC_MODE: Generate and check data with the ECC.
45	RW	MCBIST_CFG_TEST02_DONE: Done bit.
46:47	RW	MCBIST_CFG_TEST02_ADDR_SEL: Address select mode.
48:51	RW	MCBIST_CFG_TEST03_OP_TYPE: Operation type. • If Subtest(48:51) = 0111 and 57:59(Data mode) = 000 (goto command), Subtest Addr 52:56 specifies which subtest address to change to (used for looping). • If Subtest(48:51) = 0111 and 57:59(Data mode) not = 000 (refresh only command), Subtest Addr 52:56 is a don't care.
52	RW	MCBIST_CFG_TEST03_COMPL_1ST_CMD: Complement the data for the first subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
53	RW	MCBIST_CFG_TEST03_COMPL_2ND_CMD: Complement the data for the second subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
54	RW	MCBIST_CFG_TEST03_COMPL_3RD_CMD: Complement the data for the third subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
55	RW	MCBIST_CFG_TEST03_ADDR_REV_MODE: Generate addresses in reverse order.
56	RW	MCBIST_CFG_TEST03_ADDR_RAND_MODE: Generate addresses in random order.
57:59	RW	MCBIST_CFG_TEST03_DATA_MODE: Data mode.
60	RW	MCBIST_CFG_TEST03_ECC_MODE: Generate and check data with the ECC.
61	RW	MCBIST_CFG_TEST03_DONE: Done bit.
62:63	RW	MCBIST_CFG_TEST03_ADDR_SEL: Address select mode.

Register Name	**MCBIST Memory Register 1**
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBMR1Q
Address	00000000070123A9 (SCOM)
Description	MCBIST Memory Register 1

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MCBIST_CFG_TEST04_OP_TYPE: Operation type. • If Subtest(0:3) = 0111 and 9:11(Data mode) = 000 (goto command), Subtest Addr 4:8 specifies which subtest address to change to (used for looping). • If Subtest(0:3) = 0111 and 9:11(Data mode) not = 000 (refresh only command), Subtest Addr 4:8 is a don't care.
4	RW	MCBIST_CFG_TEST04_COMPL_1ST_CMD: Complement the data for the first subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
5	RW	MCBIST_CFG_TEST04_COMPL_2ND_CMD: Complement the data for the second subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
6	RW	MCBIST_CFG_TEST04_COMPL_3RD_CMD: Complement the data for the third subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
7	RW	MCBIST_CFG_TEST04_ADDR_REV_MODE: Generate addresses in reverse order.
8	RW	MCBIST_CFG_TEST04_ADDR_RAND_MODE: Generate addresses in random order.
9:11	RW	MCBIST_CFG_TEST04_DATA_MODE: Data mode.
12	RW	MCBIST_CFG_TEST04_ECC_MODE: Generate and check data with the ECC.
13	RW	MCBIST_CFG_TEST04_DONE: Done bit.
14:15	RW	MCBIST_CFG_TEST04_ADDR_SEL: Address select mode.
16:19	RW	MCBIST_CFG_TEST05_OP_TYPE: Operation type. • If Subtest(16:19) = 0111 and 25:27(Data mode) = 000 (goto command), Subtest Addr 20:24 specifies which subtest address to change to (used for looping). • If Subtest(16:19) = 0111 and 25:27(Data mode) not = 000 (refresh only command), Subtest Addr 20:24 is a don't care.
20	RW	MCBIST_CFG_TEST05_COMPL_1ST_CMD: Complement the data for the first subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
21	RW	MCBIST_CFG_TEST05_COMPL_2ND_CMD: Complement the data for the second subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
22	RW	MCBIST_CFG_TEST05_COMPL_3RD_CMD: Complement the data for the third subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
23	RW	MCBIST_CFG_TEST05_ADDR_REV_MODE: Generate addresses in reverse order.
24	RW	MCBIST_CFG_TEST05_ADDR_RAND_MODE: Generate addresses in random order.
25:27	RW	MCBIST_CFG_TEST05_DATA_MODE: Data mode.
28	RW	MCBIST_CFG_TEST05_ECC_MODE: Generate and check data with the ECC.
29	RW	MCBIST_CFG_TEST05_DONE: Done bit.
30:31	RW	MCBIST_CFG_TEST05_ADDR_SEL: Address select mode.

Bits	SCOM	Field Mnemonic: Description
32:35	RW	MCBIST_CFG_TEST06_OP_TYPE: Operation type. • If Subtest(32:35) = 0111 and 41:43(Data mode) = 000 (goto command), Subtest Addr 36:40 specifies which subtest address to change to (used for looping). • If Subtest(32:35) = 0111 and 41:43(Data mode) not = 000 (refresh only command), Subtest Addr 36:40 is a don't care.
36	RW	MCBIST_CFG_TEST06_COMPL_1ST_CMD: Complement the data for the first subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
37	RW	MCBIST_CFG_TEST06_COMPL_2ND_CMD: Complement the data for the second subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
38	RW	MCBIST_CFG_TEST06_COMPL_3RD_CMD: Complement the data for the third subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
39	RW	MCBIST_CFG_TEST06_ADDR_REV_MODE: Generate addresses in reverse order.
40	RW	MCBIST_CFG_TEST06_ADDR_RAND_MODE: Generate addresses in random order.
41:43	RW	MCBIST_CFG_TEST06_DATA_MODE: Data mode.
44	RW	MCBIST_CFG_TEST06_ECC_MODE: Generate and check data with the ECC.
45	RW	MCBIST_CFG_TEST06_DONE: Done bit.
46:47	RW	MCBIST_CFG_TEST06_ADDR_SEL: Address select mode.
48:51	RW	MCBIST_CFG_TEST07_OP_TYPE: Operation type. • If Subtest(48:51) = 0111 and 57:59(Data mode) = 000 (goto command), Subtest Addr 52:56 specifies which subtest address to change to (used for looping). • If Subtest(48:51) = 0111 and 57:59(Data mode) not = 000 (refresh only command), Subtest Addr 52:56 is a don't care.
52	RW	MCBIST_CFG_TEST07_COMPL_1ST_CMD: Complement the data for the first subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
53	RW	MCBIST_CFG_TEST07_COMPL_2ND_CMD: Complement the data for the second subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
54	RW	MCBIST_CFG_TEST07_COMPL_3RD_CMD: Complement the data for the third subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
55	RW	MCBIST_CFG_TEST07_ADDR_REV_MODE: Generate addresses in reverse order.
56	RW	MCBIST_CFG_TEST07_ADDR_RAND_MODE: Generate addresses in random order.
57:59	RW	MCBIST_CFG_TEST07_DATA_MODE: Data mode.
60	RW	MCBIST_CFG_TEST07_ECC_MODE: Generate and check data with the ECC.
61	RW	MCBIST_CFG_TEST07_DONE: Done bit.
62:63	RW	MCBIST_CFG_TEST07_ADDR_SEL: Address select mode.

Register Name	**MCBIST Memory Register 2**
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBMR2Q
Address	00000000070123AA (SCOM)
Description	MCBIST Memory Register 2

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MCBIST_CFG_TEST08_OP_TYPE: Operation type. • If Subtest(0:3) = 0111 and 9:11(Data mode) = 000 (goto command), Subtest Addr 4:8 specifies which subtest address to change to (used for looping). • If Subtest(0:3) = 0111 and 9:11(Data mode) not = 000 (refresh only command), Subtest Addr 4:8 is a don't care.
4	RW	MCBIST_CFG_TEST08_COMPL_1ST_CMD: Complement the data for the first subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
5	RW	MCBIST_CFG_TEST08_COMPL_2ND_CMD: Complement the data for the second subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
6	RW	MCBIST_CFG_TEST08_COMPL_3RD_CMD: Complement the data for the third subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
7	RW	MCBIST_CFG_TEST08_ADDR_REV_MODE: Generate addresses in reverse order.
8	RW	MCBIST_CFG_TEST08_ADDR_RAND_MODE: Generate addresses in random order.
9:11	RW	MCBIST_CFG_TEST08_DATA_MODE: Data mode.
12	RW	MCBIST_CFG_TEST08_ECC_MODE: Generate and check data with the ECC.
13	RW	MCBIST_CFG_TEST08_DONE: Done bit.
14:15	RW	MCBIST_CFG_TEST08_ADDR_SEL: Address select mode.
16:19	RW	MCBIST_CFG_TEST09_OP_TYPE: Operation type. • If Subtest(16:19) = 0111 and 25:27(Data mode) = 000 (goto command), Subtest Addr 20:24 specifies which subtest address to change to (used for looping). • If Subtest(16:19) = 0111 and 25:27(Data mode) not = 000 (refresh only command), Subtest Addr 20:24 is a don't care.
20	RW	MCBIST_CFG_TEST09_COMPL_1ST_CMD: Complement the data for the first subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
21	RW	MCBIST_CFG_TEST09_COMPL_2ND_CMD: Complement the data for the second subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
22	RW	MCBIST_CFG_TEST09_COMPL_3RD_CMD: Complement the data for the third subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
23	RW	MCBIST_CFG_TEST09_ADDR_REV_MODE: Generate addresses in reverse order.
24	RW	MCBIST_CFG_TEST09_ADDR_RAND_MODE: Generate addresses in random order.
25:27	RW	MCBIST_CFG_TEST09_DATA_MODE: Data mode.
28	RW	MCBIST_CFG_TEST09_ECC_MODE: Generate and check data with the ECC.
29	RW	MCBIST_CFG_TEST09_DONE: Done bit.
30:31	RW	MCBIST_CFG_TEST09_ADDR_SEL: Address select mode.
32:35	RW	MCBIST_CFG_TEST10_OP_TYPE: Operation type. • If Subtest(32:35) = 0111 and 41:43(Data mode) = 000 (goto command), Subtest Addr 36:40 specifies which subtest address to change to (used for looping). • If Subtest(32:35) = 0111 and 41:43(Data mode) not = 000 (refresh only command), Subtest Addr 36:40 is a don't care.
36	RW	MCBIST_CFG_TEST10_COMPL_1ST_CMD: Complement the data for the first subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
37	RW	MCBIST_CFG_TEST10_COMPL_2ND_CMD: Complement the data for the second subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.

Bits	SCOM	Field Mnemonic: Description
38	RW	MCBIST_CFG_TEST10_COMPL_3RD_CMD: Complement the data for the third subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
39	RW	MCBIST_CFG_TEST10_ADDR_REV_MODE: Generate addresses in reverse order.
40	RW	MCBIST_CFG_TEST10_ADDR_RAND_MODE: Generate addresses in random order.
41:43	RW	MCBIST_CFG_TEST10_DATA_MODE: Data mode.
44	RW	MCBIST_CFG_TEST10_ECC_MODE: Generate and check data with the ECC.
45	RW	MCBIST_CFG_TEST10_DONE: Done bit.
46:47	RW	MCBIST_CFG_TEST10_ADDR_SEL: Address select mode.
48:51	RW	MCBIST_CFG_TEST11_OP_TYPE: Operation type. • If Subtest(48:51) = 0111 and 57:59(Data mode) = 000 (goto command), Subtest Addr 52:56 specifies which subtest address to change to (used for looping). • If Subtest(48:51) = 0111 and 57:59(Data mode) not = 000 (refresh only command), Subtest Addr 52:56 is a don't care.
52	RW	MCBIST_CFG_TEST11_COMPL_1ST_CMD: Complement the data for the first subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
53	RW	MCBIST_CFG_TEST11_COMPL_2ND_CMD: Complement the data for the second subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
54	RW	MCBIST_CFG_TEST11_COMPL_3RD_CMD: Complement the data for the third subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
55	RW	MCBIST_CFG_TEST11_ADDR_REV_MODE: Generate addresses in reverse order.
56	RW	MCBIST_CFG_TEST11_ADDR_RAND_MODE: Generate addresses in random order.
57:59	RW	MCBIST_CFG_TEST11_DATA_MODE: Data mode.
60	RW	MCBIST_CFG_TEST11_ECC_MODE: Generate and check data with the ECC.
61	RW	MCBIST_CFG_TEST11_DONE: Done bit.
62:63	RW	MCBIST_CFG_TEST11_ADDR_SEL: Address select mode.

Register Name	**MCBIST Memory Register 3**
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBMR3Q
Address	00000000070123AB (SCOM)
Description	MCBIST Memory Register 3

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MCBIST_CFG_TEST12_OP_TYPE: Operation type. • If Subtest(0:3) = 0111 and 9:11(Data mode) = 000 (goto command), Subtest Addr 4:8 specifies which subtest address to change to (used for looping). • If Subtest(0:3) = 0111 and 9:11(Data mode) not = 000 (refresh only command), Subtest Addr 4:8 is a don't care.
4	RW	MCBIST_CFG_TEST12_COMPL_1ST_CMD: Complement the data for the first subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
5	RW	MCBIST_CFG_TEST12_COMPL_2ND_CMD: Complement the data for the second subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
6	RW	MCBIST_CFG_TEST12_COMPL_3RD_CMD: Complement the data for the third subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.

Bits	SCOM	Field Mnemonic: Description
7	RW	MCBIST_CFG_TEST12_ADDR_REV_MODE: Generate addresses in reverse order.
8	RW	MCBIST_CFG_TEST12_ADDR_RAND_MODE: Generate addresses in random order.
9:11	RW	MCBIST_CFG_TEST12_DATA_MODE: Data mode.
12	RW	MCBIST_CFG_TEST12_ECC_MODE: Generate and check data with the ECC.
13	RW	MCBIST_CFG_TEST12_DONE: Done bit.
14:15	RW	MCBIST_CFG_TEST12_ADDR_SEL: Address select mode.
16:19	RW	MCBIST_CFG_TEST13_OP_TYPE: Operation type. • If Subtest(16:19) = 0111 and 25:27(Data mode) = 000 (goto command), Subtest Addr 20:24 specifies which subtest address to change to (used for looping). • If Subtest(16:19) = 0111 and 25:27(Data mode) not = 000 (refresh only command), Subtest Addr 20:24 is a don't care.
20	RW	MCBIST_CFG_TEST13_COMPL_1ST_CMD: Complement the data for the first subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
21	RW	MCBIST_CFG_TEST13_COMPL_2ND_CMD: Complement the data for the second subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
22	RW	MCBIST_CFG_TEST13_COMPL_3RD_CMD: Complement the data for the third subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
23	RW	MCBIST_CFG_TEST13_ADDR_REV_MODE: Generate addresses in reverse order.
24	RW	MCBIST_CFG_TEST13_ADDR_RAND_MODE: Generate addresses in random order.
25:27	RW	MCBIST_CFG_TEST13_DATA_MODE: Data mode.
28	RW	MCBIST_CFG_TEST13_ECC_MODE: Generate and check data with the ECC.
29	RW	MCBIST_CFG_TEST13_DONE: Done bit.
30:31	RW	MCBIST_CFG_TEST13_ADDR_SEL: Address select mode.
32:35	RW	MCBIST_CFG_TEST14_OP_TYPE: Operation type. • If Subtest(32:35) = 0111 and 41:43(Data mode) = 000 (goto command), Subtest Addr 36:40 specifies which subtest address to change to (used for looping). • If Subtest(32:35) = 0111 and 41:43(Data mode) not = 000 (refresh only command), Subtest Addr 36:40 is a don't care.
36	RW	MCBIST_CFG_TEST14_COMPL_1ST_CMD: Complement the data for the first subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
37	RW	MCBIST_CFG_TEST14_COMPL_2ND_CMD: Complement the data for the second subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
38	RW	MCBIST_CFG_TEST14_COMPL_3RD_CMD: Complement the data for the third subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
39	RW	MCBIST_CFG_TEST14_ADDR_REV_MODE: Generate addresses in reverse order.
40	RW	MCBIST_CFG_TEST14_ADDR_RAND_MODE: Generate addresses in random order.
41:43	RW	MCBIST_CFG_TEST14_DATA_MODE: Data mode.
44	RW	MCBIST_CFG_TEST14_ECC_MODE: Generate and check data with the ECC.
45	RW	MCBIST_CFG_TEST14_DONE: Done bit.
46:47	RW	MCBIST_CFG_TEST14_ADDR_SEL: Address select mode.

Bits	SCOM	Field Mnemonic: Description
48:51	RW	MCBIST_CFG_TEST15_OP_TYPE: Operation type. • If Subtest(48:51) = 0111 and 57:59(Data mode) = 000 (goto command), Subtest Addr 52:56 specifies which subtest address to change to (used for looping). • If Subtest(48:51) = 0111 and 57:59(Data mode) not = 000 (refresh only command), Subtest Addr 52:56 is a don't care.
52	RW	MCBIST_CFG_TEST15_COMPL_1ST_CMD: Complement the data for the first subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
53	RW	MCBIST_CFG_TEST15_COMPL_2ND_CMD: Complement the data for the second subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
54	RW	MCBIST_CFG_TEST15_COMPL_3RD_CMD: Complement the data for the third subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
55	RW	MCBIST_CFG_TEST15_ADDR_REV_MODE: Generate addresses in reverse order.
56	RW	MCBIST_CFG_TEST15_ADDR_RAND_MODE: Generate addresses in random order.
57:59	RW	MCBIST_CFG_TEST15_DATA_MODE: Data mode.
60	RW	MCBIST_CFG_TEST15_ECC_MODE: Generate and check data with the ECC.
61	RW	MCBIST_CFG_TEST15_DONE: Done bit.
62:63	RW	MCBIST_CFG_TEST15_ADDR_SEL: Address select mode.

Register Name	**MCBIST Memory Register 4**
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBMR4Q
Address	00000000070123AC (SCOM)
Description	MCBIST Memory Register 4

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MCBIST_CFG_TEST16_OP_TYPE: Operation type. • If Subtest(0:3) = 0111 and 9:11(Data mode) = 000 (goto command), Subtest Addr 4:8 specifies which subtest address to change to (used for looping). • If Subtest(0:3) = 0111 and 9:11(Data mode) not = 000 (refresh only command), Subtest Addr 4:8 is a don't care.
4	RW	MCBIST_CFG_TEST16_COMPL_1ST_CMD: Complement the data for the first subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
5	RW	MCBIST_CFG_TEST16_COMPL_2ND_CMD: Complement the data for the second subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
6	RW	MCBIST_CFG_TEST16_COMPL_3RD_CMD: Complement the data for the third subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
7	RW	MCBIST_CFG_TEST16_ADDR_REV_MODE: Generate addresses in reverse order.
8	RW	MCBIST_CFG_TEST16_ADDR_RAND_MODE: Generate addresses in random order.
9:11	RW	MCBIST_CFG_TEST16_DATA_MODE: Data mode.
12	RW	MCBIST_CFG_TEST16_ECC_MODE: Generate and check data with the ECC.
13	RW	MCBIST_CFG_TEST16_DONE: Done bit.
14:15	RW	MCBIST_CFG_TEST16_ADDR_SEL: Address select mode.

Bits	SCOM	Field Mnemonic: Description
16:19	RW	MCBIST_CFG_TEST17_OP_TYPE: Operation type. • If Subtest(16:19) = 0111 and 25:27(Data mode) = 000 (goto command), Subtest Addr 20:24 specifies which subtest address to change to (used for looping). • If Subtest(16:19) = 0111 and 25:27(Data mode) not = 000 (refresh only command), Subtest Addr 20:24 is a don't care.
20	RW	MCBIST_CFG_TEST17_COMPL_1ST_CMD: Complement the data for the first subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
21	RW	MCBIST_CFG_TEST17_COMPL_2ND_CMD: Complement the data for the second subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
22	RW	MCBIST_CFG_TEST17_COMPL_3RD_CMD: Complement the data for the third subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
23	RW	MCBIST_CFG_TEST17_ADDR_REV_MODE: Generate addresses in reverse order.
24	RW	MCBIST_CFG_TEST17_ADDR_RAND_MODE: Generate addresses in random order.
25:27	RW	MCBIST_CFG_TEST17_DATA_MODE: Data mode.
28	RW	MCBIST_CFG_TEST17_ECC_MODE: Generate and check data with the ECC.
29	RW	MCBIST_CFG_TEST17_DONE: Done bit.
30:31	RW	MCBIST_CFG_TEST17_ADDR_SEL: Address select mode.
32:35	RW	MCBIST_CFG_TEST18_OP_TYPE: Operation type. • If Subtest(32:35) = 0111 and 41:43(Data mode) = 000 (goto command), Subtest Addr 36:40 specifies which subtest address to change to (used for looping). • If Subtest(32:35) = 0111 and 41:43(Data mode) not = 000 (refresh only command), Subtest Addr 36:40 is a don't care.
36	RW	MCBIST_CFG_TEST18_COMPL_1ST_CMD: Complement the data for the first subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
37	RW	MCBIST_CFG_TEST18_COMPL_2ND_CMD: Complement the data for the second subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
38	RW	MCBIST_CFG_TEST18_COMPL_3RD_CMD: Complement the data for the third subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
39	RW	MCBIST_CFG_TEST18_ADDR_REV_MODE: Generate addresses in reverse order.
40	RW	MCBIST_CFG_TEST18_ADDR_RAND_MODE: Generate addresses in random order.
41:43	RW	MCBIST_CFG_TEST18_DATA_MODE: Data mode.
44	RW	MCBIST_CFG_TEST18_ECC_MODE: Generate and check data with the ECC.
45	RW	MCBIST_CFG_TEST18_DONE: Done bit.
46:47	RW	MCBIST_CFG_TEST18_ADDR_SEL: Address select mode.
48:51	RW	MCBIST_CFG_TEST19_OP_TYPE: Operation type. • If Subtest(48:51) = 0111 and 57:59(Data mode) = 000 (goto command), Subtest Addr 52:56 specifies which subtest address to change to (used for looping). • If Subtest(48:51) = 0111 and 57:59(Data mode) not = 000 (refresh only command), Subtest Addr 52:56 is a don't care.
52	RW	MCBIST_CFG_TEST19_COMPL_1ST_CMD: Complement the data for the first subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
53	RW	MCBIST_CFG_TEST19_COMPL_2ND_CMD: Complement the data for the second subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.

Bits	SCOM	Field Mnemonic: Description
54	RW	MCBIST_CFG_TEST19_COMPL_3RD_CMD: Complement the data for the third subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
55	RW	MCBIST_CFG_TEST19_ADDR_REV_MODE: Generate addresses in reverse order.
56	RW	MCBIST_CFG_TEST19_ADDR_RAND_MODE: Generate addresses in random order.
57:59	RW	MCBIST_CFG_TEST19_DATA_MODE: Data mode.
60	RW	MCBIST_CFG_TEST19_ECC_MODE: Generate and check data with the ECC.
61	RW	MCBIST_CFG_TEST19_DONE: Done bit.
62:63	RW	MCBIST_CFG_TEST19_ADDR_SEL: Address select mode.

Register Name	**MCBIST Memory Register 5**
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBMR5Q
Address	00000000070123AD (SCOM)
Description	MCBIST Memory Register 5

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MCBIST_CFG_TEST20_OP_TYPE: Operation type. • If Subtest(0:3) = 0111 and 9:11(Data mode) = 000 (goto command), Subtest Addr 4:8 specifies which subtest address to change to (used for looping). • If Subtest(0:3) = 0111 and 9:11(Data mode) not = 000 (refresh only command), Subtest Addr 4:8 is a don't care.
4	RW	MCBIST_CFG_TEST20_COMPL_1ST_CMD: Complement the data for the first subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
5	RW	MCBIST_CFG_TEST20_COMPL_2ND_CMD: Complement the data for the second subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
6	RW	MCBIST_CFG_TEST20_COMPL_3RD_CMD: Complement the data for the third subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
7	RW	MCBIST_CFG_TEST20_ADDR_REV_MODE: Generate addresses in reverse order.
8	RW	MCBIST_CFG_TEST20_ADDR_RAND_MODE: Generate addresses in random order.
9:11	RW	MCBIST_CFG_TEST20_DATA_MODE: Data mode.
12	RW	MCBIST_CFG_TEST20_ECC_MODE: Generate and check data with the ECC.
13	RW	MCBIST_CFG_TEST20_DONE: Done bit.
14:15	RW	MCBIST_CFG_TEST20_ADDR_SEL: Address select mode.
16:19	RW	MCBIST_CFG_TEST21_OP_TYPE: Operation type. • If Subtest(16:19) = 0111 and 25:27(Data mode) = 000 (goto command), Subtest Addr 20:24 specifies which subtest address to change to (used for looping). • If Subtest(16:19) = 0111 and 25:27(Data mode) not = 000 (refresh only command), Subtest Addr 20:24 is a don't care.
20	RW	MCBIST_CFG_TEST21_COMPL_1ST_CMD: Complement the data for the first subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
21	RW	MCBIST_CFG_TEST21_COMPL_2ND_CMD: Complement the data for the second subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
22	RW	MCBIST_CFG_TEST21_COMPL_3RD_CMD: Complement the data for the third subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.

Bits	SCOM	Field Mnemonic: Description
23	RW	MCBIST_CFG_TEST21_ADDR_REV_MODE: Generate addresses in reverse order.
24	RW	MCBIST_CFG_TEST21_ADDR_RAND_MODE: Generate addresses in random order.
25:27	RW	MCBIST_CFG_TEST21_DATA_MODE: Data mode.
28	RW	MCBIST_CFG_TEST21_ECC_MODE: Generate and check data with the ECC.
29	RW	MCBIST_CFG_TEST21_DONE: Done bit.
30:31	RW	MCBIST_CFG_TEST21_ADDR_SEL: Address select mode.
32:35	RW	MCBIST_CFG_TEST22_OP_TYPE: Operation type. • If Subtest(32:35) = 0111 and 41:43(Data mode) = 000 (goto command), Subtest Addr 36:40 specifies which subtest address to change to (used for looping). • If Subtest(32:35) = 0111 and 41:43(Data mode) not = 000 (refresh only command), Subtest Addr 36:40 is a don't care.
36	RW	MCBIST_CFG_TEST22_COMPL_1ST_CMD: Complement the data for the first subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
37	RW	MCBIST_CFG_TEST22_COMPL_2ND_CMD: Complement the data for the second subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
38	RW	MCBIST_CFG_TEST22_COMPL_3RD_CMD: Complement the data for the third subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
39	RW	MCBIST_CFG_TEST22_ADDR_REV_MODE: Generate addresses in reverse order.
40	RW	MCBIST_CFG_TEST22_ADDR_RAND_MODE: Generate addresses in random order.
41:43	RW	MCBIST_CFG_TEST22_DATA_MODE: Data mode.
44	RW	MCBIST_CFG_TEST22_ECC_MODE: Generate and check data with the ECC.
45	RW	MCBIST_CFG_TEST22_DONE: Done bit.
46:47	RW	MCBIST_CFG_TEST22_ADDR_SEL: Address select mode.
48:51	RW	MCBIST_CFG_TEST23_OP_TYPE: Operation type. • If Subtest(48:51) = 0111 and 57:59(Data mode) = 000 (goto command), Subtest Addr 52:56 specifies which subtest address to change to (used for looping). • If Subtest(48:51) = 0111 and 57:59(Data mode) not = 000 (refresh only command), Subtest Addr 52:56 is a don't care.
52	RW	MCBIST_CFG_TEST23_COMPL_1ST_CMD: Complement the data for the first subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
53	RW	MCBIST_CFG_TEST23_COMPL_2ND_CMD: Complement the data for the second subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
54	RW	MCBIST_CFG_TEST23_COMPL_3RD_CMD: Complement the data for the third subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
55	RW	MCBIST_CFG_TEST23_ADDR_REV_MODE: Generate addresses in reverse order.
56	RW	MCBIST_CFG_TEST23_ADDR_RAND_MODE: Generate addresses in random order.
57:59	RW	MCBIST_CFG_TEST23_DATA_MODE: Data mode.
60	RW	MCBIST_CFG_TEST23_ECC_MODE: Generate and check data with the ECC.
61	RW	MCBIST_CFG_TEST23_DONE: Done bit.
62:63	RW	MCBIST_CFG_TEST23_ADDR_SEL: Address select mode.

Register Name	MCBIST Memory Register 6
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBMR6Q
Address	00000000070123AE (SCOM)
Description	MCBIST Memory Register 6

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MCBIST_CFG_TEST24_OP_TYPE: Operation type. • If Subtest(0:3) = 0111 and 9:11(Data mode) = 000 (goto command), Subtest Addr 4:8 specifies which subtest address to change to (used for looping). • If Subtest(0:3) = 0111 and 9:11(Data mode) not = 000 (refresh only command), Subtest Addr 4:8 is a don't care.
4	RW	MCBIST_CFG_TEST24_COMPL_1ST_CMD: Complement the data for the first subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
5	RW	MCBIST_CFG_TEST24_COMPL_2ND_CMD: Complement the data for the second subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
6	RW	MCBIST_CFG_TEST24_COMPL_3RD_CMD: Complement the data for the third subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
7	RW	MCBIST_CFG_TEST24_ADDR_REV_MODE: Generate addresses in reverse order.
8	RW	MCBIST_CFG_TEST24_ADDR_RAND_MODE: Generate addresses in random order.
9:11	RW	MCBIST_CFG_TEST24_DATA_MODE: Data mode.
12	RW	MCBIST_CFG_TEST24_ECC_MODE: Generate and check data with the ECC.
13	RW	MCBIST_CFG_TEST24_DONE: Done bit.
14:15	RW	MCBIST_CFG_TEST24_ADDR_SEL: Address select mode.
16:19	RW	MCBIST_CFG_TEST25_OP_TYPE: Operation type. • If Subtest(16:19) = 0111 and 25:27(Data mode) = 000 (goto command), Subtest Addr 20:24 specifies which subtest address to change to (used for looping). • If Subtest(16:19) = 0111 and 25:27(Data mode) not = 000 (refresh only command), Subtest Addr 20:24 is a don't care.
20	RW	MCBIST_CFG_TEST25_COMPL_1ST_CMD: Complement the data for the first subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
21	RW	MCBIST_CFG_TEST25_COMPL_2ND_CMD: Complement the data for the second subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
22	RW	MCBIST_CFG_TEST25_COMPL_3RD_CMD: Complement the data for the third subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
23	RW	MCBIST_CFG_TEST25_ADDR_REV_MODE: Generate addresses in reverse order.
24	RW	MCBIST_CFG_TEST25_ADDR_RAND_MODE: Generate addresses in random order.
25:27	RW	MCBIST_CFG_TEST25_DATA_MODE: Data mode.
28	RW	MCBIST_CFG_TEST25_ECC_MODE: Generate and check data with the ECC.
29	RW	MCBIST_CFG_TEST25_DONE: Done bit.
30:31	RW	MCBIST_CFG_TEST25_ADDR_SEL: Address select mode.

Bits	SCOM	Field Mnemonic: Description
32:35	RW	MCBIST_CFG_TEST26_OP_TYPE: Operation type. • If Subtest(32:35) = 0111 and 41:43(Data mode) = 000 (goto command), Subtest Addr 36:40 specifies which subtest address to change to (used for looping). • If Subtest(32:35) = 0111 and 41:43(Data mode) not = 000 (refresh only command), Subtest Addr 36:40 is a don't care.
36	RW	MCBIST_CFG_TEST26_COMPL_1ST_CMD: Complement the data for the first subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
37	RW	MCBIST_CFG_TEST26_COMPL_2ND_CMD: Complement the data for the second subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
38	RW	MCBIST_CFG_TEST26_COMPL_3RD_CMD: Complement the data for the third subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
39	RW	MCBIST_CFG_TEST26_ADDR_REV_MODE: Generate addresses in reverse order.
40	RW	MCBIST_CFG_TEST26_ADDR_RAND_MODE: Generate addresses in random order.
41:43	RW	MCBIST_CFG_TEST26_DATA_MODE: Data mode.
44	RW	MCBIST_CFG_TEST26_ECC_MODE: Generate and check data with the ECC.
45	RW	MCBIST_CFG_TEST26_DONE: Done bit.
46:47	RW	MCBIST_CFG_TEST26_ADDR_SEL: Address select mode.
48:51	RW	MCBIST_CFG_TEST27_OP_TYPE: Operation type. • If Subtest(48:51) = 0111 and 57:59(Data mode) = 000 (goto command), Subtest Addr 52:56 specifies which subtest address to change to (used for looping). • If Subtest(48:51) = 0111 and 57:59(Data mode) not = 000 (refresh only command), Subtest Addr 52:56 is a don't care.
52	RW	MCBIST_CFG_TEST27_COMPL_1ST_CMD: Complement the data for the first subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
53	RW	MCBIST_CFG_TEST27_COMPL_2ND_CMD: Complement the data for the second subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
54	RW	MCBIST_CFG_TEST27_COMPL_3RD_CMD: Complement the data for the third subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
55	RW	MCBIST_CFG_TEST27_ADDR_REV_MODE: Generate addresses in reverse order.
56	RW	MCBIST_CFG_TEST27_ADDR_RAND_MODE: Generate addresses in random order.
57:59	RW	MCBIST_CFG_TEST27_DATA_MODE: Data mode.
60	RW	MCBIST_CFG_TEST27_ECC_MODE: Generate and check data with the ECC.
61	RW	MCBIST_CFG_TEST27_DONE: Done bit.
62:63	RW	MCBIST_CFG_TEST27_ADDR_SEL: Address select mode.

Register Name	**MCBIST Memory Parameter Register**
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBPARMQ
Address	00000000070123AF (SCOM)
Description	MCBIST Memory Parameter Register

Bits	SCOM	Field Mnemonic: Description
0:11	RW	MCBPARMQ_CFG_MIN_CMD_GAP: This is the minimum number of cycles between commands when cfg_en_randcmd_gap is a 0 (disabled). If cfg_en_randcmd_gap is a 1, the last 7 bits become a seed for the LFSR that randomly generates the gap intervals between 1 - 127. A value of all zeros forces the MCBIST to issue commands as fast as possible. The value of this field can be multiplied by 2^{13} when cfg_min_gap_timebase is set to 1.
12	RW	MCBPARMQ_CFG_MIN_GAP_TIMEBASE: When set to a 1 and cfg_en_randcmd_gap is a 0, the number of minimum cycles between commands is cfg_min_cmd_gap multiplied by 2^{13}.
13:24	RW	MCBPARMQ_CFG_MIN_CMD_GAP_BLIND_STEER: This is the minimum number of cycles between commands when cfg_en_randcmd_gap = 0, cfg_ddr4e_blind_steer_mode = 1, and doing a steer command. The value of this field can be multiplied by 2^{13} when cfg_min_gap_timebase_blind_steer is set to 1.
25	RW	MCBPARMQ_CFG_MIN_GAP_TIMEBASE_BLIND_STEER: When set to a 1 and cfg_en_randcmd_gap is a 0, the number of minimum cycles between commands is cfg_min_cmd_gap multiplied by 2^{13}.
26:49	RW	MCBPARMQ_RESERVED_26_49: Not used.
50:52	RW	MCBPARMQ_CFG_RANDCMD_WGT: Specifies the weighting of random commands as follows (%Read %Write):
53:58	RW	MCBPARMQ_RESERVED_53_58: Not used.
59	RW	MCBPARMQ_CFG_CLOCK_MONITOR_EN: Enable for the clock monitor (outside MCBIST).
60	RW	MCBPARMQ_CFG_EN_RANDCMD_GAP: When set to a 1, random command gaps from 1 - 1023 cycles are enabled and cfg_min_cmd_gap is disabled. It becomes a seed for an LFSR that is randomly generating 1 - 127 cycle gaps (there is another 8-bit LFSR that is generating a 1 - 8 cycle multiplier).
61:62	RW	MCBPARMQ_CFG_RANDGAP_WGT: Forces the following command gap intervals when cfg_en_randcmd_gap is a 1: 00 = 1 to 1023 cycles. 01 = 1 to 511 cycles. 10 = 1 to 255 cycles. 11 = 1 to 127 cycles.
63	RW	MCBPARMQ_CFG_BC4_EN: BC4 enable. When set, it enables BC4 data mode. This configuration cannot be used in ECC data mode.

Register Name	MCBIST Runtime Counter Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.RUNTIMECTRQ
Address	00000000070123B0 (SCOM)
Description	MCBIST Runtime Counter Register

Bits	SCOM	Field Mnemonic: Description
0:36	RWX	RUNTIMECTRQ_CFG_RUNTIME_CTR: This is the run-time counter facility. This 37-bit counter increments every four memory clock cycles, which gives it a maximum value of 687 seconds at 800 MHz or 824 seconds at 667 MHz.
37:63	RO	Constant = 0b00000000000000000000000000000

Register Name	MCBIST Refresh Control Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBRCRQ
Address	00000000070123B1 (SCOM)
Description	MCBIST Refresh Control Register

Bits	SCOM	Field Mnemonic: Description
0:31	RW	MCBRCRQ_RESERVED_0_31: Not used.
32	RW	MCBRCRQ_CFG_RUNTIME_MCBALL: Configures what the run-time counter counts:
33:37	RW	MCBRCRQ_CFG_RUNTIME_SUBTEST: If bit 32 is a 0, these bits represent the subtest number that should be counted.
38	RW	MCBRCRQ_CFG_RUNTIME_OVERHEAD: If bit 32 is a 1, this bit configures the starting point of the run-time counter:
39	RW	MCBRCRQ_RESERVED_39: Not used.
40:63	RO	Constant = 0b000000000000000000000000

Register Name	Random Data Seed 0 Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBRDS0Q
Address	00000000070123B2 (SCOM)
Description	Random Data Seed 0 Register

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MCBRDS0Q_DGEN_RNDD_SEED0: 24-bit random data seed 0.
24:47	RW	MCBRDS0Q_DGEN_RNDD_SEED1: 24-bit random data seed 1.

Register Name	Random Data Seed 1 Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBRDS1Q
Address	00000000070123B3 (SCOM)
Description	Random Data Seed 1 Register

Bits	SCOM	Field Mnemonic: Description
0:23	RW	MCBRDS1Q_DGEN_RNDD_SEED2: 24-bit random data seed 2.

Bits	SCOM	Field Mnemonic: Description
24:63	RW	MCBRDS1Q_DGEN_RNDD_DATA_MAPPING: Each of the 10 data bytes per burst can be mapped to any of the 9 generated bytes. Each byte is configured by a 4-bit mapping field. (0: 3) configures mapping for Byte0 dq[0: 7] (4: 7) configures mapping for Byte1 dq[8:15] (8:11) configures mapping for Byte2 dq[16:23] (12:15) configures mapping for Byte3 dq[24:31] (16:19) configures mapping for Byte4 dq[32:39] (20:23) configures mapping for Byte5 dq[40:47] (24:27) configures mapping for Byte6 dq[48:55] (28:31) configures mapping for Byte7 dq[56:63] (32:35) configures mapping for Byte8 dq[64:71] (36:39) configures mapping for Byte9 dq[72:79] **Note**: DQ's 72:79 are spares and are *not* used in scale-out design This is how each of those 4-bit fields are decoded: 0000 = Use byte0 of LFSR0. 0001 = Use byte1 of LFSR0. 0010 = Use byte2 of LFSR0. 0011 = Use byte0 of LFSR1. 0100 = Use byte1 of LFSR1. 0101 = Use byte2 of LFSR1. 0110 = Use byte0 of LFSR2. 0111 = Use byte1 of LFSR2. 1000 = Use byte2 of LFSR2.

Register Name	Data Rotate Seed Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBDRSRQ
Address	00000000070123BC (SCOM)
Description	Data Rotate Seed Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MCBDRSRQ_CFG_DATA_ROT_SEED: Bits 0:63 of the data rotate seed.

Register Name	Data Rotate Configuration Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBDRCRQ
Address	00000000070123BD (SCOM)
Description	Data Rotate Configuration Register

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MCBDRCRQ_CFG_DATA_ROT: Bits to shift.
4:19	RW	MCBDRCRQ_CFG_DATA_ROT_SEED: Bits 64:79 of the data rotate seed.
20	RW	MCBDRCRQ_RESERVED_20: These bits control the final inversion of data over to the write data flow. Bit 20 = Invert MA Data.
21:22	RW	MCBDRCRQ_CFG_DATA_SEED_MODE: For fixed and random mode, determines how data seeds are used. 00 = Uses all unique data seeds. 01 = Repeats data seed 0. 10 = Repeats data seed 1. 11 = Repeats data seed 2.
23:63	RW	MCBDRCRQ_RESERVED_23_63: Not used.

Register Name	Fixed Data Seed Burst 0 Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBFD0Q
Address	00000000070123BE (SCOM)
Description	Fixed Data Seed Burst 0 Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MCBFD0Q_CFG_FIXED_SEED: Fixed data seed (0:63).

Register Name	Fixed Data Seed Burst 1 Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBFD1Q
Address	00000000070123BF (SCOM)
Description	Fixed Data Seed Burst 1 Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MCBFD1Q_CFG_FIXED_SEED: Fixed data seed (72:135).

Register Name	Fixed Data Seed Burst 2 Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBFD2Q
Address	00000000070123C0 (SCOM)
Description	Fixed Data Seed Burst 2 Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MCBFD2Q_CFG_FIXED_SEED: Fixed data seed (144:207).

Register Name	Fixed Data Seed Burst 3 Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBFD3Q
Address	00000000070123C1 (SCOM)
Description	Fixed Data Seed Burst 3 Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MCBFD3Q_CFG_FIXED_SEED: Fixed data seed (216:279).

Register Name	Fixed Data Seed Burst 4 Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBFD4Q
Address	00000000070123C2 (SCOM)
Description	Fixed Data Seed Burst 4 Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MCBFD4Q_CFG_FIXED_SEED: Fixed data seed (288:351).

Register Name	Fixed Data Seed Burst 5 Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBFD5Q
Address	00000000070123C3 (SCOM)
Description	Fixed Data Seed Burst 5 Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MCBFD5Q_CFG_FIXED_SEED: Fixed data seed(360:423).

Register Name	Fixed Data Seed Burst 6 Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBFD6Q
Address	00000000070123C4 (SCOM)
Description	Fixed Data Seed Burst 6 Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MCBFD6Q_CFG_FIXED_SEED: Fixed data seed(432:495).

Register Name	Fixed Data Seed Burst 7 Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBFD7Q
Address	00000000070123C5 (SCOM)
Description	Fixed Data Seed Burst 7 Register

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MCBFD7Q_CFG_FIXED_SEED: Fixed data seed(504:567).

Register Name	Fixed Data Seed Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBFDQ
Address	00000000070123C6 (SCOM)
Description	Fixed Data Seed Register

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MCBFDQ_CFG_FIXED_SEED1: DQ(8) burst 1 fixed data seed(64:71).
8:15	RW	MCBFDQ_CFG_FIXED_SEED2: DQ(8) burst 2 fixed data seed(136:143).
16:23	RW	MCBFDQ_CFG_FIXED_SEED3: DQ(8) burst 3 fixed data seed(208:215).
24:31	RW	MCBFDQ_CFG_FIXED_SEED4: DQ(8) burst 4 fixed data seed(280:287).
32:39	RW	MCBFDQ_CFG_FIXED_SEED5: DQ(8) burst 5 fixed data seed(352:359).
40:47	RW	MCBFDQ_CFG_FIXED_SEED6: DQ(8) burst 6 fixed data seed(424:431).
48:55	RW	MCBFDQ_CFG_FIXED_SEED7: DQ(8) burst 7 fixed data seed(496:503).
56:63	RW	MCBFDQ_CFG_FIXED_SEED8: DQ(8) burst 8 fixed data seed(568:575).

Register Name	**Port A Socket 0 Address Map Register 0**
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBAMR0A0Q
Address	00000000070123C8 (SCOM)
Description	Port A Socket 0 Address Map Register 0

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MCBAMR0A0Q_CFG_AMAP_DIMM_SELECT: DIMM select.
6:11	RW	MCBAMR0A0Q_CFG_AMAP_MRANK0: Master rank bit 0 when *not* a *5D* configuration.
12:17	RW	MCBAMR0A0Q_CFG_AMAP_MRANK1: Master rank bit 1 when *not* a 5D configuration.
18:23	RW	MCBAMR0A0Q_RESERVED_18_23: Reserved (removed mrank(2)).
24:29	RW	MCBAMR0A0Q_CFG_AMAP_SRANK0: Slave rank bit 0 (MSB) when *not* a 5D configuration. Master rank bit 0 (MSB) when a 5D configuration.
30:35	RW	MCBAMR0A0Q_CFG_AMAP_SRANK1: Slave rank bit 1 when *not* a 5D configuration. Master rank bit 1 (MSB) when a 5D configuration.
36:41	RW	MCBAMR0A0Q_CFG_AMAP_SRANK2: Slave rank rank bit 2 when *not* a 5D configuration. Master rank bit 2 (MSB) when a 5D configuration.
42:47	RW	MCBAMR0A0Q_CFG_AMAP_BANK2: DRAM bank address bit 2 (MSB).
48:53	RW	MCBAMR0A0Q_CFG_AMAP_BANK1: DRAM bank address bit 2 (MSB).
54:59	RW	MCBAMR0A0Q_CFG_AMAP_BANK0: DRAM bank address bit 1.
60:63	RW	MCBAMR0A0Q_RESERVED_60_63: Reserved.

Register Name	**Port A Socket 0 Address Map Register 1**
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBAMR1A0Q
Address	00000000070123C9 (SCOM)
Description	Port A Socket 0 Address Map Register 1

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MCBAMR1A0Q_CFG_AMAP_BANK_GROUP1: DRAM bank group address bit 1.
6:11	RW	MCBAMR1A0Q_CFG_AMAP_BANK_GROUP0: DRAM bank group address bit 0.
12:17	RW	MCBAMR1A0Q_CFG_AMAP_ROW17: DRAM row address bit 17.
18:23	RW	MCBAMR1A0Q_CFG_AMAP_ROW16: DRAM row address bit 16.
24:29	RW	MCBAMR1A0Q_CFG_AMAP_ROW15: DRAM row address bit 15.
30:35	RW	MCBAMR1A0Q_CFG_AMAP_ROW14: DRAM row address bit 14.
36:41	RW	MCBAMR1A0Q_CFG_AMAP_ROW13: DRAM row address bit 13.
42:47	RW	MCBAMR1A0Q_CFG_AMAP_ROW12: DRAM row address bit 12.
48:53	RW	MCBAMR1A0Q_CFG_AMAP_ROW11: DRAM row address bit 11.
54:59	RW	MCBAMR1A0Q_CFG_AMAP_ROW10: DRAM row address bit 10.
60:63	RW	MCBAMR1A0Q_RESERVED_60_63: Not used.

Register Name	Port A Socket 0 Address Map Register 2
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBAMR2A0Q
Address	00000000070123CA (SCOM)
Description	Port A Socket 0 Address Map Register 2

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MCBAMR2A0Q_CFG_AMAP_ROW9: DRAM row address bit 9.
6:11	RW	MCBAMR2A0Q_CFG_AMAP_ROW8: DRAM row address bit 6.
12:17	RW	MCBAMR2A0Q_CFG_AMAP_ROW7: DRAM row address bit 7.
18:23	RW	MCBAMR2A0Q_CFG_AMAP_ROW6: DRAM row address bit 6.
24:29	RW	MCBAMR2A0Q_CFG_AMAP_ROW5: DRAM row address bit 5.
30:35	RW	MCBAMR2A0Q_CFG_AMAP_ROW4: DRAM row address bit 4.
36:41	RW	MCBAMR2A0Q_CFG_AMAP_ROW3: DRAM row address bit 3.
42:47	RW	MCBAMR2A0Q_CFG_AMAP_ROW2: DRAM row address bit 2.
48:53	RW	MCBAMR2A0Q_CFG_AMAP_ROW1: DRAM row address bit 1.
54:59	RW	MCBAMR2A0Q_CFG_AMAP_ROW0: DRAM row address bit 0.
60:63	RW	MCBAMR2A0Q_RESERVED_60_63: Not used.

Register Name	Port A Socket 0 Address Map Register 3
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBAMR3A0Q
Address	00000000070123CB (SCOM)
Description	Port A Socket 0 Address Map Register 3

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MCBAMR3A0Q_CFG_AMAP_COL9: DRAM column address bit 9.
6:11	RW	MCBAMR3A0Q_CFG_AMAP_COL8: DRAM column address bit 8.
12:17	RW	MCBAMR3A0Q_CFG_AMAP_COL7: DRAM column address bit 7.
18:23	RW	MCBAMR3A0Q_CFG_AMAP_COL6: DRAM column address bit 6.
24:29	RW	MCBAMR3A0Q_CFG_AMAP_COL5: DRAM column address bit 5.
30:35	RW	MCBAMR3A0Q_CFG_AMAP_COL4: DRAM column address bit 4.
36:41	RW	MCBAMR3A0Q_CFG_AMAP_COL3: DRAM column address bit 3.
42:47	RW	MCBAMR3A0Q_CFG_AMAP_COL2: DRAM column address bit. Map to an unused address bit if *not* fixed BL = 4. **Note**: This bit is actually forced to 0 at the MCBIST-RQ interface. To not repeat the command on ADDR, this should be set as a fixed bit.
48:63	RW	MCBAMR3A0Q_RESERVED_48_63: Not used.

Register Name	Start Address 0 Configuration Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBSA0Q
Address	00000000070123CC (SCOM)
Description	Start Address 0 Configuration Register

Bits	SCOM	Field Mnemonic: Description
0:37	RW	MCBSA0Q_CFG_START_ADDR_0: Starting address when subtest addr sel = 00. Ending address when addressing is reversed. **Note**: At least one of the variable bits (non-fixed bits) must be non-zero when using random addressing.

Register Name	Start Address 1 Configuration Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBSA1Q
Address	00000000070123CD (SCOM)
Description	Start Address 1 Configuration Register

Bits	SCOM	Field Mnemonic: Description
0:37	RW	MCBSA1Q_CFG_START_ADDR_1: Starting address when subtest addr sel = 01. Ending address when addressing is reversed. **Note**: At least one of the variable bits (non-fixed bits) must be non-zero when using random addressing.

Register Name	End Address 0 Configuration Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBEA0Q
Address	00000000070123CE (SCOM)
Description	End Address 0 Configuration Register

Bits	SCOM	Field Mnemonic: Description
0:37	RW	MCBEA0Q_CFG_END_ADDR_0: Ending address when subtest addr sel = 00. Starting address when addressing is reversed. **Note**: At least one of the variable bits (non-fixed bits) must be non-zero when using random addressing.

Register Name	End Address 1 Configuration Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBEA1Q
Address	00000000070123CF (SCOM)
Description	End Address 1 Configuration Register

Bits	SCOM	Field Mnemonic: Description
0:37	RW	MCBEA1Q_CFG_END_ADDR_1: Ending address when subtest addr sel = 01. Starting address when addressing is reversed. **Note**: At least one of the variable bits (non-fixed bits) must be non-zero when using random addressing.

Register Name	Start Address 2 Configuration Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBSA2Q
Address	00000000070123D0 (SCOM)
Description	Start Address 2 Configuration Register

Bits	SCOM	Field Mnemonic: Description
0:37	RW	MCBSA2Q_CFG_START_ADDR_2: Starting address when subtest addr sel = 10. Ending address when addressing is reversed. **Note**: At least one of the variable bits (non-fixed bits) must be non-zero when using random addressing.

Register Name	Start Address 3 Configuration Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBSA3Q
Address	00000000070123D1 (SCOM)
Description	Start Address 3 Configuration Register

Bits	SCOM	Field Mnemonic: Description
0:37	RW	MCBSA3Q_CFG_START_ADDR_3: Starting address when subtest addr sel = 11. Ending address when addressing is reversed. **Note**: At least one of the variable bits (non-fixed bits) must be non-zero when using random addressing.

Register Name	End Address 2 Configuration Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBEA2Q
Address	00000000070123D2 (SCOM)
Description	End Address 2 Configuration Register

Bits	SCOM	Field Mnemonic: Description
0:37	RW	MCBEA2Q_CFG_END_ADDR_2: Ending address when subtest addr sel = 10. Starting address when addressing is reversed. **Note**: At least one of the variable bits (non-fixed bits) must be non-zero when using random addressing.

Register Name	End Address 3 Configuration Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBEA3Q
Address	00000000070123D3 (SCOM)
Description	End Address 3 Configuration Register

Bits	SCOM	Field Mnemonic: Description
0:37	RW	MCBEA3Q_CFG_END_ADDR_3: Ending address when subtest addr sel = 11. Starting address when addressing is reversed. **Note**: At least one of the variable bits (non-fixed bits) must be non-zero when using random addressing.

Register Name	Port A0 Address LFSR Configuration Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBLFSRA0Q
Address	00000000070123D4 (SCOM)
Description	Port A0 Address LFSR Configuration Register

Bits	SCOM	Field Mnemonic: Description
0:37	RW	MCBLFSRA0Q_CFG_LFSR_MASK_A0: Used to configure where feed-back XOR points are in the LFSR. If mask bit n is set and does not fall under a fixed bit, LFSR bit n is the result of a shift and XOR of bit 37. If mask bit n is not set and does not fall under a fixed bit, LFSR bit n is the result of just the shift (no XOR).
38:63	RW	MCBLFSRA0Q_RESERVED_38_63: Not used.

Register Name	MCBIST Address Counter Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBACQ
Address	00000000070123D5 (SCOM)
Description	MCBIST Address Counter

Bits	SCOM	Field Mnemonic: Description
0:37	RW	MCBACQ_CFG_ADDRESS_COUNTER: Counts the number of addresses generated internally on a subtest. **Note**: The address is staged out once from an internal generator. Therefore, the actual number of the address corresponding to the output address is MCBAC-1.

Register Name	Address Generator Configuration Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBAGRAQ
Address	00000000070123D6 (SCOM)
Description	Address Generator Configuration Register

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MCBAGRAQ_CFG_FIXED_WIDTH: Sets the number of fixed slots in the address generator. This causes the bits from (MSB to MSB + cfg_fixed_width - 1) to not be included in the address generation. Used in conjunction with the configurable address map registers. For example: Fixed Rank, Fixed Bank, Fixed Row = 3 + 3 + 16 = 22 Program 0x16 defaulted to a fixed Rank setting.
6:9	RW	MCBAGRAQ_CFG_ADDR_COUNTER_MODE: In *forward* address mode, if this is set, the end address is interpreted instead as the number of addresses to execute. In *reverse* address mode, if this is set, the start address is interpreted instead as the number of addresses to execute. Bit 0 enables counter mode for start/end address field 0. Bit 1 enables counter mode for start/end address field 1. Bit 2 enables counter mode for start/end address field 2. Bit 3 enables counter mode for start/end address field 3. **Note**: Not recommended to be used with rand_addr_all_addr_mode_en. Will replace the last address with a zero address.

Bits	SCOM	Field Mnemonic: Description
10	RW	MCBAGRAQ_CFG_MAINT_ADDR_MODE_EN: Enabling this special maintenance address mode does the following: • Subtest complement bits become a 3-bit port-DIMM selector field. **Note**: When turning this off, make sure you clear or reprogram the complement bits. • The MCBIST address map is disabled. • Agen increments by bank group, bank, col, row, srank, mrank order. • Non-existing address bits are automatically worked around • Start/end addr fields are preassigned as follows: • (36 to 37) = bank_group(0 to 1) • (33 to 35) = bank(0 to 2) • (26 to 32) = col(3 to 9) • (8 to 25) = row(0 to 17) • (5 to 7) = srank(0 to 2) • (3 to 4) = mrank(0 to 1) • (0 to 2) = nothing/spare **Note:** If cfg_addr_counter_mode = 1, this mode will not work.
11	RW	MCBAGRAQ_CFG_MAINT_BROADCAST_MODE_EN: This mode only applies when maint_addr_mode = 1 (MCBIST broadcast is controlled solely by mcbcntl_port_sel). This mode enables maint_addr_mode to broadcast commands to multiple ports. When enabled: • Maint_addr_mode port-dimm select (MCBIST_cfg_test[00-31]_compl_1st/2nd/3rd_cmd) still dictates which DIMM it will use to determine the existent address space. • Mcbcntl_port_sel(0:3) dictates which ports will receive MCBIST requests. **Important:** maint_addr_mode port_dimm select should match one of the ports selected by mcbcntl_port_sel.
12	RW	MCBAGRAQ_CFG_MAINT_DETECT_SRANK_BOUNDARIES: If this bit is set, maintenance counts slave rank boundaries when configured to pause and reset at rank boundaries. Otherwise, only the master rank boundaries are considered. **Note:** As with all rank-boundary-related logic, this is only valid when in forward, sequential, and maintenance address mode.
13:31	RW	MCBAGRAQ_RESERVED_13_31: Not used.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Maint Current Address Trap Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBMCATQ
Address	00000000070123D7 (SCOM)
Description	Maintenance Current Address Trap Register

Bits	SCOM	Field Mnemonic: Description
0:37	RW	MCBMCATQ_CFG_CURRENT_ADDR_TRAP: If MCBCFGQ_cfg_current_addr_trap_update_dis = 0, this field stores the last address that was executed in the following format: (36 to 37) = bank_group(0 to 1) (33 to 35) = bank(0 to 2) (26 to 32) = col(3 to 9) (8 to 25) = row(0 to 17) (5 to 7) = srank(0 to 2) (3 to 4) = mrank(0 to 1) (0 to 2) = nothing/spare **Note**: The address is stored here just before execution of the command on address.

Bits	SCOM	Field Mnemonic: Description
38:39	RW	MCBMCATQ_CFG_CURRENT_PORT_TRAP: If MCBCFGQ_cfg_current_addr_trap_update_dis = 0, this field stores the port. This field is ONLY valid in maint_addr_mode. Otherwise, it is garbage.
40	RW	MCBMCATQ_CFG_CURRENT_DIMM_TRAP: If MCBCFGQ_cfg_current_addr_trap_update_dis = 0, this field stores the DIMM select.

Register Name	**MCBIST Control Register**
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCB_CNTLQ
Address	00000000070123DB (SCOM)
Description	MCBIST Control Register

Bits	SCOM	Field Mnemonic: Description
0	RWX	MCB_CNTLQ_MCB_START: Start bit. This is a self-resetting bit. It kicks off the MCBIST operation.
1	RWX	MCB_CNTLQ_MCB_STOP: Stop bit. This is a self-resetting bit. It stops after the command has completed on the current address. It can also stop from a pause.
2:5	RWX	MCB_CNTLQ_MCBCNTL_PORT_SEL: Select which ports to run MCBIST on. For example: 1000 runs on port 0 only. Multiple ports at the same time (broadcast mode) are supported for single write/read subtests only (or for a maintenance read). **Important**: Broadcast mode can only be run on ports that have the same memory configurations behind those ports (same number of rows, mranks, sranks, banks). If multiple ports are being run, broadcast_sync_en must be set to 1, and broadcast_sync_wait must be set to the proper amount of time required to sync all ports. At least one port must be selected or else MCBIST will probably hang. This dial is ignored when maint_addr_mode is enabled, which provides its own port select, unless maint_broadcast_mode_en is enabled.
6	RWX	MCB_CNTLQ_MCB_RESET_TRAP_CNFG: Clears values for the MCBIST compare mask and trap configuration registers MCBCMQ (in MBS_ECC64, on all four ports) and run-time counter RUNTIMECTRQ. This is a self-resetting bit.
7	RWX	MCB_CNTLQ_MCB_RESET_ERROR_LOGS: Clears values for MCBIST, maintenance error counters, and traps. This is a self-resetting bit.
8	RWX	MCB_CNTLQ_MCB_RESUME_FROM_PAUSE: When MCBIST is paused, this bit can be used to resume from where it stopped. This is a self-resetting bit.
9:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	**Configured Command Sequence Status Register**
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCB_CNTLSTATQ
Address	00000000070123DC (SCOM)
Description	Configured Command Sequence Status Register

Bits	SCOM	Field Mnemonic: Description
0	RWX	MCB_CNTLSTATQ_MCB_IP: IP bit. Hardware sets to a '1'b when an MCBIST run is in progress.
1	RWX	MCB_CNTLSTATQ_MCB_DONE: Done bit. Hardware sets to a '1'b when an MCBIST run is complete.
2	RWX	MCB_CNTLSTATQ_MCB_FAIL: Fail bit. Hardware sets to a '1'b when an MCBIST run failed.
3:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	RCD/LRDIMM Control Words 0 Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.RCD_LRDIM_CNTL_WORD0_15Q
Address	00000000070123DD (SCOM)
Description	15

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD0: RCDLRDIM control word. BA1(0), BA0(0), A(4), A(3).
4:7	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD1: RCDLRDIM control word. BA1(0), BA0(0), A(4), A(3).
8:11	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD2: RCDLRDIM control word. BA1(0), BA0(0), A(4), A(3).
12:15	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD3: RCDLRDIM control word. BA1(0), BA0(0), A(4), A(3).
16:19	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD4: RCDLRDIM control word. BA1(0), BA0(0), A(4), A(3).
20:23	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD5: RCDLRDIM control word. BA1(0), BA0(0), A(4), A(3).
24:27	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD6: RCDLRDIM control word. BA1(0), BA0(0), A(4), A(3).
28:31	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD7: RCDLRDIM control word. BA1(0), BA0(0), A(4), A(3).
32:35	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD8: RCDLRDIM control word. BA1(0), BA0(0), A(4), A(3).
36:39	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD9: RCDLRDIM control word. BA1(0), BA0(0), A(4), A(3).
40:43	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD10: RCDLRDIM control word. BA1(0), BA0(0), A(4), A(3).
44:47	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD11: RCDLRDIM control word. BA1(0), BA0(0), A(4), A(3).
48:51	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD12: RCDLRDIM control word. BA1(0), BA0(0), A(4), A(3).
52:55	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD13: RCDLRDIM control word. BA1(0), BA0(0), A(4), A(3).
56:59	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD14: RCDLRDIM control word. BA1(0), BA0(0), A(4), A(3).
60:63	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD15: RCDLRDIM control word. BA1(0), BA0(0), A(4), A(3).

Register Name	CCS Array Error Injection Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.CCSARRERRINJQ
Address	00000000070123DE (SCOM)
Description	CCS Array Error Injection Register

Bits	SCOM	Field Mnemonic: Description
0	RW	CCSARRERRINJQ_CCS_ARRAY_CE_ERR_INJ_MODE: CE inject mode into the CCS array.

Bits	SCOM	Field Mnemonic: Description
1	RW	CCSARRERRINJQ_CCS_ARRAY_CE_ERR_INJ: CE inject into the CCS array.
2	RW	CCSARRERRINJQ_CCS_ARRAY_UE_ERR_INJ_MODE: UE inject mode into the CCS array.
3	RW	CCSARRERRINJQ_CCS_ARRAY_UE_ERR_INJ: UE inject into the CCS array.
4	RW	CCSARRERRINJQ_RESERVED_4: Reserved.
5	RW	CCSARRERRINJQ_DISABLE_2N_MODE: Disable 2N mode.
6:14	RW	CCSARRERRINJQ_RESERVED_6_14: Reserved.
15	RW	CCSARRERRINJQ_READ_RESPONSE_DELAY_ENABLE: Enables waiting for valid read data to return.
16:31	RW	CCSARRERRINJQ_CCS_LOOP_COUNTER_COMPARE0: Programmable number of loop iterations 0. **Note**: If used and referenced, this value must be non-zero.
32:47	RW	CCSARRERRINJQ_CCS_LOOP_COUNTER_COMPARE1: Programmable number of loop iterations 1. **Note**: If used and referenced, this value must be non-zero.
48:63	RW	CCSARRERRINJQ_CCS_LOOP_COUNTER_COMPARE2: Programmable number of loop iterations 2. **Note**: If used and referenced, this value must be non-zero.

Register Name	**MCBIST Memory Register 7**
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBMR7Q
Address	00000000070123DF (SCOM)
Description	MCBIST Memory Register 7

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MCBIST_CFG_TEST28_OP_TYPE: Operation type. • If Subtest(0:3) = 0111 and 9:11(Data mode) = 000 (goto command), Subtest Addr 4:8 specifies which subtest address to change to (used for looping). • If Subtest(0:3) = 0111 and 9:11(Data mode) not = 000 (refresh only command), Subtest Addr 4:8 is a don't care.
4	RW	MCBIST_CFG_TEST28_COMPL_1ST_CMD: Complement the data for the first subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-DIMM sel field.
5	RW	MCBIST_CFG_TEST28_COMPL_2ND_CMD: Complement the data for the second subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-DIMM sel field.
6	RW	MCBIST_CFG_TEST28_COMPL_3RD_CMD: Complement the data for the third subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-DIMM sel field.
7	RW	MCBIST_CFG_TEST28_ADDR_REV_MODE: Generate addresses in reverse order.
8	RW	MCBIST_CFG_TEST28_ADDR_RAND_MODE: Generate addresses in random order.
9:11	RW	MCBIST_CFG_TEST28_DATA_MODE: Data mode.
12	RW	MCBIST_CFG_TEST28_ECC_MODE: Generate and check data with the ECC.
13	RW	MCBIST_CFG_TEST28_DONE: Done bit.
14:15	RW	MCBIST_CFG_TEST28_ADDR_SEL: Address select mode.
16:19	RW	MCBIST_CFG_TEST29_OP_TYPE: Operation type. • If Subtest(16:19) = 0111 and 25:27(Data mode) = 000 (goto command), Subtest Addr 20:24 specifies which subtest address to change to (used for looping). • If Subtest(16:19) = 0111 and 25:27(Data mode) not = 000 (refresh only command), Subtest Addr 20:24 is a don't care.

Bits	SCOM	Field Mnemonic: Description
20	RW	MCBIST_CFG_TEST29_COMPL_1ST_CMD: Complement the data for the first subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-DIMM sel field.
21	RW	MCBIST_CFG_TEST29_COMPL_2ND_CMD: Complement the data for the second subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port- DIMM sel field.
22	RW	MCBIST_CFG_TEST29_COMPL_3RD_CMD: Complement the data for the third subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port- DIMM sel field.
23	RW	MCBIST_CFG_TEST29_ADDR_REV_MODE: Generate addresses in reverse order.
24	RW	MCBIST_CFG_TEST29_ADDR_RAND_MODE: Generate addresses in random order.
25:27	RW	MCBIST_CFG_TEST29_DATA_MODE: Data mode.
28	RW	MCBIST_CFG_TEST29_ECC_MODE: Generate and check data with the ECC.
29	RW	MCBIST_CFG_TEST29_DONE: Done bit.
30:31	RW	MCBIST_CFG_TEST29_ADDR_SEL: Address select mode.
32:35	RW	MCBIST_CFG_TEST30_OP_TYPE: Operation type. • If Subtest(32:35) = 0111 and 41:43(Data mode) = 000 (goto command), Subtest Addr 36:40 specifies which subtest address to change to (used for looping). • If Subtest(32:35) = 0111 and 41:43(Data mode) not = 000 (refresh only command), Subtest Addr 36:40 is a don't care.
36	RW	MCBIST_CFG_TEST30_COMPL_1ST_CMD: Complement the data for the first subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port-dimm sel field.
37	RW	MCBIST_CFG_TEST30_COMPL_2ND_CMD: Bit 37 = Complement the data for the second subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port- DIMM sel field.
38	RW	MCBIST_CFG_TEST30_COMPL_3RD_CMD: Bit 38 = Complement the data for the third subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port- DIMM sel field.
39	RW	MCBIST_CFG_TEST30_ADDR_REV_MODE: Bit 39 = Generate addresses in reverse order.
40	RW	MCBIST_CFG_TEST30_ADDR_RAND_MODE: Bit 40 = Generate addresses in random order.
41:43	RW	MCBIST_CFG_TEST30_DATA_MODE: Bits(41:43) - Data mode.
44	RW	MCBIST_CFG_TEST30_ECC_MODE: Bit 44 = Generate and check data with the ECC.
45	RW	MCBIST_CFG_TEST30_DONE: Bit 45 - Done bit.
46:47	RW	MCBIST_CFG_TEST30_ADDR_SEL: Bits(46:47) - Address select mode.
48:51	RW	MCBIST_CFG_TEST31_OP_TYPE: Bits(48:51) - Operation type. • If Subtest(48:51) = 0111 and 57:59(Data mode) = 000 (goto command), Subtest Addr 52:56 specifies which subtest address to change to (used for looping). • If Subtest(48:51) = 0111 and 57:59(Data mode) not = 000 (refresh only command), Subtest Addr 52:56 is a don't care.
52	RW	MCBIST_CFG_TEST31_COMPL_1ST_CMD: Bit 52 - Complement the data for the first subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port- DIMM sel field.
53	RW	MCBIST_CFG_TEST31_COMPL_2ND_CMD: Bit 53 - Complement the data for the second subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port- DIMM sel field.
54	RW	MCBIST_CFG_TEST31_COMPL_3RD_CMD: Bit 54 - Complement the data for the third subcommand. **Note**: When cfg_maint_addr_mode_en = 1, the three complement bits become a port- DIMM sel field.
55	RW	MCBIST_CFG_TEST31_ADDR_REV_MODE: Bit 55 - Generate addresses in reverse order.
56	RW	MCBIST_CFG_TEST31_ADDR_RAND_MODE: Bit 56 - Generate addresses in random order.
57:59	RW	MCBIST_CFG_TEST31_DATA_MODE: Bits(57:59) - Data mode.

Bits	SCOM	Field Mnemonic: Description
60	RW	MCBIST_CFG_TEST31_ECC_MODE: Bit 60 - Generate and check data with the ECC.
61	RW	MCBIST_CFG_TEST31_DONE: Bit 61 - Done bit.
62:63	RW	MCBIST_CFG_TEST31_ADDR_SEL: Bits(62:63) - Address select mode.

Register Name	MCBIST Configuration Register
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MCBCFGQ
Address	00000000070123E0 (SCOM)
Description	MCBIST Configuration Register

Bits	SCOM	Field Mnemonic: Description
0	RW	MCBCFGQ_BROADCAST_SYNC_EN: Enables the state machine to send a sync pulse and wait a programmed time specified in broadcast_sync_wait. *Must be enabled for broadcast mode*.
1:7	RW	MCBCFGQ_BROADCAST_SYNC_WAIT: Number of 1024 2:1 cycle time bases to wait starting up MCBIST for SRQs to get synchronized for broadcast mode (ranges 0 - 127).
8:9	RW	MCBCFGQ_CFG_CMD_TIMEOUT_MODE: Configures at what length the MCBIST reports a timeout when requesting and waiting for an ACK on write commands, read commands, and CCS subtest. if = 11, wait 4,194,303 cycles until timeout is called. if = 10, wait 2,097,152 cycles until timeout is called. if = 01, wait 1,048,576 cycles until timeout is called. If = 00, wait 524,288 cycles until timeout is called.
10	RW	MCBCFGQ_RESET_KEEPER: Reset keeper. Writing this bit to 1 pulses the reset of the hold latched in the MBA c_err_rpt's.
11	RW	MCBCFGQ_CFG_CURRENT_ADDR_TRAP_UPDATE_DIS: Writing this bit to 1 causes the maintenance current address (MCBMCAT) trap to stop updating, holding whatever value it last logged.
12	RW	MCBCFGQ_CFG_CCS_RETRY_DIS: This bit disables the feature to retry an MCBIST-initiated CCS subtest once upon failure.
13:33	RW	MCBCFGQ_RESERVED_13_33: Not used.
34	RW	MCBIST_CFG_FORCE_PAUSE_AFTER_RANK: Force a pause at the end of a rank MCBIST operation. Requires sequential, forward addressing and maint_addr_mode. The bit must be cleared before resuming or it continues to induce pauses.
35	RW	MCBCFGQ_CFG_RESET_CNTS_START_OF_RANK: Reset counts at the start of each rank. Only valid when in forward sequential address mode.
36	RW	MCBCFGQ_CFG_LOG_COUNTS_IN_TRACE: Enables storing error counts registers into trace after each subtest.
37	RW	MCBCFGQ_SKIP_INVALID_ADDR_DIMM_DIS: Disables the feature to skip commands to invalid addresses and (for maintenance address mode) subtests to invalid DIMMs.
38	RW	MCBCFGQ_REFRESH_ONLY_SUBTEST_EN: Enables MCBIST refresh only subtest (DD2 enhancement).
39:40	RW	MCBCFGQ_REFRESH_ONLY_SUBTEST_TIMEBASE_SEL: Configuration bits select which timebase to use for the refresh only subtest enhancement.
41	RW	MCBCFGQ_RAND_ADDR_ALL_ADDR_MODE_EN: Cheat mode that allows you to set the start address to the end address and hit the entire nonfixed address range. Running with this mode prevents execution of just a single address. This mode works in random mode only. Logically, this mode disables last address detection on the very first address generated. It replaces the end address with a “zero address” where variable bits are cleared.

Bits	SCOM	Field Mnemonic: Description
42:55	RW	MCBIST_CFG_REF_WAIT_TIME: This is the refresh wait time in memory clock cycles. When doing the refresh only subtest, the MCBIST waits this amount of time before it goes on to the next subtest. This gets multiplied by MCBCFGQ_refresh_only_subtest_timebase_sel.
56	RW	MCBCFGQ_CFG_MCB_LEN64: When high, enables 64-byte operations. When low, MCBIST will issue 128-byte operations.
57:58	RW	MCBCFGQ_CFG_PAUSE_ON_ERROR_MODE: Configures at what boundary we pause when we take on a pausable error condition: 00 = Do not pause on error. 01 = Pause for an error after an operation to the address finishes. 10 = Pause for an error after operations to the current rank finish. **Note**: Ranks must be mapped to highest-order bits in the address generator (auto for maint_addr_mode). The address generator must be sequential forward. 11 = Pause for an error after the subtest finishes.
59	RW	MCBIST_CFG_PAUSE_AFTER_CCS_SUBTEST: Pause after the CCS subtest.
60	RW	MCBIST_CFG_FORCE_PAUSE_AFTER_ADDR: Force a pause after the current address of the MCBIST operation. This bit must be cleared before resuming or it will continue to induce pauses.
61	RW	MCBIST_CFG_FORCE_PAUSE_AFTER_SUBTEST: Force a pause after the current MCBIST subtest is finished. This bit must be cleared before resuming or it will continue to induce pauses.
62	RW	MCBCFGQ_CFG_ENABLE_SPEC_ATTN: Enables FIR action of special attention for a recoverable interrupt.
63	RW	MCBCFGQ_CFG_ENABLE_HOST_ATTN: Enables FIR action of host attention for a recoverable interrupt.

Register Name	**CCS Fixed Data Register 0**
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.CCS_FIXED_DATA0Q
Address	00000000070123E5 (SCOM)
Description	CCS Fixed Data Register 0

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CCS_FIXED_DATA0Q_FIXED_DATA_0_63: Fixed data from nontraditional transparent mode.

Register Name	**CCS Fixed Data Register 1**
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.CCS_FIXED_DATA1Q
Address	00000000070123E6 (SCOM)
Description	CCS Fixed Data Register 1

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_FIXED_DATA1Q_FIXED_DATA_64_79: Fixed data from nontraditional transparent mode.

Register Name	**MBA Error Report Register**
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.MBA_MCBERRPTQ
Address	00000000070123E7 (SCOM)
Description	MBA Error Report Register

Bits	SCOM	Field Mnemonic: Description
0	ROX	MBA_MCBERRPTQ_MCB_FIR_CCS_ERR_HOLD_OUT: CCS state machine error. Linked to MCBISTFIR(2).
1	ROX	MBA_MCBERRPTQ_MCB_FIR_MCBFSM_ERR_HOLD_OUT: MCBIST state machine error. Linked to MCBISTFIR(2).
2	ROX	MBA_MCBERRPTQ_MCB_CNTLQ_PE_HOLD_OUT: An mcb_cntlq SCOM parity error (fatal SCOM error). Linked to MCBISTFIR(14).
3	ROX	MBA_MCBERRPTQ_CCS_CNTLQ_PE_HOLD_OUT: A ccs_cntlq SCOM parity error (fatal SCOM error). Linked to MCBISTFIR(14).
4	ROX	MBA_MCBERRPTQ_MCBCNTL_PE_HOLD_OUT: An mcbcntl-related SCOM parity error (recoverable SCOM error). Linked to MCBISTFIR(13).
5	ROX	MBA_MCBERRPTQ_MCBAGEN_PE_HOLD_OUT: An mcbagen-related SCOM parity error (recoverable SCOM error). Linked to MCBISTFIR(13).
6	ROX	MBA_MCBERRPTQ_MAINT_CCS_PE_HOLD_OUT: A CCS-related SCOM parity error (recoverable SCOM error). Linked to MCBISTFIR(13).
7	ROX	MBA_MCBERRPTQ_MCBDGEN_PE_HOLD_OUT: An mcbdgen-related SCOM parity error (recoverable SCOM error). Linked to MCBISTFIR(13).
8	ROX	MBA_MCBERRPTQ_MCBERR_SCOM_PE_HOLD_OUT: An mcberr-related SCOM parity error (recoverable SCOM error). Linked to MCBISTFIR(13).
9	ROX	MBA_MCBERRPTQ_ECC_MCBIST_OUT_OF_SYNC_HOLD_OUT: ECC64 and MCBIST out-of-sync error. Linked to MCBISTFIR(3).
10	ROX	MBA_MCBERRPTQ_SRQ_MCBIST_OUT_OF_SYNC_HOLD_OUT: SRQ and MCBIST out-of-sync error. Linked to MCBISTFIR(3).
11	ROX	MBA_MCBERRPTQ_WRD_MCBIST_OUT_OF_SYNC_HOLD_OUT: WRD and MCBIST out-of-sync error. Linked to MCBISTFIR(3).
12	ROX	MBA_MCBERRPTQ_SRQ_CCS_UNEXPECTED_PORT_ACTIVE_HOLD_OUT: Non-selected port's SRQ responding to CCS. Linked to MCBISTFIR(3).
13	ROX	MBA_MCBERRPTQ_FATAL_CNFG_HOLD_OUT: Fatal SCOM configuration parity error (fatal SCOM error). Linked to MCBISTFIR(14).

Register Name	**MCBIST Debug Configuration Register 0 (Debug Muxing and WAT input)**
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.DBGCFG0Q
Address	00000000070123E8 (SCOM)
Description	MCBIST Debug Configuration Register 0 (Debug Muxing and WAT input)

Bits	SCOM	Field Mnemonic: Description
0	RW	DBGCFG0Q_CFG_DBG_ENABLE: Clock enable for debug logic.
1:11	RW	DBGCFG0Q_CFG_DBG_PICK_ASYNC_PORT01: Debug mux selects per byte between port 0 versus port 1 daisy chains of asynchronous logic.
12:22	RW	DBGCFG0Q_CFG_DBG_PICK_ASYNC_PORT23: Debug mux selects per byte between port 2 versus port 3 daisy chains of asynchronous logic.
23:33	RW	DBGCFG0Q_CFG_DBG_PICK_MCBIST01: Debug mux selects per byte between winner of port 0 and 1 versus MCBIST 01 debug.
34:44	RW	DBGCFG0Q_CFG_DBG_PICK_MCBIST23: Debug mux selects per byte between winner of port 2 and 3 versus MCBIST 23 debug.

Bits	SCOM	Field Mnemonic: Description
45	RW	DBGCFG0Q_SCOM_SET_WAT_EXT_TRIGGER: Forces a pulse on TRIGGER input of WAT when written from 0 to 1.
46	RW	DBGCFG0Q_SCOM_SET_WAT_EXT_RESET: Forces a pulse on RESET input of WAT when written from 0 to 1.
47	RW	DBGCFG0Q_SCOM_SET_WAT_EXT_ARM: Forces a pulse on ARM input of WAT when written from 0 to 1.

Register Name	**MCBIST Debug Configuration Register 1 (WAT input)**
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.DBGCFG1Q
Address	00000000070123E9 (SCOM)
Description	MCBIST Debug Configuration Register 1 (WAT input)

Bits	SCOM	Field Mnemonic: Description
0	RW	DBGCFG1Q_CFG_WAT_ENABLE: Clock enable for WAT logic.
1:2	RW	DBGCFG1Q_CFG_WAT_EXT_EVENT_TO_INT: Selects which external global WAT events feed into this WAT's input. Bit 0 enables PBI01. Bit 1 enables PBI23.
3:22	RW	DBGCFG1Q_CFG_WAT_EXT_TRIGGER_SEL: Selects the WAT TRIGGER input. Bits 0: 3 select wat_triga_q(0:3). Bits 4: 7 select wat_trigb_q(0:3). Bits 8:11 select wat_trigbc_q(3). Bits 12:15 select wat_pulse_q(0:3). Bits 16:19 select ext_wat_event(0:3).
23:42	RW	DBGCFG1Q_CFG_WAT_EXT_RESET_SEL: Selects the WAT RESET input. Bits 0: 3 select wat_triga_q(0:3). Bits 4: 7 select wat_trigb_q(0:3). Bits 8:11 select wat_trigbc_q(3). Bits 12:15 select wat_pulse_q(0:3). Bits 16:19 select ext_wat_event(0:3).
43:62	RW	DBGCFG1Q_CFG_WAT_EXT_ARM_SEL: Selects the WAT ARM input. Bits 0: 3 select wat_triga_q(0:3). Bits 4: 7 select wat_trigb_q(0:3). Bits 8:11 select wat_trigbc_q(3). Bits 12:15 select wat_pulse_q(0:3). Bits 16:19 select ext_wat_event(0:3).
63	RW	DBGCFG1Q_RESERVED_63: Reserved.

Register Name	**MCBIST Debug Configuration Register 2 (WAT Output)**
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.DBGCFG2Q
Address	00000000070123EA (SCOM)
Description	MCBIST Debug Configuration Register 2 (WAT output)

Bits	SCOM	Field Mnemonic: Description
0:19	RW	DBGCFG2Q_CFG_WAT_LOC_EVENT0_SEL: Selects among the output of four WATs to drive local event bit 0. Bits 0: 3 select wat_level_q(3). Bits 4: 7 select wat_pulse_q(3). Bits 8:11 select wat_triga_q(3). Bits 12:15 select wat_trigb_q(3). Bits 16:19 select wat_trigbc_q(3).
20:39	RW	DBGCFG2Q_CFG_WAT_LOC_EVENT1_SEL: Selects among the output of four WATs to drive local event bit 1. Bits 0: 3 select wat_level_q(3). Bits 4: 7 select wat_pulse_q(3). Bits 8:11 select wat_triga_q(3). Bits 12:15 select wat_trigb_q(3). Bits 16:19 select wat_trigbc_q(3).
40:59	RW	DBGCFG2Q_CFG_WAT_LOC_EVENT2_SEL: Selects among the output of four WATs to drive local event bit 2. Bits 0: 3 select wat_level_q(3). Bits 4: 7 select wat_pulse_q(3). Bits 8:11 select wat_triga_q(3). Bits 12:15 select wat_trigb_q(3). Bits 16:19 select wat_trigbc_q(3).
60:63	RW	DBGCFG2Q_RESERVED_60_63: Reserved.

Register Name	**MCBIST Debug Configuration Register 3 (WAT Output)**
Mnemonic	MC01.MCBIST.MBA_SCOMFIR.DBGCFG3Q
Address	00000000070123EB (SCOM)
Description	MCBIST Debug Configuration Register 3 (WAT output)

Bits	SCOM	Field Mnemonic: Description
0:19	RW	DBGCFG3Q_CFG_WAT_LOC_EVENT3_SEL: Selects among the output of four WATs to drive local event bit 3. Bits 0: 3 select wat_level_q(3). Bits 4: 7 select wat_pulse_q(3). Bits 8:11 select wat_triga_q(3). Bits 12:15 select wat_trigb_q(3). Bits 16:19 select wat_trigbc_q(3).
20:22	RW	DBGCFG3Q_CFG_WAT_GLOB_EVENT0_SEL: Selector for driving global event bit 0. Bit 0 enables local event (0). Bit 1 enables PBI01 global event (0). Bit 2 enables PBI01 global event (0).
23:25	RW	DBGCFG3Q_CFG_WAT_GLOB_EVENT1_SEL: Selector for driving global event bit 1. Bit 0 enables local event (1). Bit 1 enables PBI01 global event (1). Bit 2 enables PBI01 global event (1).
26:28	RW	DBGCFG3Q_CFG_WAT_GLOB_EVENT2_SEL: Selector for driving global event bit 2. Bit 0 enables local event (2). Bit 1 enables PBI01 global event (2). Bit 2 enables PBI01 global event (2).
29:31	RW	DBGCFG3Q_CFG_WAT_GLOB_EVENT3_SEL: Selector for driving global event bit 3. Bit 0 enables local event (3). Bit 1 enables PBI01 global event (3). Bit 2 enables PBI01 global event (3).

Bits	SCOM	Field Mnemonic: Description
32	RW	DBGCFG3Q_CFG_WAT_OUTPUT_PULSE: If enabled, converts a global event to a 1:1 pulse before sending out to PBIs.
33:36	RW	DBGCFG3Q_CFG_WAT_ACT_MNT_GO_IDLE_PULSE: Enables which events can trigger WAT action: maintenance goes idle.
37:40	RW	DBGCFG3Q_CFG_WAT_ACT_SET_SPATTN_PULSE: Enables which events can trigger WAT action: sets special attention.
41:44	RW	DBGCFG3Q_CFG_WAT_ACT_FRC_TB_PULSE_PULSE: Enables which events can trigger WAT action: forces a timebase pulse.
45:50	RW	DBGCFG3Q_CFG_WAT_CNT_VALUE: cfg_wat_cnt_value.
51:58	RW	DBGCFG3Q_CFG_WAT_TMR_VALUE: cfg_wat_tmr_value.

Register Name	**Clock Ratio Observation Register**
Mnemonic	MC01.CLKMON.MONM.CLKRATIO
Address	00000000070123F0 (SCOM)
Description	**Note**: Register only updates if enabled; see MCBPARMQ[59].

Bits	SCOM	Field Mnemonic: Description
0:11	ROX	CLKRATIO_RATIO: When the ratio monitor is enabled, the ratio will be 1920 × (mem freq)/(nest freq) nest mem nominal_ratio 2.0 GHz 1.867 GHz 1792 (0x700) 2.0 GHz 2.133 GHz 2048 (0x800) 2.0 GHz 2.400 GHz 2304 (0x900) 2.0 GHz 2.667 GHz 2560 (0xa00) 2.4 GHz 2.400 GHz 1920 (0x780) The actual readout may be a few counts above or below nominal.
12	ROX	CLKRATIO_CFG0_SYNC_MODE: Actual cfg0_sync_mode (for ports 0,1).
13	ROX	CLKRATIO_CFG1_SYNC_MODE: Actual cfg1_sync_mode (for ports 2,3).

Register Name	**Configuration of CC Counters Register**
Mnemonic	TP.TCMC01.MCSLOW.SYNC_CONFIG
Address	0000000007030000 (SCOM)
Description	Configuration of CC counters

Bits	SCOM	Field Mnemonic: Description
0:3	RW	SYNC_PULSE_DELAY: Delay incoming sync pulse. The default is 8 latches including asynchronous. Cycle delay of the reset of the phase counter: 0000 = 8 0001 = 2 0010 = 3 0011 = 4 0100 = 5 0101 = 6 0110 = 7 0111 = 8 1000 = 9 1001 = 10 1010 = 11 1011 = 12 1100 = 13 1101 = 14 1110 = 15 1111 = 16
4	RW	LISTEN_TO_SYNC_PULSE_DIS: Disable phase counter synchronization by the sync_pulse signal. (The default is enabled.) **Attention**: When you enable listen_to_sync, the chiplet gets corrupted for 200 cycles.
5	RW	SYNC_PULSE_INPUT_SEL: The default is 0. When set to 1, the alternative input of the sync_pulse is used. **Attention**: When you toggle the input select, the chiplet gets corrupted for 200 cycles.
6	RW	USE_SYNC_FOR_SCAN: If set, use OPCG initial alignment for scan requests.
7	RW	CLEAR_CHIPLET_IS_ALIGNED: This bit clears the chiplet_is_aligned bit. See the Chiplet Status Register on page 68.
8	RW	UNIT_REGION_CLKCMD_DISABLE: Disable the unit interface to start or stop one dedicated region. Used for the POWER9 cache or core.
9	RW	DISABLE_PCB_ITR: Disable interrupt generation within the CC. An interrupt is sent on each HLD event.
10	RW	ENABLE_VITL_ALIGN_CHECK: Enable the VITL align check to compare the alignment of an incoming sync pulse with 2:1 VITL LCB.
11	RW	SYNC_PULSE_OUT_DIS: Disable sync_pulse output. When set to 1, the master chiplet does not send sync pulses to slave chiplets anymore.
12:19	RW	UNUSED1219: Unused.

Register Name	OPCG Align Register
Mnemonic	TP.TCMC01.MCSLOW.OPCG_ALIGN
Address	0000000007030001 (SCOM)
Description	OPCG ALIGN

Bits	SCOM	Field Mnemonic: Description
0:3	RW	INOP_ALIGN: INOP phase alignment. (0: none, 1: 2:1, 2: 3:1, 3: 4:1, 4: 6:1, 5: 8:1, 6: 12:1, 7: 16:1, 8: 24:1, 9-15: 48:1)
4:7	RW	SNOP_ALIGN: SNOP phase alignment. (0: none, 1: 2:1, 2: 3:1, 3: 4:1, 4: 6:1, 5: 8:1, 6: 12:1, 7: 16:1, 8: 24:1, 9-15: 48:1)
8:11	RW	ENOP_ALIGN: ENOP phase alignment. (0: none, 1: 2:1, 2: 3:1, 3: 4:1, 4: 6:1, 5: 8:1, 6: 12:1, 7: 16:1, 8: 24:1, 9-15: 48:1)
12:19	RW	INOP_WAIT: INOP cycle delay (0 - 255).

Bits	SCOM	Field Mnemonic: Description
20:31	RW	SNOP_WAIT: SNOP cycle delay (0 - 4095).
32:39	RW	ENOP_WAIT: ENOP cycle delay (0 - 255).
40	RW	INOP_FORCE_SG: INOP: Set SG high during INOP.
41	RW	SNOP_FORCE_SG: SNOP: Set SG high during SNOP.
42	RW	ENOP_FORCE_SG: ENOP: Set SG high during ENOP (including LOOP phase).
43	RW	NO_WAIT_ON_CLK_CMD: 0: A clock change request first waits the OPCG_WAIT cycles. 1: A clock change request does not wait when not in flush.
44:45	RW	ALIGN_SOURCE_SELECT: 0: Use the inopa setting from opcg_reg0, 1: Use the rising edge of the sync pulse. 2: Use the unit0_sync_lvl to align (for AVP - refresh0). 3: Use the unit1_sync_lvl to align (for AVP - refresh1).
46	RW	UNUSED46: Unused.
47:51	RW	SCAN_RATIO: Scan ratio (n = 0-15: (n+1):1, 16: 24:1, 17: 32:1, 18: 48:1, 19: 64:1, 20: 128:1). The default is 4:1 = 00011.
52:63	RW	OPCG_WAIT_CYCLES: Old PAD value. Delay at the beginning and end of the OPCG run, to allow DC signals to be there at the right time (0 = 4095). **Note:** Needs to be higher than the pipeline-latch depth. The default is 0x020.

Register Name	OPCG Control Register 0
Mnemonic	TP.TCMC01.MCSLOW.OPCG_REG0
Address	0000000007030002 (SCOM)
Description	OPCG Control Register 0

Bits	SCOM	Field Mnemonic: Description
0	RW	RUNN_MODE: 0 = BIST mode used for LBIST. 1 = RUNN mode used for ABIST/IOBIST.
1	RWX	OPCG_GO: OPCG go (start OPCG). This bit is cleared when the OPCG is done. Poll for opcg_done in the cplt_start register.
2	RWX	RUN_SCAN0: Run scan0 (overrides all BIST mode settings but the scan_ratio). Starts a scan0 run. The bit gets cleared when OPCG is done. Poll for opcg_done in the cplt_start register.
3	RW	SCAN0_MODE: Set PRPGs in scan0_mode, but do not run the automatic scan0 sequence.
4	RWX	OPCG_IN_SLAVE_MODE: When selected, OPCG waits for the master chiplet to get started. When Keep_MS_Mode is 0, SLAVE_MODE is cleared after the incoming trigger.
5	RWX	OPCG_IN_MASTER_MODE: When selected, OPCG sends out a trigger to all slave chiplets. When Keep_MS_MODE = 0, MASTER_MODE gets cleared after sending out one master trigger.
6	RW	KEEP_MS_MODE: When set to 1, OPCG in M/S mode bits is not cleared after one incoming OPCG trigger. The default is clear the M/S mode bits.
7	RW	TRIGGER_OPCG_ON_UNIT0_SYNC_LVL: The unit pin used for the AVP can trigger OPCG (unit0_sync_lvl).
8	RW	TRIGGER_OPCG_ON_UNIT1_SYNC_LVL: The unit pin used for the AVP can trigger OPCG (unit1_sync_lvl).
9	RWX	RUN_CHIPLET_SCAN0: Run scan0 on all regions and types. This will clear the chiplet .

Bits	SCOM	Field Mnemonic: Description
10	RWX	RUN_CHIPLET_SCAN0_NO_PLL: Run scan0 on all regions and types. will clear the chiplet at all exclude PLL region PLL can keep running.
11	RW	RUN_OPCG_ON_UPDATE_DR: Start the OPCG engine when the scan updated (update_dr) is received (set pulse). Cronus requires this bit = 1 for a setpulse WRITE.
12	RW	RUN_OPCG_ON_CAPTURE_DR: Start the OPCG engine when the scan updated (capture_dr) is received (set pulse). Cronus requires this bit = 1 for a setpulse READ.
13	RW	STOP_RUNN_ON_XSTOP: Run-N-mode: Stop run-n on a checkstop.
14	RW	OPCG_STARTS_BIST: Run-N-mode: The OPCG engine controls start_bist for ABIST or IOBIST (see the BIST register).
15:20	RW	UNUSED1520: Unused.
21:63	RWX	LOOP_COUNT: Loop counter for LBIST and RUNN. Write: target value. Read: current counter value. Counts from 0 to the target value.

Register Name	OPCG Control Register 1
Mnemonic	TP.TCMC01.MCSLOW.OPCG_REG1
Address	0000000007030003 (SCOM)
Description	OPCG Control Register 1

Bits	SCOM	Field Mnemonic: Description
0:11	RW	SCAN_COUNT: BIST mode: Channel scan count (s = 0 - 4095). Run-N-mode: The start_bist match value (0:11).
12:23	RW	MISR_A_VAL: BIST mode: The a value for the MISR aperture. Run-N-mode: The start_bist match value (12:23).
24:35	RW	MISR_B_VAL: BIST mode: The b value for the MISR aperture. Run-N-mode: The start_bist match value (24:35).
36:47	RW	MISR_INIT_WAIT: BIST mode: Delay MISR aperture. MISRs get active after this number of loops.
48	RW	OPCG_SUPPRESS_EVEN_CLK: OPCG will only create even and not odd clocks. Used for run-N to create only one clock in the fast domain. The default is 0.
49	RW	SCAN_CLK_USE_EVEN: Generate a scan clock in the even cycle instead of the odd. The default is 0, which is use odd for the scan.
50:51	RW	UNUSED2: Unused.
52	RW	RTIM_THOLD_FORCE: Force rtim_thold low when not in test_dc mode (must be 0 at all times).
53	RW	DISABLE_ARY_CLK_DURING_FILL: LBIST and SCAN0: Prevent the fire of ARY HLD during an NSL fill.
54	RW	SG_HIGH_DURING_FILL: LBIST and SCAN0: Hold SG high during an NSL fill.
55:56	RW	LBIST_SKITTER_CTL: BIST mode: 00 = Enable skitter during lbist_ip. 01 = Enable skitter when misr_active. See MISR_INIT_WAIT. 10 = Skitter OPCG_GO mode. The falling edge equals start; the rising edge equals stop. 11 = Unused.

Bits	SCOM	Field Mnemonic: Description
57	RW	MISR_MODE: BIST mode: MISR aperture mode. 0 = a-1 to b-1. 1 = Start to a and b to end.
58	RW	INFINITE_MODE: Infinite mode. RUNN and LBIST run forever and ignore the loop count.
59:63	RW	NSL_FILL_COUNT: BIST mode: NSL-fill count (0 - 31).

Register Name	OPCG Control Register 2
Mnemonic	TP.TCMC01.MCSLOW.OPCG_REG2
Address	0000000007030004 (SCOM)
Description	OPCG Control Register 2

Bits	SCOM	Field Mnemonic: Description
0	RWX	OPCG_GO2: OPCG go for broadcast sequences (start sequence).
1:3	RW	PRPG_WEIGHTING: prpg_activate: 1/2, 1/4, 1/8, 1/16, 1/2, 3/4, 7/8, 15/16.
4:15	RWX	PRPG_VALUE: Set to 0 for PRPG always on; else seed.
16:27	RW	PRPG_A_VAL: The a value for the PRPG aperture.
28:39	RW	PRPG_B_VAL: The b value for the PRPG aperture.
40	RW	PRPG_MODE: The PRPG aperture mode: 0 = a-1 to b-1 1 = Start to a and b to end
41:63	RW	UNUSED41_63: Unused.

Register Name	Scan Region and Type Register
Mnemonic	TP.TCMC01.MCSLOW.SCAN_REGION_TYPE
Address	0000000007030005 (SCOM)
Description	Scan Region and Type

Bits	SCOM	Field Mnemonic: Description
0	RWX	SYSTEM_FAST_INIT: The default is 0. When it is set to 1, the MASK bits in the CMSK chain decide which part will be scanned or scan0. MASK = 1 = scan0, MASK = 0 = part or scan chain.
1:2	RO	Constant = 0b00
3	NCX	SCAN_REGION_VITL: Scan clock region VITL (Vital = Clock).
4	RWX	SCAN_REGION_PERV: Scan clock region pervasive (Pervasive).
5	RWX	SCAN_REGION_UNIT1: Scan clock region mc01 - MCU.
6	RWX	SCAN_REGION_UNIT2: Scan clock region iom01 - d3, iod.
7	RWX	SCAN_REGION_UNIT3: Scan clock region iom23 - d3, iod.
8	RWX	SCAN_REGION_UNIT4: Scan clock region unused.
9	RWX	SCAN_REGION_UNIT5: Scan clock region unused.
10	RWX	SCAN_REGION_UNIT6: Scan clock region unused.
11	RWX	SCAN_REGION_UNIT7: Scan clock region unused.

Bits	SCOM	Field Mnemonic: Description
12	RWX	SCAN_REGION_UNIT8: Scan clock region unused.
13	RWX	SCAN_REGION_UNIT9: Scan clock region unused.
14	RWX	SCAN_REGION_UNIT10: Scan clock region pllmem - clk.
15:47	RO	Constant = 0b00000000000000000000000000000000
48	RW	SCAN_TYPE_FUNC: Scan chain func (functional).
49	RW	SCAN_TYPE_CFG: Scan chain mode (boot configuration and debug configuration).
50	RW	SCAN_TYPE_CCFG_GPTR: Scan chain CCFG / GPTR (Pervasive: CC configuration, Others: GPTR).
51	RW	SCAN_TYPE_REGF: Scan chain regf (register files).
52	RW	SCAN_TYPE_LBIST: Scan chain lbst (LBIST).
53	RW	SCAN_TYPE_ABIST: Scan chain abst (ABIST).
54	RW	SCAN_TYPE_REPR: Scan chain repr (Array Repair).
55	RW	SCAN_TYPE_TIME: Scan chain time (Array Timing).
56	RW	SCAN_TYPE_BNDY: Scan chain bndy (Boundary IO's).
57	RW	SCAN_TYPE_FARR: Scan chain farr (fast array unload).
58	RW	SCAN_TYPE_CMSK: Scan chain CMSK (LBIST channel mask).
59	RW	SCAN_TYPE_INEX: Scan chain idex (c14 ASIC).
60:63	RO	Constant = 0b0000

Register Name	**Start/Stop Clocks Register**
Mnemonic	TP.TCMC01.MCSLOW.CLK_REGION
Address	0000000007030006 (SCOM)
Description	Start/stop of clocks

Bits	SCOM	Field Mnemonic: Description
0:1	RWX	CLOCK_CMD: Command for clock control: 00 = NOP 01 = Start 10 = Stop 11 = Pulse (one pulse)
2	RWX	SLAVE_MODE: When selected, the clock command waits for the master chiplet to get started. The bit gets cleared after an incoming slave trigger, and Keep_MS_Mode_after_trigger is set to 0.
3	RWX	MASTER_MODE: When selected, the clock command sends out a trigger to all the slave chiplets. The bit gets cleared after sending out one master trigger, and Keep_MS_Mode_after_trigger is set to 0.
4	RWX	CLOCK_REGION_PERV: For clock region pervasive (Pervasive).
5	RWX	CLOCK_REGION_UNIT1: For clock region mc01 - mcu.
6	RWX	CLOCK_REGION_UNIT2: For clock region iom01 - d3, iod.
7	RWX	CLOCK_REGION_UNIT3: For clock region iom23 - d3, iod.
8	RWX	CLOCK_REGION_UNIT4: For clock region unused.
9	RWX	CLOCK_REGION_UNIT5: For clock region unused.
10	RWX	CLOCK_REGION_UNIT6: For clock region unused.
11	RWX	CLOCK_REGION_UNIT7: For clock region unused.

Bits	SCOM	Field Mnemonic: Description
12	RWX	CLOCK_REGION_UNIT8: For clock region unused.
13	RWX	CLOCK_REGION_UNIT9: For clock region unused.
14	RWX	CLOCK_REGION_UNIT10: For clock region pllmem - clk.
15:47	RO	Constant = 0b00000000000000000000000000000000
48	RWX	SEL_THOLD_SL: Select sl tholds.
49	RWX	SEL_THOLD_NSL: Select nsl tholds.
50	RWX	SEL_THOLD_ARY: Select array thold.
51	RO	Constant = 0b0
52	RW	CLOCK_PULSE_USE_EVEN: For dual mesh support. The default for pulse is an *odd* phase. When this bit is set, the pulse is applied on an *even* phase.
53:63	RO	Constant = 0b00000000000

Register Name	Clocks Running SL Register
Mnemonic	TP.TCMC01.MCSLOW.CLOCK_STAT_SL
Address	0000000007030008 (SCOM)
Description	Clocks running sl

Bits	SCOM	Field Mnemonic: Description
0:3	RO	Constant = 0b1111
4	ROX	CLOCK_STATUS_PERV_SL: Status of pervasive sl hld. 0 = Run 1 = Stop
5	ROX	CLOCK_STATUS_UNIT1_SL: Status of mc01 - mcu sl hld. 0 = Run 1 = Stop
6	ROX	CLOCK_STATUS_UNIT2_SL: Status of iom01 - d3, iod sl hld. 0 = Run 1 = Stop
7	ROX	CLOCK_STATUS_UNIT3_SL: Status of iom23 - d3, iod sl hld. 0 = Run 1 = Stop
8	ROX	CLOCK_STATUS_UNIT4_SL: Status of unused sl hld. 0 = Run 1 = Stop
9	ROX	CLOCK_STATUS_UNIT5_SL: Status of unused sl hld. 0 = Run 1 = Stop
10	ROX	CLOCK_STATUS_UNIT6_SL: Status of unused sl hld. 0 = Run 1 = Stop
11	ROX	CLOCK_STATUS_UNIT7_SL: Status of unused sl hld. 0 = Run 1 = Stop

Bits	SCOM	Field Mnemonic: Description
12	ROX	CLOCK_STATUS_UNIT8_SL: Status of unused sl hld. 0 = Run 1 = Stop
13	ROX	CLOCK_STATUS_UNIT9_SL: Status of unused sl hld. 0 = Run 1 = Stop
14	ROX	CLOCK_STATUS_UNIT10_SL: Status of pllmem - clk sl hld. 0 = Run 1 = Stop
15:63	RO	Constant = 0b11111111111111111111111111111111111111111111111111111111

Register Name	Clocks Running NSL Register
Mnemonic	TP.TCMC01.MCSLOW.CLOCK_STAT_NSL
Address	0000000007030009 (SCOM)
Description	Clocks running nsl

Bits	SCOM	Field Mnemonic: Description
0:3	RO	Constant = 0b1111
4	ROX	CLOCK_STATUS_PERV_NSL: Status of pervasive nsl hld. 0 = Run 1 = Stop
5	ROX	CLOCK_STATUS_UNIT1_NSL: Status of mc01 - mcu nsl hld. 0 = Run 1 = Stop
6	ROX	CLOCK_STATUS_UNIT2_NSL: Status of iom01 - d3, iod nsl hld. 0 = Run 1 = Stop
7	ROX	CLOCK_STATUS_UNIT3_NSL: Status of iom23 - d3, iod nsl hld. 0 = Run 1 = Stop
8	ROX	CLOCK_STATUS_UNIT4_NSL: Status of unused nsl hld. 0 = Run 1 = Stop
9	ROX	CLOCK_STATUS_UNIT5_NSL: Status of unused nsl hld. 0 = Run 1 = Stop
10	ROX	CLOCK_STATUS_UNIT6_NSL: Status of unused nsl hld. 0 = Run 1 = Stop
11	ROX	CLOCK_STATUS_UNIT7_NSL: Status of unused nsl hld. 0 = Run 1 = Stop
12	ROX	CLOCK_STATUS_UNIT8_NSL: Status of unused nsl hld. 0 = Run 1 = Stop
13	ROX	CLOCK_STATUS_UNIT9_NSL: Status of unused nsl hld. 0 = Run 1 = Stop

Bits	SCOM	Field Mnemonic: Description
14	ROX	CLOCK_STATUS_UNIT10_NSL: Status of pllmem - clk nsl hld. 0 = Run 1 = Stop
15:63	RO	Constant = 0b111111111111111111111111111111111111111111111111111111111

Register Name	Clocks Running ARY Register
Mnemonic	TP.TCMC01.MCSLOW.CLOCK_STAT_ARY
Address	000000000703000A (SCOM)
Description	Clocks running ary

Bits	SCOM	Field Mnemonic: Description
0:3	RO	Constant = 0b1111
4	ROX	CLOCK_STATUS_PERV_ARY: Status of pervasive ary hld. 0 = Run 1 = Stop
5	ROX	CLOCK_STATUS_UNIT1_ARY: Status of mc01 - mcu ary hld. 0 = Run 1 = Stop
6	ROX	CLOCK_STATUS_UNIT2_ARY: Status of iom01 - d3, iod ary hld. 0 = Run 1 = Stop
7	ROX	CLOCK_STATUS_UNIT3_ARY: Status of iom23 - d3, iod ary hld. 0 = Run 1 = Stop
8	ROX	CLOCK_STATUS_UNIT4_ARY: Status of unused ary hld. 0 = Run 1 = Stop
9	ROX	CLOCK_STATUS_UNIT5_ARY: Status of unused ary hld. 0 = Run 1 = Stop
10	ROX	CLOCK_STATUS_UNIT6_ARY: Status of unused ary hld. 0 = Run 1 = Stop
11	ROX	CLOCK_STATUS_UNIT7_ARY: Status of unused ary hld. 0 = Run 1 = Stop
12	ROX	CLOCK_STATUS_UNIT8_ARY: Status of unused ary hld. 0 = Run 1 = Stop
13	ROX	CLOCK_STATUS_UNIT9_ARY: Status of unused ary hld. 0 = Run 1 = Stop
14	ROX	CLOCK_STATUS_UNIT10_ARY: Status of pllmem - clk ary hld. 0 = Run 1 = Stop
15:63	RO	Constant = 0b111111111111111111111111111111111111111111111111111111111

Register Name	ABIST and IOBIST per Region Register
Mnemonic	TP.TCMC01.MCSLOW.BIST
Address	000000000703000B (SCOM)
Description	ABIST and IOBIST per region

Bits	SCOM	Field Mnemonic: Description
0	RW	TC_BIST_START_TEST_DC: Keep this bit 0 during ABIST/IOBIST. It can be used to bypass the RUNN start. When this bit is set, the BIST_START_TEST goes high immediately without waiting for RUNN. BIST starts with the first hld clock cycle.
1	RW	TC_SRAM_ABIST_MODE_DC: Select the ABIST engines for SRAMs.
2	RW	TC_EDRAM_ABIST_MODE_DC: Select the ABIST engines for eDRAMs.
3	RW	TC_IOBIST_MODE_DC: Select the IOBIST engines.
4	RW	BIST_PERV: Region pervasive: 1 = BIST_START_TEST for this region is triggered. 0 = Region does not take part in the ABIST/IOBIST run.
5	RW	BIST_UNIT1: Region mc01 - mcu: 1 = BIST_START_TEST for this region is triggered, 0 = Region does not take part in the ABIST/IOBIST run.
6	RW	BIST_UNIT2: Region iom01 - d3, iod: 1 = BIST_START_TEST for this region is triggered. 0 = Region does not take part in the ABIST/IOBIST run.
7	RW	BIST_UNIT3: Region iom23 - d3, iod: 1 = BIST_START_TEST for this region is triggered. 0 = Region does not take part in the ABIST/IOBIST run.
8	RW	BIST_UNIT4: Region unused: 1 = BIST_START_TEST for this region is triggered. 0 = Region does not take part in the ABIST/IOBIST run.
9	RW	BIST_UNIT5: Region unused: 1 = BIST_START_TEST for this region is triggered. 0 = Region does not take part in the ABIST/IOBIST run.
10	RW	BIST_UNIT6: Region unused: 1 = BIST_START_TEST for this region is triggered. 0 = Region does not take part in the ABIST/IOBIST run.
11	RW	BIST_UNIT7: Region unused: 1 = BIST_START_TEST for this region is triggered. 0 = Region does not take part in the ABIST/IOBIST run.
12	RW	BIST_UNIT8: Region unused: 1 = BIST_START_TEST for this region is triggered. 0 = Region does not take part in the ABIST/IOBIST run.
13	RW	BIST_UNIT9: Region unused: 1 = BIST_START_TEST for this region is triggered. 0 = Region does not take part in the ABIST/IOBIST run.
14	RW	BIST_UNIT10: Region pllmem - clk: 1 = BIST_START_TEST for this region is triggered. 0 = Region does not take part in the ABIST/IOBIST run.
15:47	RO	Constant = 0b00000000000000000000000000000000
48	RW	BIST_STROBE_WINDOW_EN: Enable strobe window only in TE = 1 mode. The OPCGGO tester pin is enabling ABIST compare, after ABIST has been started. A special setup in the ABIST engine is required. The default is 0. System mode can not enable this feature.

Bits	SCOM	Field Mnemonic: Description
49:63	RO	Constant = 0b000000000000000

Register Name	Checkstop per Region Register
Mnemonic	TP.TCMC01.MCSLOW.XSTOP1
Address	000000000703000C (SCOM)
Description	Checkstop per region

Bits	SCOM	Field Mnemonic: Description
0	RW	XSTOP1_MASK_B: Mask for a checkstop to a clockstop of select regions (see xstop_perv, xstop_unit0..n). 0 = Ignore checkstop. 1= Stop on checkstop.
1	RW	XSTOP1_UNUSED: Unused.
2	RW	TRIGGER_OPCG_ON_XSTOP1: Trigger an OPCG on a checkstop instead of performing a clockstop.
3	RW	XSTOP1_WAIT_ALLWAYS: When set to 1, a checkstop waits independent from the flush. The default is no wait, when the flush is not set.
4	RW	XSTOP1_PERV: Region pervasive: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
5	RW	XSTOP1_UNIT1: Region mc01 - mcu: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
6	RW	XSTOP1_UNIT2: Region iom01 - d3, iod: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
7	RW	XSTOP1_UNIT3: Region iom23 - d3, iod: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
8	RW	XSTOP1_UNIT4: Region unused: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
9	RW	XSTOP1_UNIT5: Region unused: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
10	RW	XSTOP1_UNIT6: Region unused: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
11	RW	XSTOP1_UNIT7: Region unused: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
12	RW	XSTOP1_UNIT8: Region unused: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
13	RW	XSTOP1_UNIT9: Region unused: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
14	RW	XSTOP1_UNIT10: Region pllmem - clk: 1 = Region is stopped. 0 = Region keeps running on a checkstop.

Bits	SCOM	Field Mnemonic: Description
15:47	RO	Constant = 0b00000000000000000000000000000000
48:59	RW	XSTOP1_WAIT_CYCLES: Defines how many cycles a checkstop waits after dropping a flush, before tholds get dropped. 0 - 4095 cycles are possible.
60:63	RO	Constant = 0b0000

Register Name	Checkstop per Region Register
Mnemonic	TP.TCMC01.MCSLOW.XSTOP2
Address	000000000703000D (SCOM)
Description	Checkstop per region

Bits	SCOM	Field Mnemonic: Description
0	RW	XSTOP2_MASK_B: Mask for a checkstop to a clockstop of select regions (see xstop_perv, xstop_unit0..n): 0 = Ignore checkstop. 1= Stop on checkstop.
1	RW	XSTOP2_UNUSED: Unused.
2	RW	TRIGGER_OPCG_ON_XSTOP2: Trigger an OPCG on a checkstop instead of performing a clockstop.
3	RW	XSTOP2_WAIT_ALLWAYS: When set to 1, a checkstop waits independent from a flush. The default is no wait, when the flush in not set.
4	RW	XSTOP2_PERV: Region pervasive: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
5	RW	XSTOP2_UNIT1: Region mc01 - mcu: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
6	RW	XSTOP2_UNIT2: Region iom01 - d3, iod: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
7	RW	XSTOP2_UNIT3: Region iom23 - d3, iod: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
8	RW	XSTOP2_UNIT4: Region unused: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
9	RW	XSTOP2_UNIT5: Region unused: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
10	RW	XSTOP2_UNIT6: Region unused: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
11	RW	XSTOP2_UNIT7: Region unused: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
12	RW	XSTOP2_UNIT8: Region unused: 1 = Region is stopped. 0 = Region keeps running on a checkstop.

Bits	SCOM	Field Mnemonic: Description
13	RW	XSTOP2_UNIT9: Region unused: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
14	RW	XSTOP2_UNIT10: Region pllmem - clk: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
15:47	RO	Constant = 0b00000000000000000000000000000000
48:59	RW	XSTOP2_WAIT_CYCLES: Defines how many cycles a checkstop waits after dropping a flush, before tholds get dropped. 0 - 4095 cycles are possible.
60:63	RO	Constant = 0b0000

Register Name	Checkstop per Region Register
Mnemonic	TP.TCMC01.MCSLOW.XSTOP3
Address	000000000703000E (SCOM)
Description	Checkstop per region

Bits	SCOM	Field Mnemonic: Description
0	RW	XSTOP3_MASK_B: Mask for a checkstop to a clockstop of select regions (see xstop_perv, xstop_unit0..n): 0 = Ignore checkstop. 1 = Stop on checkstop.
1	RW	XSTOP3_UNUSED: Unused.
2	RW	TRIGGER_OPCG_ON_XSTOP3: Trigger an OPCG on a checkstop instead of performing a clockstop.
3	RW	XSTOP3_WAIT_ALLWAYS: When set to 1, a checkstop waits independent from a flush. The default is no wait, when flush in not set.
4	RW	XSTOP3_PERV: Region pervasive: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
5	RW	XSTOP3_UNIT1: Region mc01 - mcu: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
6	RW	XSTOP3_UNIT2: Region iom01 - d3, iod: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
7	RW	XSTOP3_UNIT3: Region iom23 - d3, iod: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
8	RW	XSTOP3_UNIT4: Region unused: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
9	RW	XSTOP3_UNIT5: Region unused: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
10	RW	XSTOP3_UNIT6: Region unused: 1 = Region is stopped. 0 = Region keeps running on a checkstop.

Bits	SCOM	Field Mnemonic: Description
11	RW	XSTOP3_UNIT7: Region unused: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
12	RW	XSTOP3_UNIT8: Region unused: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
13	RW	XSTOP3_UNIT9: Region unused: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
14	RW	XSTOP3_UNIT10: Region pllmem - clk: 1 = Region is stopped. 0 = Region keeps running on a checkstop.
15:47	RO	Constant = 0b00000000000000000000000000000000
48:59	RW	XSTOP3_WAIT_CYCLES: Defines how many cycle a checkstop will wait after dropping a flush before tholds get dropped. 0 - 4095 cycles are possible.
60:63	RO	Constant = 0b0000

Register Name	Error Status of CC Register
Mnemonic	TP.TCMC01.MCSLOW.ERROR_STATUS
Address	000000000703000F (SCOM)
Description	Error Status of CC

Bits	SCOM	Field Mnemonic: Description
0	RWX	PCB_WRITE_NOT_ALLOWED_ERR: Write on read-only register.
1	RWX	PCB_READ_NOT_ALLOWED_ERR: Read not allowed, may be a write-only register.
2	RWX	PCB_PARITY_ON_CMD_ERR: Parity error on cmd.
3	RWX	PCB_ADDRESS_NOT_VALID_ERR: Invalid address.
4	RWX	PCB_PARITY_ON_ADDR_ERR: Parity error on address.
5	RWX	PCB_PARITY_ON_DATA_ERR: Parity error on data.
6	RWX	PCB_PROTECTED_ACCESS_INVALID_ERR: Protection violation.
7	RWX	PCB_PARITY_ON_SPCIF_ERR: Parity error on spcif.
8	RWX	PCB_WRITE_AND_OPCG_IP_ERR: PCB write while the OPCG is running.
9	RWX	SCAN_READ_AND_OPCG_IP_ERR: Scan read when the OPCG is running.
10	RWX	CLOCK_CMD_CONFLICT_ERR: Clock cmd in progress.
11	RWX	SCAN_COLLISION_ERR: Scan region selected of running region.
12	RWX	PREVENTED_SCAN_COLLISION_ERR: PCB request to set scan region that is running.
13	RWX	OPCG_TRIGGER_ERR: OPCG gets triggered while the OPCG is running.
14	RWX	PHASE_CNT_CORRUPTION_ERR: Phase counters inside the chiplet are out of sync.
15	RWX	CLOCK_CMD_PREVENTED_ERR: Security or scan collision prevented a clock start.
16	RWX	PARITY_ON_OPCG_SM_ERR: Parity error on an OPCG state machine.
17	RWX	PARITY_ON_CLOCK_MUX_REG_ERR: Parity error on scan/clock region/type or clock status register.
18	RWX	PARITY_ON_OPCG_REG_ERR: Parity error on OPCG registers.

Bits	SCOM	Field Mnemonic: Description
19	RWX	PARITY_ON_SYNC_CONFIG_REG_ERR: Parity error on sync configuration register.
20	RWX	PARITY_ON_XSTOP_REG_ERR: Parity error on a checkstop register.
21	RWX	PARITY_ON_GPIO_REG_ERR: Parity error on GP0, 4, 5, 6 registers.
22	RWX	CLKCMD_REQUEST_ERR: Region clkcmd has one request pending but gets a second one.
23	RWX	CBS_PROTOCOL_ERR: CBS protocol error. The REQ/ACK sequence is wrong.
24	RWX	VITL_ALIGN_ERR: VITL alignment is out of sync to sync pulse.
25	RWX	UNIT_SYNC_LVL_ERR: Unit0 and Unit1 sync lvl pulses are not in sync. The AVP is broken.
26	RWX	PARITY_ON_SELFBOOT_CMD_STATE_ERR: Parity error on selfboot cmd state.
27	RWX	UNUSED_ERROR27: Unused.
28	RWX	UNUSED_ERROR28: Unused.
29	RWX	UNUSED_ERROR29: Unused.
30	RWX	UNUSED_ERROR30: Unused.
31	RWX	UNUSED_ERROR31: Unused.

Register Name	**OPCG Control Register Capture1**
Mnemonic	TP.TCMC01.MCSLOW.OPCG_CAPT1
Address	0000000007030010 (SCOM)
Description	OPCG Control Register Capture1

Bits	SCOM	Field Mnemonic: Description
0:3	RW	Count: 0000 = 12 cycles 0001 - 1100 = cycles 1 - 12 1101 - 1111 = 24 normal, no fast
4:8	RW	SEQ_01: Sequence cycle 1 for normal/slow region (sl, nsl, ary, se, fce).
9:13	RW	SEQ_02: Sequence cycle 2 for normal/slow region (sl, nsl, ary, se, fce).
14:18	RW	SEQ_03: Sequence cycle 3 for normal/slow region (sl, nsl, ary, se, fce).
19:23	RW	SEQ_04: Sequence cycle 4 for normal/slow region (sl, nsl, ary, se, fce).
24:28	RW	SEQ_05: Sequence cycle 5 for normal/slow region (sl, nsl, ary, se, fce).
29:33	RW	SEQ_06: Sequence cycle 6 for normal/slow region (sl, nsl, ary, se, fce).
34:38	RW	SEQ_07: Sequence cycle 7 for normal/slow region (sl, nsl, ary, se, fce).
39:43	RW	SEQ_08: Sequence cycle 8 for normal/slow region (sl, nsl, ary, se, fce).
44:48	RW	SEQ_09: Sequence cycle 9 for normal/slow region (sl, nsl, ary, se, fce).
49:53	RW	SEQ_10: Sequence cycle 10 for normal/slow region (sl, nsl, ary, se, fce).
54:58	RW	SEQ_11: Sequence cycle 11 for normal/slow region (sl, nsl, ary, se, fce).
59:63	RW	SEQ_12: Sequence cycle 12 for normal/slow region (sl, nsl, ary, se, fce).

Register Name	OPCG Control Register Capture 2
Mnemonic	TP.TCMC01.MCSLOW.OPCG_CAPT2
Address	0000000007030011 (SCOM)
Description	OPCG Control Register Capture 2

Bits	SCOM	Field Mnemonic: Description
0:3	RW	UNUSED_CAPT2:
4:8	RW	SEQ_13_01EVEN: Sequence cycle 1: Even, for fast region, or cycle 13, for normal region (sl, nsl, ary, se, fce).
9:13	RW	SEQ_14_01ODD: Sequence cycle 1: Odd, for fast region, or cycle 14, for normal region (sl, nsl, ary, se, fce).
14:18	RW	SEQ_15_02EVEN: Sequence cycle 2: Even, for fast region, or cycle 15, for normal region (sl, nsl, ary, se, fce).
19:23	RW	SEQ_16_02ODD: Sequence cycle 2: Odd, for fast region, or cycle 16, for normal region (sl, nsl, ary, se, fce).
24:28	RW	SEQ_17_03EVEN: Sequence cycle 3: Even, for fast region, or cycle 17, for normal region (sl, nsl, ary, se, fce).
29:33	RW	SEQ_18_03ODD: Sequence cycle 3: Odd, for fast region, or cycle 18, for normal region (sl, nsl, ary, se, fce).
34:38	RW	SEQ_19_04EVEN: Sequence cycle 4: Even, for fast region, or cycle 19, for normal region (sl, nsl, ary, se, fce).
39:43	RW	SEQ_20_04ODD: Sequence cycle 4: Odd, for fast region, or cycle 20, for normal region (sl, nsl, ary, se, fce).
44:48	RW	SEQ_21_05EVEN: Sequence cycle 5: Even, for fast region, or cycle 21, for normal region (sl, nsl, ary, se, fce).
49:53	RW	SEQ_22_05ODD: Sequence cycle 5: Odd, for fast region, or cycle 22, for normal region (sl, nsl, ary, se, fce).
54:58	RW	SEQ_23_06EVEN: Sequence cycle 6: Even, for fast region, or cycle 23, for normal region (sl, nsl, ary, se, fce).
59:63	RW	SEQ_24_06ODD: Sequence cycle 6: Odd, for fast region, or cycle 24, for normal region (sl, nsl, ary, se, fce).

Register Name	OPCG Control Register Capture 3
Mnemonic	TP.TCMC01.MCSLOW.OPCG_CAPT3
Address	0000000007030012 (SCOM)
Description	OPCG Control Register Capture 3

Bits	SCOM	Field Mnemonic: Description
0:3	RW	UNUSED_CAPT3:
4:8	RW	SEQ_07EVEN: Sequence cycle 7: Even for fast region (sl, nsl, ary, se, fce).
9:13	RW	SEQ_07ODD: Sequence cycle 7: Odd for fast region (sl, nsl, ary, se, fce).
14:18	RW	SEQ_08EVEN: Sequence cycle 8: Even for fast region (sl, nsl, ary, se, fce).
19:23	RW	SEQ_08ODD: Sequence cycle 8: Odd for fast region (sl, nsl, ary, se, fce).
24:28	RW	SEQ_09EVEN: Sequence cycle 9: Even for fast region (sl, nsl, ary, se, fce).
29:33	RW	SEQ_09ODD: Sequence cycle 9: Odd for fast region (sl, nsl, ary, se, fce).
34:38	RW	SEQ_10EVEN: Sequence cycle 10: Even for fast region (sl, nsl, ary, se, fce).
39:43	RW	SEQ_10ODD: Sequence cycle 10: Odd for fast region (sl, nsl, ary, se, fce).
44:48	RW	SEQ_11EVEN: Sequence cycle 11: Even for fast region (sl, nsl, ary, se, fce).

Bits	SCOM	Field Mnemonic: Description
49:53	RW	SEQ_11ODD: Sequence cycle 11: Odd for fast region (sl, nsl, ary, se, fce).
54:58	RW	SEQ_12EVEN: Sequence cycle 12: Even for fast region (sl, nsl, ary, se, fce).
59:63	RW	SEQ_12ODD: Sequence cycle 12: Odd for fast region (sl, nsl, ary, se, fce).

Register Name	Debug CBS CC Register
Mnemonic	TP.TCMC01.MCSLOW.DBG_CBS_CC
Address	0000000007030013 (SCOM)
Description	Debug CBS CC Register

Bits	SCOM	Field Mnemonic: Description
0	ROX	DBG_RESET_EP: Reset endpoint. Are the CC and CTRL in a reset state?
1	ROX	DBG_OPCG_IP: OPCG in progress, not in idle.
2	ROX	DBG_VITL_CLKOFF: VITL HLD stopped when enabled. Need pipeline-latch-depth cycles to switch this latch.
3	ROX	DBG_TEST_ENABLE: Test enable.
4	ROX	DBG_CBS_REQ: CBS interface: request (latched).
5:7	ROX	DBG_CBS_CMD: CBS interface: command (latched).
8:12	ROX	DBG_CBS_STATE: CBS command state machine. 00000 = Idle
13	ROX	DBG_SECURITY_DEBUG_MODE: Status of the security mode bit.
14	ROX	DBG_CBS_PROTOCOL_ERROR: CBS protocol error. REQ raised, although the state machine is not in IDLE. Need reset_ep to clear this bit. There is no impact on IPL.
15	ROX	DBG_PCB_IDLE: PCB Interface in IDLE state.
16:19	ROX	DBG_CURRENT_OPCG_MODE: Current or latest OPCG mode: 0 = NOP 1 = LBIST 2 = ABIST 3 = RUNN 4 = SCAN0 5 = SCAN 6 = SCAN rotate 7 = SCAN with UpdateDR 8 = SCAN with CaptureDR 9 = CLK Change Request 10 - 15 = Unused
20:23	ROX	DBG_LAST_OPCG_MODE: Previous OPCG mode.
24	ROX	DBG_PCB_ERROR: PCB interface error. Read the CC Error Register or set CBS_CMD = 001 to switch FSI CBS debug information to the CC Error Register.
25	ROX	DBG_PARITY_ERROR: Any parity error or non-PCB parity. Read the CC Error Register or set CBS_CMD = 001 to switch FSI CBS Debug Information to the CC Error Register.
26	ROX	DBG_CC_ERROR: Any other CC error. Read the CC Error Register or set CBS_CMD = 001 to switch FSI CBS debug information to the CC Error Register.
27	ROX	DBG_CHIPLET_IS_ALIGNED: This bit is 1 when a valid align pulse was sent out.
28	ROX	DBG_PCB_REQUEST_SINCE_RESET: Reset clears this bit; the first PCB request sets it.
29	ROX	DBG_PARANOIA_TEST_ENABLE_CHANGE: The rising or falling edge on test enable, after reset. Need reset_ep to clear. There is no impact on the IPL.

Bits	SCOM	Field Mnemonic: Description
30	ROX	DBG_PARANOIA_VITL_CLKOFF_CHANGE: Rising or falling edge on vitl_clkoff, after reset. Need reset_ep to clear. There is no impact on IPL.
31	ROX	TP_TPFSI_CBS_ACK: Only representation of the CC ACK signal going to the FSI.

Register Name	CC Protect Mode Register
Mnemonic	TP.TCMC01.MCSLOW.CC_PROTECT_MODE_REG
Address	00000000070303FE (SCOM)
Description	This register enables read and write protection.

Bits	SCOM	Field Mnemonic: Description
0	RW	CC_READ_PROTECT_ENABLE: Enable read protection.
1	RW	CC_WRITE_PROTECT_ENABLE: Enable write protection.

Register Name	Atomic Lock Register
Mnemonic	TP.TCMC01.MCSLOW.CC_ATOMIC_LOCK_REG
Address	00000000070303FF (SCOM)
Description	This register enables an atomic lock.

Bits	SCOM	Field Mnemonic: Description
0	RW	CC_ATOMIC_LOCK_ENABLE: This bit enables an atomic lock.
1:4	ROX	CC_ATOMIC_ID: This field contains the atomic ID.
5:7	RO	Constant = 0b000
8:15	ROX	CC_ATOMIC_ACTIVITY: This field is the atomic lock counter.

Register Name	Global Checkstop FIR
Mnemonic	TP.TCMC01.MCSLOW.XFIR
Address	0000000007040000 (SCOM)
Description	This is a fault-isolation register for global FIRs.

Bits	SCOM	Field Mnemonic: Description
0	RWX	XFIR_IN0: Summary bit.
1	RWX	XFIR_IN1: Checkstop broadcast via OOB.
2	RWX	XFIR_IN2: Unused.
3	RWX	XFIR_IN3: Checkstop from the pervasive unit.
4	RWX	XFIR_IN4: Checkstop from MC01_0.
5	RWX	XFIR_IN5: Checkstop from MC01_1.
6	RWX	XFIR_IN6: Checkstop from MC01_2 FIR.
7	RWX	XFIR_IN7: Checkstop from MC01_3 FIR.
8	RWX	XFIR_IN8: Checkstop from MC01_4 FIR.

Bits	SCOM	Field Mnemonic: Description
9	RWX	XFIR_IN9: Checkstop from MC01_5 FIRP.
10	RWX	XFIR_IN10: Checkstop from MC01_6 FIR.
11	RWX	XFIR_IN11: Checkstop from MC01_7 FIRP.
12	RWX	XFIR_IN12: Checkstop from MC01_8 FIR.
13	RWX	XFIR_IN13: Checkstop from IOM01 FIRP.
14	RWX	XFIR_IN14: Checkstop from IOM23 FIR.
15	RWX	XFIR_IN15: Checkstop from IOM01 FIRP unstaged.
16	RWX	XFIR_IN16: Checkstop from IOM23 FIR unstaged.
17:25	RWX	XFIR_IN17: Unused.
26	RWX	XFIR_IN26: Checkstop on debug trigger.

Register Name	Global Recoverable FIR
Mnemonic	TP.TCMC01.MCSLOW.RFIR
Address	0000000007040001 (SCOM)
Description	This is a fault-isolation register for global recoverable errors.

Bits	SCOM	Field Mnemonic: Description
0	ROX	RFIR_IN0: Local checkstop from MC.
1	ROX	LFIR_RECOV_ERR: Recoverable error from the pervasive unit.
2	ROX	RFIR_IN4: Recoverable error from MC01_0.
3	ROX	RFIR_IN5: Recoverable error from MC01_1.
4	ROX	RFIR_IN6: Recoverable error from MC01_2 FIR.
5	ROX	RFIR_IN7: Recoverable error from MC01_3 FIR.
6	ROX	RFIR_IN8: Recoverable error from MC01_4 FIR.
7	ROX	RFIR_IN9: Recoverable error from MC01_5 FIR.
8	ROX	RFIR_IN10: Recoverable error from MC01_6 FIR.
9	ROX	RFIR_IN11: Recoverable error from MC01_7 FIR.
10	ROX	RFIR_IN12: Recoverable error from MC01_8 FIR.
11	ROX	RFIR_IN13: Recoverable error from IOM01 FIR.
12	ROX	RFIR_IN14: Recoverable error from IOM23 FIR.
13	ROX	RFIR_IN15: Recoverable error from IOM01 FIR unstaged.
14	ROX	RFIR_IN16: Recoverable error from IOM23 FIR unstaged.
15:23	ROX	RFIR_IN17: Unused.

Register Name	FIR Mask Register
Mnemonic	TP.TCMC01.MCSLOW.FIR_MASK
Address	0000000007040002 (SCOM)
Description	FIR Mask

Bits	SCOM	Field Mnemonic: Description
0	RW	FIR_MASK_IN0: Mask for XFIR summary bit.
1	RW	FIR_MASK_IN1: Mask for XFIR broadcast via OOB.
2	RW	FIR_MASK_IN2: Unused.
3	RW	FIR_MASK_IN3: Mask for XFIR/ RFIR from the pervasive unit.
4	RW	FIR_MASK_IN4: Mask for MC01_0 XFIR and RFIR.
5	RW	FIR_MASK_IN5: Mask for MC01_1 XFIR and RFIR.
6	RW	FIR_MASK_IN6: Mask for MC01_2 XFIR and RFIR.
7	RW	FIR_MASK_IN7: Mask for MC01_3 XFIR and RFIR.
8	RW	FIR_MASK_IN8: Mask for MC01_4 XFIR and RFIR.
9	RW	FIR_MASK_IN9: Mask for MC01_5 XFIR and RFIR.
10	RW	FIR_MASK_IN10: Mask for MC01_6 XFIR and RFIR.
11	RW	FIR_MASK_IN11: Mask for MC01_7 XFIR and RFIR.
12	RW	FIR_MASK_IN12: Mask for MC01_8 XFIR and RFIR.
13	RW	FIR_MASK_IN13: Mask for IOM01 XFIR and RFIR.
14	RW	FIR_MASK_IN14: Mask for IOM23 XFIR and RFIR.
15	RW	FIR_MASK_IN15: Mask for IOM01 XFIR and RFIR.
16	RW	FIR_MASK_IN16: Mask for IOM23 XFIR and RFIR.
17:25	RW	FIR_MASK_IN17: Unused.
26	RW	FIR_MASK_IN26: Mask for debug trigger and local checkstop to recoverable error.

Register Name	Special Attention Register
Mnemonic	TP.TCMC01.MCSLOW.SPATTN
Address	0000000007040004 (SCOM) 0000000007040005 (SCOM1) 0000000007040006 (SCOM2)
Description	This register contains special attention fields.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	ROX	NCX	NCX	SPATTN_IN0: Special attention from MC01_0.
1	ROX	NCX	NCX	SPATTN_IN1: Special attention from MC01_1.
2	ROX	NCX	NCX	SPATTN_IN2: Special attention from MC01_2.
3	ROX	NCX	NCX	SPATTN_IN3: Special attention from MC01_3.
4	ROX	NCX	NCX	SPATTN_IN4: Special attention from MC01_4.
5	ROX	NCX	NCX	SPATTN_IN5: Special attention from MC01_5.
6	ROX	NCX	NCX	SPATTN_IN6: Special attention from MC01_6.
7	ROX	NCX	NCX	SPATTN_IN7: Special attention from MC01_7.
8	ROX	NCX	NCX	SPATTN_IN8: Special attention from MC01_8.
9	ROX	NCX	NCX	SPATTN_IN9: Unused.

Register Name	Special Attention Mask Register
Mnemonic	TP.TCMC01.MCSLOW.SPA_MASK
Address	0000000007040007 (SCOM)
Description	This register provides a special attention mask.

Bits	SCOM	Field Mnemonic: Description
0:9	RW	SPA_MASK_IN: Special attention mask.

Register Name	Mode Register
Mnemonic	TP.TCMC01.MCSLOW.EPS.FIR.MODE_REG
Address	0000000007040008 (SCOM)
Description	This register contains mode bits.

Bits	SCOM	Field Mnemonic: Description
0	RW	MODE_IN0: Unused.
1	RW	MODE_IN1: Unused.
2	RW	MODE_IN2: Unused.
3	RW	MODE_IN3: Unused.
4	RW	MODE_IN4: Stop chip TOD on checkstop.
5	RW	MODE_IN5: Stop chip TOD on recoverable.
6	RW	MODE_IN6: Disable the propagation of checkstops to other chips.
7	RW	MODE_IN7: Unused.
8	RW	MODE_IN8: Enable checkstop on special attention.
9	RW	MODE_IN9: Mask direct/local error.
10	RW	MODE_IN10: Unused.
11	RW	MODE_IN11: Unused.
12:15	RW	MODE_IN: Unused.

Register Name	Host Attention Register
Mnemonic	TP.TCMC01.MCSLOW.HOSTATTN
Address	0000000007040009 (SCOM)
Description	This register contains host attention bits.

Bits	SCOM	Field Mnemonic: Description
0	ROX	HOSTATTN_IN0: Host attention summary bit.
1	ROX	HOSTATTN_IN1: Host attention input from MC bit 0.
2	ROX	HOSTATTN_IN2: Host attention input from MC bit 1.
3	ROX	HOSTATTN_IN3: Host attention input from MC bit 2.
4	ROX	HOSTATTN_IN4: Host attention input from MC bit 3.
5	ROX	HOSTATTN_IN5: Host attention input from MC bit 4.

Bits	SCOM	Field Mnemonic: Description
6	ROX	HOSTATTN_IN6: Host attention input from MC bit 5.
7	ROX	HOSTATTN_IN7: Host attention input from MC bit 6.
8	ROX	HOSTATTN_IN8: Host attention input from MC bit 7.
9	ROX	HOSTATTN_IN9: Host attention input from MC bit 8.
10	ROX	HOSTATTN_IN10: Unused.
11	ROX	HOSTATTN_IN11: Unused.
12	ROX	HOSTATTN_IN12: Unused.
13	ROX	HOSTATTN_IN13: Unused.
14	ROX	HOSTATTN_IN14: Unused.
15	ROX	HOSTATTN_IN15: Unused.
16	ROX	HOSTATTN_IN16: Unused.
17	ROX	HOSTATTN_IN17: Unused.
18	ROX	HOSTATTN_IN18: Unused.
19	ROX	HOSTATTN_IN19: Unused.
20	ROX	HOSTATTN_IN20: Unused.
21	ROX	HOSTATTN_IN21: Unused.
22	ROX	HOSTATTN_IN22: Unused.

Register Name	**Local FIR**
Mnemonic	TP.TCMC01.MCSLOW.LOCAL_FIR
Address	000000000704000A (SCOM) 000000000704000B (SCOM1) 000000000704000C (SCOM2)
Description	This is a fault-isolation register for local errors.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_IN0: CFIR internal parity error.
1	RWX	WOX_AND	WOX_OR	FIR_IN1: Local errors from GPIO (PCB error).
2	RWX	WOX_AND	WOX_OR	FIR_IN2: Local errors from CC (PCB error).
3	RWX	WOX_AND	WOX_OR	FIR_IN3: Local errors from CC (OPCG, parity, scan collision, and so on).
4	RWX	WOX_AND	WOX_OR	FIR_IN4: Local errors from PSC (PCB error).
5	RWX	WOX_AND	WOX_OR	FIR_IN5: Local errors from PSC (parity error).
6	RWX	WOX_AND	WOX_OR	FIR_IN6: Local errors from Thermal (parity error).
7	RWX	WOX_AND	WOX_OR	FIR_IN7: Local errors from Thermal (PCB error).
8	RWX	WOX_AND	WOX_OR	FIR_IN8: Local errors from Thermal (trip error critical).
9	RWX	WOX_AND	WOX_OR	FIR_IN9: Local errors from Thermal (trip error fatal).
10	RWX	WOX_AND	WOX_OR	FIR_IN10: Therm voltage trip error.
11	RWX	WOX_AND	WOX_OR	FIR_IN11: Local errors from debug (error).
12	RWX	WOX_AND	WOX_OR	FIR_IN12: Local errors from Trace Array 0 (SCOM error).

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
13	RWX	WOX_AND	WOX_OR	FIR_IN13: Local errors from Trace Array 0.
14	RWX	WOX_AND	WOX_OR	FIR_IN14: Local errors from MC Trace Array (SCOM error).
15	RWX	WOX_AND	WOX_OR	FIR_IN15: Local errors from MC Trace Array.
16	RWX	WOX_AND	WOX_OR	FIR_IN16: Unused.
17	RWX	WOX_AND	WOX_OR	FIR_IN17: Unused.
18	RWX	WOX_AND	WOX_OR	FIR_IN18: Unused.
19	RWX	WOX_AND	WOX_OR	FIR_IN19: Unused.
20	RWX	WOX_AND	WOX_OR	FIR_IN20: Unused.
21	RWX	WOX_AND	WOX_OR	FIR_IN21: Unused.
22	RWX	WOX_AND	WOX_OR	FIR_IN22: Unused.
23	RWX	WOX_AND	WOX_OR	FIR_IN23: Unused.
24	RWX	WOX_AND	WOX_OR	FIR_IN24: Unused.
25	RWX	WOX_AND	WOX_OR	FIR_IN25: Unused.
26	RWX	WOX_AND	WOX_OR	FIR_IN26: Unused.
27	RWX	WOX_AND	WOX_OR	FIR_IN27: Unused.
28	RWX	WOX_AND	WOX_OR	FIR_IN28: Unused.
29	RWX	WOX_AND	WOX_OR	FIR_IN29: Unused.
30	RWX	WOX_AND	WOX_OR	FIR_IN30: Unused.
31	RWX	WOX_AND	WOX_OR	FIR_IN31: Unused.
32	RWX	WOX_AND	WOX_OR	FIR_IN32: Unused.
33	RWX	WOX_AND	WOX_OR	FIR_IN33: Unused.
34	RWX	WOX_AND	WOX_OR	FIR_IN34: Unused.
35	RWX	WOX_AND	WOX_OR	FIR_IN35: Unused.
36	RWX	WOX_AND	WOX_OR	FIR_IN36: Unused.
37	RWX	WOX_AND	WOX_OR	FIR_IN37: Unused.
38	RWX	WOX_AND	WOX_OR	FIR_IN38: Unused.
39	RWX	WOX_AND	WOX_OR	FIR_IN39: Unused.
40	RWX	WOX_AND	WOX_OR	FIR_IN40: Unused.
41	RWX	WOX_AND	WOX_OR	FIR_IN41: Malfunction alert broadcast via the OOB.

Register Name	**Local FIR Mask Register**
Mnemonic	TP.TCMC01.MCSLOW.EPS.FIR.LOCAL_FIR_MASK
Address	000000000704000D (SCOM) 000000000704000E (SCOM1) 000000000704000F (SCOM2)
Description	This register masks the local FIR bits.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:41	RW	WO_AND	WO_OR	LFIR_MASK_IN: Mask for the LEM error collection vector.

Register Name	Local FIR Action0 Register
Mnemonic	TP.TCMC01.MCSLOW.EPS.FIR.LOCAL_FIR_ACTION0
Address	0000000007040010 (SCOM)
Description	Local FIR Action0

Bits	SCOM	Field Mnemonic: Description
0:41	RW	FIR_ACTION0_IN: Action0 mask.

Register Name	Local FIR Action1 Register
Mnemonic	TP.TCMC01.MCSLOW.EPS.FIR.LOCAL_FIR_ACTION1
Address	0000000007040011 (SCOM)
Description	Local FIR Action1

Bits	SCOM	Field Mnemonic: Description
0:41	RW	FIR_ACTION1_IN: Action1 mask.

Register Name	Group Checkstop Mask Register
Mnemonic	TP.TCMC01.MCSLOW.EPS.FIR.GXSTOP_TRIG_REG
Address	0000000007040013 (SCOM)
Description	This register masks group checkstops.

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP_TRIG_IN0: Mask bit for a system checkstop.
1	RW	GXSTP_TRIG_IN1: Mask bit for a recoverable error.
2	RW	GXSTP_TRIG_IN2: Mask bit for a special attention.
3	RW	GXSTP_TRIG_IN3: Mask bit for a local checkstop.
4	RW	GXSTP_TRIG_IN4: Mask bit for a type 4 error (host attention).
5	RW	GXSTP_TRIG_IN5: Mask bit for an OOB sys_checkstop input (0).
6	RW	GXSTP_TRIG_IN6: Mask bit for an OOB sys_checkstop input (1).
7	RW	GXSTP_TRIG_IN7: Mask bit for a group checkstop input (0).
8	RW	GXSTP_TRIG_IN8: Mask bit for a group checkstop input (1).
9	RW	GXSTP_TRIG_IN9: Mask bit for a debug checkstop on a trigger.
10	RW	GXSTP_TRIG_IN10: Unused.
11	RW	GXSTP_TRIG_IN11: Unused.

Register Name	Group0 Checkstop Mask Register
Mnemonic	TP.TCMC01.MCSLOW.EPS.FIR.GXSTOP0_MASK_REG
Address	0000000007040014 (SCOM)
Description	This register masks group 0 checkstops.

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP0_TRIG_IN0: Mask bit for a system checkstop.
1	RW	GXSTP0_TRIG_IN1: Mask bit for a recoverable error.
2	RW	GXSTP0_TRIG_IN2: Mask bit for a special attention.
3	RW	GXSTP0_TRIG_IN3: Mask bit for a local checkstop.
4	RW	GXSTP0_TRIG_IN4: Mask bit for a type 4 error (host attention).
5	RW	GXSTP0_TRIG_IN5: Mask bit for an OOB sys_checkstop input (0).
6	RW	GXSTP0_TRIG_IN6: Mask bit for an OOB sys_checkstop input (1).
7	RW	GXSTP0_TRIG_IN7: Mask bit for a group checkstop input (0).
8	RW	GXSTP0_TRIG_IN8: Mask bit for a group checkstop input (1).
9	RW	GXSTP0_TRIG_IN9: Mask bit for a debug checkstop on a trigger.
10	RW	GXSTP0_TRIG_IN10: Unused.
11	RW	GXSTP0_TRIG_IN11: Unused.

Register Name	Group1 Checkstop Mask Register
Mnemonic	TP.TCMC01.MCSLOW.EPS.FIR.GXSTOP1_MASK_REG
Address	0000000007040015 (SCOM)
Description	This register masks group 1 checkstops. Reg

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP1_TRIG_IN0: Mask bit for a system checkstop.
1	RW	GXSTP1_TRIG_IN1: Mask bit for a recoverable error.
2	RW	GXSTP1_TRIG_IN2: Mask bit for a special attention.
3	RW	GXSTP1_TRIG_IN3: Mask bit for a local checkstop.
4	RW	GXSTP1_TRIG_IN4: Mask bit for a type 4 error (host attention).
5	RW	GXSTP1_TRIG_IN5: Mask bit for an OOB sys_checkstop input (0).
6	RW	GXSTP1_TRIG_IN6: Mask bit for an OOB sys_checkstop input (1).
7	RW	GXSTP1_TRIG_IN7: Mask bit for a group checkstop input (0).
8	RW	GXSTP1_TRIG_IN8: Mask bit for a group checkstop input (1).
9	RW	GXSTP1_TRIG_IN9: Mask bit for a debug checkstop on a trigger.
10	RW	GXSTP1_TRIG_IN10: Unused.
11	RW	GXSTP1_TRIG_IN11: Unused.

Register Name	Group2 Checkstop Mask Register
Mnemonic	TP.TCMC01.MCSLOW.EPS.FIR.GXSTOP2_MASK_REG
Address	0000000007040016 (SCOM)
Description	This register masks group 2 checkstops.

Bits	SCOM	Field Mnemonic: Description
0	RW	GXSTP2_TRIG_IN0: Mask bit for a system checkstop.

Bits	SCOM	Field Mnemonic: Description
1	RW	GXSTP2_TRIG_IN1: Mask bit for a recoverable error.
2	RW	GXSTP2_TRIG_IN2: Mask bit for a special attention.
3	RW	GXSTP2_TRIG_IN3: Mask bit for a local checkstop.
4	RW	GXSTP2_TRIG_IN4: Mask bit for a type 4 error (host attention).
5	RW	GXSTP2_TRIG_IN5: Mask bit for an OOB sys_checkstop input (0).
6	RW	GXSTP2_TRIG_IN6: Mask bit for an OOB sys_checkstop input (1).
7	RW	GXSTP2_TRIG_IN7: Mask bit for a group checkstop input (0).
8	RW	GXSTP2_TRIG_IN8: Mask bit for a group checkstop input (1).
9	RW	GXSTP2_TRIG_IN9: Mask bit for a debug checkstop on a trigger.
10	RW	GXSTP2_TRIG_IN10: Unused.
11	RW	GXSTP2_TRIG_IN11: Unused.

Register Name	**Summary Mask Register**
Mnemonic	TP.TCMC01.MCSLOW.EPS.FIR.SUM_MASK_REG
Address	0000000007040017 (SCOM)
Description	This register contains summary bits.

Bits	SCOM	Field Mnemonic: Description
0	RW	SMASK_IN0: System checkstop summary bit.
1	RW	SMASK_IN1: Recoverable summary bit.
2	RW	SMASK_IN2: Special attention summary bit.
3	RW	SMASK_IN3: Local checkstop summary bit.
4	RW	SMASK_IN4: Type4 host attention summary bit.

Register Name	**Local Checkstop Register**
Mnemonic	TP.TCMC01.MCSLOW.LOCAL_XSTOP_ERR
Address	0000000007040018 (SCOM)
Description	This register contains local checkstop bits.

Bits	SCOM	Field Mnemonic: Description
0	ROX	LOCAL_XSTOP_IN0: Local checkstop summary bit.
1	ROX	LOCAL_XSTOP_IN1: Local checkstop error from MC bit 0.
2	ROX	LOCAL_XSTOP_IN2: Local checkstop error from MC bit 1.
3	ROX	LOCAL_XSTOP_IN3: Local checkstop error from MC bit 2.
4	ROX	LOCAL_XSTOP_IN4: Local checkstop error from MC bit 3.
5	ROX	LOCAL_XSTOP_IN5: Local checkstop error from MC bit 4.
6	ROX	LOCAL_XSTOP_IN6: Local checkstop error from MC bit 5.
7	ROX	LOCAL_XSTOP_IN7: Local checkstop error from MC bit 6.
8	ROX	LOCAL_XSTOP_IN8: Local checkstop error from MC bit 7.

Bits	SCOM	Field Mnemonic: Description
9	ROX	LOCAL_XSTOP_IN9: Local checkstop error from MC bit 8.
10	ROX	LOCAL_XSTOP_IN10: Unused.
11	ROX	LOCAL_XSTOP_IN11: Unused.
12	ROX	LOCAL_XSTOP_IN12: Unused.
13	ROX	LOCAL_XSTOP_IN13: Unused.
14	ROX	LOCAL_XSTOP_IN14: Unused.
15	ROX	LOCAL_XSTOP_IN15: Unused.
16	ROX	LOCAL_XSTOP_IN16: Unused.
17	ROX	LOCAL_XSTOP_IN17: Unused.
18	ROX	LOCAL_XSTOP_IN18: Unused.
19	ROX	LOCAL_XSTOP_IN19: Unused.
20	ROX	LOCAL_XSTOP_IN20: Unused.
21	ROX	LOCAL_XSTOP_IN21: Unused.
22	ROX	LOCAL_XSTOP_IN22: Unused.

Register Name	Local Checkstop Mask Register
Mnemonic	TP.TCMC01.MCSLOW.LOCAL_XSTOP_MASK
Address	0000000007040019 (SCOM)
Description	This register masks local checkstops.

Bits	SCOM	Field Mnemonic: Description
0:21	RW	LOCAL_XSTOP_MASK_IN: Local checkstop mask.

Register Name	Host Attention Mask Register
Mnemonic	TP.TCMC01.MCSLOW.HOSTATTN_MASK
Address	000000000704001A (SCOM)
Description	This register masks host attention.

Bits	SCOM	Field Mnemonic: Description
0:21	RW	HOSTATTN_MASK_IN: Host attention mask.

Register Name	DTS Loop1 Results Register
Mnemonic	TP.TCMC01.MCSLOW.EPS.THERM.DTS_RESULT0
Address	0000000007050000 (SCOM)
Description	This register contains digital thermal sensor (DTS) results.

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	DTS_0_RESULT: Calibrated DTS result of the sensor with ID 0.
16:31	ROX	DTS_1_RESULT: Calibrated DTS result of the sensor with ID 1.

Bits	SCOM	Field Mnemonic: Description
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	DTS Trace Results Register
Mnemonic	TP.TCMC01.MCSLOW.EPS.THERM.DTS_TRC_RESULT
Address	0000000007050003 (SCOM)
Description	This register contains DTS trace results.

Bits	SCOM	Field Mnemonic: Description
0:43	ROX	TIMESTAMP_COUNTER_VALUE: Time stamp counter value during DTS trace mode.
44	ROX	TIMESTAMP_COUNTER_OVERFLOW_ERR: Overflow error bit of the time stamp counter value during DTS trace mode.
45:47	RO	Constant = 0b000
48:63	ROX	DTS_1_RESULT: Calibrated DTS result of sensor with ID 1.

Register Name	CPM and DTS Enables and Controls Register
Mnemonic	TP.TCMC01.MCSLOW.EPS.THERM.THERM_MODE_REG
Address	000000000705000F (SCOM)
Description	This register is used to enable and control the critical path monitor (CPM) and digital thermal sensor (DTS).

Bits	SCOM	Field Mnemonic: Description
0	RW	THERM_DIS_CPM_BUBBLE_CORR: Critical path result bubble correction active.
1	RW	THERM_FORCE_THRES_ACT: This bit forces tpc_therm_thres_mac clock gating off and activates the clocks.
2:4	RW	THERM_THRES_TRIP_ENA: therm_thres_trip compare enables. 1XX = trip0 - warning X1X = trip1 - critical XX1 = trip2 - fatal
5	RW	THERM_DTS_SAMPLE_ENA: 0 = No DTS sampling. 1 = DTS sampling is enabled and a below counter compare match can occur.

Bits	SCOM	Field Mnemonic: Description
6:9	RW	THERM_SAMPLE_PULSE_CNT: A 16 MHz sample pulse is fed into an 18-bit counter. With the therm_sample_pulse_cnt it is possible to select a high-order bit of the counter to enable resolutions of sampling DTSs between 2.5 µs and 80 ms. An edge-detection circuit detects the rising edge of the selected counter bit, and this triggers a DTS sample. 0000 = 16 ms 0001 = 8 ms 0010 = 4 ms 0011 = 2 ms 0100 = 1 ms 0101 = 0.5 ms 0110 = 250 µs 0111 = 125 µs 1000 = 62 .5 µs 1001 = 31.3 µs 1010 = 15.6 µs 1011 = 7.8 µs 1100 = 3.9 µs 1101 = 2 µs 1110 = 1 µs 1111 = 0.5 µs
10:11	RW	THERM_THRES_MODE_ENA: Forces maximum or minimum mode in the threshold unit: 00 = Is off 11 = Is legal 10 = Maximum mode 01 = Minimum mode
12	RW	DTS_TRIGGER_MODE: Unused.
13	RW	DTS_TRIGGER_SEL: Unused.
14	RW	THERM_THRES_OVERFLOW_MASK: 0 = therm_overflow_err is enabled. 1 = therm_overflow_err is disabled.
15	RW	THERM_MODE_UNUSED: Unused.
16:19	RW	THERM_DTS_READ_SEL: Selects which DTS result is provided with PCB read addr_v(4): 0000 = DTS 0 0001 = DTS 1 0010 = DTS 2 0100 = DTS 4 1111 = Worst-case sensor
20:21	RW	THERM_DTS_ENABLE_L1: Loop1 DTS enables: 1X = DTS 0 available. X1 = DTS 1 available.
22:34	RO	Constant = 0b0000000000000
35:36	RW	Reserved.

Register Name	Skitter Control Register
Mnemonic	TP.TCMC01.MCSLOW.EPS.THERM.SKITTER_MODE_REG
Address	0000000007050010 (SCOM)
Description	This register controls skitter.

Bits	SCOM	Field Mnemonic: Description
0	RW	SKITTER_HOLD_SAMPLE: Forces skitter to hold the current sample.

Bits	SCOM	Field Mnemonic: Description
1	RW	DISABLE_SKITTER_STICKINESS: If '0', accumulation mode. A '1' samples a new value each cycle and resets the sticky value.
2:3	RW	SKITTER_MODE_UNUSED1: Unused.
4:5	RW	SKITTER_HOLD_DBGTRIG_SEL: bit0 = hold_on_trigger0 bit1 = hold_on_trigger1
6:7	RW	SKITTER_RESET_TRIG_SEL: bit0 = reset_sticky_on_trigger0 bit1 = reset_sticky_on_trigger1
8:9	RW	SKITTER_SAMPLE_GUTS: Selects the guts to measure: 00 = guts1 01 = guts2 10 = guts3 11 = guts4
10:43	RO	Constant = 0b00000000000000000000000000000000
44	ROX	SKITTER_HOLD_SAMPLE_WITH_TRIGGER: Forces skitter to hold the current sample on the DBG trigger. This has the highest priority.
45	ROX	SKITTER_DATA_V_LT: If '1', the data requested by a skitter force read register has finished and data is present in the skitter data register in the collector macro. The data can be read by any combination of V25/V26/V27 PCB reads.

Register Name	Error Injection Control Register
Mnemonic	TP.TCMC01.MCSLOW.EPS.THERM.INJECT_REG
Address	0000000007050011 (SCOM)
Description	This register controls error injection.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	THERM_INJECT_TRIP: 00 = No injection. 01 = Warning trip-level injection. 10 = Critical trip-level injection. 11 = Fatal trip-level injection.
2:3	RW	THERM_INJECT_MODE: 00 = No injection. 01 = Injection on the next DTS sample. 10 = Solid injection for the next DTS samples until the bit setting changes. 11 = Not used.

Register Name	Control/Force Reset Register
Mnemonic	TP.TCMC01.MCSLOW.EPS.THERM.CONTROL_REG
Address	0000000007050012 (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0	WO_1P	Reserved.
1	WO_1P	Reserved.

Bits	SCOM	Field Mnemonic: Description
2	WO_1P	Reserved.
3	WO_1P	Reserved.
4	WO_1P	Reserved.
5	WO_1P	Reserved.
6	WO_1P	Reserved.
7	WO_1P	Reserved.
8	WO_1P	Reserved.
9	WO_1P	Reserved.
10	WO_1P	Reserved.
11	WO_1P	Reserved.
12	WO_1P	Reserved.

Register Name	Thermal Error Status Register
Mnemonic	TP.TCMC01.MCSLOW.EPS.THERM.ERR_STATUS_REG
Address	0000000007050013 (SCOM)
Description	This register contains error masks.

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved.
1	ROX	Reserved.
2	ROX	Reserved.
3	ROX	Reserved.
4	ROX	Reserved.
5	ROX	Reserved.
6	ROX	Reserved.
7	ROX	Reserved.
8	ROX	Reserved.
9	ROX	Reserved.
10	ROX	Reserved.
11	ROX	Reserved.
12	ROX	Reserved.
13	ROX	Reserved.
14	ROX	Reserved.
15	ROX	Reserved.
16	ROX	SERIAL_SHIFTCNT_MODEREG_PARITY_ERR_MASK: Serial shift-count parity error mask.
17	ROX	THERM_MODEREG_PARITY_ERR_MASK: Thermal-mode register parity error mask.
18	ROX	SKITTER_MODEREG_PARITY_ERR_MASK: Skitter-mode register parity error mask.
19	ROX	SKITTER_FORCEREG_PARITY_ERR_MASK: Skitter force register parity error mask.
20	ROX	SCAN_INIT_VERSION_REG_PARITY_ERR_MASK: Scan init version register parity error mask.

Bits	SCOM	Field Mnemonic: Description
21	ROX	VOLT_MODEREG_PARITY_ERR_MASK: Volt mode register parity error mask.
22	RO	Constant = 0b0
23	ROX	COUNT_STATE_ERR_MASK: Count state machine error mask.
24	ROX	RUN_STATE_ERR_MASK: Run state machine error mask.
25	ROX	THRES_STATE_ERR_MASK: Threshold state machine error mask.
26	ROX	OVERFLOW_ERR_MASK: DTS calibration calculation overflow error mask.
27	ROX	SHIFTER_PARITY_ERR_MASK: Shifter parity error mask.
28	ROX	SHIFTER_VALID_ERR_MASK: Shifter valid error mask.
29	ROX	TIMEOUT_ERR_MASK: Timeout error mask.
30	ROX	F_SKITTER_READ_ERR_MASK: Force skitter read one hot error mask.
31	ROX	PCB_ERR_MASK: Pervasive control bus error mask.
32:39	RO	Constant = 0b00000000
40:43	ROX	Reserved.
44:46	ROX	Reserved.
47	ROX	Reserved.
48	ROX	Reserved.
49:50	ROX	Reserved.
51:54	ROX	Reserved.
55	ROX	Reserved.
56	ROX	Reserved.
57	ROX	Reserved.
58	ROX	Reserved.
59	ROX	Reserved.
60:63	RO	Constant = 0b0000

Register Name	Skitter Force Read Register
Mnemonic	TP.TCMC01.MCSLOW.EPS.THERM.SKITTER_FORCE_REG
Address	0000000007050014 (SCOM)
Description	This register forces a skitter read.

Bits	SCOM	Field Mnemonic: Description
0	RW	F_SKITTER_READ: Forces the read of that particular skitter.

Register Name	Skitter Clock SRC Control Register
Mnemonic	TP.TCMC01.MCSLOW.EPS.THERM.SKITTER_CLKSRC_REG
Address	0000000007050016 (SCOM)
Description	This register contains skitter controls.

Bits	SCOM	Field Mnemonic: Description
0:2	RW	SKITTER0_CLKSRC: Selects the clock to measure: 000 = Local mesh clock 001 = External pin skitter_c1_1_in 010 = Local d1clk only if d_mode = 1 011 = External pin skitter_c1_2_in 100 = Local lclk only if d_mode = 1 101 = External pin skitter_c1_3_in 110 = Unused 111 = External pin skitter_c1_4_in
3:35	RO	Constant = 0b00000000000000000000000000000000
36:37	RW	SKITTER0_DELAY_SELECT: Selects the delay to be added between the clock source multiplexer and the inverter chain of skitter0. (The base line delay is 12.2 psec.) 00 = No delay 01 = 0.6 psec 10 = 1.8 psec 11 = 5 psec

Register Name	Skitter Data Register Read Bits 0:63
Mnemonic	TP.TCMC01.MCSLOW.EPS.THERM.SKITTER_DATA0
Address	0000000007050019 (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved.

Register Name	Skitter Data Register Read Bits 32:95
Mnemonic	TP.TCMC01.MCSLOW.EPS.THERM.SKITTER_DATA1
Address	000000000705001A (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved.

Register Name	Skitter Data Register Read Bits 64:127
Mnemonic	TP.TCMC01.MCSLOW.EPS.THERM.SKITTER_DATA2
Address	000000000705001B (SCOM)
Description	This is a reserved register.

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	Reserved.

Register Name	Time-stamp Counter Read Register
Mnemonic	TP.TCMC01.MCSLOW.EPS.THERM.TIMESTAMP_COUNTER_READ
Address	000000000705001C (SCOM)
Description	This register contains the time-stamp counter value during DTS trace mode and an overflow error bit.

Bits	SCOM	Field Mnemonic: Description
0:43	ROX	TIMESTAMP_COUNTER_VALUE: Time-stamp counter value during DTS trace mode.
44	ROX	TIMESTAMP_COUNTER_OVERFLOW_ERR: Overflow error bit of the time-stamp counter value during DTS trace mode.

4. Memory PCB Slave Registers

The memory pervasive control bus (PCB) slave registers are listed alphabetically by mnemonic in the following address table.

Mnemonic	Address	Page
TP.TPCHIP.NET.PCBSLMC01.ASSIST_INTERRUPT_REG	0x00000000070F0011	480
TP.TPCHIP.NET.PCBSLMC01.ATOMIC_LOCK_REG	0x00000000070F03FF	487
TP.TPCHIP.NET.PCBSLMC01.ATTN_INTERRUPT_REG	0x00000000070F001A	481
TP.TPCHIP.NET.PCBSLMC01.EDRAM_STATUS	0x00000000070F0029	485
TP.TPCHIP.NET.PCBSLMC01.ERROR_REG	0x00000000070F001F	482
TP.TPCHIP.NET.PCBSLMC01.HANG_PULSE_0_REG	0x00000000070F0020	483
TP.TPCHIP.NET.PCBSLMC01.HANG_PULSE_1_REG	0x00000000070F0021	483
TP.TPCHIP.NET.PCBSLMC01.HANG_PULSE_2_REG	0x00000000070F0022	483
TP.TPCHIP.NET.PCBSLMC01.HANG_PULSE_3_REG	0x00000000070F0023	484
TP.TPCHIP.NET.PCBSLMC01.HANG_PULSE_4_REG	0x00000000070F0024	484
TP.TPCHIP.NET.PCBSLMC01.HANG_PULSE_5_REG	0x00000000070F0025	484
TP.TPCHIP.NET.PCBSLMC01.HANG_PULSE_6_REG	0x00000000070F0026	484
TP.TPCHIP.NET.PCBSLMC01.HEARTBEAT_REG	0x00000000070F0018	481
TP.TPCHIP.NET.PCBSLMC01.MULTICAST_GROUP_1	0x00000000070F0001	478
TP.TPCHIP.NET.PCBSLMC01.MULTICAST_GROUP_2	0x00000000070F0002	478
TP.TPCHIP.NET.PCBSLMC01.MULTICAST_GROUP_3	0x00000000070F0003	479
TP.TPCHIP.NET.PCBSLMC01.MULTICAST_GROUP_4	0x00000000070F0004	479
TP.TPCHIP.NET.PCBSLMC01.NET_CTRL0	0x00000000070F0040	485
TP.TPCHIP.NET.PCBSLMC01.NET_CTRL1	0x00000000070F0044	486
TP.TPCHIP.NET.PCBSLMC01.PLL_LOCK_REG	0x00000000070F0019	481
TP.TPCHIP.NET.PCBSLMC01.PRE_COUNTER_REG	0x00000000070F0028	485
TP.TPCHIP.NET.PCBSLMC01.PRIMARY_ADDRESS_REG	0x00000000070F0000	478
TP.TPCHIP.NET.PCBSLMC01.PROTECT_MODE_REG	0x00000000070F03FE	487
TP.TPCHIP.NET.PCBSLMC01.RECOV_INTERRUPT_REG	0x00000000070F001B	481
TP.TPCHIP.NET.PCBSLMC01.SLAVE_CONFIG_REG	0x00000000070F001E	482
TP.TPCHIP.NET.PCBSLMC01.TIMEOUT_REG	0x00000000070F0010	480
TP.TPCHIP.NET.PCBSLMC01.VITAL_SCAN_OUT	0x00000000070F0017	480
TP.TPCHIP.NET.PCBSLMC01.XSTOP_INTERRUPT_REG	0x00000000070F001C	481

The memory PCB slave registers are listed in the following tables.

Register Name	Primary PCB Slave Address Register
Mnemonic	TP.TPCHIP.NET.PCBSLMC01.PRIMARY_ADDRESS_REG
Address	00000000070F0000 (SCOM)
Description	This register contains the PCB slave's primary address.

Bits	SCOM	Field Mnemonic: Description
0:5	RO	Reserved. This is the primary_address setting.

Register Name	Multicast Group 1 Register
Mnemonic	TP.TPCHIP.NET.PCBSLMC01.MULTICAST_GROUP_1
Address	00000000070F0001 (SCOM)
Description	Multicast Group Registers 1 – 4 are used to are used to assign chiplets to a specific multicast group within the pervasive connect bus (PCB). Multicast groups make it possible to address more than a single chiplet at a time. They are used to read or write the same resource in multiple chiplets at the same time. **Note:** Multicast groups are initially set up at IPL, but they can be modified at any time by firmware or power management code.

Bits	SCOM	Field Mnemonic: Description
0:2	RO	Constant = 0b111
3:5	RW	MULTICAST1_GROUP: Multicast group1 setting. Set this field to a multicast group that this chiplet should be a member of. The chiplet can be assigned to up to four multicast groups by setting this field in the four multicast group registers to the corresponding multicast group numbers. If the chiplet is member of less than four multicast groups, set this field to 0b111 in the multicast group register that is not required. The 0b111 setting indicates multicast group 7; all chiplets are members of multicast group 7 regardless of any multicast register being set to 0b111. 000: Multicast group 0. 001: Multicast group 1. 010: Multicast group 2. 011: Multicast group 3. 100: Multicast group 4 – unused. 101: Multicast group 5 – unused. 110: Multicast group 6 – unused. 111: Multicast group 7.

Register Name	Multicast Group 2 Register
Mnemonic	TP.TPCHIP.NET.PCBSLMC01.MULTICAST_GROUP_2
Address	00000000070F0002 (SCOM)
Description	Multicast Group Registers 1 – 4 are used to are used to assign chiplets to a specific multicast group within the pervasive connect bus (PCB). Multicast groups make it possible to address more than a single chiplet at a time. They are used to read or write the same resource in multiple chiplets at the same time. **Note:** Multicast groups are initially set up at IPL, but they can be modified at any time by firmware or power management code.

Bits	SCOM	Field Mnemonic: Description
0:2	RO	Constant = 0b111

Bits	SCOM	Field Mnemonic: Description
3:5	RW	MULTICAST2_GROUP: Multicast group2 setting. Set this field to a multicast group that this chiplet should be a member of. The chiplet can be assigned to up to four multicast groups by setting this field in the four multicast group registers to the corresponding multicast group numbers. If the chiplet is member of less than four multicast groups, set this field to 0b111 in the multicast group register that is not required. The 0b111 setting indicates multicast group 7; all chiplets are members of multicast group 7 regardless of any multicast register being set to 0b111. 000: Multicast group 0. 001: Multicast group 1. 010: Multicast group 2. 011: Multicast group 3. 100: Multicast group 4 – unused. 101: Multicast group 5 – unused. 110: Multicast group 6 – unused. 111: Multicast group 7.

Register Name	**Multicast Group 3 Register**
Mnemonic	TP.TPCHIP.NET.PCBSLMC01.MULTICAST_GROUP_3
Address	00000000070F0003 (SCOM)
Description	Multicast Group Registers 1 – 4 are used to are used to assign chiplets to a specific multicast group within the pervasive connect bus (PCB). Multicast groups make it possible to address more than a single chiplet at a time. They are used to read or write the same resource in multiple chiplets at the same time. **Note:** Multicast groups are initially set up at IPL, but they can be modified at any time by firmware or power management code.

Bits	SCOM	Field Mnemonic: Description
0:2	RO	Constant = 0b111
3:5	RW	MULTICAST3_GROUP: Multicast group3 setting. Set this field to a multicast group that this chiplet should be a member of. The chiplet can be assigned to up to four multicast groups by setting this field in the four multicast group registers to the corresponding multicast group numbers. If the chiplet is member of less than four multicast groups, set this field to 0b111 in the multicast group register that is not required. The 0b111 setting indicates multicast group 7; all chiplets are members of multicast group 7 regardless of any multicast register being set to 0b111. 000: Multicast group 0. 001: Multicast group 1. 010: Multicast group 2. 011: Multicast group 3. 100: Multicast group 4 – unused. 101: Multicast group 5 – unused. 110: Multicast group 6 – unused. 111: Multicast group 7.

Register Name	**Multicast Group 4 Register**
Mnemonic	TP.TPCHIP.NET.PCBSLMC01.MULTICAST_GROUP_4
Address	00000000070F0004 (SCOM)
Description	Multicast Group Registers 1 – 4 are used to are used to assign chiplets to a specific multicast group within the pervasive connect bus (PCB). Multicast groups make it possible to address more than a single chiplet at a time. They are used to read or write the same resource in multiple chiplets at the same time. **Note:** Multicast groups are initially set up at IPL, but they can be modified at any time by firmware or power management code.

Bits	SCOM	Field Mnemonic: Description
0:2	RO	Constant = 0b111
3:5	RW	MULTICAST4_GROUP: Multicast group4 setting. Set this field to a multicast group that this chiplet should be a member of. The chiplet can be assigned to up to four multicast groups by setting this field in the four multicast group registers to the corresponding multicast group numbers. If the chiplet is member of less than four multicast groups, set this field to 0b111 in the multicast group register that is not required. The 0b111 setting indicates multicast group 7; all chiplets are members of multicast group 7 regardless of any multicast register being set to 0b111. 000: Multicast group 0. 001: Multicast group 1. 010: Multicast group 2. 011: Multicast group 3. 100: Multicast group 4 – unused. 101: Multicast group 5 – unused. 110: Multicast group 6 – unused. 111: Multicast group 7.

Register Name	Timeout Select Register
Mnemonic	TP.TPCHIP.NET.PCBSLMC01.TIMEOUT_REG
Address	00000000070F0010 (SCOM)
Description	This register contains the int_timeout setting.

Bits	SCOM	Field Mnemonic: Description
0:1	RW	Reserved. This is the int_timeout setting.

Register Name	Assist Interrupt Register
Mnemonic	TP.TPCHIP.NET.PCBSLMC01.ASSIST_INTERRUPT_REG
Address	00000000070F0011 (SCOM)
Description	This register contains the attn, recov, and xstop (checkstop) settings.

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved. This is the attn setting.
1	ROX	Reserved. This is the recov setting.
2	ROX	Reserved. This is the xstop setting.

Register Name	Vital Scan Out Register
Mnemonic	TP.TPCHIP.NET.PCBSLMC01.VITAL_SCAN_OUT
Address	00000000070F0017 (SCOM)
Description	This register contains the vital scan out settings.

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved.

Register Name	Chiplet Heartbeat Register
Mnemonic	TP.TPCHIP.NET.PCBSLMC01.HEARTBEAT_REG
Address	00000000070F0018 (SCOM)
Description	This register indicates whether a chiplet heartbeat is detected.

Bits	SCOM	Field Mnemonic: Description
0	ROX	HEARTBEAT_DEAD: A chiplet heartbeat is not detected.

Register Name	PLL Lock Indications Register
Mnemonic	TP.TPCHIP.NET.PCBSLMC01.PLL_LOCK_REG
Address	00000000070F0019 (SCOM)
Description	This register contains lock indications from the PLLs,

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	Reserved. This is the lock setting.

Register Name	Attention Interrupt Register
Mnemonic	TP.TPCHIP.NET.PCBSLMC01.ATTN_INTERRUPT_REG
Address	00000000070F001A (SCOM)
Description	This register contains the attn setting.

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved. This is the attn setting.

Register Name	Recoverable Interrupt Register
Mnemonic	TP.TPCHIP.NET.PCBSLMC01.RECOV_INTERRUPT_REG
Address	00000000070F001B (SCOM)
Description	This register contains the recoverable interrupt setting.

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved. This is the recov setting.

Register Name	Checkstop Interrupt Register
Mnemonic	TP.TPCHIP.NET.PCBSLMC01.XSTOP_INTERRUPT_REG
Address	00000000070F001C (SCOM)
Description	This register contains the checkstop interrupt setting.

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved. This is the xstop setting.

Register Name	Slave Configuration Register
Mnemonic	TP.TPCHIP.NET.PCBSLMC01.SLAVE_CONFIG_REG
Address	00000000070F001E (SCOM)
Description	This is the slave configuration register.

Bits	SCOM	Field Mnemonic: Description
0	RW	CFG_DISABLE_PERV_THOLD_CHECK: This bit disables the pervasive threshold check.
1	RW	CFG_DISABLE_MALF_PULSE_GEN: This bit disables pulse generation for a malfunction alert. Switch back to level.
2	RW	CFG_STOP_HANG_CNT_SYS_XSTP: This bit disables the hang counter stop for a system checkstop.
3	RW	CFG_DISABLE_CL_ATOMIC_LOCK: This bit disables the atomic lock for chiplet accesses.
4	RW	CFG_DISABLE_HEARTBEAT: This bit disables the check for voltage and gridclock in the chiplet.
5	RW	CFG_DISABLE_FORCE_TO_ZERO: This bit disables the force to zero for error cases.
6	RW	CFG_PM_DISABLE: This bit disables the power management set/reset interface for net_ctrl registers.
7	RW	CFG_PM_MUX_DISABLE: This bit disables the power-management mux request signal.
8:13	RW	ERROR_MASK: These are mask bits for slave error reporting.
14:15	RW	Reserved.

Register Name	Error Capture Register
Mnemonic	TP.TPCHIP.NET.PCBSLMC01.ERROR_REG
Address	00000000070F001F (SCOM)
Description	This register is used to capture errors.

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLEAR	CE_ERROR: Correctable error on a PCB bus.
1:3	RWX_WCLEAR	CHIPLET_ERRORS: Errors reported by the chiplet. 000 = No error. 001 = XSCOM command blocked due to pending errors. 010 = Chiplet offline. 011 = Partial good. 100 = Invalid address, address error, or bad access type. 101 = Clock error. 110 = Parity error, received unexpected packet, or wrong packet number. 111 = Timeout. This register is for debug purposes only. It only holds meaningful data if it is cleared after each error.
4	RWX_WCLEAR	PARITY_ERROR: Parity error on the PCB Interface.
5	RWX_WCLEAR	DATA_BUFFER_ERROR: Parity error in the data buffer.
6	RWX_WCLEAR	ADDR_BUFFER_ERROR: Parity error in the address buffer.
7	RWX_WCLEAR	PCB_FSM_ERROR: Invalid state error in the PCB FSM.
8	RWX_WCLEAR	CL_FSM_ERROR: Invalid state error in the chiplet FSM.
9	RWX_WCLEAR	INT_RX_FSM_ERROR: Invalid state error in the interrupt RX FSM.
10	RWX_WCLEAR	INT_TX_FSM_ERROR: Invalid state error in the interrupt TX FSM.
11	RWX_WCLEAR	INT_TYPE_ERROR: Invalid interrupt type.

Bits	SCOM	Field Mnemonic: Description
12	RWX_WCLEAR	CL_DATA_ERROR: Parity error on the chiplet interface.
13	RWX_WCLEAR	INFO_ERROR: Parity error on the chiplet information lines.
14	RWX_WCLEAR	UNUSED_0:
15	RWX_WCLEAR	CHIPLET_ATOMIC_LOCK_ERROR: Chiplet atomic lock error.
16	RWX_WCLEAR	PCB_INTERFACE_ERROR: Error of the PCB interface component for the internal endpoint.
17	RWX_WCLEAR	CHIPLET_OFFLINE: A heartbeat check indicated that the chiplet is offline.
18	RWX_WCLEAR	EDRAM_SEQUENCE_ERR: Error in the eDRAM power-up sequence.
19	RWX_WCLEAR	CTRL_REG_PARITY_ERROR: The control register parity is bad.
20	RWX_WCLEAR	ADDRESS_REG_PARITY_ERROR: The address register parity is bad.
21	RWX_WCLEAR	TIMEOUT_REG_PARITY_ERROR: The timeout select register parity is bad.
22	RWX_WCLEAR	CONFIG_REG_PARITY_ERROR: The slave configuration register parity is bad.
23	RWX_WCLEAR	UNUSED_1:
24	RWX_WCLEAR	DIV_REG_PARITY_ERROR: The divider register parity is bad.
25:28	RWX_WCLEAR	PLL_UNLOCK_ERROR: Unlock from the chiplet PLL.

Register Name	Hang Pulse Generation Register 0
Mnemonic	TP.TPCHIP.NET.PCBSLMC01.HANG_PULSE_0_REG
Address	00000000070F0020 (SCOM)
Description	This register contains hang pulse 0 information.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_0: This field contains the value of hang pulse 0. The time period equals 2^{value} x (precounter_reg + 1) / pcb_freq. The range of valid values is 34 – 0.
6	RW	SUPPRESS_HANG_0: If set to '1', hang pulses are suppressed in case of a checkstop.

Register Name	Hang Pulse Generation Register 1
Mnemonic	TP.TPCHIP.NET.PCBSLMC01.HANG_PULSE_1_REG
Address	00000000070F0021 (SCOM)
Description	This register contains hang pulse 1 information.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_1: This field contains the value of hang pulse 1. The time period equals 2^{value} x (precounter_reg + 1) / pcb_freq. The range of valid values is 34 – 0.
6	RW	SUPPRESS_HANG_1: If set to '1', hang pulses are suppressed in case of a checkstop.

Register Name	Hang Pulse Generation Register 2
Mnemonic	TP.TPCHIP.NET.PCBSLMC01.HANG_PULSE_2_REG
Address	00000000070F0022 (SCOM)
Description	This register contains hang pulse 2 information.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_2: The value of hang pulse 2. The time period equals 2^{value} x (precounter_reg + 1) / pcb_freq. The range of valid values is 34 – 0.
6	RW	SUPPRESS_HANG_2: If set to '1', hang pulses are suppressed in case of a checkstop.

Register Name	Hang Pulse Generation Register 3
Mnemonic	TP.TPCHIP.NET.PCBSLMC01.HANG_PULSE_3_REG
Address	00000000070F0023 (SCOM)
Description	This register contains hang pulse 3 information.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_3: This field contains the value of hang pulse 3. The time period equals 2^{value} x (precounter_reg + 1) / pcb_freq. The range of valid values is 34 – 0.
6	RW	SUPPRESS_HANG_3: If set to '1', hang pulses are suppressed in case of a checkstop.

Register Name	Hang Pulse Generation Register 4
Mnemonic	TP.TPCHIP.NET.PCBSLMC01.HANG_PULSE_4_REG
Address	00000000070F0024 (SCOM)
Description	This register contains hang pulse 4 information.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_4: This field contains the value of hang pulse 4. The time period equals 2^{value} x (precounter_reg + 1) / pcb_freq. The range of valid values is 34 – 0.
6	RW	SUPPRESS_HANG_4: If set to '1', hang pulses are suppressed in case of a checkstop.

Register Name	Hang Pulse Generation Register 5
Mnemonic	TP.TPCHIP.NET.PCBSLMC01.HANG_PULSE_5_REG
Address	00000000070F0025 (SCOM)
Description	This register contains hang pulse 5 information. This hang counter is exclusively used to generate the malfunction alert pulse.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_5: This field contains the value of hang pulse 5. The time period equals 2^{value} x (precounter_reg + 1) / pcb_freq. The range of valid values is 34 – 0.
6	RW	SUPPRESS_HANG_5: If set to '1', hang pulses are suppressed in case of a checkstop.

Register Name	Hang Pulse Generation Register 6
Mnemonic	TP.TPCHIP.NET.PCBSLMC01.HANG_PULSE_6_REG
Address	00000000070F0026 (SCOM)
Description	This register contains hang pulse 6 information. This hang counter is exclusively used for the heartbeat generation

Bits	SCOM	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_6: This field contains the value of hang pulse 6. Time period = $2^{value} \times$ (precounter_reg + 1) / pcb_freq, The range of valid values is 34 – 0.
6	RW	SUPPRESS_HANG_6: If set to '1', hang pulses are suppressed in case of a checkstop.

Register Name	Hang Counter Clock Divider Register
Mnemonic	TP.TPCHIP.NET.PCBSLMC01.PRE_COUNTER_REG
Address	00000000070F0028 (SCOM)
Description	This register is the divider for the hang counter clock.

Bits	SCOM	Field Mnemonic: Description
0:7	RW	PRE_COUNTER: Divider for the hang counter clock. Divides the clock by n + 1 (Default: n = 0).

Register Name	eDRAM Control Status Register
Mnemonic	TP.TPCHIP.NET.PCBSLMC01.EDRAM_STATUS
Address	00000000070F0029 (SCOM)
Description	This register contains the eDRAM control status.

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	EDRAM_STAT: This field contains the eDRAM control status.

Register Name	NET CTRL0 Register
Mnemonic	TP.TPCHIP.NET.PCBSLMC01.NET_CTRL0
Address	00000000070F0040 (SCOM) 00000000070F0041 (SCOM1) 00000000070F0042 (SCOM2)
Description	This register contains NET controls. It is not applicable to the pervasive chiplet.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	CHIPLET_ENABLE: This bit is set if the chiplet is good.
1	RWX	RWX_WAND	RWX_WOR	PCB_EP_RESET: The output is ORed to the global EP reset.
2	RWX	RWX_WAND	RWX_WOR	CLK_ASYNC_RESET: POWER9 cache chiplet: EQ skew adjust reset. POWER9 core chiplet: Core duty cycle adjust reset. POWER9 memory chiplet: Memory glitchless multiplexer asynchronous reset.
3	RWX	RWX_WAND	RWX_WOR	PLL_TEST_EN: Test enable for the chiplet PLL.
4	RWX	RWX_WAND	RWX_WOR	PLL_RESET: Reset for the chiplet PLL.
5	RWX	RWX_WAND	RWX_WOR	PLL_BYPASS: Enable bypass for the chiplet PLL.
6	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN: Scan control for the chiplet vital domain.
7	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN_IN: Scan in for the chiplet vital domain.
8	RWX	RWX_WAND	RWX_WOR	VITAL_PHASE: Phase for the vital domain.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
9	RWX	RWX_WAND	RWX_WOR	FLUSH_ALIGN_OVR: When set to 1, this mechanism overrides automatic control by the clock controller of the flush, flush_nto1, and align signals in the chiplet.
10	RWX	RWX_WAND	RWX_WOR	VITAL_AL: Align for the vital domain.
11	RWX	RWX_WAND	RWX_WOR	ACT_DIS: ACT disable control for LCBs in the VITAL logic.
12	RWX	RWX_WAND	RWX_WOR	MPW1: Modify pulse width 1 (MPW1) control for LCBs in the VITAL logic.
13	RWX	RWX_WAND	RWX_WOR	MPW2: Modify pulse width 2 (MPW2) control for LCBs in the VITAL logic.
14	RWX	RWX_WAND	RWX_WOR	MPW3: Modify pulse width 3 (MPW3) control for LCBs in the VITAL logic.
15	RWX	RWX_WAND	RWX_WOR	DELAY_LCLKR: LCB control signal for the vital logic.
16	RWX	RWX_WAND	RWX_WOR	VITAL_THOLD: Threshold for the chiplet vital domain.
17	RWX	RWX_WAND	RWX_WOR	FLUSH_SCAN_N: Flush scan control.
18	RWX	RWX_WAND	RWX_WOR	FENCE_EN: Fencing signal for the chiplet.
19	RWX	RWX_WAND	RWX_WOR	CPLT_RCTRL: Chiplet receiver enable.
20	RWX	RWX_WAND	RWX_WOR	CPLT_DCTRL: Chiplet driver enable.
21	RWX	RWX_WAND	RWX_WOR	Reserved. (Access type is pm_access.)
22	RWX	RWX_WAND	RWX_WOR	ADJ_FUNC_CLKSEL: Clock select for the skew adjust and duty cycle adjust logic.
23:24	RWX	RWX_WAND	RWX_WOR	Reserved. This is the pm_access setting.
25	RWX	RWX_WAND	RWX_WOR	TP_FENCE_PCB: Fence the chiplet from the PCB bus. If set, the PCB slave reports “Chiplet Offline.”
26	RWX	RWX_WAND	RWX_WOR	LVLTRANS_FENCE: Fence control for the level translators.
27	RWX	RWX_WAND	RWX_WOR	ARRAY_WRITE_ASSIST_EN: Array write assist.
28	RWX	RWX_WAND	RWX_WOR	HTB_INTEST: HTB intest mode.
29	RWX	RWX_WAND	RWX_WOR	HTB_EXTEST: HTB intest mode.
30	RWX	RWX_WAND	RWX_WOR	Reserved. This is the pm_access setting.
31	RWX	RWX_WAND	RWX_WOR	PLLFORCE_OUT_EN: PLL force out enable.

Register Name	NET CTRL1 Register
Mnemonic	TP.TPCHIP.NET.PCBSLMC01.NET_CTRL1
Address	00000000070F0044 (SCOM) 00000000070F0045 (SCOM1) 00000000070F0046 (SCOM2)
Description	This register contains NET controls. It is not applicable to the pervasive chiplet.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	PLL_CLKIN_SEL: PLL clkin select.
1	RWX	RWX_WAND	RWX_WOR	CLK_DCC_BYPASS_EN: POWER9 cache chiplet: L2-0, L2-1, L3 duty cycle control bypass. POWER9 core chiplet: Core duty cycle control bypass. POWER9 memory chiplet: Memory duty cycle control bypass.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
2	RWX	RWX_WAND	RWX_WOR	CLK_PDLY_BYPASS_EN: POWER9 cache chiplet: L2-0, L2-1, L3 programmable delay bypass. POWER9 core chiplet: core programmable delay bypass. POWER9 memory chiplet: memory programmable delay bypass.
3	RWX	RWX_WAND	RWX_WOR	CLK_DIV_BYPASS_EN: Enable clock divider bypass.
4	RWX	RWX_WAND	RWX_WOR	REFCLK_CLKMUX0_SEL: Select for reference clock mux0.
5	RWX	RWX_WAND	RWX_WOR	REFCLK_CLKMUX1_SEL: Select for reference clock mux1.
6	RWX	RWX_WAND	RWX_WOR	PLL_BNDY_BYPASS_EN: Bypass for IOP PLL.
7	RWX	RWX_WAND	RWX_WOR	Reserved. This is the pcb_access setting.
8:15	RWX	RWX_WAND	RWX_WOR	DPLL_TEST_SEL: DPLL testout MUXing.
16:19	RWX	RWX_WAND	RWX_WOR	SB_STRENGTH: Sector buffer driver strength.
20	RWX	RWX_WAND	RWX_WOR	ASYNC_TYPE: This is a control signal for testing latches with asynchronous set and reset capabilities.
21	RWX	RWX_WAND	RWX_WOR	ASYNC_OBS: This is a control signal for testing latches with asynchronous set and reset capabilities.
22	RWX	RWX_WAND	RWX_WOR	CPM_CAL_SET: CPM calibrate.
23	RWX	RWX_WAND	RWX_WOR	SENSEADJ_RESET0: POWER9 cache chiplet: L2-0 duty cycle adjust reset.
24	RWX	RWX_WAND	RWX_WOR	SENSEADJ_RESET1: POWER9 cache chiplet: L2-1 duty cycle adjust reset.
25	RWX	RWX_WAND	RWX_WOR	CLK_PULSE_EN: Clock pulse mode enable.
26:27	RWX	RWX_WAND	RWX_WOR	CLK_PULSE_MODE: Clock pulse mode setting.
28:31	RWX	RWX_WAND	RWX_WOR	Reserved. This is the pcb_access setting.

Register Name	Protect Mode Register
Mnemonic	TP.TPCHIP.NET.PCBSLMC01.PROTECT_MODE_REG
Address	00000000070F03FE (SCOM)
Description	This register is used to enable read and write protection.

Bits	SCOM	Field Mnemonic: Description
0	RW	READ_PROTECT_ENABLE: Enable read protection.
1	RW	WRITE_PROTECT_ENABLE: Enable write protection.

Register Name	Atomic Lock Register
Mnemonic	TP.TPCHIP.NET.PCBSLMC01.ATOMIC_LOCK_REG
Address	00000000070F03FF (SCOM)
Description	This register contains atomic lock information.

Bits	SCOM	Field Mnemonic: Description
0	RW	ATOMIC_LOCK_ENABLE: This bit enables the atomic lock.
1:4	ROX	ATOMIC_ID: This field contains the atomic ID.

Bits	SCOM	Field Mnemonic: Description
5:7	RO	Constant = 0b000
8:15	ROX	ATOMIC_ACTIVITY: This is the atomic lock counter.

5. DDRPHY: ADR Registers

The address (ADR) architecture consists of a 24-bit master ADR block, attached to two ADR12 blocks, and a 20-bit slave ADR block, attached to an ADR12 block and an ADR8 block. The master and slave ADR blocks contain:

- The digital data processing blocks (APINs)
- The register and control interface
- An analog block that contains the PLL and phase rotators used to generate the phased clocks used as the time base for the memory interface signals

The ADR analog block contains the analog FIFO circuit and I/O. Both the master and slave ADR blocks have a side A and a side B as shown in the following table.

Configuration	Side A	Side B
24 (master)	ADR12 ('40xx'h)	ADR12 ('44xx'h)
20 (slave)	ADR12 ('48xx'h)	ADR8 ('4Cxx'h)

These double data rate physical interface (DDRPHY) ADR path registers are specific to each address/command lane of the 12- or 8-lane groups.

This section contains the addressable registers that are associated with an ADR partition. An ADR partition can be 12 bits or 8 bits. Each register is 16 bits wide, but only the width of the partition is used. All other bits are unused. The DDRPHY ADR registers are listed alphabetically by mnemonic in the following address table.

Mnemonic	Address	Page
IOM0.DDRPHY_ADR_DCD_CONTROL_P1_ADR32S0	0x800080380701143F	659
IOM0.DDRPHY_ADR_DCD_CONTROL_P1_ADR32S1	0x800084380701143F	698
IOM0.DDRPHY_ADR_DCD_CONTROL_P2_ADR32S0	0x800080380701183F	660
IOM0.DDRPHY_ADR_DCD_CONTROL_P2_ADR32S1	0x800084380701183F	699
IOM0.DDRPHY_ADR_DCD_CONTROL_P3_ADR32S0	0x8000803807011C3F	660
IOM0.DDRPHY_ADR_DCD_CONTROL_P3_ADR32S1	0x8000843807011C3F	700
IOM0.DDRPHY_ADR_DELAY0_P0_ADR0	0x800040040701103F	504
IOM0.DDRPHY_ADR_DELAY0_P0_ADR1	0x800044040701103F	537
IOM0.DDRPHY_ADR_DELAY0_P0_ADR2	0x800048040701103F	571
IOM0.DDRPHY_ADR_DELAY0_P0_ADR3	0x80004C040701103F	605
IOM0.DDRPHY_ADR_DELAY0_P1_ADR0	0x800040040701143F	504
IOM0.DDRPHY_ADR_DELAY0_P1_ADR1	0x800044040701143F	538
IOM0.DDRPHY_ADR_DELAY0_P1_ADR2	0x800048040701143F	572
IOM0.DDRPHY_ADR_DELAY0_P1_ADR3	0x80004C040701143F	606
IOM0.DDRPHY_ADR_DELAY0_P2_ADR0	0x800040040701183F	504
IOM0.DDRPHY_ADR_DELAY0_P2_ADR1	0x800044040701183F	538
IOM0.DDRPHY_ADR_DELAY0_P2_ADR2	0x800048040701183F	572
IOM0.DDRPHY_ADR_DELAY0_P2_ADR3	0x80004C040701183F	606
IOM0.DDRPHY_ADR_DELAY0_P3_ADR0	0x8000400407011C3F	505
IOM0.DDRPHY_ADR_DELAY0_P3_ADR1	0x8000440407011C3F	538
IOM0.DDRPHY_ADR_DELAY0_P3_ADR2	0x8000480407011C3F	572
IOM0.DDRPHY_ADR_DELAY0_P3_ADR3	0x80004C0407011C3F	606
IOM0.DDRPHY_ADR_DELAY1_P0_ADR0	0x800040050701103F	505
IOM0.DDRPHY_ADR_DELAY1_P0_ADR1	0x800044050701103F	539
IOM0.DDRPHY_ADR_DELAY1_P0_ADR2	0x800048050701103F	573
IOM0.DDRPHY_ADR_DELAY1_P0_ADR3	0x80004C050701103F	607
IOM0.DDRPHY_ADR_DELAY1_P1_ADR0	0x800040050701143F	506
IOM0.DDRPHY_ADR_DELAY1_P1_ADR1	0x800044050701143F	539
IOM0.DDRPHY_ADR_DELAY1_P1_ADR2	0x800048050701143F	573
IOM0.DDRPHY_ADR_DELAY1_P1_ADR3	0x80004C050701143F	607
IOM0.DDRPHY_ADR_DELAY1_P2_ADR0	0x800040050701183F	506
IOM0.DDRPHY_ADR_DELAY1_P2_ADR1	0x800044050701183F	540
IOM0.DDRPHY_ADR_DELAY1_P2_ADR2	0x800048050701183F	574
IOM0.DDRPHY_ADR_DELAY1_P2_ADR3	0x80004C050701183F	608
IOM0.DDRPHY_ADR_DELAY1_P3_ADR0	0x8000400507011C3F	506
IOM0.DDRPHY_ADR_DELAY1_P3_ADR1	0x8000440507011C3F	540
IOM0.DDRPHY_ADR_DELAY1_P3_ADR2	0x8000480507011C3F	574
IOM0.DDRPHY_ADR_DELAY1_P3_ADR3	0x80004C0507011C3F	608
IOM0.DDRPHY_ADR_DELAY2_P0_ADR0	0x800040060701103F	507
IOM0.DDRPHY_ADR_DELAY2_P0_ADR1	0x800044060701103F	540
IOM0.DDRPHY_ADR_DELAY2_P0_ADR2	0x800048060701103F	574
IOM0.DDRPHY_ADR_DELAY2_P0_ADR3	0x80004C060701103F	608
IOM0.DDRPHY_ADR_DELAY2_P1_ADR0	0x800040060701143F	507

Mnemonic	Address	Page
IOM0.DDRPHY_ADR_DELAY2_P1_ADR1	0x800044060701143F	541
IOM0.DDRPHY_ADR_DELAY2_P1_ADR2	0x800048060701143F	575
IOM0.DDRPHY_ADR_DELAY2_P1_ADR3	0x80004C060701143F	609
IOM0.DDRPHY_ADR_DELAY2_P2_ADR0	0x800040060701183F	508
IOM0.DDRPHY_ADR_DELAY2_P2_ADR1	0x800044060701183F	541
IOM0.DDRPHY_ADR_DELAY2_P2_ADR2	0x800048060701183F	575
IOM0.DDRPHY_ADR_DELAY2_P2_ADR3	0x80004C060701183F	609
IOM0.DDRPHY_ADR_DELAY2_P3_ADR0	0x8000400607011C3F	508
IOM0.DDRPHY_ADR_DELAY2_P3_ADR1	0x8000440607011C3F	542
IOM0.DDRPHY_ADR_DELAY2_P3_ADR2	0x8000480607011C3F	576
IOM0.DDRPHY_ADR_DELAY2_P3_ADR3	0x80004C0607011C3F	610
IOM0.DDRPHY_ADR_DELAY3_P0_ADR0	0x800040070701103F	508
IOM0.DDRPHY_ADR_DELAY3_P0_ADR1	0x800044070701103F	542
IOM0.DDRPHY_ADR_DELAY3_P0_ADR2	0x800048070701103F	576
IOM0.DDRPHY_ADR_DELAY3_P0_ADR3	0x80004C070701103F	610
IOM0.DDRPHY_ADR_DELAY3_P1_ADR0	0x800040070701143F	509
IOM0.DDRPHY_ADR_DELAY3_P1_ADR1	0x800044070701143F	542
IOM0.DDRPHY_ADR_DELAY3_P1_ADR2	0x800048070701143F	576
IOM0.DDRPHY_ADR_DELAY3_P1_ADR3	0x80004C070701143F	610
IOM0.DDRPHY_ADR_DELAY3_P2_ADR0	0x800040070701183F	509
IOM0.DDRPHY_ADR_DELAY3_P2_ADR1	0x800044070701183F	543
IOM0.DDRPHY_ADR_DELAY3_P2_ADR2	0x800048070701183F	577
IOM0.DDRPHY_ADR_DELAY3_P2_ADR3	0x80004C070701183F	611
IOM0.DDRPHY_ADR_DELAY3_P3_ADR0	0x8000400707011C3F	510
IOM0.DDRPHY_ADR_DELAY3_P3_ADR1	0x8000440707011C3F	543
IOM0.DDRPHY_ADR_DELAY3_P3_ADR2	0x8000480707011C3F	577
IOM0.DDRPHY_ADR_DELAY3_P3_ADR3	0x80004C0707011C3F	611
IOM0.DDRPHY_ADR_DELAY4_P0_ADR0	0x800040080701103F	510
IOM0.DDRPHY_ADR_DELAY4_P0_ADR1	0x800044080701103F	544
IOM0.DDRPHY_ADR_DELAY4_P0_ADR2	0x800048080701103F	578
IOM0.DDRPHY_ADR_DELAY4_P0_ADR3	0x80004C080701103F	612
IOM0.DDRPHY_ADR_DELAY4_P1_ADR0	0x800040080701143F	510
IOM0.DDRPHY_ADR_DELAY4_P1_ADR1	0x800044080701143F	544
IOM0.DDRPHY_ADR_DELAY4_P1_ADR2	0x800048080701143F	578
IOM0.DDRPHY_ADR_DELAY4_P1_ADR3	0x80004C080701143F	612
IOM0.DDRPHY_ADR_DELAY4_P2_ADR0	0x800040080701183F	511
IOM0.DDRPHY_ADR_DELAY4_P2_ADR1	0x800044080701183F	544
IOM0.DDRPHY_ADR_DELAY4_P2_ADR2	0x800048080701183F	578
IOM0.DDRPHY_ADR_DELAY4_P2_ADR3	0x80004C080701183F	612
IOM0.DDRPHY_ADR_DELAY4_P3_ADR0	0x8000400807011C3F	511
IOM0.DDRPHY_ADR_DELAY4_P3_ADR1	0x8000440807011C3F	545
IOM0.DDRPHY_ADR_DELAY4_P3_ADR2	0x8000480807011C3F	579
IOM0.DDRPHY_ADR_DELAY4_P3_ADR3	0x80004C0807011C3F	613

Mnemonic	Address	Page
IOM0.DDRPHY_ADR_DELAY5_P0_ADR0	0x800040090701103F	512
IOM0.DDRPHY_ADR_DELAY5_P0_ADR1	0x800044090701103F	545
IOM0.DDRPHY_ADR_DELAY5_P0_ADR2	0x800048090701103F	579
IOM0.DDRPHY_ADR_DELAY5_P0_ADR3	0x80004C090701103F	613
IOM0.DDRPHY_ADR_DELAY5_P1_ADR0	0x800040090701143F	512
IOM0.DDRPHY_ADR_DELAY5_P1_ADR1	0x800044090701143F	546
IOM0.DDRPHY_ADR_DELAY5_P1_ADR2	0x800048090701143F	580
IOM0.DDRPHY_ADR_DELAY5_P1_ADR3	0x80004C090701143F	614
IOM0.DDRPHY_ADR_DELAY5_P2_ADR0	0x800040090701183F	512
IOM0.DDRPHY_ADR_DELAY5_P2_ADR1	0x800044090701183F	546
IOM0.DDRPHY_ADR_DELAY5_P2_ADR2	0x800048090701183F	580
IOM0.DDRPHY_ADR_DELAY5_P2_ADR3	0x80004C090701183F	614
IOM0.DDRPHY_ADR_DELAY5_P3_ADR0	0x8000400907011C3F	513
IOM0.DDRPHY_ADR_DELAY5_P3_ADR1	0x8000440907011C3F	546
IOM0.DDRPHY_ADR_DELAY5_P3_ADR2	0x8000480907011C3F	580
IOM0.DDRPHY_ADR_DELAY5_P3_ADR3	0x80004C0907011C3F	614
IOM0.DDRPHY_ADR_DELAY6_P0_ADR0	0x8000400A0701103F	513
IOM0.DDRPHY_ADR_DELAY6_P0_ADR1	0x8000440A0701103F	547
IOM0.DDRPHY_ADR_DELAY6_P0_ADR2	0x8000480A0701103F	581
IOM0.DDRPHY_ADR_DELAY6_P0_ADR3	0x80004C0A0701103F	615
IOM0.DDRPHY_ADR_DELAY6_P1_ADR0	0x8000400A0701143F	514
IOM0.DDRPHY_ADR_DELAY6_P1_ADR1	0x8000440A0701143F	547
IOM0.DDRPHY_ADR_DELAY6_P1_ADR2	0x8000480A0701143F	581
IOM0.DDRPHY_ADR_DELAY6_P1_ADR3	0x80004C0A0701143F	615
IOM0.DDRPHY_ADR_DELAY6_P2_ADR0	0x8000400A0701183F	514
IOM0.DDRPHY_ADR_DELAY6_P2_ADR1	0x8000440A0701183F	548
IOM0.DDRPHY_ADR_DELAY6_P2_ADR2	0x8000480A0701183F	582
IOM0.DDRPHY_ADR_DELAY6_P2_ADR3	0x80004C0A0701183F	616
IOM0.DDRPHY_ADR_DELAY6_P3_ADR0	0x8000400A07011C3F	514
IOM0.DDRPHY_ADR_DELAY6_P3_ADR1	0x8000440A07011C3F	548
IOM0.DDRPHY_ADR_DELAY6_P3_ADR2	0x8000480A07011C3F	582
IOM0.DDRPHY_ADR_DELAY6_P3_ADR3	0x80004C0A07011C3F	616
IOM0.DDRPHY_ADR_DELAY7_P0_ADR0	0x8000400B0701103F	515
IOM0.DDRPHY_ADR_DELAY7_P0_ADR1	0x8000440B0701103F	548
IOM0.DDRPHY_ADR_DELAY7_P0_ADR2	0x8000480B0701103F	582
IOM0.DDRPHY_ADR_DELAY7_P0_ADR3	0x80004C0B0701103F	616
IOM0.DDRPHY_ADR_DELAY7_P1_ADR0	0x8000400B0701143F	515
IOM0.DDRPHY_ADR_DELAY7_P1_ADR1	0x8000440B0701143F	549
IOM0.DDRPHY_ADR_DELAY7_P1_ADR2	0x8000480B0701143F	583
IOM0.DDRPHY_ADR_DELAY7_P1_ADR3	0x80004C0B0701143F	617
IOM0.DDRPHY_ADR_DELAY7_P2_ADR0	0x8000400B0701183F	516
IOM0.DDRPHY_ADR_DELAY7_P2_ADR1	0x8000440B0701183F	549
IOM0.DDRPHY_ADR_DELAY7_P2_ADR2	0x8000480B0701183F	583

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IOM0.DDRPHY_ADR_DELAY7_P2_ADR3	0x80004C0B0701183F	617
IOM0.DDRPHY_ADR_DELAY7_P3_ADR0	0x8000400B07011C3F	516
IOM0.DDRPHY_ADR_DELAY7_P3_ADR1	0x8000440B07011C3F	550
IOM0.DDRPHY_ADR_DELAY7_P3_ADR2	0x8000480B07011C3F	584
IOM0.DDRPHY_ADR_DELAY7_P3_ADR3	0x80004C0B07011C3F	618
IOM0.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P0_ADR0	0x8000400C0701103F	516
IOM0.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P0_ADR1	0x8000440C0701103F	550
IOM0.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P0_ADR2	0x8000480C0701103F	584
IOM0.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P0_ADR3	0x80004C0C0701103F	618
IOM0.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P1_ADR0	0x8000400C0701143F	517
IOM0.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P1_ADR1	0x8000440C0701143F	551
IOM0.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P1_ADR2	0x8000480C0701143F	585
IOM0.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P1_ADR3	0x80004C0C0701143F	619
IOM0.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P2_ADR0	0x8000400C0701183F	518
IOM0.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P2_ADR1	0x8000440C0701183F	552
IOM0.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P2_ADR2	0x8000480C0701183F	586
IOM0.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P2_ADR3	0x80004C0C0701183F	620
IOM0.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P3_ADR0	0x8000400C07011C3F	519
IOM0.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P3_ADR1	0x8000440C07011C3F	552
IOM0.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P3_ADR2	0x8000480C07011C3F	586
IOM0.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P3_ADR3	0x80004C0C07011C3F	620
IOM0.DDRPHY_ADR_DIFFPAIR_ENABLE_P0_ADR0	0x800040010701103F	501
IOM0.DDRPHY_ADR_DIFFPAIR_ENABLE_P0_ADR1	0x800044010701103F	534
IOM0.DDRPHY_ADR_DIFFPAIR_ENABLE_P0_ADR2	0x800048010701103F	568
IOM0.DDRPHY_ADR_DIFFPAIR_ENABLE_P0_ADR3	0x80004C010701103F	602
IOM0.DDRPHY_ADR_DIFFPAIR_ENABLE_P1_ADR0	0x800040010701143F	501
IOM0.DDRPHY_ADR_DIFFPAIR_ENABLE_P1_ADR1	0x800044010701143F	535
IOM0.DDRPHY_ADR_DIFFPAIR_ENABLE_P1_ADR2	0x800048010701143F	569
IOM0.DDRPHY_ADR_DIFFPAIR_ENABLE_P1_ADR3	0x80004C010701143F	603
IOM0.DDRPHY_ADR_DIFFPAIR_ENABLE_P2_ADR0	0x800040010701183F	502
IOM0.DDRPHY_ADR_DIFFPAIR_ENABLE_P2_ADR1	0x800044010701183F	536
IOM0.DDRPHY_ADR_DIFFPAIR_ENABLE_P2_ADR2	0x800048010701183F	570
IOM0.DDRPHY_ADR_DIFFPAIR_ENABLE_P2_ADR3	0x80004C010701183F	604
IOM0.DDRPHY_ADR_DIFFPAIR_ENABLE_P3_ADR0	0x8000400107011C3F	503
IOM0.DDRPHY_ADR_DIFFPAIR_ENABLE_P3_ADR1	0x8000440107011C3F	536
IOM0.DDRPHY_ADR_DIFFPAIR_ENABLE_P3_ADR2	0x8000480107011C3F	570
IOM0.DDRPHY_ADR_DIFFPAIR_ENABLE_P3_ADR3	0x80004C0107011C3F	604
IOM0.DDRPHY_ADR_DLL_CNTL_P0_ADR32S0	0x8000803A0701103F	662
IOM0.DDRPHY_ADR_DLL_CNTL_P0_ADR32S1	0x8000843A0701103F	702
IOM0.DDRPHY_ADR_DLL_CNTL_P1_ADR32S0	0x8000803A0701143F	663
IOM0.DDRPHY_ADR_DLL_CNTL_P1_ADR32S1	0x8000843A0701143F	703
IOM0.DDRPHY_ADR_DLL_CNTL_P2_ADR32S0	0x8000803A0701183F	664
IOM0.DDRPHY_ADR_DLL_CNTL_P2_ADR32S1	0x8000843A0701183F	704

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IOM0.DDRPHY_ADR_DLL_CNTL_P3_ADR32S0	0x8000803A07011C3F	665
IOM0.DDRPHY_ADR_DLL_CNTL_P3_ADR32S1	0x8000843A07011C3F	705
IOM0.DDRPHY_ADR_DLL_DAC_LOWER_P0_ADR32S0	0x8000803B0701103F	666
IOM0.DDRPHY_ADR_DLL_DAC_LOWER_P0_ADR32S1	0x8000843B0701103F	706
IOM0.DDRPHY_ADR_DLL_DAC_LOWER_P1_ADR32S0	0x8000803B0701143F	666
IOM0.DDRPHY_ADR_DLL_DAC_LOWER_P1_ADR32S1	0x8000843B0701143F	706
IOM0.DDRPHY_ADR_DLL_DAC_LOWER_P2_ADR32S0	0x8000803B0701183F	667
IOM0.DDRPHY_ADR_DLL_DAC_LOWER_P2_ADR32S1	0x8000843B0701183F	706
IOM0.DDRPHY_ADR_DLL_DAC_LOWER_P3_ADR32S0	0x8000803B07011C3F	667
IOM0.DDRPHY_ADR_DLL_DAC_LOWER_P3_ADR32S1	0x8000843B07011C3F	707
IOM0.DDRPHY_ADR_DLL_DAC_UPPER_P0_ADR32S0	0x8000803C0701103F	668
IOM0.DDRPHY_ADR_DLL_DAC_UPPER_P0_ADR32S1	0x8000843C0701103F	707
IOM0.DDRPHY_ADR_DLL_DAC_UPPER_P1_ADR32S0	0x8000803C0701143F	668
IOM0.DDRPHY_ADR_DLL_DAC_UPPER_P1_ADR32S1	0x8000843C0701143F	707
IOM0.DDRPHY_ADR_DLL_DAC_UPPER_P2_ADR32S0	0x8000803C0701183F	668
IOM0.DDRPHY_ADR_DLL_DAC_UPPER_P2_ADR32S1	0x8000843C0701183F	708
IOM0.DDRPHY_ADR_DLL_DAC_UPPER_P3_ADR32S0	0x8000803C07011C3F	668
IOM0.DDRPHY_ADR_DLL_DAC_UPPER_P3_ADR32S1	0x8000843C07011C3F	708
IOM0.DDRPHY_ADR_DLL_SLAVE_VREG_LOWER_P0_ADR32S0	0x8000802E0701103F	636
IOM0.DDRPHY_ADR_DLL_SLAVE_VREG_LOWER_P0_ADR32S1	0x8000842E0701103F	676
IOM0.DDRPHY_ADR_DLL_SLAVE_VREG_LOWER_P1_ADR32S0	0x8000802E0701143F	637
IOM0.DDRPHY_ADR_DLL_SLAVE_VREG_LOWER_P1_ADR32S1	0x8000842E0701143F	676
IOM0.DDRPHY_ADR_DLL_SLAVE_VREG_LOWER_P2_ADR32S0	0x8000802E0701183F	637
IOM0.DDRPHY_ADR_DLL_SLAVE_VREG_LOWER_P2_ADR32S1	0x8000842E0701183F	676
IOM0.DDRPHY_ADR_DLL_SLAVE_VREG_LOWER_P3_ADR32S0	0x8000802E07011C3F	637
IOM0.DDRPHY_ADR_DLL_SLAVE_VREG_LOWER_P3_ADR32S1	0x8000842E07011C3F	676
IOM0.DDRPHY_ADR_DLL_SLAVE_VREG_UPPER_P0_ADR32S0	0x8000802F0701103F	637
IOM0.DDRPHY_ADR_DLL_SLAVE_VREG_UPPER_P0_ADR32S1	0x8000842F0701103F	677
IOM0.DDRPHY_ADR_DLL_SLAVE_VREG_UPPER_P1_ADR32S0	0x8000802F0701143F	638
IOM0.DDRPHY_ADR_DLL_SLAVE_VREG_UPPER_P1_ADR32S1	0x8000842F0701143F	677
IOM0.DDRPHY_ADR_DLL_SLAVE_VREG_UPPER_P2_ADR32S0	0x8000802F0701183F	638
IOM0.DDRPHY_ADR_DLL_SLAVE_VREG_UPPER_P2_ADR32S1	0x8000842F0701183F	677
IOM0.DDRPHY_ADR_DLL_SLAVE_VREG_UPPER_P3_ADR32S0	0x8000802F07011C3F	638
IOM0.DDRPHY_ADR_DLL_SLAVE_VREG_UPPER_P3_ADR32S1	0x8000842F07011C3F	678
IOM0.DDRPHY_ADR_DLL_SW_CONTROL_0_P0_ADR32S0	0x800080300701103F	639
IOM0.DDRPHY_ADR_DLL_SW_CONTROL_0_P0_ADR32S1	0x800084300701103F	678
IOM0.DDRPHY_ADR_DLL_SW_CONTROL_0_P1_ADR32S0	0x800080300701143F	640
IOM0.DDRPHY_ADR_DLL_SW_CONTROL_0_P1_ADR32S1	0x800084300701143F	679
IOM0.DDRPHY_ADR_DLL_SW_CONTROL_0_P2_ADR32S0	0x800080300701183F	641
IOM0.DDRPHY_ADR_DLL_SW_CONTROL_0_P2_ADR32S1	0x800084300701183F	680
IOM0.DDRPHY_ADR_DLL_SW_CONTROL_0_P3_ADR32S0	0x8000803007011C3F	642
IOM0.DDRPHY_ADR_DLL_SW_CONTROL_0_P3_ADR32S1	0x8000843007011C3F	681
IOM0.DDRPHY_ADR_DLL_SW_CONTROL_1_P0_ADR32S0	0x8000802D0701103F	634

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IOM0.DDRPHY_ADR_DLL_SW_CONTROL_1_P0_ADR32S1	0x8000842D0701103F	673
IOM0.DDRPHY_ADR_DLL_SW_CONTROL_1_P1_ADR32S0	0x8000802D0701143F	635
IOM0.DDRPHY_ADR_DLL_SW_CONTROL_1_P1_ADR32S1	0x8000842D0701143F	674
IOM0.DDRPHY_ADR_DLL_SW_CONTROL_1_P2_ADR32S0	0x8000802D0701183F	635
IOM0.DDRPHY_ADR_DLL_SW_CONTROL_1_P2_ADR32S1	0x8000842D0701183F	674
IOM0.DDRPHY_ADR_DLL_SW_CONTROL_1_P3_ADR32S0	0x8000802D07011C3F	636
IOM0.DDRPHY_ADR_DLL_SW_CONTROL_1_P3_ADR32S1	0x8000842D07011C3F	675
IOM0.DDRPHY_ADR_DLL_VREG_COARSE_P0_ADR32S0	0x8000803E0701103F	671
IOM0.DDRPHY_ADR_DLL_VREG_COARSE_P0_ADR32S1	0x8000843E0701103F	711
IOM0.DDRPHY_ADR_DLL_VREG_COARSE_P1_ADR32S0	0x8000803E0701143F	672
IOM0.DDRPHY_ADR_DLL_VREG_COARSE_P1_ADR32S1	0x8000843E0701143F	711
IOM0.DDRPHY_ADR_DLL_VREG_COARSE_P2_ADR32S0	0x8000803E0701183F	672
IOM0.DDRPHY_ADR_DLL_VREG_COARSE_P2_ADR32S1	0x8000843E0701183F	712
IOM0.DDRPHY_ADR_DLL_VREG_COARSE_P3_ADR32S0	0x8000803E07011C3F	673
IOM0.DDRPHY_ADR_DLL_VREG_COARSE_P3_ADR32S1	0x8000843E07011C3F	712
IOM0.DDRPHY_ADR_DLL_VREG_CONFIG_1_P0_ADR32S0	0x800080310701103F	643
IOM0.DDRPHY_ADR_DLL_VREG_CONFIG_1_P0_ADR32S1	0x800084310701103F	682
IOM0.DDRPHY_ADR_DLL_VREG_CONFIG_1_P1_ADR32S0	0x800080310701143F	643
IOM0.DDRPHY_ADR_DLL_VREG_CONFIG_1_P1_ADR32S1	0x800084310701143F	683
IOM0.DDRPHY_ADR_DLL_VREG_CONFIG_1_P2_ADR32S0	0x800080310701183F	644
IOM0.DDRPHY_ADR_DLL_VREG_CONFIG_1_P2_ADR32S1	0x800084310701183F	683
IOM0.DDRPHY_ADR_DLL_VREG_CONFIG_1_P3_ADR32S0	0x8000803107011C3F	644
IOM0.DDRPHY_ADR_DLL_VREG_CONFIG_1_P3_ADR32S1	0x8000843107011C3F	684
IOM0.DDRPHY_ADR_DLL_VREG_CONTROL_P0_ADR32S0	0x8000803D0701103F	669
IOM0.DDRPHY_ADR_DLL_VREG_CONTROL_P0_ADR32S1	0x8000843D0701103F	708
IOM0.DDRPHY_ADR_DLL_VREG_CONTROL_P1_ADR32S0	0x8000803D0701143F	669
IOM0.DDRPHY_ADR_DLL_VREG_CONTROL_P1_ADR32S1	0x8000843D0701143F	709
IOM0.DDRPHY_ADR_DLL_VREG_CONTROL_P2_ADR32S0	0x8000803D0701183F	670
IOM0.DDRPHY_ADR_DLL_VREG_CONTROL_P2_ADR32S1	0x8000843D0701183F	710
IOM0.DDRPHY_ADR_DLL_VREG_CONTROL_P3_ADR32S0	0x8000803D07011C3F	671
IOM0.DDRPHY_ADR_DLL_VREG_CONTROL_P3_ADR32S1	0x8000843D07011C3F	710
IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P0_ADR0	0x800040200701103F	519
IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P0_ADR1	0x800044200701103F	553
IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P0_ADR2	0x800048200701103F	587
IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P0_ADR3	0x80004C200701103F	621
IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P1_ADR0	0x800040200701143F	521
IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P1_ADR1	0x800044200701143F	554
IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P1_ADR2	0x800048200701143F	588
IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P1_ADR3	0x80004C200701143F	622
IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P2_ADR0	0x800040200701183F	522
IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P2_ADR1	0x800044200701183F	555
IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P2_ADR2	0x800048200701183F	589
IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P2_ADR3	0x80004C200701183F	623

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IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P3_ADR0	0x8000402007011C3F	523
IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P3_ADR1	0x8000442007011C3F	556
IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P3_ADR2	0x8000482007011C3F	590
IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P3_ADR3	0x80004C2007011C3F	624
IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P0_ADR0	0x800040210701103F	524
IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P0_ADR1	0x800044210701103F	558
IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P0_ADR2	0x800048210701103F	592
IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P0_ADR3	0x80004C210701103F	626
IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P1_ADR0	0x800040210701143F	525
IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P1_ADR1	0x800044210701143F	559
IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P1_ADR2	0x800048210701143F	593
IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P1_ADR3	0x80004C210701143F	627
IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P2_ADR0	0x800040210701183F	526
IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P2_ADR1	0x800044210701183F	560
IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P2_ADR2	0x800048210701183F	594
IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P2_ADR3	0x80004C210701183F	628
IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P3_ADR0	0x8000402107011C3F	527
IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P3_ADR1	0x8000442107011C3F	561
IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P3_ADR2	0x8000482107011C3F	595
IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P3_ADR3	0x80004C2107011C3F	629
IOM0.DDRPHY_ADR_MCCLK_WRCLK_PR_STATIC_OFFSET_P0_ADR32S0	0x800080330701103F	650
IOM0.DDRPHY_ADR_MCCLK_WRCLK_PR_STATIC_OFFSET_P0_ADR32S1	0x800084330701103F	690
IOM0.DDRPHY_ADR_MCCLK_WRCLK_PR_STATIC_OFFSET_P1_ADR32S0	0x800080330701143F	651
IOM0.DDRPHY_ADR_MCCLK_WRCLK_PR_STATIC_OFFSET_P1_ADR32S1	0x800084330701143F	690
IOM0.DDRPHY_ADR_MCCLK_WRCLK_PR_STATIC_OFFSET_P2_ADR32S0	0x800080330701183F	651
IOM0.DDRPHY_ADR_MCCLK_WRCLK_PR_STATIC_OFFSET_P2_ADR32S1	0x800084330701183F	690
IOM0.DDRPHY_ADR_MCCLK_WRCLK_PR_STATIC_OFFSET_P3_ADR32S0	0x8000803307011C3F	651
IOM0.DDRPHY_ADR_MCCLK_WRCLK_PR_STATIC_OFFSET_P3_ADR32S1	0x8000843307011C3F	691
IOM0.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE0_P0_ADR32S0	0x800080360701103F	656
IOM0.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE0_P0_ADR32S1	0x800084360701103F	695
IOM0.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE0_P1_ADR32S0	0x800080360701143F	656
IOM0.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE0_P1_ADR32S1	0x800084360701143F	696
IOM0.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE0_P2_ADR32S0	0x800080360701183F	656
IOM0.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE0_P2_ADR32S1	0x800084360701183F	696
IOM0.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE0_P3_ADR32S0	0x8000803607011C3F	657
IOM0.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE0_P3_ADR32S1	0x8000843607011C3F	696
IOM0.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE1_P0_ADR32S0	0x800080370701103F	657
IOM0.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE1_P0_ADR32S1	0x800084370701103F	696
IOM0.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE1_P1_ADR32S0	0x800080370701143F	657
IOM0.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE1_P1_ADR32S1	0x800084370701143F	697
IOM0.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE1_P2_ADR32S0	0x800080370701183F	658
IOM0.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE1_P2_ADR32S1	0x800084370701183F	697
IOM0.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE1_P3_ADR32S0	0x8000803707011C3F	658

Mnemonic	Address	Page
IOM0.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE1_P3_ADR32S1	0x8000843707011C3F	697
IOM0.DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR32S0	0x800080350701103F	654
IOM0.DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR32S1	0x800084350701103F	693
IOM0.DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR32S0	0x800080350701143F	654
IOM0.DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR32S1	0x800084350701143F	694
IOM0.DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P2_ADR32S0	0x800080350701183F	655
IOM0.DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P2_ADR32S1	0x800084350701183F	694
IOM0.DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P3_ADR32S0	0x8000803507011C3F	655
IOM0.DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P3_ADR32S1	0x8000843507011C3F	695
IOM0.DDRPHY_ADR_POWERDOWN_2_P0_ADR0	0x8000402C0701103F	530
IOM0.DDRPHY_ADR_POWERDOWN_2_P0_ADR1	0x8000442C0701103F	564
IOM0.DDRPHY_ADR_POWERDOWN_2_P0_ADR2	0x8000482C0701103F	598
IOM0.DDRPHY_ADR_POWERDOWN_2_P0_ADR3	0x80004C2C0701103F	632
IOM0.DDRPHY_ADR_POWERDOWN_2_P1_ADR0	0x8000402C0701143F	531
IOM0.DDRPHY_ADR_POWERDOWN_2_P1_ADR1	0x8000442C0701143F	565
IOM0.DDRPHY_ADR_POWERDOWN_2_P1_ADR2	0x8000482C0701143F	599
IOM0.DDRPHY_ADR_POWERDOWN_2_P1_ADR3	0x80004C2C0701143F	633
IOM0.DDRPHY_ADR_POWERDOWN_2_P2_ADR0	0x8000402C0701183F	531
IOM0.DDRPHY_ADR_POWERDOWN_2_P2_ADR1	0x8000442C0701183F	565
IOM0.DDRPHY_ADR_POWERDOWN_2_P2_ADR2	0x8000482C0701183F	599
IOM0.DDRPHY_ADR_POWERDOWN_2_P2_ADR3	0x80004C2C0701183F	633
IOM0.DDRPHY_ADR_POWERDOWN_2_P3_ADR0	0x8000402C07011C3F	532
IOM0.DDRPHY_ADR_POWERDOWN_2_P3_ADR1	0x8000442C07011C3F	566
IOM0.DDRPHY_ADR_POWERDOWN_2_P3_ADR2	0x8000482C07011C3F	600
IOM0.DDRPHY_ADR_POWERDOWN_2_P3_ADR3	0x80004C2C07011C3F	634
IOM0.DDRPHY_ADR_RESERVED10_P0_ADR0	0x8000402A0701103F	528
IOM0.DDRPHY_ADR_RESERVED10_P0_ADR1	0x8000442A0701103F	562
IOM0.DDRPHY_ADR_RESERVED10_P0_ADR2	0x8000482A0701103F	596
IOM0.DDRPHY_ADR_RESERVED10_P0_ADR3	0x80004C2A0701103F	630
IOM0.DDRPHY_ADR_RESERVED10_P1_ADR0	0x8000402A0701143F	528
IOM0.DDRPHY_ADR_RESERVED10_P1_ADR1	0x8000442A0701143F	562
IOM0.DDRPHY_ADR_RESERVED10_P1_ADR2	0x8000482A0701143F	596
IOM0.DDRPHY_ADR_RESERVED10_P1_ADR3	0x80004C2A0701143F	630
IOM0.DDRPHY_ADR_RESERVED10_P2_ADR0	0x8000402A0701183F	529
IOM0.DDRPHY_ADR_RESERVED10_P2_ADR1	0x8000442A0701183F	563
IOM0.DDRPHY_ADR_RESERVED10_P2_ADR2	0x8000482A0701183F	597
IOM0.DDRPHY_ADR_RESERVED10_P2_ADR3	0x80004C2A0701183F	631
IOM0.DDRPHY_ADR_RESERVED10_P3_ADR0	0x8000402A07011C3F	529
IOM0.DDRPHY_ADR_RESERVED10_P3_ADR1	0x8000442A07011C3F	563
IOM0.DDRPHY_ADR_RESERVED10_P3_ADR2	0x8000482A07011C3F	597
IOM0.DDRPHY_ADR_RESERVED10_P3_ADR3	0x80004C2A07011C3F	631
IOM0.DDRPHY_ADR_RESERVED11_P0_ADR0	0x8000402B0701103F	529
IOM0.DDRPHY_ADR_RESERVED11_P0_ADR1	0x8000442B0701103F	563

Mnemonic	Address	Page
IOM0.DDRPHY_ADR_RESERVED11_P0_ADR2	0x8000482B0701103F	597
IOM0.DDRPHY_ADR_RESERVED11_P0_ADR3	0x80004C2B0701103F	631
IOM0.DDRPHY_ADR_RESERVED11_P1_ADR0	0x8000402B0701143F	529
IOM0.DDRPHY_ADR_RESERVED11_P1_ADR1	0x8000442B0701143F	563
IOM0.DDRPHY_ADR_RESERVED11_P1_ADR2	0x8000482B0701143F	597
IOM0.DDRPHY_ADR_RESERVED11_P1_ADR3	0x80004C2B0701143F	631
IOM0.DDRPHY_ADR_RESERVED11_P2_ADR0	0x8000402B0701183F	530
IOM0.DDRPHY_ADR_RESERVED11_P2_ADR1	0x8000442B0701183F	564
IOM0.DDRPHY_ADR_RESERVED11_P2_ADR2	0x8000482B0701183F	598
IOM0.DDRPHY_ADR_RESERVED11_P2_ADR3	0x80004C2B0701183F	632
IOM0.DDRPHY_ADR_RESERVED11_P3_ADR0	0x8000402B07011C3F	530
IOM0.DDRPHY_ADR_RESERVED11_P3_ADR1	0x8000442B07011C3F	564
IOM0.DDRPHY_ADR_RESERVED11_P3_ADR2	0x8000482B07011C3F	598
IOM0.DDRPHY_ADR_RESERVED11_P3_ADR3	0x80004C2B07011C3F	632
IOM0.DDRPHY_ADR_RESERVED2_P0_ADR32S0	0x800080390701103F	661
IOM0.DDRPHY_ADR_RESERVED2_P0_ADR32S1	0x800084390701103F	701
IOM0.DDRPHY_ADR_RESERVED2_P1_ADR32S0	0x800080390701143F	661
IOM0.DDRPHY_ADR_RESERVED2_P1_ADR32S1	0x800084390701143F	701
IOM0.DDRPHY_ADR_RESERVED2_P2_ADR32S0	0x800080390701183F	662
IOM0.DDRPHY_ADR_RESERVED2_P2_ADR32S1	0x800084390701183F	701
IOM0.DDRPHY_ADR_RESERVED2_P3_ADR32S0	0x8000803907011C3F	662
IOM0.DDRPHY_ADR_RESERVED2_P3_ADR32S1	0x8000843907011C3F	701
IOM0.DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR32S0	0x800080320701103F	645
IOM0.DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR32S1	0x800084320701103F	684
IOM0.DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR32S0	0x800080320701143F	646
IOM0.DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR32S1	0x800084320701143F	686
IOM0.DDRPHY_ADR_SYSCLK_CNTL_PR_P2_ADR32S0	0x800080320701183F	648
IOM0.DDRPHY_ADR_SYSCLK_CNTL_PR_P2_ADR32S1	0x800084320701183F	687
IOM0.DDRPHY_ADR_SYSCLK_CNTL_PR_P3_ADR32S0	0x8000803207011C3F	649
IOM0.DDRPHY_ADR_SYSCLK_CNTL_PR_P3_ADR32S1	0x8000843207011C3F	688
IOM0.DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P0_ADR32S0	0x800080340701103F	652
IOM0.DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P0_ADR32S1	0x800084340701103F	691
IOM0.DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P1_ADR32S0	0x800080340701143F	652
IOM0.DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P1_ADR32S1	0x800084340701143F	692
IOM0.DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P2_ADR32S0	0x800080340701183F	653
IOM0.DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P2_ADR32S1	0x800084340701183F	692
IOM0.DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P3_ADR32S0	0x8000803407011C3F	653
IOM0.DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P3_ADR32S1	0x8000843407011C3F	693

The DDRPHY ADDR path registers are listed in the following tables.

Register Name	ADR Bit Enable Register
Mnemonic	IOM0.DDRPHY_ADR_BIT_ENABLE_P0_ADR0
Address	800040000701103F (SCOM)
Description	An ADR12 has 12 possible outputs, and an ADR8 has 8 possible outputs. This register is used to enable and disable each of the 12 pins or 8 pins. Any pins used on an ADR must be enabled via this register. The pins on an ADR can be used to send clocks or control (command, address, and so on) signals to memory devices.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:59	RW	BIT_ENABLE_0_11: 1 = Indicates that the ADR bit is enabled and is used for sending clocks or control (command, address, and so on) signals to the memory device. 0 = Indicates that the ADR bit is not used and not enabled. Bit 0 controls MEMINTC00O(n). Bit 1 controls MEMINTC01O(n). Bit 2 controls MEMINTC02O(n). ... Bit 11 controls MEMINTC11O(n). where n is the ADR instance number. ADR12 uses bits 48:59. ADR8 uses bits 48:55, with bits 56:59 reserved.
60:63	RW	Reserved.

Register Name	ADR Bit Enable Register
Mnemonic	IOM0.DDRPHY_ADR_BIT_ENABLE_P1_ADR0
Address	800040000701143F (SCOM)
Description	An ADR12 has 12 possible outputs, and an ADR8 has 8 possible outputs. This register is used to enable and disable each of the 12 pins or 8 pins. Any pins used on an ADR must be enabled via this register. The pins on an ADR can be used to send clocks or control (command, address, and so on) signals to memory devices.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:59	RW	BIT_ENABLE_0_11: 1 = Indicates that the ADR bit is enabled and is used for sending clocks or control (command, address, and so on) signals to the memory device. 0 = Indicates that the ADR bit is not used and not enabled. Bit 0 controls MEMINTC00O(n). Bit 1 controls MEMINTC01O(n). Bit 2 controls MEMINTC02O(n). ... Bit 11 controls MEMINTC11O(n). where n is the ADR instance number. ADR12 uses bits 48:59. ADR8 uses bits 48:55, with bits 56:59 reserved.
60:63	RW	Reserved.

Register Name	ADR Bit Enable Register
Mnemonic	IOM0.DDRPHY_ADR_BIT_ENABLE_P2_ADR0
Address	800040000701183F (SCOM)
Description	An ADR12 has 12 possible outputs, and an ADR8 has 8 possible outputs. This register is used to enable and disable each of the 12 pins or 8 pins. Any pins used on an ADR must be enabled via this register. The pins on an ADR can be used to send clocks or control (command, address, and so on) signals to memory devices.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:59	RW	BIT_ENABLE_0_11: 1 = Indicates that the ADR bit is enabled and is used for sending clocks or control (command, address, and so on) signals to the memory device. 0 = Indicates that the ADR bit is not used and not enabled. Bit 0 controls MEMINTC00O(n). Bit 1 controls MEMINTC01O(n). Bit 2 controls MEMINTC02O(n). ... Bit 11 controls MEMINTC11O(n). where n is the ADR instance number. ADR12 uses bits 48:59. ADR8 uses bits 48:55, with bits 56:59 reserved.
60:63	RW	Reserved.

Register Name	ADR Bit Enable Register
Mnemonic	IOM0.DDRPHY_ADR_BIT_ENABLE_P3_ADR0
Address	8000400007011C3F (SCOM)
Description	An ADR12 has 12 possible outputs, and an ADR8 has 8 possible outputs. This register is used to enable and disable each of the 12 pins or 8 pins. Any pins used on an ADR must be enabled via this register. The pins on an ADR can be used to send clocks or control (command, address, and so on) signals to memory devices.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:59	RW	BIT_ENABLE_0_11: 1 = Indicates that the ADR bit is enabled and is used for sending clocks or control (command, address, and so on) signals to the memory device. 0 = Indicates that the ADR bit is not used and not enabled. Bit 0 controls MEMINTC00O(n). Bit 1 controls MEMINTC01O(n). Bit 2 controls MEMINTC02O(n). ... Bit 11 controls MEMINTC11O(n). where n is the ADR instance number. ADR12 uses bits 48:59. ADR8 uses bits 48:55, with bits 56:59 reserved.
60:63	RW	Reserved.

Register Name	ADR Differential Pair Enable Register
Mnemonic	IOM0.DDRPHY_ADR_DIFFPAIR_ENABLE_P0_ADR0
Address	800040010701103F (SCOM)
Description	An ADR12 has 12 possible outputs, and an ADR8 has 8 possible outputs, any of which can be paired together for memory clock generation (CK/CK#). This register is used to enable or disable each pair of ADR pins to be used as differential outputs or as two single-ended outputs. When a pair of ADR pins is configured as a differential output, the delays associated with both outputs of the differential pair must be programmed to the same value in the ADR Delay Value {0-7} Registers for that pair. When a pair of ADR pins is enabled as a differential pair in this register, both of the pins must be enabled in the ADR Bit Enable Register. When a pair of ADR pins is enabled as a differential pair in this register, the even-numbered pin is the true, and the odd-numbered pin is the complement signal.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	DI_ADR0_ADR1: 0 = Lanes 0 and 1 are not a differential clock pair. 1 = Lanes 0 and 1 are a differential clock pair.
49	RW	DI_ADR2_ADR3: 0 = Lanes 2 and 3 are not a differential clock pair. 1 = Lanes 2 and 3 are a differential clock pair.
50	RW	DI_ADR4_ADR5: 0 = Lanes 4 and 5 are not a differential clock pair. 1 = Lanes 4 and 5 are a differential clock pair.
51	RW	DI_ADR6_ADR7: 0 = Lanes 6 and 7 are not a differential clock pair. 1 = Lanes 6 and 7 are a differential clock pair.
52	RW	DI_ADR8_ADR9: 0 = Lanes 8 and 9 are not a differential clock pair. 1 = Lanes 8 and 9 are a differential clock pair. Reserved for ADR8.
53	RW	DI_ADR10_ADR11: 0 = Lanes 10 and 11 are not a differential clock pair. 1 = Lanes 10 and 11 are a differential clock pair. Reserved for ADR8.
54:63	RW	Reserved.

Register Name	ADR Differential Pair Enable Register
Mnemonic	IOM0.DDRPHY_ADR_DIFFPAIR_ENABLE_P1_ADR0
Address	800040010701143F (SCOM)
Description	An ADR12 has 12 possible outputs, and an ADR8 has 8 possible outputs, any of which can be paired together for memory clock generation (CK/CK#). This register is used to enable or disable each pair of ADR pins to be used as differential outputs or as two single-ended outputs. When a pair of ADR pins is configured as a differential output, the delays associated with both outputs of the differential pair must be programmed to the same value in the ADR Delay Value {0-7} Registers for that pair. When a pair of ADR pins is enabled as a differential pair in this register, both of the pins must be enabled in the ADR Bit Enable Register. When a pair of ADR pins is enabled as a differential pair in this register, the even-numbered pin is the true, and the odd-numbered pin is the complement signal.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	DI_ADR0_ADR1: 0 = Lanes 0 and 1 are not a differential clock pair. 1 = Lanes 0 and 1 are a differential clock pair.
49	RW	DI_ADR2_ADR3: 0 = Lanes 2 and 3 are not a differential clock pair. 1 = Lanes 2 and 3 are a differential clock pair.
50	RW	DI_ADR4_ADR5: 0 = Lanes 4 and 5 are not a differential clock pair. 1 = Lanes 4 and 5 are a differential clock pair.
51	RW	DI_ADR6_ADR7: 0 = Lanes 6 and 7 are not a differential clock pair. 1 = Lanes 6 and 7 are a differential clock pair.
52	RW	DI_ADR8_ADR9: 0 = Lanes 8 and 9 are not a differential clock pair. 1 = Lanes 8 and 9 are a differential clock pair. Reserved for ADR8.
53	RW	DI_ADR10_ADR11: 0 = Lanes 10 and 11 are not a differential clock pair. 1 = Lanes 10 and 11 are a differential clock pair. Reserved for ADR8.
54:63	RW	Reserved.

Register Name	**ADR Differential Pair Enable Register**
Mnemonic	IOM0.DDRPHY_ADR_DIFFPAIR_ENABLE_P2_ADR0
Address	800040010701183F (SCOM)
Description	An ADR12 has 12 possible outputs, and an ADR8 has 8 possible outputs, any of which can be paired together for memory clock generation (CK/CK#). This register is used to enable or disable each pair of ADR pins to be used as differential outputs or as two single-ended outputs. When a pair of ADR pins is configured as a differential output, the delays associated with both outputs of the differential pair must be programmed to the same value in the ADR Delay Value {0-7} Registers for that pair. When a pair of ADR pins is enabled as a differential pair in this register, both of the pins must be enabled in the ADR Bit Enable Register. When a pair of ADR pins is enabled as a differential pair in this register, the even-numbered pin is the true, and the odd-numbered pin is the complement signal.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	DI_ADR0_ADR1: 0 = Lanes 0 and 1 are not a differential clock pair. 1 = Lanes 0 and 1 are a differential clock pair.
49	RW	DI_ADR2_ADR3: 0 = Lanes 2 and 3 are not a differential clock pair. 1 = Lanes 2 and 3 are a differential clock pair.
50	RW	DI_ADR4_ADR5: 0 = Lanes 4 and 5 are not a differential clock pair. 1 = Lanes 4 and 5 are a differential clock pair.
51	RW	DI_ADR6_ADR7: 0 = Lanes 6 and 7 are not a differential clock pair. 1 = Lanes 6 and 7 are a differential clock pair.

Bits	SCOM	Field Mnemonic: Description
52	RW	DI_ADR8_ADR9: 0 = Lanes 8 and 9 are not a differential clock pair. 1 = Lanes 8 and 9 are a differential clock pair. Reserved for ADR8.
53	RW	DI_ADR10_ADR11: 0 = Lanes 10 and 11 are not a differential clock pair. 1 = Lanes 10 and 11 are a differential clock pair. Reserved for ADR8.
54:63	RW	Reserved.

Register Name	ADR Differential Pair Enable Register
Mnemonic	IOM0.DDRPHY_ADR_DIFFPAIR_ENABLE_P3_ADR0
Address	8000400107011C3F (SCOM)
Description	An ADR12 has 12 possible outputs, and an ADR8 has 8 possible outputs, any of which can be paired together for memory clock generation (CK/CK#). This register is used to enable or disable each pair of ADR pins to be used as differential outputs or as two single-ended outputs. When a pair of ADR pins is configured as a differential output, the delays associated with both outputs of the differential pair must be programmed to the same value in the ADR Delay Value {0-7} Registers for that pair. When a pair of ADR pins is enabled as a differential pair in this register, both of the pins must be enabled in the ADR Bit Enable Register. When a pair of ADR pins is enabled as a differential pair in this register, the even-numbered pin is the true, and the odd-numbered pin is the complement signal.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	DI_ADR0_ADR1: 0 = Lanes 0 and 1 are not a differential clock pair. 1 = Lanes 0 and 1 are a differential clock pair.
49	RW	DI_ADR2_ADR3: 0 = Lanes 2 and 3 are not a differential clock pair. 1 = Lanes 2 and 3 are a differential clock pair.
50	RW	DI_ADR4_ADR5: 0 = Lanes 4 and 5 are not a differential clock pair. 1 = Lanes 4 and 5 are a differential clock pair.
51	RW	DI_ADR6_ADR7: 0 = Lanes 6 and 7 are not a differential clock pair. 1 = Lanes 6 and 7 are a differential clock pair.
52	RW	DI_ADR8_ADR9: 0 = Lanes 8 and 9 are not a differential clock pair. 1 = Lanes 8 and 9 are a differential clock pair. Reserved for ADR8.
53	RW	DI_ADR10_ADR11: 0 = Lanes 10 and 11 are not a differential clock pair. 1 = Lanes 10 and 11 are a differential clock pair. Reserved for ADR8.
54:63	RW	Reserved.

Register Name	ADR Delay Value 0 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY0_P0_ADR0
Address	800040040701103F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY0: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY1: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 0 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY0_P1_ADR0
Address	800040040701143F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY0: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY1: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 0 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY0_P2_ADR0
Address	800040040701183F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY0: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY1: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 0 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY0_P3_ADR0
Address	8000400407011C3F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY0: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY1: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 1 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY1_P0_ADR0
Address	800040050701103F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY2: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY3: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 1 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY1_P1_ADR0
Address	800040050701143F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY2: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY3: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 1 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY1_P2_ADR0
Address	800040050701183F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY2: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY3: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 1 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY1_P3_ADR0
Address	8000400507011C3F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY2: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY3: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 2 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY2_P0_ADR0
Address	800040060701103F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY4: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY5: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 2 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY2_P1_ADR0
Address	800040060701143F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY4: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY5: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 2 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY2_P2_ADR0
Address	800040060701183F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY4: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY5: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 2 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY2_P3_ADR0
Address	8000400607011C3F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY4: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY5: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 3 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY3_P0_ADR0
Address	800040070701103F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY6: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY7: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 3 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY3_P1_ADR0
Address	800040070701143F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY6: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY7: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 3 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY3_P2_ADR0
Address	800040070701183F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY6: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY7: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 3 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY3_P3_ADR0
Address	8000400707011C3F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY6: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY7: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 4 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY4_P0_ADR0
Address	800040080701103F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY8: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY9: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 4 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY4_P1_ADR0
Address	800040080701143F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY8: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY9: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 4 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY4_P2_ADR0
Address	800040080701183F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY8: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY9: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 4 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY4_P3_ADR0
Address	8000400807011C3F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY8: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY9: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 5 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY5_P0_ADR0
Address	800040090701103F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY10: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY11: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 5 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY5_P1_ADR0
Address	800040090701143F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY10: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY11: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 5 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY5_P2_ADR0
Address	800040090701183F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY10: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY11: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 5 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY5_P3_ADR0
Address	8000400907011C3F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY10: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY11: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 6 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY6_P0_ADR0
Address	8000400A0701103F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY12: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY13: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 6 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY6_P1_ADR0
Address	8000400A0701143F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY12: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY13: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 6 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY6_P2_ADR0
Address	8000400A0701183F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY12: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY13: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 6 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY6_P3_ADR0
Address	8000400A07011C3F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY12: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY13: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 7 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY7_P0_ADR0
Address	8000400B0701103F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY14: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY15: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 7 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY7_P1_ADR0
Address	8000400B0701143F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY14: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY15: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 7 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY7_P2_ADR0
Address	8000400B0701183F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY14: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY15: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 7 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY7_P3_ADR0
Address	8000400B07011C3F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY14: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY15: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR DFT Wrap Status and Control Register
Mnemonic	IOM0.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P0_ADR0
Address	8000400C0701103F (SCOM)
Description	This register provides the status and control of the ADR wrap test for a given ADR8/12 instance. This register must only be used to perform diagnostic, manufacturing, or characterization testing. Contact your IBM representative before modifying this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	ROX	ADR_TEST_LANE_PAIR_FAIL: **Note:** Bits 48:55 of this register are read only. These bits can be reset, but they are written with a free running dphy_gckn clock. Therefore, any read of these bits returns the value from the loopback test logic. If that logic has not been reset and the error bits are cleared, this field is X. Reading this register does not automatically clear these bits. When set, these bits must be reset by asserting bit 62 of this register. For PRBS7 error detection in the memory-clock domain: Bit 0 represents the miscompare detect for wrap0 and wrap1. Bit 1 represents the miscompare detect for wrap2 and wrap3. Bit 2 represents the miscompare detect for wrap4 and wrap5. Bit 3 represents the miscompare detect for wrap6 and wrap7. Bit 4 represents the miscompare detect for wrap8 and wrap9. Reserved for ADR8. Bit 5 represents the miscompare detect for wrap10 and wrap11. Reserved for ADR8.
54:55	ROX	Reserved.
56	RW	ADR_TEST_DATA_EN: When high, this bit selects macro test data. Otherwise, functional mode is used.
57:58	RW	ADR_TEST_MODE: These bits are reserved for manufacturing test.
59	RW	ADR_TEST_4TO1_MODE: When active, the pseudo-random binary sequence (PRBS) generates a 4-bit output every cycle. Otherwise, it outputs two bits. This signal is in the memory-clock domain.
60	RW	ADR_TEST_RESET: Reset. This signal is in the memory-clock domain.
61	RW	ADR_TEST_GEN_EN: Pattern generator enable. This signal is in the memory-clock domain. This signal must be active before enabling the check_enable_i; which is 8 cycles for loading the checker plus the latency between the generator and the wrap through APIN.
62	RW	ADR_TEST_CLEAR_ERROR: Clear error bits. This signal is in the memory-clock domain. The generator must be active before clr_error_i, and the macrotest_mode_i must be selecting WRAP clocks to all the corresponding checkers' latches.
63	RW	ADR_TEST_CHECK_EN: Enable the pattern checker. This signal is in the memory-clock domain. When active, the checker performs a PRBS7 sequence check on the corresponding WRAP channel.

Register Name	**ADR DFT Wrap Status and Control Register**
Mnemonic	IOM0.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P1_ADR0
Address	8000400C0701143F (SCOM)
Description	This register provides the status and control of the ADR wrap test for a given ADR8/12 instance. This register must only be used to perform diagnostic, manufacturing, or characterization testing. Contact your IBM representative before modifying this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:53	ROX	ADR_TEST_LANE_PAIR_FAIL: **Note:** Bits 48:55 of this register are read only. These bits can be reset, but they are written with a free running dphy_gckn clock. Therefore, any read of these bits returns the value from the loopback test logic. If that logic has not been reset and the error bits are cleared, this field is X. Reading this register does not automatically clear these bits. When set, these bits must be reset by asserting bit 62 of this register. For PRBS7 error detection in the memory-clock domain: Bit 0 represents the miscompare detect for wrap0 and wrap1. Bit 1 represents the miscompare detect for wrap2 and wrap3. Bit 2 represents the miscompare detect for wrap4 and wrap5. Bit 3 represents the miscompare detect for wrap6 and wrap7. Bit 4 represents the miscompare detect for wrap8 and wrap9. Reserved for ADR8. Bit 5 represents the miscompare detect for wrap10 and wrap11. Reserved for ADR8.
54:55	ROX	Reserved.

Bits	SCOM	Field Mnemonic: Description
56	RW	ADR_TEST_DATA_EN: When high, this bit selects macrotest data. Otherwise, functional mode is used.
57:58	RW	ADR_TEST_MODE: These bits are reserved for manufacturing test.
59	RW	ADR_TEST_4TO1_MODE: When active, the PRBS generates a 4-bit output every cycle. Otherwise, it outputs two bits. This signal is in the memory-clock domain.
60	RW	ADR_TEST_RESET: Reset. This signal is in the memory-clock domain.
61	RW	ADR_TEST_GEN_EN: Pattern generator enable. This signal is in the memory-clock domain. This signal must be active before enabling the check_enable_i; which is 8 cycles for loading the checker plus the latency between the generator and the wrap through APIN.
62	RW	ADR_TEST_CLEAR_ERROR: Clear error bits. This signal is in the memory-clock domain. The generator must be active before clr_error_i, and the macrotest_mode_i must be selecting WRAP clocks to all the corresponding checkers' latches.
63	RW	ADR_TEST_CHECK_EN: Enable the pattern checker. This signal is in the memory-clock domain. When active, the checker performs a PRBS7 sequence check on the corresponding WRAP channel.

Register Name	**ADR DFT Wrap Status and Control Register**
Mnemonic	IOM0.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P2_ADR0
Address	8000400C0701183F (SCOM)
Description	This register provides the status and control of the ADR wrap test for a given ADR8/12 instance. This register must only be used to perform diagnostic, manufacturing, or characterization testing. Contact your IBM representative before modifying this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:53	ROX	ADR_TEST_LANE_PAIR_FAIL: **Note:** Bits 48:55 of this register are read only. These bits can be reset, but they are written with a free running dphy_gckn clock. Therefore, any read of these bits returns the value from the loopback test logic. If that logic has not been reset and the error bits are cleared, this field is X. Reading this register does not automatically clear these bits. When set, these bits must be reset by asserting bit 62 of this register. For PRBS7 error detection in the memory-clock domain: Bit 0 represents the miscompare detect for wrap0 and wrap1. Bit 1 represents the miscompare detect for wrap2 and wrap3. Bit 2 represents the miscompare detect for wrap4 and wrap5. Bit 3 represents the miscompare detect for wrap6 and wrap7. Bit 4 represents the miscompare detect for wrap8 and wrap9. Reserved for ADR8. Bit 5 represents the miscompare detect for wrap10 and wrap11. Reserved for ADR8.
54:55	ROX	Reserved.
56	RW	ADR_TEST_DATA_EN: When high, this bit selects macrotest data. Otherwise, functional mode is used.
57:58	RW	ADR_TEST_MODE: These bits are reserved for manufacturing test.
59	RW	ADR_TEST_4TO1_MODE: When active, the PRBS generates a 4-bit output every cycle. Otherwise, it outputs two bits. This signal is in the memory-clock domain.
60	RW	ADR_TEST_RESET: Reset. This signal is in the memory-clock domain.
61	RW	ADR_TEST_GEN_EN: Pattern generator enable. This signal is in the memory-clock domain. This signal must be active before enabling the check_enable_i; which is 8 cycles for loading the checker plus the latency between the generator and the wrap through APIN.
62	RW	ADR_TEST_CLEAR_ERROR: Clear error bits. This signal is in the memory-clock domain. The generator must be active before clr_error_i, and the macrotest_mode_i must be selecting WRAP clocks to all the corresponding checkers' latches.

Bits	SCOM	Field Mnemonic: Description
63	RW	ADR_TEST_CHECK_EN: Enable the pattern checker. This signal is in the memory-clock domain. When active, the checker performs a PRBS7 sequence check on the corresponding WRAP channel.

Register Name	ADR DFT Wrap Status and Control Register
Mnemonic	IOM0.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P3_ADR0
Address	8000400C07011C3F (SCOM)
Description	This register provides the status and control of the ADR wrap test for a given ADR8/12 instance. This register must only be used to perform diagnostic, manufacturing, or characterization testing. Contact your IBM representative before modifying this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:53	ROX	ADR_TEST_LANE_PAIR_FAIL: **Note:** Bits 48:55 of this register are read only. These bits can be reset, but they are written with a free running dphy_gckn clock. Therefore, any read of these bits returns the value from the loopback test logic. If that logic has not been reset and the error bits are cleared, this field is X. Reading this register does not automatically clear these bits. When set, these bits must be reset by asserting bit 62 of this register. For PRBS7 error detection in the memory-clock domain: Bit 0 represents the miscompare detect for wrap0 and wrap1. Bit 1 represents the miscompare detect for wrap2 and wrap3. Bit 2 represents the miscompare detect for wrap4 and wrap5. Bit 3 represents the miscompare detect for wrap6 and wrap7. Bit 4 represents the miscompare detect for wrap8 and wrap9. Reserved for ADR8. Bit 5 represents the miscompare detect for wrap10 and wrap11. Reserved for ADR8.
54:55	ROX	Reserved.
56	RW	ADR_TEST_DATA_EN: When high, this bit selects macrotest data. Otherwise, functional mode is used.
57:58	RW	ADR_TEST_MODE: These bits are reserved for manufacturing test.
59	RW	ADR_TEST_4TO1_MODE: When active, the PRBS generates a 4-bit output every cycle. Otherwise, it outputs two bits. This signal is in the memory-clock domain.
60	RW	ADR_TEST_RESET: Reset. This signal is in the memory-clock domain.
61	RW	ADR_TEST_GEN_EN: Pattern generator enable. This signal is in the memory-clock domain. This signal must be active before enabling the check_enable_i; which is 8 cycles for loading the checker plus the latency between the generator and the wrap through APIN.
62	RW	ADR_TEST_CLEAR_ERROR: Clear error bits. This signal is in the memory-clock domain. The generator must be active before clr_error_i, and the macrotest_mode_i must be selecting WRAP clocks to all the corresponding checkers' latches.
63	RW	ADR_TEST_CHECK_EN: Enable the pattern checker. This signal is in the memory-clock domain. When active, the checker performs a PRBS7 sequence check on the corresponding WRAP channel.

Register Name	ADR I/O FET Slice Enable Map 0 Register
Mnemonic	IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P0_ADR0
Address	800040200701103F (SCOM)
Description	Each predefined pin on the ADR can be mapped to predetermined I/O field-effect transistor (FET) slice enable values to implement 30 Ω or 40 Ω drive impedance. Pins are defined by the mnemonic {{0-1}*8+n}, with n = 0 – 7. Register 0 contains lanes 0:7, and register 1 contains lanes 8:15.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000
48	RW	SLICE_SEL0: Select impedance values to be used for MEMINTC00O (ADR I/O FET Slice Enable Map 0) and MEMINTC08O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
49	RW	Reserved.
50	RW	SLICE_SEL1: Select impedance values to be used for MEMINTC01O (ADR I/O FET Slice Enable Map 0) and MEMINTC09O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
51	RW	Reserved.
52	RW	SLICE_SEL2: Select impedance values to be used for MEMINTC02O (ADR I/O FET Slice Enable Map 0) and MEMINTC10O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
53	RW	Reserved.
54	RW	SLICE_SEL3: Select impedance values to be used for MEMINTC03O (ADR I/O FET Slice Enable Map 0) and MEMINTC11O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
55	RW	Reserved.
56	RW	SLICE_SEL4: Select impedance values to be used for MEMINTC04O (ADR I/O FET Slice Enable Map 0) and MEMINTC12O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
57	RW	Reserved.
58	RW	SLICE_SEL5: Select impedance values to be used for MEMINTC05O (ADR I/O FET Slice Enable Map 0) and MEMINTC13O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
59	RW	Reserved.
60	RW	SLICE_SEL6: Select impedance values to be used for MEMINTC06O (ADR I/O FET Slice Enable Map 0) and MEMINTC14O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
61	RW	Reserved.
62	RW	SLICE_SEL7: Select impedance values to be used for MEMINTC07O (ADR I/O FET Slice Enable Map 0) and MEMINTC15O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
63	RW	Reserved.

Register Name	ADR I/O FET Slice Enable Map 0 Register
Mnemonic	IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P1_ADR0
Address	800040200701143F (SCOM)
Description	Each predefined pin on the ADR can be mapped to predetermined I/O FET slice enable values to implement 30 Ω or 40 Ω drive impedance. Pins are defined by the mnemonic {{0-1}*8+n}, with n = 0 – 7. Register 0 contains lanes 0:7, and register 1 contains lanes 8:15.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	SLICE_SEL0: Select impedance values to be used for MEMINTC00O (ADR I/O FET Slice Enable Map 0) and MEMINTC08O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
49	RW	Reserved.
50	RW	SLICE_SEL1: Select impedance values to be used for MEMINTC01O (ADR I/O FET Slice Enable Map 0) and MEMINTC09O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
51	RW	Reserved.
52	RW	SLICE_SEL2: Select impedance values to be used for MEMINTC02O (ADR I/O FET Slice Enable Map 0) and MEMINTC10O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
53	RW	Reserved.
54	RW	SLICE_SEL3: Select impedance values to be used for MEMINTC03O (ADR I/O FET Slice Enable Map 0) and MEMINTC11O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
55	RW	Reserved.
56	RW	SLICE_SEL4: Select impedance values to be used for MEMINTC04O (ADR I/O FET Slice Enable Map 0) and MEMINTC12O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
57	RW	Reserved.
58	RW	SLICE_SEL5: Select impedance values to be used for MEMINTC05O (ADR I/O FET Slice Enable Map 0) and MEMINTC13O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
59	RW	Reserved.
60	RW	SLICE_SEL6: Select impedance values to be used for MEMINTC06O (ADR I/O FET Slice Enable Map 0) and MEMINTC14O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
61	RW	Reserved.
62	RW	SLICE_SEL7: Select impedance values to be used for MEMINTC07O (ADR I/O FET Slice Enable Map 0) and MEMINTC15O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
63	RW	Reserved.

Register Name	**ADR I/O FET Slice Enable Map 0 Register**
Mnemonic	IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P2_ADR0
Address	800040200701183F (SCOM)
Description	Each predefined pin on the ADR can be mapped to predetermined I/O FET slice enable values to implement 30 Ω or 40 Ω drive impedance. Pins are defined by the mnemonic {{0-1}*8+n}, with n = 0 – 7. Register 0 contains lanes 0:7, and register 1 contains lanes 8:15.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	SLICE_SEL0: Select impedance values to be used for MEMINTC00O (ADR I/O FET Slice Enable Map 0) and MEMINTC08O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
49	RW	Reserved.
50	RW	SLICE_SEL1: Select impedance values to be used for MEMINTC01O (ADR I/O FET Slice Enable Map 0) and MEMINTC09O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
51	RW	Reserved.
52	RW	SLICE_SEL2: Select impedance values to be used for MEMINTC02O (ADR I/O FET Slice Enable Map 0) and MEMINTC10O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
53	RW	Reserved.
54	RW	SLICE_SEL3: Select impedance values to be used for MEMINTC03O (ADR I/O FET Slice Enable Map 0) and MEMINTC11O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
55	RW	Reserved.
56	RW	SLICE_SEL4: Select impedance values to be used for MEMINTC04O (ADR I/O FET Slice Enable Map 0) and MEMINTC12O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
57	RW	Reserved.
58	RW	SLICE_SEL5: Select impedance values to be used for MEMINTC05O (ADR I/O FET Slice Enable Map 0) and MEMINTC13O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
59	RW	Reserved.
60	RW	SLICE_SEL6: Select impedance values to be used for MEMINTC06O (ADR I/O FET Slice Enable Map 0) and MEMINTC14O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
61	RW	Reserved.
62	RW	SLICE_SEL7: Select impedance values to be used for MEMINTC07O (ADR I/O FET Slice Enable Map 0) and MEMINTC15O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.

Bits	SCOM	Field Mnemonic: Description
63	RW	Reserved.

Register Name	ADR I/O FET Slice Enable Map 0 Register
Mnemonic	IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P3_ADR0
Address	8000402007011C3F (SCOM)
Description	Each predefined pin on the ADR can be mapped to predetermined I/O FET slice enable values to implement 30 Ω or 40 Ω drive impedance. Pins are defined by the mnemonic {{0-1}*8+n}, with n = 0 – 7. Register 0 contains lanes 0:7, and register 1 contains lanes 8:15.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48	RW	SLICE_SEL0: Select impedance values to be used for MEMINTC00O (ADR I/O FET Slice Enable Map 0) and MEMINTC08O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
49	RW	Reserved.
50	RW	SLICE_SEL1: Select impedance values to be used for MEMINTC01O (ADR I/O FET Slice Enable Map 0) and MEMINTC09O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
51	RW	Reserved.
52	RW	SLICE_SEL2: Select impedance values to be used for MEMINTC02O (ADR I/O FET Slice Enable Map 0) and MEMINTC10O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
53	RW	Reserved.
54	RW	SLICE_SEL3: Select impedance values to be used for MEMINTC03O (ADR I/O FET Slice Enable Map 0) and MEMINTC11O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
55	RW	Reserved.
56	RW	SLICE_SEL4: Select impedance values to be used for MEMINTC04O (ADR I/O FET Slice Enable Map 0) and MEMINTC12O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
57	RW	Reserved.
58	RW	SLICE_SEL5: Select impedance values to be used for MEMINTC05O (ADR I/O FET Slice Enable Map 0) and MEMINTC13O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
59	RW	Reserved.
60	RW	SLICE_SEL6: Select impedance values to be used for MEMINTC06O (ADR I/O FET Slice Enable Map 0) and MEMINTC14O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
61	RW	Reserved.

Bits	SCOM	Field Mnemonic: Description
62	RW	SLICE_SEL7: Select impedance values to be used for MEMINTC07O (ADR I/O FET Slice Enable Map 0) and MEMINTC15O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
63	RW	Reserved.

Register Name	ADR I/O FET Slice Enable Map 1 Register
Mnemonic	IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P0_ADR0
Address	800040210701103F (SCOM)
Description	Each predefined pin on the ADR can be mapped to predetermined I/O FET slice enable values to implement 30 Ω or 40 Ω drive impedance. Pins are defined by the mnemonic {{0-1}*8+n}, with n = 0 – 7. Register 0 contains lanes 0:7, and register 1 contains lanes 8:15.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48	RW	SLICE_SEL8: Select impedance values to be used for MEMINTC00O (ADR I/O FET Slice Enable Map 0) and MEMINTC08O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
49	RW	Reserved.
50:51	RW	SLICE_SEL9: Select one of four impedance values to be used for MEMINTC01O (ADR I/O FET Slice Enable Map 0) and MEMINTC09O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
52:53	RW	SLICE_SEL10: Select one of four impedance values to be used for MEMINTC02O (ADR I/O FET Slice Enable Map 0) and MEMINTC10O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
54:55	RW	SLICE_SEL11: Select one of four impedance values to be used for MEMINTC03O (ADR I/O FET Slice Enable Map 0) and MEMINTC11O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
56:57	RW	SLICE_SEL12: Select one of four impedance values to be used for MEMINTC04O (ADR I/O FET Slice Enable Map 0) and MEMINTC12O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
58:59	RW	SLICE_SEL13: Select one of four impedance values to be used for MEMINTC05O (ADR I/O FET Slice Enable Map 0) and MEMINTC13O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.

Bits	SCOM	Field Mnemonic: Description
60:61	RW	SLICE_SEL14: Select one of four impedance values to be used for MEMINTC06O (ADR I/O FET Slice Enable Map 0) and MEMINTC14O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
62:63	RW	SLICE_SEL15: Select one of four impedance values to be used for MEMINTC07O (ADR I/O FET Slice Enable Map 0) and MEMINTC15O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.

Register Name	**ADR I/O FET Slice Enable Map 1 Register**
Mnemonic	IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P1_ADR0
Address	800040210701143F (SCOM)
Description	Each predefined pin on the ADR can be mapped to predetermined I/O FET slice enable values to implement 30 Ω or 40 Ω drive impedance. Pins are defined by the mnemonic {{0-1}*8+n}, with n = 0 – 7. Register 0 contains lanes 0:7, and register 1 contains lanes 8:15.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48	RW	SLICE_SEL8: Select impedance values to be used for MEMINTC00O (ADR I/O FET Slice Enable Map 0) and MEMINTC08O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
49	RW	Reserved.
50:51	RW	SLICE_SEL9: Select one of four impedance values to be used for MEMINTC01O (ADR I/O FET Slice Enable Map 0) and MEMINTC09O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
52:53	RW	SLICE_SEL10: Select one of four impedance values to be used for MEMINTC02O (ADR I/O FET Slice Enable Map 0) and MEMINTC10O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
54:55	RW	SLICE_SEL11: Select one of four impedance values to be used for MEMINTC03O (ADR I/O FET Slice Enable Map 0) and MEMINTC11O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
56:57	RW	SLICE_SEL12: Select one of four impedance values to be used for MEMINTC04O (ADR I/O FET Slice Enable Map 0) and MEMINTC12O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.

Bits	SCOM	Field Mnemonic: Description
58:59	RW	SLICE_SEL13: Select one of four impedance values to be used for MEMINTC05O (ADR I/O FET Slice Enable Map 0) and MEMINTC13O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
60:61	RW	SLICE_SEL14: Select one of four impedance values to be used for MEMINTC06O (ADR I/O FET Slice Enable Map 0) and MEMINTC14O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
62:63	RW	SLICE_SEL15: Select one of four impedance values to be used for MEMINTC07O (ADR I/O FET Slice Enable Map 0) and MEMINTC15O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.

Register Name	**ADR I/O FET Slice Enable Map 1 Register**
Mnemonic	IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P2_ADR0
Address	800040210701183F (SCOM)
Description	Each predefined pin on the ADR can be mapped to predetermined I/O FET slice enable values to implement 30 Ω or 40 Ω drive impedance. Pins are defined by the mnemonic {{0-1}*8+n}, with n = 0 – 7. Register 0 contains lanes 0:7, and register 1 contains lanes 8:15.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	SLICE_SEL8: Select impedance values to be used for MEMINTC00O (ADR I/O FET Slice Enable Map 0) and MEMINTC08O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
49	RW	Reserved.
50:51	RW	SLICE_SEL9: Select one of four impedance values to be used for MEMINTC01O (ADR I/O FET Slice Enable Map 0) and MEMINTC09O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
52:53	RW	SLICE_SEL10: Select one of four impedance values to be used for MEMINTC02O (ADR I/O FET Slice Enable Map 0) and MEMINTC10O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
54:55	RW	SLICE_SEL11: Select one of four impedance values to be used for MEMINTC03O (ADR I/O FET Slice Enable Map 0) and MEMINTC11O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.

Bits	SCOM	Field Mnemonic: Description
56:57	RW	SLICE_SEL12: Select one of four impedance values to be used for MEMINTC04O (ADR I/O FET Slice Enable Map 0) and MEMINTC12O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
58:59	RW	SLICE_SEL13: Select one of four impedance values to be used for MEMINTC05O (ADR I/O FET Slice Enable Map 0) and MEMINTC13O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
60:61	RW	SLICE_SEL14: Select one of four impedance values to be used for MEMINTC06O (ADR I/O FET Slice Enable Map 0) and MEMINTC14O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
62:63	RW	SLICE_SEL15: Select one of four impedance values to be used for MEMINTC07O (ADR I/O FET Slice Enable Map 0) and MEMINTC15O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.

Register Name	**ADR I/O FET Slice Enable Map 1 Register**
Mnemonic	IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P3_ADR0
Address	8000402107011C3F (SCOM)
Description	Each predefined pin on the ADR can be mapped to predetermined I/O FET slice enable values to implement 30 Ω or 40 Ω drive impedance. Pins are defined by the mnemonic {{0-1}*8+n}, with n = 0 – 7. Register 0 contains lanes 0:7, and register 1 contains lanes 8:15.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	SLICE_SEL8: Select impedance values to be used for MEMINTC00O (ADR I/O FET Slice Enable Map 0) and MEMINTC08O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
49	RW	Reserved.
50:51	RW	SLICE_SEL9: Select one of four impedance values to be used for MEMINTC01O (ADR I/O FET Slice Enable Map 0) and MEMINTC09O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
52:53	RW	SLICE_SEL10: Select one of four impedance values to be used for MEMINTC02O (ADR I/O FET Slice Enable Map 0) and MEMINTC10O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.

Bits	SCOM	Field Mnemonic: Description
54:55	RW	SLICE_SEL11: Select one of four impedance values to be used for MEMINTC03O (ADR I/O FET Slice Enable Map 0) and MEMINTC11O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
56:57	RW	SLICE_SEL12: Select one of four impedance values to be used for MEMINTC04O (ADR I/O FET Slice Enable Map 0) and MEMINTC12O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
58:59	RW	SLICE_SEL13: Select one of four impedance values to be used for MEMINTC05O (ADR I/O FET Slice Enable Map 0) and MEMINTC13O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
60:61	RW	SLICE_SEL14: Select one of four impedance values to be used for MEMINTC06O (ADR I/O FET Slice Enable Map 0) and MEMINTC14O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
62:63	RW	SLICE_SEL15: Select one of four impedance values to be used for MEMINTC07O (ADR I/O FET Slice Enable Map 0) and MEMINTC15O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.

Register Name	ADR RESERVED 10 Register
Mnemonic	IOM0.DDRPHY_ADR_RESERVED10_P0_ADR0
Address	8000402A0701103F (SCOM)
Description	Currently reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	Reserved.

Register Name	ADR RESERVED 10 Register
Mnemonic	IOM0.DDRPHY_ADR_RESERVED10_P1_ADR0
Address	8000402A0701143F (SCOM)
Description	Currently reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	Reserved.

Register Name	ADR RESERVED 10 Register
Mnemonic	IOM0.DDRPHY_ADR_RESERVED10_P2_ADR0
Address	8000402A0701183F (SCOM)
Description	Currently reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	Reserved.

Register Name	ADR RESERVED 10 Register
Mnemonic	IOM0.DDRPHY_ADR_RESERVED10_P3_ADR0
Address	8000402A07011C3F (SCOM)
Description	Currently reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	Reserved.

Register Name	ADR RESERVED 11 Register
Mnemonic	IOM0.DDRPHY_ADR_RESERVED11_P0_ADR0
Address	8000402B0701103F (SCOM)
Description	Currently reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	Reserved.

Register Name	ADR RESERVED 11 Register
Mnemonic	IOM0.DDRPHY_ADR_RESERVED11_P1_ADR0
Address	8000402B0701143F (SCOM)
Description	Currently reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	Reserved.

Register Name	ADR RESERVED 11 Register
Mnemonic	IOM0.DDRPHY_ADR_RESERVED11_P2_ADR0
Address	8000402B0701183F (SCOM)
Description	Currently reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	Reserved.

Register Name	ADR RESERVED 11 Register
Mnemonic	IOM0.DDRPHY_ADR_RESERVED11_P3_ADR0
Address	8000402B07011C3F (SCOM)
Description	Currently reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	Reserved.

Register Name	ADR Power Down 2 Register
Mnemonic	IOM0.DDRPHY_ADR_POWERDOWN_2_P0_ADR0
Address	8000402C0701103F (SCOM)
Description	This register provides control of the ADR power-down modes.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:55	RW	ADR_LANE_0_7_PD: 0 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{0-7} is at high-Z (tri-stated). 1 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{0-7} drives the value programmed in bit 55 the PC Power Down 1 Register at the impedance programmed into the ADR I/O FET Slice Enable Map {0-1} Register.
56:59	RW	ADR_Lane_8_11_PD: ADR12: 0 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{8-11} is at high-Z (tri-stated). 1 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{8-11} drives the value programmed in bit 55 of PC Power Down 1 Register at the impedance programmed into the ADR I/O FET Slice Enable Map {0-1} Register. ADR8: Reserved.
60:63	RW	ADR_LANE_12_15_PD: Reserved.

Register Name	ADR Power Down 2 Register
Mnemonic	IOM0.DDRPHY_ADR_POWERDOWN_2_P1_ADR0
Address	8000402C0701143F (SCOM)
Description	This register provides control of the ADR power-down modes.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:55	RW	ADR_LANE_0_7_PD: 0 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{0-7} is at high-Z (tri-stated). 1 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{0-7} drives the value programmed in bit 55 the PC Power Down 1 Register at the impedance programmed into the ADR I/O FET Slice Enable Map {0-1} Register.
56:59	RW	ADR_Lane_8_11_PD: ADR12: 0 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{8-11} is at high-Z (tri-stated). 1 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{8-11} drives the value programmed in bit 55 of PC Power Down 1 Register at the impedance programmed into the ADR I/O FET Slice Enable Map {0-1} Register. ADR8: Reserved.
60:63	RW	ADR_LANE_12_15_PD: Reserved.

Register Name	ADR Power Down 2 Register
Mnemonic	IOM0.DDRPHY_ADR_POWERDOWN_2_P2_ADR0
Address	8000402C0701183F (SCOM)
Description	This register provides control of the ADR power-down modes.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:55	RW	ADR_LANE_0_7_PD: 0 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{0-7} is at high-Z (tri-stated). 1 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{0-7} drives the value programmed in bit 55 the PC Power Down 1 Register at the impedance programmed into the ADR I/O FET Slice Enable Map {0-1} Register.
56:59	RW	ADR_Lane_8_11_PD: ADR12: 0 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{8-11} is at high-Z (tri-stated). 1 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{8-11} drives the value programmed in bit 55 of PC Power Down 1 Register at the impedance programmed into the ADR I/O FET Slice Enable Map {0-1} Register. ADR8: Reserved.
60:63	RW	ADR_LANE_12_15_PD: Reserved.

Register Name	ADR Power Down 2 Register
Mnemonic	IOM0.DDRPHY_ADR_POWERDOWN_2_P3_ADR0
Address	8000402C07011C3F (SCOM)
Description	This register provides control of the ADR power-down modes.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:55	RW	ADR_LANE_0_7_PD: 0 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{0-7} is at high-Z (tri-stated). 1 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{0-7} drives the value programmed in bit 55 the PC Power Down 1 Register at the impedance programmed into the ADR I/O FET Slice Enable Map {0-1} Register.
56:59	RW	ADR_Lane_8_11_PD: ADR12: 0 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{8-11} is at high-Z (tri-stated). 1 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{8-11} drives the value programmed in bit 55 of PC Power Down 1 Register at the impedance programmed into the ADR I/O FET Slice Enable Map {0-1} Register. ADR8: Reserved.
60:63	RW	ADR_LANE_12_15_PD: Reserved.

Register Name	ADR Bit Enable Register
Mnemonic	IOM0.DDRPHY_ADR_BIT_ENABLE_P0_ADR1
Address	800044000701103F (SCOM)
Description	An ADR12 has 12 possible outputs, and an ADR8 has 8 possible outputs. This register is used to enable and disable each of the 12 pins or 8 pins. Any pins used on an ADR must be enabled via this register. The pins on an ADR can be used to send clocks or control (command, address, and so on) signals to memory devices.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:59	RW	BIT_ENABLE_0_11: 1 = Indicates that the ADR bit is enabled and is used for sending clocks or control (command, address, and so on) signals to the memory device. 0 = Indicates that the ADR bit is not used and not enabled. Bit 0 controls MEMINTC00O(n). Bit 1 controls MEMINTC01O(n). Bit 2 controls MEMINTC02O(n). ... Bit 11 controls MEMINTC11O(n). where n is the ADR instance number. ADR12 uses bits 48:59. ADR8 uses bits 48:55, with bits 56:59 reserved.
60:63	RW	Reserved.

Register Name	ADR Bit Enable Register
Mnemonic	IOM0.DDRPHY_ADR_BIT_ENABLE_P1_ADR1
Address	800044000701143F (SCOM)
Description	An ADR12 has 12 possible outputs, and an ADR8 has 8 possible outputs. This register is used to enable and disable each of the 12 pins or 8 pins. Any pins used on an ADR must be enabled via this register. The pins on an ADR can be used to send clocks or control (command, address, and so on) signals to memory devices.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:59	RW	BIT_ENABLE_0_11: 1 = Indicates that the ADR bit is enabled and is used for sending clocks or control (command, address, and so on) signals to the memory device. 0 = Indicates that the ADR bit is not used and not enabled. Bit 0 controls MEMINTC00O(n). Bit 1 controls MEMINTC01O(n). Bit 2 controls MEMINTC02O(n). ... Bit 11 controls MEMINTC11O(n). where n is the ADR instance number. ADR12 uses bits 48:59. ADR8 uses bits 48:55, with bits 56:59 reserved.
60:63	RW	Reserved.

Register Name	ADR Bit Enable Register
Mnemonic	IOM0.DDRPHY_ADR_BIT_ENABLE_P2_ADR1
Address	800044000701183F (SCOM)
Description	An ADR12 has 12 possible outputs, and an ADR8 has 8 possible outputs. This register is used to enable and disable each of the 12 pins or 8 pins. Any pins used on an ADR must be enabled via this register. The pins on an ADR can be used to send clocks or control (command, address, and so on) signals to memory devices.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:59	RW	BIT_ENABLE_0_11: 1 = Indicates that the ADR bit is enabled and is used for sending clocks or control (command, address, and so on) signals to the memory device. 0 = Indicates that the ADR bit is not used and not enabled. Bit 0 controls MEMINTC00O(n). Bit 1 controls MEMINTC01O(n). Bit 2 controls MEMINTC02O(n). ... Bit 11 controls MEMINTC11O(n). where n is the ADR instance number. ADR12 uses bits 48:59. ADR8 uses bits 48:55, with bits 56:59 reserved.
60:63	RW	Reserved.

Register Name	ADR Bit Enable Register
Mnemonic	IOM0.DDRPHY_ADR_BIT_ENABLE_P3_ADR1
Address	8000440007011C3F (SCOM)
Description	An ADR12 has 12 possible outputs, and an ADR8 has 8 possible outputs. This register is used to enable and disable each of the 12 pins or 8 pins. Any pins used on an ADR must be enabled via this register. The pins on an ADR can be used to send clocks or control (command, address, and so on) signals to memory devices.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:59	RW	BIT_ENABLE_0_11: 1 = Indicates that the ADR bit is enabled and is used for sending clocks or control (command, address, and so on) signals to the memory device. 0 = Indicates that the ADR bit is not used and not enabled. Bit 0 controls MEMINTC00O(n). Bit 1 controls MEMINTC01O(n). Bit 2 controls MEMINTC02O(n). ... Bit 11 controls MEMINTC11O(n). where n is the ADR instance number. ADR12 uses bits 48:59. ADR8 uses bits 48:55, with bits 56:59 reserved.
60:63	RW	Reserved.

Register Name	ADR Differential Pair Enable Register
Mnemonic	IOM0.DDRPHY_ADR_DIFFPAIR_ENABLE_P0_ADR1
Address	800044010701103F (SCOM)
Description	An ADR12 has 12 possible outputs, and an ADR8 has 8 possible outputs, any of which can be paired together for memory clock generation (CK/CK#). This register is used to enable or disable each pair of ADR pins to be used as differential outputs or as two single-ended outputs. When a pair of ADR pins is configured as a differential output, the delays associated with both outputs of the differential pair must be programmed to the same value in the ADR Delay Value {0-7} Registers for that pair. When a pair of ADR pins is enabled as a differential pair in this register, both of the pins must be enabled in the ADR Bit Enable Register. When a pair of ADR pins is enabled as a differential pair in this register, the even-numbered pin is the true, and the odd-numbered pin is the complement signal.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	DI_ADR0_ADR1: 0 = Lanes 0 and 1 are not a differential clock pair. 1 = Lanes 0 and 1 are a differential clock pair.
49	RW	DI_ADR2_ADR3: 0 = Lanes 2 and 3 are not a differential clock pair. 1 = Lanes 2 and 3 are a differential clock pair.
50	RW	DI_ADR4_ADR5: 0 = Lanes 4 and 5 are not a differential clock pair. 1 = Lanes 4 and 5 are a differential clock pair.
51	RW	DI_ADR6_ADR7: 0 = Lanes 6 and 7 are not a differential clock pair. 1 = Lanes 6 and 7 are a differential clock pair.

Bits	SCOM	Field Mnemonic: Description
52	RW	DI_ADR8_ADR9: 0 = Lanes 8 and 9 are not a differential clock pair. 1 = Lanes 8 and 9 are a differential clock pair. Reserved for ADR8.
53	RW	DI_ADR10_ADR11: 0 = Lanes 10 and 11 are not a differential clock pair. 1 = Lanes 10 and 11 are a differential clock pair. Reserved for ADR8.
54:63	RW	Reserved.

Register Name	ADR Differential Pair Enable Register
Mnemonic	IOM0.DDRPHY_ADR_DIFFPAIR_ENABLE_P1_ADR1
Address	800044010701143F (SCOM)
Description	An ADR12 has 12 possible outputs, and an ADR8 has 8 possible outputs, any of which can be paired together for memory clock generation (CK/CK#). This register is used to enable or disable each pair of ADR pins to be used as differential outputs or as two single-ended outputs. When a pair of ADR pins is configured as a differential output, the delays associated with both outputs of the differential pair must be programmed to the same value in the ADR Delay Value {0-7} Registers for that pair. When a pair of ADR pins is enabled as a differential pair in this register, both of the pins must be enabled in the ADR Bit Enable Register. When a pair of ADR pins is enabled as a differential pair in this register, the even-numbered pin is the true, and the odd-numbered pin is the complement signal.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	DI_ADR0_ADR1: 0 = Lanes 0 and 1 are not a differential clock pair. 1 = Lanes 0 and 1 are a differential clock pair.
49	RW	DI_ADR2_ADR3: 0 = Lanes 2 and 3 are not a differential clock pair. 1 = Lanes 2 and 3 are a differential clock pair.
50	RW	DI_ADR4_ADR5: 0 = Lanes 4 and 5 are not a differential clock pair. 1 = Lanes 4 and 5 are a differential clock pair.
51	RW	DI_ADR6_ADR7: 0 = Lanes 6 and 7 are not a differential clock pair. 1 = Lanes 6 and 7 are a differential clock pair.
52	RW	DI_ADR8_ADR9: 0 = Lanes 8 and 9 are not a differential clock pair. 1 = Lanes 8 and 9 are a differential clock pair. Reserved for ADR8.
53	RW	DI_ADR10_ADR11: 0 = Lanes 10 and 11 are not a differential clock pair. 1 = Lanes 10 and 11 are a differential clock pair. Reserved for ADR8.
54:63	RW	Reserved.

Register Name	ADR Differential Pair Enable Register
Mnemonic	IOM0.DDRPHY_ADR_DIFFPAIR_ENABLE_P2_ADR1
Address	800044010701183F (SCOM)
Description	An ADR12 has 12 possible outputs, and an ADR8 has 8 possible outputs, any of which can be paired together for memory clock generation (CK/CK#). This register is used to enable or disable each pair of ADR pins to be used as differential outputs or as two single-ended outputs. When a pair of ADR pins is configured as a differential output, the delays associated with both outputs of the differential pair must be programmed to the same value in the ADR Delay Value {0-7} Registers for that pair. When a pair of ADR pins is enabled as a differential pair in this register, both of the pins must be enabled in the ADR Bit Enable Register. When a pair of ADR pins is enabled as a differential pair in this register, the even-numbered pin is the true, and the odd-numbered pin is the complement signal.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	DI_ADR0_ADR1: 0 = Lanes 0 and 1 are not a differential clock pair. 1 = Lanes 0 and 1 are a differential clock pair.
49	RW	DI_ADR2_ADR3: 0 = Lanes 2 and 3 are not a differential clock pair. 1 = Lanes 2 and 3 are a differential clock pair.
50	RW	DI_ADR4_ADR5: 0 = Lanes 4 and 5 are not a differential clock pair. 1 = Lanes 4 and 5 are a differential clock pair.
51	RW	DI_ADR6_ADR7: 0 = Lanes 6 and 7 are not a differential clock pair. 1 = Lanes 6 and 7 are a differential clock pair.
52	RW	DI_ADR8_ADR9: 0 = Lanes 8 and 9 are not a differential clock pair. 1 = Lanes 8 and 9 are a differential clock pair. Reserved for ADR8.
53	RW	DI_ADR10_ADR11: 0 = Lanes 10 and 11 are not a differential clock pair. 1 = Lanes 10 and 11 are a differential clock pair. Reserved for ADR8.
54:63	RW	Reserved.

Register Name	ADR Differential Pair Enable Register
Mnemonic	IOM0.DDRPHY_ADR_DIFFPAIR_ENABLE_P3_ADR1
Address	8000440107011C3F (SCOM)
Description	An ADR12 has 12 possible outputs, and an ADR8 has 8 possible outputs, any of which can be paired together for memory clock generation (CK/CK#). This register is used to enable or disable each pair of ADR pins to be used as differential outputs or as two single-ended outputs. When a pair of ADR pins is configured as a differential output, the delays associated with both outputs of the differential pair must be programmed to the same value in the ADR Delay Value {0-7} Registers for that pair. When a pair of ADR pins is enabled as a differential pair in this register, both of the pins must be enabled in the ADR Bit Enable Register. When a pair of ADR pins is enabled as a differential pair in this register, the even-numbered pin is the true, and the odd-numbered pin is the complement signal.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RW	DI_ADR0_ADR1: 0 = Lanes 0 and 1 are not a differential clock pair. 1 = Lanes 0 and 1 are a differential clock pair.
49	RW	DI_ADR2_ADR3: 0 = Lanes 2 and 3 are not a differential clock pair. 1 = Lanes 2 and 3 are a differential clock pair.
50	RW	DI_ADR4_ADR5: 0 = Lanes 4 and 5 are not a differential clock pair. 1 = Lanes 4 and 5 are a differential clock pair.
51	RW	DI_ADR6_ADR7: 0 = Lanes 6 and 7 are not a differential clock pair. 1 = Lanes 6 and 7 are a differential clock pair.
52	RW	DI_ADR8_ADR9: 0 = Lanes 8 and 9 are not a differential clock pair. 1 = Lanes 8 and 9 are a differential clock pair. Reserved for ADR8.
53	RW	DI_ADR10_ADR11: 0 = Lanes 10 and 11 are not a differential clock pair. 1 = Lanes 10 and 11 are a differential clock pair. Reserved for ADR8.
54:63	RW	Reserved.

Register Name	ADR Delay Value 0 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY0_P0_ADR1
Address	800044040701103F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY0: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY1: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 0 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY0_P1_ADR1
Address	800044040701143F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY0: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY1: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 0 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY0_P2_ADR1
Address	800044040701183F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY0: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY1: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 0 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY0_P3_ADR1
Address	8000440407011C3F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY0: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY1: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 1 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY1_P0_ADR1
Address	800044050701103F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY2: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY3: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 1 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY1_P1_ADR1
Address	800044050701143F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY2: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY3: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 1 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY1_P2_ADR1
Address	800044050701183F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY2: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY3: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 1 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY1_P3_ADR1
Address	8000440507011C3F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY2: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY3: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 2 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY2_P0_ADR1
Address	800044060701103F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY4: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY5: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 2 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY2_P1_ADR1
Address	800044060701143F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY4: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY5: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 2 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY2_P2_ADR1
Address	800044060701183F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY4: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY5: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 2 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY2_P3_ADR1
Address	8000440607011C3F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY4: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY5: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 3 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY3_P0_ADR1
Address	800044070701103F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY6: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY7: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 3 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY3_P1_ADR1
Address	800044070701143F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY6: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY7: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 3 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY3_P2_ADR1
Address	800044070701183F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY6: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY7: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 3 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY3_P3_ADR1
Address	8000440707011C3F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY6: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY7: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 4 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY4_P0_ADR1
Address	800044080701103F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY8: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY9: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 4 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY4_P1_ADR1
Address	800044080701143F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY8: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY9: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 4 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY4_P2_ADR1
Address	800044080701183F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY8: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY9: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 4 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY4_P3_ADR1
Address	8000440807011C3F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY8: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY9: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 5 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY5_P0_ADR1
Address	800044090701103F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY10: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY11: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 5 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY5_P1_ADR1
Address	800044090701143F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY10: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY11: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 5 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY5_P2_ADR1
Address	800044090701183F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY10: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY11: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 5 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY5_P3_ADR1
Address	8000440907011C3F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY10: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY11: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 6 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY6_P0_ADR1
Address	8000440A0701103F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY12: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY13: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 6 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY6_P1_ADR1
Address	8000440A0701143F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY12: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY13: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 6 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY6_P2_ADR1
Address	8000440A0701183F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY12: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY13: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 6 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY6_P3_ADR1
Address	8000440A07011C3F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY12: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY13: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 7 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY7_P0_ADR1
Address	8000440B0701103F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY14: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY15: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 7 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY7_P1_ADR1
Address	8000440B0701143F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY14: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY15: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 7 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY7_P2_ADR1
Address	8000440B0701183F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY14: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY15: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 7 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY7_P3_ADR1
Address	8000440B07011C3F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY14: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY15: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR DFT Wrap Status and Control Register
Mnemonic	IOM0.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P0_ADR1
Address	8000440C0701103F (SCOM)
Description	This register provides the status and control of the ADR wrap test for a given ADR8/12 instance. This register must only be used to perform diagnostic, manufacturing, or characterization testing. Contact your IBM representative before modifying this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:53	ROX	ADR_TEST_LANE_PAIR_FAIL: **Note:** Bits 48:55 of this register are read only. These bits can be reset, but they are written with a free running dphy_gckn clock. Therefore, any read of these bits returns the value from the loopback test logic. If that logic has not been reset and the error bits are cleared, this field is X. Reading this register does not automatically clear these bits. When set, these bits must be reset by asserting bit 62 of this register. For PRBS7 error detection in the memory-clock domain: Bit 0 represents the miscompare detect for wrap0 and wrap1. Bit 1 represents the miscompare detect for wrap2 and wrap3. Bit 2 represents the miscompare detect for wrap4 and wrap5. Bit 3 represents the miscompare detect for wrap6 and wrap7. Bit 4 represents the miscompare detect for wrap8 and wrap9. Reserved for ADR8. Bit 5 represents the miscompare detect for wrap10 and wrap11. Reserved for ADR8.
54:55	ROX	Reserved.
56	RW	ADR_TEST_DATA_EN: When high, this bit selects macrotest data. Otherwise, functional mode is used.
57:58	RW	ADR_TEST_MODE: These bits are reserved for manufacturing test.
59	RW	ADR_TEST_4TO1_MODE: When active, the PRBS generates a 4-bit output every cycle. Otherwise, it outputs two bits. This signal is in the memory-clock domain.
60	RW	ADR_TEST_RESET: Reset. This signal is in the memory-clock domain.
61	RW	ADR_TEST_GEN_EN: Pattern generator enable. This signal is in the memory-clock domain. This signal must be active before enabling the check_enable_i; which is 8 cycles for loading the checker plus the latency between the generator and the wrap through APIN.

Bits	SCOM	Field Mnemonic: Description
62	RW	ADR_TEST_CLEAR_ERROR: Clear error bits. This signal is in the memory-clock domain. The generator must be active before clr_error_i, and the macrotest_mode_i must be selecting WRAP clocks to all the corresponding checkers' latches.
63	RW	ADR_TEST_CHECK_EN: Enable the pattern checker. This signal is in the memory-clock domain. When active, the checker performs a PRBS7 sequence check on the corresponding WRAP channel.

Register Name	**ADR DFT Wrap Status and Control Register**
Mnemonic	IOM0.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P1_ADR1
Address	8000440C0701143F (SCOM)
Description	This register provides the status and control of the ADR wrap test for a given ADR8/12 instance. This register must only be used to perform diagnostic, manufacturing, or characterization testing. Contact your IBM representative before modifying this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:53	ROX	ADR_TEST_LANE_PAIR_FAIL: **Note:** Bits 48:55 of this register are read only. These bits can be reset, but they are written with a free running dphy_gckn clock. Therefore, any read of these bits returns the value from the loopback test logic. If that logic has not been reset and the error bits are cleared, this field is X. Reading this register does not automatically clear these bits. When set, these bits must be reset by asserting bit 62 of this register. For PRBS7 error detection in the memory-clock domain: Bit 0 represents the miscompare detect for wrap0 and wrap1. Bit 1 represents the miscompare detect for wrap2 and wrap3. Bit 2 represents the miscompare detect for wrap4 and wrap5. Bit 3 represents the miscompare detect for wrap6 and wrap7. Bit 4 represents the miscompare detect for wrap8 and wrap9. Reserved for ADR8. Bit 5 represents the miscompare detect for wrap10 and wrap11. Reserved for ADR8.
54:55	ROX	Reserved.
56	RW	ADR_TEST_DATA_EN: When high, this bit selects macrotest data. Otherwise, functional mode is used.
57:58	RW	ADR_TEST_MODE: These bits are reserved for manufacturing test.
59	RW	ADR_TEST_4TO1_MODE: When active, the PRBS generates a 4-bit output every cycle. Otherwise, it outputs two bits. This signal is in the memory-clock domain.
60	RW	ADR_TEST_RESET: Reset. This signal is in the memory-clock domain.
61	RW	ADR_TEST_GEN_EN: Pattern generator enable. This signal is in the memory-clock domain. This signal must be active before enabling the check_enable_i; which is 8 cycles for loading the checker plus the latency between the generator and the wrap through APIN.
62	RW	ADR_TEST_CLEAR_ERROR: Clear error bits. This signal is in the memory-clock domain. The generator must be active before clr_error_i, and the macrotest_mode_i must be selecting WRAP clocks to all the corresponding checkers' latches.
63	RW	ADR_TEST_CHECK_EN: Enable the pattern checker. This signal is in the memory-clock domain. When active, the checker performs a PRBS7 sequence check on the corresponding WRAP channel.

Register Name	ADR DFT Wrap Status and Control Register
Mnemonic	IOM0.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P2_ADR1
Address	8000440C0701183F (SCOM)
Description	This register provides the status and control of the ADR wrap test for a given ADR8/12 instance. This register must only be used to perform diagnostic, manufacturing, or characterization testing. Contact your IBM representative before modifying this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:53	ROX	ADR_TEST_LANE_PAIR_FAIL: **Note:** Bits 48:55 of this register are read only. These bits can be reset, but they are written with a free running dphy_gckn clock. Therefore, any read of these bits returns the value from the loopback test logic. If that logic has not been reset and the error bits are cleared, this field is X. Reading this register does not automatically clear these bits. When set, these bits must be reset by asserting bit 62 of this register. For PRBS7 error detection in the memory-clock domain: Bit 0 represents the miscompare detect for wrap0 and wrap1. Bit 1 represents the miscompare detect for wrap2 and wrap3. Bit 2 represents the miscompare detect for wrap4 and wrap5. Bit 3 represents the miscompare detect for wrap6 and wrap7. Bit 4 represents the miscompare detect for wrap8 and wrap9. Reserved for ADR8. Bit 5 represents the miscompare detect for wrap10 and wrap11. Reserved for ADR8.
54:55	ROX	Reserved.
56	RW	ADR_TEST_DATA_EN: When high, this bit selects macrotest data. Otherwise, functional mode is used.
57:58	RW	ADR_TEST_MODE: These bits are reserved for manufacturing test.
59	RW	ADR_TEST_4TO1_MODE: When active, the PRBS generates a 4-bit output every cycle. Otherwise, it outputs two bits. This signal is in the memory-clock domain.
60	RW	ADR_TEST_RESET: Reset. This signal is in the memory-clock domain.
61	RW	ADR_TEST_GEN_EN: Pattern generator enable. This signal is in the memory-clock domain. This signal must be active before enabling the check_enable_i; which is 8 cycles for loading the checker plus the latency between the generator and the wrap through APIN.
62	RW	ADR_TEST_CLEAR_ERROR: Clear error bits. This signal is in the memory-clock domain. The generator must be active before clr_error_i, and the macrotest_mode_i must be selecting WRAP clocks to all the corresponding checkers' latches.
63	RW	ADR_TEST_CHECK_EN: Enable the pattern checker. This signal is in the memory-clock domain. When active, the checker performs a PRBS7 sequence check on the corresponding WRAP channel.

Register Name	ADR DFT Wrap Status and Control Register
Mnemonic	IOM0.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P3_ADR1
Address	8000440C07011C3F (SCOM)
Description	This register provides the status and control of the ADR wrap test for a given ADR8/12 instance. This register must only be used to perform diagnostic, manufacturing, or characterization testing. Contact your IBM representative before modifying this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	ROX	ADR_TEST_LANE_PAIR_FAIL: **Note:** Bits 48:55 of this register are read only. These bits can be reset, but they are written with a free running dphy_gckn clock. Therefore, any read of these bits returns the value from the loopback test logic. If that logic has not been reset and the error bits are cleared, this field is X. Reading this register does not automatically clear these bits. When set, these bits must be reset by asserting bit 62 of this register. For PRBS7 error detection in the memory-clock domain: Bit 0 represents the miscompare detect for wrap0 and wrap1. Bit 1 represents the miscompare detect for wrap2 and wrap3. Bit 2 represents the miscompare detect for wrap4 and wrap5. Bit 3 represents the miscompare detect for wrap6 and wrap7. Bit 4 represents the miscompare detect for wrap8 and wrap9. Reserved for ADR8. Bit 5 represents the miscompare detect for wrap10 and wrap11. Reserved for ADR8.
54:55	ROX	Reserved.
56	RW	ADR_TEST_DATA_EN: When high, this bit selects macrotest data. Otherwise, functional mode is used.
57:58	RW	ADR_TEST_MODE: These bits are reserved for manufacturing test.
59	RW	ADR_TEST_4TO1_MODE: When active, the PRBS generates a 4-bit output every cycle. Otherwise, it outputs two bits. This signal is in the memory-clock domain.
60	RW	ADR_TEST_RESET: Reset. This signal is in the memory-clock domain.
61	RW	ADR_TEST_GEN_EN: Pattern generator enable. This signal is in the memory-clock domain. This signal must be active before enabling the check_enable_i; which is 8 cycles for loading the checker plus the latency between the generator and the wrap through APIN.
62	RW	ADR_TEST_CLEAR_ERROR: Clear error bits. This signal is in the memory-clock domain. The generator must be active before clr_error_i, and the macrotest_mode_i must be selecting WRAP clocks to all the corresponding checkers' latches.
63	RW	ADR_TEST_CHECK_EN: Enable the pattern checker. This signal is in the memory-clock domain. When active, the checker performs a PRBS7 sequence check on the corresponding WRAP channel.

Register Name	**ADR I/O FET Slice Enable Map 0 Register**
Mnemonic	IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P0_ADR1
Address	800044200701103F (SCOM)
Description	Each predefined pin on the ADR can be mapped to predetermined I/O FET slice enable values to implement 30 Ω or 40 Ω drive impedance. Pins are defined by the mnemonic {{0-1}*8+n}, with n = 0 – 7. Register 0 contains lanes 0:7, and register 1 contains lanes 8:15.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48	RW	SLICE_SEL0: Select impedance values to be used for MEMINTC00O (ADR I/O FET Slice Enable Map 0) and MEMINTC08O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
49	RW	Reserved.
50	RW	SLICE_SEL1: Select impedance values to be used for MEMINTC01O (ADR I/O FET Slice Enable Map 0) and MEMINTC09O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
51	RW	Reserved.

Bits	SCOM	Field Mnemonic: Description
52	RW	SLICE_SEL2: Select impedance values to be used for MEMINTC02O (ADR I/O FET Slice Enable Map 0) and MEMINTC10O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
53	RW	Reserved.
54	RW	SLICE_SEL3: Select impedance values to be used for MEMINTC03O (ADR I/O FET Slice Enable Map 0) and MEMINTC11O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
55	RW	Reserved.
56	RW	SLICE_SEL4: Select impedance values to be used for MEMINTC04O (ADR I/O FET Slice Enable Map 0) and MEMINTC12O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
57	RW	Reserved.
58	RW	SLICE_SEL5: Select impedance values to be used for MEMINTC05O (ADR I/O FET Slice Enable Map 0) and MEMINTC13O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
59	RW	Reserved.
60	RW	SLICE_SEL6: Select impedance values to be used for MEMINTC06O (ADR I/O FET Slice Enable Map 0) and MEMINTC14O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
61	RW	Reserved.
62	RW	SLICE_SEL7: Select impedance values to be used for MEMINTC07O (ADR I/O FET Slice Enable Map 0) and MEMINTC15O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
63	RW	Reserved.

Register Name	**ADR I/O FET Slice Enable Map 0 Register**
Mnemonic	IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P1_ADR1
Address	800044200701143F (SCOM)
Description	Each predefined pin on the ADR can be mapped to predetermined I/O FET slice enable values to implement 30 Ω or 40 Ω drive impedance. Pins are defined by the mnemonic {{0-1}*8+n}, with n = 0 – 7. Register 0 contains lanes 0:7, and register 1 contains lanes 8:15.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48	RW	SLICE_SEL0: Select impedance values to be used for MEMINTC00O (ADR I/O FET Slice Enable Map 0) and MEMINTC08O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
49	RW	Reserved.

Bits	SCOM	Field Mnemonic: Description
50	RW	SLICE_SEL1: Select impedance values to be used for MEMINTC01O (ADR I/O FET Slice Enable Map 0) and MEMINTC09O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
51	RW	Reserved.
52	RW	SLICE_SEL2: Select impedance values to be used for MEMINTC02O (ADR I/O FET Slice Enable Map 0) and MEMINTC10O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
53	RW	Reserved.
54	RW	SLICE_SEL3: Select impedance values to be used for MEMINTC03O (ADR I/O FET Slice Enable Map 0) and MEMINTC11O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
55	RW	Reserved.
56	RW	SLICE_SEL4: Select impedance values to be used for MEMINTC04O (ADR I/O FET Slice Enable Map 0) and MEMINTC12O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
57	RW	Reserved.
58	RW	SLICE_SEL5: Select impedance values to be used for MEMINTC05O (ADR I/O FET Slice Enable Map 0) and MEMINTC13O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
59	RW	Reserved.
60	RW	SLICE_SEL6: Select impedance values to be used for MEMINTC06O (ADR I/O FET Slice Enable Map 0) and MEMINTC14O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
61	RW	Reserved.
62	RW	SLICE_SEL7: Select impedance values to be used for MEMINTC07O (ADR I/O FET Slice Enable Map 0) and MEMINTC15O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
63	RW	Reserved.

Register Name	**ADR I/O FET Slice Enable Map 0 Register**
Mnemonic	IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P2_ADR1
Address	800044200701183F (SCOM)
Description	Each predefined pin on the ADR can be mapped to predetermined I/O FET slice enable values to implement 30 Ω or 40 Ω drive impedance. Pins are defined by the mnemonic {{0-1}*8+n}, with n = 0 – 7. Register 0 contains lanes 0:7, and register 1 contains lanes 8:15.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RW	SLICE_SEL0: Select impedance values to be used for MEMINTC00O (ADR I/O FET Slice Enable Map 0) and MEMINTC08O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
49	RW	Reserved.
50	RW	SLICE_SEL1: Select impedance values to be used for MEMINTC01O (ADR I/O FET Slice Enable Map 0) and MEMINTC09O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
51	RW	Reserved.
52	RW	SLICE_SEL2: Select impedance values to be used for MEMINTC02O (ADR I/O FET Slice Enable Map 0) and MEMINTC10O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
53	RW	Reserved.
54	RW	SLICE_SEL3: Select impedance values to be used for MEMINTC03O (ADR I/O FET Slice Enable Map 0) and MEMINTC11O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
55	RW	Reserved.
56	RW	SLICE_SEL4: Select impedance values to be used for MEMINTC04O (ADR I/O FET Slice Enable Map 0) and MEMINTC12O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
57	RW	Reserved.
58	RW	SLICE_SEL5: Select impedance values to be used for MEMINTC05O (ADR I/O FET Slice Enable Map 0) and MEMINTC13O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
59	RW	Reserved.
60	RW	SLICE_SEL6: Select impedance values to be used for MEMINTC06O (ADR I/O FET Slice Enable Map 0) and MEMINTC14O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
61	RW	Reserved.
62	RW	SLICE_SEL7: Select impedance values to be used for MEMINTC07O (ADR I/O FET Slice Enable Map 0) and MEMINTC15O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
63	RW	Reserved.

Register Name	**ADR I/O FET Slice Enable Map 0 Register**
Mnemonic	IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P3_ADR1
Address	8000442007011C3F (SCOM)
Description	Each predefined pin on the ADR can be mapped to predetermined I/O FET slice enable values to implement 30 Ω or 40 Ω drive impedance. Pins are defined by the mnemonic {{0-1}*8+n}, with n = 0 – 7. Register 0 contains lanes 0:7, and register 1 contains lanes 8:15.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	SLICE_SEL0: Select impedance values to be used for MEMINTC00O (ADR I/O FET Slice Enable Map 0) and MEMINTC08O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
49	RW	Reserved.
50	RW	SLICE_SEL1: Select impedance values to be used for MEMINTC01O (ADR I/O FET Slice Enable Map 0) and MEMINTC09O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
51	RW	Reserved.
52	RW	SLICE_SEL2: Select impedance values to be used for MEMINTC02O (ADR I/O FET Slice Enable Map 0) and MEMINTC10O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
53	RW	Reserved.
54	RW	SLICE_SEL3: Select impedance values to be used for MEMINTC03O (ADR I/O FET Slice Enable Map 0) and MEMINTC11O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
55	RW	Reserved.
56	RW	SLICE_SEL4: Select impedance values to be used for MEMINTC04O (ADR I/O FET Slice Enable Map 0) and MEMINTC12O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
57	RW	Reserved.
58	RW	SLICE_SEL5: Select impedance values to be used for MEMINTC05O (ADR I/O FET Slice Enable Map 0) and MEMINTC13O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
59	RW	Reserved.
60	RW	SLICE_SEL6: Select impedance values to be used for MEMINTC06O (ADR I/O FET Slice Enable Map 0) and MEMINTC14O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
61	RW	Reserved.
62	RW	SLICE_SEL7: Select impedance values to be used for MEMINTC07O (ADR I/O FET Slice Enable Map 0) and MEMINTC15O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
63	RW	Reserved.

Register Name	**ADR I/O FET Slice Enable Map 1 Register**
Mnemonic	IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P0_ADR1
Address	800044210701103F (SCOM)
Description	Each predefined pin on the ADR can be mapped to predetermined I/O FET slice enable values to implement 30 Ω or 40 Ω drive impedance. Pins are defined by the mnemonic {{0-1}*8+n}, with n = 0 – 7. Register 0 contains lanes 0:7, and register 1 contains lanes 8:15.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	SLICE_SEL8: Select impedance values to be used for MEMINTC00O (ADR I/O FET Slice Enable Map 0) and MEMINTC08O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
49	RW	Reserved.
50:51	RW	SLICE_SEL9: Select one of four impedance values to be used for MEMINTC01O (ADR I/O FET Slice Enable Map 0) and MEMINTC09O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
52:53	RW	SLICE_SEL10: Select one of four impedance values to be used for MEMINTC02O (ADR I/O FET Slice Enable Map 0) and MEMINTC10O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
54:55	RW	SLICE_SEL11: Select one of four impedance values to be used for MEMINTC03O (ADR I/O FET Slice Enable Map 0) and MEMINTC11O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
56:57	RW	SLICE_SEL12: Select one of four impedance values to be used for MEMINTC04O (ADR I/O FET Slice Enable Map 0) and MEMINTC12O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
58:59	RW	SLICE_SEL13: Select one of four impedance values to be used for MEMINTC05O (ADR I/O FET Slice Enable Map 0) and MEMINTC13O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
60:61	RW	SLICE_SEL14: Select one of four impedance values to be used for MEMINTC06O (ADR I/O FET Slice Enable Map 0) and MEMINTC14O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.

Bits	SCOM	Field Mnemonic: Description
62:63	RW	SLICE_SEL15: Select one of four impedance values to be used for MEMINTC07O (ADR I/O FET Slice Enable Map 0) and MEMINTC15O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.

Register Name	ADR I/O FET Slice Enable Map 1 Register
Mnemonic	IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P1_ADR1
Address	800044210701143F (SCOM)
Description	Each predefined pin on the ADR can be mapped to predetermined I/O FET slice enable values to implement 30 Ω or 40 Ω drive impedance. Pins are defined by the mnemonic {{0-1}*8+n}, with n = 0 – 7. Register 0 contains lanes 0:7, and register 1 contains lanes 8:15.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	SLICE_SEL8: Select impedance values to be used for MEMINTC00O (ADR I/O FET Slice Enable Map 0) and MEMINTC08O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
49	RW	Reserved.
50:51	RW	SLICE_SEL9: Select one of four impedance values to be used for MEMINTC01O (ADR I/O FET Slice Enable Map 0) and MEMINTC09O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
52:53	RW	SLICE_SEL10: Select one of four impedance values to be used for MEMINTC02O (ADR I/O FET Slice Enable Map 0) and MEMINTC10O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
54:55	RW	SLICE_SEL11: Select one of four impedance values to be used for MEMINTC03O (ADR I/O FET Slice Enable Map 0) and MEMINTC11O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
56:57	RW	SLICE_SEL12: Select one of four impedance values to be used for MEMINTC04O (ADR I/O FET Slice Enable Map 0) and MEMINTC12O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
58:59	RW	SLICE_SEL13: Select one of four impedance values to be used for MEMINTC05O (ADR I/O FET Slice Enable Map 0) and MEMINTC13O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.

Bits	SCOM	Field Mnemonic: Description
60:61	RW	SLICE_SEL14: Select one of four impedance values to be used for MEMINTC06O (ADR I/O FET Slice Enable Map 0) and MEMINTC14O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
62:63	RW	SLICE_SEL15: Select one of four impedance values to be used for MEMINTC07O (ADR I/O FET Slice Enable Map 0) and MEMINTC15O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.

Register Name	**ADR I/O FET Slice Enable Map 1 Register**
Mnemonic	IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P2_ADR1
Address	800044210701183F (SCOM)
Description	Each predefined pin on the ADR can be mapped to predetermined I/O FET slice enable values to implement 30 Ω or 40 Ω drive impedance. Pins are defined by the mnemonic {{0-1}*8+n}, with n = 0 – 7. Register 0 contains lanes 0:7, and register 1 contains lanes 8:15.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48	RW	SLICE_SEL8: Select impedance values to be used for MEMINTC00O (ADR I/O FET Slice Enable Map 0) and MEMINTC08O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
49	RW	Reserved.
50:51	RW	SLICE_SEL9: Select one of four impedance values to be used for MEMINTC01O (ADR I/O FET Slice Enable Map 0) and MEMINTC09O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
52:53	RW	SLICE_SEL10: Select one of four impedance values to be used for MEMINTC02O (ADR I/O FET Slice Enable Map 0) and MEMINTC10O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
54:55	RW	SLICE_SEL11: Select one of four impedance values to be used for MEMINTC03O (ADR I/O FET Slice Enable Map 0) and MEMINTC11O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
56:57	RW	SLICE_SEL12: Select one of four impedance values to be used for MEMINTC04O (ADR I/O FET Slice Enable Map 0) and MEMINTC12O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.

Bits	SCOM	Field Mnemonic: Description
58:59	RW	SLICE_SEL13: Select one of four impedance values to be used for MEMINTC05O (ADR I/O FET Slice Enable Map 0) and MEMINTC13O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
60:61	RW	SLICE_SEL14: Select one of four impedance values to be used for MEMINTC06O (ADR I/O FET Slice Enable Map 0) and MEMINTC14O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
62:63	RW	SLICE_SEL15: Select one of four impedance values to be used for MEMINTC07O (ADR I/O FET Slice Enable Map 0) and MEMINTC15O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.

Register Name	**ADR I/O FET Slice Enable Map 1 Register**
Mnemonic	IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P3_ADR1
Address	8000442107011C3F (SCOM)
Description	Each predefined pin on the ADR can be mapped to predetermined I/O FET slice enable values to implement 30 Ω or 40 Ω drive impedance. Pins are defined by the mnemonic {{0-1}*8+n}, with n = 0 – 7. Register 0 contains lanes 0:7, and register 1 contains lanes 8:15.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	SLICE_SEL8: Select impedance values to be used for MEMINTC00O (ADR I/O FET Slice Enable Map 0) and MEMINTC08O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
49	RW	Reserved.
50:51	RW	SLICE_SEL9: Select one of four impedance values to be used for MEMINTC01O (ADR I/O FET Slice Enable Map 0) and MEMINTC09O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
52:53	RW	SLICE_SEL10: Select one of four impedance values to be used for MEMINTC02O (ADR I/O FET Slice Enable Map 0) and MEMINTC10O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
54:55	RW	SLICE_SEL11: Select one of four impedance values to be used for MEMINTC03O (ADR I/O FET Slice Enable Map 0) and MEMINTC11O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.

Bits	SCOM	Field Mnemonic: Description
56:57	RW	SLICE_SEL12: Select one of four impedance values to be used for MEMINTC04O (ADR I/O FET Slice Enable Map 0) and MEMINTC12O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
58:59	RW	SLICE_SEL13: Select one of four impedance values to be used for MEMINTC05O (ADR I/O FET Slice Enable Map 0) and MEMINTC13O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
60:61	RW	SLICE_SEL14: Select one of four impedance values to be used for MEMINTC06O (ADR I/O FET Slice Enable Map 0) and MEMINTC14O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
62:63	RW	SLICE_SEL15: Select one of four impedance values to be used for MEMINTC07O (ADR I/O FET Slice Enable Map 0) and MEMINTC15O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.

Register Name	ADR RESERVED 10 Register
Mnemonic	IOM0.DDRPHY_ADR_RESERVED10_P0_ADR1
Address	8000442A0701103F (SCOM)
Description	Currently reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	Reserved.

Register Name	ADR RESERVED 10 Register
Mnemonic	IOM0.DDRPHY_ADR_RESERVED10_P1_ADR1
Address	8000442A0701143F (SCOM)
Description	Currently reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	Reserved.

Register Name	ADR RESERVED 10 Register
Mnemonic	IOM0.DDRPHY_ADR_RESERVED10_P2_ADR1
Address	8000442A0701183F (SCOM)
Description	Currently reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	Reserved.

Register Name	ADR RESERVED 10 Register
Mnemonic	IOM0.DDRPHY_ADR_RESERVED10_P3_ADR1
Address	8000442A07011C3F (SCOM)
Description	Currently reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	Reserved.

Register Name	ADR RESERVED 11 Register
Mnemonic	IOM0.DDRPHY_ADR_RESERVED11_P0_ADR1
Address	8000442B0701103F (SCOM)
Description	Currently reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	Reserved.

Register Name	ADR RESERVED 11 Register
Mnemonic	IOM0.DDRPHY_ADR_RESERVED11_P1_ADR1
Address	8000442B0701143F (SCOM)
Description	Currently reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	Reserved.

Register Name	ADR RESERVED 11 Register
Mnemonic	IOM0.DDRPHY_ADR_RESERVED11_P2_ADR1
Address	8000442B0701183F (SCOM)
Description	Currently reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	Reserved.

Register Name	ADR RESERVED 11 Register
Mnemonic	IOM0.DDRPHY_ADR_RESERVED11_P3_ADR1
Address	8000442B07011C3F (SCOM)
Description	Currently reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	Reserved.

Register Name	ADR Power Down 2 Register
Mnemonic	IOM0.DDRPHY_ADR_POWERDOWN_2_P0_ADR1
Address	8000442C0701103F (SCOM)
Description	This register provides control of the ADR power-down modes.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:55	RW	ADR_LANE_0_7_PD: 0 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{0-7} is at high-Z (tri-stated). 1 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{0-7} drives the value programmed in bit 55 the PC Power Down 1 Register at the impedance programmed into the ADR I/O FET Slice Enable Map {0-1} Register.
56:59	RW	ADR_Lane_8_11_PD: ADR12: 0 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{8-11} is at high-Z (tri-stated). 1 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{8-11} drives the value programmed in bit 55 of PC Power Down 1 Register at the impedance programmed into the ADR I/O FET Slice Enable Map {0-1} Register. ADR8: Reserved.
60:63	RW	ADR_LANE_12_15_PD: Reserved.

Register Name	ADR Power Down 2 Register
Mnemonic	IOM0.DDRPHY_ADR_POWERDOWN_2_P1_ADR1
Address	8000442C0701143F (SCOM)
Description	This register provides control of the ADR power-down modes.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:55	RW	ADR_LANE_0_7_PD: 0 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{0-7} is at high-Z (tri-stated). 1 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{0-7} drives the value programmed in bit 55 the PC Power Down 1 Register at the impedance programmed into the ADR I/O FET Slice Enable Map {0-1} Register.
56:59	RW	ADR_Lane_8_11_PD: ADR12: 0 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{8-11} is at high-Z (tri-stated). 1 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{8-11} drives the value programmed in bit 55 of PC Power Down 1 Register at the impedance programmed into the ADR I/O FET Slice Enable Map {0-1} Register. ADR8: Reserved.
60:63	RW	ADR_LANE_12_15_PD: Reserved.

Register Name	ADR Power Down 2 Register
Mnemonic	IOM0.DDRPHY_ADR_POWERDOWN_2_P2_ADR1
Address	8000442C0701183F (SCOM)
Description	This register provides control of the ADR power-down modes.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:55	RW	ADR_LANE_0_7_PD: 0 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{0-7} is at high-Z (tri-stated). 1 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{0-7} drives the value programmed in bit 55 the PC Power Down 1 Register at the impedance programmed into the ADR I/O FET Slice Enable Map {0-1} Register.
56:59	RW	ADR_Lane_8_11_PD: ADR12: 0 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{8-11} is at high-Z (tri-stated). 1 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{8-11} drives the value programmed in bit 55 of PC Power Down 1 Register at the impedance programmed into the ADR I/O FET Slice Enable Map {0-1} Register. ADR8: Reserved.
60:63	RW	ADR_LANE_12_15_PD: Reserved.

Register Name	ADR Power Down 2 Register
Mnemonic	IOM0.DDRPHY_ADR_POWERDOWN_2_P3_ADR1
Address	8000442C07011C3F (SCOM)
Description	This register provides control of the ADR power-down modes.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:55	RW	ADR_LANE_0_7_PD: 0 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{0-7} is at high-Z (tri-stated). 1 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{0-7} drives the value programmed in bit 55 the PC Power Down 1 Register at the impedance programmed into the ADR I/O FET Slice Enable Map {0-1} Register.
56:59	RW	ADR_Lane_8_11_PD: ADR12: 0 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{8-11} is at high-Z (tri-stated). 1 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{8-11} drives the value programmed in bit 55 of PC Power Down 1 Register at the impedance programmed into the ADR I/O FET Slice Enable Map {0-1} Register. ADR8: Reserved.
60:63	RW	ADR_LANE_12_15_PD: Reserved.

Register Name	ADR Bit Enable Register
Mnemonic	IOM0.DDRPHY_ADR_BIT_ENABLE_P0_ADR2
Address	800048000701103F (SCOM)
Description	An ADR12 has 12 possible outputs, and an ADR8 has 8 possible outputs. This register is used to enable and disable each of the 12 pins or 8 pins. Any pins used on an ADR must be enabled via this register. The pins on an ADR can be used to send clocks or control (command, address, and so on) signals to memory devices.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:59	RW	BIT_ENABLE_0_11: 1 = Indicates that the ADR bit is enabled and is used for sending clocks or control (command, address, and so on) signals to the memory device. 0 = Indicates that the ADR bit is not used and not enabled. Bit 0 controls MEMINTC00O(n). Bit 1 controls MEMINTC01O(n). Bit 2 controls MEMINTC02O(n). ... Bit 11 controls MEMINTC11O(n). where n is the ADR instance number. ADR12 uses bits 48:59. ADR8 uses bits 48:55, with bits 56:59 reserved.
60:63	RW	Reserved.

Register Name	ADR Bit Enable Register
Mnemonic	IOM0.DDRPHY_ADR_BIT_ENABLE_P1_ADR2
Address	800048000701143F (SCOM)
Description	An ADR12 has 12 possible outputs, and an ADR8 has 8 possible outputs. This register is used to enable and disable each of the 12 pins or 8 pins. Any pins used on an ADR must be enabled via this register. The pins on an ADR can be used to send clocks or control (command, address, and so on) signals to memory devices.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:59	RW	BIT_ENABLE_0_11: 1 = Indicates that the ADR bit is enabled and is used for sending clocks or control (command, address, and so on) signals to the memory device. 0 = Indicates that the ADR bit is not used and not enabled. Bit 0 controls MEMINTC00O(n). Bit 1 controls MEMINTC01O(n). Bit 2 controls MEMINTC02O(n). ... Bit 11 controls MEMINTC11O(n). where n is the ADR instance number. ADR12 uses bits 48:59. ADR8 uses bits 48:55, with bits 56:59 reserved.
60:63	RW	Reserved.

Register Name	ADR Bit Enable Register
Mnemonic	IOM0.DDRPHY_ADR_BIT_ENABLE_P2_ADR2
Address	800048000701183F (SCOM)
Description	An ADR12 has 12 possible outputs, and an ADR8 has 8 possible outputs. This register is used to enable and disable each of the 12 pins or 8 pins. Any pins used on an ADR must be enabled via this register. The pins on an ADR can be used to send clocks or control (command, address, and so on) signals to memory devices.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:59	RW	BIT_ENABLE_0_11: 1 = Indicates that the ADR bit is enabled and is used for sending clocks or control (command, address, and so on) signals to the memory device. 0 = Indicates that the ADR bit is not used and not enabled. Bit 0 controls MEMINTC00O(n). Bit 1 controls MEMINTC01O(n). Bit 2 controls MEMINTC02O(n). ... Bit 11 controls MEMINTC11O(n). where n is the ADR instance number. ADR12 uses bits 48:59. ADR8 uses bits 48:55, with bits 56:59 reserved.
60:63	RW	Reserved.

Register Name	ADR Bit Enable Register
Mnemonic	IOM0.DDRPHY_ADR_BIT_ENABLE_P3_ADR2
Address	8000480007011C3F (SCOM)
Description	An ADR12 has 12 possible outputs, and an ADR8 has 8 possible outputs. This register is used to enable and disable each of the 12 pins or 8 pins. Any pins used on an ADR must be enabled via this register. The pins on an ADR can be used to send clocks or control (command, address, and so on) signals to memory devices.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:59	RW	BIT_ENABLE_0_11: 1 = Indicates that the ADR bit is enabled and is used for sending clocks or control (command, address, and so on) signals to the memory device. 0 = Indicates that the ADR bit is not used and not enabled. Bit 0 controls MEMINTC00O(n). Bit 1 controls MEMINTC01O(n). Bit 2 controls MEMINTC02O(n). ... Bit 11 controls MEMINTC11O(n). where n is the ADR instance number. ADR12 uses bits 48:59. ADR8 uses bits 48:55, with bits 56:59 reserved.
60:63	RW	Reserved.

Register Name	ADR Differential Pair Enable Register
Mnemonic	IOM0.DDRPHY_ADR_DIFFPAIR_ENABLE_P0_ADR2
Address	800048010701103F (SCOM)
Description	An ADR12 has 12 possible outputs, and an ADR8 has 8 possible outputs, any of which can be paired together for memory clock generation (CK/CK#). This register is used to enable or disable each pair of ADR pins to be used as differential outputs or as two single-ended outputs. When a pair of ADR pins is configured as a differential output, the delays associated with both outputs of the differential pair must be programmed to the same value in the ADR Delay Value {0-7} Registers for that pair. When a pair of ADR pins is enabled as a differential pair in this register, both of the pins must be enabled in the ADR Bit Enable Register. When a pair of ADR pins is enabled as a differential pair in this register, the even-numbered pin is the true, and the odd-numbered pin is the complement signal.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	DI_ADR0_ADR1: 0 = Lanes 0 and 1 are not a differential clock pair. 1 = Lanes 0 and 1 are a differential clock pair.
49	RW	DI_ADR2_ADR3: 0 = Lanes 2 and 3 are not a differential clock pair. 1 = Lanes 2 and 3 are a differential clock pair.
50	RW	DI_ADR4_ADR5: 0 = Lanes 4 and 5 are not a differential clock pair. 1 = Lanes 4 and 5 are a differential clock pair.
51	RW	DI_ADR6_ADR7: 0 = Lanes 6 and 7 are not a differential clock pair. 1 = Lanes 6 and 7 are a differential clock pair.

Bits	SCOM	Field Mnemonic: Description
52	RW	DI_ADR8_ADR9: 0 = Lanes 8 and 9 are not a differential clock pair. 1 = Lanes 8 and 9 are a differential clock pair. Reserved for ADR8.
53	RW	DI_ADR10_ADR11: 0 = Lanes 10 and 11 are not a differential clock pair. 1 = Lanes 10 and 11 are a differential clock pair. Reserved for ADR8.
54:63	RW	Reserved.

Register Name	ADR Differential Pair Enable Register
Mnemonic	IOM0.DDRPHY_ADR_DIFFPAIR_ENABLE_P1_ADR2
Address	800048010701143F (SCOM)
Description	An ADR12 has 12 possible outputs, and an ADR8 has 8 possible outputs, any of which can be paired together for memory clock generation (CK/CK#). This register is used to enable or disable each pair of ADR pins to be used as differential outputs or as two single-ended outputs. When a pair of ADR pins is configured as a differential output, the delays associated with both outputs of the differential pair must be programmed to the same value in the ADR Delay Value {0-7} Registers for that pair. When a pair of ADR pins is enabled as a differential pair in this register, both of the pins must be enabled in the ADR Bit Enable Register. When a pair of ADR pins is enabled as a differential pair in this register, the even-numbered pin is the true, and the odd-numbered pin is the complement signal.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	DI_ADR0_ADR1: 0 = Lanes 0 and 1 are not a differential clock pair. 1 = Lanes 0 and 1 are a differential clock pair.
49	RW	DI_ADR2_ADR3: 0 = Lanes 2 and 3 are not a differential clock pair. 1 = Lanes 2 and 3 are a differential clock pair.
50	RW	DI_ADR4_ADR5: 0 = Lanes 4 and 5 are not a differential clock pair. 1 = Lanes 4 and 5 are a differential clock pair.
51	RW	DI_ADR6_ADR7: 0 = Lanes 6 and 7 are not a differential clock pair. 1 = Lanes 6 and 7 are a differential clock pair.
52	RW	DI_ADR8_ADR9: 0 = Lanes 8 and 9 are not a differential clock pair. 1 = Lanes 8 and 9 are a differential clock pair. Reserved for ADR8.
53	RW	DI_ADR10_ADR11: 0 = Lanes 10 and 11 are not a differential clock pair. 1 = Lanes 10 and 11 are a differential clock pair. Reserved for ADR8.
54:63	RW	Reserved.

Register Name	ADR Differential Pair Enable Register
Mnemonic	IOM0.DDRPHY_ADR_DIFFPAIR_ENABLE_P2_ADR2
Address	800048010701183F (SCOM)
Description	An ADR12 has 12 possible outputs, and an ADR8 has 8 possible outputs, any of which can be paired together for memory clock generation (CK/CK#). This register is used to enable or disable each pair of ADR pins to be used as differential outputs or as two single-ended outputs. When a pair of ADR pins is configured as a differential output, the delays associated with both outputs of the differential pair must be programmed to the same value in the ADR Delay Value {0-7} Registers for that pair. When a pair of ADR pins is enabled as a differential pair in this register, both of the pins must be enabled in the ADR Bit Enable Register. When a pair of ADR pins is enabled as a differential pair in this register, the even-numbered pin is the true, and the odd-numbered pin is the complement signal.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	DI_ADR0_ADR1: 0 = Lanes 0 and 1 are not a differential clock pair. 1 = Lanes 0 and 1 are a differential clock pair.
49	RW	DI_ADR2_ADR3: 0 = Lanes 2 and 3 are not a differential clock pair. 1 = Lanes 2 and 3 are a differential clock pair.
50	RW	DI_ADR4_ADR5: 0 = Lanes 4 and 5 are not a differential clock pair. 1 = Lanes 4 and 5 are a differential clock pair.
51	RW	DI_ADR6_ADR7: 0 = Lanes 6 and 7 are not a differential clock pair. 1 = Lanes 6 and 7 are a differential clock pair.
52	RW	DI_ADR8_ADR9: 0 = Lanes 8 and 9 are not a differential clock pair. 1 = Lanes 8 and 9 are a differential clock pair. Reserved for ADR8.
53	RW	DI_ADR10_ADR11: 0 = Lanes 10 and 11 are not a differential clock pair. 1 = Lanes 10 and 11 are a differential clock pair. Reserved for ADR8.
54:63	RW	Reserved.

Register Name	ADR Differential Pair Enable Register
Mnemonic	IOM0.DDRPHY_ADR_DIFFPAIR_ENABLE_P3_ADR2
Address	8000480107011C3F (SCOM)
Description	An ADR12 has 12 possible outputs, and an ADR8 has 8 possible outputs, any of which can be paired together for memory clock generation (CK/CK#). This register is used to enable or disable each pair of ADR pins to be used as differential outputs or as two single-ended outputs. When a pair of ADR pins is configured as a differential output, the delays associated with both outputs of the differential pair must be programmed to the same value in the ADR Delay Value {0-7} Registers for that pair. When a pair of ADR pins is enabled as a differential pair in this register, both of the pins must be enabled in the ADR Bit Enable Register. When a pair of ADR pins is enabled as a differential pair in this register, the even-numbered pin is the true, and the odd-numbered pin is the complement signal.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RW	DI_ADR0_ADR1: 0 = Lanes 0 and 1 are not a differential clock pair. 1 = Lanes 0 and 1 are a differential clock pair.
49	RW	DI_ADR2_ADR3: 0 = Lanes 2 and 3 are not a differential clock pair. 1 = Lanes 2 and 3 are a differential clock pair.
50	RW	DI_ADR4_ADR5: 0 = Lanes 4 and 5 are not a differential clock pair. 1 = Lanes 4 and 5 are a differential clock pair.
51	RW	DI_ADR6_ADR7: 0 = Lanes 6 and 7 are not a differential clock pair. 1 = Lanes 6 and 7 are a differential clock pair.
52	RW	DI_ADR8_ADR9: 0 = Lanes 8 and 9 are not a differential clock pair. 1 = Lanes 8 and 9 are a differential clock pair. Reserved for ADR8.
53	RW	DI_ADR10_ADR11: 0 = Lanes 10 and 11 are not a differential clock pair. 1 = Lanes 10 and 11 are a differential clock pair. Reserved for ADR8.
54:63	RW	Reserved.

Register Name	**ADR Delay Value 0 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY0_P0_ADR2
Address	800048040701103F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY0: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY1: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 0 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY0_P1_ADR2
Address	800048040701143F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY0: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY1: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 0 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY0_P2_ADR2
Address	800048040701183F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY0: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY1: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 0 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY0_P3_ADR2
Address	8000480407011C3F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY0: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY1: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 1 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY1_P0_ADR2
Address	800048050701103F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY2: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY3: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 1 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY1_P1_ADR2
Address	800048050701143F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY2: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY3: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 1 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY1_P2_ADR2
Address	800048050701183F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY2: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY3: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 1 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY1_P3_ADR2
Address	8000480507011C3F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY2: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY3: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 2 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY2_P0_ADR2
Address	800048060701103F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY4: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY5: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 2 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY2_P1_ADR2
Address	800048060701143F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY4: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY5: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 2 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY2_P2_ADR2
Address	800048060701183F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY4: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY5: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 2 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY2_P3_ADR2
Address	8000480607011C3F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY4: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY5: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 3 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY3_P0_ADR2
Address	800048070701103F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY6: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY7: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 3 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY3_P1_ADR2
Address	800048070701143F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY6: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY7: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 3 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY3_P2_ADR2
Address	800048070701183F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY6: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY7: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 3 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY3_P3_ADR2
Address	8000480707011C3F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY6: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY7: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 4 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY4_P0_ADR2
Address	800048080701103F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY8: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY9: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 4 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY4_P1_ADR2
Address	800048080701143F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY8: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY9: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 4 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY4_P2_ADR2
Address	800048080701183F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY8: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY9: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 4 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY4_P3_ADR2
Address	8000480807011C3F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY8: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY9: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 5 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY5_P0_ADR2
Address	800048090701103F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY10: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY11: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 5 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY5_P1_ADR2
Address	800048090701143F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY10: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY11: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 5 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY5_P2_ADR2
Address	800048090701183F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY10: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY11: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 5 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY5_P3_ADR2
Address	8000480907011C3F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY10: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY11: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 6 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY6_P0_ADR2
Address	8000480A0701103F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY12: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY13: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 6 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY6_P1_ADR2
Address	8000480A0701143F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY12: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY13: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 6 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY6_P2_ADR2
Address	8000480A0701183F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY12: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY13: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 6 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY6_P3_ADR2
Address	8000480A07011C3F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY12: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY13: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 7 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY7_P0_ADR2
Address	8000480B0701103F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY14: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY15: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 7 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY7_P1_ADR2
Address	8000480B0701143F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY14: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY15: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 7 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY7_P2_ADR2
Address	8000480B0701183F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY14: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY15: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 7 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY7_P3_ADR2
Address	8000480B07011C3F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY14: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY15: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR DFT Wrap Status and Control Register
Mnemonic	IOM0.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P0_ADR2
Address	8000480C0701103F (SCOM)
Description	This register provides the status and control of the ADR wrap test for a given ADR8/12 instance. This register must only be used to perform diagnostic, manufacturing, or characterization testing. Contact your IBM representative before modifying this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:53	ROX	ADR_TEST_LANE_PAIR_FAIL: **Note:** Bits 48:55 of this register are read only. These bits can be reset, but they are written with a free running dphy_gckn clock. Therefore, any read of these bits returns the value from the loopback test logic. If that logic has not been reset and the error bits are cleared, this field is X. Reading this register does not automatically clear these bits. When set, these bits must be reset by asserting bit 62 of this register. For PRBS7 error detection in the memory-clock domain: Bit 0 represents the miscompare detect for wrap0 and wrap1. Bit 1 represents the miscompare detect for wrap2 and wrap3. Bit 2 represents the miscompare detect for wrap4 and wrap5. Bit 3 represents the miscompare detect for wrap6 and wrap7. Bit 4 represents the miscompare detect for wrap8 and wrap9. Reserved for ADR8. Bit 5 represents the miscompare detect for wrap10 and wrap11. Reserved for ADR8.
54:55	ROX	Reserved.
56	RW	ADR_TEST_DATA_EN: When high, this bit selects macrotest data. Otherwise, functional mode is used.
57:58	RW	ADR_TEST_MODE: These bits are reserved for manufacturing test.
59	RW	ADR_TEST_4TO1_MODE: When active, the PRBS generates a 4-bit output every cycle. Otherwise, it outputs two bits. This signal is in the memory-clock domain.
60	RW	ADR_TEST_RESET: Reset. This signal is in the memory-clock domain.
61	RW	ADR_TEST_GEN_EN: Pattern generator enable. This signal is in the memory-clock domain. This signal must be active before enabling the check_enable_i; which is 8 cycles for loading the checker plus the latency between the generator and the wrap through APIN.

Bits	SCOM	Field Mnemonic: Description
62	RW	ADR_TEST_CLEAR_ERROR: Clear error bits. This signal is in the memory-clock domain. The generator must be active before clr_error_i, and the macrotest_mode_i must be selecting WRAP clocks to all the corresponding checkers' latches.
63	RW	ADR_TEST_CHECK_EN: Enable the pattern checker. This signal is in the memory-clock domain. When active, the checker performs a PRBS7 sequence check on the corresponding WRAP channel.

Register Name	**ADR DFT Wrap Status and Control Register**
Mnemonic	IOM0.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P1_ADR2
Address	8000480C0701143F (SCOM)
Description	This register provides the status and control of the ADR wrap test for a given ADR8/12 instance. This register must only be used to perform diagnostic, manufacturing, or characterization testing. Contact your IBM representative before modifying this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:53	ROX	ADR_TEST_LANE_PAIR_FAIL: **Note:** Bits 48:55 of this register are read only. These bits can be reset, but they are written with a free running dphy_gckn clock. Therefore, any read of these bits returns the value from the loopback test logic. If that logic has not been reset and the error bits are cleared, this field is X. Reading this register does not automatically clear these bits. When set, these bits must be reset by asserting bit 62 of this register. For PRBS7 error detection in the memory-clock domain: Bit 0 represents the miscompare detect for wrap0 and wrap1. Bit 1 represents the miscompare detect for wrap2 and wrap3. Bit 2 represents the miscompare detect for wrap4 and wrap5. Bit 3 represents the miscompare detect for wrap6 and wrap7. Bit 4 represents the miscompare detect for wrap8 and wrap9. Reserved for ADR8. Bit 5 represents the miscompare detect for wrap10 and wrap11. Reserved for ADR8.
54:55	ROX	Reserved.
56	RW	ADR_TEST_DATA_EN: When high, this bit selects macrotest data. Otherwise, functional mode is used.
57:58	RW	ADR_TEST_MODE: These bits are reserved for manufacturing test.
59	RW	ADR_TEST_4TO1_MODE: When active, the PRBS generates a 4-bit output every cycle. Otherwise, it outputs two bits. This signal is in the memory-clock domain.
60	RW	ADR_TEST_RESET: Reset. This signal is in the memory-clock domain.
61	RW	ADR_TEST_GEN_EN: Pattern generator enable. This signal is in the memory-clock domain. This signal must be active before enabling the check_enable_i; which is 8 cycles for loading the checker plus the latency between the generator and the wrap through APIN.
62	RW	ADR_TEST_CLEAR_ERROR: Clear error bits. This signal is in the memory-clock domain. The generator must be active before clr_error_i, and the macrotest_mode_i must be selecting WRAP clocks to all the corresponding checkers' latches.
63	RW	ADR_TEST_CHECK_EN: Enable the pattern checker. This signal is in the memory-clock domain. When active, the checker performs a PRBS7 sequence check on the corresponding WRAP channel.

Register Name	ADR DFT Wrap Status and Control Register
Mnemonic	IOM0.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P2_ADR2
Address	8000480C0701183F (SCOM)
Description	This register provides the status and control of the ADR wrap test for a given ADR8/12 instance. This register must only be used to perform diagnostic, manufacturing, or characterization testing. Contact your IBM representative before modifying this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:53	ROX	ADR_TEST_LANE_PAIR_FAIL: **Note:** Bits 48:55 of this register are read only. These bits can be reset, but they are written with a free running dphy_gckn clock. Therefore, any read of these bits returns the value from the loopback test logic. If that logic has not been reset and the error bits are cleared, this field is X. Reading this register does not automatically clear these bits. When set, these bits must be reset by asserting bit 62 of this register. For PRBS7 error detection in the memory-clock domain: Bit 0 represents the miscompare detect for wrap0 and wrap1. Bit 1 represents the miscompare detect for wrap2 and wrap3. Bit 2 represents the miscompare detect for wrap4 and wrap5. Bit 3 represents the miscompare detect for wrap6 and wrap7. Bit 4 represents the miscompare detect for wrap8 and wrap9. Reserved for ADR8. Bit 5 represents the miscompare detect for wrap10 and wrap11. Reserved for ADR8.
54:55	ROX	Reserved.
56	RW	ADR_TEST_DATA_EN: When high, this bit selects macrotest data. Otherwise, functional mode is used.
57:58	RW	ADR_TEST_MODE: These bits are reserved for manufacturing test.
59	RW	ADR_TEST_4TO1_MODE: When active, the PRBS generates a 4-bit output every cycle. Otherwise, it outputs two bits. This signal is in the memory-clock domain.
60	RW	ADR_TEST_RESET: Reset. This signal is in the memory-clock domain.
61	RW	ADR_TEST_GEN_EN: Pattern generator enable. This signal is in the memory-clock domain. This signal must be active before enabling the check_enable_i; which is 8 cycles for loading the checker plus the latency between the generator and the wrap through APIN.
62	RW	ADR_TEST_CLEAR_ERROR: Clear error bits. This signal is in the memory-clock domain. The generator must be active before clr_error_i, and the macrotest_mode_i must be selecting WRAP clocks to all the corresponding checkers' latches.
63	RW	ADR_TEST_CHECK_EN: Enable the pattern checker. This signal is in the memory-clock domain. When active, the checker performs a PRBS7 sequence check on the corresponding WRAP channel.

Register Name	ADR DFT Wrap Status and Control Register
Mnemonic	IOM0.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P3_ADR2
Address	8000480C07011C3F (SCOM)
Description	This register provides the status and control of the ADR wrap test for a given ADR8/12 instance. This register must only be used to perform diagnostic, manufacturing, or characterization testing. Contact your IBM representative before modifying this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	ROX	ADR_TEST_LANE_PAIR_FAIL: **Note:** Bits 48:55 of this register are read only. These bits can be reset, but they are written with a free running dphy_gckn clock. Therefore, any read of these bits returns the value from the loopback test logic. If that logic has not been reset and the error bits are cleared, this field is X. Reading this register does not automatically clear these bits. When set, these bits must be reset by asserting bit 62 of this register. For PRBS7 error detection in the memory-clock domain: Bit 0 represents the miscompare detect for wrap0 and wrap1. Bit 1 represents the miscompare detect for wrap2 and wrap3. Bit 2 represents the miscompare detect for wrap4 and wrap5. Bit 3 represents the miscompare detect for wrap6 and wrap7. Bit 4 represents the miscompare detect for wrap8 and wrap9. Reserved for ADR8. Bit 5 represents the miscompare detect for wrap10 and wrap11. Reserved for ADR8.
54:55	ROX	Reserved.
56	RW	ADR_TEST_DATA_EN: When high, this bit selects macrotest data. Otherwise, functional mode is used.
57:58	RW	ADR_TEST_MODE: These bits are reserved for manufacturing test.
59	RW	ADR_TEST_4TO1_MODE: When active, the PRBS generates a 4-bit output every cycle. Otherwise, it outputs two bits. This signal is in the memory-clock domain.
60	RW	ADR_TEST_RESET: Reset. This signal is in the memory-clock domain.
61	RW	ADR_TEST_GEN_EN: Pattern generator enable. This signal is in the memory-clock domain. This signal must be active before enabling the check_enable_i; which is 8 cycles for loading the checker plus the latency between the generator and the wrap through APIN.
62	RW	ADR_TEST_CLEAR_ERROR: Clear error bits. This signal is in the memory-clock domain. The generator must be active before clr_error_i, and the macrotest_mode_i must be selecting WRAP clocks to all the corresponding checkers' latches.
63	RW	ADR_TEST_CHECK_EN: Enable the pattern checker. This signal is in the memory-clock domain. When active, the checker performs a PRBS7 sequence check on the corresponding WRAP channel.

Register Name	**ADR I/O FET Slice Enable Map 0 Register**
Mnemonic	IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P0_ADR2
Address	800048200701103F (SCOM)
Description	Each predefined pin on the ADR can be mapped to predetermined I/O FET slice enable values to implement 30 Ω or 40 Ω drive impedance. Pins are defined by the mnemonic {{0-1}*8+n}, with n = 0 – 7. Register 0 contains lanes 0:7, and register 1 contains lanes 8:15.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	SLICE_SEL0: Select impedance values to be used for MEMINTC00O (ADR I/O FET Slice Enable Map 0) and MEMINTC08O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
49	RW	Reserved.
50	RW	SLICE_SEL1: Select impedance values to be used for MEMINTC01O (ADR I/O FET Slice Enable Map 0) and MEMINTC09O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
51	RW	Reserved.

Bits	SCOM	Field Mnemonic: Description
52	RW	SLICE_SEL2: Select impedance values to be used for MEMINTC02O (ADR I/O FET Slice Enable Map 0) and MEMINTC10O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
53	RW	Reserved.
54	RW	SLICE_SEL3: Select impedance values to be used for MEMINTC03O (ADR I/O FET Slice Enable Map 0) and MEMINTC11O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
55	RW	Reserved.
56	RW	SLICE_SEL4: Select impedance values to be used for MEMINTC04O (ADR I/O FET Slice Enable Map 0) and MEMINTC12O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
57	RW	Reserved.
58	RW	SLICE_SEL5: Select impedance values to be used for MEMINTC05O (ADR I/O FET Slice Enable Map 0) and MEMINTC13O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
59	RW	Reserved.
60	RW	SLICE_SEL6: Select impedance values to be used for MEMINTC06O (ADR I/O FET Slice Enable Map 0) and MEMINTC14O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
61	RW	Reserved.
62	RW	SLICE_SEL7: Select impedance values to be used for MEMINTC07O (ADR I/O FET Slice Enable Map 0) and MEMINTC15O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
63	RW	Reserved.

Register Name	**ADR I/O FET Slice Enable Map 0 Register**
Mnemonic	IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P1_ADR2
Address	800048200701143F (SCOM)
Description	Each predefined pin on the ADR can be mapped to predetermined I/O FET slice enable values to implement 30 Ω or 40 Ω drive impedance. Pins are defined by the mnemonic {{0-1}*8+n}, with n = 0 – 7. Register 0 contains lanes 0:7, and register 1 contains lanes 8:15.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48	RW	SLICE_SEL0: Select impedance values to be used for MEMINTC00O (ADR I/O FET Slice Enable Map 0) and MEMINTC08O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
49	RW	Reserved.

Bits	SCOM	Field Mnemonic: Description
50	RW	SLICE_SEL1: Select impedance values to be used for MEMINTC01O (ADR I/O FET Slice Enable Map 0) and MEMINTC09O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
51	RW	Reserved.
52	RW	SLICE_SEL2: Select impedance values to be used for MEMINTC02O (ADR I/O FET Slice Enable Map 0) and MEMINTC10O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
53	RW	Reserved.
54	RW	SLICE_SEL3: Select impedance values to be used for MEMINTC03O (ADR I/O FET Slice Enable Map 0) and MEMINTC11O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
55	RW	Reserved.
56	RW	SLICE_SEL4: Select impedance values to be used for MEMINTC04O (ADR I/O FET Slice Enable Map 0) and MEMINTC12O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
57	RW	Reserved.
58	RW	SLICE_SEL5: Select impedance values to be used for MEMINTC05O (ADR I/O FET Slice Enable Map 0) and MEMINTC13O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
59	RW	Reserved.
60	RW	SLICE_SEL6: Select impedance values to be used for MEMINTC06O (ADR I/O FET Slice Enable Map 0) and MEMINTC14O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
61	RW	Reserved.
62	RW	SLICE_SEL7: Select impedance values to be used for MEMINTC07O (ADR I/O FET Slice Enable Map 0) and MEMINTC15O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
63	RW	Reserved.

Register Name	**ADR I/O FET Slice Enable Map 0 Register**
Mnemonic	IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P2_ADR2
Address	800048200701183F (SCOM)
Description	Each predefined pin on the ADR can be mapped to predetermined I/O FET slice enable values to implement 30 Ω or 40 Ω drive impedance. Pins are defined by the mnemonic {{0-1}*8+n}, with n = 0 – 7. Register 0 contains lanes 0:7, and register 1 contains lanes 8:15.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RW	SLICE_SEL0: Select impedance values to be used for MEMINTC00O (ADR I/O FET Slice Enable Map 0) and MEMINTC08O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
49	RW	Reserved.
50	RW	SLICE_SEL1: Select impedance values to be used for MEMINTC01O (ADR I/O FET Slice Enable Map 0) and MEMINTC09O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
51	RW	Reserved.
52	RW	SLICE_SEL2: Select impedance values to be used for MEMINTC02O (ADR I/O FET Slice Enable Map 0) and MEMINTC10O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
53	RW	Reserved.
54	RW	SLICE_SEL3: Select impedance values to be used for MEMINTC03O (ADR I/O FET Slice Enable Map 0) and MEMINTC11O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
55	RW	Reserved.
56	RW	SLICE_SEL4: Select impedance values to be used for MEMINTC04O (ADR I/O FET Slice Enable Map 0) and MEMINTC12O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
57	RW	Reserved.
58	RW	SLICE_SEL5: Select impedance values to be used for MEMINTC05O (ADR I/O FET Slice Enable Map 0) and MEMINTC13O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
59	RW	Reserved.
60	RW	SLICE_SEL6: Select impedance values to be used for MEMINTC06O (ADR I/O FET Slice Enable Map 0) and MEMINTC14O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
61	RW	Reserved.
62	RW	SLICE_SEL7: Select impedance values to be used for MEMINTC07O (ADR I/O FET Slice Enable Map 0) and MEMINTC15O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
63	RW	Reserved.

Register Name	**ADR I/O FET Slice Enable Map 0 Register**
Mnemonic	IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P3_ADR2
Address	8000482007011C3F (SCOM)
Description	Each predefined pin on the ADR can be mapped to predetermined I/O FET slice enable values to implement 30 Ω or 40 Ω drive impedance. Pins are defined by the mnemonic {{0-1}*8+n}, with n = 0 – 7. Register 0 contains lanes 0:7, and register 1 contains lanes 8:15.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	SLICE_SEL0: Select impedance values to be used for MEMINTC00O (ADR I/O FET Slice Enable Map 0) and MEMINTC08O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
49	RW	Reserved.
50	RW	SLICE_SEL1: Select impedance values to be used for MEMINTC01O (ADR I/O FET Slice Enable Map 0) and MEMINTC09O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
51	RW	Reserved.
52	RW	SLICE_SEL2: Select impedance values to be used for MEMINTC02O (ADR I/O FET Slice Enable Map 0) and MEMINTC10O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
53	RW	Reserved.
54	RW	SLICE_SEL3: Select impedance values to be used for MEMINTC03O (ADR I/O FET Slice Enable Map 0) and MEMINTC11O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
55	RW	Reserved.
56	RW	SLICE_SEL4: Select impedance values to be used for MEMINTC04O (ADR I/O FET Slice Enable Map 0) and MEMINTC12O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
57	RW	Reserved.
58	RW	SLICE_SEL5: Select impedance values to be used for MEMINTC05O (ADR I/O FET Slice Enable Map 0) and MEMINTC13O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
59	RW	Reserved.
60	RW	SLICE_SEL6: Select impedance values to be used for MEMINTC06O (ADR I/O FET Slice Enable Map 0) and MEMINTC14O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
61	RW	Reserved.
62	RW	SLICE_SEL7: Select impedance values to be used for MEMINTC07O (ADR I/O FET Slice Enable Map 0) and MEMINTC15O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
63	RW	Reserved.

Register Name	**ADR I/O FET Slice Enable Map 1 Register**
Mnemonic	IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P0_ADR2
Address	800048210701103F (SCOM)
Description	Each predefined pin on the ADR can be mapped to predetermined I/O FET slice enable values to implement 30 Ω or 40 Ω drive impedance. Pins are defined by the mnemonic {{0-1}*8+n}, with n = 0 – 7. Register 0 contains lanes 0:7, and register 1 contains lanes 8:15.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	SLICE_SEL8: Select impedance values to be used for MEMINTC00O (ADR I/O FET Slice Enable Map 0) and MEMINTC08O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
49	RW	Reserved.
50:51	RW	SLICE_SEL9: Select one of four impedance values to be used for MEMINTC01O (ADR I/O FET Slice Enable Map 0) and MEMINTC09O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
52:53	RW	SLICE_SEL10: Select one of four impedance values to be used for MEMINTC02O (ADR I/O FET Slice Enable Map 0) and MEMINTC10O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
54:55	RW	SLICE_SEL11: Select one of four impedance values to be used for MEMINTC03O (ADR I/O FET Slice Enable Map 0) and MEMINTC11O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
56:57	RW	SLICE_SEL12: Select one of four impedance values to be used for MEMINTC04O (ADR I/O FET Slice Enable Map 0) and MEMINTC12O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
58:59	RW	SLICE_SEL13: Select one of four impedance values to be used for MEMINTC05O (ADR I/O FET Slice Enable Map 0) and MEMINTC13O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
60:61	RW	SLICE_SEL14: Select one of four impedance values to be used for MEMINTC06O (ADR I/O FET Slice Enable Map 0) and MEMINTC14O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.

Bits	SCOM	Field Mnemonic: Description
62:63	RW	SLICE_SEL15: Select one of four impedance values to be used for MEMINTC07O (ADR I/O FET Slice Enable Map 0) and MEMINTC15O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.

Register Name	ADR I/O FET Slice Enable Map 1 Register
Mnemonic	IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P1_ADR2
Address	800048210701143F (SCOM)
Description	Each predefined pin on the ADR can be mapped to predetermined I/O FET slice enable values to implement 30 Ω or 40 Ω drive impedance. Pins are defined by the mnemonic {{0-1}*8+n}, with n = 0 – 7. Register 0 contains lanes 0:7, and register 1 contains lanes 8:15.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	SLICE_SEL8: Select impedance values to be used for MEMINTC00O (ADR I/O FET Slice Enable Map 0) and MEMINTC08O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
49	RW	Reserved.
50:51	RW	SLICE_SEL9: Select one of four impedance values to be used for MEMINTC01O (ADR I/O FET Slice Enable Map 0) and MEMINTC09O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
52:53	RW	SLICE_SEL10: Select one of four impedance values to be used for MEMINTC02O (ADR I/O FET Slice Enable Map 0) and MEMINTC10O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
54:55	RW	SLICE_SEL11: Select one of four impedance values to be used for MEMINTC03O (ADR I/O FET Slice Enable Map 0) and MEMINTC11O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
56:57	RW	SLICE_SEL12: Select one of four impedance values to be used for MEMINTC04O (ADR I/O FET Slice Enable Map 0) and MEMINTC12O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
58:59	RW	SLICE_SEL13: Select one of four impedance values to be used for MEMINTC05O (ADR I/O FET Slice Enable Map 0) and MEMINTC13O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.

Bits	SCOM	Field Mnemonic: Description
60:61	RW	SLICE_SEL14: Select one of four impedance values to be used for MEMINTC06O (ADR I/O FET Slice Enable Map 0) and MEMINTC14O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
62:63	RW	SLICE_SEL15: Select one of four impedance values to be used for MEMINTC07O (ADR I/O FET Slice Enable Map 0) and MEMINTC15O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.

Register Name	**ADR I/O FET Slice Enable Map 1 Register**
Mnemonic	IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P2_ADR2
Address	800048210701183F (SCOM)
Description	Each predefined pin on the ADR can be mapped to predetermined I/O FET slice enable values to implement 30 Ω or 40 Ω drive impedance. Pins are defined by the mnemonic {{0-1}*8+n}, with n = 0 – 7. Register 0 contains lanes 0:7, and register 1 contains lanes 8:15.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48	RW	SLICE_SEL8: Select impedance values to be used for MEMINTC00O (ADR I/O FET Slice Enable Map 0) and MEMINTC08O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
49	RW	Reserved.
50:51	RW	SLICE_SEL9: Select one of four impedance values to be used for MEMINTC01O (ADR I/O FET Slice Enable Map 0) and MEMINTC09O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
52:53	RW	SLICE_SEL10: Select one of four impedance values to be used for MEMINTC02O (ADR I/O FET Slice Enable Map 0) and MEMINTC10O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
54:55	RW	SLICE_SEL11: Select one of four impedance values to be used for MEMINTC03O (ADR I/O FET Slice Enable Map 0) and MEMINTC11O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
56:57	RW	SLICE_SEL12: Select one of four impedance values to be used for MEMINTC04O (ADR I/O FET Slice Enable Map 0) and MEMINTC12O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.

Bits	SCOM	Field Mnemonic: Description
58:59	RW	SLICE_SEL13: Select one of four impedance values to be used for MEMINTC05O (ADR I/O FET Slice Enable Map 0) and MEMINTC13O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
60:61	RW	SLICE_SEL14: Select one of four impedance values to be used for MEMINTC06O (ADR I/O FET Slice Enable Map 0) and MEMINTC14O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
62:63	RW	SLICE_SEL15: Select one of four impedance values to be used for MEMINTC07O (ADR I/O FET Slice Enable Map 0) and MEMINTC15O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.

Register Name	**ADR I/O FET Slice Enable Map 1 Register**
Mnemonic	IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P3_ADR2
Address	8000482107011C3F (SCOM)
Description	Each predefined pin on the ADR can be mapped to predetermined I/O FET slice enable values to implement 30 Ω or 40 Ω drive impedance. Pins are defined by the mnemonic {{0-1}*8+n}, with n = 0 – 7. Register 0 contains lanes 0:7, and register 1 contains lanes 8:15.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	SLICE_SEL8: Select impedance values to be used for MEMINTC00O (ADR I/O FET Slice Enable Map 0) and MEMINTC08O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
49	RW	Reserved.
50:51	RW	SLICE_SEL9: Select one of four impedance values to be used for MEMINTC01O (ADR I/O FET Slice Enable Map 0) and MEMINTC09O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
52:53	RW	SLICE_SEL10: Select one of four impedance values to be used for MEMINTC02O (ADR I/O FET Slice Enable Map 0) and MEMINTC10O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
54:55	RW	SLICE_SEL11: Select one of four impedance values to be used for MEMINTC03O (ADR I/O FET Slice Enable Map 0) and MEMINTC11O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.

Bits	SCOM	Field Mnemonic: Description
56:57	RW	SLICE_SEL12: Select one of four impedance values to be used for MEMINTC04O (ADR I/O FET Slice Enable Map 0) and MEMINTC12O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
58:59	RW	SLICE_SEL13: Select one of four impedance values to be used for MEMINTC05O (ADR I/O FET Slice Enable Map 0) and MEMINTC13O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
60:61	RW	SLICE_SEL14: Select one of four impedance values to be used for MEMINTC06O (ADR I/O FET Slice Enable Map 0) and MEMINTC14O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
62:63	RW	SLICE_SEL15: Select one of four impedance values to be used for MEMINTC07O (ADR I/O FET Slice Enable Map 0) and MEMINTC15O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.

Register Name	ADR RESERVED 10 Register
Mnemonic	IOM0.DDRPHY_ADR_RESERVED10_P0_ADR2
Address	8000482A0701103F (SCOM)
Description	Currently reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	Reserved.

Register Name	ADR RESERVED 10 Register
Mnemonic	IOM0.DDRPHY_ADR_RESERVED10_P1_ADR2
Address	8000482A0701143F (SCOM)
Description	Currently reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	Reserved.

Register Name	ADR RESERVED 10 Register
Mnemonic	IOM0.DDRPHY_ADR_RESERVED10_P2_ADR2
Address	8000482A0701183F (SCOM)
Description	Currently reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	Reserved.

Register Name	ADR RESERVED 10 Register
Mnemonic	IOM0.DDRPHY_ADR_RESERVED10_P3_ADR2
Address	8000482A07011C3F (SCOM)
Description	Currently reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	Reserved.

Register Name	ADR RESERVED 11 Register
Mnemonic	IOM0.DDRPHY_ADR_RESERVED11_P0_ADR2
Address	8000482B0701103F (SCOM)
Description	Currently reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	Reserved.

Register Name	ADR RESERVED 11 Register
Mnemonic	IOM0.DDRPHY_ADR_RESERVED11_P1_ADR2
Address	8000482B0701143F (SCOM)
Description	Currently reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	Reserved.

Register Name	ADR RESERVED 11 Register
Mnemonic	IOM0.DDRPHY_ADR_RESERVED11_P2_ADR2
Address	8000482B0701183F (SCOM)
Description	Currently reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	Reserved.

Register Name	ADR RESERVED 11 Register
Mnemonic	IOM0.DDRPHY_ADR_RESERVED11_P3_ADR2
Address	8000482B07011C3F (SCOM)
Description	Currently reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	Reserved.

Register Name	ADR Power Down 2 Register
Mnemonic	IOM0.DDRPHY_ADR_POWERDOWN_2_P0_ADR2
Address	8000482C0701103F (SCOM)
Description	This register provides control of the ADR power-down modes.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:55	RW	ADR_LANE_0_7_PD: 0 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{0-7} is at high-Z (tri-stated). 1 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{0-7} drives the value programmed in bit 55 the PC Power Down 1 Register at the impedance programmed into the ADR I/O FET Slice Enable Map {0-1} Register.
56:59	RW	ADR_Lane_8_11_PD: ADR12: 0 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{8-11} is at high-Z (tri-stated). 1 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{8-11} drives the value programmed in bit 55 of PC Power Down 1 Register at the impedance programmed into the ADR I/O FET Slice Enable Map {0-1} Register. ADR8: Reserved.
60:63	RW	ADR_LANE_12_15_PD: Reserved.

Register Name	ADR Power Down 2 Register
Mnemonic	IOM0.DDRPHY_ADR_POWERDOWN_2_P1_ADR2
Address	8000482C0701143F (SCOM)
Description	This register provides control of the ADR power-down modes.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:55	RW	ADR_LANE_0_7_PD: 0 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{0-7} is at high-Z (tri-stated). 1 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{0-7} drives the value programmed in bit 55 the PC Power Down 1 Register at the impedance programmed into the ADR I/O FET Slice Enable Map {0-1} Register.
56:59	RW	ADR_Lane_8_11_PD: ADR12: 0 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{8-11} is at high-Z (tri-stated). 1 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{8-11} drives the value programmed in bit 55 of PC Power Down 1 Register at the impedance programmed into the ADR I/O FET Slice Enable Map {0-1} Register. ADR8: Reserved.
60:63	RW	ADR_LANE_12_15_PD: Reserved.

Register Name	ADR Power Down 2 Register
Mnemonic	IOM0.DDRPHY_ADR_POWERDOWN_2_P2_ADR2
Address	8000482C0701183F (SCOM)
Description	This register provides control of the ADR power-down modes.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:55	RW	ADR_LANE_0_7_PD: 0 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{0-7} is at high-Z (tri-stated). 1 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{0-7} drives the value programmed in bit 55 the PC Power Down 1 Register at the impedance programmed into the ADR I/O FET Slice Enable Map {0-1} Register.
56:59	RW	ADR_Lane_8_11_PD: ADR12: 0 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{8-11} is at high-Z (tri-stated). 1 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{8-11} drives the value programmed in bit 55 of PC Power Down 1 Register at the impedance programmed into the ADR I/O FET Slice Enable Map {0-1} Register. ADR8: Reserved.
60:63	RW	ADR_LANE_12_15_PD: Reserved.

Register Name	ADR Power Down 2 Register
Mnemonic	IOM0.DDRPHY_ADR_POWERDOWN_2_P3_ADR2
Address	8000482C07011C3F (SCOM)
Description	This register provides control of the ADR power-down modes.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:55	RW	ADR_LANE_0_7_PD: 0 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{0-7} is at high-Z (tri-stated). 1 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{0-7} drives the value programmed in bit 55 the PC Power Down 1 Register at the impedance programmed into the ADR I/O FET Slice Enable Map {0-1} Register.
56:59	RW	ADR_Lane_8_11_PD: ADR12: 0 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{8-11} is at high-Z (tri-stated). 1 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{8-11} drives the value programmed in bit 55 of PC Power Down 1 Register at the impedance programmed into the ADR I/O FET Slice Enable Map {0-1} Register. ADR8: Reserved.
60:63	RW	ADR_LANE_12_15_PD: Reserved.

Register Name	ADR Bit Enable Register
Mnemonic	IOM0.DDRPHY_ADR_BIT_ENABLE_P0_ADR3
Address	80004C000701103F (SCOM)
Description	An ADR12 has 12 possible outputs, and an ADR8 has 8 possible outputs. This register is used to enable and disable each of the 12 pins or 8 pins. Any pins used on an ADR must be enabled via this register. The pins on an ADR can be used to send clocks or control (command, address, and so on) signals to memory devices.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:59	RW	BIT_ENABLE_0_11: 1 = Indicates that the ADR bit is enabled and is used for sending clocks or control (command, address, and so on) signals to the memory device. 0 = Indicates that the ADR bit is not used and not enabled. Bit 0 controls MEMINTC00O(n). Bit 1 controls MEMINTC01O(n). Bit 2 controls MEMINTC02O(n). ... Bit 11 controls MEMINTC11O(n). where n is the ADR instance number. ADR12 uses bits 48:59. ADR8 uses bits 48:55, with bits 56:59 reserved.
60:63	RW	Reserved.

Register Name	ADR Bit Enable Register
Mnemonic	IOM0.DDRPHY_ADR_BIT_ENABLE_P1_ADR3
Address	80004C000701143F (SCOM)
Description	An ADR12 has 12 possible outputs, and an ADR8 has 8 possible outputs. This register is used to enable and disable each of the 12 pins or 8 pins. Any pins used on an ADR must be enabled via this register. The pins on an ADR can be used to send clocks or control (command, address, and so on) signals to memory devices.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:59	RW	BIT_ENABLE_0_11: 1 = Indicates that the ADR bit is enabled and is used for sending clocks or control (command, address, and so on) signals to the memory device. 0 = Indicates that the ADR bit is not used and not enabled. Bit 0 controls MEMINTC00O(n). Bit 1 controls MEMINTC01O(n). Bit 2 controls MEMINTC02O(n). ... Bit 11 controls MEMINTC11O(n). where n is the ADR instance number. ADR12 uses bits 48:59. ADR8 uses bits 48:55, with bits 56:59 reserved.
60:63	RW	Reserved.

Register Name	ADR Bit Enable Register
Mnemonic	IOM0.DDRPHY_ADR_BIT_ENABLE_P2_ADR3
Address	80004C000701183F (SCOM)
Description	An ADR12 has 12 possible outputs, and an ADR8 has 8 possible outputs. This register is used to enable and disable each of the 12 pins or 8 pins. Any pins used on an ADR must be enabled via this register. The pins on an ADR can be used to send clocks or control (command, address, and so on) signals to memory devices.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:59	RW	BIT_ENABLE_0_11: 1 = Indicates that the ADR bit is enabled and is used for sending clocks or control (command, address, and so on) signals to the memory device. 0 = Indicates that the ADR bit is not used and not enabled. Bit 0 controls MEMINTC00O(n). Bit 1 controls MEMINTC01O(n). Bit 2 controls MEMINTC02O(n). ... Bit 11 controls MEMINTC11O(n). where n is the ADR instance number. ADR12 uses bits 48:59. ADR8 uses bits 48:55, with bits 56:59 reserved.
60:63	RW	Reserved.

Register Name	ADR Bit Enable Register
Mnemonic	IOM0.DDRPHY_ADR_BIT_ENABLE_P3_ADR3
Address	80004C0007011C3F (SCOM)
Description	An ADR12 has 12 possible outputs, and an ADR8 has 8 possible outputs. This register is used to enable and disable each of the 12 pins or 8 pins. Any pins used on an ADR must be enabled via this register. The pins on an ADR can be used to send clocks or control (command, address, and so on) signals to memory devices.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:59	RW	BIT_ENABLE_0_11: 1 = Indicates that the ADR bit is enabled and is used for sending clocks or control (command, address, and so on) signals to the memory device. 0 = Indicates that the ADR bit is not used and not enabled. Bit 0 controls MEMINTC00O(n). Bit 1 controls MEMINTC01O(n). Bit 2 controls MEMINTC02O(n). ... Bit 11 controls MEMINTC11O(n). where n is the ADR instance number. ADR12 uses bits 48:59. ADR8 uses bits 48:55, with bits 56:59 reserved.
60:63	RW	Reserved.

Register Name	ADR Differential Pair Enable Register
Mnemonic	IOM0.DDRPHY_ADR_DIFFPAIR_ENABLE_P0_ADR3
Address	80004C010701103F (SCOM)
Description	An ADR12 has 12 possible outputs, and an ADR8 has 8 possible outputs, any of which can be paired together for memory clock generation (CK/CK#). This register is used to enable or disable each pair of ADR pins to be used as differential outputs or as two single-ended outputs. When a pair of ADR pins is configured as a differential output, the delays associated with both outputs of the differential pair must be programmed to the same value in the ADR Delay Value {0-7} Registers for that pair. When a pair of ADR pins is enabled as a differential pair in this register, both of the pins must be enabled in the ADR Bit Enable Register. When a pair of ADR pins is enabled as a differential pair in this register, the even-numbered pin is the true, and the odd-numbered pin is the complement signal.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	DI_ADR0_ADR1: 0 = Lanes 0 and 1 are not a differential clock pair. 1 = Lanes 0 and 1 are a differential clock pair.
49	RW	DI_ADR2_ADR3: 0 = Lanes 2 and 3 are not a differential clock pair. 1 = Lanes 2 and 3 are a differential clock pair.
50	RW	DI_ADR4_ADR5: 0 = Lanes 4 and 5 are not a differential clock pair. 1 = Lanes 4 and 5 are a differential clock pair.
51	RW	DI_ADR6_ADR7: 0 = Lanes 6 and 7 are not a differential clock pair. 1 = Lanes 6 and 7 are a differential clock pair.

Bits	SCOM	Field Mnemonic: Description
52	RW	DI_ADR8_ADR9: 0 = Lanes 8 and 9 are not a differential clock pair. 1 = Lanes 8 and 9 are a differential clock pair. Reserved for ADR8.
53	RW	DI_ADR10_ADR11: 0 = Lanes 10 and 11 are not a differential clock pair. 1 = Lanes 10 and 11 are a differential clock pair. Reserved for ADR8.
54:63	RW	Reserved.

Register Name	ADR Differential Pair Enable Register
Mnemonic	IOM0.DDRPHY_ADR_DIFFPAIR_ENABLE_P1_ADR3
Address	80004C010701143F (SCOM)
Description	An ADR12 has 12 possible outputs, and an ADR8 has 8 possible outputs, any of which can be paired together for memory clock generation (CK/CK#). This register is used to enable or disable each pair of ADR pins to be used as differential outputs or as two single-ended outputs. When a pair of ADR pins is configured as a differential output, the delays associated with both outputs of the differential pair must be programmed to the same value in the ADR Delay Value {0-7} Registers for that pair. When a pair of ADR pins is enabled as a differential pair in this register, both of the pins must be enabled in the ADR Bit Enable Register. When a pair of ADR pins is enabled as a differential pair in this register, the even-numbered pin is the true, and the odd-numbered pin is the complement signal.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	DI_ADR0_ADR1: 0 = Lanes 0 and 1 are not a differential clock pair. 1 = Lanes 0 and 1 are a differential clock pair.
49	RW	DI_ADR2_ADR3: 0 = Lanes 2 and 3 are not a differential clock pair. 1 = Lanes 2 and 3 are a differential clock pair.
50	RW	DI_ADR4_ADR5: 0 = Lanes 4 and 5 are not a differential clock pair. 1 = Lanes 4 and 5 are a differential clock pair.
51	RW	DI_ADR6_ADR7: 0 = Lanes 6 and 7 are not a differential clock pair. 1 = Lanes 6 and 7 are a differential clock pair.
52	RW	DI_ADR8_ADR9: 0 = Lanes 8 and 9 are not a differential clock pair. 1 = Lanes 8 and 9 are a differential clock pair. Reserved for ADR8.
53	RW	DI_ADR10_ADR11: 0 = Lanes 10 and 11 are not a differential clock pair. 1 = Lanes 10 and 11 are a differential clock pair. Reserved for ADR8.
54:63	RW	Reserved.

Register Name	ADR Differential Pair Enable Register
Mnemonic	IOM0.DDRPHY_ADR_DIFFPAIR_ENABLE_P2_ADR3
Address	80004C010701183F (SCOM)
Description	An ADR12 has 12 possible outputs, and an ADR8 has 8 possible outputs, any of which can be paired together for memory clock generation (CK/CK#). This register is used to enable or disable each pair of ADR pins to be used as differential outputs or as two single-ended outputs. When a pair of ADR pins is configured as a differential output, the delays associated with both outputs of the differential pair must be programmed to the same value in the ADR Delay Value {0-7} Registers for that pair. When a pair of ADR pins is enabled as a differential pair in this register, both of the pins must be enabled in the ADR Bit Enable Register. When a pair of ADR pins is enabled as a differential pair in this register, the even-numbered pin is the true, and the odd-numbered pin is the complement signal.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	DI_ADR0_ADR1: 0 = Lanes 0 and 1 are not a differential clock pair. 1 = Lanes 0 and 1 are a differential clock pair.
49	RW	DI_ADR2_ADR3: 0 = Lanes 2 and 3 are not a differential clock pair. 1 = Lanes 2 and 3 are a differential clock pair.
50	RW	DI_ADR4_ADR5: 0 = Lanes 4 and 5 are not a differential clock pair. 1 = Lanes 4 and 5 are a differential clock pair.
51	RW	DI_ADR6_ADR7: 0 = Lanes 6 and 7 are not a differential clock pair. 1 = Lanes 6 and 7 are a differential clock pair.
52	RW	DI_ADR8_ADR9: 0 = Lanes 8 and 9 are not a differential clock pair. 1 = Lanes 8 and 9 are a differential clock pair. Reserved for ADR8.
53	RW	DI_ADR10_ADR11: 0 = Lanes 10 and 11 are not a differential clock pair. 1 = Lanes 10 and 11 are a differential clock pair. Reserved for ADR8.
54:63	RW	Reserved.

Register Name	ADR Differential Pair Enable Register
Mnemonic	IOM0.DDRPHY_ADR_DIFFPAIR_ENABLE_P3_ADR3
Address	80004C0107011C3F (SCOM)
Description	An ADR12 has 12 possible outputs, and an ADR8 has 8 possible outputs, any of which can be paired together for memory clock generation (CK/CK#). This register is used to enable or disable each pair of ADR pins to be used as differential outputs or as two single-ended outputs. When a pair of ADR pins is configured as a differential output, the delays associated with both outputs of the differential pair must be programmed to the same value in the ADR Delay Value {0-7} Registers for that pair. When a pair of ADR pins is enabled as a differential pair in this register, both of the pins must be enabled in the ADR Bit Enable Register. When a pair of ADR pins is enabled as a differential pair in this register, the even-numbered pin is the true, and the odd-numbered pin is the complement signal.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RW	DI_ADR0_ADR1: 0 = Lanes 0 and 1 are not a differential clock pair. 1 = Lanes 0 and 1 are a differential clock pair.
49	RW	DI_ADR2_ADR3: 0 = Lanes 2 and 3 are not a differential clock pair. 1 = Lanes 2 and 3 are a differential clock pair.
50	RW	DI_ADR4_ADR5: 0 = Lanes 4 and 5 are not a differential clock pair. 1 = Lanes 4 and 5 are a differential clock pair.
51	RW	DI_ADR6_ADR7: 0 = Lanes 6 and 7 are not a differential clock pair. 1 = Lanes 6 and 7 are a differential clock pair.
52	RW	DI_ADR8_ADR9: 0 = Lanes 8 and 9 are not a differential clock pair. 1 = Lanes 8 and 9 are a differential clock pair. Reserved for ADR8.
53	RW	DI_ADR10_ADR11: 0 = Lanes 10 and 11 are not a differential clock pair. 1 = Lanes 10 and 11 are a differential clock pair. Reserved for ADR8.
54:63	RW	Reserved.

Register Name	**ADR Delay Value 0 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY0_P0_ADR3
Address	80004C040701103F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY0: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY1: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 0 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY0_P1_ADR3
Address	80004C040701143F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY0: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY1: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 0 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY0_P2_ADR3
Address	80004C040701183F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY0: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY1: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 0 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY0_P3_ADR3
Address	80004C0407011C3F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY0: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY1: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 1 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY1_P0_ADR3
Address	80004C050701103F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY2: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY3: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 1 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY1_P1_ADR3
Address	80004C050701143F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY2: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY3: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 1 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY1_P2_ADR3
Address	80004C050701183F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY2: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY3: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 1 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY1_P3_ADR3
Address	80004C0507011C3F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY2: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY3: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 2 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY2_P0_ADR3
Address	80004C060701103F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY4: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY5: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 2 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY2_P1_ADR3
Address	80004C060701143F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY4: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY5: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 2 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY2_P2_ADR3
Address	80004C060701183F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY4: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY5: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 2 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY2_P3_ADR3
Address	80004C0607011C3F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY4: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY5: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 3 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY3_P0_ADR3
Address	80004C070701103F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY6: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY7: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 3 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY3_P1_ADR3
Address	80004C070701143F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY6: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY7: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 3 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY3_P2_ADR3
Address	80004C070701183F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY6: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY7: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 3 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY3_P3_ADR3
Address	80004C0707011C3F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY6: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY7: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 4 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY4_P0_ADR3
Address	80004C080701103F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY8: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY9: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 4 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY4_P1_ADR3
Address	80004C080701143F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY8: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY9: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 4 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY4_P2_ADR3
Address	80004C080701183F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY8: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY9: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 4 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY4_P3_ADR3
Address	80004C0807011C3F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY8: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY9: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 5 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY5_P0_ADR3
Address	80004C090701103F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY10: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY11: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 5 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY5_P1_ADR3
Address	80004C090701143F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY10: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY11: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 5 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY5_P2_ADR3
Address	80004C090701183F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY10: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY11: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 5 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY5_P3_ADR3
Address	80004C0907011C3F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY10: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY11: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 6 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY6_P0_ADR3
Address	80004C0A0701103F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY12: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY13: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 6 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY6_P1_ADR3
Address	80004C0A0701143F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY12: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY13: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 6 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY6_P2_ADR3
Address	80004C0A0701183F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY12: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY13: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 6 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY6_P3_ADR3
Address	80004C0A07011C3F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY12: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY13: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 7 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY7_P0_ADR3
Address	80004C0B0701103F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY14: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY15: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 7 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY7_P1_ADR3
Address	80004C0B0701143F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY14: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY15: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	**ADR Delay Value 7 Register**
Mnemonic	IOM0.DDRPHY_ADR_DELAY7_P2_ADR3
Address	80004C0B0701183F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY14: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY15: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR Delay Value 7 Register
Mnemonic	IOM0.DDRPHY_ADR_DELAY7_P3_ADR3
Address	80004C0B07011C3F (SCOM)
Description	Each register in this set holds the delay values for two of the MEMINTCnnO pins within the ADR. This register set is not updated by the calibration algorithms. If the reset value is not sufficient for the given system, these registers must be set via the programming interface. Note that the mnemonic {{0-7}*2}+n, where n is 0 to 1, indicates that there are eight total registers, each containing values for two consecutive lanes; 0 - 1, 2 - 3, and so on.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	ADR_DELAY14: Output delay for the MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	Reserved.
57:63	RW	ADR_DELAY15: Output delay for the MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	ADR DFT Wrap Status and Control Register
Mnemonic	IOM0.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P0_ADR3
Address	80004C0C0701103F (SCOM)
Description	This register provides the status and control of the ADR wrap test for a given ADR8/12 instance. This register must only be used to perform diagnostic, manufacturing, or characterization testing. Contact your IBM representative before modifying this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:53	ROX	ADR_TEST_LANE_PAIR_FAIL: **Note:** Bits 48:55 of this register are read only. These bits can be reset, but they are written with a free running dphy_gckn clock. Therefore, any read of these bits returns the value from the loopback test logic. If that logic has not been reset and the error bits are cleared, this field is X. Reading this register does not automatically clear these bits. When set, these bits must be reset by asserting bit 62 of this register. For PRBS7 error detection in the memory-clock domain: Bit 0 represents the miscompare detect for wrap0 and wrap1. Bit 1 represents the miscompare detect for wrap2 and wrap3. Bit 2 represents the miscompare detect for wrap4 and wrap5. Bit 3 represents the miscompare detect for wrap6 and wrap7. Bit 4 represents the miscompare detect for wrap8 and wrap9. Reserved for ADR8. Bit 5 represents the miscompare detect for wrap10 and wrap11. Reserved for ADR8.
54:55	ROX	Reserved.
56	RW	ADR_TEST_DATA_EN: When high, this bit selects macrotest data. Otherwise, functional mode is used.
57:58	RW	ADR_TEST_MODE: These bits are reserved for manufacturing test.
59	RW	ADR_TEST_4TO1_MODE: When active, the PRBS generates a 4-bit output every cycle. Otherwise, it outputs two bits. This signal is in the memory-clock domain.
60	RW	ADR_TEST_RESET: Reset. This signal is in the memory-clock domain.
61	RW	ADR_TEST_GEN_EN: Pattern generator enable. This signal is in the memory-clock domain. This signal must be active before enabling the check_enable_i; which is 8 cycles for loading the checker plus the latency between the generator and the wrap through APIN.

Bits	SCOM	Field Mnemonic: Description
62	RW	ADR_TEST_CLEAR_ERROR: Clear error bits. This signal is in the memory-clock domain. The generator must be active before clr_error_i, and the macrotest_mode_i must be selecting WRAP clocks to all the corresponding checkers' latches.
63	RW	ADR_TEST_CHECK_EN: Enable the pattern checker. This signal is in the memory-clock domain. When active, the checker performs a PRBS7 sequence check on the corresponding WRAP channel.

Register Name	**ADR DFT Wrap Status and Control Register**
Mnemonic	IOM0.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P1_ADR3
Address	80004C0C0701143F (SCOM)
Description	This register provides the status and control of the ADR wrap test for a given ADR8/12 instance. This register must only be used to perform diagnostic, manufacturing, or characterization testing. Contact your IBM representative before modifying this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:53	ROX	ADR_TEST_LANE_PAIR_FAIL: **Note:** Bits 48:55 of this register are read only. These bits can be reset, but they are written with a free running dphy_gckn clock. Therefore, any read of these bits returns the value from the loopback test logic. If that logic has not been reset and the error bits are cleared, this field is X. Reading this register does not automatically clear these bits. When set, these bits must be reset by asserting bit 62 of this register. For PRBS7 error detection in the memory-clock domain: Bit 0 represents the miscompare detect for wrap0 and wrap1. Bit 1 represents the miscompare detect for wrap2 and wrap3. Bit 2 represents the miscompare detect for wrap4 and wrap5. Bit 3 represents the miscompare detect for wrap6 and wrap7. Bit 4 represents the miscompare detect for wrap8 and wrap9. Reserved for ADR8. Bit 5 represents the miscompare detect for wrap10 and wrap11. Reserved for ADR8.
54:55	ROX	RESERVED.
56	RW	ADR_TEST_DATA_EN: When high, this bit selects macrotest data. Otherwise, functional mode is used.
57:58	RW	ADR_TEST_MODE: These bits are reserved for manufacturing test.
59	RW	ADR_TEST_4TO1_MODE: When active, the PRBS generates a 4-bit output every cycle. Otherwise, it outputs two bits. This signal is in the memory-clock domain.
60	RW	ADR_TEST_RESET: Reset. This signal is in the memory-clock domain.
61	RW	ADR_TEST_GEN_EN: Pattern generator enable. This signal is in the memory-clock domain. This signal must be active before enabling the check_enable_i; which is 8 cycles for loading the checker plus the latency between the generator and the wrap through APIN.
62	RW	ADR_TEST_CLEAR_ERROR: Clear error bits. This signal is in the memory-clock domain. The generator must be active before clr_error_i, and the macrotest_mode_i must be selecting WRAP clocks to all the corresponding checkers' latches.
63	RW	ADR_TEST_CHECK_EN: Enable the pattern checker. This signal is in the memory-clock domain. When active, the checker performs a PRBS7 sequence check on the corresponding WRAP channel.

Register Name	ADR DFT Wrap Status and Control Register
Mnemonic	IOM0.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P2_ADR3
Address	80004C0C0701183F (SCOM)
Description	This register provides the status and control of the ADR wrap test for a given ADR8/12 instance. This register must only be used to perform diagnostic, manufacturing, or characterization testing. Contact your IBM representative before modifying this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:53	ROX	ADR_TEST_LANE_PAIR_FAIL: **Note:** Bits 48:55 of this register are read only. These bits can be reset, but they are written with a free running dphy_gckn clock. Therefore, any read of these bits returns the value from the loopback test logic. If that logic has not been reset and the error bits are cleared, this field is X. Reading this register does not automatically clear these bits. When set, these bits must be reset by asserting bit 62 of this register. For PRBS7 error detection in the memory-clock domain: Bit 0 represents the miscompare detect for wrap0 and wrap1. Bit 1 represents the miscompare detect for wrap2 and wrap3. Bit 2 represents the miscompare detect for wrap4 and wrap5. Bit 3 represents the miscompare detect for wrap6 and wrap7. Bit 4 represents the miscompare detect for wrap8 and wrap9. Reserved for ADR8. Bit 5 represents the miscompare detect for wrap10 and wrap11. Reserved for ADR8.
54:55	ROX	Reserved.
56	RW	ADR_TEST_DATA_EN: When high, this bit selects macrotest data. Otherwise, functional mode is used.
57:58	RW	ADR_TEST_MODE: These bits are reserved for manufacturing test.
59	RW	ADR_TEST_4TO1_MODE: When active, the PRBS generates a 4-bit output every cycle. Otherwise, it outputs two bits. This signal is in the memory-clock domain.
60	RW	ADR_TEST_RESET: Reset. This signal is in the memory-clock domain.
61	RW	ADR_TEST_GEN_EN: Pattern generator enable. This signal is in the memory-clock domain. This signal must be active before enabling the check_enable_i; which is 8 cycles for loading the checker plus the latency between the generator and the wrap through APIN.
62	RW	ADR_TEST_CLEAR_ERROR: Clear error bits. This signal is in the memory-clock domain. The generator must be active before clr_error_i, and the macrotest_mode_i must be selecting WRAP clocks to all the corresponding checkers' latches.
63	RW	ADR_TEST_CHECK_EN: Enable the pattern checker. This signal is in the memory-clock domain. When active, the checker performs a PRBS7 sequence check on the corresponding WRAP channel.

Register Name	ADR DFT Wrap Status and Control Register
Mnemonic	IOM0.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P3_ADR3
Address	80004C0C07011C3F (SCOM)
Description	This register provides the status and control of the ADR wrap test for a given ADR8/12 instance. This register must only be used to perform diagnostic, manufacturing, or characterization testing. Contact your IBM representative before modifying this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	ROX	ADR_TEST_LANE_PAIR_FAIL: **Note:** Bits 48:55 of this register are read only. These bits can be reset, but they are written with a free running dphy_gckn clock. Therefore, any read of these bits returns the value from the loopback test logic. If that logic has not been reset and the error bits are cleared, this field is X. Reading this register does not automatically clear these bits. When set, these bits must be reset by asserting bit 62 of this register. For PRBS7 error detection in the memory-clock domain: Bit 0 represents the miscompare detect for wrap0 and wrap1. Bit 1 represents the miscompare detect for wrap2 and wrap3. Bit 2 represents the miscompare detect for wrap4 and wrap5. Bit 3 represents the miscompare detect for wrap6 and wrap7. Bit 4 represents the miscompare detect for wrap8 and wrap9. Reserved for ADR8. Bit 5 represents the miscompare detect for wrap10 and wrap11. Reserved for ADR8.
54:55	ROX	Reserved.
56	RW	ADR_TEST_DATA_EN: When high, this bit selects macrotest data. Otherwise, functional mode is used.
57:58	RW	ADR_TEST_MODE: These bits are reserved for manufacturing test.
59	RW	ADR_TEST_4TO1_MODE: When active, the PRBS generates a 4-bit output every cycle. Otherwise, it outputs two bits. This signal is in the memory-clock domain.
60	RW	ADR_TEST_RESET: Reset. This signal is in the memory-clock domain.
61	RW	ADR_TEST_GEN_EN: Pattern generator enable. This signal is in the memory-clock domain. This signal must be active before enabling the check_enable_i; which is 8 cycles for loading the checker plus the latency between the generator and the wrap through APIN.
62	RW	ADR_TEST_CLEAR_ERROR: Clear error bits. This signal is in the memory-clock domain. The generator must be active before clr_error_i, and the macrotest_mode_i must be selecting WRAP clocks to all the corresponding checkers' latches.
63	RW	ADR_TEST_CHECK_EN: Enable the pattern checker. This signal is in the memory-clock domain. When active, the checker performs a PRBS7 sequence check on the corresponding WRAP channel.

Register Name	**ADR I/O FET Slice Enable Map 0 Register**
Mnemonic	IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P0_ADR3
Address	80004C200701103F (SCOM)
Description	Each predefined pin on the ADR can be mapped to predetermined I/O FET slice enable values to implement 30 Ω or 40 Ω drive impedance. Pins are defined by the mnemonic {{0-1}*8+n}, with n = 0 – 7. Register 0 contains lanes 0:7, and register 1 contains lanes 8:15.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	SLICE_SEL0: Select impedance values to be used for MEMINTC00O (ADR I/O FET Slice Enable Map 0) and MEMINTC08O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
49	RW	Reserved.
50	RW	SLICE_SEL1: Select impedance values to be used for MEMINTC01O (ADR I/O FET Slice Enable Map 0) and MEMINTC09O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
51	RW	Reserved.

Bits	SCOM	Field Mnemonic: Description
52	RW	SLICE_SEL2: Select impedance values to be used for MEMINTC02O (ADR I/O FET Slice Enable Map 0) and MEMINTC10O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
53	RW	Reserved.
54	RW	SLICE_SEL3: Select impedance values to be used for MEMINTC03O (ADR I/O FET Slice Enable Map 0) and MEMINTC11O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
55	RW	Reserved.
56	RW	SLICE_SEL4: Select impedance values to be used for MEMINTC04O (ADR I/O FET Slice Enable Map 0) and MEMINTC12O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
57	RW	Reserved.
58	RW	SLICE_SEL5: Select impedance values to be used for MEMINTC05O (ADR I/O FET Slice Enable Map 0) and MEMINTC13O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
59	RW	Reserved.
60	RW	SLICE_SEL6: Select impedance values to be used for MEMINTC06O (ADR I/O FET Slice Enable Map 0) and MEMINTC14O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
61	RW	Reserved.
62	RW	SLICE_SEL7: Select impedance values to be used for MEMINTC07O (ADR I/O FET Slice Enable Map 0) and MEMINTC15O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
63	RW	Reserved.

Register Name	**ADR I/O FET Slice Enable Map 0 Register**
Mnemonic	IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P1_ADR3
Address	80004C200701143F (SCOM)
Description	Each predefined pin on the ADR can be mapped to predetermined I/O FET slice enable values to implement 30 Ω or 40 Ω drive impedance. Pins are defined by the mnemonic {{0-1}*8+n}, with n = 0 – 7. Register 0 contains lanes 0:7, and register 1 contains lanes 8:15.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48	RW	SLICE_SEL0: Select impedance values to be used for MEMINTC00O (ADR I/O FET Slice Enable Map 0) and MEMINTC08O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
49	RW	Reserved.

Bits	SCOM	Field Mnemonic: Description
50	RW	SLICE_SEL1: Select impedance values to be used for MEMINTC01O (ADR I/O FET Slice Enable Map 0) and MEMINTC09O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
51	RW	Reserved.
52	RW	SLICE_SEL2: Select impedance values to be used for MEMINTC02O (ADR I/O FET Slice Enable Map 0) and MEMINTC10O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
53	RW	Reserved.
54	RW	SLICE_SEL3: Select impedance values to be used for MEMINTC03O (ADR I/O FET Slice Enable Map 0) and MEMINTC11O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
55	RW	Reserved.
56	RW	SLICE_SEL4: Select impedance values to be used for MEMINTC04O (ADR I/O FET Slice Enable Map 0) and MEMINTC12O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
57	RW	Reserved.
58	RW	SLICE_SEL5: Select impedance values to be used for MEMINTC05O (ADR I/O FET Slice Enable Map 0) and MEMINTC13O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
59	RW	Reserved.
60	RW	SLICE_SEL6: Select impedance values to be used for MEMINTC06O (ADR I/O FET Slice Enable Map 0) and MEMINTC14O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
61	RW	Reserved.
62	RW	SLICE_SEL7: Select impedance values to be used for MEMINTC07O (ADR I/O FET Slice Enable Map 0) and MEMINTC15O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
63	RW	Reserved.

Register Name	**ADR I/O FET Slice Enable Map 0 Register**
Mnemonic	IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P2_ADR3
Address	80004C200701183F (SCOM)
Description	Each predefined pin on the ADR can be mapped to predetermined I/O FET slice enable values to implement 30 Ω or 40 Ω drive impedance. Pins are defined by the mnemonic {{0-1}*8+n}, with n = 0 – 7. Register 0 contains lanes 0:7, and register 1 contains lanes 8:15.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RW	SLICE_SEL0: Select impedance values to be used for MEMINTC00O (ADR I/O FET Slice Enable Map 0) and MEMINTC08O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
49	RW	Reserved.
50	RW	SLICE_SEL1: Select impedance values to be used for MEMINTC01O (ADR I/O FET Slice Enable Map 0) and MEMINTC09O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
51	RW	Reserved.
52	RW	SLICE_SEL2: Select impedance values to be used for MEMINTC02O (ADR I/O FET Slice Enable Map 0) and MEMINTC10O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
53	RW	Reserved.
54	RW	SLICE_SEL3: Select impedance values to be used for MEMINTC03O (ADR I/O FET Slice Enable Map 0) and MEMINTC11O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
55	RW	Reserved.
56	RW	SLICE_SEL4: Select impedance values to be used for MEMINTC04O (ADR I/O FET Slice Enable Map 0) and MEMINTC12O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
57	RW	Reserved.
58	RW	SLICE_SEL5: Select impedance values to be used for MEMINTC05O (ADR I/O FET Slice Enable Map 0) and MEMINTC13O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
59	RW	Reserved.
60	RW	SLICE_SEL6: Select impedance values to be used for MEMINTC06O (ADR I/O FET Slice Enable Map 0) and MEMINTC14O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
61	RW	Reserved.
62	RW	SLICE_SEL7: Select impedance values to be used for MEMINTC07O (ADR I/O FET Slice Enable Map 0) and MEMINTC15O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
63	RW	Reserved.

Register Name	**ADR I/O FET Slice Enable Map 0 Register**
Mnemonic	IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P3_ADR3
Address	80004C2007011C3F (SCOM)
Description	Each predefined pin on the ADR can be mapped to predetermined I/O FET slice enable values to implement 30 Ω or 40 Ω drive impedance. Pins are defined by the mnemonic {{0-1}*8+n}, with n = 0 – 7. Register 0 contains lanes 0:7, and register 1 contains lanes 8:15.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	SLICE_SEL0: Select impedance values to be used for MEMINTC00O (ADR I/O FET Slice Enable Map 0) and MEMINTC08O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
49	RW	Reserved.
50	RW	SLICE_SEL1: Select impedance values to be used for MEMINTC01O (ADR I/O FET Slice Enable Map 0) and MEMINTC09O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
51	RW	Reserved.
52	RW	SLICE_SEL2: Select impedance values to be used for MEMINTC02O (ADR I/O FET Slice Enable Map 0) and MEMINTC10O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
53	RW	Reserved.
54	RW	SLICE_SEL3: Select impedance values to be used for MEMINTC03O (ADR I/O FET Slice Enable Map 0) and MEMINTC11O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
55	RW	Reserved.
56	RW	SLICE_SEL4: Select impedance values to be used for MEMINTC04O (ADR I/O FET Slice Enable Map 0) and MEMINTC12O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
57	RW	Reserved.
58	RW	SLICE_SEL5: Select impedance values to be used for MEMINTC05O (ADR I/O FET Slice Enable Map 0) and MEMINTC13O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
59	RW	Reserved.
60	RW	SLICE_SEL6: Select impedance values to be used for MEMINTC06O (ADR I/O FET Slice Enable Map 0) and MEMINTC14O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
61	RW	Reserved.
62	RW	SLICE_SEL7: Select impedance values to be used for MEMINTC07O (ADR I/O FET Slice Enable Map 0) and MEMINTC15O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
63	RW	Reserved.

Register Name	**ADR I/O FET Slice Enable Map 1 Register**
Mnemonic	IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P0_ADR3
Address	80004C210701103F (SCOM)
Description	Each predefined pin on the ADR can be mapped to predetermined I/O FET slice enable values to implement 30 Ω or 40 Ω drive impedance. Pins are defined by the mnemonic {{0-1}*8+n}, with n = 0 – 7. Register 0 contains lanes 0:7, and register 1 contains lanes 8:15.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	SLICE_SEL8: Select impedance values to be used for MEMINTC00O (ADR I/O FET Slice Enable Map 0) and MEMINTC08O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
49	RW	Reserved.
50:51	RW	SLICE_SEL9: Select one of four impedance values to be used for MEMINTC01O (ADR I/O FET Slice Enable Map 0) and MEMINTC09O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
52:53	RW	SLICE_SEL10: Select one of four impedance values to be used for MEMINTC02O (ADR I/O FET Slice Enable Map 0) and MEMINTC10O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
54:55	RW	SLICE_SEL11: Select one of four impedance values to be used for MEMINTC03O (ADR I/O FET Slice Enable Map 0) and MEMINTC11O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
56:57	RW	SLICE_SEL12: Select one of four impedance values to be used for MEMINTC04O (ADR I/O FET Slice Enable Map 0) and MEMINTC12O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
58:59	RW	SLICE_SEL13: Select one of four impedance values to be used for MEMINTC05O (ADR I/O FET Slice Enable Map 0) and MEMINTC13O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
60:61	RW	SLICE_SEL14: Select one of four impedance values to be used for MEMINTC06O (ADR I/O FET Slice Enable Map 0) and MEMINTC14O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.

Bits	SCOM	Field Mnemonic: Description
62:63	RW	SLICE_SEL15: Select one of four impedance values to be used for MEMINTC07O (ADR I/O FET Slice Enable Map 0) and MEMINTC15O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.

Register Name	ADR I/O FET Slice Enable Map 1 Register
Mnemonic	IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P1_ADR3
Address	80004C210701143F (SCOM)
Description	Each predefined pin on the ADR can be mapped to predetermined I/O FET slice enable values to implement 30 Ω or 40 Ω drive impedance. Pins are defined by the mnemonic {{0-1}*8+n}, with n = 0 – 7. Register 0 contains lanes 0:7, and register 1 contains lanes 8:15.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	SLICE_SEL8: Select impedance values to be used for MEMINTC00O (ADR I/O FET Slice Enable Map 0) and MEMINTC08O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
49	RW	Reserved.
50:51	RW	SLICE_SEL9: Select one of four impedance values to be used for MEMINTC01O (ADR I/O FET Slice Enable Map 0) and MEMINTC09O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
52:53	RW	SLICE_SEL10: Select one of four impedance values to be used for MEMINTC02O (ADR I/O FET Slice Enable Map 0) and MEMINTC10O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
54:55	RW	SLICE_SEL11: Select one of four impedance values to be used for MEMINTC03O (ADR I/O FET Slice Enable Map 0) and MEMINTC11O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
56:57	RW	SLICE_SEL12: Select one of four impedance values to be used for MEMINTC04O (ADR I/O FET Slice Enable Map 0) and MEMINTC12O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
58:59	RW	SLICE_SEL13: Select one of four impedance values to be used for MEMINTC05O (ADR I/O FET Slice Enable Map 0) and MEMINTC13O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.

Bits	SCOM	Field Mnemonic: Description
60:61	RW	SLICE_SEL14: Select one of four impedance values to be used for MEMINTC06O (ADR I/O FET Slice Enable Map 0) and MEMINTC14O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
62:63	RW	SLICE_SEL15: Select one of four impedance values to be used for MEMINTC07O (ADR I/O FET Slice Enable Map 0) and MEMINTC15O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.

Register Name	**ADR I/O FET Slice Enable Map 1 Register**
Mnemonic	IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P2_ADR3
Address	80004C210701183F (SCOM)
Description	Each predefined pin on the ADR can be mapped to predetermined I/O FET slice enable values to implement 30 Ω or 40 Ω drive impedance. Pins are defined by the mnemonic {{0-1}*8+n}, with n = 0 – 7. Register 0 contains lanes 0:7, and register 1 contains lanes 8:15.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48	RW	SLICE_SEL8: Select impedance values to be used for MEMINTC00O (ADR I/O FET Slice Enable Map 0) and MEMINTC08O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
49	RW	Reserved.
50:51	RW	SLICE_SEL9: Select one of four impedance values to be used for MEMINTC01O (ADR I/O FET Slice Enable Map 0) and MEMINTC09O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
52:53	RW	SLICE_SEL10: Select one of four impedance values to be used for MEMINTC02O (ADR I/O FET Slice Enable Map 0) and MEMINTC10O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
54:55	RW	SLICE_SEL11: Select one of four impedance values to be used for MEMINTC03O (ADR I/O FET Slice Enable Map 0) and MEMINTC11O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
56:57	RW	SLICE_SEL12: Select one of four impedance values to be used for MEMINTC04O (ADR I/O FET Slice Enable Map 0) and MEMINTC12O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.

Bits	SCOM	Field Mnemonic: Description
58:59	RW	SLICE_SEL13: Select one of four impedance values to be used for MEMINTC05O (ADR I/O FET Slice Enable Map 0) and MEMINTC13O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
60:61	RW	SLICE_SEL14: Select one of four impedance values to be used for MEMINTC06O (ADR I/O FET Slice Enable Map 0) and MEMINTC14O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
62:63	RW	SLICE_SEL15: Select one of four impedance values to be used for MEMINTC07O (ADR I/O FET Slice Enable Map 0) and MEMINTC15O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.

Register Name	**ADR I/O FET Slice Enable Map 1 Register**
Mnemonic	IOM0.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P3_ADR3
Address	80004C2107011C3F (SCOM)
Description	Each predefined pin on the ADR can be mapped to predetermined I/O FET slice enable values to implement 30 Ω or 40 Ω drive impedance. Pins are defined by the mnemonic {{0-1}*8+n}, with n = 0 – 7. Register 0 contains lanes 0:7, and register 1 contains lanes 8:15.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	SLICE_SEL8: Select impedance values to be used for MEMINTC00O (ADR I/O FET Slice Enable Map 0) and MEMINTC08O (ADR I/O FET Slice Enable Map 1). 1 = Use 30 Ω drive impedance. 0 = Use 40 Ω drive impedance.
49	RW	Reserved.
50:51	RW	SLICE_SEL9: Select one of four impedance values to be used for MEMINTC01O (ADR I/O FET Slice Enable Map 0) and MEMINTC09O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
52:53	RW	SLICE_SEL10: Select one of four impedance values to be used for MEMINTC02O (ADR I/O FET Slice Enable Map 0) and MEMINTC10O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
54:55	RW	SLICE_SEL11: Select one of four impedance values to be used for MEMINTC03O (ADR I/O FET Slice Enable Map 0) and MEMINTC11O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.

Bits	SCOM	Field Mnemonic: Description
56:57	RW	SLICE_SEL12: Select one of four impedance values to be used for MEMINTC04O (ADR I/O FET Slice Enable Map 0) and MEMINTC12O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
58:59	RW	SLICE_SEL13: Select one of four impedance values to be used for MEMINTC05O (ADR I/O FET Slice Enable Map 0) and MEMINTC13O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
60:61	RW	SLICE_SEL14: Select one of four impedance values to be used for MEMINTC06O (ADR I/O FET Slice Enable Map 0) and MEMINTC14O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.
62:63	RW	SLICE_SEL15: Select one of four impedance values to be used for MEMINTC07O (ADR I/O FET Slice Enable Map 0) and MEMINTC15O (ADR I/O FET Slice Enable Map 1). 00 = Use 15 Ω drive impedance. 01 = Use 20 Ω drive impedance. 10 = Use 30 Ω drive impedance. 11 = Use 40 Ω drive impedance.

Register Name	ADR RESERVED 10 Register
Mnemonic	IOM0.DDRPHY_ADR_RESERVED10_P0_ADR3
Address	80004C2A0701103F (SCOM)
Description	Currently reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	Reserved.

Register Name	ADR RESERVED 10 Register
Mnemonic	IOM0.DDRPHY_ADR_RESERVED10_P1_ADR3
Address	80004C2A0701143F (SCOM)
Description	Currently reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	Reserved.

Register Name	ADR RESERVED 10 Register
Mnemonic	IOM0.DDRPHY_ADR_RESERVED10_P2_ADR3
Address	80004C2A0701183F (SCOM)
Description	Currently reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	Reserved.

Register Name	ADR RESERVED 10 Register
Mnemonic	IOM0.DDRPHY_ADR_RESERVED10_P3_ADR3
Address	80004C2A07011C3F (SCOM)
Description	Currently reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	Reserved.

Register Name	ADR RESERVED 11 Register
Mnemonic	IOM0.DDRPHY_ADR_RESERVED11_P0_ADR3
Address	80004C2B0701103F (SCOM)
Description	Currently reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	Reserved.

Register Name	ADR RESERVED 11 Register
Mnemonic	IOM0.DDRPHY_ADR_RESERVED11_P1_ADR3
Address	80004C2B0701143F (SCOM)
Description	Currently reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	Reserved.

Register Name	ADR RESERVED 11 Register
Mnemonic	IOM0.DDRPHY_ADR_RESERVED11_P2_ADR3
Address	80004C2B0701183F (SCOM)
Description	Currently reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	Reserved.

Register Name	ADR RESERVED 11 Register
Mnemonic	IOM0.DDRPHY_ADR_RESERVED11_P3_ADR3
Address	80004C2B07011C3F (SCOM)
Description	Currently reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	Reserved.

Register Name	ADR Power Down 2 Register
Mnemonic	IOM0.DDRPHY_ADR_POWERDOWN_2_P0_ADR3
Address	80004C2C0701103F (SCOM)
Description	This register provides control of the ADR power-down modes.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:55	RW	ADR_LANE_0_7_PD: 0 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{0-7} is at high-Z (tri-stated). 1 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{0-7} drives the value programmed in bit 55 the PC Power Down 1 Register at the impedance programmed into the ADR I/O FET Slice Enable Map {0-1} Register.
56:59	RW	ADR_Lane_8_11_PD: ADR12: 0 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{8-11} is at high-Z (tri-stated). 1 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{8-11} drives the value programmed in bit 55 of PC Power Down 1 Register at the impedance programmed into the ADR I/O FET Slice Enable Map {0-1} Register. ADR8: Reserved.
60:63	RW	ADR_LANE_12_15_PD: Reserved.

Register Name	ADR Power Down 2 Register
Mnemonic	IOM0.DDRPHY_ADR_POWERDOWN_2_P1_ADR3
Address	80004C2C0701143F (SCOM)
Description	This register provides control of the ADR power-down modes.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:55	RW	ADR_LANE_0_7_PD: 0 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{0-7} is at high-Z (tri-stated). 1 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{0-7} drives the value programmed in bit 55 the PC Power Down 1 Register at the impedance programmed into the ADR I/O FET Slice Enable Map {0-1} Register.
56:59	RW	ADR_Lane_8_11_PD: ADR12: 0 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{8-11} is at high-Z (tri-stated). 1 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{8-11} drives the value programmed in bit 55 of PC Power Down 1 Register at the impedance programmed into the ADR I/O FET Slice Enable Map {0-1} Register. ADR8: Reserved.
60:63	RW	ADR_LANE_12_15_PD: Reserved.

Register Name	ADR Power Down 2 Register
Mnemonic	IOM0.DDRPHY_ADR_POWERDOWN_2_P2_ADR3
Address	80004C2C0701183F (SCOM)
Description	This register provides control of the ADR power-down modes.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:55	RW	ADR_LANE_0_7_PD: 0 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{0-7} is at high-Z (tri-stated). 1 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{0-7} drives the value programmed in bit 55 the PC Power Down 1 Register at the impedance programmed into the ADR I/O FET Slice Enable Map {0-1} Register.
56:59	RW	ADR_Lane_8_11_PD: ADR12: 0 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{8-11} is at high-Z (tri-stated). 1 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{8-11} drives the value programmed in bit 55 of PC Power Down 1 Register at the impedance programmed into the ADR I/O FET Slice Enable Map {0-1} Register. ADR8: Reserved.
60:63	RW	ADR_LANE_12_15_PD: Reserved.

Register Name	ADR Power Down 2 Register
Mnemonic	IOM0.DDRPHY_ADR_POWERDOWN_2_P3_ADR3
Address	80004C2C07011C3F (SCOM)
Description	This register provides control of the ADR power-down modes.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:55	RW	ADR_LANE_0_7_PD: 0 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{0-7} is at high-Z (tri-stated). 1 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{0-7} drives the value programmed in bit 55 the PC Power Down 1 Register at the impedance programmed into the ADR I/O FET Slice Enable Map {0-1} Register.
56:59	RW	ADR_Lane_8_11_PD: ADR12: 0 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{8-11} is at high-Z (tri-stated). 1 = When bits 48 and 62 of the PC Power Down 1 Register are ‘1’b, MEMINTC{8-11} drives the value programmed in bit 55 of PC Power Down 1 Register at the impedance programmed into the ADR I/O FET Slice Enable Map {0-1} Register. ADR8: Reserved.
60:63	RW	ADR_LANE_12_15_PD: Reserved.

Register Name	ADR DLL Software Control 1 Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_SW_CONTROL_1_P0_ADR32S0
Address	8000802D0701103F (SCOM)
Description	This register enables software to take control of the slave regulators’ VREG controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	SLAVE_VREG_OVERRIDE: When 0, the master regulator controls for REF_SEL and NVT/PVT (derived from VREG_DAC_COARSE) are sent to the slave regulators. This enables the slave to track the master's settings during VREG calibration. When 1, this register takes control over the slave regulator REF_SEL and NVT/PVT (via VREG_DAC_COARSE) inputs. This enables software to manage the master and slave regulators completely independently.
49:51	RW	SLAVE_VREG_REF_SEL_DC: When SLAVE_VREG_OVERRIDE = 0, this field is not used. The master and slave share the master's VREG_REF_SEL_DC(0:2) setting. When SLAVE_VREG_OVERRIDE = 1, this field is sent to the slave regulators as VREG_REF_SEL_DC(0:2).
52:58	RW	SLAVE_VREG_DAC_COARSE: When SLAVE_VREG_OVERRIDE = 0, this field is not used. The master and slave share the master's VREG_DAC_COARSE(0:6) setting. When SLAVE_VREG_OVERRIDE = 1, this field is sent to the slave regulators as VREG_DAC_COARSE(0:6), which is converted to NVT(0:3) and PVT(0:3) by the delay-locked loop (DLL) logic.
59:62	RO	Reserved.
63	RW	DD2_ADR_IE_FIX_DISABLE: 0 = Enable the DD2 function for ADR input enable (IE) assertion when FORCE_MCLK_LOW is asserted. 1 = Enable the DD1 function.

Register Name	ADR DLL Software Control 1 Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_SW_CONTROL_1_P1_ADR32S0
Address	8000802D0701143F (SCOM)
Description	This register enables software to take control of the slave regulators' VREG controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	SLAVE_VREG_OVERRIDE: When 0, the master regulator controls for REF_SEL and NVT/PVT (derived from VREG_DAC_COARSE) are sent to the slave regulators. This enables the slave to track the master's settings during VREG calibration. When 1, this register takes control over the slave regulator REF_SEL and NVT/PVT (via VREG_DAC_COARSE) inputs. This enables software to manage the master and slave regulators completely independently.
49:51	RW	SLAVE_VREG_REF_SEL_DC: When SLAVE_VREG_OVERRIDE = 0, this field is not used. The master and slave share the master's VREG_REF_SEL_DC(0:2) setting. When SLAVE_VREG_OVERRIDE = 1, this field is sent to the slave regulators as VREG_REF_SEL_DC(0:2).
52:58	RW	SLAVE_VREG_DAC_COARSE: When SLAVE_VREG_OVERRIDE = 0, this field is not used. The master and slave share the master's VREG_DAC_COARSE(0:6) setting. When SLAVE_VREG_OVERRIDE = 1, this field is sent to the slave regulators as VREG_DAC_COARSE(0:6), which is converted to NVT(0:3) and PVT(0:3) by the DLL logic.
59:62	RO	Reserved.
63	RW	DD2_ADR_IE_FIX_DISABLE: 0 = Enable the DD2 function for ADR IE assertion when FORCE_MCLK_LOW is asserted. 1 = Enable the DD1 function.

Register Name	ADR DLL Software Control 1 Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_SW_CONTROL_1_P2_ADR32S0
Address	8000802D0701183F (SCOM)
Description	This register enables software to take control of the slave regulators' VREG controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	SLAVE_VREG_OVERRIDE: When 0, the master regulator controls for REF_SEL and NVT/PVT (derived from VREG_DAC_COARSE) are sent to the slave regulators. This enables the slave to track the master's settings during VREG calibration. When 1, this register takes control over the slave regulator REF_SEL and NVT/PVT (via VREG_DAC_COARSE) inputs. This enables software to manage the master and slave regulators completely independently.
49:51	RW	SLAVE_VREG_REF_SEL_DC: When SLAVE_VREG_OVERRIDE = 0, this field is not used. The master and slave share the master's VREG_REF_SEL_DC(0:2) setting. When SLAVE_VREG_OVERRIDE = 1, this field is sent to the slave regulators as VREG_REF_SEL_DC(0:2).
52:58	RW	SLAVE_VREG_DAC_COARSE: When SLAVE_VREG_OVERRIDE = 0, this field is not used. The master and slave share the master's VREG_DAC_COARSE(0:6) setting. When SLAVE_VREG_OVERRIDE = 1, this field is sent to the slave regulators as VREG_DAC_COARSE(0:6), which is converted to NVT(0:3) and PVT(0:3) by the DLL logic.
59:62	RO	Reserved.

Bits	SCOM	Field Mnemonic: Description
63	RW	DD2_ADR_IE_FIX_DISABLE: 0 = Enable the DD2 function for ADR IE assertion when FORCE_MCLK_LOW is asserted. 1 = Enable the DD1 function.

Register Name	ADR DLL Software Control 1 Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_SW_CONTROL_1_P3_ADR32S0
Address	8000802D07011C3F (SCOM)
Description	This register enables software to take control of the slave regulators' VREG controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	RW	SLAVE_VREG_OVERRIDE: When 0, the master regulator controls for REF_SEL and NVT/PVT (derived from VREG_DAC_COARSE) are sent to the slave regulators. This enables the slave to track the master's settings during VREG calibration. When 1, this register takes control over the slave regulator REF_SEL and NVT/PVT (via VREG_DAC_COARSE) inputs. This enables software to manage the master and slave regulators completely independently.
49:51	RW	SLAVE_VREG_REF_SEL_DC: When SLAVE_VREG_OVERRIDE = 0, this field is not used. The master and slave share the master's VREG_REF_SEL_DC(0:2) setting. When SLAVE_VREG_OVERRIDE = 1, this field is sent to the slave regulators as VREG_REF_SEL_DC(0:2).
52:58	RW	SLAVE_VREG_DAC_COARSE: When SLAVE_VREG_OVERRIDE = 0, this field is not used. The master and slave share the master's VREG_DAC_COARSE(0:6) setting. When SLAVE_VREG_OVERRIDE = 1, this field is sent to the slave regulators as VREG_DAC_COARSE(0:6), which is converted to NVT(0:3) and PVT(0:3) by the DLL logic.
59:62	RO	Reserved.
63	RW	DD2_ADR_IE_FIX_DISABLE: 0 = Enable the DD2 function for ADR IE assertion when FORCE_MCLK_LOW is asserted. 1 = Enable the DD1 function.

Register Name	ADR DLL Slave VREG Lower Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_SLAVE_VREG_LOWER_P0_ADR32S0
Address	8000802E0701103F (SCOM)
Description	This register holds the "lower" control for the slave voltage regulators.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:62	RW	SLAVE_VREG_LOWER: This field controls the value of the slave regulators' VREG. Bits set to 1 are independent of each other; it is the total number of them that matters. For example, these settings have the same effect: b100...00, b001...00, b000...10). Adding more 1s increases the VREG. Recommendation: Change the bits in thermometer-code fashion.
63	RO	Constant = 0b0

Register Name	ADR DLL Slave VREG Lower Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_SLAVE_VREG_LOWER_P1_ADR32S0
Address	8000802E0701143F (SCOM)
Description	This register holds the "lower" control for the slave voltage regulators.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:62	RW	SLAVE_VREG_LOWER: This field controls the value of the slave regulators' VREG. Bits set to 1 are independent of each other; it is the total number of them that matters. For example, these settings have the same effect: b100...00, b001...00, b000...10). Adding more 1s increases the VREG. Recommendation: Change the bits in thermometer-code fashion.
63	RO	Constant = 0b0

Register Name	ADR DLL Slave VREG Lower Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_SLAVE_VREG_LOWER_P2_ADR32S0
Address	8000802E0701183F (SCOM)
Description	This register holds the "lower" control for the slave voltage regulators.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:62	RW	SLAVE_VREG_LOWER: This field controls the value of the slave regulators' VREG. Bits set to 1 are independent of each other; it is the total number of them that matters. For example, these settings have the same effect: b100...00, b001...00, b000...10). Adding more 1s increases the VREG. Recommendation: Change the bits in thermometer-code fashion.
63	RO	Constant = 0b0

Register Name	ADR DLL Slave VREG Lower Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_SLAVE_VREG_LOWER_P3_ADR32S0
Address	8000802E07011C3F (SCOM)
Description	This register holds the "lower" control for the slave voltage regulators.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:62	RW	SLAVE_VREG_LOWER: This field controls the value of the slave regulators' VREG. Bits set to 1 are independent of each other; it is the total number of them that matters. For example, these settings have the same effect: b100...00, b001...00, b000...10). Adding more 1s increases the VREG. Recommendation: Change the bits in thermometer-code fashion.
63	RO	Constant = 0b0

Register Name	ADR DLL Slave VREG Upper Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_SLAVE_VREG_UPPER_P0_ADR32S0
Address	8000802F0701103F (SCOM)
Description	This register holds the "upper" control for the slave voltage regulators.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:62	RW	SLAVE_VREG_UPPER: Same behavior as SLAVE_VREG_LOWER, except the effect on VREG is 16 times larger for each bit.
63	RO	Constant = 0b0

Register Name	ADR DLL Slave VREG Upper Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_SLAVE_VREG_UPPER_P1_ADR32S0
Address	8000802F0701143F (SCOM)
Description	This register holds the "upper" control for the slave voltage regulators.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:62	RW	SLAVE_VREG_UPPER: Same behavior as SLAVE_VREG_LOWER, except the effect on VREG is 16 times larger for each bit.
63	RO	Constant = 0b0

Register Name	ADR DLL Slave VREG Upper Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_SLAVE_VREG_UPPER_P2_ADR32S0
Address	8000802F0701183F (SCOM)
Description	This register holds the "upper" control for the slave voltage regulators.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:62	RW	SLAVE_VREG_UPPER: Same behavior as SLAVE_VREG_LOWER, except the effect on VREG is 16 times larger for each bit.
63	RO	Constant = 0b0

Register Name	ADR DLL Slave VREG Upper Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_SLAVE_VREG_UPPER_P3_ADR32S0
Address	8000802F07011C3F (SCOM)
Description	This register holds the "upper" control for the slave voltage regulators.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:62	RW	SLAVE_VREG_UPPER: Same behavior as SLAVE_VREG_LOWER, except the effect on VREG is 16 times larger for each bit.
63	RO	Constant = 0b0

Register Name	ADR DLL Software Control 0 Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_SW_CONTROL_0_P0_ADR32S0
Address	800080300701103F (SCOM)
Description	This register exposes internal delay locked loop (DLL) signals to software to enable it to override the hardware DLL calibration algorithm. META indicates that the signals have safely crossed into the grid clock domain so they should not exhibit metastability. Non-META signals can be read after they stabilize.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	DLL_SW_OVERRIDE: When 0, the hardware DLL algorithm is used. When 1, this register takes control over the DLL analog inputs and outputs allowing firmware to perform calibration.
49	RW	DLL_SW_CAL_PD_ENABLE: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_CAL_PD_ENABLE_SLOW.
50	RW	DLL_SW_MAIN_PD_ENABLE: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_MAIN_PD_ENABLE_SLOW.
51	RW	DLL_SW_DETECT_REQ: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_DETECT_REQ_SLOW.
52	RW	SLAVE_CAL_CKT_POWERDOWN: Control the CAL_CIRCUIT_POWERDOWN input to the slave regulators. When 1, regulators are powered down. When 0, regulators are powered up.
53:55	RO	Constant = 0b000
56	ROX	VREG_RXCAL_COMP_OUT_META: (Read only.) The result of the master VREG comparator, used during VREG calibration. 1 = VREG is less than the reference set by REF_SEL(0:2). 0 = VREG is greater than the reference set by REF_SEL(0:2).
57	ROX	RXCAL_DETECT_DONE_META: (Read only.) Used during coarse and fine calibration. When 0, it means that the analog lead/lag comparator values are still being determined. When 1, it means that the analog lead/lag comparator values are valid and ready to read.
58	ROX	RXCAL_PD_CAL_LAG_META: (Read only.) Used during coarse and fine calibration. 1 = Grid clock and 67.5 degree delay line output clock are in a lag relationship. 0 = Indeterminate. Either the CAL PD filter/phase detector needs more time to evaluate, or the clocks are in a lead relationship.
59	ROX	RXCAL_PD_MAIN_LEAD_META: (Read only.) Used during coarse and fine calibration. 1 = Grid clock and 360 degree delay line output clock are in a lead relationship. 0 = Indeterminate. Either the main PD filter/phase detector needs more time to evaluate or the clocks are in a lag relationship.
60	ROX	RXCAL_PD_MAIN_LAG_META: (Read only.) Used during coarse and fine calibration. 1 = Grid clock and 360 degree delay line output clock are in a lag relationship. 0 = Indeterminate. Either the main PD filter/phase detector needs more time to evaluate, or clocks are in a lead relationship.
61	ROX	VREG_SLAVE1_COMP_OUT: (Read only.) Result of the slave 1 VREG comparator. 1 = VREG is less than the reference set by REF_SEL(0:2). 0 = VREG is greater than the reference set by REF_SEL(0:2). It is safe to read 256 grid clock cycles after REF_SEL is changed.
62	ROX	VREG_SLAVE2_COMP_OUT: (Read only.) Result of the slave 2 VREG comparator. 1 = VREG is less than the reference set by REF_SEL(0:2). 0 = VREG is greater than the reference set by REF_SEL(0:2). It is safe to read 256 grid clock cycles after REF_SEL is changed.
63	RO	Reserved.

Register Name	ADR DLL Software Control 0 Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_SW_CONTROL_0_P1_ADR32S0
Address	800080300701143F (SCOM)
Description	This register exposes internal delay locked loop (DLL) signals to software to enable it to override the hardware DLL calibration algorithm. META indicates that the signals have safely crossed into the grid clock domain so they should not exhibit metastability. Non-META signals can be read after they stabilize.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	DLL_SW_OVERRIDE: When 0, the hardware DLL algorithm is used. When 1, this register takes control over the DLL analog inputs and outputs allowing firmware to perform calibration.
49	RW	DLL_SW_CAL_PD_ENABLE: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_CAL_PD_ENABLE_SLOW.
50	RW	DLL_SW_MAIN_PD_ENABLE: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_MAIN_PD_ENABLE_SLOW.
51	RW	DLL_SW_DETECT_REQ: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_DETECT_REQ_SLOW.
52	RW	SLAVE_CAL_CKT_POWERDOWN: Control the CAL_CIRCUIT_POWERDOWN input to the slave regulators. When 1, regulators are powered down. When 0, regulators are powered up.
53:55	RO	Constant = 0b000
56	ROX	VREG_RXCAL_COMP_OUT_META: (Read only.)The result of the master VREG comparator, used during VREG calibration. 1 = VREG is less than the reference set by REF_SEL(0:2). 0 = VREG is greater than the reference set by REF_SEL(0:2).
57	ROX	RXCAL_DETECT_DONE_META: (Read only.) Used during coarse and fine calibration. When 0, it means that the analog lead/lag comparator values are still being determined. When 1, it means that the analog lead/lag comparator values are valid and ready to read.
58	ROX	RXCAL_PD_CAL_LAG_META: (Read only.) Used during coarse and fine calibration. 1 = Grid clock and 67.5 degree delay line output clock are in a lag relationship. 0 = Indeterminate. Either the CAL PD filter/phase detector needs more time to evaluate, or the clocks are in a lead relationship.
59	ROX	RXCAL_PD_MAIN_LEAD_META: (Read only.) Used during coarse and fine calibration. 1 = Grid clock and 360 degree delay line output clock are in a lead relationship. 0 = Indeterminate. Either the main PD filter/phase detector needs more time to evaluate, or clocks are in a lag relationship.
60	ROX	RXCAL_PD_MAIN_LAG_META: (Read only.) Used during coarse and fine calibration. 1 = Grid clock and 360 degree delay line output clock are in a lag relationship. 0 = Indeterminate. Either the main PD filter/phase detector needs more time to evaluate, or clocks are in a lead relationship.
61	ROX	VREG_SLAVE1_COMP_OUT: (Read only.) Result of the slave 1 VREG comparator. 1 = VREG is less than the reference set by REF_SEL(0:2). 0 = VREG is greater than the reference set by REF_SEL(0:2). It is safe to read 256 grid clock cycles after REF_SEL is changed.

Bits	SCOM	Field Mnemonic: Description
62	ROX	VREG_SLAVE2_COMP_OUT: (Read only.) Result of the slave 2 VREG comparator. 1 = VREG is less than the reference set by REF_SEL(0:2). 0 = VREG is greater than the reference set by REF_SEL(0:2). It is safe to read 256 grid clock cycles after REF_SEL is changed.
63	RO	Reserved.

Register Name	ADR DLL Software Control 0 Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_SW_CONTROL_0_P2_ADR32S0
Address	800080300701183F (SCOM)
Description	This register exposes internal delay locked loop (DLL) signals to software to enable it to override the hardware DLL calibration algorithm. META indicates that the signals have safely crossed into the grid clock domain so they should not exhibit metastability. Non-META signals can be read after they stabilize.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48	RW	DLL_SW_OVERRIDE: When 0, the hardware DLL algorithm is used. When 1, this register takes control over the DLL analog inputs and outputs allowing firmware to perform calibration.
49	RW	DLL_SW_CAL_PD_ENABLE: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_CAL_PD_ENABLE_SLOW.
50	RW	DLL_SW_MAIN_PD_ENABLE: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_MAIN_PD_ENABLE_SLOW.
51	RW	DLL_SW_DETECT_REQ: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_DETECT_REQ_SLOW.
52	RW	SLAVE_CAL_CKT_POWERDOWN: Control the CAL_CIRCUIT_POWERDOWN input to the slave regulators. When 1, regulators are powered down. When 0, regulators are powered up.
53:55	RO	Constant = 0b000
56	ROX	VREG_RXCAL_COMP_OUT_META: (Read only.)The result of the master VREG comparator, used during VREG calibration. 1 = VREG is less than the reference set by REF_SEL(0:2). 0 = VREG is greater than the reference set by REF_SEL(0:2).
57	ROX	RXCAL_DETECT_DONE_META: (Read only.) Used during coarse and fine calibration. When 0, it means that the analog lead/lag comparator values are still being determined. When 1, it means that the analog lead/lag comparator values are valid and ready to read.
58	ROX	RXCAL_PD_CAL_LAG_META: (Read only.) Used during coarse and fine calibration. 1 = Grid clock and 67.5 degree delay line output clock are in a lag relationship. 0 = Indeterminate. Either the CAL PD filter/phase detector needs more time to evaluate, or the clocks are in a lead relationship.
59	ROX	RXCAL_PD_MAIN_LEAD_META: (Read only.) Used during coarse and fine calibration. 1 = Grid clock and 360 degree delay line output clock are in a lead relationship. 0 = Indeterminate. Either the main PD filter/phase detector needs more time to evaluate, or clocks are in a lag relationship.
60	ROX	RXCAL_PD_MAIN_LAG_META: (Read only.) Used during coarse and fine calibration. 1 = Grid clock and 360 degree delay line output clock are in a lag relationship. 0 = Indeterminate. Either the main PD filter/phase detector needs more time to evaluate, or clocks are in a lead relationship.

Bits	SCOM	Field Mnemonic: Description
61	ROX	VREG_SLAVE1_COMP_OUT: (Read only.) Result of the slave 1 VREG comparator. 1 = VREG is less than the reference set by REF_SEL(0:2). 0 = VREG is greater than the reference set by REF_SEL(0:2). It is safe to read 256 grid clock cycles after REF_SEL is changed.
62	ROX	VREG_SLAVE2_COMP_OUT: (Read only.) Result of the slave 2 VREG comparator. 1 = VREG is less than the reference set by REF_SEL(0:2). 0 = VREG is greater than the reference set by REF_SEL(0:2). It is safe to read 256 grid clock cycles after REF_SEL is changed.
63	RO	Reserved.

Register Name	ADR DLL Software Control 0 Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_SW_CONTROL_0_P3_ADR32S0
Address	8000803007011C3F (SCOM)
Description	This register exposes internal delay locked loop (DLL) signals to software to enable it to override the hardware DLL calibration algorithm. META indicates that the signals have safely crossed into the grid clock domain so they should not exhibit metastability. Non-META signals can be read after they stabilize.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48	RW	DLL_SW_OVERRIDE: When 0, the hardware DLL algorithm is used. When 1, this register takes control over the DLL analog inputs and outputs allowing firmware to perform calibration.
49	RW	DLL_SW_CAL_PD_ENABLE: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_CAL_PD_ENABLE_SLOW.
50	RW	DLL_SW_MAIN_PD_ENABLE: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_MAIN_PD_ENABLE_SLOW.
51	RW	DLL_SW_DETECT_REQ: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_DETECT_REQ_SLOW.
52	RW	SLAVE_CAL_CKT_POWERDOWN: Control the CAL_CIRCUIT_POWERDOWN input to the slave regulators. When 1, regulators are powered down. When 0, regulators are powered up.
53:55	RO	Constant = 0b000
56	ROX	VREG_RXCAL_COMP_OUT_META: (Read only.)The result of the master VREG comparator, used during VREG calibration. 1 = VREG is less than the reference set by REF_SEL(0:2). 0 = VREG is greater than the reference set by REF_SEL(0:2).
57	ROX	RXCAL_DETECT_DONE_META: (Read only.) Used during coarse and fine calibration. When 0, it means that the analog lead/lag comparator values are still being determined. When 1, it means that the analog lead/lag comparator values are valid and ready to read.
58	ROX	RXCAL_PD_CAL_LAG_META: (Read only.) Used during coarse and fine calibration. 1 = Grid clock and 67.5 degree delay line output clock are in a lag relationship. 0 = Indeterminate. Either the CAL PD filter/phase detector needs more time to evaluate, or the clocks are in a lead relationship.
59	ROX	RXCAL_PD_MAIN_LEAD_META: (Read only.) Used during coarse and fine calibration. 1 = Grid clock and 360 degree delay line output clock are in a lead relationship. 0 = Indeterminate. Either the main PD filter/phase detector needs more time to evaluate, or clocks are in a lag relationship.

Bits	SCOM	Field Mnemonic: Description
60	ROX	RXCAL_PD_MAIN_LAG_META: (Read only.) Used during coarse and fine calibration. 1 = Grid clock and 360 degree delay line output clock are in a lag relationship. 0 = Indeterminate. Either the main PD filter/phase detector needs more time to evaluate, or clocks are in a lead relationship.
61	ROX	VREG_SLAVE1_COMP_OUT: (Read only.) Result of the slave 1 VREG comparator. 1 = VREG is less than the reference set by REF_SEL(0:2). 0 = VREG is greater than the reference set by REF_SEL(0:2). It is safe to read 256 grid clock cycles after REF_SEL is changed.
62	ROX	VREG_SLAVE2_COMP_OUT: (Read only.) Result of the slave 2 VREG comparator. 1 = VREG is less than the reference set by REF_SEL(0:2). 0 = VREG is greater than the reference set by REF_SEL(0:2). It is safe to read 256 grid clock cycles after REF_SEL is changed.
63	RO	Reserved.

Register Name	ADR DLL/VREG Configuration 1 Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_VREG_CONFIG_1_P0_ADR32S0
Address	800080310701103F (SCOM)
Description	This is the second of two registers that configure a variety of DLL and VREG programming values.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	HS_DLLMUX_SEL_0_3: Select 1 of 16 DLL phases to send out to the high-speed MUX structure.
52:53	RW	Reserved.
54	RW	Reserved.
55:56	RW	Reserved.
57:58	RW	Reserved.
59:62	RW	STRENGTH: Phase rotator strength bits. Set this field as follows for the given data rate: 0000 = DDR PHY is not operational. 0001 = 1866 megatransfers per second (MT/s). 0010 = 2133 MT/s. 0100 = 2400 MT/s. 1000 = 2666 MT/s. All other values are reserved.
63	RW	ANALOG_WRAPON: Wrap data control to the attached ADR12s or ADR8s.

Register Name	ADR DLL/VREG Configuration 1 Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_VREG_CONFIG_1_P1_ADR32S0
Address	800080310701143F (SCOM)
Description	This is the second of two registers that configure a variety of DLL and VREG programming values.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	HS_DLLMUX_SEL_0_3: Select 1 of 16 DLL phases to send out to the high-speed MUX structure.

Bits	SCOM	Field Mnemonic: Description
52:53	RW	Reserved.
54	RW	Reserved.
55:56	RW	Reserved.
57:58	RW	Reserved.
59:62	RW	STRENGTH: Phase rotator strength bits. Set this field as follows for the given data rate: 0000 = DDR PHY is not operational. 0001 = 1866 MT/s. 0010 = 2133 MT/s. 0100 = 2400 MT/s. 1000 = 2666 MT/s. All other values are reserved.
63	RW	ANALOG_WRAPON: Wrap data control to the attached ADR12s or ADR8s.

Register Name	ADR DLL/VREG Configuration 1 Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_VREG_CONFIG_1_P2_ADR32S0
Address	800080310701183F (SCOM)
Description	This is the second of two registers that configure a variety of DLL and VREG programming values.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	HS_DLLMUX_SEL_0_3: Select 1 of 16 DLL phases to send out to the high-speed MUX structure.
52:53	RW	Reserved.
54	RW	Reserved.
55:56	RW	Reserved.
57:58	RW	Reserved.
59:62	RW	STRENGTH: Phase rotator strength bits. Set this field as follows for the given data rate: 0000 = DDR PHY is not operational. 0001 = 1866 MT/s. 0010 = 2133 MT/s. 0100 = 2400 MT/s. 1000 = 2666 MT/s. All other values are reserved.
63	RW	ANALOG_WRAPON: Wrap data control to the attached ADR12s or ADR8s.

Register Name	ADR DLL/VREG Configuration 1 Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_VREG_CONFIG_1_P3_ADR32S0
Address	8000803107011C3F (SCOM)
Description	This is the second of two registers that configure a variety of DLL and VREG programming values.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	HS_DLLMUX_SEL_0_3: Select 1 of 16 DLL phases to send out to the high-speed MUX structure.

Bits	SCOM	Field Mnemonic: Description
52:53	RW	Reserved.
54	RW	Reserved.
55:56	RW	Reserved.
57:58	RW	Reserved.
59:62	RW	STRENGTH: Phase rotator strength bits. Set this field as follows for the given data rate: 0000 = DDR PHY is not operational. 0001 = 1866 MT/s. 0010 = 2133 MT/s. 0100 = 2400 MT/s. 1000 = 2666 MT/s. All other values are reserved.
63	RW	ANALOG_WRAPON: Wrap data control to the attached ADR12s or ADR8s.

Register Name	ADR SysClk Phase Rotator Control Register
Mnemonic	IOM0.DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR32S0
Address	800080320701103F (SCOM)
Description	This register controls the circuit that aligns the internal SysClk to the incoming dphy_gckn clock.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	SYSCLK_ROT_OVERRIDE: This field has a dual purpose: override control and lock control. When SYSCLK_ROT_OVERRIDE_EN = 1, this field is in override control mode. When SYSCLK_ROT_OVERRIDE_EN = 0, this field is in lock control. For override control: System clock (SysClk) phase-rotator override value. The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by four dphy_gckn clock cycles. Back-to-back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field in the ADR SysClk Phase Rotator Value is reserved. For lock control: Write this field to all zeros unless instructed otherwise by your IBM representative. bit 2: Lock select. Selects between lock status and sticky lock. 0 = Selects the current status of the lock. When the dphy_gckn detect has reached alignment between the dphy_gckn and SysClk, the BB_LOCK field in the ADR SysClk Phase Rotator Value Register is asserted. 1 = Selects the sticky lock to the BB_LOCK field in the ADR SysClk Phase Rotator Value. The sticky lock is controlled by bit 4, sticky lock enable. When the sticky lock is set, it remains set. bit 4: Sticky lock enable. bits 5:7: Adjustable BB_LOCK window: 000 = At most, a one-count increment or decrement occurs to indicate a lock. 001 = At most, a two-count increment or decrement occurs to indicate a lock. 010 = At most, a three-count increment or decrement occurs to indicate a lock. 011 = At most, a four-count increment or decrement occurs to indicate a lock. 100 = At most, a five-count increment or decrement occurs to indicate a lock.

Bits	SCOM	Field Mnemonic: Description
56	RW	SYSCLK_ROT_OVERRIDE_EN: Enables the use of the SYSCLK_ROT_OVERRIDE register value rather than the internally calculated SYSCLK_ROT value in the ADR SysClk Phase Rotator Value Register when set to 1. The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by four dphy_gckn clock cycles. Back-to-back APB write operations to this register provide the required separation. When this bit is written to 0 and was 1, the SYSCLK_ROT value in the ADR SysClk Phase Rotator Value Register is reset to zero.
57	RW	SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_gckn, the SysClk Phase Alignment Controller. This bit must be asserted after the PLL locks; it must be active for at least five SysClk cycles.
58	RW	SYSCLK_PHASE_CNTL_EN: Alignment enable to dphy_gckn, the SysClk Phase Alignment Controller. When high, it enables the controller. This bit must be asserted low at least 25 SysClk cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.
59	RW	SYSCLK_PHASE_DEFAULT_EN: This bit enables default start-up values to be output by dphy_gckn, the SysClk Phase Alignment Controller. This bit must be asserted during system reset and de-asserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	SYSCLK_POS_EDGE_ALIGN: This bit must be 0 for proper functional operation. It is an edge alignment strap to dphy_gckn, the SysClk Phase Alignment Controller. When high, it enables positive-edge alignment between dphy_gckn and SysClk. When low, it enables negative-edge alignment between dphy_gckn and SysClk. This bit is required to be low for ADR (negative-edge alignment).
61	RW	CONTINUOUS_UPDATE: 1 = The dphy_gckn, the SysClk Phase Alignment Controller, runs continuously and, thus, continuously aligns the dphy_gckn clock to the internal SysClk clock. 0 = The dphy_gckn, the SysClk Phase Alignment Controller, is only updated periodically under hardware control when an update will not interfere with the PHY functional operations.
62	RW	Reserved.
63	RW	DD2_ADR_CG_DISABLE: 0 = Enable DD2 enhanced clock gating on ADR registers. 1 = Enable DD1 function.

Register Name	ADR SysClk Phase Rotator Control Register
Mnemonic	IOM0.DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR32S0
Address	800080320701143F (SCOM)
Description	This register controls the circuit that aligns the internal SysClk to the incoming dphy_gckn clock.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	Reserved.

Bits	SCOM	Field Mnemonic: Description
49:55	RW	SYSCLK_ROT_OVERRIDE: This field has a dual purpose: override control and lock control. When SYSCLK_ROT_OVERRIDE_EN = 1, this field is in override control mode. When SYSCLK_ROT_OVERRIDE_EN = 0, this field is in lock control. For override control: System clock (SysClk) phase-rotator override value. The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by four dphy_gckn clock cycles. Back-to-back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field in the ADR SysClk Phase Rotator Value Register is reserved. For lock control: Write this field to all zeros unless instructed otherwise by your IBM representative. bit 2: Lock select. Selects between lock status and sticky lock. 0 = Selects the current status of the lock. When the dphy_gckn detect has reached alignment between the dphy_gckn and SysClk, the BB_LOCK field in the ADR SysClk Phase Rotator Value Register is asserted. 1 = Selects the sticky lock to the BB_LOCK field in the ADR SysClk Phase Rotator Value Register. The sticky lock is controlled by bit 4, sticky lock enable. When the sticky lock is set, it remains set. bit 4: Sticky lock enable. bits 5:7: Adjustable BB_LOCK window: 000 = At most, a one-count increment or decrement occurs to indicate a lock. 001 = At most, a two-count increment or decrement occurs to indicate a lock. 010 = At most, a three-count increment or decrement occurs to indicate a lock. 011 = At most, a four-count increment or decrement occurs to indicate a lock. 100 = At most, a five-count increment or decrement occurs to indicate a lock.
56	RW	SYSCLK_ROT_OVERRIDE_EN: Enables the use of the SYSCLK_ROT_OVERRIDE register value rather than the internally calculated SYSCLK_ROT value in the ADR SysClk Phase Rotator Value Register when set to 1. The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by four dphy_gckn clock cycles. Back-to-back APB write operations to this register provide the required separation. When this bit is written to 0 and was 1, the SYSCLK_ROT value in the ADR SysClk Phase Rotator Value Register is reset to zero.
57	RW	SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_gckn, the SysClk Phase Alignment Controller. This bit must be asserted after the PLL locks; it must be active for at least five SysClk cycles.
58	RW	SYSCLK_PHASE_CNTL_EN: Alignment enable to dphy_gckn, the SysClk Phase Alignment Controller. When high, it enables the controller. This bit must be asserted low at least 25 SysClk cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.
59	RW	SYSCLK_PHASE_DEFAULT_EN: This bit enables default start-up values to be output by dphy_gckn, the SysClk Phase Alignment Controller. This bit must be asserted during system reset and de-asserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	SYSCLK_POS_EDGE_ALIGN: This bit must be 0 for proper functional operation. It is an edge alignment strap to dphy_gckn, the SysClk Phase Alignment Controller. When high, it enables positive-edge alignment between dphy_gckn and SysClk. When low, it enables negative-edge alignment between dphy_gckn and SysClk. This bit is required to be low for ADR (negative-edge alignment).
61	RW	CONTINUOUS_UPDATE: 1 = The dphy_gckn, the SysClk Phase Alignment Controller, runs continuously and, thus, continuously aligns the dphy_gckn clock to the internal SysClk clock. 0 = The dphy_gckn, the SysClk Phase Alignment Controller, is only updated periodically under hardware control when an update will not interfere with the PHY functional operations.
62	RW	Reserved.

Bits	SCOM	Field Mnemonic: Description
63	RW	DD2_ADR_CG_DISABLE: 0 = Enable DD2 enhanced clock gating on ADR registers. 1 = Enable DD1 function.

Register Name	**ADR SysClk Phase Rotator Control Register**
Mnemonic	IOM0.DDRPHY_ADR_SYSCLK_CNTL_PR_P2_ADR32S0
Address	800080320701183F (SCOM)
Description	This register controls the circuit that aligns the internal SysClk to the incoming dphy_gckn clock.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	SYSCLK_ROT_OVERRIDE: This field has a dual purpose: override control and lock control. When SYSCLK_ROT_OVERRIDE_EN = 1, this field is in override control mode. When SYSCLK_ROT_OVERRIDE_EN = 0, this field is in lock control. For override control: System clock (SysClk) phase-rotator override value. The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by four dphy_gckn clock cycles. Back-to-back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field in the ADR SysClk Phase Rotator Value Register is reserved. For lock control: Write this field to all zeros unless instructed otherwise by your IBM representative. bit 2: Lock select. Selects between lock status and sticky lock. 0 = Selects the current status of the lock. When the dphy_gckn detect has reached alignment between the dphy_gckn and SysClk, the BB_LOCK field in the ADR SysClk Phase Rotator Value Register is asserted. 1 = Selects the sticky lock to the BB_LOCK field in the ADR SysClk Phase Rotator Value Register. The sticky lock is controlled by bit 4, sticky lock enable. When the sticky lock is set, it remains set. bit 4: Sticky lock enable. bits 5:7: Adjustable BB_LOCK window: 000 = At most, a one-count increment or decrement occurs to indicate a lock. 001 = At most, a two-count increment or decrement occurs to indicate a lock. 010 = At most, a three-count increment or decrement occurs to indicate a lock. 011 = At most, a four-count increment or decrement occurs to indicate a lock. 100 = At most, a five-count increment or decrement occurs to indicate a lock.
56	RW	SYSCLK_ROT_OVERRIDE_EN: Enables the use of the SYSCLK_ROT_OVERRIDE register value rather than the internally calculated SYSCLK_ROT value in the ADR SysClk Phase Rotator Value Register when set to 1. The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by four dphy_gckn clock cycles. Back-to-back APB write operations to this register provide the required separation. When this bit is written to 0 and was 1, the SYSCLK_ROT value in the ADR SysClk Phase Rotator Value Register is reset to zero.
57	RW	SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_gckn, the SysClk Phase Alignment Controller. This bit must be asserted after the PLL locks; it must be active for at least five SysClk cycles.
58	RW	SYSCLK_PHASE_CNTL_EN: Alignment enable to dphy_gckn, the SysClk Phase Alignment Controller. When high, it enables the controller. This bit must be asserted low at least 25 SysClk cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.

Bits	SCOM	Field Mnemonic: Description
59	RW	SYSCLK_PHASE_DEFAULT_EN: This bit enables default start-up values to be output by dphy_gckn, the SysClk Phase Alignment Controller. This bit must be asserted during system reset and de-asserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	SYSCLK_POS_EDGE_ALIGN: This bit must be 0 for proper functional operation. It is an edge alignment strap to dphy_gckn, the SysClk Phase Alignment Controller. When high, it enables positive-edge alignment between dphy_gckn and SysClk. When low, it enables negative-edge alignment between dphy_gckn and SysClk. This bit is required to be low for ADR (negative-edge alignment).
61	RW	CONTINUOUS_UPDATE: 1 = The dphy_gckn, the SysClk Phase Alignment Controller, runs continuously and, thus, continuously aligns the dphy_gckn clock to the internal SysClk clock. 0 = The dphy_gckn, the SysClk Phase Alignment Controller, is only updated periodically under hardware control when an update will not interfere with the PHY functional operations.
62	RW	Reserved.
63	RW	DD2_ADR_CG_DISABLE: 0 = Enable DD2 enhanced clock gating on ADR registers. 1 = Enable DD1 function.

Register Name	ADR SysClk Phase Rotator Control Register
Mnemonic	IOM0.DDRPHY_ADR_SYSCLK_CNTL_PR_P3_ADR32S0
Address	8000803207011C3F (SCOM)
Description	This register controls the circuit that aligns the internal SysClk to the incoming dphy_gckn clock.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	SYSCLK_ROT_OVERRIDE: This field has a dual purpose: override control and lock control. When SYSCLK_ROT_OVERRIDE_EN = 1, this field is in override control mode. When SYSCLK_ROT_OVERRIDE_EN = 0, this field is in lock control. For override control: System clock (SysClk) phase-rotator override value. The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by four dphy_gckn clock cycles. Back-to-back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field in the ADR SysClk Phase Rotator Value Register is reserved. For lock control: Write this field to all zeros unless instructed otherwise by your IBM representative. bit 2: Lock select. Selects between lock status and sticky lock. 0 = Selects the current status of the lock. When the dphy_gckn detect has reached alignment between the dphy_gckn and SysClk, the BB_LOCK field in the ADR SysClk Phase Rotator Value Register is asserted. 1 = Selects the sticky lock to the BB_LOCK field in the ADR SysClk Phase Rotator Value. Register The sticky lock is controlled by bit 4, sticky lock enable. When the sticky lock is set, it remains set. bit 4: Sticky lock enable. bits 5:7: Adjustable BB_LOCK window: 000 = At most, a one-count increment or decrement occurs to indicate a lock. 001 = At most, a two-count increment or decrement occurs to indicate a lock. 010 = At most, a three-count increment or decrement occurs to indicate a lock. 011 = At most, a four-count increment or decrement occurs to indicate a lock. 100 = At most, a five-count increment or decrement occurs to indicate a lock.

Bits	SCOM	Field Mnemonic: Description
56	RW	SYSCLK_ROT_OVERRIDE_EN: Enables the use of the SYSCLK_ROT_OVERRIDE register value rather than the internally calculated SYSCLK_ROT value in the ADR SysClk Phase Rotator Value Register when set to 1. The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by four dphy_gckn clock cycles. Back-to-back APB write operations to this register provide the required separation. When this bit is written to 0 and was 1, the SYSCLK_ROT value in the ADR SysClk Phase Rotator Value Register is reset to zero.
57	RW	SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_gckn, the SysClk Phase Alignment Controller. This bit must be asserted after the PLL locks; it must be active for at least five SysClk cycles.
58	RW	SYSCLK_PHASE_CNTL_EN: Alignment enable to dphy_gckn, the SysClk Phase Alignment Controller. When high, it enables the controller. This bit must be asserted low at least 25 SysClk cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.
59	RW	SYSCLK_PHASE_DEFAULT_EN: This bit enables default start-up values to be output by dphy_gckn, the SysClk Phase Alignment Controller. This bit must be asserted during system reset and de-asserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	SYSCLK_POS_EDGE_ALIGN: This bit must be 0 for proper functional operation. It is an edge alignment strap to dphy_gckn, the SysClk Phase Alignment Controller. When high, it enables positive-edge alignment between dphy_gckn and SysClk. When low, it enables negative-edge alignment between dphy_gckn and SysClk. This bit is required to be low for ADR (negative-edge alignment).
61	RW	CONTINUOUS_UPDATE: 1 = The dphy_gckn, the SysClk Phase Alignment Controller, runs continuously and, thus, continuously aligns the dphy_gckn clock to the internal SysClk clock. 0 = The dphy_gckn, the SysClk Phase Alignment Controller, is only updated periodically under hardware control when an update will not interfere with the PHY functional operations.
62	RW	Reserved.
63	RW	DD2_ADR_CG_DISABLE: 0 = Enable DD2 enhanced clock gating on ADR registers. 1 = Enable DD1 function.

Register Name	ADR WRClk Phase Rotator Offset Value Register
Mnemonic	IOM0.DDRPHY_ADR_MCCLK_WRCLK_PR_STATIC_OFFSET_P0_ADR32S0
Address	800080330701103F (SCOM)
Description	The phase rotator static offset value is used to determine the phase of the WrClk with respect to the SysClk.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	TSYS_WRCLK: The static value of the system clock (SysClk) phase rotator to the write clock (WrClk) phase rotator. Set to ‘19’h for 2666 MT/s. Set to ‘17’h for 2400 MT/s. Set to ‘14’h for 2133 MT/s. Set to ‘12’h for 1866 MT/s. For zero-delay simulations, or simulations where the delay of the SysClk tree and the WrClk tree are equal, set this field to 60h.
56:63	RW	Reserved.

Register Name	ADR WRClk Phase Rotator Offset Value Register
Mnemonic	IOM0.DDRPHY_ADR_MCCLK_WRCLK_PR_STATIC_OFFSET_P1_ADR32S0
Address	800080330701143F (SCOM)
Description	The phase rotator static offset value is used to determine the phase of the WrClk with respect to the SysClk.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	TSYS_WRCLK: The static value of the system clock (SysClk) phase rotator to the write clock (WrClk) phase rotator. Set to ‘19’h for 2666 MT/s. Set to ‘17’h for 2400 MT/s. Set to ‘14’h for 2133 MT/s. Set to ‘12’h for 1866 MT/s. For zero-delay simulations, or simulations where the delay of the SysClk tree and the WrClk tree are equal, set this field to 60h.
56:63	RW	Reserved.

Register Name	ADR WRClk Phase Rotator Offset Value Register
Mnemonic	IOM0.DDRPHY_ADR_MCCLK_WRCLK_PR_STATIC_OFFSET_P2_ADR32S0
Address	800080330701183F (SCOM)
Description	The phase rotator static offset value is used to determine the phase of the WrClk with respect to the SysClk.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	TSYS_WRCLK: The static value of the system clock (SysClk) phase rotator to the write clock (WrClk) phase rotator. Set to ‘19’h for 2666 MT/s. Set to ‘17’h for 2400 MT/s. Set to ‘14’h for 2133 MT/s. Set to ‘12’h for 1866 MT/s. For zero-delay simulations, or simulations where the delay of the SysClk tree and the WrClk tree are equal, set this field to 60h.
56:63	RW	Reserved.

Register Name	ADR WRClk Phase Rotator Offset Value Register
Mnemonic	IOM0.DDRPHY_ADR_MCCLK_WRCLK_PR_STATIC_OFFSET_P3_ADR32S0
Address	8000803307011C3F (SCOM)
Description	The phase rotator static offset value is used to determine the phase of the WrClk with respect to the SysClk.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	Reserved.

Bits	SCOM	Field Mnemonic: Description
49:55	RW	TSYS_WRCLK: The static value of the system clock (SysClk) phase rotator to the write clock (WrClk) phase rotator. Set to '19'h for 2666 MT/s. Set to '17'h for 2400 MT/s. Set to '14'h for 2133 MT/s. Set to '12'h for 1866 MT/s. For zero-delay simulations, or simulations where the delay of the SysClk tree and the WrClk tree are equal, set this field to 60h.
56:63	RW	Reserved.

Register Name	ADR SysClk Phase Rotator Value Register
Mnemonic	IOM0.DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P0_ADR32S0
Address	800080340701103F (SCOM)
Description	This register provides read-only access to the value of the SysClk phase rotator calculated value, which represents the phase difference between the MCClk phase and SysClk initial phase.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	ROX	SYSCLK_ROT: Internally calculated value of the dphy_gckn clock phase to the SysClock (SysClk) phase offset. Used to set the SysClock phase rotator when SYSCLK_ROT_OVERRIDE_EN = 0. For more information, see the ADR SysClk Phase Rotator Control Register. These bits reset, but are continually loaded with the dphy_gckn to SysClk alignment circuit calculated value for the SysClk delay, exclusive of reset.
56	RO	BB_LOCK: 1 = The dphy_gckn/SysClk phase-alignment controller has reached alignment between the dphy_gckn and SysClk as of the last update by the dphy_gckn/SysClk phase-alignment controller. 0 = The dphy_gckn and SysClk are not in alignment as of the last update by the dphy_gckn/SysClk phase-alignment controller. There are two types of locks. Refer to the SYSCLK_ROT_OVERRIDE field in the ADR SysClk Phase Rotator Control Register.
57:63	RO	Reserved.

Register Name	ADR SysClk Phase Rotator Value Register
Mnemonic	IOM0.DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P1_ADR32S0
Address	800080340701143F (SCOM)
Description	This register provides read-only access to the value of the SysClk phase rotator calculated value, which represents the phase difference between the MCClk phase and SysClk initial phase.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	ROX	SYSCLK_ROT: Internally calculated value of the dphy_gckn clock phase to the SysClock (SysClk) phase offset. Used to set the SysClock phase rotator when SYSCLK_ROT_OVERRIDE_EN = 0. For more information, see the ADR SysClk Phase Rotator Control Register. These bits reset, but are continually loaded with the dphy_gckn to SysClk alignment circuit calculated value for the SysClk delay, exclusive of reset.

Bits	SCOM	Field Mnemonic: Description
56	RO	BB_LOCK: 1 = The dphy_gckn/SysClk phase-alignment controller has reached alignment between the dphy_gckn and SysClk as of the last update by the dphy_gckn/SysClk phase-alignment controller. 0 = The dphy_gckn and SysClk are not in alignment as of the last update by the dphy_gckn/SysClk phase-alignment controller. There are two types of locks. Refer to the SYSCLK_ROT_OVERRIDE field in the ADR SysClk Phase Rotator Control Register.
57:63	RO	Reserved.

Register Name	ADR SysClk Phase Rotator Value Register
Mnemonic	IOM0.DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P2_ADR32S0
Address	800080340701183F (SCOM)
Description	This register provides read-only access to the value of the SysClk phase rotator calculated value, which represents the phase difference between the MCClk phase and SysClk initial phase.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	ROX	SYSCLK_ROT: Internally calculated value of the dphy_gckn clock phase to the SysClock (SysClk) phase offset. Used to set the SysClock phase rotator when SYSCLK_ROT_OVERRIDE_EN = 0. For more information, see the ADR SysClk Phase Rotator Control Register. These bits reset, but are continually loaded with the dphy_gckn to SysClk alignment circuit calculated value for the SysClk delay, exclusive of reset.
56	RO	BB_LOCK: 1 = The dphy_gckn/SysClk phase-alignment controller has reached alignment between the dphy_gckn and SysClk as of the last update by the dphy_gckn/SysClk phase-alignment controller. 0 = The dphy_gckn and SysClk are not in alignment as of the last update by the dphy_gckn/SysClk phase-alignment controller. There are two types of locks. Refer to the SYSCLK_ROT_OVERRIDE field in the ADR SysClk Phase Rotator Control Register.
57:63	RO	Reserved.

Register Name	ADR SysClk Phase Rotator Value Register
Mnemonic	IOM0.DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P3_ADR32S0
Address	8000803407011C3F (SCOM)
Description	This register provides read-only access to the value of the SysClk phase rotator calculated value, which represents the phase difference between the MCClk phase and SysClk initial phase.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	ROX	SYSCLK_ROT: Internally calculated value of the dphy_gckn clock phase to the SysClock (SysClk) phase offset. Used to set the SysClock phase rotator when SYSCLK_ROT_OVERRIDE_EN = 0. For more information, see the ADR SysClk Phase Rotator Control Register. These bits reset, but are continually loaded with the dphy_gckn to SysClk alignment circuit calculated value for the SysClk delay, exclusive of reset.

Bits	SCOM	Field Mnemonic: Description
56	RO	BB_LOCK: 1 = The dphy_gckn/SysClk phase-alignment controller has reached alignment between the dphy_gckn and SysClk as of the last update by the dphy_gckn/SysClk phase-alignment controller. 0 = The dphy_gckn and SysClk are not in alignment as of the last update by the dphy_gckn/SysClk phase-alignment controller. There are two types of locks. Refer to the SYSCLK_ROT_OVERRIDE field in the ADR SysClk Phase Rotator Control Register.
57:63	RO	Reserved.

Register Name	ADR Output Driver Force and ATEST Control Register
Mnemonic	IOM0.DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR32S0
Address	800080350701103F (SCOM)
Description	This register provides control for forcing outputs to known states for characterization and analog test pin (ATEST) control. This register is reserved for manufacturing test and characterization purposes. It resets to a functional value, and its contents must not be altered by the user.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	RW	FLUSH: Manufacturing macro test control for ANALOG. This bit controls whether the transmit FIFO is flushed or not (when flushed, half-rate data is no longer valid).
49	RW	FORCE_EN: Output force enable bit.
50	RW	INIT_IO: Enables the DC-level translator in front of the TX output stages, which initialize the top plate voltage of the fly cap in the AC-level translator at startup. This voltage must be applied for a minimum of five clock cycles after startup, and before the I/Os can be used. This requirement also applies to all manufacturing test modes.
51:54	RW	HS_PROBE_A_SEL_0_3: High-speed probe A select.
55:58	RW	HS_PROBE_B_SEL_0_3: High-speed probe B select.
59:61	RW	ATESTSEL_0_2: Lowest level of ATEST selection, ATESTSEL(0:2).
62:63	RW	Reserved.

Register Name	ADR Output Driver Force and ATEST Control Register
Mnemonic	IOM0.DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR32S0
Address	800080350701143F (SCOM)
Description	This register provides control for forcing outputs to known states for characterization and ATEST control. This register is reserved for manufacturing test and characterization purposes. It resets to a functional value, and its contents must not be altered by the user.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	RW	FLUSH: Manufacturing macro test control for ANALOG. This bit controls whether the transmit FIFO is flushed or not (when flushed, half-rate data is no longer valid).
49	RW	FORCE_EN: Output force enable bit.

Bits	SCOM	Field Mnemonic: Description
50	RW	INIT_IO: Enables the DC-level translator in front of the TX output stages, which initialize the top plate voltage of the fly cap in the AC-level translator at startup. This voltage must be applied for a minimum of five clock cycles after startup, and before the I/Os can be used. This requirement also applies to all manufacturing test modes.
51:54	RW	HS_PROBE_A_SEL_0_3: High-speed probe A select.
55:58	RW	HS_PROBE_B_SEL_0_3: High-speed probe B select.
59:61	RW	ATESTSEL_0_2: Lowest level of ATEST selection, ATESTSEL(0:2).
62:63	RW	Reserved.

Register Name	ADR Output Driver Force and ATEST Control Register
Mnemonic	IOM0.DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P2_ADR32S0
Address	800080350701183F (SCOM)
Description	This register provides control for forcing outputs to known states for characterization and ATEST control. This register is reserved for manufacturing test and characterization purposes. It resets to a functional value, and its contents must not be altered by the user.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	FLUSH: Manufacturing macro test control for ANALOG. This bit controls whether the transmit FIFO is flushed or not (when flushed, half-rate data is no longer valid).
49	RW	FORCE_EN: Output force enable bit.
50	RW	INIT_IO: Enables the DC-level translator in front of the TX output stages, which initialize the top plate voltage of the fly cap in the AC-level translator at startup. This voltage must be applied for a minimum of five clock cycles after startup, and before the I/Os can be used. This requirement also applies to all manufacturing test modes.
51:54	RW	HS_PROBE_A_SEL_0_3: High-speed probe A select.
55:58	RW	HS_PROBE_B_SEL_0_3: High-speed probe B select.
59:61	RW	ATESTSEL_0_2: Lowest level of ATEST selection, ATESTSEL(0:2).
62:63	RW	Reserved.

Register Name	ADR Output Driver Force and ATEST Control Register
Mnemonic	IOM0.DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P3_ADR32S0
Address	8000803507011C3F (SCOM)
Description	This register provides control for forcing outputs to known states for characterization and ATEST control. This register is reserved for manufacturing test and characterization purposes. It resets to a functional value, and its contents must not be altered by the user.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	FLUSH: Manufacturing macro test control for ANALOG. This bit controls whether the transmit FIFO is flushed or not (when flushed, half-rate data is no longer valid).
49	RW	FORCE_EN: Output force enable bit.

Bits	SCOM	Field Mnemonic: Description
50	RW	INIT_IO: Enables the DC-level translator in front of the TX output stages, which initialize the top plate voltage of the fly cap in the AC-level translator at startup. This voltage must be applied for a minimum of five clock cycles after startup, and before the I/Os can be used. This requirement also applies to all manufacturing test modes.
51:54	RW	HS_PROBE_A_SEL_0_3: High-speed probe A select.
55:58	RW	HS_PROBE_B_SEL_0_3: High-speed probe B select.
59:61	RW	ATESTSEL_0_2: Lowest level of ATEST selection, ATESTSEL(0:2).
62:63	RW	Reserved.

Register Name	ADR Output Driver Force Value 0 Register
Mnemonic	IOM0.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE0_P0_ADR32S0
Address	800080360701103F (SCOM)
Description	These registers provide the values to be forced out of the drivers for characterization. Each bit of each register controls its respective lane on the appropriate side. Bits must be enabled in the ADR Bit Enable Register to be controlled by this register. These registers are reserved for manufacturing test and characterization purposes.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	OUTPUT_DRIVER_FORCE_VALUE: The value to be forced out of the driver. Bit assignments represent the respective lanes under test. Reserved.

Register Name	ADR Output Driver Force Value 0 Register
Mnemonic	IOM0.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE0_P1_ADR32S0
Address	800080360701143F (SCOM)
Description	These registers provide the values to be forced out of the drivers for characterization. Each bit of each register controls its respective lane on the appropriate side. Bits must be enabled in the ADR Bit Enable Register to be controlled by this register. These registers are reserved for manufacturing test and characterization purposes.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	OUTPUT_DRIVER_FORCE_VALUE: The value to be forced out of the driver. Bit assignments represent the respective lanes under test. Reserved.

Register Name	ADR Output Driver Force Value 0 Register
Mnemonic	IOM0.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE0_P2_ADR32S0
Address	800080360701183F (SCOM)
Description	These registers provide the values to be forced out of the drivers for characterization. Each bit of each register controls its respective lane on the appropriate side. Bits must be enabled in the ADR Bit Enable Register to be controlled by this register. These registers are reserved for manufacturing test and characterization purposes.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	OUTPUT_DRIVER_FORCE_VALUE: The value to be forced out of the driver. Bit assignments represent the respective lanes under test. Reserved.

Register Name	ADR Output Driver Force Value 0 Register
Mnemonic	IOM0.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE0_P3_ADR32S0
Address	8000803607011C3F (SCOM)
Description	These registers provide the values to be forced out of the drivers for characterization. Each bit of each register controls its respective lane on the appropriate side. Bits must be enabled in the ADR Bit Enable Register to be controlled by this register. These registers are reserved for manufacturing test and characterization purposes.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	OUTPUT_DRIVER_FORCE_VALUE: The value to be forced out of the driver. Bit assignments represent the respective lanes under test. Reserved.

Register Name	ADR Output Driver Force Value 1 Register
Mnemonic	IOM0.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE1_P0_ADR32S0
Address	800080370701103F (SCOM)
Description	These registers provide the values to be forced out of the drivers for characterization. Each bit of each register controls its respective lane on the appropriate side. Bits must be enabled in the ADR Bit Enable Register to be controlled by this register. These registers are reserved for manufacturing test and characterization purposes.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	OUTPUT_DRIVER_FORCE_VALUE: The value to be forced out of the driver. Bit assignments represent the respective lanes under test. Reserved.

Register Name	ADR Output Driver Force Value 1 Register
Mnemonic	IOM0.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE1_P1_ADR32S0
Address	800080370701143F (SCOM)
Description	These registers provide the values to be forced out of the drivers for characterization. Each bit of each register controls its respective lane on the appropriate side. Bits must be enabled in the ADR Bit Enable Register to be controlled by this register. These registers are reserved for manufacturing test and characterization purposes.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	OUTPUT_DRIVER_FORCE_VALUE: The value to be forced out of the driver. Bit assignments represent the respective lanes under test. Reserved.

Register Name	ADR Output Driver Force Value 1 Register
Mnemonic	IOM0.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE1_P2_ADR32S0
Address	800080370701183F (SCOM)
Description	These registers provide the values to be forced out of the drivers for characterization. Each bit of each register controls its respective lane on the appropriate side. Bits must be enabled in the ADR Bit Enable Register to be controlled by this register. These registers are reserved for manufacturing test and characterization purposes.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	OUTPUT_DRIVER_FORCE_VALUE: The value to be forced out of the driver. Bit assignments represent the respective lanes under test. Reserved.

Register Name	ADR Output Driver Force Value 1 Register
Mnemonic	IOM0.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE1_P3_ADR32S0
Address	8000803707011C3F (SCOM)
Description	These registers provide the values to be forced out of the drivers for characterization. Each bit of each register controls its respective lane on the appropriate side. Bits must be enabled in the ADR Bit Enable Register to be controlled by this register. These registers are reserved for manufacturing test and characterization purposes.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	OUTPUT_DRIVER_FORCE_VALUE: The value to be forced out of the driver. Bit assignments represent the respective lanes under test. Reserved.

Register Name	ADR DCD Control Register
Mnemonic	IOM0.DDRPHY_ADR_DCD_CONTROL_P0_ADR32S0
Address	800080380701103F (SCOM)
Description	This register controls the duty cycle distortion (DCD) analog circuitry on the clock feeding the DLL. **Note:** When writing the register, software must write bit 63 to 0b0 to avoid a parity error.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	DLL_DCD_ADJUST: This value controls the amount of duty cycle correction that occurs on the grid clock before it enters the DLL. As the value increases, the clock = 1 part gets longer. As values decrease, the clock = 0 part gets longer. This is the seed value for the DCD calibration algorithm.
56	RW	DLL_DCD_CORRECT_EN: Determine whether the duty cycle distortion logic in the DLL includes a loop to further correct for DCD. 0 = Loop is not included. 1 = Loop is included.
57	RW	DLL_DCD_ITER_A: Controls the connection of DCD comparator input to null out comparator offset. 0 = B answer. 1 = A answer. The A and B answers must be averaged to determine the DLL_DCD_ADJUST value.
58	RW	DLL_DCD_CAL_ENABLE: DCD calibration enable. 0 = Reset the calibration state machine (clears DLL_DCD_CAL_DONE and DLL_DCD_CAL_ERROR). 1 = Enables calibration (calibration is complete with the assertion of DLL_DCD_CAL_DONE).

Bits	SCOM	Field Mnemonic: Description
59	RW	Reserved.
60	RW	DLL_DCD_POWERDOWN: 0 = Normal operation. 1 = Power down the DCD circuit for power savings.
61	RWX	DLL_DCD_CAL_DONE: When DCD_CAL_ENABLE is set, this bit indicates the calibration is complete and the calibrated value has been loaded into the DLL_DCD_ADJUST field of this register.
62	RWX	DLL_DCD_CAL_ERROR: If this bit is asserted along with DLL_DCD_CAL_DONE, it indicates the calibration failed to find a solution. Either DLL_DCD_ADJUST reached a maximum value of 0xFF or a minimum value of 0x00.
63	RO	DLL_DCD_COMPARE_OUT: (Read only.) Result of the DCD comparator. 0 = Need to increase DLL_DCD_ADJUST. 1 = Need to decrease DLL_DCD_ADJUST.

Register Name	ADR DCD Control Register
Mnemonic	IOM0.DDRPHY_ADR_DCD_CONTROL_P1_ADR32S0
Address	800080380701143F (SCOM)
Description	This register controls the duty cycle distortion (DCD) analog circuitry on the clock feeding the DLL. **Note:** When writing the register, software must write bit 63 to 0b0 to avoid a parity error.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	DLL_DCD_ADJUST: This value controls the amount of duty cycle correction that occurs on the grid clock before it enters the DLL. As the value increases, the clock = 1 part gets longer. As values decrease, the clock = 0 part gets longer. This is the seed value for the DCD calibration algorithm.
56	RW	DLL_DCD_CORRECT_EN: Determine whether the duty cycle distortion logic in the DLL includes a loop to further correct for DCD. 0 = Loop is not included. 1 = Loop is included.
57	RW	DLL_DCD_ITER_A: Controls the connection of DCD comparator input to null out comparator offset. 0 = B answer. 1 = A answer. The A and B answers must be averaged to determine the DLL_DCD_ADJUST value.
58	RW	DLL_DCD_CAL_ENABLE: DCD calibration enable. 0 = Reset the calibration state machine (clears DLL_DCD_CAL_DONE and DLL_DCD_CAL_ERROR). 1 = Enables calibration (calibration is complete with the assertion of DLL_DCD_CAL_DONE).
59	RW	Reserved.
60	RWX	DLL_DCD_POWERDOWN: 0 = Normal operation. 1 = Power down the DCD circuit for power savings.
61	RWX	DLL_DCD_CAL_DONE: When DCD_CAL_ENABLE is set, this bit indicates the calibration is complete and the calibrated value has been loaded into the DLL_DCD_ADJUST field of this register.
62	RW	DLL_DCD_CAL_ERROR: If this bit is asserted along with DLL_DCD_CAL_DONE, it indicates the calibration failed to find a solution. Either DLL_DCD_ADJUST reached a maximum value of 0xFF or a minimum value of 0x00.
63	RO	DLL_DCD_COMPARE_OUT: (Read only.) Result of the DCD comparator. 0 = Need to increase DLL_DCD_ADJUST. 1 = Need to decrease DLL_DCD_ADJUST.

Register Name	ADR DCD Control Register
Mnemonic	IOM0.DDRPHY_ADR_DCD_CONTROL_P2_ADR32S0
Address	800080380701183F (SCOM)
Description	This register controls the duty cycle distortion (DCD) analog circuitry on the clock feeding the DLL. **Note:** When writing the register, software must write bit 63 to 0b0 to avoid a parity error.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	DLL_DCD_ADJUST: This value controls the amount of duty cycle correction that occurs on the grid clock before it enters the DLL. As the value increases, the clock = 1 part gets longer. As values decrease, the clock = 0 part gets longer. This is the seed value for the DCD calibration algorithm.
56	RW	DLL_DCD_CORRECT_EN: Determine whether the duty cycle distortion logic in the DLL includes a loop to further correct for DCD. 0 = Loop is not included. 1 = Loop is included.
57	RW	DLL_DCD_ITER_A: Controls the connection of DCD comparator input to null out comparator offset. 0 = B answer. 1 = A answer. The A and B answers must be averaged to determine the DLL_DCD_ADJUST value.
58	RW	DLL_DCD_CAL_ENABLE: DCD calibration enable. 0 = Reset the calibration state machine (clears DLL_DCD_CAL_DONE and DLL_DCD_CAL_ERROR). 1 = Enables calibration (calibration is complete with the assertion of DLL_DCD_CAL_DONE).
59	RW	Reserved.
60	RW	DLL_DCD_POWERDOWN: 0 = Normal operation. 1 = Power down the DCD circuit for power savings.
61	RWX	DLL_DCD_CAL_DONE: When DCD_CAL_ENABLE is set, this bit indicates the calibration is complete and the calibrated value has been loaded into the DLL_DCD_ADJUST field of this register.
62	RWX	DLL_DCD_CAL_ERROR: If this bit is asserted along with DLL_DCD_CAL_DONE, it indicates the calibration failed to find a solution. Either DLL_DCD_ADJUST reached a maximum value of 0xFF or a minimum value of 0x00.
63	RO	DLL_DCD_COMPARE_OUT: (Read only.) Result of the DCD comparator. 0 = Need to increase DLL_DCD_ADJUST. 1 = Need to decrease DLL_DCD_ADJUST.

Register Name	ADR DCD Control Register
Mnemonic	IOM0.DDRPHY_ADR_DCD_CONTROL_P3_ADR32S0
Address	8000803807011C3F (SCOM)
Description	This register controls the duty cycle distortion (DCD) analog circuitry on the clock feeding the DLL. **Note:** When writing the register, software must write bit 63 to 0b0 to avoid a parity error.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	DLL_DCD_ADJUST: This value controls the amount of duty cycle correction that occurs on the grid clock before it enters the DLL. As the value increases, the clock = 1 part gets longer. As values decrease, the clock = 0 part gets longer. This is the seed value for the DCD calibration algorithm.

Bits	SCOM	Field Mnemonic: Description
56	RW	DLL_DCD_CORRECT_EN: Determine whether the duty cycle distortion logic in the DLL includes a loop to further correct for DCD. 0 = Loop is not included. 1 = Loop is included.
57	RW	DLL_DCD_ITER_A: Controls the connection of DCD comparator input to null out comparator offset. 0 = B answer. 1 = A answer. The A and B answers must be averaged to determine the DLL_DCD_ADJUST value.
58	RW	DLL_DCD_CAL_ENABLE: DCD calibration enable. 0 = Reset the calibration state machine (clears DLL_DCD_CAL_DONE and DLL_DCD_CAL_ERROR). 1 = Enables calibration (calibration is complete with the assertion of DLL_DCD_CAL_DONE).
59	RW	Reserved.
60	RW	DLL_DCD_POWERDOWN: 0 = Normal operation. 1 = Power down the DCD circuit for power savings.
61	RWX	DLL_DCD_CAL_DONE: When DCD_CAL_ENABLE is set, this bit indicates the calibration is complete and the calibrated value has been loaded into the DLL_DCD_ADJUST field of this register.
62	RWX	DLL_DCD_CAL_ERROR: If this bit is asserted along with DLL_DCD_CAL_DONE, it indicates the calibration failed to find a solution. Either DLL_DCD_ADJUST reached a maximum value of 0xFF or a minimum value of 0x00.
63	RO	DLL_DCD_COMPARE_OUT: (Read only.) Result of the DCD comparator. 0 = Need to increase DLL_DCD_ADJUST. 1 = Need to decrease DLL_DCD_ADJUST.

Register Name	ADR RESERVED 3 Register
Mnemonic	IOM0.DDRPHY_ADR_RESERVED2_P0_ADR32S0
Address	800080390701103F (SCOM)
Description	Currently reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	Reserved.

Register Name	ADR RESERVED 3 Register
Mnemonic	IOM0.DDRPHY_ADR_RESERVED2_P1_ADR32S0
Address	800080390701143F (SCOM)
Description	Currently reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	Reserved.

Register Name	ADR RESERVED 3 Register
Mnemonic	IOM0.DDRPHY_ADR_RESERVED2_P2_ADR32S0
Address	800080390701183F (SCOM)
Description	Currently reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	Reserved.

Register Name	ADR RESERVED 3 Register
Mnemonic	IOM0.DDRPHY_ADR_RESERVED2_P3_ADR32S0
Address	8000803907011C3F (SCOM)
Description	Currently reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	Reserved.

Register Name	ADR DLL Control Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_CNTL_P0_ADR32S0
Address	8000803A0701103F (SCOM)
Description	This register controls the DLL calibration logic. **CAUTION:** This register must not be written while hardware calibration is active. **Note:** When writing the register, software must write bits 61:63 to 0b000 to avoid a parity error.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	INIT_RXDLL_CAL_RESET: 1 = DLL reset; the DLL output clocks are not correct. 0 = Initiate full calibration. Leave this bit at ‘0’ after calibration. **Note:** Power must be on and stable to the analog DLL logic a minimum of 100 ns before deactivating reset.
49	RW	INIT_RXDLL_CAL_UPDATE: When 1, requests DLL calibration to update/adjust fine delays only. VREG and coarse calibration are skipped, although they must have completed successfully before writing this bit to 1. **Note:** This bit starts at 0, but hardware automatically sets it to 1 on the riding edge of "cal_good," which should occur after full calibration. This enables fine calibration to run continuously after full calibration. When software writes this bit to 0, reads of the bit might still show 1 until the current fine calibration sequence finishes. **Note:** Power must be on and stable to the analog DLL logic for a minimum of 100 ns before activating CAL_UPDATE.
50:51	RW	REGS_RXDLL_CAL_SKIP: Skip calibration steps (requires manual presets too). bit 0: When 1, skip VREG calibration. bit 1: When 1, skip coarse delay calibration.

Bits	SCOM	Field Mnemonic: Description
52	RW	REGS_RXDLL_COARSE_ADJ_BY2: At the end of coarse calibration, the DAC code is reduced to set the total delay under one period before entering fine calibration. This bit controls whether the reduction is one or two code increments. When 0, change final coarse delay setting by one. (default). When 1, change final coarse delay setting by two. **Note:** This bit has lower priority than REGS_RXDLL_COARSE_ADJ_BY0 if both are set.
53:55	RW	RXREG_DLL_FILTER_LENGTH_DC: Adjusts the number of lead/lag samples to filter out. A smaller binary code gives a smaller number of samples.
56:58	RW	RXREG_DLL_LEAD_LAG_SEPARATION_DC: Adjusts the number of lead more than lag or lag more than lead to get a + phase adjustment or a - phase adjustment.
59	RW	DLL_EN_DRIVER_INVFB_DC: Enable driver inverter feedback. Controls when cross-coupled inverters are included across DLL output drivers. Adding the inverters can improve driver performance, but might introduce excessive current if the DLL outputs are not close to their final values. The intent is to exclude the cross coupling during initial calibration, but possibly include it when repeating fine calibration only because DLL outputs are close to their optimal values during fine calibration. 0 = Disable use of cross-coupled inverters on DLL output drivers. 1 = Enable use of cross-coupled inverters on DLL output drivers.
60	RO	Reserved.
61	ROX	CAL_GOOD: (Read only.) When 1, calibration finished successfully. When 0, calibration is on-going or resulted in an error if either CAL_ERROR or CAL_ERROR_FINE is set. **Note:** This is the local copy of CAL_GOOD directly from the DLL calibration logic. Thus, it will alternate between 0 and 1 when fine calibration runs continuously.
62	ROX	CAL_ERROR: (Read only.) When 1, VREG or coarse calibration finished with an error.
63	ROX	CAL_ERROR_FINE: (Read only.) When 1, fine calibration finished with an error.

Register Name	**ADR DLL Control Register**
Mnemonic	IOM0.DDRPHY_ADR_DLL_CNTL_P1_ADR32S0
Address	8000803A0701143F (SCOM)
Description	This register controls the DLL calibration logic. **CAUTION:** This register must not be written while hardware calibration is active. **Note:** When writing the register, software must write bits 61:63 to 0b000 to avoid a parity error.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	INIT_RXDLL_CAL_RESET: 1 = DLL reset; the DLL output clocks are not correct. 0 = Initiate full calibration. Leave this bit at ‘0’ after calibration. **Note:** Power must be on and stable to the analog DLL logic a minimum of 100 ns before deactivating reset.
49	RW	INIT_RXDLL_CAL_UPDATE: When 1, requests DLL calibration to update/adjust fine delays only. VREG and coarse calibration are skipped, although they must have completed successfully before writing this bit to 1. **Note:** This bit starts at 0, but hardware automatically sets it to 1 on the riding edge of "cal_good," which should occur after full calibration. This enables fine calibration to run continuously after full calibration. When software writes this bit to 0, reads of the bit might still show 1 until the current fine calibration sequence finishes. **Note:** Power must be on and stable to the analog DLL logic for a minimum of 100 ns before activating CAL_UPDATE.
50:51	RW	REGS_RXDLL_CAL_SKIP: Skip calibration steps (requires manual presets too). bit 0: When 1, skip VREG calibration. bit 1: When 1, skip coarse delay calibration.

Bits	SCOM	Field Mnemonic: Description
52	RW	REGS_RXDLL_COARSE_ADJ_BY2: At the end of coarse calibration, the DAC code is reduced to set the total delay under one period before entering fine calibration. This bit controls whether the reduction is one or two code increments. When 0, change final coarse delay setting by one.(default). When 1, change final coarse delay setting by two. **Note:** This bit has lower priority than REGS_RXDLL_COARSE_ADJ_BY0 if both are set.
53:55	RW	RXREG_DLL_FILTER_LENGTH_DC: Adjusts the number of lead/lag samples to filter out. A smaller binary code gives a smaller number of samples.
56:58	RW	RXREG_DLL_LEAD_LAG_SEPARATION_DC: Adjusts the number of lead more than lag or lag more than lead to get a + phase adjustment or a - phase adjustment.
59	RW	DLL_EN_DRIVER_INVFB_DC: Enable driver inverter feedback. Controls when cross-coupled inverters are included across DLL output drivers. Adding the inverters can improve driver performance, but might introduce excessive current if the DLL outputs are not close to their final values. The intent is to exclude the cross coupling during initial calibration, but possibly include it when repeating fine calibration only because DLL outputs are close to their optimal values during fine calibration. 0 = Disable use of cross-coupled inverters on DLL output drivers. 1 = Enable use of cross-coupled inverters on DLL output drivers.
60	RO	Reserved.
61	ROX	CAL_GOOD: (Read only.)When 1, calibration finished successfully. When 0, calibration is on-going or resulted in an error if either CAL_ERROR or CAL_ERROR_FINE is set. **Note:** This is the local copy of CAL_GOOD directly from the DLL calibration logic. Thus, it will alternate between 0 and 1 when fine calibration runs continuously.
62	ROX	CAL_ERROR: (Read only.)When 1, VREG or coarse calibration finished with an error.
63	ROX	CAL_ERROR_FINE: (Read only.)When 1, fine calibration finished with an error.

Register Name	**ADR DLL Control Register**
Mnemonic	IOM0.DDRPHY_ADR_DLL_CNTL_P2_ADR32S0
Address	8000803A0701183F (SCOM)
Description	This register controls the DLL calibration logic. **CAUTION:** This register must not be written while hardware calibration is active. **Note:** When writing the register, software must write bits 61:63 to 0b000 to avoid a parity error.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	INIT_RXDLL_CAL_RESET: 1 = DLL reset; the DLL output clocks are not correct. 0 = Initiate full calibration. Leave this bit at '0' after calibration. **Note:** Power must be on and stable to the analog DLL logic a minimum of 100 ns before deactivating reset.
49	RW	INIT_RXDLL_CAL_UPDATE: When 1, requests DLL calibration to update/adjust fine delays only. VREG and coarse calibration are skipped, although they must have completed successfully before writing this bit to 1. **Note:** This bit starts at 0, but hardware automatically sets it to 1 on the riding edge of "cal_good," which should occur after full calibration. This enables fine calibration to run continuously after full calibration. When software writes this bit to 0, reads of the bit might still show 1 until the current fine calibration sequence finishes. **Note:** Power must be on and stable to the analog DLL logic for a minimum of 100 ns before activating CAL_UPDATE.
50:51	RW	REGS_RXDLL_CAL_SKIP: Skip calibration steps (requires manual presets too). bit 0: When 1, skip VREG calibration. bit 1: When 1, skip coarse delay calibration.

Bits	SCOM	Field Mnemonic: Description
52	RW	REGS_RXDLL_COARSE_ADJ_BY2: At the end of coarse calibration, the DAC code is reduced to set the total delay under one period before entering fine calibration. This bit controls whether the reduction is one or two code increments. When 0, change final coarse delay setting by one.(default). When 1, change final coarse delay setting by two. **Note:** This bit has lower priority than REGS_RXDLL_COARSE_ADJ_BY0 if both are set.
53:55	RW	RXREG_DLL_FILTER_LENGTH_DC: Adjusts the number of lead/lag samples to filter out. A smaller binary code gives a smaller number of samples.
56:58	RW	RXREG_DLL_LEAD_LAG_SEPARATION_DC: Adjusts the number of lead more than lag or lag more than lead to get a + phase adjustment or a - phase adjustment.
60	RO	Reserved.
60	RW	RXREG_FINECAL_2XILSB_DC: Double the effect that each lower code change has on VREG. This extends the range of fine calibration codes by doubling the current and, thus, the effect that each least significant bit has change on VREG. This in turn doubles the delay of the delay line for each code change. 0 = Use normal LSB current. 1 = Double the LSB current, doubling the effect of each code change.
61	ROX	CAL_GOOD: (Read only.)When 1, calibration finished successfully. When 0, calibration is on-going or resulted in an error if either CAL_ERROR or CAL_ERROR_FINE is set. **Note:** This is the local copy of CAL_GOOD directly from the DLL calibration logic. Thus, it will alternate between 0 and 1 when fine calibration runs continuously.
62	ROX	CAL_ERROR: (Read only.)When 1, VREG or coarse calibration finished with an error.
63	ROX	CAL_ERROR_FINE: (Read only.)When 1, fine calibration finished with an error.

Register Name	ADR DLL Control Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_CNTL_P3_ADR32S0
Address	8000803A07011C3F (SCOM)
Description	This register controls the DLL calibration logic. **CAUTION:** This register must not be written while hardware calibration is active. **Note:** When writing the register, software must write bits 61:63 to 0b000 to avoid a parity error.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	INIT_RXDLL_CAL_RESET: 1 = DLL reset; the DLL output clocks are not correct. 0 = Initiate full calibration. Leave this bit at ‘0’ after calibration. **Note:** Power must be on and stable to the analog DLL logic a minimum of 100 ns before deactivating reset.
49	RW	INIT_RXDLL_CAL_UPDATE: When 1, requests DLL calibration to update/adjust fine delays only. VREG and coarse calibration are skipped, although they must have completed successfully before writing this bit to 1. **Note:** This bit starts at 0, but hardware automatically sets it to 1 on the riding edge of "cal_good," which should occur after full calibration. This enables fine calibration to run continuously after full calibration. When software writes this bit to 0, reads of the bit might still show 1 until the current fine calibration sequence finishes. **Note:** Power must be on and stable to the analog DLL logic for a minimum of 100 ns before activating CAL_UPDATE.
50:51	RW	REGS_RXDLL_CAL_SKIP: Skip calibration steps (requires manual presets too). bit 0: When 1, skip VREG calibration. bit 1: When 1, skip coarse delay calibration.

Bits	SCOM	Field Mnemonic: Description
52	RW	REGS_RXDLL_COARSE_ADJ_BY2: At the end of coarse calibration, the DAC code is reduced to set the total delay under one period before entering fine calibration. This bit controls whether the reduction is one or two code increments. When 0, change final coarse delay setting by one.(default). When 1, change final coarse delay setting by two. **Note:** This bit has lower priority than REGS_RXDLL_COARSE_ADJ_BY0 if both are set.
53:55	RW	RXREG_DLL_FILTER_LENGTH_DC: Adjusts the number of lead/lag samples to filter out. A smaller binary code gives a smaller number of samples.
56:58	RW	RXREG_DLL_LEAD_LAG_SEPARATION_DC: Adjusts the number of lead more than lag or lag more than lead to get a + phase adjustment or a - phase adjustment.
59	RW	DLL_EN_DRIVER_INVFB_DC: Enable driver inverter feedback. Controls when cross-coupled inverters are included across DLL output drivers. Adding the inverters can improve driver performance, but might introduce excessive current if the DLL outputs are not close to their final values. The intent is to exclude the cross coupling during initial calibration, but possibly include it when repeating fine calibration only because DLL outputs are close to their optimal values during fine calibration. 0 = Disable use of cross-coupled inverters on DLL output drivers. 1 = Enable use of cross-coupled inverters on DLL output drivers.
60	RO	Reserved.
61	ROX	CAL_GOOD: (Read only.)When 1, calibration finished successfully. When 0, calibration is on-going or resulted in an error if either CAL_ERROR or CAL_ERROR_FINE is set. **Note:** This is the local copy of CAL_GOOD directly from the DLL calibration logic. Thus, it will alternate between 0 and 1 when fine calibration runs continuously.
62	ROX	CAL_ERROR: (Read only.)When 1, VREG or coarse calibration finished with an error.
63	ROX	CAL_ERROR_FINE: (Read only.)When 1, fine calibration finished with an error.

Register Name	**ADR DLL DAC Lower Register**
Mnemonic	IOM0.DDRPHY_ADR_DLL_DAC_LOWER_P0_ADR32S0
Address	8000803B0701103F (SCOM)
Description	This register holds the lower bound for DLL calibration logic. **CAUTION:** This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:62	RW	REGS_RXDLL_VREG_DAC_LOWER: This field controls the value of VREG during fine calibration. Bits set to 1 are independent of each other; it is the total number of them that matter. For example, these values have the same effect: b100...00, b001...00, b000...10. VREG and delay line element propagation time are inversely proportional because higher values of VREG mean faster delay elements. Therefore, adding more 1s increases VREG and makes faster delay elements. Recommendation: Change bits in a thermometer-code fashion because that is how the digital calibration logic does it.
63	RO	Constant = 0b0

Register Name	**ADR DLL DAC Lower Register**
Mnemonic	IOM0.DDRPHY_ADR_DLL_DAC_LOWER_P1_ADR32S0
Address	8000803B0701143F (SCOM)
Description	This register holds the lower bound for DLL calibration logic. **CAUTION:** This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:62	RW	REGS_RXDLL_VREG_DAC_LOWER: This field controls the value of VREG during fine calibration. Bits set to 1 are independent of each other; it is the total number of them that matter. For example, these values have the same effect: b100...00, b001...00, b000...10. VREG and delay line element propagation time are inversely proportional because higher values of VREG mean faster delay elements. Therefore, adding more 1s increases VREG and makes faster delay elements. Recommendation: Change bits in a thermometer-code fashion because that is how the digital calibration logic does it.
63	RO	Constant = 0b0

Register Name	**ADR DLL DAC Lower Register**
Mnemonic	IOM0.DDRPHY_ADR_DLL_DAC_LOWER_P2_ADR32S0
Address	8000803B0701183F (SCOM)
Description	This register holds the lower bound for DLL calibration logic. **CAUTION:** This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:62	RW	REGS_RXDLL_VREG_DAC_LOWER: This field controls the value of VREG during fine calibration. Bits set to 1 are independent of each other; it is the total number of them that matter. For example, these values have the same effect: b100...00, b001...00, b000...10. VREG and delay line element propagation time are inversely proportional because higher values of VREG mean faster delay elements. Therefore, adding more 1s increases VREG and makes faster delay elements. Recommendation: Change bits in a thermometer-code fashion because that is how the digital calibration logic does it.
63	RO	Constant = 0b0

Register Name	**ADR DLL DAC Lower Register**
Mnemonic	IOM0.DDRPHY_ADR_DLL_DAC_LOWER_P3_ADR32S0
Address	8000803B07011C3F (SCOM)
Description	This register holds the lower bound for DLL calibration logic. **CAUTION:** This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:62	RW	REGS_RXDLL_VREG_DAC_LOWER: This field controls the value of VREG during fine calibration. Bits set to 1 are independent of each other; it is the total number of them that matter. For example, these values have the same effect: b100...00, b001...00, b000...10. VREG and delay line element propagation time are inversely proportional because higher values of VREG mean faster delay elements. Therefore, adding more 1s increases VREG and makes faster delay elements. Recommendation: Change bits in a thermometer-code fashion because that is how the digital calibration logic does it.
63	RO	Constant = 0b0

Register Name	ADR DLL DAC Upper Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_DAC_UPPER_P0_ADR32S0
Address	8000803C0701103F (SCOM)
Description	This register holds the upper bound for DLL calibration logic. **CAUTION:** This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:62	RW	REGS_RXDLL_VREG_DAC_UPPER: Same behavior as REGS_RXDLL_VREG_DAC_LOWER, except the effect on VREG and delay is 16 times larger for each bit.
63	RO	Constant = 0b0

Register Name	ADR DLL DAC Upper Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_DAC_UPPER_P1_ADR32S0
Address	8000803C0701143F (SCOM)
Description	This register holds the upper bound for DLL calibration logic. **CAUTION:** This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:62	RW	REGS_RXDLL_VREG_DAC_UPPER: Same behavior as REGS_RXDLL_VREG_DAC_LOWER, except the effect on VREG and delay is 16 times larger for each bit.
63	RO	Constant = 0b0

Register Name	ADR DLL DAC Upper Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_DAC_UPPER_P2_ADR32S0
Address	8000803C0701183F (SCOM)
Description	This register holds the upper bound for DLL calibration logic. **CAUTION:** This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:62	RW	REGS_RXDLL_VREG_DAC_UPPER: Same behavior as REGS_RXDLL_VREG_DAC_LOWER, except the effect on VREG and delay is 16 times larger for each bit.
63	RO	Constant = 0b0

Register Name	ADR DLL DAC Upper Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_DAC_UPPER_P3_ADR32S0
Address	8000803C07011C3F (SCOM)
Description	This register holds the upper bound for DLL calibration logic. **CAUTION:** This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:62	RW	REGS_RXDLL_VREG_DAC_UPPER: Same behavior as REGS_RXDLL_VREG_DAC_LOWER, except the effect on VREG and delay is 16 times larger for each bit.
63	RO	Constant = 0b0

Register Name	ADR DLL VREG Control Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_VREG_CONTROL_P0_ADR32S0
Address	8000803D0701103F (SCOM)
Description	This register controls the voltage regulator of the DLL calibration logic. **CAUTION:** This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:50	RW	RXREG_VREG_COMPCON_DC: This bit affects the compensation capacitor for the regulator. Contact your IBM representative for details.
51	RW	Reserved.
52	RW	RXREG_VREG_DAC_PULLUP_DC: This bit is a mode switch for the regulator. It is normally not changed.
53:55	RW	RXREG_VREG_DRVCON_DC: This field determines the positive field-effect transistor (PFET) size for the regulator. It is a mode switch that is normally not changed.
56:58	RW	RXREG_VREG_REF_SEL_DC: This field adjusts the target value of VREG for VREG calibration. The lowest value (0b000) corresponds to the highest VREG target. The highest value (0b111) corresponds to the lowest VREG target. The recommended value is 0b011.
59	RW	REGS_RXDLL_COARSE_ADJ_BY0: Typically, the transition from coarse to fine calibration decrements the code by 1. Therefore, fine calibration always tries to increase the delay by lowering VREG. Sometimes, however, the typical calibration routine produces a less ideal setting. When set, this bit does not decrement the code. Therefore, fine calibration tries to decrease the delay by increasing VREG. 0 = This bit has no effect. 1 = Do not decrement the coarse code during the transition from coarse to fine calibration. **Note:** This bit takes priority over REGS_RXDLL_COARSE_ADJ_BY2 if both are set. Contact your IBM representative for details.
60:62	RO	Constant = 0b000
63	RW	DLL_CAL_CKTS_ACTIVE: This bit is a mode switch to force DLL calibration analog circuits to always be powered on. 0 = After VREG calibration, some analog circuits are powered down. 1 = Override automatic power down, keeping analog calibration circuits active.

Register Name	ADR DLL VREG Control Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_VREG_CONTROL_P1_ADR32S0
Address	8000803D0701143F (SCOM)
Description	This register controls the voltage regulator of the DLL calibration logic. **CAUTION:** This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RW	RXREG_VREG_COMPCON_DC: This bit affects the compensation capacitor for the regulator. Contact your IBM representative for details.
51	RW	Reserved.
52	RW	RXREG_VREG_DAC_PULLUP_DC: This bit is a mode switch for the regulator. It is normally not changed.
53:55	RW	RXREG_VREG_DRVCON_DC: This field determines the PFET size for the regulator. It is a mode switch that is normally not changed.
56:58	RW	RXREG_VREG_REF_SEL_DC: This field adjusts the target value of VREG for VREG calibration. The lowest value (0b000) corresponds to the highest VREG target. The highest value (0b111) corresponds to the lowest VREG target. The recommended value is 0b011.
59	RW	REGS_RXDLL_COARSE_ADJ_BY0: Typically, the transition from coarse to fine calibration decrements the code by 1. Therefore, fine calibration always tries to increase the delay by lowering VREG. Sometimes, however, the typical calibration routine produces a less ideal setting. When set, this bit does not decrement the code. Therefore, fine calibration tries to decrease the delay by increasing VREG. 0 = This bit has no effect. 1 = Do not decrement the coarse code during the transition from coarse to fine calibration. **Note:** This bit takes priority over REGS_RXDLL_COARSE_ADJ_BY2 if both are set. Contact your IBM representative for details.
60:62	RO	Constant = 0b000
63	RW	DLL_CAL_CKTS_ACTIVE: This bit is a mode switch to force DLL calibration analog circuits to always be powered on. 0 = After VREG calibration, some analog circuits are powered down. 1 = Override automatic power down, keeping analog calibration circuits active.

Register Name	ADR DLL VREG Control Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_VREG_CONTROL_P2_ADR32S0
Address	8000803D0701183F (SCOM)
Description	This register controls the voltage regulator of the DLL calibration logic. **CAUTION:** This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48:50	RW	RXREG_VREG_COMPCON_DC: This bit affects the compensation capacitor for the regulator. Contact your IBM representative for details.
51	RW	Reserved.
52	RW	RXREG_VREG_DAC_PULLUP_DC: This bit is a mode switch for the regulator. It is normally not changed.
53:55	RW	RXREG_VREG_DRVCON_DC: This field determines the PFET size for the regulator. It is a mode switch that is normally not changed.
56:58	RW	RXREG_VREG_REF_SEL_DC: This field adjusts the target value of VREG for VREG calibration. The lowest value (0b000) corresponds to the highest VREG target. The highest value (0b111) corresponds to the lowest VREG target. The recommended value is 0b011.
59	RW	REGS_RXDLL_COARSE_ADJ_BY0: Typically, the transition from coarse to fine calibration decrements the code by 1. Therefore, fine calibration always tries to increase the delay by lowering VREG. Sometimes, however, the typical calibration routine produces a less ideal setting. When set, this bit does not decrement the code. Therefore, fine calibration tries to decrease the delay by increasing VREG. 0 = This bit has no effect. 1 = Do not decrement the coarse code during the transition from coarse to fine calibration. **Note:** This bit takes priority over REGS_RXDLL_COARSE_ADJ_BY2 if both are set. Contact your IBM representative for details.

Bits	SCOM	Field Mnemonic: Description
60:62	RO	Constant = 0b000
63	RW	DLL_CAL_CKTS_ACTIVE: This bit is a mode switch to force DLL calibration analog circuits to always be powered on. 0 = After VREG calibration, some analog circuits are powered down. 1 = Override automatic power down, keeping analog calibration circuits active.

Register Name	ADR DLL VREG Control Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_VREG_CONTROL_P3_ADR32S0
Address	8000803D07011C3F (SCOM)
Description	This register controls the voltage regulator of the DLL calibration logic. **CAUTION:** This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	RXREG_VREG_COMPCON_DC: This bit affects the compensation capacitor for the regulator. Contact your IBM representative for details.
51	RW	Reserved.
52	RW	RXREG_VREG_DAC_PULLUP_DC: This bit is a mode switch for the regulator. It is normally not changed.
53:55	RW	RXREG_VREG_DRVCON_DC: This field determines the PFET size for the regulator. It is a mode switch that is normally not changed.
56:58	RW	RXREG_VREG_REF_SEL_DC: This field adjusts the target value of VREG for VREG calibration. The lowest value (0b000) corresponds to the highest VREG target. The highest value (0b111) corresponds to the lowest VREG target. The recommended value is 0b011.
59	RW	REGS_RXDLL_COARSE_ADJ_BY0: Typically, the transition from coarse to fine calibration decrements the code by 1. Therefore, fine calibration always tries to increase the delay by lowering VREG. Sometimes, however, the typical calibration routine produces a less ideal setting. When set, this bit does not decrement the code. Therefore, fine calibration tries to decrease the delay by increasing VREG. 0 = This bit has no effect. 1 = Do not decrement the coarse code during the transition from coarse to fine calibration. **Note:** This bit takes priority over REGS_RXDLL_COARSE_ADJ_BY2 if both are set. Contact your IBM representative for details.
60:62	RO	Constant = 0b000
63	RW	DLL_CAL_CKTS_ACTIVE: This bit is a mode switch to force DLL calibration analog circuits to always be powered on. 0 = After VREG calibration, some analog circuits are powered down. 1 = Override automatic power down, keeping analog calibration circuits active.

Register Name	ADR DLL VREG Coarse Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_VREG_COARSE_P0_ADR32S0
Address	8000803E0701103F (SCOM)
Description	This register controls the coarse calibration of DLL calibration logic. **CAUTION:** This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RW	REGS_RXDLL_COARSE_EN: This field adjusts the delay of each element in the delay line. The larger the code, the larger the delay. Usually, software reads this register at the end of coarse calibration to see where the setting ended up. However, under special situations (that is, lab testing), it can be written to force a specific delay. **Note:** The POWER9 version of analog DLL only uses 5 bits (0:4). Thus, only the lowest 5 bits of this register (1:5) are connected. Bit 0 exists in the digital logic, but is left unconnected at the digital/analog boundary.
54:55	RO	Constant = 0b00
56:62	RW	REGS_RXDLL_VREG_DAC_COARSE: This field adjusts the value of VREG during VREG calibration. The smallest code (0b0000000) produces the highest VREG voltage; the largest code (0b1111111) produces the lowest VREG voltage. Usually, software reads this register at the end of VREG calibration to see where the setting ended up. However, under special situations (that is, lab testing), it can be written to force a VREG value.
63	RO	Constant = 0b0

Register Name	ADR DLL VREG Coarse Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_VREG_COARSE_P1_ADR32S0
Address	8000803E0701143F (SCOM)
Description	This register controls the coarse calibration of DLL calibration logic. **CAUTION:** This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:53	RW	REGS_RXDLL_COARSE_EN: This field adjusts the delay of each element in the delay line. The larger the code, the larger the delay. Usually, software reads this register at the end of coarse calibration to see where the setting ended up. However, under special situations (that is, lab testing), it can be written to force a specific delay. **Note:** The POWER9 version of analog DLL only uses 5 bits (0:4). Thus, only the lowest 5 bits of this register (1:5) are connected. Bit 0 exists in the digital logic, but is left unconnected at the digital/analog boundary.
54:55	RO	Constant = 0b00
56:62	RW	REGS_RXDLL_VREG_DAC_COARSE: This field adjusts the value of VREG during VREG calibration. The smallest code (0b0000000) produces the highest VREG voltage; the largest code (0b1111111) produces the lowest VREG voltage. Usually, software reads this register at the end of VREG calibration to see where the setting ended up. However, under special situations (that is, lab testing), it can be written to force a VREG value.
63	RO	Constant = 0b0

Register Name	ADR DLL VREG Coarse Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_VREG_COARSE_P2_ADR32S0
Address	8000803E0701183F (SCOM)
Description	This register controls the coarse calibration of DLL calibration logic. **CAUTION:** This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RW	REGS_RXDLL_COARSE_EN: This field adjusts the delay of each element in the delay line. The larger the code, the larger the delay. Usually, software reads this register at the end of coarse calibration to see where the setting ended up. However, under special situations (that is, lab testing), it can be written to force a specific delay. **Note:** The POWER9 version of analog DLL only uses 5 bits (0:4). Thus, only the lowest 5 bits of this register (1:5) are connected. Bit 0 exists in the digital logic, but is left unconnected at the digital/analog boundary.
54:55	RO	Constant = 0b00
56:62	RW	REGS_RXDLL_VREG_DAC_COARSE: This field adjusts the value of VREG during VREG calibration. The smallest code (0b0000000) produces the highest VREG voltage; the largest code (0b1111111) produces the lowest VREG voltage. Usually, software reads this register at the end of VREG calibration to see where the setting ended up. However, under special situations (that is, lab testing), it can be written to force a VREG value.
63	RO	Constant = 0b0

Register Name	ADR DLL VREG Coarse Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_VREG_COARSE_P3_ADR32S0
Address	8000803E07011C3F (SCOM)
Description	This register controls the coarse calibration of DLL calibration logic. **CAUTION:** This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:53	RW	REGS_RXDLL_COARSE_EN: This field adjusts the delay of each element in the delay line. The larger the code, the larger the delay. Usually, software reads this register at the end of coarse calibration to see where the setting ended up. However, under special situations (that is, lab testing), it can be written to force a specific delay. **Note:** The POWER9 version of analog DLL only uses 5 bits (0:4). Thus, only the lowest 5 bits of this register (1:5) are connected. Bit 0 exists in the digital logic, but is left unconnected at the digital/analog boundary.
54:55	RO	Constant = 0b00
56:62	RW	REGS_RXDLL_VREG_DAC_COARSE: This field adjusts the value of VREG during VREG calibration. The smallest code (0b0000000) produces the highest VREG voltage; the largest code (0b1111111) produces the lowest VREG voltage. Usually, software reads this register at the end of VREG calibration to see where the setting ended up. However, under special situations (that is, lab testing), it can be written to force a VREG value.
63	RO	Constant = 0b0

Register Name	ADR DLL Software Control 1 Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_SW_CONTROL_1_P0_ADR32S1
Address	8000842D0701103F (SCOM)
Description	This register enables software to take control of the slave regulators' VREG controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RW	SLAVE_VREG_OVERRIDE: When 0, the master regulator controls for REF_SEL and NVT/PVT (derived from VREG_DAC_COARSE) are sent to the slave regulators. This enables the slave to track the master's settings during VREG calibration. When 1, this register takes control over the slave regulator REF_SEL and NVT/PVT (via VREG_DAC_COARSE) inputs. This enables software to manage the master and slave regulators completely independently.
49:51	RW	SLAVE_VREG_REF_SEL_DC: When SLAVE_VREG_OVERRIDE = 0, this field is not used. The master and slave share the master's VREG_REF_SEL_DC(0:2) setting. When SLAVE_VREG_OVERRIDE = 1, this field is sent to the slave regulators as VREG_REF_SEL_DC(0:2).
52:58	RW	SLAVE_VREG_DAC_COARSE: When SLAVE_VREG_OVERRIDE = 0, this field is not used. The master and slave share the master's VREG_DAC_COARSE(0:6) setting. When SLAVE_VREG_OVERRIDE = 1, this field is sent to the slave regulators as VREG_DAC_COARSE(0:6), which is converted to NVT(0:3) and PVT(0:3) by the DLL logic.
59:62	RO	Reserved.
63	RW	DD2_ADR_IE_FIX_DISABLE: 0 = Enable the DD2 function for ADR IE assertion when FORCE_MCLK_LOW is asserted. 1 = Enable the DD1 function.

Register Name	ADR DLL Software Control 1 Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_SW_CONTROL_1_P1_ADR32S1
Address	8000842D0701143F (SCOM)
Description	This register enables software to take control of the slave regulators' VREG controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	RW	SLAVE_VREG_OVERRIDE: When 0, the master regulator controls for REF_SEL and NVT/PVT (derived from VREG_DAC_COARSE) are sent to the slave regulators. This enables the slave to track the master's settings during VREG calibration. When 1, this register takes control over the slave regulator REF_SEL and NVT/PVT (via VREG_DAC_COARSE) inputs. This enables software to manage the master and slave regulators completely independently.
49:51	RW	SLAVE_VREG_REF_SEL_DC: When SLAVE_VREG_OVERRIDE = 0, this field is not used. The master and slave share the master's VREG_REF_SEL_DC(0:2) setting. When SLAVE_VREG_OVERRIDE = 1, this field is sent to the slave regulators as VREG_REF_SEL_DC(0:2).
52:58	RW	SLAVE_VREG_DAC_COARSE: When SLAVE_VREG_OVERRIDE = 0, this field is not used. The master and slave share the master's VREG_DAC_COARSE(0:6) setting. When SLAVE_VREG_OVERRIDE = 1, this field is sent to the slave regulators as VREG_DAC_COARSE(0:6), which is converted to NVT(0:3) and PVT(0:3) by the DLL logic.
59:62	RO	Reserved.
63	RW	DD2_ADR_IE_FIX_DISABLE: 0 = Enable the DD2 function for ADR IE assertion when FORCE_MCLK_LOW is asserted. 1 = Enable the DD1 function.

Register Name	ADR DLL Software Control 1 Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_SW_CONTROL_1_P2_ADR32S1
Address	8000842D0701183F (SCOM)
Description	This register enables software to take control of the slave regulators' VREG controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	SLAVE_VREG_OVERRIDE: When 0, the master regulator controls for REF_SEL and NVT/PVT (derived from VREG_DAC_COARSE) are sent to the slave regulators. This enables the slave to track the master's settings during VREG calibration. When 1, this register takes control over the slave regulator REF_SEL and NVT/PVT (via VREG_DAC_COARSE) inputs. This enables software to manage the master and slave regulators completely independently.
49:51	RW	SLAVE_VREG_REF_SEL_DC: When SLAVE_VREG_OVERRIDE = 0, this field is not used. The master and slave share the master's VREG_REF_SEL_DC(0:2) setting. When SLAVE_VREG_OVERRIDE = 1, this field is sent to the slave regulators as VREG_REF_SEL_DC(0:2).
52:58	RW	SLAVE_VREG_DAC_COARSE: When SLAVE_VREG_OVERRIDE = 0, this field is not used. The master and slave share the master's VREG_DAC_COARSE(0:6) setting. When SLAVE_VREG_OVERRIDE = 1, this field is sent to the slave regulators as VREG_DAC_COARSE(0:6), which is converted to NVT(0:3) and PVT(0:3) by the DLL logic.
59:62	RO	Reserved.
63	RW	DD2_ADR_IE_FIX_DISABLE: 0 = Enable the DD2 function for ADR IE assertion when FORCE_MCLK_LOW is asserted. 1 = Enable the DD1 function.

Register Name	**ADR DLL Software Control 1 Register**
Mnemonic	IOM0.DDRPHY_ADR_DLL_SW_CONTROL_1_P3_ADR32S1
Address	8000842D07011C3F (SCOM)
Description	This register enables software to take control of the slave regulators' VREG controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	SLAVE_VREG_OVERRIDE: When 0, the master regulator controls for REF_SEL and NVT/PVT (derived from VREG_DAC_COARSE) are sent to the slave regulators. This enables the slave to track the master's settings during VREG calibration. When 1, this register takes control over the slave regulator REF_SEL and NVT/PVT (via VREG_DAC_COARSE) inputs. This enables software to manage the master and slave regulators completely independently.
49:51	RW	SLAVE_VREG_REF_SEL_DC: When SLAVE_VREG_OVERRIDE = 0, this field is not used. The master and slave share the master's VREG_REF_SEL_DC(0:2) setting. When SLAVE_VREG_OVERRIDE = 1, this field is sent to the slave regulators as VREG_REF_SEL_DC(0:2).
52:58	RW	SLAVE_VREG_DAC_COARSE: When SLAVE_VREG_OVERRIDE = 0, this field is not used. The master and slave share the master's VREG_DAC_COARSE(0:6) setting. When SLAVE_VREG_OVERRIDE = 1, this field is sent to the slave regulators as VREG_DAC_COARSE(0:6), which is converted to NVT(0:3) and PVT(0:3) by the DLL logic.
59:62	RO	Reserved.
63	RW	DD2_ADR_IE_FIX_DISABLE: 0 = Enable the DD2 function for ADR IE assertion when FORCE_MCLK_LOW is asserted. 1 = Enable the DD1 function.

Register Name	ADR DLL Slave VREG Lower Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_SLAVE_VREG_LOWER_P0_ADR32S1
Address	8000842E0701103F (SCOM)
Description	This register holds the "lower" control for the slave voltage regulators.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:62	RW	SLAVE_VREG_LOWER: This field controls the value of the slave regulators' VREG. Bits set to 1 are independent of each other; it is the total number of them that matters. For example, these settings have the same effect: b100...00, b001...00, b000...10). Adding more 1s increases the VREG. Recommendation: Change the bits in thermometer-code fashion.
63	RO	Constant = 0b0

Register Name	ADR DLL Slave VREG Lower Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_SLAVE_VREG_LOWER_P1_ADR32S1
Address	8000842E0701143F (SCOM)
Description	This register holds the "lower" control for the slave voltage regulators.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:62	RW	SLAVE_VREG_LOWER: This field controls the value of the slave regulators' VREG. Bits set to 1 are independent of each other; it is the total number of them that matters. For example, these settings have the same effect: b100...00, b001...00, b000...10). Adding more 1s increases the VREG. Recommendation: Change the bits in thermometer-code fashion.
63	RO	Constant = 0b0

Register Name	ADR DLL Slave VREG Lower Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_SLAVE_VREG_LOWER_P2_ADR32S1
Address	8000842E0701183F (SCOM)
Description	This register holds the "lower" control for the slave voltage regulators.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:62	RW	SLAVE_VREG_LOWER: This field controls the value of the slave regulators' VREG. Bits set to 1 are independent of each other; it is the total number of them that matters. For example, these settings have the same effect: b100...00, b001...00, b000...10). Adding more 1s increases the VREG. Recommendation: Change the bits in thermometer-code fashion.
63	RO	Constant = 0b0

Register Name	ADR DLL Slave VREG Lower Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_SLAVE_VREG_LOWER_P3_ADR32S1
Address	8000842E07011C3F (SCOM)
Description	This register holds the "lower" control for the slave voltage regulators.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:62	RW	SLAVE_VREG_LOWER: This field controls the value of the slave regulators' VREG. Bits set to 1 are independent of each other; it is the total number of them that matters. For example, these settings have the same effect: b100...00, b001...00, b000...10). Adding more 1s increases the VREG. Recommendation: Change the bits in thermometer-code fashion.
63	RO	Constant = 0b0

Register Name	ADR DLL Slave VREG Upper Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_SLAVE_VREG_UPPER_P0_ADR32S1
Address	8000842F0701103F (SCOM)
Description	This register holds the "upper" control for the slave voltage regulators.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:62	RW	SLAVE_VREG_UPPER: Same behavior as SLAVE_VREG_LOWER, except the effect on VREG is 16 times larger for each bit.
63	RO	Constant = 0b0

Register Name	ADR DLL Slave VREG Upper Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_SLAVE_VREG_UPPER_P1_ADR32S1
Address	8000842F0701143F (SCOM)
Description	This register holds the "upper" control for the slave voltage regulators.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:62	RW	SLAVE_VREG_UPPER: Same behavior as SLAVE_VREG_LOWER, except the effect on VREG is 16 times larger for each bit.
63	RO	Constant = 0b0

Register Name	ADR DLL Slave VREG Upper Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_SLAVE_VREG_UPPER_P2_ADR32S1
Address	8000842F0701183F (SCOM)
Description	This register holds the "upper" control for the slave voltage regulators.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:62	RW	SLAVE_VREG_UPPER: Same behavior as SLAVE_VREG_LOWER, except the effect on VREG is 16 times larger for each bit.
63	RO	Constant = 0b0

Register Name	ADR DLL Slave VREG Upper Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_SLAVE_VREG_UPPER_P3_ADR32S1
Address	8000842F07011C3F (SCOM)
Description	This register holds the "upper" control for the slave voltage regulators.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:62	RW	SLAVE_VREG_UPPER: Same behavior as SLAVE_VREG_LOWER, except the effect on VREG is 16 times larger for each bit.
63	RO	Constant = 0b0

Register Name	ADR DLL Software Control 0 Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_SW_CONTROL_0_P0_ADR32S1
Address	800084300701103F (SCOM)
Description	This register exposes internal delay locked loop (DLL) signals to software to enable it to override the hardware DLL calibration algorithm. META indicates that the signals have safely crossed into the grid clock domain so they should not exhibit metastability. Non-META signals can be read after they stabilize.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	DLL_SW_OVERRIDE: When 0, the hardware DLL algorithm is used. When 1, this register takes control over the DLL analog inputs and outputs allowing firmware to perform calibration.
49	RW	DLL_SW_CAL_PD_ENABLE: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_CAL_PD_ENABLE_SLOW.
50	RW	DLL_SW_MAIN_PD_ENABLE: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_MAIN_PD_ENABLE_SLOW.
51	RW	DLL_SW_DETECT_REQ: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_DETECT_REQ_SLOW.
52	RW	SLAVE_CAL_CKT_POWERDOWN: Control the CAL_CIRCUIT_POWERDOWN input to the slave regulators. When 1, regulators are powered down. When 0, regulators are powered up.
53:55	RO	Constant = 0b000
56	ROX	VREG_RXCAL_COMP_OUT_META: (Read only.)The result of the master VREG comparator, used during VREG calibration. 1 = VREG is less than the reference set by REF_SEL(0:2). 0 = VREG is greater than the reference set by REF_SEL(0:2).
57	ROX	RXCAL_DETECT_DONE_META: (Read only.) Used during coarse and fine calibration. When 0, it means that the analog lead/lag comparator values are still being determined. When 1, it means that the analog lead/lag comparator values are valid and ready to read.
58	ROX	RXCAL_PD_CAL_LAG_META: (Read only.) Used during coarse and fine calibration. 1 = Grid clock and 67.5 degree delay line output clock are in a lag relationship. 0 = Indeterminate. Either the CAL PD filter/phase detector needs more time to evaluate, or the clocks are in a lead relationship.

Bits	SCOM	Field Mnemonic: Description
59	ROX	RXCAL_PD_MAIN_LEAD_META: (Read only.) Used during coarse and fine calibration. 1 = Grid clock and 360 degree delay line output clock are in a lead relationship. 0 = Indeterminate. Either the main PD filter/phase detector needs more time to evaluate, or clocks are in a lag relationship.
60	ROX	RXCAL_PD_MAIN_LAG_META: (Read only.) Used during coarse and fine calibration. 1 = Grid clock and 360 degree delay line output clock are in a lag relationship. 0 = Indeterminate. Either the main PD filter/phase detector needs more time to evaluate, or clocks are in a lead relationship.
61	ROX	VREG_SLAVE1_COMP_OUT: (Read only.) Result of the slave 1 VREG comparator. 1 = VREG is less than the reference set by REF_SEL(0:2). 0 = VREG is greater than the reference set by REF_SEL(0:2). It is safe to read 256 grid clock cycles after REF_SEL is changed.
62	ROX	VREG_SLAVE2_COMP_OUT: (Read only.) Result of the slave 2 VREG comparator. 1 = VREG is less than the reference set by REF_SEL(0:2). 0 = VREG is greater than the reference set by REF_SEL(0:2). It is safe to read 256 grid clock cycles after REF_SEL is changed.
63	RO	Reserved.

Register Name	**ADR DLL Software Control 0 Register**
Mnemonic	IOM0.DDRPHY_ADR_DLL_SW_CONTROL_0_P1_ADR32S1
Address	800084300701143F (SCOM)
Description	This register exposes internal delay locked loop (DLL) signals to software to enable it to override the hardware DLL calibration algorithm. META indicates that the signals have safely crossed into the grid clock domain so they should not exhibit metastability. Non-META signals can be read after they stabilize.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	DLL_SW_OVERRIDE: When 0, the hardware DLL algorithm is used. When 1, this register takes control over the DLL analog inputs and outputs allowing firmware to perform calibration.
49	RW	DLL_SW_CAL_PD_ENABLE: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_CAL_PD_ENABLE_SLOW.
50	RW	DLL_SW_MAIN_PD_ENABLE: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_MAIN_PD_ENABLE_SLOW.
51	RW	DLL_SW_DETECT_REQ: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_DETECT_REQ_SLOW.
52	RW	SLAVE_CAL_CKT_POWERDOWN: Control the CAL_CIRCUIT_POWERDOWN input to the slave regulators. When 1, regulators are powered down. When 0, regulators are powered up.
53:55	RO	Constant = 0b000
56	ROX	VREG_RXCAL_COMP_OUT_META: (Read only.)The result of the master VREG comparator, used during VREG calibration. 1 = VREG is less than the reference set by REF_SEL(0:2). 0 = VREG is greater than the reference set by REF_SEL(0:2).
57	ROX	RXCAL_DETECT_DONE_META: (Read only.) Used during coarse and fine calibration. When 0, it means that the analog lead/lag comparator values are still being determined. When 1, it means that the analog lead/lag comparator values are valid and ready to read.

Bits	SCOM	Field Mnemonic: Description
58	ROX	RXCAL_PD_CAL_LAG_META: (Read only.) Used during coarse and fine calibration. 1 = Grid clock and 67.5 degree delay line output clock are in a lag relationship. 0 = Indeterminate. Either the CAL PD filter/phase detector needs more time to evaluate, or the clocks are in a lead relationship.
59	ROX	RXCAL_PD_MAIN_LEAD_META: (Read only.) Used during coarse and fine calibration. 1 = Grid clock and 360 degree delay line output clock are in a lead relationship. 0 = Indeterminate. Either the main PD filter/phase detector needs more time to evaluate, or clocks are in a lag relationship.
60	ROX	RXCAL_PD_MAIN_LAG_META: (Read only.) Used during coarse and fine calibration. 1 = Grid clock and 360 degree delay line output clock are in a lag relationship. 0 = Indeterminate. Either the main PD filter/phase detector needs more time to evaluate, or clocks are in a lead relationship.
61	ROX	VREG_SLAVE1_COMP_OUT: (Read only.) Result of the slave 1 VREG comparator. 1 = VREG is less than the reference set by REF_SEL(0:2). 0 = VREG is greater than the reference set by REF_SEL(0:2). It is safe to read 256 grid clock cycles after REF_SEL is changed.
62	ROX	VREG_SLAVE2_COMP_OUT: (Read only.) Result of the slave 2 VREG comparator. 1 = VREG is less than the reference set by REF_SEL(0:2). 0 = VREG is greater than the reference set by REF_SEL(0:2). It is safe to read 256 grid clock cycles after REF_SEL is changed.
63	RO	Reserved.

Register Name	**ADR DLL Software Control 0 Register**
Mnemonic	IOM0.DDRPHY_ADR_DLL_SW_CONTROL_0_P2_ADR32S1
Address	800084300701183F (SCOM)
Description	This register exposes internal delay locked loop (DLL) signals to software to enable it to override the hardware DLL calibration algorithm. META indicates that the signals have safely crossed into the grid clock domain so they should not exhibit metastability. Non-META signals can be read after they stabilize.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	RW	DLL_SW_OVERRIDE: When 0, the hardware DLL algorithm is used. When 1, this register takes control over the DLL analog inputs and outputs allowing firmware to perform calibration.
49	RW	DLL_SW_CAL_PD_ENABLE: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_CAL_PD_ENABLE_SLOW.
50	RW	DLL_SW_MAIN_PD_ENABLE: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_MAIN_PD_ENABLE_SLOW.
51	RW	DLL_SW_DETECT_REQ: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_DETECT_REQ_SLOW.
52	RW	SLAVE_CAL_CKT_POWERDOWN: Control the CAL_CIRCUIT_POWERDOWN input to the slave regulators. When 1, regulators are powered down. When 0, regulators are powered up.
53:55	RO	Constant = 0b000
56	ROX	VREG_RXCAL_COMP_OUT_META: (Read only.)The result of the master VREG comparator, used during VREG calibration. 1 = VREG is less than the reference set by REF_SEL(0:2). 0 = VREG is greater than the reference set by REF_SEL(0:2).

Bits	SCOM	Field Mnemonic: Description
57	ROX	RXCAL_DETECT_DONE_META: (Read only.) Used during coarse and fine calibration. When 0, it means that the analog lead/lag comparator values are still being determined. When 1, it means that the analog lead/lag comparator values are valid and ready to read.
58	ROX	RXCAL_PD_CAL_LAG_META: (Read only.) Used during coarse and fine calibration. 1 = Grid clock and 67.5 degree delay line output clock are in a lag relationship. 0 = Indeterminate. Either the CAL PD filter/phase detector needs more time to evaluate, or the clocks are in a lead relationship.
59	ROX	RXCAL_PD_MAIN_LEAD_META: (Read only.) Used during coarse and fine calibration. 1 = Grid clock and 360 degree delay line output clock are in a lead relationship. 0 = Indeterminate. Either the main PD filter/phase detector needs more time to evaluate, or clocks are in a lag relationship.
60	ROX	RXCAL_PD_MAIN_LAG_META: (Read only.) Used during coarse and fine calibration. 1 = Grid clock and 360 degree delay line output clock are in a lag relationship. 0 = Indeterminate. Either the main PD filter/phase detector needs more time to evaluate, or clocks are in a lead relationship.
61	ROX	VREG_SLAVE1_COMP_OUT: (Read only.) Result of the slave 1 VREG comparator. 1 = VREG is less than the reference set by REF_SEL(0:2). 0 = VREG is greater than the reference set by REF_SEL(0:2). It is safe to read 256 grid clock cycles after REF_SEL is changed.
62	ROX	VREG_SLAVE2_COMP_OUT: (Read only.) Result of the slave 2 VREG comparator. 1 = VREG is less than the reference set by REF_SEL(0:2). 0 = VREG is greater than the reference set by REF_SEL(0:2). It is safe to read 256 grid clock cycles after REF_SEL is changed.
63	RO	Reserved.

Register Name	**ADR DLL Software Control 0 Register**
Mnemonic	IOM0.DDRPHY_ADR_DLL_SW_CONTROL_0_P3_ADR32S1
Address	8000843007011C3F (SCOM)
Description	This register exposes internal delay locked loop (DLL) signals to software to enable it to override the hardware DLL calibration algorithm. META indicates that the signals have safely crossed into the grid clock domain so they should not exhibit metastability. Non-META signals can be read after they stabilize.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	RW	DLL_SW_OVERRIDE: When 0, the hardware DLL algorithm is used. When 1, this register takes control over the DLL analog inputs and outputs allowing firmware to perform calibration.
49	RW	DLL_SW_CAL_PD_ENABLE: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_CAL_PD_ENABLE_SLOW.
50	RW	DLL_SW_MAIN_PD_ENABLE: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_MAIN_PD_ENABLE_SLOW.
51	RW	DLL_SW_DETECT_REQ: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_DETECT_REQ_SLOW.
52	RW	SLAVE_CAL_CKT_POWERDOWN: Control the CAL_CIRCUIT_POWERDOWN input to the slave regulators. When 1, regulators are powered down. When 0, regulators are powered up.
53:55	RO	Constant = 0b000

Bits	SCOM	Field Mnemonic: Description
56	ROX	VREG_RXCAL_COMP_OUT_META: (Read only.)The result of the master VREG comparator, used during VREG calibration. 1 = VREG is less than the reference set by REF_SEL(0:2). 0 = VREG is greater than the reference set by REF_SEL(0:2).
57	ROX	RXCAL_DETECT_DONE_META: (Read only.) Used during coarse and fine calibration. When 0, it means that the analog lead/lag comparator values are still being determined. When 1, it means that the analog lead/lag comparator values are valid and ready to read.
58	ROX	RXCAL_PD_CAL_LAG_META: (Read only.) Used during coarse and fine calibration. 1 = Grid clock and 67.5 degree delay line output clock are in a lag relationship. 0 = Indeterminate. Either the CAL PD filter/phase detector needs more time to evaluate, or the clocks are in a lead relationship.
59	ROX	RXCAL_PD_MAIN_LEAD_META: (Read only.) Used during coarse and fine calibration. 1 = Grid clock and 360 degree delay line output clock are in a lead relationship. 0 = Indeterminate. Either the main PD filter/phase detector needs more time to evaluate, or clocks are in a lag relationship.
60	ROX	RXCAL_PD_MAIN_LAG_META: (Read only.) Used during coarse and fine calibration. 1 = Grid clock and 360 degree delay line output clock are in a lag relationship. 0 = Indeterminate. Either the main PD filter/phase detector needs more time to evaluate, or clocks are in a lead relationship.
61	ROX	VREG_SLAVE1_COMP_OUT: (Read only.) Result of the slave 1 VREG comparator. 1 = VREG is less than the reference set by REF_SEL(0:2). 0 = VREG is greater than the reference set by REF_SEL(0:2). It is safe to read 256 grid clock cycles after REF_SEL is changed.
62	ROX	VREG_SLAVE2_COMP_OUT: (Read only.) Result of the slave 2 VREG comparator. 1 = VREG is less than the reference set by REF_SEL(0:2). 0 = VREG is greater than the reference set by REF_SEL(0:2). It is safe to read 256 grid clock cycles after REF_SEL is changed.
63	RO	Reserved.

Register Name	**ADR DLL/VREG Configuration 1 Register**
Mnemonic	IOM0.DDRPHY_ADR_DLL_VREG_CONFIG_1_P0_ADR32S1
Address	800084310701103F (SCOM)
Description	This is the second of two registers that configure a variety of DLL and VREG programming values.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	HS_DLLMUX_SEL_0_3: Select 1 of 16 DLL phases to send out to the high-speed MUX structure.
52:53	RW	Reserved.
54	RW	Reserved.
55:56	RW	Reserved.
57:58	RW	Reserved.

Bits	SCOM	Field Mnemonic: Description
59:62	RW	STRENGTH: Phase rotator strength bits. Set this field as follows for the given data rate: 0000 = DDR PHY is not operational. 0001 = 1866 MT/s. 0010 = 2133 MT/s. 0100 = 2400 MT/s. 1000 = 2666 MT/s. All other values are reserved.
63	RW	ANALOG_WRAPON: Wrap data control to the attached ADR16s or ADR12s.

Register Name	ADR DLL/VREG Configuration 1 Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_VREG_CONFIG_1_P1_ADR32S1
Address	800084310701143F (SCOM)
Description	This is the second of two registers that configure a variety of DLL and VREG programming values.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	HS_DLLMUX_SEL_0_3: Select 1 of 16 DLL phases to send out to the high-speed MUX structure.
52:53	RW	Reserved.
54	RW	Reserved.
55:56	RW	Reserved.
57:58	RW	Reserved.
59:62	RW	STRENGTH: Phase rotator strength bits. Set this field as follows for the given data rate: 0000 = DDR PHY is not operational. 0001 = 1866 MT/s. 0010 = 2133 MT/s. 0100 = 2400 MT/s. 1000 = 2666 MT/s. All other values are reserved.
63	RW	ANALOG_WRAPON: Wrap data control to the attached ADR16s or ADR12s.

Register Name	ADR DLL/VREG Configuration 1 Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_VREG_CONFIG_1_P2_ADR32S1
Address	800084310701183F (SCOM)
Description	This is the second of two registers that configure a variety of DLL and VREG programming values.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	HS_DLLMUX_SEL_0_3: Select 1 of 16 DLL phases to send out to the high-speed MUX structure.
52:53	RW	Reserved.
54	RW	Reserved.
55:56	RW	Reserved.
57:58	RW	Reserved.

Bits	SCOM	Field Mnemonic: Description
59:62	RW	STRENGTH: Phase rotator strength bits. Set this field as follows for the given data rate: 0000 = DDR PHY is not operational. 0001 = 1866 MT/s. 0010 = 2133 MT/s. 0100 = 2400 MT/s. 1000 = 2666 MT/s. All other values are reserved.
63	RW	ANALOG_WRAPON: Wrap data control to the attached ADR16s or ADR12s.

Register Name	**ADR DLL/VREG Configuration 1 Register**
Mnemonic	IOM0.DDRPHY_ADR_DLL_VREG_CONFIG_1_P3_ADR32S1
Address	8000843107011C3F (SCOM)
Description	This is the second of two registers that configure a variety of DLL and VREG programming values.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	HS_DLLMUX_SEL_0_3: Select 1 of 16 DLL phases to send out to the high-speed MUX structure.
52:53	RW	Reserved.
54	RW	Reserved.
55:56	RW	Reserved.
57:58	RW	Reserved.
59:62	RW	STRENGTH: Phase rotator strength bits. Set this field as follows for the given data rate: 0000 = DDR PHY is not operational. 0001 = 1866 MT/s. 0010 = 2133 MT/s. 0100 = 2400 MT/s. 1000 = 2666 MT/s. All other values are reserved.
63	RW	ANALOG_WRAPON: Wrap data control to the attached ADR16s or ADR12s.

Register Name	**ADR SysClk Phase Rotator Control Register**
Mnemonic	IOM0.DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR32S1
Address	800084320701103F (SCOM)
Description	This register controls the circuit that aligns the internal SysClk to the incoming dphy_gckn clock.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	Reserved.

Bits	SCOM	Field Mnemonic: Description
49:55	RW	SYSCLK_ROT_OVERRIDE: This field has a dual purpose: override control and lock control. When SYSCLK_ROT_OVERRIDE_EN = 1, this field is in override control mode. When SYSCLK_ROT_OVERRIDE_EN = 0, this field is in lock control. For override control: System clock (SysClk) phase-rotator override value. The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by four dphy_gckn clock cycles. Back-to-back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field in the ADR SysClk Phase Rotator Value Register is reserved. For lock control: Write this field to all zeros unless instructed otherwise by your IBM representative. bit 2: Lock select. Selects between lock status and sticky lock. 0 = Selects the current status of the lock. When the dphy_gckn detect has reached alignment between the dphy_gckn and SysClk, the BB_LOCK field in the ADR SysClk Phase Rotator Value Register is asserted. 1 = Selects the sticky lock to the BB_LOCK field in the ADR SysClk Phase Rotator Value Register. The sticky lock is controlled by bit 4, sticky lock enable. When the sticky lock is set, it remains set. bit 4: Sticky lock enable. bits 5:7: Adjustable BB_LOCK window: 000 = At most, a one-count increment or decrement occurs to indicate a lock. 001 = At most, a two-count increment or decrement occurs to indicate a lock. 010 = At most, a three-count increment or decrement occurs to indicate a lock. 011 = At most, a four-count increment or decrement occurs to indicate a lock. 100 = At most, a five-count increment or decrement occurs to indicate a lock.
56	RW	SYSCLK_ROT_OVERRIDE_EN: Enables the use of the SYSCLK_ROT_OVERRIDE register value rather than the internally calculated SYSCLK_ROT value in the ADR SysClk Phase Rotator Value Register when set to 1. The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by four dphy_gckn clock cycles. Back-to-back APB write operations to this register provide the required separation. When this bit is written to 0 and was 1, the SYSCLK_ROT value in the ADR SysClk Phase Rotator Value Register is reset to zero.
57	RW	SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_gckn, the SysClk Phase Alignment Controller. This bit must be asserted after the PLL locks; it must be active for at least five SysClk cycles.
58	RW	SYSCLK_PHASE_CNTL_EN: Alignment enable to dphy_gckn, the SysClk Phase Alignment Controller. When high, it enables the controller. This bit must be asserted low at least 25 SysClk cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.
59	RW	SYSCLK_PHASE_DEFAULT_EN: This bit enables default start-up values to be output by dphy_gckn, the SysClk Phase Alignment Controller. This bit must be asserted during system reset and de-asserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	SYSCLK_POS_EDGE_ALIGN: This bit must be 0 for proper functional operation. It is an edge alignment strap to dphy_gckn, the SysClk Phase Alignment Controller. When high, it enables positive-edge alignment between dphy_gckn and SysClk. When low, it enables negative-edge alignment between dphy_gckn and SysClk. This bit is required to be low for ADR (negative-edge alignment).
61	RW	CONTINUOUS_UPDATE: 1 = The dphy_gckn, the SysClk Phase Alignment Controller, runs continuously and, thus, continuously aligns the dphy_gckn clock to the internal SysClk clock. 0 = The dphy_gckn, the SysClk Phase Alignment Controller, is only updated periodically under hardware control when an update will not interfere with the PHY functional operations.
62	RW	Reserved.

Bits	SCOM	Field Mnemonic: Description
63	RW	DD2_ADR_CG_DISABLE: 0 = Enable DD2 enhanced clock gating on ADR registers. 1 = Enable DD1 function.

Register Name	**ADR SysClk Phase Rotator Control Register**
Mnemonic	IOM0.DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR32S1
Address	800084320701143F (SCOM)
Description	This register controls the circuit that aligns the internal SysClk to the incoming dphy_gckn clock.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	SYSCLK_ROT_OVERRIDE: This field has a dual purpose: override control and lock control. When SYSCLK_ROT_OVERRIDE_EN = 1, this field is in override control mode. When SYSCLK_ROT_OVERRIDE_EN = 0, this field is in lock control. For override control: System clock (SysClk) phase-rotator override value. The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by four dphy_gckn clock cycles. Back-to-back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field in the ADR SysClk Phase Rotator Value Register is reserved. For lock control: Write this field to all zeros unless instructed otherwise by your IBM representative. bit 2: Lock select. Selects between lock status and sticky lock. 0 = Selects the current status of the lock. When the dphy_gckn detect has reached alignment between the dphy_gckn and SysClk, the BB_LOCK field in the ADR SysClk Phase Rotator Value Register is asserted. 1 = Selects the sticky lock to the BB_LOCK field in the ADR SysClk Phase Rotator Value Register. The sticky lock is controlled by bit 4, sticky lock enable. When the sticky lock is set, it remains set. bit 4: Sticky lock enable. bits 5:7: Adjustable BB_LOCK window: 000 = At most, a one-count increment or decrement occurs to indicate a lock. 001 = At most, a two-count increment or decrement occurs to indicate a lock. 010 = At most, a three-count increment or decrement occurs to indicate a lock. 011 = At most, a four-count increment or decrement occurs to indicate a lock. 100 = At most, a five-count increment or decrement occurs to indicate a lock.
56	RW	SYSCLK_ROT_OVERRIDE_EN: Enables the use of the SYSCLK_ROT_OVERRIDE register value rather than the internally calculated SYSCLK_ROT value in the ADR SysClk Phase Rotator Value Register when set to 1. The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by four dphy_gckn clock cycles. Back-to-back APB write operations to this register provide the required separation. When this bit is written to 0 and was 1, the SYSCLK_ROT value in the ADR SysClk Phase Rotator Value Register is reset to zero.
57	RW	SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_gckn, the SysClk Phase Alignment Controller. This bit must be asserted after the PLL locks; it must be active for at least five SysClk cycles.
58	RW	SYSCLK_PHASE_CNTL_EN: Alignment enable to dphy_gckn, the SysClk Phase Alignment Controller. When high, it enables the controller. This bit must be asserted low at least 25 SysClk cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.

Bits	SCOM	Field Mnemonic: Description
59	RW	SYSCLK_PHASE_DEFAULT_EN: This bit enables default start-up values to be output by dphy_gckn, the SysClk Phase Alignment Controller. This bit must be asserted during system reset and de-asserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	SYSCLK_POS_EDGE_ALIGN: This bit must be 0 for proper functional operation. It is an edge alignment strap to dphy_gckn, the SysClk Phase Alignment Controller. When high, it enables positive-edge alignment between dphy_gckn and SysClk. When low, it enables negative-edge alignment between dphy_gckn and SysClk. This bit is required to be low for ADR (negative-edge alignment).
61	RW	CONTINUOUS_UPDATE: 1 = The dphy_gckn, the SysClk Phase Alignment Controller, runs continuously and, thus, continuously aligns the dphy_gckn clock to the internal SysClk clock. 0 = The dphy_gckn , the SysClk Phase Alignment Controller, is only updated periodically under hardware control when an update will not interfere with the PHY functional operations.
62	RW	Reserved.
63	RW	DD2_ADR_CG_DISABLE: 0 = Enable DD2 enhanced clock gating on ADR registers. 1 = Enable DD1 function.

Register Name	ADR SysClk Phase Rotator Control Register
Mnemonic	IOM0.DDRPHY_ADR_SYSCLK_CNTL_PR_P2_ADR32S1
Address	800084320701183F (SCOM)
Description	This register controls the circuit that aligns the internal SysClk to the incoming dphy_gckn clock.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	SYSCLK_ROT_OVERRIDE: This field has a dual purpose: override control and lock control. When SYSCLK_ROT_OVERRIDE_EN = 1, this field is in override control mode. When SYSCLK_ROT_OVERRIDE_EN = 0, this field is in lock control. For override control: System clock (SysClk) phase-rotator override value. The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by four dphy_gckn clock cycles. Back-to-back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field in the ADR SysClk Phase Rotator Value Register is reserved. For lock control: Write this field to all zeros unless instructed otherwise by your IBM representative. bit 2: Lock select. Selects between lock status and sticky lock. 0 = Selects the current status of the lock. When the dphy_gckn detect has reached alignment between the dphy_gckn and SysClk, the BB_LOCK field in the ADR SysClk Phase Rotator Value Register is asserted. 1 = Selects the sticky lock to the BB_LOCK field in the ADR SysClk Phase Rotator Value Register. The sticky lock is controlled by bit 4, sticky lock enable. When the sticky lock is set, it remains set. bit 4: Sticky lock enable. bits 5:7: Adjustable BB_LOCK window: 000 = At most, a one-count increment or decrement occurs to indicate a lock. 001 = At most, a two-count increment or decrement occurs to indicate a lock. 010 = At most, a three-count increment or decrement occurs to indicate a lock. 011 = At most, a four-count increment or decrement occurs to indicate a lock. 100 = At most, a five-count increment or decrement occurs to indicate a lock.

Bits	SCOM	Field Mnemonic: Description
56	RW	SYSCLK_ROT_OVERRIDE_EN: Enables the use of the SYSCLK_ROT_OVERRIDE register value rather than the internally calculated SYSCLK_ROT value in the ADR SysClk Phase Rotator Value Register when set to 1. The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by four dphy_gckn clock cycles. Back-to-back APB write operations to this register provide the required separation. When this bit is written to 0 and was 1, the SYSCLK_ROT value in the ADR SysClk Phase Rotator Value Register is reset to zero.
57	RW	SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_gckn, the SysClk Phase Alignment Controller. This bit must be asserted after the PLL locks; it must be active for at least five SysClk cycles.
58	RW	SYSCLK_PHASE_CNTL_EN: Alignment enable to dphy_gckn, the SysClk Phase Alignment Controller. When high, it enables the controller. This bit must be asserted low at least 25 SysClk cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.
59	RW	SYSCLK_PHASE_DEFAULT_EN: This bit enables default start-up values to be output by dphy_gckn, the SysClk Phase Alignment Controller. This bit must be asserted during system reset and de-asserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	SYSCLK_POS_EDGE_ALIGN: This bit must be 0 for proper functional operation. It is an edge alignment strap to dphy_gckn, the SysClk Phase Alignment Controller. When high, it enables positive-edge alignment between dphy_gckn and SysClk. When low, it enables negative-edge alignment between dphy_gckn and SysClk. This bit is required to be low for ADR (negative-edge alignment).
61	RW	CONTINUOUS_UPDATE: 1 = The dphy_gckn, the SysClk Phase Alignment Controller, runs continuously and, thus, continuously aligns the dphy_gckn clock to the internal SysClk clock. 0 = The dphy_gckn, the SysClk Phase Alignment Controller, is only updated periodically under hardware control when an update will not interfere with the PHY functional operations.
62	RW	Reserved.
63	RW	DD2_ADR_CG_DISABLE: 0 = Enable DD2 enhanced clock gating on ADR registers. 1 = Enable DD1 function.

Register Name	ADR SysClk Phase Rotator Control Register
Mnemonic	IOM0.DDRPHY_ADR_SYSCLK_CNTL_PR_P3_ADR32S1
Address	8000843207011C3F (SCOM)
Description	This register controls the circuit that aligns the internal SysClk to the incoming dphy_gckn clock.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	Reserved.

Bits	SCOM	Field Mnemonic: Description
49:55	RW	SYSCLK_ROT_OVERRIDE: This field has a dual purpose: override control and lock control. When SYSCLK_ROT_OVERRIDE_EN = 1, this field is in override control mode. When SYSCLK_ROT_OVERRIDE_EN = 0, this field is in lock control. For override control: System clock (SysClk) phase-rotator override value. The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by four dphy_gckn clock cycles. Back-to-back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field in the ADR SysClk Phase Rotator Value Register is reserved. For lock control: Write this field to all zeros unless instructed otherwise by your IBM representative. bit 2: Lock select. Selects between lock status and sticky lock. 0 = Selects the current status of the lock. When the dphy_gckn detect has reached alignment between the dphy_gckn and SysClk, the BB_LOCK field in the ADR SysClk Phase Rotator Value Register is asserted. 1 = Selects the sticky lock to the BB_LOCK field in the ADR SysClk Phase Rotator Value Register. The sticky lock is controlled by bit 4, sticky lock enable. When the sticky lock is set, it remains set. bit 4: Sticky lock enable. bits 5:7: Adjustable BB_LOCK window: 000 = At most, a one-count increment or decrement occurs to indicate a lock. 001 = At most, a two-count increment or decrement occurs to indicate a lock. 010 = At most, a three-count increment or decrement occurs to indicate a lock. 011 = At most, a four-count increment or decrement occurs to indicate a lock. 100 = At most, a five-count increment or decrement occurs to indicate a lock.
56	RW	SYSCLK_ROT_OVERRIDE_EN: Enables the use of the SYSCLK_ROT_OVERRIDE register value rather than the internally calculated SYSCLK_ROT value in the ADR SysClk Phase Rotator Value Register when set to 1. The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by four dphy_gckn clock cycles. Back-to-back APB write operations to this register provide the required separation. When this bit is written to 0 and was 1, the SYSCLK_ROT value in the ADR SysClk Phase Rotator Value Register is reset to zero.
57	RW	SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_gckn, the SysClk Phase Alignment Controller. This bit must be asserted after the PLL locks; it must be active for at least five SysClk cycles.
58	RW	SYSCLK_PHASE_CNTL_EN: Alignment enable to dphy_gckn, the SysClk Phase Alignment Controller. When high, it enables the controller. This bit must be asserted low at least 25 SysClk cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.
59	RW	SYSCLK_PHASE_DEFAULT_EN: This bit enables default start-up values to be output by dphy_gckn, the SysClk Phase Alignment Controller. This bit must be asserted during system reset and de-asserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	SYSCLK_POS_EDGE_ALIGN: This bit must be 0 for proper functional operation. It is an edge alignment strap to dphy_gckn, the SysClk Phase Alignment Controller. When high, it enables positive-edge alignment between dphy_gckn and SysClk. When low, it enables negative-edge alignment between dphy_gckn and SysClk. This bit is required to be low for ADR (negative-edge alignment).
61	RW	CONTINUOUS_UPDATE: 1 = The dphy_gckn, the SysClk Phase Alignment Controller, runs continuously and, thus, continuously aligns the dphy_gckn clock to the internal SysClk clock. 0 = The dphy_gckn, the SysClk Phase Alignment Controller, is only updated periodically under hardware control when an update will not interfere with the PHY functional operations.
62	RW	Reserved.

Bits	SCOM	Field Mnemonic: Description
63	RW	DD2_ADR_CG_DISABLE: 0 = Enable DD2 enhanced clock gating on ADR registers. 1 = Enable DD1 function.

Register Name	ADR WRClk Phase Rotator Offset Value Register
Mnemonic	IOM0.DDRPHY_ADR_MCCLK_WRCLK_PR_STATIC_OFFSET_P0_ADR32S1
Address	800084330701103F (SCOM)
Description	The phase rotator static offset value is used to determine the phase of the WrClk with respect to the SysClk.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	TSYS_WRCLK: The static value of the system clock (SysClk) phase rotator to the write clock (WrClk) phase rotator. Set to ‘19’h for 2666 MT/s. Set to ‘17’h for 2400 MT/s. Set to ‘14’h for 2133 MT/s. Set to ‘12’h for 1866 MT/s. For zero-delay simulations, or simulations where the delay of the SysClk tree and the WrClk tree are equal, set this field to 60h.
56:63	RW	Reserved.

Register Name	ADR WRClk Phase Rotator Offset Value Register
Mnemonic	IOM0.DDRPHY_ADR_MCCLK_WRCLK_PR_STATIC_OFFSET_P1_ADR32S1
Address	800084330701143F (SCOM)
Description	The phase rotator static offset value is used to determine the phase of the WrClk with respect to the SysClk.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	TSYS_WRCLK: The static value of the system clock (SysClk) phase rotator to the write clock (WrClk) phase rotator. Set to ‘19’h for 2666 MT/s. Set to ‘17’h for 2400 MT/s. Set to ‘14’h for 2133 MT/s. Set to ‘12’h for 1866 MT/s. For zero-delay simulations, or simulations where the delay of the SysClk tree and the WrClk tree are equal, set this field to 60h.
56:63	RW	Reserved.

Register Name	ADR WRClk Phase Rotator Offset Value Register
Mnemonic	IOM0.DDRPHY_ADR_MCCLK_WRCLK_PR_STATIC_OFFSET_P2_ADR32S1
Address	800084330701183F (SCOM)
Description	The phase rotator static offset value is used to determine the phase of the WrClk with respect to the SysClk.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	TSYS_WRCLK: The static value of the system clock (SysClk) phase rotator to the write clock (WrClk) phase rotator. Set to '19'h for 2666 MT/s. Set to '17'h for 2400 MT/s. Set to '14'h for 2133 MT/s. Set to '12'h for 1866 MT/s. For zero-delay simulations, or simulations where the delay of the SysClk tree and the WrClk tree are equal, set this field to 60h.
56:63	RW	Reserved.

Register Name	ADR WRClk Phase Rotator Offset Value Register
Mnemonic	IOM0.DDRPHY_ADR_MCCLK_WRCLK_PR_STATIC_OFFSET_P3_ADR32S1
Address	8000843307011C3F (SCOM)
Description	The phase rotator static offset value is used to determine the phase of the WrClk with respect to the SysClk.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	TSYS_WRCLK: The static value of the system clock (SysClk) phase rotator to the write clock (WrClk) phase rotator. Set to '19'h for 2666 MT/s. Set to '17'h for 2400 MT/s. Set to '14'h for 2133 MT/s. Set to '12'h for 1866 MT/s. For zero-delay simulations, or simulations where the delay of the SysClk tree and the WrClk tree are equal, set this field to 60h.
56:63	RW	Reserved.

Register Name	ADR SysClk Phase Rotator Value Register
Mnemonic	IOM0.DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P0_ADR32S1
Address	800084340701103F (SCOM)
Description	This register provides read-only access to the value of the SysClk phase rotator calculated value, which represents the phase difference between the MCClk phase and SysClk initial phase.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b0000000000000000000000000000000000000000000000000
49:55	ROX	SYSCLK_ROT: Internally calculated value of the dphy_gckn clock phase to the SysClock (SysClk) phase offset. Used to set the SysClock phase rotator when SYSCLK_ROT_OVERRIDE_EN = 0. For more information, see the ADR SysClk Phase Rotator Control Register. These bits reset, but are continually loaded with the dphy_gckn to SysClk alignment circuit calculated value for the SysClk delay, exclusive of reset.

Bits	SCOM	Field Mnemonic: Description
56	RO	BB_LOCK: 1 = The dphy_gckn/SysClk phase-alignment controller has reached alignment between the dphy_gckn and SysClk as of the last update by the dphy_gckn/SysClk phase-alignment controller. 0 = The dphy_gckn and SysClk are not in alignment as of the last update by the dphy_gckn/SysClk phase-alignment controller. There are two types of locks. Refer to the SYSCLK_ROT_OVERRIDE field in the ADR SysClk Phase Rotator Control Register.
57:63	RO	Reserved.

Register Name	ADR SysClk Phase Rotator Value Register
Mnemonic	IOM0.DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P1_ADR32S1
Address	800084340701143F (SCOM)
Description	This register provides read-only access to the value of the SysClk phase rotator calculated value, which represents the phase difference between the MCClk phase and SysClk initial phase.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	ROX	SYSCLK_ROT: Internally calculated value of the dphy_gckn clock phase to the SysClock (SysClk) phase offset. Used to set the SysClock phase rotator when SYSCLK_ROT_OVERRIDE_EN = 0. For more information, see the ADR SysClk Phase Rotator Control Register. These bits reset, but are continually loaded with the dphy_gckn to SysClk alignment circuit calculated value for the SysClk delay, exclusive of reset.
56	RO	BB_LOCK: 1 = The dphy_gckn/SysClk phase-alignment controller has reached alignment between the dphy_gckn and SysClk as of the last update by the dphy_gckn/SysClk phase-alignment controller. 0 = The dphy_gckn and SysClk are not in alignment as of the last update by the dphy_gckn/SysClk phase-alignment controller. There are two types of locks. Refer to the SYSCLK_ROT_OVERRIDE field in the ADR SysClk Phase Rotator Control Register.
57:63	RO	Reserved.

Register Name	ADR SysClk Phase Rotator Value Register
Mnemonic	IOM0.DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P2_ADR32S1
Address	800084340701183F (SCOM)
Description	This register provides read-only access to the value of the SysClk phase rotator calculated value, which represents the phase difference between the MCClk phase and SysClk initial phase.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	ROX	SYSCLK_ROT: Internally calculated value of the dphy_gckn clock phase to the SysClock (SysClk) phase offset. Used to set the SysClock phase rotator when SYSCLK_ROT_OVERRIDE_EN = 0. For more information, see the ADR SysClk Phase Rotator Control Register. These bits reset, but are continually loaded with the dphy_gckn to SysClk alignment circuit calculated value for the SysClk delay, exclusive of reset.

Bits	SCOM	Field Mnemonic: Description
56	RO	BB_LOCK: 1 = The dphy_gckn/SysClk phase-alignment controller has reached alignment between the dphy_gckn and SysClk as of the last update by the dphy_gckn/SysClk phase-alignment controller. 0 = The dphy_gckn and SysClk are not in alignment as of the last update by the dphy_gckn/SysClk phase-alignment controller. There are two types of locks. Refer to the SYSCLK_ROT_OVERRIDE field in the ADR SysClk Phase Rotator Control Register.
57:63	RO	Reserved.

Register Name	ADR SysClk Phase Rotator Value Register
Mnemonic	IOM0.DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P3_ADR32S1
Address	8000843407011C3F (SCOM)
Description	This register provides read-only access to the value of the SysClk phase rotator calculated value, which represents the phase difference between the MCClk phase and SysClk initial phase.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	ROX	SYSCLK_ROT: Internally calculated value of the dphy_gckn clock phase to the SysClock (SysClk) phase offset. Used to set the SysClock phase rotator when SYSCLK_ROT_OVERRIDE_EN = 0. For more information, see the ADR SysClk Phase Rotator Control Register. These bits reset, but are continually loaded with the dphy_gckn to SysClk alignment circuit calculated value for the SysClk delay, exclusive of reset.
56	RO	BB_LOCK: 1 = The dphy_gckn/SysClk phase-alignment controller has reached alignment between the dphy_gckn and SysClk as of the last update by the dphy_gckn/SysClk phase-alignment controller. 0 = The dphy_gckn and SysClk are not in alignment as of the last update by the dphy_gckn/SysClk phase-alignment controller. There are two types of locks. Refer to the SYSCLK_ROT_OVERRIDE field in the ADR SysClk Phase Rotator Control Register.
57:63	RO	Reserved.

Register Name	ADR Output Driver Force and ATEST Control Register
Mnemonic	IOM0.DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR32S1
Address	800084350701103F (SCOM)
Description	This register provides control for forcing outputs to known states for characterization and ATEST control. This register is reserved for manufacturing test and characterization purposes. It resets to a functional value, and its contents must not be altered by the user.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48	RW	FLUSH: Manufacturing macro test control for ANALOG. This bit controls whether the transmit FIFO is flushed or not (when flushed, half-rate data is no longer valid).
49	RW	FORCE_EN: Output force enable bit.
50	RW	INIT_IO: Enables the DC-level translator in front of the TX output stages, which initialize the top plate voltage of the fly cap in the AC-level translator at startup. This voltage must be applied for a minimum of five clock cycles after startup, and before the I/Os can be used. This requirement also applies to all manufacturing test modes.

Bits	SCOM	Field Mnemonic: Description
51:54	RW	HS_PROBE_A_SEL_0_3: High-speed probe A select.
55:58	RW	HS_PROBE_B_SEL_0_3: High-speed probe B select.
59:61	RW	ATESTSEL_0_2: Lowest level of ATEST selection, ATESTSEL(0:2).
62:63	RW	Reserved.

Register Name	ADR Output Driver Force and ATEST Control Register
Mnemonic	IOM0.DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR32S1
Address	800084350701143F (SCOM)
Description	This register provides control for forcing outputs to known states for characterization and ATEST control. This register is reserved for manufacturing test and characterization purposes. It resets to a functional value, and its contents must not be altered by the user.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	RW	FLUSH: Manufacturing macro test control for ANALOG. This bit controls whether the transmit FIFO is flushed or not (when flushed, half-rate data is no longer valid).
49	RW	FORCE_EN: Output force enable bit.
50	RW	INIT_IO: Enables the DC-level translator in front of the TX output stages, which initialize the top plate voltage of the fly cap in the AC-level translator at startup. This voltage must be applied for a minimum of five clock cycles after startup, and before the I/Os can be used. This requirement also applies to all manufacturing test modes.
51:54	RW	HS_PROBE_A_SEL_0_3: High-speed probe A select.
55:58	RW	HS_PROBE_B_SEL_0_3: High-speed probe B select.
59:61	RW	ATESTSEL_0_2: Lowest level of ATEST selection, ATESTSEL(0:2).
62:63	RW	Reserved.

Register Name	ADR Output Driver Force and ATEST Control Register
Mnemonic	IOM0.DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P2_ADR32S1
Address	800084350701183F (SCOM)
Description	This register provides control for forcing outputs to known states for characterization and ATEST control. This register is reserved for manufacturing test and characterization purposes. It resets to a functional value, and its contents must not be altered by the user.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	RW	FLUSH: Manufacturing macro test control for ANALOG. This bit controls whether the transmit FIFO is flushed or not (when flushed, half-rate data is no longer valid).
49	RW	FORCE_EN: Output force enable bit.
50	RW	INIT_IO: Enables the DC-level translator in front of the TX output stages, which initialize the top plate voltage of the fly cap in the AC-level translator at startup. This voltage must be applied for a minimum of five clock cycles after startup, and before the I/Os can be used. This requirement also applies to all manufacturing test modes.
51:54	RW	HS_PROBE_A_SEL_0_3: High-speed probe A select.

Bits	SCOM	Field Mnemonic: Description
55:58	RW	HS_PROBE_B_SEL_0_3: High-speed probe B select.
59:61	RW	ATESTSEL_0_2: Lowest level of ATEST selection, ATESTSEL(0:2).
62:63	RW	Reserved.

Register Name	ADR Output Driver Force and ATEST Control Register
Mnemonic	IOM0.DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P3_ADR32S1
Address	8000843507011C3F (SCOM)
Description	This register provides control for forcing outputs to known states for characterization and ATEST control. This register is reserved for manufacturing test and characterization purposes. It resets to a functional value, and its contents must not be altered by the user.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48	RW	FLUSH: Manufacturing macro test control for ANALOG. This bit controls whether the transmit FIFO is flushed or not (when flushed, half-rate data is no longer valid).
49	RW	FORCE_EN: Output force enable bit.
50	RW	INIT_IO: Enables the DC-level translator in front of the TX output stages, which initialize the top plate voltage of the fly cap in the AC-level translator at startup. This voltage must be applied for a minimum of five clock cycles after startup, and before the I/Os can be used. This requirement also applies to all manufacturing test modes.
51:54	RW	HS_PROBE_A_SEL_0_3: High-speed probe A select.
55:58	RW	HS_PROBE_B_SEL_0_3: High-speed probe B select.
59:61	RW	ATESTSEL_0_2: Lowest level of ATEST selection, ATESTSEL(0:2).
62:63	RW	Reserved.

Register Name	ADR Output Driver Force Value 0 Register
Mnemonic	IOM0.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE0_P0_ADR32S1
Address	800084360701103F (SCOM)
Description	These registers provide the values to be forced out of the drivers for characterization. Each bit of each register controls its respective lane on the appropriate side. Bits must be enabled in the ADR Bit Enable Register to be controlled by this register. These registers are reserved for manufacturing test and characterization purposes.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48:63	RW	OUTPUT_DRIVER_FORCE_VALUE: The value to be forced out of the driver. Bit assignments represent the respective lanes under test. Reserved.

Register Name	ADR Output Driver Force Value 0 Register
Mnemonic	IOM0.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE0_P1_ADR32S1
Address	800084360701143F (SCOM)
Description	These registers provide the values to be forced out of the drivers for characterization. Each bit of each register controls its respective lane on the appropriate side. Bits must be enabled in the ADR Bit Enable Register to be controlled by this register. These registers are reserved for manufacturing test and characterization purposes.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	OUTPUT_DRIVER_FORCE_VALUE: The value to be forced out of the driver. Bit assignments represent the respective lanes under test. Reserved.

Register Name	ADR Output Driver Force Value 0 Register
Mnemonic	IOM0.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE0_P2_ADR32S1
Address	800084360701183F (SCOM)
Description	These registers provide the values to be forced out of the drivers for characterization. Each bit of each register controls its respective lane on the appropriate side. Bits must be enabled in the ADR Bit Enable Register to be controlled by this register. These registers are reserved for manufacturing test and characterization purposes.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	OUTPUT_DRIVER_FORCE_VALUE: The value to be forced out of the driver. Bit assignments represent the respective lanes under test. Reserved.

Register Name	ADR Output Driver Force Value 0 Register
Mnemonic	IOM0.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE0_P3_ADR32S1
Address	8000843607011C3F (SCOM)
Description	These registers provide the values to be forced out of the drivers for characterization. Each bit of each register controls its respective lane on the appropriate side. Bits must be enabled in the ADR Bit Enable Register to be controlled by this register. These registers are reserved for manufacturing test and characterization purposes.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	OUTPUT_DRIVER_FORCE_VALUE: The value to be forced out of the driver. Bit assignments represent the respective lanes under test. Reserved.

Register Name	ADR Output Driver Force Value 1 Register
Mnemonic	IOM0.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE1_P0_ADR32S1
Address	800084370701103F (SCOM)
Description	These registers provide the values to be forced out of the drivers for characterization. Each bit of each register controls its respective lane on the appropriate side. Bits must be enabled in the ADR Bit Enable Register to be controlled by this register. These registers are reserved for manufacturing test and characterization purposes.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	OUTPUT_DRIVER_FORCE_VALUE: The value to be forced out of the driver. Bit assignments represent the respective lanes under test. Reserved.

Register Name	ADR Output Driver Force Value 1 Register
Mnemonic	IOM0.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE1_P1_ADR32S1
Address	800084370701143F (SCOM)
Description	These registers provide the values to be forced out of the drivers for characterization. Each bit of each register controls its respective lane on the appropriate side. Bits must be enabled in the ADR Bit Enable Register to be controlled by this register. These registers are reserved for manufacturing test and characterization purposes.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	OUTPUT_DRIVER_FORCE_VALUE: The value to be forced out of the driver. Bit assignments represent the respective lanes under test. Reserved.

Register Name	ADR Output Driver Force Value 1 Register
Mnemonic	IOM0.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE1_P2_ADR32S1
Address	800084370701183F (SCOM)
Description	These registers provide the values to be forced out of the drivers for characterization. Each bit of each register controls its respective lane on the appropriate side. Bits must be enabled in the ADR Bit Enable Register to be controlled by this register. These registers are reserved for manufacturing test and characterization purposes.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	OUTPUT_DRIVER_FORCE_VALUE: The value to be forced out of the driver. Bit assignments represent the respective lanes under test. Reserved.

Register Name	ADR Output Driver Force Value 1 Register
Mnemonic	IOM0.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE1_P3_ADR32S1
Address	8000843707011C3F (SCOM)
Description	These registers provide the values to be forced out of the drivers for characterization. Each bit of each register controls its respective lane on the appropriate side. Bits must be enabled in the ADR Bit Enable Register to be controlled by this register. These registers are reserved for manufacturing test and characterization purposes.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	OUTPUT_DRIVER_FORCE_VALUE: The value to be forced out of the driver. Bit assignments represent the respective lanes under test. Reserved.

Register Name	ADR DCD Control Register
Mnemonic	IOM0.DDRPHY_ADR_DCD_CONTROL_P0_ADR32S1
Address	800084380701103F (SCOM)
Description	This register controls the duty cycle distortion (DCD) analog circuitry on the clock feeding the DLL. **Note:** When writing the register, software must write bit 63 to 0b0 to avoid a parity error.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:55	RWX	DLL_DCD_ADJUST: This value controls the amount of duty cycle correction that occurs on the grid clock before it enters the DLL. As the value increases, the clock = 1 part gets longer. As values decrease, the clock = 0 part gets longer. This is the seed value for the DCD calibration algorithm.
56	RW	DLL_DCD_CORRECT_EN: Determine whether the duty cycle distortion logic in the DLL includes a loop to further correct for DCD. 0 = Loop is not included. 1 = Loop is included.
57	RW	DLL_DCD_ITER_A: Controls the connection of DCD comparator input to null out comparator offset. 0 = B answer. 1 = A answer. The A and B answers must be averaged to determine the DLL_DCD_ADJUST value.
58	RW	DLL_DCD_CAL_ENABLE: DCD calibration enable. 0 = Reset the calibration state machine (clears DLL_DCD_CAL_DONE and DLL_DCD_CAL_ERROR). 1 = Enables calibration (calibration is complete with the assertion of DLL_DCD_CAL_DONE).
59	RW	Reserved.
60	RW	DLL_DCD_POWERDOWN: 0 = Normal operation. 1 = Power down the DCD circuit for power savings.
61	RWX	DLL_DCD_CAL_DONE: When DCD_CAL_ENABLE is set, this bit indicates the calibration is complete and the calibrated value has been loaded into the DLL_DCD_ADJUST field of this register.
62	RWX	DLL_DCD_CAL_ERROR: If this bit is asserted along with DLL_DCD_CAL_DONE, it indicates the calibration failed to find a solution. Either DLL_DCD_ADJUST reached a maximum value of 0xFF or a minimum value of 0x00.
63	RO	DLL_DCD_COMPARE_OUT: (Read only.) Result of the DCD comparator. 0 = Need to increase DLL_DCD_ADJUST. 1 = Need to decrease DLL_DCD_ADJUST.

Register Name	ADR DCD Control Register
Mnemonic	IOM0.DDRPHY_ADR_DCD_CONTROL_P1_ADR32S1
Address	800084380701143F (SCOM)
Description	This register controls the duty cycle distortion (DCD) analog circuitry on the clock feeding the DLL. **Note:** When writing the register, software must write bit 63 to 0b0 to avoid a parity error.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:55	RWX	DLL_DCD_ADJUST: This value controls the amount of duty cycle correction that occurs on the grid clock before it enters the DLL. As the value increases, the clock = 1 part gets longer. As values decrease, the clock = 0 part gets longer. This is the seed value for the DCD calibration algorithm.

Bits	SCOM	Field Mnemonic: Description
56	RW	DLL_DCD_CORRECT_EN: Determine whether the duty cycle distortion logic in the DLL includes a loop to further correct for DCD. 0 = Loop is not included. 1 = Loop is included.
57	RW	DLL_DCD_ITER_A: Controls the connection of DCD comparator input to null out comparator offset. 0 = B answer. 1 = A answer. The A and B answers must be averaged to determine the DLL_DCD_ADJUST value.
58	RW	DLL_DCD_CAL_ENABLE: DCD calibration enable. 0 = Reset the calibration state machine (clears DLL_DCD_CAL_DONE and DLL_DCD_CAL_ERROR). 1 = Enables calibration (calibration is complete with the assertion of DLL_DCD_CAL_DONE).
59	RW	Reserved.
60	RW	DLL_DCD_POWERDOWN: 0 = Normal operation. 1 = Power down the DCD circuit for power savings.
61	RWX	DLL_DCD_CAL_DONE: When DCD_CAL_ENABLE is set, this bit indicates the calibration is complete and the calibrated value has been loaded into the DLL_DCD_ADJUST field of this register.
62	RWX	DLL_DCD_CAL_ERROR: If this bit is asserted along with DLL_DCD_CAL_DONE, it indicates the calibration failed to find a solution. Either DLL_DCD_ADJUST reached a maximum value of 0xFF or a minimum value of 0x00.
63	RO	DLL_DCD_COMPARE_OUT: (Read only.) Result of the DCD comparator. 0 = Need to increase DLL_DCD_ADJUST. 1 = Need to decrease DLL_DCD_ADJUST.

Register Name	ADR DCD Control Register
Mnemonic	IOM0.DDRPHY_ADR_DCD_CONTROL_P2_ADR32S1
Address	800084380701183F (SCOM)
Description	This register controls the duty cycle distortion (DCD) analog circuitry on the clock feeding the DLL. **Note:** When writing the register, software must write bit 63 to 0b0 to avoid a parity error.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	DLL_DCD_ADJUST: This value controls the amount of duty cycle correction that occurs on the grid clock before it enters the DLL. As the value increases, the clock = 1 part gets longer. As values decrease, the clock = 0 part gets longer. This is the seed value for the DCD calibration algorithm.
56	RW	DLL_DCD_CORRECT_EN: Determine whether the duty cycle distortion logic in the DLL includes a loop to further correct for DCD. 0 = Loop is not included. 1 = Loop is included.
57	RW	DLL_DCD_ITER_A: Controls the connection of DCD comparator input to null out comparator offset. 0 = B answer. 1 = A answer. The A and B answers must be averaged to determine the DLL_DCD_ADJUST value.
58	RW	DLL_DCD_CAL_ENABLE: DCD calibration enable. 0 = Reset the calibration state machine (clears DLL_DCD_CAL_DONE and DLL_DCD_CAL_ERROR). 1 = Enables calibration (calibration is complete with the assertion of DLL_DCD_CAL_DONE).
59	RW	Reserved.

Bits	SCOM	Field Mnemonic: Description
60	RW	DLL_DCD_POWERDOWN: 0 = Normal operation. 1 = Power down the DCD circuit for power savings.
61	RWX	DLL_DCD_CAL_DONE: When DCD_CAL_ENABLE is set, this bit indicates the calibration is complete and the calibrated value has been loaded into the DLL_DCD_ADJUST field of this register.
62	RWX	DLL_DCD_CAL_ERROR: If this bit is asserted along with DLL_DCD_CAL_DONE, it indicates the calibration failed to find a solution. Either DLL_DCD_ADJUST reached a maximum value of 0xFF or a minimum value of 0x00.
63	RO	DLL_DCD_COMPARE_OUT: (Read only.) Result of the DCD comparator. 0 = Need to increase DLL_DCD_ADJUST. 1 = Need to decrease DLL_DCD_ADJUST.

Register Name	**ADR DCD Control Register**
Mnemonic	IOM0.DDRPHY_ADR_DCD_CONTROL_P3_ADR32S1
Address	8000843807011C3F (SCOM)
Description	This register controls the duty cycle distortion (DCD) analog circuitry on the clock feeding the DLL. **Note:** When writing the register, software must write bit 63 to 0b0 to avoid a parity error.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:55	RWX	DLL_DCD_ADJUST: This value controls the amount of duty cycle correction that occurs on the grid clock before it enters the DLL. As the value increases, the clock = 1 part gets longer. As values decrease, the clock = 0 part gets longer. This is the seed value for the DCD calibration algorithm.
56	RW	DLL_DCD_CORRECT_EN: Determine whether the duty cycle distortion logic in the DLL includes a loop to further correct for DCD. 0 = Loop is not included. 1 = Loop is included.
57	RW	DLL_DCD_ITER_A: Controls the connection of DCD comparator input to null out comparator offset. 0 = B answer. 1 = A answer. The A and B answers must be averaged to determine the DLL_DCD_ADJUST value.
58	RW	DLL_DCD_CAL_ENABLE: DCD calibration enable. 0 = Reset the calibration state machine (clears DLL_DCD_CAL_DONE and DLL_DCD_CAL_ERROR). 1 = Enables calibration (calibration is complete with the assertion of DLL_DCD_CAL_DONE).
59	RW	Reserved.
60	RW	DLL_DCD_POWERDOWN: 0 = Normal operation. 1 = Power down the DCD circuit for power savings.
61	RWX	DLL_DCD_CAL_DONE: When DCD_CAL_ENABLE is set, this bit indicates the calibration is complete and the calibrated value has been loaded into the DLL_DCD_ADJUST field of this register.
62	RWX	DLL_DCD_CAL_ERROR: If this bit is asserted along with DLL_DCD_CAL_DONE, it indicates the calibration failed to find a solution. Either DLL_DCD_ADJUST reached a maximum value of 0xFF or a minimum value of 0x00.
63	RO	DLL_DCD_COMPARE_OUT: (Read only.) Result of the DCD comparator. 0 = Need to increase DLL_DCD_ADJUST. 1 = Need to decrease DLL_DCD_ADJUST.

Register Name	ADR RESERVED 3 Register
Mnemonic	IOM0.DDRPHY_ADR_RESERVED2_P0_ADR32S1
Address	800084390701103F (SCOM)
Description	Currently reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	Reserved.

Register Name	ADR RESERVED 3 Register
Mnemonic	IOM0.DDRPHY_ADR_RESERVED2_P1_ADR32S1
Address	800084390701143F (SCOM)
Description	Currently reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	Reserved.

Register Name	ADR RESERVED 3 Register
Mnemonic	IOM0.DDRPHY_ADR_RESERVED2_P2_ADR32S1
Address	800084390701183F (SCOM)
Description	Currently reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	Reserved.

Register Name	ADR RESERVED 3 Register
Mnemonic	IOM0.DDRPHY_ADR_RESERVED2_P3_ADR32S1
Address	8000843907011C3F (SCOM)
Description	Currently reserved register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	Reserved.

Register Name	ADR DLL Control Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_CNTL_P0_ADR32S1
Address	8000843A0701103F (SCOM)
Description	This register controls the DLL calibration logic. **CAUTION:** This register must not be written while hardware calibration is active. **Note:** When writing the register, software must write bits 61:63 to 0b000 to avoid a parity error.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	INIT_RXDLL_CAL_RESET: 1 = DLL reset; the DLL output clocks are not correct. 0 = Initiate full calibration. Leave this bit at '0' after calibration. **Note:** Power must be on and stable to the analog DLL logic a minimum of 100 ns before deactivating reset.
49	RW	INIT_RXDLL_CAL_UPDATE: When 1, requests DLL calibration to update/adjust fine delays only. VREG and coarse calibration are skipped, although they must have completed successfully before writing this bit to 1. **Note:** This bit starts at 0, but hardware automatically sets it to 1 on the riding edge of "cal_good," which should occur after full calibration. This enables fine calibration to run continuously after full calibration. When software writes this bit to 0, reads of the bit might still show 1 until the current fine calibration sequence finishes. **Note:** Power must be on and stable to the analog DLL logic for a minimum of 100 sec before activating CAL_UPDATE.
50:51	RW	REGS_RXDLL_CAL_SKIP: Skip calibration steps (requires manual presets too). bit 0: When 1, skip VREG calibration. bit 1: When 1, skip coarse delay calibration.
52	RW	REGS_RXDLL_COARSE_ADJ_BY2: At the end of coarse calibration, the DAC code is reduced to set the total delay under one period before entering fine calibration. This bit controls whether the reduction is one or two code increments. When 0, change final coarse delay setting by one.(default). When 1, change final coarse delay setting by two. **Note:** This bit has lower priority than REGS_RXDLL_COARSE_ADJ_BY0 if both are set.
53:55	RW	RXREG_DLL_FILTER_LENGTH_DC: Adjusts the number of lead/lag samples to filter out. A smaller binary code gives a smaller number of samples.
56:58	RW	RXREG_DLL_LEAD_LAG_SEPARATION_DC: Adjusts the number of lead more than lag or lag more than lead to get a + phase adjustment or a - phase adjustment.
59	RW	DLL_EN_DRIVER_INVFB_DC: Enable driver inverter feedback. Controls when cross-coupled inverters are included across DLL output drivers. Adding the inverters can improve driver performance, but might introduce excessive current if the DLL outputs are not close to their final values. The intent is to exclude the cross coupling during initial calibration, but possibly include it when repeating fine calibration only because DLL outputs are close to their optimal values during fine calibration. 0 = Disable use of cross-coupled inverters on DLL output drivers. 1 = Enable use of cross-coupled inverters on DLL output drivers.
60	RO	Reserved.
61	ROX	CAL_GOOD: (Read only.)When 1, calibration finished successfully. When 0, calibration is on-going or resulted in an error if either CAL_ERROR or CAL_ERROR_FINE is set. **Note:** This is the local copy of CAL_GOOD directly from the DLL calibration logic. Thus, it will alternate between 0 and 1 when fine calibration runs continuously.
62	ROX	CAL_ERROR: (Read only.)When 1, VREG or coarse calibration finished with an error.
63	ROX	CAL_ERROR_FINE: (Read only.)When 1, fine calibration finished with an error.

Register Name	ADR DLL Control Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_CNTL_P1_ADR32S1
Address	8000843A0701143F (SCOM)
Description	This register controls the DLL calibration logic. **CAUTION:** This register must not be written while hardware calibration is active. **Note:** When writing the register, software must write bits 61:63 to 0b000 to avoid a parity error.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	RW	INIT_RXDLL_CAL_RESET: 1 = DLL reset; the DLL output clocks are not correct. 0 = Initiate full calibration. Leave this bit at '0' after calibration. **Note:** Power must be on and stable to the analog DLL logic a minimum of 100 ns before deactivating reset.
49	RW	INIT_RXDLL_CAL_UPDATE: When 1, requests DLL calibration to update/adjust fine delays only. VREG and coarse calibration are skipped, although they must have completed successfully before writing this bit to 1. **Note:** This bit starts at 0, but hardware automatically sets it to 1 on the riding edge of "cal_good," which should occur after full calibration. This enables fine calibration to run continuously after full calibration. When software writes this bit to 0, reads of the bit might still show 1 until the current fine calibration sequence finishes. **Note:** Power must be on and stable to the analog DLL logic for a minimum of 100 ns before activating CAL_UPDATE.
50:51	RW	REGS_RXDLL_CAL_SKIP: Skip calibration steps (requires manual presets too). bit 0: When 1, skip VREG calibration. bit 1: When 1, skip coarse delay calibration.
52	RW	REGS_RXDLL_COARSE_ADJ_BY2: At the end of coarse calibration, the DAC code is reduced to set the total delay under one period before entering fine calibration. This bit controls whether the reduction is one or two code increments. When 0, change final coarse delay setting by one.(default). When 1, change final coarse delay setting by two. **Note:** This bit has lower priority than REGS_RXDLL_COARSE_ADJ_BY0 if both are set.
53:55	RW	RXREG_DLL_FILTER_LENGTH_DC: Adjusts the number of lead/lag samples to filter out. A smaller binary code gives a smaller number of samples.
56:58	RW	RXREG_DLL_LEAD_LAG_SEPARATION_DC: Adjusts the number of lead more than lag or lag more than lead to get a + phase adjustment or a - phase adjustment.
59	RW	DLL_EN_DRIVER_INVFB_DC: Enable driver inverter feedback. Controls when cross-coupled inverters are included across DLL output drivers. Adding the inverters can improve driver performance, but might introduce excessive current if the DLL outputs are not close to their final values. The intent is to exclude the cross coupling during initial calibration, but possibly include it when repeating fine calibration only because DLL outputs are close to their optimal values during fine calibration. 0 = Disable use of cross-coupled inverters on DLL output drivers. 1 = Enable use of cross-coupled inverters on DLL output drivers.
60	RO	Reserved.
61	ROX	CAL_GOOD: (Read only.)When 1, calibration finished successfully. When 0, calibration is on-going or resulted in an error if either CAL_ERROR or CAL_ERROR_FINE is set. **Note:** This is the local copy of CAL_GOOD directly from the DLL calibration logic. Thus, it will alternate between 0 and 1 when fine calibration runs continuously.
62	ROX	CAL_ERROR: (Read only.)When 1, VREG or coarse calibration finished with an error.
63	ROX	CAL_ERROR_FINE: (Read only.)When 1, fine calibration finished with an error.

Register Name	ADR DLL Control Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_CNTL_P2_ADR32S1
Address	8000843A0701183F (SCOM)
Description	This register controls the DLL calibration logic. **CAUTION:** This register must not be written while hardware calibration is active. **Note:** When writing the register, software must write bits 61:63 to 0b000 to avoid a parity error.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	INIT_RXDLL_CAL_RESET: 1 = DLL reset; the DLL output clocks are not correct. 0 = Initiate full calibration. Leave this bit at '0' after calibration. **Note:** Power must be on and stable to the analog DLL logic a minimum of 100 ns before deactivating reset.
49	RW	INIT_RXDLL_CAL_UPDATE: When 1, requests DLL calibration to update/adjust fine delays only. VREG and coarse calibration are skipped, although they must have completed successfully before writing this bit to 1. **Note:** This bit starts at 0, but hardware automatically sets it to 1 on the riding edge of "cal_good," which should occur after full calibration. This enables fine calibration to run continuously after full calibration. When software writes this bit to 0, reads of the bit might still show 1 until the current fine calibration sequence finishes. **Note:** Power must be on and stable to the analog DLL logic for a minimum of 100 ns before activating CAL_UPDATE.
50:51	RW	REGS_RXDLL_CAL_SKIP: Skip calibration steps (requires manual presets too). bit 0: When 1, skip VREG calibration. bit 1: When 1, skip coarse delay calibration.
52	RW	REGS_RXDLL_COARSE_ADJ_BY2: At the end of coarse calibration, the DAC code is reduced to set the total delay under one period before entering fine calibration. This bit controls whether the reduction is one or two code increments. When 0, change final coarse delay setting by one.(default). When 1, change final coarse delay setting by two. **Note:** This bit has lower priority than REGS_RXDLL_COARSE_ADJ_BY0 if both are set.
53:55	RW	RXREG_DLL_FILTER_LENGTH_DC: Adjusts the number of lead/lag samples to filter out. A smaller binary code gives a smaller number of samples.
56:58	RW	RXREG_DLL_LEAD_LAG_SEPARATION_DC: Adjusts the number of lead more than lag or lag more than lead to get a + phase adjustment or a - phase adjustment.
59	RW	DLL_EN_DRIVER_INVFB_DC: Enable driver inverter feedback. Controls when cross-coupled inverters are included across DLL output drivers. Adding the inverters can improve driver performance, but might introduce excessive current if the DLL outputs are not close to their final values. The intent is to exclude the cross coupling during initial calibration, but possibly include it when repeating fine calibration only because DLL outputs are close to their optimal values during fine calibration. 0 = Disable use of cross-coupled inverters on DLL output drivers. 1 = Enable use of cross-coupled inverters on DLL output drivers.
60	RO	Reserved.
61	ROX	CAL_GOOD: (Read only.) When 1, calibration finished successfully. When 0, calibration is on-going or resulted in an error if either CAL_ERROR or CAL_ERROR_FINE is set. **Note:** This is the local copy of CAL_GOOD directly from the DLL calibration logic. Thus, it will alternate between 0 and 1 when fine calibration runs continuously.
62	ROX	CAL_ERROR: (Read only.) When 1, VREG or coarse calibration finished with an error.
63	ROX	CAL_ERROR_FINE: (Read only.) When 1, fine calibration finished with an error.

Register Name	ADR DLL Control Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_CNTL_P3_ADR32S1
Address	8000843A07011C3F (SCOM)
Description	This register controls the DLL calibration logic. **CAUTION:** This register must not be written while hardware calibration is active. **Note:** When writing the register, software must write bits 61:63 to 0b000 to avoid a parity error.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	INIT_RXDLL_CAL_RESET: 1 = DLL reset; the DLL output clocks are not correct. 0 = Initiate full calibration. Leave this bit at '0' after calibration. **Note:** Power must be on and stable to the analog DLL logic a minimum of 100 ns before deactivating reset.
49	RW	INIT_RXDLL_CAL_UPDATE: When 1, requests DLL calibration to update/adjust fine delays only. VREG and coarse calibration are skipped, although they must have completed successfully before writing this bit to 1. **Note:** This bit starts at 0, but hardware automatically sets it to 1 on the riding edge of "cal_good," which should occur after full calibration. This enables fine calibration to run continuously after full calibration. When software writes this bit to 0, reads of the bit might still show 1 until the current fine calibration sequence finishes. **Note:** Power must be on and stable to the analog DLL logic for a minimum of 100 ns before activating CAL_UPDATE.
50:51	RW	REGS_RXDLL_CAL_SKIP: Skip calibration steps (requires manual presets too). bit 0: When 1, skip VREG calibration. bit 1: When 1, skip coarse delay calibration.
52	RW	REGS_RXDLL_COARSE_ADJ_BY2: At the end of coarse calibration, the DAC code is reduced to set the total delay under one period before entering fine calibration. This bit controls whether the reduction is one or two code increments. When 0, change final coarse delay setting by one.(default). When 1, change final coarse delay setting by two. **Note:** This bit has lower priority than REGS_RXDLL_COARSE_ADJ_BY0 if both are set.
53:55	RW	RXREG_DLL_FILTER_LENGTH_DC: Adjusts the number of lead/lag samples to filter out. A smaller binary code gives a smaller number of samples.
56:58	RW	RXREG_DLL_LEAD_LAG_SEPARATION_DC: Adjusts the number of lead more than lag or lag more than lead to get a + phase adjustment or a - phase adjustment.
59	RW	DLL_EN_DRIVER_INVFB_DC: Enable driver inverter feedback. Controls when cross-coupled inverters are included across DLL output drivers. Adding the inverters can improve driver performance, but might introduce excessive current if the DLL outputs are not close to their final values. The intent is to exclude the cross coupling during initial calibration, but possibly include it when repeating fine calibration only because DLL outputs are close to their optimal values during fine calibration. 0 = Disable use of cross-coupled inverters on DLL output drivers. 1 = Enable use of cross-coupled inverters on DLL output drivers.
60	RO	Reserved.
61	ROX	CAL_GOOD: (Read only.)When 1, calibration finished successfully. When 0, calibration is on-going or resulted in an error if either CAL_ERROR or CAL_ERROR_FINE is set. **Note:** This is the local copy of CAL_GOOD directly from the DLL calibration logic. Thus, it will alternate between 0 and 1 when fine calibration runs continuously.
62	ROX	CAL_ERROR: (Read only.)When 1, VREG or coarse calibration finished with an error.
63	ROX	CAL_ERROR_FINE: (Read only.)When 1, fine calibration finished with an error.

Register Name	ADR DLL DAC Lower Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_DAC_LOWER_P0_ADR32S1
Address	8000843B0701103F (SCOM)
Description	This register holds the lower bound for DLL calibration logic. **CAUTION:** This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:62	RW	REGS_RXDLL_VREG_DAC_LOWER: This field controls the value of VREG during fine calibration. Bits set to 1 are independent of each other; it is the total number of them that matter. For example, these values have the same effect: b100...00, b001...00, b000...10. VREG and delay line element propagation time are inversely proportional because higher values of VREG mean faster delay elements. Therefore, adding more 1s increases VREG and makes faster delay elements. Recommendation: Change bits in a thermometer-code fashion because that is how the digital calibration logic does it.
63	RO	Constant = 0b0

Register Name	ADR DLL DAC Lower Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_DAC_LOWER_P1_ADR32S1
Address	8000843B0701143F (SCOM)
Description	This register holds the lower bound for DLL calibration logic. **CAUTION:** This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:62	RW	REGS_RXDLL_VREG_DAC_LOWER: This field controls the value of VREG during fine calibration. Bits set to 1 are independent of each other; it is the total number of them that matter. For example, these values have the same effect: b100...00, b001...00, b000...10. VREG and delay line element propagation time are inversely proportional because higher values of VREG mean faster delay elements. Therefore, adding more 1s increases VREG and makes faster delay elements. Recommendation: Change bits in a thermometer-code fashion because that is how the digital calibration logic does it.
63	RO	Constant = 0b0

Register Name	ADR DLL DAC Lower Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_DAC_LOWER_P2_ADR32S1
Address	8000843B0701183F (SCOM)
Description	This register holds the lower bound for DLL calibration logic. **CAUTION:** This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:62	RW	REGS_RXDLL_VREG_DAC_LOWER: This field controls the value of VREG during fine calibration. Bits set to 1 are independent of each other; it is the total number of them that matter. For example, these values have the same effect: b100...00, b001...00, b000...10. VREG and delay line element propagation time are inversely proportional because higher values of VREG mean faster delay elements. Therefore, adding more 1s increases VREG and makes faster delay elements. Recommendation: Change bits in a thermometer-code fashion because that is how the digital calibration logic does it.
63	RO	Constant = 0b0

Register Name	ADR DLL DAC Lower Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_DAC_LOWER_P3_ADR32S1
Address	8000843B07011C3F (SCOM)
Description	This register holds the lower bound for DLL calibration logic. **CAUTION:** This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:62	RW	REGS_RXDLL_VREG_DAC_LOWER: This field controls the value of VREG during fine calibration. Bits set to 1 are independent of each other; it is the total number of them that matter. For example, these values have the same effect: b100...00, b001...00, b000...10. VREG and delay line element propagation time are inversely proportional because higher values of VREG mean faster delay elements. Therefore, adding more 1s increases VREG and makes faster delay elements. Recommendation: Change bits in a thermometer-code fashion because that is how the digital calibration logic does it.
63	RO	Constant = 0b0

Register Name	ADR DLL DAC Upper Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_DAC_UPPER_P0_ADR32S1
Address	8000843C0701103F (SCOM)
Description	This register holds the upper bound for DLL calibration logic. **CAUTION:** This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:62	RW	REGS_RXDLL_VREG_DAC_UPPER: Same behavior as REGS_RXDLL_VREG_DAC_LOWER, except the effect on VREG and delay is 16 times larger for each bit.
63	RO	Constant = 0b0

Register Name	ADR DLL DAC Upper Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_DAC_UPPER_P1_ADR32S1
Address	8000843C0701143F (SCOM)
Description	This register holds the upper bound for DLL calibration logic. **CAUTION:** This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:62	RW	REGS_RXDLL_VREG_DAC_UPPER: Same behavior as REGS_RXDLL_VREG_DAC_LOWER, except the effect on VREG and delay is 16 times larger for each bit.
63	RO	Constant = 0b0

Register Name	**ADR DLL DAC Upper Register**
Mnemonic	IOM0.DDRPHY_ADR_DLL_DAC_UPPER_P2_ADR32S1
Address	8000843C0701183F (SCOM)
Description	This register holds the upper bound for DLL calibration logic. **CAUTION:** This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:62	RW	REGS_RXDLL_VREG_DAC_UPPER: Same behavior as REGS_RXDLL_VREG_DAC_LOWER, except the effect on VREG and delay is 16 times larger for each bit.
63	RO	Constant = 0b0

Register Name	**ADR DLL DAC Upper Register**
Mnemonic	IOM0.DDRPHY_ADR_DLL_DAC_UPPER_P3_ADR32S1
Address	8000843C07011C3F (SCOM)
Description	This register holds the upper bound for DLL calibration logic. **CAUTION:** This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:62	RW	REGS_RXDLL_VREG_DAC_UPPER: Same behavior as REGS_RXDLL_VREG_DAC_LOWER, except the effect on VREG and delay is 16 times larger for each bit.
63	RO	Constant = 0b0

Register Name	**ADR DLL VREG Control Register**
Mnemonic	IOM0.DDRPHY_ADR_DLL_VREG_CONTROL_P0_ADR32S1
Address	8000843D0701103F (SCOM)
Description	This register controls the voltage regulator of the DLL calibration logic. **CAUTION:** This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:50	RW	RXREG_VREG_COMPCON_DC: This bit affects the compensation capacitor for the regulator. Contact your IBM representative for details.
51	RW	Reserved.
52	RW	RXREG_VREG_DAC_PULLUP_DC: This bit is a mode switch for the regulator. It is normally not changed.

Bits	SCOM	Field Mnemonic: Description
53:55	RW	RXREG_VREG_DRVCON_DC: This field determines the PFET size for the regulator. It is a mode switch that is normally not changed.
56:58	RW	RXREG_VREG_REF_SEL_DC: This field adjusts the target value of VREG for VREG calibration. The lowest value (0b000) corresponds to the highest VREG target. The highest value (0b111) corresponds to the lowest VREG target. The recommended value is 0b011.
59	RW	REGS_RXDLL_COARSE_ADJ_BY0: Typically, the transition from coarse to fine calibration decrements the code by 1. Therefore, fine calibration always tries to increase the delay by lowering VREG. Sometimes, however, the typical calibration routine produces a less ideal setting. When set, this bit does not decrement the code. Therefore, fine calibration tries to decrease the delay by increasing VREG. 0 = This bit has no effect. 1 = Do not decrement the coarse code during the transition from coarse to fine calibration. **Note:** This bit takes priority over REGS_RXDLL_COARSE_ADJ_BY2 if both are set. Contact your IBM representative for details.
60:62	RO	Constant = 0b000
63	RW	DLL_CAL_CKTS_ACTIVE: This bit is a mode switch to force DLL calibration analog circuits to always be powered on. 0 = After VREG calibration, some analog circuits are powered down. 1 = Override automatic power down, keeping analog calibration circuits active.

Register Name	**ADR DLL VREG Control Register**
Mnemonic	IOM0.DDRPHY_ADR_DLL_VREG_CONTROL_P1_ADR32S1
Address	8000843D0701143F (SCOM)
Description	This register controls the voltage regulator of the DLL calibration logic. **CAUTION:** This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48:50	RW	RXREG_VREG_COMPCON_DC: This bit affects the compensation capacitor for the regulator. Contact your IBM representative for details.
51	RW	Reserved.
52	RW	RXREG_VREG_DAC_PULLUP_DC: This bit is a mode switch for the regulator. It is normally not changed.
53:55	RW	RXREG_VREG_DRVCON_DC: This field determines the PFET size for the regulator. It is a mode switch that is normally not changed.
56:58	RW	RXREG_VREG_REF_SEL_DC: This field adjusts the target value of VREG for VREG calibration. The lowest value (0b000) corresponds to the highest VREG target. The highest value (0b111) corresponds to the lowest VREG target. The recommended value is 0b011.
59	RW	REGS_RXDLL_COARSE_ADJ_BY0: Typically, the transition from coarse to fine calibration decrements the code by 1. Therefore, fine calibration always tries to increase the delay by lowering VREG. Sometimes, however, the typical calibration routine produces a less ideal setting. When set, this bit does not decrement the code. Therefore, fine calibration tries to decrease the delay by increasing VREG. 0 = This bit has no effect. 1 = Do not decrement the coarse code during the transition from coarse to fine calibration. **Note:** This bit takes priority over REGS_RXDLL_COARSE_ADJ_BY2 if both are set. Contact your IBM representative for details.
60:62	RO	Constant = 0b000
63	RW	DLL_CAL_CKTS_ACTIVE: This bit is a mode switch to force DLL calibration analog circuits to always be powered on. 0 = After VREG calibration, some analog circuits are powered down. 1 = Override automatic power down, keeping analog calibration circuits active.

Register Name	ADR DLL VREG Control Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_VREG_CONTROL_P2_ADR32S1
Address	8000843D0701183F (SCOM)
Description	This register controls the voltage regulator of the DLL calibration logic. **CAUTION:** This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:50	RW	RXREG_VREG_COMPCON_DC: This bit affects the compensation capacitor for the regulator. Contact your IBM representative for details.
51	RW	Reserved.
52	RW	RXREG_VREG_DAC_PULLUP_DC: This bit is a mode switch for the regulator. It is normally not changed.
53:55	RW	RXREG_VREG_DRVCON_DC: This field determines the PFET size for the regulator. It is a mode switch that is normally not changed.
56:58	RW	RXREG_VREG_REF_SEL_DC: This field adjusts the target value of VREG for VREG calibration. The lowest value (0b000) corresponds to the highest VREG target. The highest value (0b111) corresponds to the lowest VREG target. The recommended value is 0b011.
59	RW	REGS_RXDLL_COARSE_ADJ_BY0: Typically, the transition from coarse to fine calibration decrements the code by 1. Therefore, fine calibration always tries to increase the delay by lowering VREG. Sometimes, however, the typical calibration routine produces a less ideal setting. When set, this bit does not decrement the code. Therefore, fine calibration tries to decrease the delay by increasing VREG. 0 = This bit has no effect. 1 = Do not decrement the coarse code during the transition from coarse to fine calibration. **Note:** This bit takes priority over REGS_RXDLL_COARSE_ADJ_BY2 if both are set. Contact your IBM representative for details.
60:62	RO	Constant = 0b000
63	RW	DLL_CAL_CKTS_ACTIVE: This bit is a mode switch to force DLL calibration analog circuits to always be powered on. 0 = After VREG calibration, some analog circuits are powered down. 1 = Override automatic power down, keeping analog calibration circuits active.

Register Name	ADR DLL VREG Control Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_VREG_CONTROL_P3_ADR32S1
Address	8000843D07011C3F (SCOM)
Description	This register controls the voltage regulator of the DLL calibration logic. **CAUTION:** This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:50	RW	RXREG_VREG_COMPCON_DC: This bit affects the compensation capacitor for the regulator. Contact your IBM representative for details.
51	RW	Reserved.
52	RW	RXREG_VREG_DAC_PULLUP_DC: This bit is a mode switch for the regulator. It is normally not changed.
53:55	RW	RXREG_VREG_DRVCON_DC: This field determines the PFET size for the regulator. It is a mode switch that is normally not changed.

Bits	SCOM	Field Mnemonic: Description
56:58	RW	RXREG_VREG_REF_SEL_DC: This field adjusts the target value of VREG for VREG calibration. The lowest value (0b000) corresponds to the highest VREG target. The highest value (0b111) corresponds to the lowest VREG target. The recommended value is 0b011.
59	RW	REGS_RXDLL_COARSE_ADJ_BY0: Typically, the transition from coarse to fine calibration decrements the code by 1. Therefore, fine calibration always tries to increase the delay by lowering VREG. Sometimes, however, the typical calibration routine produces a less ideal setting. When set, this bit does not decrement the code. Therefore, fine calibration tries to decrease the delay by increasing VREG. 0 = This bit has no effect. 1 = Do not decrement the coarse code during the transition from coarse to fine calibration. **Note:** This bit takes priority over REGS_RXDLL_COARSE_ADJ_BY2 if both are set. Contact your IBM representative for details.
60:62	RO	Constant = 0b000
63	RW	DLL_CAL_CKTS_ACTIVE: This bit is a mode switch to force DLL calibration analog circuits to always be powered on. 0 = After VREG calibration, some analog circuits are powered down. 1 = Override automatic power down, keeping analog calibration circuits active.

Register Name	ADR DLL VREG Coarse Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_VREG_COARSE_P0_ADR32S1
Address	8000843E0701103F (SCOM)
Description	This register controls the coarse calibration of DLL calibration logic. **CAUTION:** This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:53	RW	REGS_RXDLL_COARSE_EN: This field adjusts the delay of each element in the delay line. The larger the code, the larger the delay. Usually, software reads this register at the end of coarse calibration to see where the setting ended up. However, under special situations (that is, lab testing), it can be written to force a specific delay. **Note:** The POWER9 version of analog DLL only uses 5 bits (0:4). Thus, only the lowest 5 bits of this register (1:5) are connected. Bit 0 exists in the digital logic, but is left unconnected at the digital/analog boundary.
54:55	RO	Constant = 0b00
56:62	RW	REGS_RXDLL_VREG_DAC_COARSE: This field adjusts the value of VREG during VREG calibration. The smallest code (0b0000000) produces the highest VREG voltage; the largest code (0b1111111) produces the lowest VREG voltage. Usually, software reads this register at the end of VREG calibration to see where the setting ended up. However, under special situations (that is, lab testing), it can be written to force a VREG value.
63	RO	Constant = 0b0

Register Name	ADR DLL VREG Coarse Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_VREG_COARSE_P1_ADR32S1
Address	8000843E0701143F (SCOM)
Description	This register controls the coarse calibration of DLL calibration logic. **CAUTION:** This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RW	REGS_RXDLL_COARSE_EN: This field adjusts the delay of each element in the delay line. The larger the code, the larger the delay. Usually, software reads this register at the end of coarse calibration to see where the setting ended up. However, under special situations (that is, lab testing), it can be written to force a specific delay. **Note:** The POWER9 version of analog DLL only uses 5 bits (0:4). Thus, only the lowest 5 bits of this register (1:5) are connected. Bit 0 exists in the digital logic, but is left unconnected at the digital/analog boundary.
54:55	RO	Constant = 0b00
56:62	RW	REGS_RXDLL_VREG_DAC_COARSE: This field adjusts the value of VREG during VREG calibration. The smallest code (0b0000000) produces the highest VREG voltage; the largest code (0b1111111) produces the lowest VREG voltage. Usually, software reads this register at the end of VREG calibration to see where the setting ended up. However, under special situations (that is, lab testing), it can be written to force a VREG value.
63	RO	Constant = 0b0

Register Name	ADR DLL VREG Coarse Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_VREG_COARSE_P2_ADR32S1
Address	8000843E0701183F (SCOM)
Description	This register controls the coarse calibration of DLL calibration logic. **CAUTION:** This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:53	RW	REGS_RXDLL_COARSE_EN: This field adjusts the delay of each element in the delay line. The larger the code, the larger the delay. Usually, software reads this register at the end of coarse calibration to see where the setting ended up. However, under special situations (that is, lab testing), it can be written to force a specific delay. **Note:** The POWER9 version of analog DLL only uses 5 bits (0:4). Thus, only the lowest 5 bits of this register (1:5) are connected. Bit 0 exists in the digital logic, but is left unconnected at the digital/analog boundary.
54:55	RO	Constant = 0b00
56:62	RW	REGS_RXDLL_VREG_DAC_COARSE: This field adjusts the value of VREG during VREG calibration. The smallest code (0b0000000) produces the highest VREG voltage; the largest code (0b1111111) produces the lowest VREG voltage. Usually, software reads this register at the end of VREG calibration to see where the setting ended up. However, under special situations (that is, lab testing), it can be written to force a VREG value.
63	RO	Constant = 0b0

Register Name	ADR DLL VREG Coarse Register
Mnemonic	IOM0.DDRPHY_ADR_DLL_VREG_COARSE_P3_ADR32S1
Address	8000843E07011C3F (SCOM)
Description	This register controls the coarse calibration of DLL calibration logic. **CAUTION:** This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:53	RW	REGS_RXDLL_COARSE_EN: This field adjusts the delay of each element in the delay line. The larger the code, the larger the delay. Usually, software reads this register at the end of coarse calibration to see where the setting ended up. However, under special situations (that is, lab testing), it can be written to force a specific delay. **Note:** The POWER9 version of analog DLL only uses 5 bits (0:4). Thus, only the lowest 5 bits of this register (1:5) are connected. Bit 0 exists in the digital logic, but is left unconnected at the digital/analog boundary.
54:55	RO	Constant = 0b00
56:62	RW	REGS_RXDLL_VREG_DAC_COARSE: This field adjusts the value of VREG during VREG calibration. The smallest code (0b0000000) produces the highest VREG voltage; the largest code (0b1111111) produces the lowest VREG voltage. Usually, software reads this register at the end of VREG calibration to see where the setting ended up. However, under special situations (that is, lab testing), it can be written to force a VREG value.
63	RO	Constant = 0b0

6. DDRPHY: APB Registers

The registers in this section are contained in the advanced peripheral bus (APB) interface control logic. The APB registers are listed alphabetically by mnemonic in the following address table.

Mnemonic	Address	Page
IOM0.DDRPHY_APB_ATEST_MUX_SEL_P0	0x8000D0050701103F	724
IOM0.DDRPHY_APB_ATEST_MUX_SEL_P1	0x8000D0050701143F	725
IOM0.DDRPHY_APB_ATEST_MUX_SEL_P2	0x8000D0050701183F	726
IOM0.DDRPHY_APB_ATEST_MUX_SEL_P3	0x8000D00507011C3F	726
IOM0.DDRPHY_APB_CONFIG0_P0	0x8000D0000701103F	715
IOM0.DDRPHY_APB_CONFIG0_P1	0x8000D0000701143F	716
IOM0.DDRPHY_APB_CONFIG0_P2	0x8000D0000701183F	716
IOM0.DDRPHY_APB_CONFIG0_P3	0x8000D00007011C3F	717
IOM0.DDRPHY_APB_ERROR_MASK0_P0	0x8000D0020701103F	719
IOM0.DDRPHY_APB_ERROR_MASK0_P1	0x8000D0020701143F	720
IOM0.DDRPHY_APB_ERROR_MASK0_P2	0x8000D0020701183F	720
IOM0.DDRPHY_APB_ERROR_MASK0_P3	0x8000D00207011C3F	720
IOM0.DDRPHY_APB_ERROR_STATUS0_P0	0x8000D0010701103F	718
IOM0.DDRPHY_APB_ERROR_STATUS0_P1	0x8000D0010701143F	719
IOM0.DDRPHY_APB_ERROR_STATUS0_P2	0x8000D0010701183F	719
IOM0.DDRPHY_APB_ERROR_STATUS0_P3	0x8000D00107011C3F	719
IOM0.DDRPHY_APB_FIR_ERR0_P0	0x8000D0060701103F	727
IOM0.DDRPHY_APB_FIR_ERR0_P1	0x8000D0060701143F	728
IOM0.DDRPHY_APB_FIR_ERR0_P2	0x8000D0060701183F	728
IOM0.DDRPHY_APB_FIR_ERR0_P3	0x8000D00607011C3F	729
IOM0.DDRPHY_APB_FIR_ERR1_P0	0x8000D0070701103F	729
IOM0.DDRPHY_APB_FIR_ERR1_P1	0x8000D0070701143F	730
IOM0.DDRPHY_APB_FIR_ERR1_P2	0x8000D0070701183F	730
IOM0.DDRPHY_APB_FIR_ERR1_P3	0x8000D00707011C3F	731
IOM0.DDRPHY_APB_FIR_ERR2_P0	0x8000D0030701103F	721
IOM0.DDRPHY_APB_FIR_ERR2_P1	0x8000D0030701143F	721
IOM0.DDRPHY_APB_FIR_ERR2_P2	0x8000D0030701183F	722
IOM0.DDRPHY_APB_FIR_ERR2_P3	0x8000D00307011C3F	722
IOM0.DDRPHY_APB_FIR_ERR3_P0	0x8000D0040701103F	722
IOM0.DDRPHY_APB_FIR_ERR3_P1	0x8000D0040701143F	723
IOM0.DDRPHY_APB_FIR_ERR3_P2	0x8000D0040701183F	723
IOM0.DDRPHY_APB_FIR_ERR3_P3	0x8000D00407011C3F	724
IOM0.DDRPHY_APB_LO_PROBE_SEL_P0	0x8000D0080701103F	731
IOM0.DDRPHY_APB_LO_PROBE_SEL_P1	0x8000D0080701143F	732
IOM0.DDRPHY_APB_LO_PROBE_SEL_P2	0x8000D0080701183F	732
IOM0.DDRPHY_APB_LO_PROBE_SEL_P3	0x8000D00807011C3F	733

The APB registers are listed in the following tables.

Register Name	APB Configuration 0 Register
Mnemonic	IOM0.DDRPHY_APB_CONFIG0_P0
Address	8000D0000701103F (SCOM)
Description	This register contains global configuration information to control the APB control logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	RW	DISABLE_PARITY_CHECKER: If the core was not configured for parity (APB_PARITY = false), this bit is reserved. If the PHY was configured for parity (APB_PARITY = true), this bit disables the parity checker on the write data. This allows write data with bad parity to be written into the registers, and the PSLVERRO is not asserted due to bad write data parity.
49	RW	RESET_ERR_RPT: Write this bit to 1b, and then write this bit to 0b (toggle) to reset the registers defined in the APB FIR Error 0 and APB FIR Error 1 registers.
50	RW	FORCE_ON_CLK_GATE: When set to 1b, the clock gate in the APB control logic block is forced active to permit all clocks to be free running. This bit also forces the clock gate signal that is generated by the APB control logic block to go to other logic blocks when the PHY is active.
51:55	RW	DEBUG_BUS_SEL: Bit 51 selects between "PHY NORTH" (= 0) and "PHY SOUTH" (= 1). Bits 52:55 enable or disable the high-speed probes, and select which DP16 or ADR43 core is driving the probes. **Note:** This register also controls debug bus selection.
56	RW	ADR_SLAVE_SEL: Chooses whether to use the master or slave probes if ADR43 is selected with bits 52:55. 0 = Master. 1 = Slave. Defaults to master.
57:60	RW	DEBUG_BUS_SEL2: Select the source for bits 45:87 of the debug bus. Like DEBUG_SUB_SEL bits 52:55, but these bits select the source for a second DP16 instance to be gated onto the trace bus. When set to b1111, it has a special meaning. It puts the ninth group of data, out of eleven groups, onto the trace bus instead of the second DP16 instance.
61	RW	LOW_PROBE_TRACE_GATE: Acts as a gate between the low-speed probes and the trace trigger. To trigger the trace array, the low-speed probes are routed through this gate. If the low-speed probes are configured as desired, setting this bit to 1 enables the low-speed signals to act as a trigger for the trace array. In port 0, this bit gates the low-speed probes from 0 and 1. In port 2, it gates the low-speed probes from port 2 and 3. In port 1 and 3, this bit has no effect. To have an effect, the port feeding the trace array and this trigger must match. That is, If port 1 is feeding the trace array, this bit in port 0 must be set because it covers ports 0 and 1.
62	RW	HS_PROBE_TOP_SEL: Selects the source of the high-speed probe among ports 0/1 and ports 2/3. DEBUG_BUS_SEL(0) in this register selects between the PHY NORTH and PHY SOUTH of each pair. This bit selects between those two outputs. 0 selects port 0 or 1, whichever is selected by DEBUG_BUS_SEL(0). 1 selects port 2 or 3, whichever is selected by DEBUG_BUS_SEL(0).
63	RW	Reserved.

Register Name	APB Configuration 0 Register
Mnemonic	IOM0.DDRPHY_APB_CONFIG0_P1
Address	8000D0000701143F (SCOM)
Description	This register contains global configuration information to control the APB control logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	DISABLE_PARITY_CHECKER: If the core was not configured for parity (APB_PARITY = false), this bit is reserved. If the PHY was configured for parity (APB_PARITY = true), this bit disables the parity checker on the write data. This allows write data with bad parity to be written into the registers, and the PSLVERRO is not asserted due to bad write data parity.
49	RW	RESET_ERR_RPT: Write this bit to 1b, and then write this bit to 0b (toggle) to reset the registers defined in the APB FIR Error 0 and APB FIR Error 1 registers.
50	RW	FORCE_ON_CLK_GATE: When set to 1b, the clock gate in the APB control logic block is forced active to permit all clocks to be free running. This bit also forces the clock gate signal that is generated by the APB control logic block to go to other logic blocks when the PHY is active.
51:55	RW	DEBUG_BUS_SEL: Bit 51 selects between "PHY NORTH" (= 0) and "PHY SOUTH" (= 1). Bits 52:55 enable or disable the high-speed probes, and select which DP16 or ADR43 core is driving the probes. **Note:** This register also controls debug bus selection.
56	RW	ADR_SLAVE_SEL: Chooses whether to use the master or slave probes if ADR43 is selected with bits 52:55. 0 = Master. 1 = Slave. Defaults to master.
57:60	RW	DEBUG_BUS_SEL2: Select the source for bits 45:87 of the debug bus. Like DEBUG_SUB_SEL bits 52:55, but these bits select the source for a second DP16 instance to be gated onto the trace bus. When set to b1111, it has a special meaning. It puts the ninth group of data, out of eleven groups, onto the trace bus instead of the second DP16 instance.
61	RW	LOW_PROBE_TRACE_GATE: Acts as a gate between the low-speed probes and the trace trigger. To trigger the trace array, the low-speed probes are routed through this gate. If the low-speed probes are configured as desired, setting this bit to 1 enables the low-speed signals to act as a trigger for the trace array. In port 0, this bit gates the low-speed probes from 0 and 1. In port 2, it gates the low-speed probes from port 2 and 3. In port 1 and 3, this bit has no effect. To have an effect, the port feeding the trace array and this trigger must match. That is, If port 1 is feeding the trace array, this bit in port 0 must be set because it covers ports 0 and 1.
62	RW	HS_PROBE_TOP_SEL: Selects the source of the high-speed probe among ports 0/1 and ports 2/3. DEBUG_BUS_SEL(0) in this register selects between the PHY NORTH and PHY SOUTH of each pair. This bit selects between those two outputs. 0 selects port 0 or 1, whichever is selected by DEBUG_BUS_SEL(0). 1 selects port 2 or 3, whichever is selected by DEBUG_BUS_SEL(0).
63	RW	Reserved.

Register Name	APB Configuration 0 Register
Mnemonic	IOM0.DDRPHY_APB_CONFIG0_P2
Address	8000D0000701183F (SCOM)
Description	This register contains global configuration information to control the APB control logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	DISABLE_PARITY_CHECKER: If the core was not configured for parity (APB_PARITY = false), this bit is reserved. If the PHY was configured for parity (APB_PARITY = true), this bit disables the parity checker on the write data. This allows write data with bad parity to be written into the registers, and the PSLVERRO is not asserted due to bad write data parity.
49	RW	RESET_ERR_RPT: Write this bit to 1b, and then write this bit to 0b (toggle) to reset the registers defined in the APB FIR Error 0 and APB FIR Error 1 registers.
50	RW	FORCE_ON_CLK_GATE: When set to 1b, the clock gate in the APB control logic block is forced active to permit all clocks to be free running. This bit also forces the clock gate signal that is generated by the APB control logic block to go to other logic blocks when the PHY is active.
51:55	RW	DEBUG_BUS_SEL: Bit 51 selects between "PHY NORTH" (= 0) and "PHY SOUTH" (= 1). Bits 52:55 enable or disable the high-speed probes, and select which DP16 or ADR43 core is driving the probes. **Note:** This register also controls debug bus selection.
56	RW	ADR_SLAVE_SEL: Chooses whether to use the master or slave probes if ADR43 is selected with bits 52:55. 0 = Master. 1 = Slave. Defaults to master.
57:60	RW	DEBUG_BUS_SEL2: Select the source for bits 45:87 of the debug bus. Like DEBUG_SUB_SEL bits 52:55, but these bits select the source for a second DP16 instance to be gated onto the trace bus. When set to b1111, it has a special meaning. It puts the ninth group of data, out of eleven groups, onto the trace bus instead of the second DP16 instance.
61	RW	LOW_PROBE_TRACE_GATE: Acts as a gate between the low-speed probes and the trace trigger. To trigger the trace array, the low-speed probes are routed through this gate. If the low-speed probes are configured as desired, setting this bit to 1 enables the low-speed signals to act as a trigger for the trace array. In port 0, this bit gates the low-speed probes from 0 and 1. In port 2, it gates the low-speed probes from port 2 and 3. In port 1 and 3, this bit has no effect. To have an effect, the port feeding the trace array and this trigger must match. That is, If port 1 is feeding the trace array, this bit in port 0 must be set because it covers ports 0 and 1.
62	RW	HS_PROBE_TOP_SEL: Selects the source of the high-speed probe among ports 0/1 and ports 2/3. DEBUG_BUS_SEL(0) in this register selects between the PHY NORTH and PHY SOUTH of each pair. This bit selects between those two outputs. 0 selects port 0 or 1, whichever is selected by DEBUG_BUS_SEL(0). 1 selects port 2 or 3, whichever is selected by DEBUG_BUS_SEL(0).
63	RW	Reserved.

Register Name	**APB Configuration 0 Register**
Mnemonic	IOM0.DDRPHY_APB_CONFIG0_P3
Address	8000D00007011C3F (SCOM)
Description	This register contains global configuration information to control the APB control logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	DISABLE_PARITY_CHECKER: If the core was not configured for parity (APB_PARITY = false), this bit is reserved. If the PHY was configured for parity (APB_PARITY = true), this bit disables the parity checker on the write data. This allows write data with bad parity to be written into the registers, and the PSLVERRO is not asserted due to bad write data parity.

Bits	SCOM	Field Mnemonic: Description
49	RW	RESET_ERR_RPT: Write this bit to 1b, and then write this bit to 0b (toggle) to reset the registers defined in the APB FIR Error 0 and APB FIR Error 1 registers.
50	RW	FORCE_ON_CLK_GATE: When set to 1b, the clock gate in the APB control logic block is forced active to permit all clocks to be free running. This bit also forces the clock gate signal that is generated by the APB control logic block to go to other logic blocks when the PHY is active.
51:55	RW	DEBUG_BUS_SEL: Bit 51 selects between "PHY NORTH" (= 0) and "PHY SOUTH" (= 1). Bits 52:55 enable or disable the high-speed probes, and select which DP16 or ADR43 core is driving the probes. **Note:** This register also controls debug bus selection.
56	RW	ADR_SLAVE_SEL: Chooses whether to use the master or slave probes if ADR43 is selected with bits 52:55. 0 = Master. 1 = Slave. Defaults to master.
57:60	RW	DEBUG_BUS_SEL2: Select the source for bits 45:87 of the debug bus. Like DEBUG_SUB_SEL bits 52:55, but these bits select the source for a second DP16 instance to be gated onto the trace bus. When set to b1111, it has a special meaning. It puts the ninth group of data, out of eleven groups, onto the trace bus instead of the second DP16 instance.
61	RW	LOW_PROBE_TRACE_GATE: Acts as a gate between the low-speed probes and the trace trigger. To trigger the trace array, the low-speed probes are routed through this gate. If the low-speed probes are configured as desired, setting this bit to 1 enables the low-speed signals to act as a trigger for the trace array. In port 0, this bit gates the low-speed probes from 0 and 1. In port 2, it gates the low-speed probes from port 2 and 3. In port 1 and 3, this bit has no effect. To have an effect, the port feeding the trace array and this trigger must match. That is, If port 1 is feeding the trace array, this bit in port 0 must be set because it covers ports 0 and 1.
62	RW	HS_PROBE_TOP_SEL: Selects the source of the high-speed probe among ports 0/1 and ports 2/3. DEBUG_BUS_SEL(0) in this register selects between the PHY NORTH and PHY SOUTH of each pair. This bit selects between those two outputs. 0 selects port 0 or 1, whichever is selected by DEBUG_BUS_SEL(0). 1 selects port 2 or 3, whichever is selected by DEBUG_BUS_SEL(0).
63	RW	Reserved.

Register Name	APB Error Status 0 Register
Mnemonic	IOM0.DDRPHY_APB_ERROR_STATUS0_P0
Address	8000D0010701103F (SCOM)
Description	This register contains error and status information about the APB control logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RWX	INVALID_ADDRESS: 1b = Register read or write to an invalid, undefined, or unused address.
49	RWX	WR_PAR_ERR: 1b = Write data during a write operation on the APB interface did not have odd parity (parity error).
50:63	RO	Constant = 0b00000000000000

Register Name	APB Error Status 0 Register
Mnemonic	IOM0.DDRPHY_APB_ERROR_STATUS0_P1
Address	8000D0010701143F (SCOM)
Description	This register contains error and status information about the APB control logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RWX	INVALID_ADDRESS: 1b = Register read or write to an invalid, undefined, or unused address.
49	RWX	WR_PAR_ERR: 1b = Write data during a write operation on the APB interface did not have odd parity (parity error).
50:63	RO	Constant = 0b00000000000000

Register Name	APB Error Status 0 Register
Mnemonic	IOM0.DDRPHY_APB_ERROR_STATUS0_P2
Address	8000D0010701183F (SCOM)
Description	This register contains error and status information about the APB control logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RWX	INVALID_ADDRESS: 1b = Register read or write to an invalid, undefined, or unused address.
49	RWX	WR_PAR_ERR: 1b = Write data during a write operation on the APB interface did not have odd parity (parity error).
50:63	RO	Constant = 0b00000000000000

Register Name	APB Error Status 0 Register
Mnemonic	IOM0.DDRPHY_APB_ERROR_STATUS0_P3
Address	8000D00107011C3F (SCOM)
Description	This register contains error and status information about the APB control logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RWX	INVALID_ADDRESS: 1b = Register read or write to an invalid, undefined, or unused address.
49	RWX	WR_PAR_ERR: 1b = Write data during a write operation on the APB interface did not have odd parity (parity error).
50:63	RO	Constant = 0b00000000000000

Register Name	APB Error Mask 0 Register
Mnemonic	IOM0.DDRPHY_APB_ERROR_MASK0_P0
Address	8000D0020701103F (SCOM)
Description	This register masks errors in the APB Error Status 0 Register and prevents the APB_ERROR bit from being set in the PC Error Status 0 Register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	INVALID_ADDRESS_MASK: 1b = Mask INVALID_ADDRESS error. When an INVALID_ADDRESS error occurs, it is not reported to the higher error reporting registers.
49	RW	WR_PAR_ERR_MASK: 1b = Mask WR_PAR_ERR error. When a WR_PAR_ERR error occurs, it is not reported to a higher error reporting register.
50:63	RO	Constant = 0b00000000000000

Register Name	APB Error Mask 0 Register
Mnemonic	IOM0.DDRPHY_APB_ERROR_MASK0_P1
Address	8000D0020701143F (SCOM)
Description	This register masks errors in the APB Error Status 0 Register and prevents the APB_ERROR bit from being set in the PC Error Status 0 Register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	INVALID_ADDRESS_MASK: 1b = Mask INVALID_ADDRESS error. When an INVALID_ADDRESS error occurs, it is not reported to the higher error reporting registers.
49	RW	WR_PAR_ERR_MASK: 1b = Mask WR_PAR_ERR error. When a WR_PAR_ERR error occurs, it is not reported to a higher error reporting register.
50:63	RO	Constant = 0b00000000000000

Register Name	APB Error Mask 0 Register
Mnemonic	IOM0.DDRPHY_APB_ERROR_MASK0_P2
Address	8000D0020701183F (SCOM)
Description	This register masks errors in the APB Error Status 0 Register and prevents the APB_ERROR bit from being set in the PC Error Status 0 Register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	INVALID_ADDRESS_MASK: 1b = Mask INVALID_ADDRESS error. When an INVALID_ADDRESS error occurs, it is not reported to the higher error reporting registers.
49	RW	WR_PAR_ERR_MASK: 1b = Mask WR_PAR_ERR error. When a WR_PAR_ERR error occurs, it is not reported to a higher error reporting register.
50:63	RO	Constant = 0b00000000000000

Register Name	APB Error Mask 0 Register
Mnemonic	IOM0.DDRPHY_APB_ERROR_MASK0_P3
Address	8000D00207011C3F (SCOM)
Description	This register masks errors in the APB Error Status 0 Register and prevents the APB_ERROR bit from being set in the PC Error Status 0 Register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	INVALID_ADDRESS_MASK: 1b = Mask INVALID_ADDRESS error. When an INVALID_ADDRESS error occurs, it is not reported to the higher error reporting registers.
49	RW	WR_PAR_ERR_MASK: 1b = Mask WR_PAR_ERR error. When a WR_PAR_ERR error occurs, it is not reported to a higher error reporting register.
50:63	RO	Constant = 0b00000000000000

Register Name	APB FIR Error 2 Register
Mnemonic	IOM0.DDRPHY_APB_FIR_ERR2_P0
Address	8000D0030701103F (SCOM)
Description	This register is used to read the state of the c_err_rpt error conditions. The error report, c_err_rpt, is a standard VHDL component instantiated for each error bit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:52	ROX	FIR_ERR0_REG_DP16: Indicates a Level 0 register parity error (affects up to16 DQ bits) in DP16 #0 to #4 logic (respectively). Sets FIR bit 57. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
53:57	ROX	FIR_ERR1_REG_DP16: Indicates a Level 1 register parity error (affects up to 8 DQ bits) in DP16 #0 to #4 logic (respectively). Sets FIR bit 58. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
58:62	ROX	FIR_ERR2_REG_DP16: Indicates a Level 2 register parity error (affects up to 4 DQ bits) in DP16 #0 to #4 logic (respectively). Sets FIR bit 59. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
63	RO	Constant = 0b0

Register Name	APB FIR Error 2 Register
Mnemonic	IOM0.DDRPHY_APB_FIR_ERR2_P1
Address	8000D0030701143F (SCOM)
Description	This register is used to read the state of the c_err_rpt error conditions. The error report, c_err_rpt, is a standard VHDL component instantiated for each error bit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:52	ROX	FIR_ERR0_REG_DP16: Indicates a Level 0 register parity error (affects up to16 DQ bits) in DP16 #0 to #4 logic (respectively). Sets FIR bit 57. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
53:57	ROX	FIR_ERR1_REG_DP16: Indicates a Level 1 register parity error (affects up to 8 DQ bits) in DP16 #0 to #4 logic (respectively). Sets FIR bit 58. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
58:62	ROX	FIR_ERR2_REG_DP16: Indicates a Level 2 register parity error (affects up to 4 DQ bits) in DP16 #0 to #4 logic (respectively). Sets FIR bit 59. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
63	RO	Constant = 0b0

Register Name	APB FIR Error 2 Register
Mnemonic	IOM0.DDRPHY_APB_FIR_ERR2_P2
Address	8000D0030701183F (SCOM)
Description	This register is used to read the state of the c_err_rpt error conditions. The error report, c_err_rpt, is a standard VHDL component instantiated for each error bit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:52	ROX	FIR_ERR0_REG_DP16: Indicates a Level 0 register parity error (affects up to16 DQ bits) in DP16 #0 to #4 logic (respectively). Sets FIR bit 57. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
53:57	ROX	FIR_ERR1_REG_DP16: Indicates a Level 1 register parity error (affects up to 8 DQ bits) in DP16 #0 to #4 logic (respectively). Sets FIR bit 58. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
58:62	ROX	FIR_ERR2_REG_DP16: Indicates a Level 2 register parity error (affects up to 4 DQ bits) in DP16 #0 to #4 logic (respectively). Sets FIR bit 59. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
63	RO	Constant = 0b0

Register Name	APB FIR Error 2 Register
Mnemonic	IOM0.DDRPHY_APB_FIR_ERR2_P3
Address	8000D00307011C3F (SCOM)
Description	This register is used to read the state of the c_err_rpt error conditions. The error report, c_err_rpt, is a standard VHDL component instantiated for each error bit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:52	ROX	FIR_ERR0_REG_DP16: Indicates a Level 0 register parity error (affects up to16 DQ bits) in DP16 #0 to #4 logic (respectively). Sets FIR bit 57. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
53:57	ROX	FIR_ERR1_REG_DP16: Indicates a Level 1 register parity error (affects up to 8 DQ bits) in DP16 #0 to #4 logic (respectively). Sets FIR bit 58. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
58:62	ROX	FIR_ERR2_REG_DP16: Indicates a Level 2 register parity error (affects up to 4 DQ bits) in DP16 #0 to #4 logic (respectively). Sets FIR bit 59. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
63	RO	Constant = 0b0

Register Name	APB FIR Error 3 Register
Mnemonic	IOM0.DDRPHY_APB_FIR_ERR3_P0
Address	8000D0040701103F (SCOM)
Description	This register is used to read the state of the c_err_rpt error conditions. The error report, c_err_rpt, is a standard VHDL component instantiated for each error bit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:52	ROX	FIR_ERR3_REG_DP16: Indicates a Level 3 register parity error (affects 1 DQ bit) in DP16 #0 to #4 logic (respectively). Sets FIR bit 60. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
53:57	ROX	FIR_ERR4_REG_DP16: Indicates a Level 4 register parity error in DP16 #0 to #4 logic (respectively). Sets FIR bit 61. Reset by RESET_ERR_RPT in the APB Configuration 0 Register. (Currently not used.)

Bits	SCOM	Field Mnemonic: Description
58:62	ROX	FIR_ERR5_REG_DP16: Indicates a Level 5 register parity error (registers only used during calibration) in DP16 #0 to #4 logic (respectively). Sets FIR bit 61. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
63	RO	Constant = 0b0

Register Name	APB FIR Error 3 Register
Mnemonic	IOM0.DDRPHY_APB_FIR_ERR3_P1
Address	8000D0040701143F (SCOM)
Description	This register is used to read the state of the c_err_rpt error conditions. The error report, c_err_rpt, is a standard VHDL component instantiated for each error bit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:52	ROX	FIR_ERR3_REG_DP16: Indicates a Level 3 register parity error (affects 1 DQ bit) in DP16 #0 to #4 logic (respectively). Sets FIR bit 60. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
53:57	ROX	FIR_ERR4_REG_DP16: Indicates a Level 4 register parity error in DP16 #0 to #4 logic (respectively). Sets FIR bit 61. Reset by RESET_ERR_RPT in the APB Configuration 0 Register. Currently not used.)
58:62	ROX	FIR_ERR5_REG_DP16: Indicates a Level 5 register parity error (registers only used during calibration) in DP16 #0 to #4 logic (respectively). Sets FIR bit 61. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
63	RO	Constant = 0b0

Register Name	APB FIR Error 3 Register
Mnemonic	IOM0.DDRPHY_APB_FIR_ERR3_P2
Address	8000D0040701183F (SCOM)
Description	This register is used to read the state of the c_err_rpt error conditions. The error report, c_err_rpt, is a standard VHDL component instantiated for each error bit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:52	ROX	FIR_ERR3_REG_DP16: Indicates a Level 3 register parity error (affects 1 DQ bit) in DP16 #0 to #4 logic (respectively). Sets FIR bit 60. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
53:57	ROX	FIR_ERR4_REG_DP16: Indicates a Level 4 register parity error in DP16 #0 to #4 logic (respectively). Sets FIR bit 61. Reset by RESET_ERR_RPT in the APB Configuration 0 Register. Currently not used.)
58:62	ROX	FIR_ERR5_REG_DP16: Indicates a Level 5 register parity error (registers only used during calibration) in DP16 #0 to #4 logic (respectively). Sets FIR bit 61. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
63	RO	Constant = 0b0

Register Name	APB FIR Error 3 Register
Mnemonic	IOM0.DDRPHY_APB_FIR_ERR3_P3
Address	8000D00407011C3F (SCOM)
Description	This register is used to read the state of the c_err_rpt error conditions. The error report, c_err_rpt, is a standard VHDL component instantiated for each error bit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:52	ROX	FIR_ERR3_REG_DP16: Indicates a Level 3 register parity error (affects 1 DQ bit) in DP16 #0 to #4 logic (respectively). Sets FIR bit 60. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
53:57	ROX	FIR_ERR4_REG_DP16: Indicates a Level 4 register parity error in DP16 #0 to #4 logic (respectively). Sets FIR bit 61. Reset by RESET_ERR_RPT in the APB Configuration 0 Register. Currently not used.)
58:62	ROX	FIR_ERR5_REG_DP16: Indicates a Level 5 register parity error (registers only used during calibration) in DP16 #0 to #4 logic (respectively). Sets FIR bit 61. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
63	RO	Constant = 0b0

Register Name	APB ATEST Multiplexer Select Register
Mnemonic	IOM0.DDRPHY_APB_ATEST_MUX_SEL_P0
Address	8000D00507011O3F (SCOM)
Description	This register enables and selects ATEST data from the multiple hard cores within the DDR PHY. This register is reserved for manufacturing test and characterization purposes. It resets to a functional value, and its contents must not be changed by the user.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:52	RW	ATEST_CNTL: Bits 0:1: First level of ATEST selection above macros. There are two outputs per port, multiplexed down in the second level: Upper output: 00 = DP16 #4. 01 = 0. 10 = DP16 #3. 11 = DP16 #2. Lower output: 00 = ADR43 A. 01 = ADR43 B. 10 = DP16 #1. 11 = DP16 #0. Bits 2:3: Second level of ATEST selection; must be programmed in port 0: 00 = Upper output of port 0/1. 01 = Lower output of port 0/1. 10 = Upper Output of port 2/3. 11 = Lower Output of port 2/3. Bit 4: Top level of ATEST selection; must be programmed in port 0: 0 = Port 0/2. 1 = Port 1/3.
53	RW	Reserved.
54	RW	INJECT_FIR_ERR0_4: Inject an error on FIR bit 0 when INJECT_FIR_ERR_SEL = 0 or FIR bit 4 when 1.
55	RW	INJECT_FIR_ERR1_5: Inject an error on FIR bit 1 when INJECT_FIR_ERR_SEL = 0 or FIR bit 5 when 1.

Bits	SCOM	Field Mnemonic: Description
56	RW	INJECT_FIR_ERR2_6: Inject an error on FIR bit 2 when INJECT_FIR_ERR_SEL = 0 or FIR bit 6 when 1.
57	RW	INJECT_FIR_ERR3_7: Inject an error on FIR bit 3 when INJECT_FIR_ERR_SEL = 0 or FIR bit 7 when 1.
58	RW	INJECT_FIR_ERR_SEL: Inject an error on FIR bit 0, 1, 2, or 3 when 0, or FIR bit 4, 5, 6, or 7 when 1.
59:63	RW	Reserved.

Register Name	APB ATEST Multiplexer Select Register
Mnemonic	IOM0.DDRPHY_APB_ATEST_MUX_SEL_P1
Address	8000D0050701143F (SCOM)
Description	This register enables and selects ATEST data from the multiple hard cores within the DDR PHY. This register is reserved for manufacturing test and characterization purposes. It resets to a functional value, and its contents must not be changed by the user.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:52	RW	ATEST_CNTL: Bits 0:1: First level of ATEST selection above macros. There are two outputs per port, multiplexed down in the second level: Upper output: 00 = DP16 #4. 01 = 0. 10 = DP16 #3. 11 = DP16 #2. Lower output: 00 = ADR43 A. 01 = ADR43 B. 10 = DP16 #1. 11 = DP16 #0. Bits 2:3: Second level of ATEST selection; must be programmed in port 0: 00 = Upper output of port 0/1. 01 = Lower output of port 0/1. 10 = Upper Output of port 2/3. 11 = Lower Output of port 2/3. Bit 4: Top level of ATEST selection; must be programmed in port 0: 0 = Port 0/2. 1 = Port 1/3.
53	RW	Reserved.
54	RW	INJECT_FIR_ERR0_4: Inject an error on FIR bit 0 when INJECT_FIR_ERR_SEL = 0 or FIR bit 4 when 1.
55	RW	INJECT_FIR_ERR1_5: Inject an error on FIR bit 1 when INJECT_FIR_ERR_SEL = 0 or FIR bit 5 when 1.
56	RW	INJECT_FIR_ERR2_6: Inject an error on FIR bit 2 when INJECT_FIR_ERR_SEL = 0 or FIR bit 6 when 1.
57	RW	INJECT_FIR_ERR3_7: Inject an error on FIR bit 3 when INJECT_FIR_ERR_SEL = 0 or FIR bit 7 when 1.
58	RW	INJECT_FIR_ERR_SEL: Inject an error on FIR bit 0, 1, 2, or 3 when 0, or FIR bit 4, 5, 6, or 7 when 1.
59:63	RW	Reserved.

Register Name	APB ATEST Multiplexer Select Register
Mnemonic	IOM0.DDRPHY_APB_ATEST_MUX_SEL_P2
Address	8000D0050701183F (SCOM)
Description	This register enables and selects ATEST data from the multiple hard cores within the DDR PHY. This register is reserved for manufacturing test and characterization purposes. It resets to a functional value, and its contents must not be changed by the user.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:52	RW	ATEST_CNTL: Bits 0:1: First level of ATEST selection above macros. There are two outputs per port, multiplexed down in the second level: Upper output: 00 = DP16 #4. 01 = 0. 10 = DP16 #3. 11 = DP16 #2. Lower output: 00 = ADR43 A. 01 = ADR43 B. 10 = DP16 #1. 11 = DP16 #0. Bits 2:3: Second level of ATEST selection; must be programmed in port 0: 00 = Upper output of port 0/1. 01 = Lower output of port 0/1. 10 = Upper Output of port 2/3. 11 = Lower Output of port 2/3. Bit 4: Top level of ATEST selection; must be programmed in port 0: 0 = Port 0/2. 1 = Port 1/3.
53	RW	Reserved.
54	RW	INJECT_FIR_ERR0_4: Inject an error on FIR bit 0 when INJECT_FIR_ERR_SEL = 0 or FIR bit 4 when 1.
55	RW	INJECT_FIR_ERR1_5: Inject an error on FIR bit 1 when INJECT_FIR_ERR_SEL = 0 or FIR bit 5 when 1.
56	RW	INJECT_FIR_ERR2_6: Inject an error on FIR bit 2 when INJECT_FIR_ERR_SEL = 0 or FIR bit 6 when 1.
57	RW	INJECT_FIR_ERR3_7: Inject an error on FIR bit 3 when INJECT_FIR_ERR_SEL = 0 or FIR bit 7 when 1.
58	RW	INJECT_FIR_ERR_SEL: Inject an error on FIR bit 0, 1, 2, or 3 when 0, or FIR bit 4, 5, 6, or 7 when 1.
59:63	RW	Reserved.

Register Name	APB ATEST Multiplexer Select Register
Mnemonic	IOM0.DDRPHY_APB_ATEST_MUX_SEL_P3
Address	8000D00507011C3F (SCOM)
Description	This register enables and selects ATEST data from the multiple hard cores within the DDR PHY. This register is reserved for manufacturing test and characterization purposes. It resets to a functional value, and its contents must not be changed by the user.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:52	RW	ATEST_CNTL: Bits 0:1: First level of ATEST selection above macros. There are two outputs per port, multiplexed down in the second level: Upper output: 00 = DP16 #4. 01 = 0. 10 = DP16 #3. 11 = DP16 #2. Lower output: 00 = ADR43 A. 01 = ADR43 B. 10 = DP16 #1. 11 = DP16 #0. Bits 2:3: Second level of ATEST selection; must be programmed in port 0: 00 = Upper output of port 0/1. 01 = Lower output of port 0/1. 10 = Upper Output of port 2/3. 11 = Lower Output of port 2/3. Bit 4: Top level of ATEST selection; must be programmed in port 0: 0 = Port 0/2. 1 = Port 1/3.
53	RW	Reserved.
54	RW	INJECT_FIR_ERR0_4: Inject an error on FIR bit 0 when INJECT_FIR_ERR_SEL = 0 or FIR bit 4 when 1.
55	RW	INJECT_FIR_ERR1_5: Inject an error on FIR bit 1 when INJECT_FIR_ERR_SEL = 0 or FIR bit 5 when 1.
56	RW	INJECT_FIR_ERR2_6: Inject an error on FIR bit 2 when INJECT_FIR_ERR_SEL = 0 or FIR bit 6 when 1.
57	RW	INJECT_FIR_ERR3_7: Inject an error on FIR bit 3 when INJECT_FIR_ERR_SEL = 0 or FIR bit 7 when 1.
58	RW	INJECT_FIR_ERR_SEL: Inject an error on FIR bit 0, 1, 2, or 3 when 0, or FIR bit 4, 5, 6, or 7 when 1.
59:63	RW	Reserved.

Register Name	**APB FIR Error 0 Register**
Mnemonic	IOM0.DDRPHY_APB_FIR_ERR0_P0
Address	8000D0060701103F (SCOM)
Description	This register is used to read the state of the c_err_rpt error conditions. The error report, c_err_rpt, is a standard VHDL component instantiated for each error bit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	ROX	FIR_ERR_SET0: Indicates a nonrecoverable FSM state checker error in the PHYTOP logic. Sets FIR bit 54. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
49	ROX	FIR_ERR_SET1: Indicates a nonrecoverable register parity error in the PHYTOP logic. Sets FIR bit 55. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
50	ROX	FIR_ERR_SET2: Indicates a recoverable FSM state checker error in the PHYTOP logic. Sets FIR bit 56. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
51	ROX	FIR_ERR_SET3: Indicates a recoverable register parity error in the PHYTOP logic. Sets FIR bit 55. Reset by RESET_ERR_RPT in the APB Configuration 0 Register. **Note:** These errors are now considered nonrecoverable in POWER9.
52	ROX	FIR_ERR_SET4: Indicates a nonrecoverable register parity error in the ADR master-side logic. Sets FIR bit 55. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.

Bits	SCOM	Field Mnemonic: Description
53	ROX	FIR_ERR_SET5: Indicates a nonrecoverable register parity error in the ADR slave-side logic. Sets FIR bit 55. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
54:58	ROX	FIR_ERR_FSM_DP16: Indicates a recoverable FSM state checker error in DP16 #0 to #4 logic (respectively). Sets FIR bit 56. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
59:63	RO	PC_ERR_STATUS0: Indicates that a calibration error was latched in bits 0:2, 4:5 of the PC Error Status 0 Register respectively. Sets FIR bit 61. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.

Register Name	APB FIR Error 0 Register
Mnemonic	IOM0.DDRPHY_APB_FIR_ERR0_P1
Address	8000D0060701143F (SCOM)
Description	This register is used to read the state of the c_err_rpt error conditions. The error report, c_err_rpt, is a standard VHDL component instantiated for each error bit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	ROX	FIR_ERR_SET0: Indicates a nonrecoverable FSM state checker error in the PHYTOP logic. Sets FIR bit 54. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
49	ROX	FIR_ERR_SET1: Indicates a nonrecoverable register parity error in the PHYTOP logic. Sets FIR bit 55. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
50	ROX	FIR_ERR_SET2: Indicates a recoverable FSM state checker error in the PHYTOP logic. Sets FIR bit 56. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
51	ROX	FIR_ERR_SET3: Indicates a recoverable register parity error in the PHYTOP logic. Sets FIR bit 55. Reset by RESET_ERR_RPT in the APB Configuration 0 Register. **Note:** These errors are now considered nonrecoverable in POWER9.
52	ROX	FIR_ERR_SET4: Indicates a nonrecoverable register parity error in the ADR master-side logic. Sets FIR bit 55. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
53	ROX	FIR_ERR_SET5: Indicates a nonrecoverable register parity error in the ADR slave-side logic. Sets FIR bit 55. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
54:58	ROX	FIR_ERR_FSM_DP16: Indicates a recoverable FSM state checker error in DP16 #0 to #4 logic (respectively). Sets FIR bit 56. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
59:63	RO	PC_ERR_STATUS0: Indicates that a calibration error was latched in bits 0:2, 4:5 of the PC Error Status 0 Register respectively. Sets FIR bit 61. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.

Register Name	APB FIR Error 0 Register
Mnemonic	IOM0.DDRPHY_APB_FIR_ERR0_P2
Address	8000D0060701183F (SCOM)
Description	This register is used to read the state of the c_err_rpt error conditions. The error report, c_err_rpt, is a standard VHDL component instantiated for each error bit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	ROX	FIR_ERR_SET0: Indicates a nonrecoverable FSM state checker error in the PHYTOP logic. Sets FIR bit 54. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
49	ROX	FIR_ERR_SET1: Indicates a nonrecoverable register parity error in the PHYTOP logic. Sets FIR bit 55. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.

Bits	SCOM	Field Mnemonic: Description
50	ROX	FIR_ERR_SET2: Indicates a recoverable FSM state checker error in the PHYTOP logic. Sets FIR bit 56. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
51	ROX	FIR_ERR_SET3: Indicates a recoverable register parity error in the PHYTOP logic. Sets FIR bit 55. Reset by RESET_ERR_RPT in the APB Configuration 0 Register. **Note:** These errors are now considered nonrecoverable in POWER9.
52	ROX	FIR_ERR_SET4: Indicates a nonrecoverable register parity error in the ADR master-side logic. Sets FIR bit 55. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
53	ROX	FIR_ERR_SET5: Indicates a nonrecoverable register parity error in the ADR slave-side logic. Sets FIR bit 55. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
54:58	ROX	FIR_ERR_FSM_DP16: Indicates a recoverable FSM state checker error in DP16 #0 to #4 logic (respectively). Sets FIR bit 56. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
59:63	RO	PC_ERR_STATUS0: Indicates that a calibration error was latched in bits 0:2, 4:5 of the PC Error Status 0 Register respectively. Sets FIR bit 61. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.

Register Name	**APB FIR Error 0 Register**
Mnemonic	IOM0.DDRPHY_APB_FIR_ERR0_P3
Address	8000D00607011C3F (SCOM)
Description	This register is used to read the state of the c_err_rpt error conditions. The error report, c_err_rpt, is a standard VHDL component instantiated for each error bit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	ROX	FIR_ERR_SET0: Indicates a nonrecoverable FSM state checker error in the PHYTOP logic. Sets FIR bit 54. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
49	ROX	FIR_ERR_SET1: Indicates a nonrecoverable register parity error in the PHYTOP logic. Sets FIR bit 55. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
50	ROX	FIR_ERR_SET2: Indicates a recoverable FSM state checker error in the PHYTOP logic. Sets FIR bit 56. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
51	ROX	FIR_ERR_SET3: Indicates a recoverable register parity error in the PHYTOP logic. Sets FIR bit 55. Reset by RESET_ERR_RPT in the APB Configuration 0 Register. **Note:** These errors are now considered nonrecoverable in POWER9.
52	ROX	FIR_ERR_SET4: Indicates a nonrecoverable register parity error in the ADR master-side logic. Sets FIR bit 55. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
53	ROX	FIR_ERR_SET5: Indicates a nonrecoverable register parity error in the ADR slave-side logic. Sets FIR bit 55. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
54:58	ROX	FIR_ERR_FSM_DP16: Indicates a recoverable FSM state checker error in DP16 #0 to #4 logic (respectively). Sets FIR bit 56. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
59:63	RO	PC_ERR_STATUS0: Indicates that a calibration error was latched in bits 0:2, 4:5 of the PC Error Status 0 Register respectively. Sets FIR bit 61. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.

Register Name	**APB FIR Error 1 Register**
Mnemonic	IOM0.DDRPHY_APB_FIR_ERR1_P0
Address	8000D0070701103F (SCOM)
Description	This register is used to read the state of the c_err_rpt error conditions. The error report, c_err_rpt, is a standard VHDL component instantiated for each error bit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:59	ROX	PC_INIT_CAL_ERR: Indicates that a calibration error was latched in bits 0:11 of the PC Initial Calibration Error Register respectively. Sets FIR bit 61. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
60	ROX	DP_DLL_CAL_ERROR: This bit comes from the PC DLL/ZCAL Calibration Status Register, bit 1. Sets FIR bits 57 and 61. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
61	ROX	DP_DLL_CAL_ERROR_FINE: This bit comes from the PC DLL/ZCAL Calibration Status Register, bit 2. Sets FIR bits 57 and 61. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
62	ROX	ADR_DLL_CAL_ERROR: This bit comes from the PC DLL/ZCAL Calibration Status Register, bit 4. Sets FIR bits 57 and 61. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
63	ROX	ADR_DLL_CAL_ERROR_FINE: This bit comes from the PC DLL/ZCAL Calibration Status Register, bit 5. Sets FIR bits 57 and 61. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.

Register Name	APB FIR Error 1 Register
Mnemonic	IOM0.DDRPHY_APB_FIR_ERR1_P1
Address	8000D0070701143F (SCOM)
Description	This register is used to read the state of the c_err_rpt error conditions. The error report, c_err_rpt, is a standard VHDL component instantiated for each error bit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:59	ROX	PC_INIT_CAL_ERR: Indicates that a calibration error was latched in bits 0:11 of the PC Initial Calibration Error Register respectively. Sets FIR bit 61. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
60	ROX	DP_DLL_CAL_ERROR: This bit comes from the PC DLL/ZCAL Calibration Status Register, bit 1. Sets FIR bits 57 and 61. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
61	ROX	DP_DLL_CAL_ERROR_FINE: This bit comes from the PC DLL/ZCAL Calibration Status Register, bit 2. Sets FIR bits 57 and 61. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
62	ROX	ADR_DLL_CAL_ERROR: This bit comes from the PC DLL/ZCAL Calibration Status Register, bit 4. Sets FIR bits 57 and 61. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
63	ROX	ADR_DLL_CAL_ERROR_FINE: This bit comes from the PC DLL/ZCAL Calibration Status Register, bit 5. Sets FIR bits 57 and 61. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.

Register Name	APB FIR Error 1 Register
Mnemonic	IOM0.DDRPHY_APB_FIR_ERR1_P2
Address	8000D0070701183F (SCOM)
Description	This register is used to read the state of the c_err_rpt error conditions. The error report, c_err_rpt, is a standard VHDL component instantiated for each error bit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:59	ROX	PC_INIT_CAL_ERR: Indicates that a calibration error was latched in bits 0:11 of the PC Initial Calibration Error Register respectively. Sets FIR bit 61. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
60	ROX	DP_DLL_CAL_ERROR: This bit comes from the PC DLL/ZCAL Calibration Status Register, bit 1. Sets FIR bits 57 and 61. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.

Bits	SCOM	Field Mnemonic: Description
61	ROX	DP_DLL_CAL_ERROR_FINE: This bit comes from the PC DLL/ZCAL Calibration Status Register, bit 2. Sets FIR bits 57 and 61. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
62	ROX	ADR_DLL_CAL_ERROR: This bit comes from the PC DLL/ZCAL Calibration Status Register, bit 4. Sets FIR bits 57 and 61. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
63	ROX	ADR_DLL_CAL_ERROR_FINE: This bit comes from the PC DLL/ZCAL Calibration Status Register, bit 5. Sets FIR bits 57 and 61. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.

Register Name	**APB FIR Error 1 Register**
Mnemonic	IOM0.DDRPHY_APB_FIR_ERR1_P3
Address	8000D00707011C3F (SCOM)
Description	This register is used to read the state of the c_err_rpt error conditions. The error report, c_err_rpt, is a standard VHDL component instantiated for each error bit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:59	ROX	PC_INIT_CAL_ERR: Indicates that a calibration error was latched in bits 0:11 of the PC Initial Calibration Error Register respectively. Sets FIR bit 61. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
60	ROX	DP_DLL_CAL_ERROR: This bit comes from the PC DLL/ZCAL Calibration Status Register, bit 1. Sets FIR bits 57 and 61. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
61	ROX	DP_DLL_CAL_ERROR_FINE: This bit comes from the PC DLL/ZCAL Calibration Status Register, bit 2. Sets FIR bits 57 and 61. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
62	ROX	ADR_DLL_CAL_ERROR: This bit comes from the PC DLL/ZCAL Calibration Status Register, bit 4. Sets FIR bits 57 and 61. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.
63	ROX	ADR_DLL_CAL_ERROR_FINE: This bit comes from the PC DLL/ZCAL Calibration Status Register, bit 5. Sets FIR bits 57 and 61. Reset by RESET_ERR_RPT in the APB Configuration 0 Register.

Register Name	**APB Low-Speed Probe Select Register**
Mnemonic	IOM0.DDRPHY_APB_LO_PROBE_SEL_P0
Address	8000D00807011103F (SCOM)
Description	Select sources of low-speed probing in the APB. Both low-speed probes (0 and 1) can pass the source value through unchanged (pulse mode) or capture a b0 →b1 transition on the input and hold the value at b1 until explicitly reset (hold mode).

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	WO_1P	LO_PROBE_RESET_0: When written to b1, resets the value on low-speed probe 0. If the probe is held high, writing this to b1 resets it to b0 and allows it to be triggered again. Hardware automatically returns this bit to b0 after it is written to b1.
49	RW	LO_PROBE_HOLD_0: In pulse mode, low-speed probe 0 takes the continuous value of the bit being monitored. In hold mode, when low-speed probe 0 finds a rising edge, it holds at the high value until reset by LO_PROBE_RESET_0. b0 = Pulse mode. b1 = Hold mode.
50:55	RW	LO_PROBE_SEL_0: Select source 0 into the low-speed probe tree.

Bits	SCOM	Field Mnemonic: Description
56	WO_1P	LO_PROBE_RESET_1: When written to b1, resets the value on low-speed probe 1. If the probe is held high, writing this to b1 resets it to b0 and allows it to be triggered again. Hardware automatically returns this bit to b0 after it is written to b1.
57	RW	LO_PROBE_HOLD_1: In pulse mode, low-speed probe 1 takes the continuous value of the bit being monitored. In hold mode, when low-speed probe 1 finds a rising edge, it holds at the high value until reset by LO_PROBE_RESET_1. b0 = Pulse mode. b1 = Hold mode.
58:63	RW	LO_PROBE_SEL_1: Select source 1 into the low-speed probe tree.

Register Name	APB Low-Speed Probe Select Register
Mnemonic	IOM0.DDRPHY_APB_LO_PROBE_SEL_P1
Address	8000D0080701143F (SCOM)
Description	Select sources of low-speed probing in the APB. Both low-speed probes (0 and 1) can pass the source value through unchanged (pulse mode) or capture a b0 →b1 transition on the input and hold the value at b1 until explicitly reset (hold mode).

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	WO_1P	LO_PROBE_RESET_0: When written to b1, resets the value on low-speed probe 0. If the probe is held high, writing this to b1 resets it to b0 and allows it to be triggered again. Hardware automatically returns this bit to b0 after it is written to b1.
49	RW	LO_PROBE_HOLD_0: In pulse mode, low-speed probe 0 takes the continuous value of the bit being monitored. In hold mode, when low-speed probe 0 finds a rising edge, it holds at the high value until reset by LO_PROBE_RESET_0. b0 = Pulse mode. b1 = Hold mode.
50:55	RW	LO_PROBE_SEL_0: Select source 0 into the low-speed probe tree.
56	WO_1P	LO_PROBE_RESET_1: When written to b1, resets the value on low-speed probe 1. If the probe is held high, writing this to b1 resets it to b0 and allows it to be triggered again. Hardware automatically returns this bit to b0 after it is written to b1.
57	RW	LO_PROBE_HOLD_1: In pulse mode, low-speed probe 1 takes the continuous value of the bit being monitored. In hold mode, when low-speed probe 1 finds a rising edge, it holds at the high value until reset by LO_PROBE_RESET_1. b0 = Pulse mode. b1 = Hold mode.
58:63	RW	LO_PROBE_SEL_1: Select source 1 into the low-speed probe tree.

Register Name	APB Low-Speed Probe Select Register
Mnemonic	IOM0.DDRPHY_APB_LO_PROBE_SEL_P2
Address	8000D0080701183F (SCOM)
Description	Select sources of low-speed probing in the APB. Both low-speed probes (0 and 1) can pass the source value through unchanged (pulse mode) or capture a b0 →b1 transition on the input and hold the value at b1 until explicitly reset (hold mode).

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	WO_1P	LO_PROBE_RESET_0: When written to b1, resets the value on low-speed probe 0. If the probe is held high, writing this to b1 resets it to b0 and allows it to be triggered again. Hardware automatically returns this bit to b0 after it is written to b1.
49	RW	LO_PROBE_HOLD_0: In pulse mode, low-speed probe 0 takes the continuous value of the bit being monitored. In hold mode, when low-speed probe 0 finds a rising edge, it holds at the high value until reset by LO_PROBE_RESET_0. b0 = Pulse mode. b1 = Hold mode.
50:55	RW	LO_PROBE_SEL_0: Select source 0 into the low-speed probe tree.
56	WO_1P	LO_PROBE_RESET_1: When written to b1, resets the value on low-speed probe 1. If the probe is held high, writing this to b1 resets it to b0 and allows it to be triggered again. Hardware automatically returns this bit to b0 after it is written to b1.
57	RW	LO_PROBE_HOLD_1: In pulse mode, low-speed probe 1 takes the continuous value of the bit being monitored. In hold mode, when low-speed probe 1 finds a rising edge, it holds at the high value until reset by LO_PROBE_RESET_1. b0 = Pulse mode. b1 = Hold mode.
58:63	RW	LO_PROBE_SEL_1: Select source 1 into the low-speed probe tree.

Register Name	**APB Low-Speed Probe Select Register**
Mnemonic	IOM0.DDRPHY_APB_LO_PROBE_SEL_P3
Address	8000D00807011C3F (SCOM)
Description	Select sources of low-speed probing in the APB. Both low-speed probes (0 and 1) can pass the source value through unchanged (pulse mode) or capture a b0 →b1 transition on the input and hold the value at b1 until explicitly reset (hold mode).

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	WO_1P	LO_PROBE_RESET_0: When written to b1, resets the value on low-speed probe 0. If the probe is held high, writing this to b1 resets it to b0 and allows it to be triggered again. Hardware automatically returns this bit to b0 after it is written to b1.
49	RW	LO_PROBE_HOLD_0: In pulse mode, low-speed probe 0 takes the continuous value of the bit being monitored. In hold mode, when low-speed probe 0 finds a rising edge, it holds at the high value until reset by LO_PROBE_RESET_0. b0 = Pulse mode. b1 = Hold mode.
50:55	RW	LO_PROBE_SEL_0: Select source 0 into the low-speed probe tree.
56	WO_1P	LO_PROBE_RESET_1: When written to b1, resets the value on low-speed probe 1. If the probe is held high, writing this to b1 resets it to b0 and allows it to be triggered again. Hardware automatically returns this bit to b0 after it is written to b1.
57	RW	LO_PROBE_HOLD_1: In pulse mode, low-speed probe 1 takes the continuous value of the bit being monitored. In hold mode, when low-speed probe 1 finds a rising edge, it holds at the high value until reset by LO_PROBE_RESET_1. b0 = Pulse mode. b1 = Hold mode.
58:63	RW	LO_PROBE_SEL_1: Select source 1 into the low-speed probe tree.

7. DDRPHY: PC Registers

This section contains the registers that are located in the PHY control (PC) logic. The PC registers are listed alphabetically by mnemonic in the following address table.

Mnemonic	Address	Page
IOM0.DDRPHY_PC_BASE_CNTR0_P0	0x8000C0040701103F	752
IOM0.DDRPHY_PC_BASE_CNTR0_P1	0x8000C0040701143F	753
IOM0.DDRPHY_PC_BASE_CNTR0_P2	0x8000C0040701183F	753
IOM0.DDRPHY_PC_BASE_CNTR0_P3	0x8000C00407011C3F	753
IOM0.DDRPHY_PC_BASE_CNTR1_P0	0x8000C0060701103F	755
IOM0.DDRPHY_PC_BASE_CNTR1_P1	0x8000C0060701143F	756
IOM0.DDRPHY_PC_BASE_CNTR1_P2	0x8000C0060701183F	756
IOM0.DDRPHY_PC_BASE_CNTR1_P3	0x8000C00607011C3F	756
IOM0.DDRPHY_PC_CAL_TIMER_P0	0x8000C0070701103F	757
IOM0.DDRPHY_PC_CAL_TIMER_P1	0x8000C0070701143F	757
IOM0.DDRPHY_PC_CAL_TIMER_P2	0x8000C0070701183F	758
IOM0.DDRPHY_PC_CAL_TIMER_P3	0x8000C00707011C3F	758
IOM0.DDRPHY_PC_CAL_TIMER_RELOAD_VALUE_P0	0x8000C0080701103F	759
IOM0.DDRPHY_PC_CAL_TIMER_RELOAD_VALUE_P1	0x8000C0080701143F	759
IOM0.DDRPHY_PC_CAL_TIMER_RELOAD_VALUE_P2	0x8000C0080701183F	759
IOM0.DDRPHY_PC_CAL_TIMER_RELOAD_VALUE_P3	0x8000C00807011C3F	760
IOM0.DDRPHY_PC_CONFIG0_P0	0x8000C00C0701103F	767
IOM0.DDRPHY_PC_CONFIG0_P1	0x8000C00C0701143F	769
IOM0.DDRPHY_PC_CONFIG0_P2	0x8000C00C0701183F	770
IOM0.DDRPHY_PC_CONFIG0_P3	0x8000C00C07011C3F	771
IOM0.DDRPHY_PC_CONFIG1_P0	0x8000C00D0701103F	773
IOM0.DDRPHY_PC_CONFIG1_P1	0x8000C00D0701143F	774
IOM0.DDRPHY_PC_CONFIG1_P2	0x8000C00D0701183F	775
IOM0.DDRPHY_PC_CONFIG1_P3	0x8000C00D07011C3F	776
IOM0.DDRPHY_PC_CSID_CFG_P0	0x8000C0330701103F	834
IOM0.DDRPHY_PC_CSID_CFG_P1	0x8000C0330701143F	834
IOM0.DDRPHY_PC_CSID_CFG_P2	0x8000C0330701183F	835
IOM0.DDRPHY_PC_CSID_CFG_P3	0x8000C03307011C3F	835
IOM0.DDRPHY_PC_DLL_ZCAL_CAL_STATUS_P0	0x8000C0000701103F	741
IOM0.DDRPHY_PC_DLL_ZCAL_CAL_STATUS_P1	0x8000C0000701143F	742
IOM0.DDRPHY_PC_DLL_ZCAL_CAL_STATUS_P2	0x8000C0000701183F	743
IOM0.DDRPHY_PC_DLL_ZCAL_CAL_STATUS_P3	0x8000C00007011C3F	743
IOM0.DDRPHY_PC_ERROR_MASK0_P0	0x8000C0130701103F	793
IOM0.DDRPHY_PC_ERROR_MASK0_P1	0x8000C0130701143F	794
IOM0.DDRPHY_PC_ERROR_MASK0_P2	0x8000C0130701183F	794
IOM0.DDRPHY_PC_ERROR_MASK0_P3	0x8000C01307011C3F	795
IOM0.DDRPHY_PC_ERROR_STATUS0_P0	0x8000C0120701103F	792
IOM0.DDRPHY_PC_ERROR_STATUS0_P1	0x8000C0120701143F	792

Mnemonic	Address	Page
IOM0.DDRPHY_PC_ERROR_STATUS0_P2	0x8000C0120701183F	793
IOM0.DDRPHY_PC_ERROR_STATUS0_P3	0x8000C01207011C3F	793
IOM0.DDRPHY_PC_INIT_CAL_CONFIG0_P0	0x8000C0160701103F	798
IOM0.DDRPHY_PC_INIT_CAL_CONFIG0_P1	0x8000C0160701143F	799
IOM0.DDRPHY_PC_INIT_CAL_CONFIG0_P2	0x8000C0160701183F	800
IOM0.DDRPHY_PC_INIT_CAL_CONFIG0_P3	0x8000C01607011C3F	801
IOM0.DDRPHY_PC_INIT_CAL_CONFIG1_P0	0x8000C0170701103F	802
IOM0.DDRPHY_PC_INIT_CAL_CONFIG1_P1	0x8000C0170701143F	803
IOM0.DDRPHY_PC_INIT_CAL_CONFIG1_P2	0x8000C0170701183F	804
IOM0.DDRPHY_PC_INIT_CAL_CONFIG1_P3	0x8000C01707011C3F	805
IOM0.DDRPHY_PC_INIT_CAL_ERROR_P0	0x8000C0180701103F	806
IOM0.DDRPHY_PC_INIT_CAL_ERROR_P1	0x8000C0180701143F	807
IOM0.DDRPHY_PC_INIT_CAL_ERROR_P2	0x8000C0180701183F	808
IOM0.DDRPHY_PC_INIT_CAL_ERROR_P3	0x8000C01807011C3F	809
IOM0.DDRPHY_PC_INIT_CAL_MASK_P0	0x8000C01A0701103F	812
IOM0.DDRPHY_PC_INIT_CAL_MASK_P1	0x8000C01A0701143F	812
IOM0.DDRPHY_PC_INIT_CAL_MASK_P2	0x8000C01A0701183F	813
IOM0.DDRPHY_PC_INIT_CAL_MASK_P3	0x8000C01A07011C3F	813
IOM0.DDRPHY_PC_INIT_CAL_STATUS_P0	0x8000C0190701103F	809
IOM0.DDRPHY_PC_INIT_CAL_STATUS_P1	0x8000C0190701143F	810
IOM0.DDRPHY_PC_INIT_CAL_STATUS_P2	0x8000C0190701183F	811
IOM0.DDRPHY_PC_INIT_CAL_STATUS_P3	0x8000C01907011C3F	811
IOM0.DDRPHY_PC_IO_PVT_FET_CONTROL_P0	0x8000C0140701103F	795
IOM0.DDRPHY_PC_IO_PVT_FET_CONTROL_P1	0x8000C0140701143F	795
IOM0.DDRPHY_PC_IO_PVT_FET_CONTROL_P2	0x8000C0140701183F	796
IOM0.DDRPHY_PC_IO_PVT_FET_CONTROL_P3	0x8000C01407011C3F	796
IOM0.DDRPHY_PC_IO_PVT_FET_STATUS_P0	0x8000C01B0701103F	814
IOM0.DDRPHY_PC_IO_PVT_FET_STATUS_P1	0x8000C01B0701143F	814
IOM0.DDRPHY_PC_IO_PVT_FET_STATUS_P2	0x8000C01B0701183F	815
IOM0.DDRPHY_PC_IO_PVT_FET_STATUS_P3	0x8000C01B07011C3F	815
IOM0.DDRPHY_PC_MIRROR_CONFIG_P0	0x8000C0110701103F	789
IOM0.DDRPHY_PC_MIRROR_CONFIG_P1	0x8000C0110701143F	790
IOM0.DDRPHY_PC_MIRROR_CONFIG_P2	0x8000C0110701183F	791
IOM0.DDRPHY_PC_MIRROR_CONFIG_P3	0x8000C01107011C3F	791
IOM0.DDRPHY_PC_MR0_RP0_P0	0x8000C01C0701103F	816
IOM0.DDRPHY_PC_MR0_RP0_P1	0x8000C01C0701143F	816
IOM0.DDRPHY_PC_MR0_RP0_P2	0x8000C01C0701183F	817
IOM0.DDRPHY_PC_MR0_RP0_P3	0x8000C01C07011C3F	817
IOM0.DDRPHY_PC_MR0_RP1_P0	0x8000C11C0701103F	837
IOM0.DDRPHY_PC_MR0_RP1_P1	0x8000C11C0701143F	838
IOM0.DDRPHY_PC_MR0_RP1_P2	0x8000C11C0701183F	838
IOM0.DDRPHY_PC_MR0_RP1_P3	0x8000C11C07011C3F	838
IOM0.DDRPHY_PC_MR0_RP2_P0	0x8000C21C0701103F	849

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IOM0.DDRPHY_PC_MR0_RP2_P1	0x8000C21C0701143F	850
IOM0.DDRPHY_PC_MR0_RP2_P2	0x8000C21C0701183F	850
IOM0.DDRPHY_PC_MR0_RP2_P3	0x8000C21C07011C3F	850
IOM0.DDRPHY_PC_MR0_RP3_P0	0x8000C31C0701103F	861
IOM0.DDRPHY_PC_MR0_RP3_P1	0x8000C31C0701143F	862
IOM0.DDRPHY_PC_MR0_RP3_P2	0x8000C31C0701183F	862
IOM0.DDRPHY_PC_MR0_RP3_P3	0x8000C31C07011C3F	862
IOM0.DDRPHY_PC_MR1_RP0_P0	0x8000C01D0701103F	817
IOM0.DDRPHY_PC_MR1_RP0_P1	0x8000C01D0701143F	818
IOM0.DDRPHY_PC_MR1_RP0_P2	0x8000C01D0701183F	818
IOM0.DDRPHY_PC_MR1_RP0_P3	0x8000C01D07011C3F	819
IOM0.DDRPHY_PC_MR1_RP1_P0	0x8000C11D0701103F	839
IOM0.DDRPHY_PC_MR1_RP1_P1	0x8000C11D0701143F	839
IOM0.DDRPHY_PC_MR1_RP1_P2	0x8000C11D0701183F	840
IOM0.DDRPHY_PC_MR1_RP1_P3	0x8000C11D07011C3F	840
IOM0.DDRPHY_PC_MR1_RP2_P0	0x8000C21D0701103F	851
IOM0.DDRPHY_PC_MR1_RP2_P1	0x8000C21D0701143F	851
IOM0.DDRPHY_PC_MR1_RP2_P2	0x8000C21D0701183F	852
IOM0.DDRPHY_PC_MR1_RP2_P3	0x8000C21D07011C3F	852
IOM0.DDRPHY_PC_MR1_RP3_P0	0x8000C31D0701103F	863
IOM0.DDRPHY_PC_MR1_RP3_P1	0x8000C31D0701143F	863
IOM0.DDRPHY_PC_MR1_RP3_P2	0x8000C31D0701183F	864
IOM0.DDRPHY_PC_MR1_RP3_P3	0x8000C31D07011C3F	864
IOM0.DDRPHY_PC_MR2_RP0_P0	0x8000C01E0701103F	819
IOM0.DDRPHY_PC_MR2_RP0_P1	0x8000C01E0701143F	819
IOM0.DDRPHY_PC_MR2_RP0_P2	0x8000C01E0701183F	820
IOM0.DDRPHY_PC_MR2_RP0_P3	0x8000C01E07011C3F	820
IOM0.DDRPHY_PC_MR2_RP1_P0	0x8000C11E0701103F	840
IOM0.DDRPHY_PC_MR2_RP1_P1	0x8000C11E0701143F	841
IOM0.DDRPHY_PC_MR2_RP1_P2	0x8000C11E0701183F	841
IOM0.DDRPHY_PC_MR2_RP1_P3	0x8000C11E07011C3F	842
IOM0.DDRPHY_PC_MR2_RP2_P0	0x8000C21E0701103F	852
IOM0.DDRPHY_PC_MR2_RP2_P1	0x8000C21E0701143F	853
IOM0.DDRPHY_PC_MR2_RP2_P2	0x8000C21E0701183F	853
IOM0.DDRPHY_PC_MR2_RP2_P3	0x8000C21E07011C3F	854
IOM0.DDRPHY_PC_MR2_RP3_P0	0x8000C31E0701103F	864
IOM0.DDRPHY_PC_MR2_RP3_P1	0x8000C31E0701143F	865
IOM0.DDRPHY_PC_MR2_RP3_P2	0x8000C31E0701183F	865
IOM0.DDRPHY_PC_MR2_RP3_P3	0x8000C31E07011C3F	866
IOM0.DDRPHY_PC_MR3_RP0_P0	0x8000C01F0701103F	821
IOM0.DDRPHY_PC_MR3_RP0_P1	0x8000C01F0701143F	821
IOM0.DDRPHY_PC_MR3_RP0_P2	0x8000C01F0701183F	821
IOM0.DDRPHY_PC_MR3_RP0_P3	0x8000C01F07011C3F	822

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IOM0.DDRPHY_PC_MR3_RP1_P0	0x8000C11F0701103F	842
IOM0.DDRPHY_PC_MR3_RP1_P1	0x8000C11F0701143F	842
IOM0.DDRPHY_PC_MR3_RP1_P2	0x8000C11F0701183F	843
IOM0.DDRPHY_PC_MR3_RP1_P3	0x8000C11F07011C3F	843
IOM0.DDRPHY_PC_MR3_RP2_P0	0x8000C21F0701103F	854
IOM0.DDRPHY_PC_MR3_RP2_P1	0x8000C21F0701143F	854
IOM0.DDRPHY_PC_MR3_RP2_P2	0x8000C21F0701183F	855
IOM0.DDRPHY_PC_MR3_RP2_P3	0x8000C21F07011C3F	855
IOM0.DDRPHY_PC_MR3_RP3_P0	0x8000C31F0701103F	866
IOM0.DDRPHY_PC_MR3_RP3_P1	0x8000C31F0701143F	866
IOM0.DDRPHY_PC_MR3_RP3_P2	0x8000C31F0701183F	867
IOM0.DDRPHY_PC_MR3_RP3_P3	0x8000C31F07011C3F	867
IOM0.DDRPHY_PC_MR4_RP0_P0	0x8000C0200701103F	822
IOM0.DDRPHY_PC_MR4_RP0_P1	0x8000C0200701143F	823
IOM0.DDRPHY_PC_MR4_RP0_P2	0x8000C0200701183F	823
IOM0.DDRPHY_PC_MR4_RP0_P3	0x8000C02007011C3F	823
IOM0.DDRPHY_PC_MR4_RP1_P0	0x8000C1200701103F	844
IOM0.DDRPHY_PC_MR4_RP1_P1	0x8000C1200701143F	844
IOM0.DDRPHY_PC_MR4_RP1_P2	0x8000C1200701183F	844
IOM0.DDRPHY_PC_MR4_RP1_P3	0x8000C12007011C3F	845
IOM0.DDRPHY_PC_MR4_RP2_P0	0x8000C2200701103F	856
IOM0.DDRPHY_PC_MR4_RP2_P1	0x8000C2200701143F	856
IOM0.DDRPHY_PC_MR4_RP2_P2	0x8000C2200701183F	856
IOM0.DDRPHY_PC_MR4_RP2_P3	0x8000C22007011C3F	857
IOM0.DDRPHY_PC_MR4_RP3_P0	0x8000C3200701103F	868
IOM0.DDRPHY_PC_MR4_RP3_P1	0x8000C3200701143F	868
IOM0.DDRPHY_PC_MR4_RP3_P2	0x8000C3200701183F	868
IOM0.DDRPHY_PC_MR4_RP3_P3	0x8000C32007011C3F	869
IOM0.DDRPHY_PC_MR5_RP0_P0	0x8000C0210701103F	824
IOM0.DDRPHY_PC_MR5_RP0_P1	0x8000C0210701143F	824
IOM0.DDRPHY_PC_MR5_RP0_P2	0x8000C0210701183F	825
IOM0.DDRPHY_PC_MR5_RP0_P3	0x8000C02107011C3F	825
IOM0.DDRPHY_PC_MR5_RP1_P0	0x8000C1210701103F	845
IOM0.DDRPHY_PC_MR5_RP1_P1	0x8000C1210701143F	846
IOM0.DDRPHY_PC_MR5_RP1_P2	0x8000C1210701183F	846
IOM0.DDRPHY_PC_MR5_RP1_P3	0x8000C12107011C3F	846
IOM0.DDRPHY_PC_MR5_RP2_P0	0x8000C2210701103F	857
IOM0.DDRPHY_PC_MR5_RP2_P1	0x8000C2210701143F	858
IOM0.DDRPHY_PC_MR5_RP2_P2	0x8000C2210701183F	858
IOM0.DDRPHY_PC_MR5_RP2_P3	0x8000C22107011C3F	858
IOM0.DDRPHY_PC_MR5_RP3_P0	0x8000C3210701103F	869
IOM0.DDRPHY_PC_MR5_RP3_P1	0x8000C3210701143F	870
IOM0.DDRPHY_PC_MR5_RP3_P2	0x8000C3210701183F	870

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IOM0.DDRPHY_PC_MR5_RP3_P3	0x8000C32107011C3F	870
IOM0.DDRPHY_PC_MR6_RP0_P0	0x8000C0220701103F	825
IOM0.DDRPHY_PC_MR6_RP0_P1	0x8000C0220701143F	826
IOM0.DDRPHY_PC_MR6_RP0_P2	0x8000C0220701183F	826
IOM0.DDRPHY_PC_MR6_RP0_P3	0x8000C02207011C3F	827
IOM0.DDRPHY_PC_MR6_RP1_P0	0x8000C1220701103F	847
IOM0.DDRPHY_PC_MR6_RP1_P1	0x8000C1220701143F	847
IOM0.DDRPHY_PC_MR6_RP1_P2	0x8000C1220701183F	848
IOM0.DDRPHY_PC_MR6_RP1_P3	0x8000C12207011C3F	848
IOM0.DDRPHY_PC_MR6_RP2_P0	0x8000C2220701103F	859
IOM0.DDRPHY_PC_MR6_RP2_P1	0x8000C2220701143F	859
IOM0.DDRPHY_PC_MR6_RP2_P2	0x8000C2220701183F	860
IOM0.DDRPHY_PC_MR6_RP2_P3	0x8000C22207011C3F	860
IOM0.DDRPHY_PC_MR6_RP3_P0	0x8000C3220701103F	871
IOM0.DDRPHY_PC_MR6_RP3_P1	0x8000C3220701143F	871
IOM0.DDRPHY_PC_MR6_RP3_P2	0x8000C3220701183F	872
IOM0.DDRPHY_PC_MR6_RP3_P3	0x8000C32207011C3F	872
IOM0.DDRPHY_PC_MR7_RP0_P0	0x8000C0230701103F	827
IOM0.DDRPHY_PC_MR7_RP0_P1	0x8000C0230701143F	827
IOM0.DDRPHY_PC_MR7_RP0_P2	0x8000C0230701183F	828
IOM0.DDRPHY_PC_MR7_RP0_P3	0x8000C02307011C3F	828
IOM0.DDRPHY_PC_MR7_RP1_P0	0x8000C1230701103F	848
IOM0.DDRPHY_PC_MR7_RP1_P1	0x8000C1230701143F	849
IOM0.DDRPHY_PC_MR7_RP1_P2	0x8000C1230701183F	849
IOM0.DDRPHY_PC_MR7_RP1_P3	0x8000C12307011C3F	849
IOM0.DDRPHY_PC_MR7_RP2_P0	0x8000C2230701103F	860
IOM0.DDRPHY_PC_MR7_RP2_P1	0x8000C2230701143F	861
IOM0.DDRPHY_PC_MR7_RP2_P2	0x8000C2230701183F	861
IOM0.DDRPHY_PC_MR7_RP2_P3	0x8000C22307011C3F	861
IOM0.DDRPHY_PC_MR7_RP3_P0	0x8000C3230701103F	872
IOM0.DDRPHY_PC_MR7_RP3_P1	0x8000C3230701143F	873
IOM0.DDRPHY_PC_MR7_RP3_P2	0x8000C3230701183F	873
IOM0.DDRPHY_PC_MR7_RP3_P3	0x8000C32307011C3F	873
IOM0.DDRPHY_PC_PBA_CONTROL_P0	0x8000C0150701103F	796
IOM0.DDRPHY_PC_PBA_CONTROL_P1	0x8000C0150701143F	797
IOM0.DDRPHY_PC_PBA_CONTROL_P2	0x8000C0150701183F	797
IOM0.DDRPHY_PC_PBA_CONTROL_P3	0x8000C01507011C3F	797
IOM0.DDRPHY_PC_PER_CAL_CONFIG_P0	0x8000C00B0701103F	763
IOM0.DDRPHY_PC_PER_CAL_CONFIG_P1	0x8000C00B0701143F	764
IOM0.DDRPHY_PC_PER_CAL_CONFIG_P2	0x8000C00B0701183F	765
IOM0.DDRPHY_PC_PER_CAL_CONFIG_P3	0x8000C00B07011C3F	766
IOM0.DDRPHY_PC_PER_ERR_INJECT_P0	0x8000C0010701103F	744
IOM0.DDRPHY_PC_PER_ERR_INJECT_P1	0x8000C0010701143F	745

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IOM0.DDRPHY_PC_PER_ERR_INJECT_P2	0x8000C0010701183F	745
IOM0.DDRPHY_PC_PER_ERR_INJECT_P3	0x8000C00107011C3F	746
IOM0.DDRPHY_PC_PER_ZCAL_CONFIG_P0	0x8000C00F0701103F	782
IOM0.DDRPHY_PC_PER_ZCAL_CONFIG_P1	0x8000C00F0701143F	783
IOM0.DDRPHY_PC_PER_ZCAL_CONFIG_P2	0x8000C00F0701183F	783
IOM0.DDRPHY_PC_PER_ZCAL_CONFIG_P3	0x8000C00F07011C3F	784
IOM0.DDRPHY_PC_POWERDOWN_1_P0	0x8000C0100701103F	785
IOM0.DDRPHY_PC_POWERDOWN_1_P1	0x8000C0100701143F	786
IOM0.DDRPHY_PC_POWERDOWN_1_P2	0x8000C0100701183F	787
IOM0.DDRPHY_PC_POWERDOWN_1_P3	0x8000C01007011C3F	788
IOM0.DDRPHY_PC_RANK_GROUP_EXT_P0	0x8000C0350701103F	836
IOM0.DDRPHY_PC_RANK_GROUP_EXT_P1	0x8000C0350701143F	836
IOM0.DDRPHY_PC_RANK_GROUP_EXT_P2	0x8000C0350701183F	836
IOM0.DDRPHY_PC_RANK_GROUP_EXT_P3	0x8000C03507011C3F	837
IOM0.DDRPHY_PC_RANK_PAIR0_P0	0x8000C0020701103F	747
IOM0.DDRPHY_PC_RANK_PAIR0_P1	0x8000C0020701143F	747
IOM0.DDRPHY_PC_RANK_PAIR0_P2	0x8000C0020701183F	748
IOM0.DDRPHY_PC_RANK_PAIR0_P3	0x8000C00207011C3F	749
IOM0.DDRPHY_PC_RANK_PAIR1_P0	0x8000C0030701103F	750
IOM0.DDRPHY_PC_RANK_PAIR1_P1	0x8000C0030701143F	750
IOM0.DDRPHY_PC_RANK_PAIR1_P2	0x8000C0030701183F	751
IOM0.DDRPHY_PC_RANK_PAIR1_P3	0x8000C00307011C3F	752
IOM0.DDRPHY_PC_RANK_PAIR2_P0	0x8000C0300701103F	828
IOM0.DDRPHY_PC_RANK_PAIR2_P1	0x8000C0300701143F	829
IOM0.DDRPHY_PC_RANK_PAIR2_P2	0x8000C0300701183F	830
IOM0.DDRPHY_PC_RANK_PAIR2_P3	0x8000C03007011C3F	830
IOM0.DDRPHY_PC_RANK_PAIR3_P0	0x8000C0310701103F	831
IOM0.DDRPHY_PC_RANK_PAIR3_P1	0x8000C0310701143F	832
IOM0.DDRPHY_PC_RANK_PAIR3_P2	0x8000C0310701183F	832
IOM0.DDRPHY_PC_RANK_PAIR3_P3	0x8000C03107011C3F	833
IOM0.DDRPHY_PC_RELOAD_VALUE0_P0	0x8000C0050701103F	754
IOM0.DDRPHY_PC_RELOAD_VALUE0_P1	0x8000C0050701143F	754
IOM0.DDRPHY_PC_RELOAD_VALUE0_P2	0x8000C0050701183F	754
IOM0.DDRPHY_PC_RELOAD_VALUE0_P3	0x8000C00507011C3F	755
IOM0.DDRPHY_PC_RESETS_P0	0x8000C00E0701103F	777
IOM0.DDRPHY_PC_RESETS_P1	0x8000C00E0701143F	779
IOM0.DDRPHY_PC_RESETS_P2	0x8000C00E0701183F	780
IOM0.DDRPHY_PC_RESETS_P3	0x8000C00E07011C3F	781
IOM0.DDRPHY_PC_ZCAL_TIMER_P0	0x8000C0090701103F	760
IOM0.DDRPHY_PC_ZCAL_TIMER_P1	0x8000C0090701143F	760
IOM0.DDRPHY_PC_ZCAL_TIMER_P2	0x8000C0090701183F	761
IOM0.DDRPHY_PC_ZCAL_TIMER_P3	0x8000C00907011C3F	761
IOM0.DDRPHY_PC_ZCAL_TIMER_RELOAD_VALUE_P0	0x8000C00A0701103F	762

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IOM0.DDRPHY_PC_ZCAL_TIMER_RELOAD_VALUE_P1	0x8000C00A0701143F	762
IOM0.DDRPHY_PC_ZCAL_TIMER_RELOAD_VALUE_P2	0x8000C00A0701183F	762
IOM0.DDRPHY_PC_ZCAL_TIMER_RELOAD_VALUE_P3	0x8000C00A07011C3F	763

The PC registers are listed in the following tables.

Register Name	**PC DLL / ZCAL Calibration Status Register**
Mnemonic	IOM0.DDRPHY_PC_DLL_ZCAL_CAL_STATUS_P0
Address	8000C0000701103F (SCOM)
Description	This PHY control (PC) register is a combined summary of the delay locked loop (DLL) calibration status over all the data path 16 (DP16) instances and address (ADR) instances. The individual DLL status is stored in the DP16 and ADR registers. This register also contains the status of the impedance calibration (ZCAL) and impedance control (ZCONTROL) logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RO	DP_DLL_CAL_GOOD: 0 = DLL calibration was not started or did not complete successfully. 1 = DLL calibration was successful. **Note:** To provide a more stable value for software to poll, each DLL sets this bit to 1 when either the local DLLs CAL_GOOD = 1 or when it is continuously performing fine calibration while neither CAL_ERROR nor CAL_ERROR_FINE is present. **Note:** The CAL_GOODs from all the DP16s are ANDed together to form this summary bit. Thus, all DLLs in all DP16s must be trained successfully for it to be 1.
49	RO	DP_DLL_CAL_ERROR: 1 = A fatal error occurred during voltage regulation (VREG) or coarse calibration. 0 = No error occurred. **Note:** The CAL_ERRORs from all the DP16s are ORed together to form this summary bit. Thus, any DP16 DLL that trained unsuccessfully can set this bit.
50	RO	DP_DLL_CAL_ERROR_FINE: 1 = A fatal error occurred during fine calibration. 0 = No error occurred. **Note:** The CAL_ERROR_FINEs from all DP16s are ORed together to form this summary bit. Thus, any DP16 DLL that trained unsuccessfully can set this bit.
51	RO	ADR_DLL_CAL_GOOD: 0 = DLL calibration was not started or did not complete successfully. 1 = DLL calibration was successful. **Note:** To provide a more stable value for software to poll, each DLL sets this bit to 1 when either the local DLLs CAL_GOOD = 1 or when it is continuously performing fine calibration while neither CAL_ERROR nor CAL_ERROR_FINE is present.
52	RO	ADR_DLL_CAL_ERROR: 1 = A fatal error occurred during VREG or coarse calibration. 0 = No error occurred.
53	RO	ADR_DLL_CAL_ERROR_FINE: 1 = A fatal error occurred during fine calibration. 0 = No error occurred.
54:62	RO	Constant = 0b000000000

Bits	SCOM	Field Mnemonic: Description
63	RO	ZCAL_DONE: 1 = The ZCAL / ZCONTROL algorithm is complete. 0 = The ZCAL / ZCONTROL is running or has not been started.

Register Name	**PC DLL / ZCAL Calibration Status Register**
Mnemonic	IOM0.DDRPHY_PC_DLL_ZCAL_CAL_STATUS_P1
Address	8000C0000701143F (SCOM)
Description	This PHY control (PC) register is a combined summary of the delay locked loop (DLL) calibration status over all the DP16 instances and ADR instances. The individual DLL status is stored in the DP16 and ADR registers. This register also contains the status of the ZCAL and ZCONTROL logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RO	DP_DLL_CAL_GOOD: 0 = DLL calibration was not started or did not complete successfully. 1 = DLL calibration was successful. **Note:** To provide a more stable value for software to poll, each DLL sets this bit to 1 when either the local DLLs CAL_GOOD = 1 or when it is continuously performing fine calibration while neither CAL_ERROR nor CAL_ERROR_FINE is present. **Note:** The CAL_GOODs from all the DP16s are ANDed together to form this summary bit. Thus, all DLLs in all DP16s must be trained successfully for it to be 1.
49	RO	DP_DLL_CAL_ERROR: 1 = A fatal error occurred during VREG or coarse calibration. 0 = No error occurred. **Note:** The CAL_ERRORs from all the DP16s are ORed together to form this summary bit. Thus, any DP16 DLL that trained unsuccessfully can set this bit.
50	RO	DP_DLL_CAL_ERROR_FINE: 1 = A fatal error occurred during fine calibration. 0 = No error occurred. **Note:** The CAL_ERROR_FINEs from all DP16s are ORed together to form this summary bit. Thus, any DP16 DLL that trained unsuccessfully can set this bit.
51	RO	ADR_DLL_CAL_GOOD: 0 = DLL calibration was not started or did not complete successfully. 1 = DLL calibration was successful **Note:** To provide a more stable value for software to poll, each DLL sets this bit to 1 when either the local DLLs CAL_GOOD = 1 or when it is continuously performing fine calibration while neither CAL_ERROR nor CAL_ERROR_FINE is present.
52	RO	ADR_DLL_CAL_ERROR: 1 = A fatal error occurred during VREG or coarse calibration. 0 = No error occurred.
53	RO	ADR_DLL_CAL_ERROR_FINE: 1 = A fatal error occurred during fine calibration. 0 = No error occurred.
54:62	RO	Constant = 0b000000000
63	RO	ZCAL_DONE: 1 = The ZCAL / ZCONTROL algorithm is complete. 0 = The ZCAL / ZCONTROL is running or has not been started.

Register Name	PC DLL / ZCAL Calibration Status Register
Mnemonic	IOM0.DDRPHY_PC_DLL_ZCAL_CAL_STATUS_P2
Address	8000C0000701183F (SCOM)
Description	This PHY control (PC) register is a combined summary of the delay locked loop (DLL) calibration status over all the DP16 instances and ADR instances. The individual DLL status is stored in the DP16 and ADR registers. This register also contains the status of the ZCAL and ZCONTROL logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RO	DP_DLL_CAL_GOOD: 0 = DLL calibration was not started or did not complete successfully. 1 = DLL calibration was successful. **Note:** To provide a more stable value for software to poll, each DLL sets this bit to 1 when either the local DLLs CAL_GOOD = 1 or when it is continuously performing fine calibration while neither CAL_ERROR nor CAL_ERROR_FINE is present. **Note:** The CAL_GOODs from all the DP16s are ANDed together to form this summary bit. Thus, all DLLs in all DP16s must be trained successfully for it to be 1.
49	RO	DP_DLL_CAL_ERROR: 1 = A fatal error occurred during VREG or coarse calibration. 0 = No error occurred. **Note:** The CAL_ERRORs from all the DP16s are ORed together to form this summary bit. Thus, any DP16 DLL that trained unsuccessfully can set this bit.
50	RO	DP_DLL_CAL_ERROR_FINE: 1 = A fatal error occurred during fine calibration. 0 = No error occurred. **Note:** The CAL_ERROR_FINEs from all DP16s are ORed together to form this summary bit. Thus, any DP16 DLL that trained unsuccessfully can set this bit.
51	RO	ADR_DLL_CAL_GOOD: 0 = DLL calibration was not started or did not complete successfully. 1 = DLL calibration was successful **Note:** To provide a more stable value for software to poll, each DLL sets this bit to 1 when either the local DLLs CAL_GOOD = 1 or when it is continuously performing fine calibration while neither CAL_ERROR nor CAL_ERROR_FINE is present.
52	RO	ADR_DLL_CAL_ERROR: 1 = A fatal error occurred during VREG or coarse calibration. 0 = No error occurred.
53	RO	ADR_DLL_CAL_ERROR_FINE: 1 = A fatal error occurred during fine calibration. 0 = No error occurred.
54:62	RO	Constant = 0b000000000
63	RO	ZCAL_DONE: 1 = The ZCAL / ZCONTROL algorithm is complete. 0 = The ZCAL / ZCONTROL is running or has not been started.

Register Name	PC DLL / ZCAL Calibration Status Register
Mnemonic	IOM0.DDRPHY_PC_DLL_ZCAL_CAL_STATUS_P3
Address	8000C00007011C3F (SCOM)
Description	This PHY control (PC) register is a combined summary of the delay locked loop (DLL) calibration status over all the DP16 instances and ADR instances. The individual DLL status is stored in the DP16 and ADR registers. This register also contains the status of the ZCAL and ZCONTROL logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RO	DP_DLL_CAL_GOOD: 0 = DLL calibration was not started or did not complete successfully. 1 = DLL calibration was successful. **Note:** To provide a more stable value for software to poll, each DLL sets this bit to 1 when either the local DLLs CAL_GOOD = 1 or when it is continuously performing fine calibration while neither CAL_ERROR nor CAL_ERROR_FINE is present. **Note:** The CAL_GOODs from all the DP16s are ANDed together to form this summary bit. Thus, all DLLs in all DP16s must be trained successfully for it to be 1.
49	RO	DP_DLL_CAL_ERROR: 1 = A fatal error occurred during VREG or coarse calibration. 0 = No error occurred. **Note:** The CAL_ERRORs from all the DP16s are ORed together to form this summary bit. Thus, any DP16 DLL that trained unsuccessfully can set this bit.
50	RO	DP_DLL_CAL_ERROR_FINE: 1 = A fatal error occurred during fine calibration. 0 = No error occurred. **Note:** The CAL_ERROR_FINEs from all DP16s are ORed together to form this summary bit. Thus, any DP16 DLL that trained unsuccessfully can set this bit.
51	RO	ADR_DLL_CAL_GOOD: 0 = DLL calibration was not started or did not complete successfully. 1 = DLL calibration was successful **Note:** To provide a more stable value for software to poll, each DLL sets this bit to 1 when either the local DLLs CAL_GOOD = 1 or when it is continuously performing fine calibration while neither CAL_ERROR nor CAL_ERROR_FINE is present.
52	RO	ADR_DLL_CAL_ERROR: 1 = A fatal error occurred during VREG or coarse calibration. 0 = No error occurred.
53	RO	ADR_DLL_CAL_ERROR_FINE: 1 = A fatal error occurred during fine calibration. 0 = No error occurred.
54:62	RO	Constant = 0b000000000
63	RO	ZCAL_DONE: 1 = The ZCAL / ZCONTROL algorithm is complete. 0 = The ZCAL / ZCONTROL is running or has not been started.

Register Name	PC Periodic Calibration Error Inject
Mnemonic	IOM0.DDRPHY_PC_PER_ERR_INJECT_P0
Address	8000C0010701103F (SCOM)
Description	This register is used to inject errors during periodic calibration to validate the error recovery features of the physical layer (PHY). This register must not be modified during normal operation.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	CA_PARITY_ERR_INJECT: 0 = Disable command/address error injection. 1 = Enable command/address error injection.
49	RW	HARD_ERROR: When EN_ERR_INJECT = 1: 0 = Enable a soft error. 1 = Enable a hard error.

Bits	SCOM	Field Mnemonic: Description
50	RW	HAS_FIRED: 0 = No errors. 1 = An error was previously fired.
51	RW	RECUR_ERROR: 0 = A soft error will fire once. 1 = A soft error will reoccur.
52:57	RW	CONFIG_CNT: Sets the number of calibration cycles before an error fires.
58	RW	EN_PARITY_ERROR: When EN_ERR_INJECT = 1: 0 = No parity error injection. 1 = Parity error injection.
59:63	RW	ERROR_THROWN_COUNT: Counts the number of errors thrown over time.

Register Name	PC Periodic Calibration Error Inject
Mnemonic	IOM0.DDRPHY_PC_PER_ERR_INJECT_P1
Address	8000C0010701143F (SCOM)
Description	This register is used to inject errors during periodic calibration to validate the error recovery features of the PHY. This register must not be modified during normal operation.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	CA_PARITY_ERR_INJECT: 0 = Disable command/address error injection. 1 = Enable command/address error injection.
49	RW	HARD_ERROR: When EN_ERR_INJECT = 1: 0 = Enable a soft error. 1 = Enable a hard error.
50	RW	HAS_FIRED: 0 = No errors. 1 = An error was previously fired.
51	RW	RECUR_ERROR: 0 = A soft error will fire once. 1 = A soft error will reoccur.
52:57	RW	CONFIG_CNT: Sets the number of calibration cycles before an error fires.
58	RW	EN_PARITY_ERROR: When EN_ERR_INJECT = 1: 0 = No parity error injection. 1 = Parity error injection.
59:63	RW	ERROR_THROWN_COUNT: Counts the number of errors thrown over time.

Register Name	PC Periodic Calibration Error Inject
Mnemonic	IOM0.DDRPHY_PC_PER_ERR_INJECT_P2
Address	8000C0010701183F (SCOM)
Description	This register is used to inject errors during periodic calibration to validate the error recovery features of the PHY. This register must not be modified during normal operation.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	CA_PARITY_ERR_INJECT: 0 = Disable command/address error injection. 1 = Enable command/address error injection.
49	RW	HARD_ERROR: When EN_ERR_INJECT = 1: 0 = Enable a soft error. 1 = Enable a hard error.
50	RW	HAS_FIRED: 0 = No errors. 1 = An error was previously fired.
51	RW	RECUR_ERROR: 0 = A soft error will fire once. 1 = A soft error will reoccur.
52:57	RW	CONFIG_CNT: Sets the number of calibration cycles before an error fires.
58	RW	EN_PARITY_ERROR: When EN_ERR_INJECT = 1: 0 = No parity error injection. 1 = Parity error injection.
59:63	RW	ERROR_THROWN_COUNT: Counts the number of errors thrown over time.

Register Name	PC Periodic Calibration Error Inject
Mnemonic	IOM0.DDRPHY_PC_PER_ERR_INJECT_P3
Address	8000C00107011C3F (SCOM)
Description	This register is used to inject errors during periodic calibration to validate the error recovery features of the PHY. This register must not be modified during normal operation.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	CA_PARITY_ERR_INJECT: 0 = Disable command/address error injection. 1 = Enable command/address error injection.
49	RW	HARD_ERROR: When EN_ERR_INJECT = 1: 0 = Enable a soft error. 1 = Enable a hard error.
50	RW	HAS_FIRED: 0 = No errors. 1 = An error was previously fired.
51	RW	RECUR_ERROR: 0 = A soft error will fire once. 1 = A soft error will reoccur.
52:57	RW	CONFIG_CNT: Sets the number of calibration cycles before an error fires.
58	RW	EN_PARITY_ERROR: When EN_ERR_INJECT = 1: 0 = No parity error injection. 1 = Parity error injection.
59:63	RW	ERROR_THROWN_COUNT: Counts the number of errors thrown over time.

Register Name	PC Rank Pair 0 Register
Mnemonic	IOM0.DDRPHY_PC_RANK_PAIR0_P0
Address	8000C0020701103F (SCOM)
Description	These four registers assign rank numbers to the rank groups. The double data rate (DDR) PHY supports up to four ranks. Ranks in a rank group must have the same system timing and delay characteristics. The DDR PHY core calibrates the primary rank in the rank group, and uses the delay settings when any rank in the rank group is accessed. In the DDR PHY core, all parameters that are rank dependent are stored in one of four rank group (or rank pair) register sets. By configuring these registers, one to four ranks can be assigned to a rank group. When a rank is accessed, the parameter values used are determined by the configuration of this rank pair association register. Assigning one rank to multiple rank groups causes indeterminate behavior of the DDR PHY core.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	RANK_PAIR0_PRI: Primary rank of rank pair 0. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011). The primary rank of rank pair 0 must be defined and valid for proper PHY functionality. Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Mode Register latency programming for all enabled ranks and rank pairs must be consistent.
51	RW	RANK_PAIR0_PRI_V: The value in the RANK_PAIR0_PRI field is valid.
52:54	RW	RANK_PAIR0_SEC: Secondary rank of rank pair 0. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
55	RW	RANK_PAIR0_SEC_V: The value in the RANK_PAIR0_SEC field is valid. If this bit is set, the RANK_PAIR0_PRI_V bit must be set.
56:58	RW	RANK_PAIR1_PRI: Primary rank of rank pair 1. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
59	RW	RANK_PAIR1_PRI_V: The value in the RANK_PAIR1_PRI field is valid. If this bit is set, the RANK_PAIR0_PRI_V bit must be set.
60:62	RW	RANK_PAIR1_SEC: Secondary rank of rank pair 1. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
63	RW	RANK_PAIR1_SEC_V: The value in the RANK_PAIR1_SEC field is valid. If this bit is set, the RANK_PAIR1_PRI_V bit must be set.

Register Name	PC Rank Pair 0 Register
Mnemonic	IOM0.DDRPHY_PC_RANK_PAIR0_P1
Address	8000C0020701143F (SCOM)
Description	These four registers assign rank numbers to the rank groups. The DDR PHY supports up to four ranks. Each rank beyond the fourth rank must be grouped with another rank. Ranks in a rank group must have the same system timing and delay characteristics. The DDR PHY core calibrates the primary rank in the rank group, and uses the delay settings when any rank in the rank group is accessed. In the DDR PHY core, all parameters that are rank dependent are stored in one of four rank group (or rank pair) register sets. By configuring these registers, one to four ranks can be assigned to a rank group. When a rank is accessed, the parameter values used are determined by the configuration of this rank pair association register. Assigning one rank to multiple rank groups causes indeterminate behavior of the DDR PHY core.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:50	RW	RANK_PAIR0_PRI: Primary rank of rank pair 0. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011). The primary rank of rank pair 0 must be defined and valid for proper PHY functionality. Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Mode Register latency programming for all enabled ranks and rank pairs must be consistent.
51	RW	RANK_PAIR0_PRI_V: The value in the RANK_PAIR0_PRI field is valid.
52:54	RW	RANK_PAIR0_SEC: Secondary rank of rank pair 0. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
55	RW	RANK_PAIR0_SEC_V: The value in the RANK_PAIR0_SEC field is valid. If this bit is set, the RANK_PAIR0_PRI_V bit must be set.
56:58	RW	RANK_PAIR1_PRI: Primary rank of rank pair 1. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
59	RW	RANK_PAIR1_PRI_V: The value in the RANK_PAIR1_PRI field is valid. If this bit is set, the RANK_PAIR0_PRI_V bit must be set.
60:62	RW	RANK_PAIR1_SEC: Secondary rank of rank pair 1. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
63	RW	RANK_PAIR1_SEC_V: The value in the RANK_PAIR1_SEC field is valid. If this bit is set, the RANK_PAIR1_PRI_V bit must be set.

Register Name	**PC Rank Pair 0 Register**
Mnemonic	IOM0.DDRPHY_PC_RANK_PAIR0_P2
Address	8000C0020701183F (SCOM)
Description	These four registers assign rank numbers to the rank groups. The DDR PHY supports up to four ranks. Each rank beyond the fourth rank must be grouped with another rank. Ranks in a rank group must have the same system timing and delay characteristics. The DDR PHY core calibrates the primary rank in the rank group, and uses the delay settings when any rank in the rank group is accessed. In the DDR PHY core, all parameters that are rank dependent are stored in one of four rank group (or rank pair) register sets. By configuring these registers, one to four ranks can be assigned to a rank group. When a rank is accessed, the parameter values used are determined by the configuration of this rank pair association register. Assigning one rank to multiple rank groups causes indeterminate behavior of the DDR PHY core.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:50	RW	RANK_PAIR0_PRI: Primary rank of rank pair 0. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011). The primary rank of rank pair 0 must be defined and valid for proper PHY functionality. Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Mode Register latency programming for all enabled ranks and rank pairs must be consistent.
51	RW	RANK_PAIR0_PRI_V: The value in the RANK_PAIR0_PRI field is valid.
52:54	RW	RANK_PAIR0_SEC: Secondary rank of rank pair 0. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
55	RW	RANK_PAIR0_SEC_V: The value in the RANK_PAIR0_SEC field is valid. If this bit is set, the RANK_PAIR0_PRI_V bit must be set.
56:58	RW	RANK_PAIR1_PRI: Primary rank of rank pair 1. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
59	RW	RANK_PAIR1_PRI_V: The value in the RANK_PAIR1_PRI field is valid. If this bit is set, the RANK_PAIR0_PRI_V bit must be set.

Bits	SCOM	Field Mnemonic: Description
60:62	RW	RANK_PAIR1_SEC: Secondary rank of rank pair 1. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
63	RW	RANK_PAIR1_SEC_V: The value in the RANK_PAIR1_SEC field is valid. If this bit is set, the RANK_PAIR1_PRI_V bit must be set.

Register Name	**PC Rank Pair 0 Register**
Mnemonic	IOM0.DDRPHY_PC_RANK_PAIR0_P3
Address	8000C00207011C3F (SCOM)
Description	These four registers assign rank numbers to the rank groups. The DDR PHY supports up to four ranks. Each rank beyond the fourth rank must be grouped with another rank. Ranks in a rank group must have the same system timing and delay characteristics. The DDR PHY core calibrates the primary rank in the rank group, and uses the delay settings when any rank in the rank group is accessed. In the DDR PHY core, all parameters that are rank dependent are stored in one of four rank group (or rank pair) register sets. By configuring these registers, one to four ranks can be assigned to a rank group. When a rank is accessed, the parameter values used are determined by the configuration of this rank pair association register. Assigning one rank to multiple rank groups causes indeterminate behavior of the DDR PHY core.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	RANK_PAIR0_PRI: Primary rank of rank pair 0. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011). The primary rank of rank pair 0 must be defined and valid for proper PHY functionality. Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Mode Register latency programming for all enabled ranks and rank pairs must be consistent.
51	RW	RANK_PAIR0_PRI_V: The value in the RANK_PAIR0_PRI field is valid.
52:54	RW	RANK_PAIR0_SEC: Secondary rank of rank pair 0. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
55	RW	RANK_PAIR0_SEC_V: The value in the RANK_PAIR0_SEC field is valid. If this bit is set, the RANK_PAIR0_PRI_V bit must be set.
56:58	RW	RANK_PAIR1_PRI: Primary rank of rank pair 1. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
59	RW	RANK_PAIR1_PRI_V: The value in the RANK_PAIR1_PRI field is valid. If this bit is set, the RANK_PAIR0_PRI_V bit must be set.
60:62	RW	RANK_PAIR1_SEC: Secondary rank of rank pair 1. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
63	RW	RANK_PAIR1_SEC_V: The value in the RANK_PAIR1_SEC field is valid. If this bit is set, the RANK_PAIR1_PRI_V bit must be set.

Register Name	PC Rank Pair 1 Register
Mnemonic	IOM0.DDRPHY_PC_RANK_PAIR1_P0
Address	8000C0030701103F (SCOM)
Description	These four registers assign rank numbers to the rank groups. The DDR PHY supports up to four ranks. Ranks in a rank group must have the same system timing and delay characteristics. The DDR PHY core calibrates the primary rank in the rank group, and uses the delay settings when any rank in the rank group is accessed. In the DDR PHY core, all parameters that are rank dependent are stored in one of four rank group (or rank pair) register sets. By configuring these registers, one to four ranks can be assigned to a rank group. When a rank is accessed, the parameter values used are determined by the configuration of this rank pair association register. Assigning one rank to multiple rank groups causes indeterminate behavior of the DDR PHY core.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	RANK_PAIR2_PRI: Primary rank of rank pair 2. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
51	RW	RANK_PAIR2_PRI_V: The value in the RANK_PAIR2_PRI field is valid. If this bit is set, the RANK_PAIR1_PRI_V bit must be set in the PC Rank Pair 0 Register.
52:54	RW	RANK_PAIR2_SEC: Secondary rank of rank pair 2. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
55	RW	RANK_PAIR2_SEC_V: The value in the RANK_PAIR2_SEC field is valid. If this bit is set, the RANK_PAIR2_PRI_V bit must be set.
56:58	RW	RANK_PAIR3_PRI: Primary rank of rank pair 3. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
59	RW	RANK_PAIR3_PRI_V: The value in the RANK_PAIR3_PRI field is valid. If this bit is set, the RANK_PAIR2_PRI_V bit must be set.
60:62	RW	RANK_PAIR3_SEC: Secondary rank of rank pair 3. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
63	RW	RANK_PAIR3_SEC_V: The value in the RANK_PAIR3_SEC field is valid. If this bit is set, the RANK_PAIR3_PRI_V bit must be set.

Register Name	PC Rank Pair 1 Register
Mnemonic	IOM0.DDRPHY_PC_RANK_PAIR1_P1
Address	8000C0030701143F (SCOM)
Description	These four registers assign rank numbers to the rank groups. The DDR PHY supports up to four ranks. Ranks in a rank group must have the same system timing and delay characteristics. The DDR PHY core calibrates the primary rank in the rank group, and uses the delay settings when any rank in the rank group is accessed. In the DDR PHY core, all parameters that are rank dependent are stored in one of four rank group (or rank pair) register sets. By configuring these registers, one to four ranks can be assigned to a rank group. When a rank is accessed, the parameter values used are determined by the configuration of this rank pair association register. Assigning one rank to multiple rank groups causes indeterminate behavior of the DDR PHY core.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	RANK_PAIR2_PRI: Primary rank of rank pair 2. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
51	RW	RANK_PAIR2_PRI_V: The value in the RANK_PAIR2_PRI field is valid. If this bit is set, the RANK_PAIR1_PRI_V bit must be set in the PC Rank Pair 0 Register.
52:54	RW	RANK_PAIR2_SEC: Secondary rank of rank pair 2. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).

Bits	SCOM	Field Mnemonic: Description
55	RW	RANK_PAIR2_SEC_V: The value in the RANK_PAIR2_SEC field is valid. If this bit is set, the RANK_PAIR2_PRI_V bit must be set.
56:58	RW	RANK_PAIR3_PRI: Primary rank of rank pair 3. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
59	RW	RANK_PAIR3_PRI_V: The value in the RANK_PAIR3_PRI field is valid. If this bit is set, the RANK_PAIR2_PRI_V bit must be set.
60:62	RW	RANK_PAIR3_SEC: Secondary rank of rank pair 3. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
63	RW	RANK_PAIR3_SEC_V: The value in the RANK_PAIR3_SEC field is valid. If this bit is set, the RANK_PAIR3_PRI_V bit must be set.

Register Name	PC Rank Pair 1 Register
Mnemonic	IOM0.DDRPHY_PC_RANK_PAIR1_P2
Address	8000C0030701183F (SCOM)
Description	These four registers assign rank numbers to the rank groups. The DDR PHY supports up to four ranks. Ranks in a rank group must have the same system timing and delay characteristics. The DDR PHY core calibrates the primary rank in the rank group, and uses the delay settings when any rank in the rank group is accessed. In the DDR PHY core, all parameters that are rank dependent are stored in one of four rank group (or rank pair) register sets. By configuring these registers, one to four ranks can be assigned to a rank group. When a rank is accessed, the parameter values used are determined by the configuration of this rank pair association register. Assigning one rank to multiple rank groups causes indeterminate behavior of the DDR PHY core.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	RANK_PAIR2_PRI: Primary rank of rank pair 2. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
51	RW	RANK_PAIR2_PRI_V: The value in the RANK_PAIR2_PRI field is valid. If this bit is set, the RANK_PAIR1_PRI_V bit must be set in the PC Rank Pair 0 Register.
52:54	RW	RANK_PAIR2_SEC: Secondary rank of rank pair 2. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
55	RW	RANK_PAIR2_SEC_V: The value in the RANK_PAIR2_SEC field is valid. If this bit is set, the RANK_PAIR2_PRI_V bit must be set.
56:58	RW	RANK_PAIR3_PRI: Primary rank of rank pair 3. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
59	RW	RANK_PAIR3_PRI_V: The value in the RANK_PAIR3_PRI field is valid. If this bit is set, the RANK_PAIR2_PRI_V bit must be set.
60:62	RW	RANK_PAIR3_SEC: Secondary rank of rank pair 3. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
63	RW	RANK_PAIR3_SEC_V: The value in the RANK_PAIR3_SEC field is valid. If this bit is set, the RANK_PAIR3_PRI_V bit must be set.

Register Name	PC Rank Pair 1 Register
Mnemonic	IOM0.DDRPHY_PC_RANK_PAIR1_P3
Address	8000C00307011C3F (SCOM)
Description	These four registers assign rank numbers to the rank groups. The DDR PHY supports up to four ranks. Ranks in a rank group must have the same system timing and delay characteristics. The DDR PHY core calibrates the primary rank in the rank group, and uses the delay settings when any rank in the rank group is accessed. In the DDR PHY core, all parameters that are rank dependent are stored in one of four rank group (or rank pair) register sets. By configuring these registers, one to four ranks can be assigned to a rank group. When a rank is accessed, the parameter values used are determined by the configuration of this rank pair association register. Assigning one rank to multiple rank groups causes indeterminate behavior of the DDR PHY core.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	RANK_PAIR2_PRI: Primary rank of rank pair 2. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
51	RW	RANK_PAIR2_PRI_V: The value in the RANK_PAIR2_PRI field is valid. If this bit is set, the RANK_PAIR1_PRI_V bit must be set in the PC Rank Pair 0 Register.
52:54	RW	RANK_PAIR2_SEC: Secondary rank of rank pair 2. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
55	RW	RANK_PAIR2_SEC_V: The value in the RANK_PAIR2_SEC field is valid. If this bit is set, the RANK_PAIR2_PRI_V bit must be set.
56:58	RW	RANK_PAIR3_PRI: Primary rank of rank pair 3. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
59	RW	RANK_PAIR3_PRI_V: The value in the RANK_PAIR3_PRI field is valid. If this bit is set, the RANK_PAIR2_PRI_V bit must be set.
60:62	RW	RANK_PAIR3_SEC: Secondary rank of rank pair 3. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
63	RW	RANK_PAIR3_SEC_V: The value in the RANK_PAIR3_SEC field is valid. If this bit is set, the RANK_PAIR3_PRI_V bit must be set.

Register Name	PC Periodic Base Counter 0 Register
Mnemonic	IOM0.DDRPHY_PC_BASE_CNTR0_P0
Address	8000C0040701103F (SCOM)
Description	This register generates a periodic one-clock-cycle enable signal for the PC Periodic Base Counter 1 Register. This register is the first of three cascaded counters.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	ROX	PERIODIC_BASE_CNTR0: Periodic base counter 0. When enabled via PERIODIC_CAL_REQ_EN in the PC Periodic Reload Value 0 Register, the counter is free running (counts every dphy_gckn clock cycle). When this counter rolls over, it is reloaded with the value {PERIODIC_RELOAD_VALUE0 & 0} from the PC Periodic Reload Value 0 Register. This counter enables the PC Periodic Base Counter 1 for one count (one dphy_gckn clock cycle) every (PERIODIC_RELOAD_VALUE0 x 2) + 1 dphy_gckn cycles. This counter is used by internal state machines during initial calibration and periodic calibrations. Therefore, during initial calibrations and periodic calibrations, the read value of this register is undefined.

Register Name	PC Periodic Base Counter 0 Register
Mnemonic	IOM0.DDRPHY_PC_BASE_CNTR0_P1
Address	8000C0040701143F (SCOM)
Description	This register generates a periodic one-clock-cycle enable signal for the PC Periodic Base Counter 1 Register. This register is the first of three cascaded counters.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	ROX	PERIODIC_BASE_CNTR0: Periodic base counter 0. When enabled via PERIODIC_CAL_REQ_EN in the PC Periodic Reload Value 0 Register, the counter is free running (counts every dphy_gckn clock cycle). When this counter rolls over, it is reloaded with the value {PERIODIC_RELOAD_VALUE0 & 0} from the PC Periodic Reload Value 0 Register. This counter enables the PC Periodic Base Counter 1 for one count (one dphy_gckn clock cycle) every (PERIODIC_RELOAD_VALUE0 x 2) + 1 dphy_gckn cycles. This counter is used by internal state machines during initial calibration and periodic calibrations. Therefore, during initial calibrations and periodic calibrations, the read value of this register is undefined.

Register Name	PC Periodic Base Counter 0 Register
Mnemonic	IOM0.DDRPHY_PC_BASE_CNTR0_P2
Address	8000C0040701183F (SCOM)
Description	This register generates a periodic one-clock-cycle enable signal for the PC Periodic Base Counter 1 Register. This register is the first of three cascaded counters.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	ROX	PERIODIC_BASE_CNTR0: Periodic base counter 0. When enabled via PERIODIC_CAL_REQ_EN in the PC Periodic Reload Value 0 Register, the counter is free running (counts every dphy_gckn clock cycle). When this counter rolls over, it is reloaded with the value {PERIODIC_RELOAD_VALUE0 & 0} from the PC Periodic Reload Value 0 Register. This counter enables the PC Periodic Base Counter 1 for one count (one dphy_gckn clock cycle) every (PERIODIC_RELOAD_VALUE0 x 2) + 1 dphy_gckn cycles. This counter is used by internal state machines during initial calibration and periodic calibrations. Therefore, during initial calibrations and periodic calibrations, the read value of this register is undefined.

Register Name	PC Periodic Base Counter 0 Register
Mnemonic	IOM0.DDRPHY_PC_BASE_CNTR0_P3
Address	8000C00407011C3F (SCOM)
Description	This register generates a periodic one-clock-cycle enable signal for the PC Periodic Base Counter 1 Register. This register is the first of three cascaded counters.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	ROX	PERIODIC_BASE_CNTR0: Periodic base counter 0. When enabled via PERIODIC_CAL_REQ_EN in the PC Periodic Reload Value 0 Register, the counter is free running (counts every dphy_gckn clock cycle). When this counter rolls over, it is reloaded with the value {PERIODIC_RELOAD_VALUE0 & 0} from the PC Periodic Reload Value 0 Register. This counter enables the PC Periodic Base Counter 1 for one count (one dphy_gckn clock cycle) every (PERIODIC_RELOAD_VALUE0 x 2) + 1 dphy_gckn cycles. This counter is used by internal state machines during initial calibration and periodic calibrations. Therefore, during initial calibrations and periodic calibrations, the read value of this register is undefined.

Register Name	PC Periodic Reload Value 0 Register
Mnemonic	IOM0.DDRPHY_PC_RELOAD_VALUE0_P0
Address	8000C0050701103F (SCOM)
Description	The value in this register is loaded into PC Periodic Base Counter 0 when it rolls over.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	PERIODIC_CAL_REQ_EN: 1 = Enable periodic calibration request generation from the PHY. 0 = Disable periodic calibration request generation from the PHY.
49:63	RW	PERIODIC_RELOAD_VALUE0: Periodic reload value 0. This value is loaded into bits 0 - 14 of the PC Periodic Base Counter 0 when it rolls over. Bit 15 is always loaded with 0b when it rolls over. When this field is written to zero and the PERIODIC_CAL_REQ_EN is set to 1b, exactly one periodic calibration (MEMCTLCPURO) is requested by the DDR PHY core.

Register Name	PC Periodic Reload Value 0 Register
Mnemonic	IOM0.DDRPHY_PC_RELOAD_VALUE0_P1
Address	8000C0050701143F (SCOM)
Description	The value in this register is loaded into PC Periodic Base Counter 0 when it rolls over.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	PERIODIC_CAL_REQ_EN: 1 = Enable periodic calibration request generation from the PHY. 0 = Disable periodic calibration request generation from the PHY.
49:63	RW	PERIODIC_RELOAD_VALUE0: Periodic reload value 0. This value is loaded into bits 0 - 14 of the PC Periodic Base Counter 0 when it rolls over. Bit 15 is always loaded with 0b when it rolls over. When this field is written to zero and the PERIODIC_CAL_REQ_EN is set to 1b, exactly one periodic calibration (MEMCTLCPURO) is requested by the DDR PHY core.

Register Name	PC Periodic Reload Value 0 Register
Mnemonic	IOM0.DDRPHY_PC_RELOAD_VALUE0_P2
Address	8000C0050701183F (SCOM)
Description	The value in this register is loaded into PC Periodic Base Counter 0 when it rolls over.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	PERIODIC_CAL_REQ_EN: 1 = Enable periodic calibration request generation from the PHY. 0 = Disable periodic calibration request generation from the PHY.
49:63	RW	PERIODIC_RELOAD_VALUE0: Periodic reload value 0. This value is loaded into bits 0 - 14 of the PC Periodic Base Counter 0 when it rolls over. Bit 15 is always loaded with 0b when it rolls over. When this field is written to zero and the PERIODIC_CAL_REQ_EN is set to 1b, exactly one periodic calibration (MEMCTLCPURO) is requested by the DDR PHY core.

Register Name	PC Periodic Reload Value 0 Register
Mnemonic	IOM0.DDRPHY_PC_RELOAD_VALUE0_P3
Address	8000C00507011C3F (SCOM)
Description	The value in this register is loaded into PC Periodic Base Counter 0 when it rolls over.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	PERIODIC_CAL_REQ_EN: 1 = Enable periodic calibration request generation from the PHY. 0 = Disable periodic calibration request generation from the PHY.
49:63	RW	PERIODIC_RELOAD_VALUE0: Periodic reload value 0. This value is loaded into bits 0 - 14 of the PC Periodic Base Counter 0 when it rolls over. Bit 15 is always loaded with 0b when it rolls over. When this field is written to zero and the PERIODIC_CAL_REQ_EN is set to 1b, exactly one periodic calibration (MEMCTLCPURO) is requested by the DDR PHY core.

Register Name	PC Periodic Base Counter 1 Register
Mnemonic	IOM0.DDRPHY_PC_BASE_CNTR1_P0
Address	8000C0060701103F (SCOM)
Description	This register generates a periodic one-clock-cycle enable signal for the PC Periodic Calibration Timer. This register is the second of three cascaded counters.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	ROX	PERIODIC_BASE_CNTR1: Periodic base counter 1. This counter is enabled for one dphy_gckn clock cycle (1 count) each time the PC Periodic Base Counter 0 Register performs one counting sequence. When this counter rolls over and the FAST_SIM_PER_CNTR bit is not set in the PC Periodic Calibration Configuration Register, it is reloaded with the value FFFFh. This register enables the PC Periodic Calibration Timer Register and the PC Periodic Impedance Calibration Timer Register every (216 -1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) dphy_gckn clock cycles. When this counter rolls over and the FAST_SIM_PER_CNTR bit is set in the PC Periodic Calibration Configuration Register, it is reloaded with the value 00FFh. When the FAST_SIM_PER_CNTR bit is set in the PC Periodic Calibration Configuration Register, this register enables the PC Periodic Calibration Timer and the PC Periodic Impedance Calibration Timer every (28 -1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) dphy_gckn clock cycles.

Register Name	PC Periodic Base Counter 1 Register
Mnemonic	IOM0.DDRPHY_PC_BASE_CNTR1_P1
Address	8000C0060701143F (SCOM)
Description	This register generates a periodic one-clock-cycle enable signal for the PC Periodic Calibration Timer. This register is the second of three cascaded counters.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	ROX	PERIODIC_BASE_CNTR1: Periodic base counter 1. This counter is enabled for one dphy_gckn clock cycle (1 count) each time the PC Periodic Base Counter 0 Register performs one counting sequence. When this counter rolls over and the FAST_SIM_PER_CNTR bit is not set in the PC Periodic Calibration Configuration Register, it is reloaded with the value FFFFh. This register enables the PC Periodic Calibration Timer Register and the PC Periodic Impedance Calibration Timer Register every (216 -1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) dphy_gckn clock cycles. When this counter rolls over and the FAST_SIM_PER_CNTR bit is set in the PC Periodic Calibration Configuration Register, it is reloaded with the value 00FFh. When the FAST_SIM_PER_CNTR bit is set in the PC Periodic Calibration Configuration Register, this register enables the PC Periodic Calibration Timer and the PC Periodic Impedance Calibration Timer every (28 -1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) dphy_gckn clock cycle

Register Name	PC Periodic Base Counter 1 Register
Mnemonic	IOM0.DDRPHY_PC_BASE_CNTR1_P2
Address	8000C0060701183F (SCOM)
Description	This register generates a periodic one-clock-cycle enable signal for the PC Periodic Calibration Timer. This register is the second of three cascaded counters.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	ROX	PERIODIC_BASE_CNTR1: Periodic base counter 1. This counter is enabled for one dphy_gckn clock cycle (1 count) each time the PC Periodic Base Counter 0 Register performs one counting sequence. When this counter rolls over and the FAST_SIM_PER_CNTR bit is not set in the PC Periodic Calibration Configuration Register, it is reloaded with the value FFFFh. This register enables the PC Periodic Calibration Timer Register and the PC Periodic Impedance Calibration Timer Register every (216 -1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) dphy_gckn clock cycles. When this counter rolls over and the FAST_SIM_PER_CNTR bit is set in the PC Periodic Calibration Configuration Register, it is reloaded with the value 00FFh. When the FAST_SIM_PER_CNTR bit is set in the PC Periodic Calibration Configuration Register, this register enables the PC Periodic Calibration Timer and the PC Periodic Impedance Calibration Timer every (28 -1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) dphy_gckn clock cycle.

Register Name	PC Periodic Base Counter 1 Register
Mnemonic	IOM0.DDRPHY_PC_BASE_CNTR1_P3
Address	8000C00607011C3F (SCOM)
Description	This register generates a periodic one-clock-cycle enable signal for the PC Periodic Calibration Timer. This register is the second of three cascaded counters.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	ROX	PERIODIC_BASE_CNTR1: Periodic base counter 1. This counter is enabled for one dphy_gckn clock cycle (1 count) each time the PC Periodic Base Counter 0 Register performs one counting sequence. When this counter rolls over and the FAST_SIM_PER_CNTR bit is not set in the PC Periodic Calibration Configuration Register, it is reloaded with the value FFFFh. This register enables the PC Periodic Calibration Timer Register and the PC Periodic Impedance Calibration Timer Register every (216 -1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) dphy_gckn clock cycles. When this counter rolls over and the FAST_SIM_PER_CNTR bit is set in the PC Periodic Calibration Configuration Register, it is reloaded with the value 00FFh. When the FAST_SIM_PER_CNTR bit is set in the PC Periodic Calibration Configuration Register, this register enables the PC Periodic Calibration Timer and the PC Periodic Impedance Calibration Timer every (28 -1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) dphy_gckn clock cycle

Register Name	PC Periodic Calibration Timer Register
Mnemonic	IOM0.DDRPHY_PC_CAL_TIMER_P0
Address	8000C0070701103F (SCOM)
Description	This register generates a periodic calibration request (Update Request) on the memory controller (MEMCTL) interface by the PHY.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	ROX	PERIODIC_CAL_TIMER: Periodic calibration timer. This counter is enabled for one dphy_gckn clock cycle (1 count) each time the PC Periodic Base Counter 1 Register performs one counting sequence. When this counter rolls over, it is reloaded with the PERIODIC_TIMER_RELOAD_VALUE from the PC Periodic Calibration Timer Reload Value Register. This register requests a periodic calibration (MEMCTLCPURO) every (216 - 1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) x (PERIODIC_TIMER_RELOAD_VALUE - 1) dphy_gckn clock cycles. When the FAST_SIM_PER_CNTR bit is set in the PC Periodic Calibration Configuration Register, this register requests a periodic calibration (MEMCTLCPURO) every (28 - 1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) x (PERIODIC_TIMER_RELOAD_VALUE - 1) dphy_gckn clock cycles. **Note:** The periodic calibration is performed on one rank for each request. Therefore, if a memory system has four rank pairs, four requests must occur before all rank pairs have received one periodic calibration.

Register Name	PC Periodic Calibration Timer Register
Mnemonic	IOM0.DDRPHY_PC_CAL_TIMER_P1
Address	8000C0070701143F (SCOM)
Description	This register generates a periodic calibration request (Update Request) on the MEMCTL interface by the PHY.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	ROX	PERIODIC_CAL_TIMER: Periodic calibration timer. This counter is enabled for one dphy_gckn clock cycle (1 count) each time the PC Periodic Base Counter 1 Register performs one counting sequence. When this counter rolls over, it is reloaded with the PERIODIC_TIMER_RELOAD_VALUE from the PC Periodic Calibration Timer Reload Value Register. This register requests a periodic calibration (MEMCTLCPURO) every (216 - 1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) x (PERIODIC_TIMER_RELOAD_VALUE - 1) dphy_gckn clock cycles. When the FAST_SIM_PER_CNTR bit is set in the PC Periodic Calibration Configuration Register, this register requests a periodic calibration (MEMCTLCPURO) every (28 - 1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) x (PERIODIC_TIMER_RELOAD_VALUE - 1) dphy_gckn clock cycles. **Note:** The periodic calibration is performed on one rank for each request. Therefore, if a memory system has four rank pairs, four requests must occur before all rank pairs have received one periodic calibration.

Register Name	PC Periodic Calibration Timer Register
Mnemonic	IOM0.DDRPHY_PC_CAL_TIMER_P2
Address	8000C0070701183F (SCOM)
Description	This register generates a periodic calibration request (Update Request) on the MEMCTL interface by the PHY.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	ROX	PERIODIC_CAL_TIMER: Periodic calibration timer. This counter is enabled for one dphy_gckn clock cycle (1 count) each time the PC Periodic Base Counter 1 Register performs one counting sequence. When this counter rolls over, it is reloaded with the PERIODIC_TIMER_RELOAD_VALUE from the PC Periodic Calibration Timer Reload Value Register. This register requests a periodic calibration (MEMCTLCPURO) every (216 - 1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) x (PERIODIC_TIMER_RELOAD_VALUE - 1) dphy_gckn clock cycles. When the FAST_SIM_PER_CNTR bit is set in the PC Periodic Calibration Configuration Register, this register requests a periodic calibration (MEMCTLCPURO) every (28 - 1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) x (PERIODIC_TIMER_RELOAD_VALUE - 1) dphy_gckn clock cycles. **Note:** The periodic calibration is performed on one rank for each request. Therefore, if a memory system has four rank pairs, four requests must occur before all rank pairs have received one periodic calibration.

Register Name	PC Periodic Calibration Timer Register
Mnemonic	IOM0.DDRPHY_PC_CAL_TIMER_P3
Address	8000C00707011C3F (SCOM)
Description	This register generates a periodic calibration request (Update Request) on the MEMCTL interface by the PHY.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	ROX	PERIODIC_CAL_TIMER: Periodic calibration timer. This counter is enabled for one dphy_gckn clock cycle (1 count) each time the PC Periodic Base Counter 1 Register performs one counting sequence. When this counter rolls over, it is reloaded with the PERIODIC_TIMER_RELOAD_VALUE from the PC Periodic Calibration Timer Reload Value Register. This register requests a periodic calibration (MEMCTLCPURO) every (216 - 1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) x (PERIODIC_TIMER_RELOAD_VALUE - 1) dphy_gckn clock cycles. When the FAST_SIM_PER_CNTR bit is set in the PC Periodic Calibration Configuration Register, this register requests a periodic calibration (MEMCTLCPURO) every (28 - 1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) x (PERIODIC_TIMER_RELOAD_VALUE - 1) dphy_gckn clock cycles. **Note:** The periodic calibration is performed on one rank for each request. Therefore, if a memory system has four rank pairs, four requests must occur before all rank pairs have received one periodic calibration.

Register Name	PC Periodic Calibration Timer Reload Value Register
Mnemonic	IOM0.DDRPHY_PC_CAL_TIMER_RELOAD_VALUE_P0
Address	8000C0080701103F (SCOM)
Description	The value in this register is loaded into the PC Periodic Calibration Timer when it rolls over.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	PERIODIC_TIMER_RELOAD_VALUE: Periodic reload value 0. This value is loaded into the PC periodic calibration timer when it rolls over. This register must be set to a value greater than or equal to 2.

Register Name	PC Periodic Calibration Timer Reload Value Register
Mnemonic	IOM0.DDRPHY_PC_CAL_TIMER_RELOAD_VALUE_P1
Address	8000C0080701143F (SCOM)
Description	The value in this register is loaded into the PC Periodic Calibration Timer when it rolls over.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	PERIODIC_TIMER_RELOAD_VALUE: Periodic reload value 0. This value is loaded into the PC periodic calibration timer when it rolls over. This register must be set to a value greater than or equal to 2.

Register Name	PC Periodic Calibration Timer Reload Value Register
Mnemonic	IOM0.DDRPHY_PC_CAL_TIMER_RELOAD_VALUE_P2
Address	8000C0080701183F (SCOM)
Description	The value in this register is loaded into the PC Periodic Calibration Timer when it rolls over.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	PERIODIC_TIMER_RELOAD_VALUE: Periodic reload value 0. This value is loaded into the PC periodic calibration timer when it rolls over. This register must be set to a value greater than or equal to 2.

Register Name	PC Periodic Calibration Timer Reload Value Register
Mnemonic	IOM0.DDRPHY_PC_CAL_TIMER_RELOAD_VALUE_P3
Address	8000C00807011C3F (SCOM)
Description	The value in this register is loaded into the PC Periodic Calibration Timer when it rolls over.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	PERIODIC_TIMER_RELOAD_VALUE: Periodic reload value 0. This value is loaded into the PC periodic calibration timer when it rolls over. This register must be set to a value greater than or equal to 2.

Register Name	PC Periodic Impedance Calibration Timer Register
Mnemonic	IOM0.DDRPHY_PC_ZCAL_TIMER_P0
Address	8000C0090701103F (SCOM)
Description	This register generates a periodic external impedance calibration request on the memory controller (MEMCTL) interface.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	ROX	PERIODIC_ZCAL_TIMER: Periodic external impedance calibration timer. This counter is enabled for one dphy_gckn clock cycle (1 count) each time the PC Periodic Base Counter 1 Register performs one counting sequence. When this counter rolls over, it is reloaded with the value PERIODIC_ZCAL_TIMER_RELOAD_VALUE from the PC Periodic Impedance Calibration Timer Reload Value Register. This register requests a periodic impedance calibration (ZCNTLCPURO) every (216 - 1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) x (PERIODIC_ZCAL_TIMER_RELOAD_VALUE - 1) dphy_gckn clock cycles. When the FAST_SIM_PER_CNTR bit is set in the PC Periodic Calibration Configuration Register, this register requests a periodic impedance calibration (ZCNTLCPURO) every (28 - 1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) x (PERIODIC_ZCAL_TIMER_RELOAD_VALUE - 1) dphy_gckn clock cycles. **Note:** The periodic external impedance calibration is performed on one rank for each request. Therefore, if a memory system has four ranks, four requests must occur before all ranks have received one periodic impedance calibration.

Register Name	PC Periodic Impedance Calibration Timer Register
Mnemonic	IOM0.DDRPHY_PC_ZCAL_TIMER_P1
Address	8000C0090701143F (SCOM)
Description	This register generates a periodic external impedance calibration request on the memory controller (MEMCTL) interface.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	ROX	PERIODIC_ZCAL_TIMER: Periodic external impedance calibration timer. This counter is enabled for one dphy_gckn clock cycle (1 count) each time the PC Periodic Base Counter 1 Register performs one counting sequence. When this counter rolls over, it is reloaded with the value PERIODIC_ZCAL_TIMER_RELOAD_VALUE from the PC Periodic Impedance Calibration Timer Reload Value Register. This register requests a periodic impedance calibration (ZCNTLCPURO) every (216 - 1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) x (PERIODIC_ZCAL_TIMER_RELOAD_VALUE - 1) dphy_gckn clock cycles. When the FAST_SIM_PER_CNTR bit is set in the PC Periodic Calibration Configuration Register, this register requests a periodic impedance calibration (ZCNTLCPURO) every (28 - 1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) x (PERIODIC_ZCAL_TIMER_RELOAD_VALUE - 1) dphy_gckn clock cycles. **Note:** The periodic external impedance calibration is performed on one rank for each request. Therefore, if a memory system has four ranks, four requests must occur before all ranks have received one periodic impedance calibration.

Register Name	PC Periodic Impedance Calibration Timer Register
Mnemonic	IOM0.DDRPHY_PC_ZCAL_TIMER_P2
Address	8000C0090701183F (SCOM)
Description	This register generates a periodic external impedance calibration request on the memory controller (MEMCTL) interface.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	ROX	PERIODIC_ZCAL_TIMER: Periodic external impedance calibration timer. This counter is enabled for one dphy_gckn clock cycle (1 count) each time the PC Periodic Base Counter 1 Register performs one counting sequence. When this counter rolls over, it is reloaded with the value PERIODIC_ZCAL_TIMER_RELOAD_VALUE from the PC Periodic Impedance Calibration Timer Reload Value Register. This register requests a periodic impedance calibration (ZCNTLCPURO) every (216 - 1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) x (PERIODIC_ZCAL_TIMER_RELOAD_VALUE - 1) dphy_gckn clock cycles. When the FAST_SIM_PER_CNTR bit is set in the PC Periodic Calibration Configuration Register, this register requests a periodic impedance calibration (ZCNTLCPURO) every (28 - 1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) x (PERIODIC_ZCAL_TIMER_RELOAD_VALUE - 1) dphy_gckn clock cycles. **Note:** The periodic external impedance calibration is performed on one rank for each request. Therefore, if a memory system has four ranks, four requests must occur before all ranks have received one periodic impedance calibration.

Register Name	PC Periodic Impedance Calibration Timer Register
Mnemonic	IOM0.DDRPHY_PC_ZCAL_TIMER_P3
Address	8000C00907011C3F (SCOM)
Description	This register generates a periodic external impedance calibration request on the memory controller (MEMCTL) interface.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	ROX	PERIODIC_ZCAL_TIMER: Periodic external impedance calibration timer. This counter is enabled for one dphy_gckn clock cycle (1 count) each time the PC Periodic Base Counter 1 Register performs one counting sequence. When this counter rolls over, it is reloaded with the value PERIODIC_ZCAL_TIMER_RELOAD_VALUE from the PC Periodic Impedance Calibration Timer Reload Value Register. This register requests a periodic impedance calibration (ZCNTLCPURO) every (216 - 1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) x (PERIODIC_ZCAL_TIMER_RELOAD_VALUE - 1) dphy_gckn clock cycles. When the FAST_SIM_PER_CNTR bit is set in the PC Periodic Calibration Configuration Register, this register requests a periodic impedance calibration (ZCNTLCPURO) every (28 - 1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) x (PERIODIC_ZCAL_TIMER_RELOAD_VALUE - 1) dphy_gckn clock cycles. **Note:** The periodic external impedance calibration is performed on one rank for each request. Therefore, if a memory system has four ranks, four requests must occur before all ranks have received one periodic impedance calibration.

Register Name	PC Periodic Impedance Calibration Timer Reload Value Register
Mnemonic	IOM0.DDRPHY_PC_ZCAL_TIMER_RELOAD_VALUE_P0
Address	8000C00A0701103F (SCOM)
Description	The value in this register is loaded into the PC Periodic Impedance Calibration Timer when it rolls over.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	PERIODIC_TIMER_RELOAD_VALUE: Periodic external impedance calibration timer reload value. This value is loaded into the PC Periodic Impedance Calibration Timer when it rolls over. The register must be set to a value greater than or equal to 2.

Register Name	PC Periodic Impedance Calibration Timer Reload Value Register
Mnemonic	IOM0.DDRPHY_PC_ZCAL_TIMER_RELOAD_VALUE_P1
Address	8000C00A0701143F (SCOM)
Description	The value in this register is loaded into the PC Periodic Impedance Calibration Timer when it rolls over.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	PERIODIC_TIMER_RELOAD_VALUE: Periodic external impedance calibration timer reload value. This value is loaded into the PC Periodic Impedance Calibration Timer when it rolls over. The register must be set to a value greater than or equal to 2.

Register Name	PC Periodic Impedance Calibration Timer Reload Value Register
Mnemonic	IOM0.DDRPHY_PC_ZCAL_TIMER_RELOAD_VALUE_P2
Address	8000C00A0701183F (SCOM)
Description	The value in this register is loaded into the PC Periodic Impedance Calibration Timer when it rolls over.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	PERIODIC_TIMER_RELOAD_VALUE: Periodic external impedance calibration timer reload value. This value is loaded into the PC Periodic Impedance Calibration Timer when it rolls over. The register must be set to a value greater than or equal to 2.

Register Name	PC Periodic Impedance Calibration Timer Reload Value Register
Mnemonic	IOM0.DDRPHY_PC_ZCAL_TIMER_RELOAD_VALUE_P3
Address	8000C00A07011C3F (SCOM)
Description	The value in this register is loaded into the PC Periodic Impedance Calibration Timer when it rolls over.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	PERIODIC_TIMER_RELOAD_VALUE: Periodic external impedance calibration timer reload value. This value is loaded into the PC Periodic Impedance Calibration Timer when it rolls over. The register must be set to a value greater than or equal to 2.

Register Name	PC Periodic Calibration Configuration Register
Mnemonic	IOM0.DDRPHY_PC_PER_CAL_CONFIG_P0
Address	8000C00B0701103F (SCOM)
Description	This register controls the periodic calibration logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	PER_ENA_RANK_PAIR: 1 = Periodic calibration is enabled. 0 = Periodic calibration is disabled. Bit 48 contains the enable bit for rank pair 0. Bit 49 contains the enable bit for rank pair 1. Bit 50 contains the enable bit for rank pair 2. Bit 51 contains the enable bit for rank pair 3.
52	RW	PER_ENA_ZCAL: Enables the periodic external impedance calibration logic.
53	RW	PER_ENA_SYSCLK_ALIGN: Enables the periodic alignment of the internal SYSCLK with the memory controller clock (dphy_gckn/SYSCLK alignment).
54	RW	ENA_PER_READ_CTR: 1 = Enable the updating of the DP16 Read Delay Value {0-11} Registers during periodic read centering. 0 = Prevent the updating of the DP16 Read Delay Value {0-11} Registers during periodic read centering.
55	RW	ENA_PER_RDCLK_ALIGN: 1 = Enable the updating of the DP16 DQS Read Phase Select Register at the conclusion of periodic read centering on a nibble of data (DQ) lanes. 0 = Prevent the updating of the DP16 DQS Read Phase Select Register at the conclusion of periodic read centering on a nibble of DQ lanes.
56	RW	ENA_PER_DQS_ALIGN: Enables periodic alignment of the data strobes (DQSs) (read) from memory to the internally generated DQS strobes (DQS alignment).
57:58	RWX	PER_NEXT_RANK_PAIR: Indicates which rank pair is scheduled for the next periodic calibration operation. This field is updated by the PHY as it sequences through periodic calibrations on each enabled rank pair. This field must equal one of the rank pair numbers enabled in the PER_ENA_RANK_PAIR field when at least one rank pair is enabled in the PER_ENA_RANK_PAIR field.

Bits	SCOM	Field Mnemonic: Description
59	RW	FAST_SIM_PER_CNTR: This bit must be 0b in hardware. This bit is a method for behavioral simulations to reduce the time between periodic calibrations. A 1b causes the PC Periodic Base Counter 1 Register to roll over to 00FFh. A 0b has no effect on the behavior of the PC Periodic Base Counter 1 Register.
60	RW	START_INIT_CAL: When this bit is written to 1b, the DDR PHY initiates an initial calibration for all ranks enabled in the PC Initial Calibration Config0 Register. When this bit is written to 0b, no action is taken by the DDR PHY. When read, this bit always returns the last value written.
61	RW	START_PER_CAL: When this bit is written to 1b, the DDR PHY initiates a single periodic calibration (equivalent to a periodic timer pop). When this bit is written to 0b, no action is taken by the DDR PHY. When read, this bit always returns the last value written.
62	RW	ABORT_ON_ERR_EN: Periodic calibration abort on error enable. 1 = Enable the detection of the pc_errn_in. 0 = Disable the detection of the pc_errn_in.
63	RW	DD2_FIX_DIS: 1 = Disable CDD2 fixes. 0 = Normal operation.

Register Name	PC Periodic Calibration Configuration Register
Mnemonic	IOM0.DDRPHY_PC_PER_CAL_CONFIG_P1
Address	8000C00B0701143F (SCOM)
Description	This register controls the periodic calibration logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	PER_ENA_RANK_PAIR: 1 = Periodic calibration is enabled. 0 = Periodic calibration is disabled. Bit 48 contains the enable bit for rank pair 0. Bit 49 contains the enable bit for rank pair 1. Bit 50 contains the enable bit for rank pair 2. Bit 51 contains the enable bit for rank pair 3.
52	RW	PER_ENA_ZCAL: Enables the periodic external impedance calibration logic.
53	RW	PER_ENA_SYSCLK_ALIGN: Enables the periodic alignment of the internal SYSCLK with the memory controller clock (dphy_gckn/SYSCLK alignment).
54	RW	ENA_PER_READ_CTR: 1 = Enable the updating of the DP16 Read Delay Value {0-11} Registers during periodic read centering. 0 = Prevent the updating of the DP16 Read Delay Value {0-11} Registers during periodic read centering.
55	RW	ENA_PER_RDCLK_ALIGN: 1 = Enable the updating of the DP16 DQS Read Phase Select Register at the conclusion of periodic read centering on a nibble of DQ lanes. 0 = Prevent the updating of the DP16 DQS Read Phase Select Register at the conclusion of periodic read centering on a nibble of DQ lanes.
56	RW	ENA_PER_DQS_ALIGN: Enables periodic alignment of the DQS (read) strobes from memory to the internally generated DQS strobes (DQS alignment).

Bits	SCOM	Field Mnemonic: Description
57:58	RWX	PER_NEXT_RANK_PAIR: Indicates which rank pair is scheduled for the next periodic calibration operation. This field is updated by the PHY as it sequences through periodic calibrations on each enabled rank pair. This field must equal one of the rank pair numbers enabled in the PER_ENA_RANK_PAIR field when at least one rank pair is enabled in the PER_ENA_RANK_PAIR field.
59	RW	FAST_SIM_PER_CNTR: This bit must be 0b in hardware. This bit is a method for behavioral simulations to reduce the time between periodic calibrations. A 1b causes the PC Periodic Base Counter 1 Register to roll over to 00FFh. A 0b has no effect on the behavior of the PC Periodic Base Counter 1 Register.
60	RW	START_INIT_CAL: When this bit is written to 1b, the DDR PHY initiates an initial calibration for all ranks enabled in the PC Initial Calibration Config0 Register. When this bit is written to 0b, no action is taken by the DDR PHY. When read, this bit always returns the last value written.
61	RW	START_PER_CAL: When this bit is written to 1b, the DDR PHY initiates a single periodic calibration (equivalent to a periodic timer pop). When this bit is written to 0b, no action is taken by the DDR PHY. When read, this bit always returns the last value written.
62	RW	ABORT_ON_ERR_EN: Periodic calibration abort on error enable. 1 = Enable the detection of the pc_errn_in. 0 = Disable the detection of the pc_errn_in.
63	RW	DD2_FIX_DIS: 1 = Disable CDD2 fixes. 0 = Normal operation.

Register Name	PC Periodic Calibration Configuration Register
Mnemonic	IOM0.DDRPHY_PC_PER_CAL_CONFIG_P2
Address	8000C00B0701183F (SCOM)
Description	This register controls the periodic calibration logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	PER_ENA_RANK_PAIR: 1 = Periodic calibration is enabled. 0 = Periodic calibration is disabled. Bit 48 contains the enable bit for rank pair 0. Bit 49 contains the enable bit for rank pair 1. Bit 50 contains the enable bit for rank pair 2. Bit 51 contains the enable bit for rank pair 3.
52	RW	PER_ENA_ZCAL: Enables the periodic external impedance calibration logic.
53	RW	PER_ENA_SYSCLK_ALIGN: Enables the periodic alignment of the internal SYSCLK with the memory controller clock (dphy_gckn/SYSCLK alignment).
54	RW	ENA_PER_READ_CTR: 1 = Enable the updating of the DP16 Read Delay Value {0-11} Registers during periodic read centering. 0 = Prevent the updating of the DP16 Read Delay Value {0-11} Registers during periodic read centering.
55	RW	ENA_PER_RDCLK_ALIGN: 1 = Enable the updating of the DP16 DQS Read Phase Select Register at the conclusion of periodic read centering on a nibble of DQ lanes. 0 = Prevent the updating of the DP16 DQS Read Phase Select Register at the conclusion of periodic read centering on a nibble of DQ lanes.

Bits	SCOM	Field Mnemonic: Description
56	RW	ENA_PER_DQS_ALIGN: Enables periodic alignment of the DQS (read) strobes from memory to the internally generated DQS strobes (DQS alignment).
57:58	RWX	PER_NEXT_RANK_PAIR: Indicates which rank pair is scheduled for the next periodic calibration operation. This field is updated by the PHY as it sequences through periodic calibrations on each enabled rank pair. This field must equal one of the rank pair numbers enabled in the PER_ENA_RANK_PAIR field when at least one rank pair is enabled in the PER_ENA_RANK_PAIR field.
59	RW	FAST_SIM_PER_CNTR: This bit must be 0b in hardware. This bit is a method for behavioral simulations to reduce the time between periodic calibrations. A 1b causes the PC Periodic Base Counter 1 Register to roll over to 00FFh. A 0b has no effect on the behavior of the PC Periodic Base Counter 1 Register.
60	RW	START_INIT_CAL: When this bit is written to 1b, the DDR PHY initiates an initial calibration for all ranks enabled in the PC Initial Calibration Config0 Register. When this bit is written to 0b, no action is taken by the DDR PHY. When read, this bit always returns the last value written.
61	RW	START_PER_CAL: When this bit is written to 1b, the DDR PHY initiates a single periodic calibration (equivalent to a periodic timer pop). When this bit is written to 0b, no action is taken by the DDR PHY. When read, this bit always returns the last value written.
62	RW	ABORT_ON_ERR_EN: Periodic calibration abort on error enable. 1 = Enable the detection of the pc_errn_in. 0 = Disable the detection of the pc_errn_in.
63	RW	DD2_FIX_DIS: 1 = Disable CDD2 fixes. 0 = Normal operation.

Register Name	PC Periodic Calibration Configuration Register
Mnemonic	IOM0.DDRPHY_PC_PER_CAL_CONFIG_P3
Address	8000C00B07011C3F (SCOM)
Description	This register controls the periodic calibration logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	PER_ENA_RANK_PAIR: 1 = Periodic calibration is enabled. 0 = Periodic calibration is disabled. Bit 48 contains the enable bit for rank pair 0. Bit 49 contains the enable bit for rank pair 1. Bit 50 contains the enable bit for rank pair 2. Bit 51 contains the enable bit for rank pair 3.
52	RW	PER_ENA_ZCAL: Enables the periodic external impedance calibration logic.
53	RW	PER_ENA_SYSCLK_ALIGN: Enables the periodic alignment of the internal SYSCLK with the memory controller clock (dphy_gckn/SYSCLK alignment).
54	RW	ENA_PER_READ_CTR: 1 = Enable the updating of the DP16 Read Delay Value {0-11} Registers during periodic read centering. 0 = Prevent the updating of the DP16 Read Delay Value {0-11} Registers during periodic read centering.

Bits	SCOM	Field Mnemonic: Description
55	RW	ENA_PER_RDCLK_ALIGN: 1 = Enable the updating of the DP16 DQS Read Phase Select Register at the conclusion of periodic read centering on a nibble of DQ lanes. 0 = Prevent the updating of the DP16 DQS Read Phase Select Register at the conclusion of periodic read centering on a nibble of DQ lanes.
56	RW	ENA_PER_DQS_ALIGN: Enables periodic alignment of the DQS (read) strobes from memory to the internally generated DQS strobes (DQS alignment).
57:58	RWX	PER_NEXT_RANK_PAIR: Indicates which rank pair is scheduled for the next periodic calibration operation. This field is updated by the PHY as it sequences through periodic calibrations on each enabled rank pair. This field must equal one of the rank pair numbers enabled in the PER_ENA_RANK_PAIR field when at least one rank pair is enabled in the PER_ENA_RANK_PAIR field.
59	RW	FAST_SIM_PER_CNTR: This bit must be 0b in hardware. This bit is a method for behavioral simulations to reduce the time between periodic calibrations. A 1b causes the PC Periodic Base Counter 1 Register to roll over to 00FFh. A 0b has no effect on the behavior of the PC Periodic Base Counter 1 Register.
60	RW	START_INIT_CAL: When this bit is written to 1b, the DDR PHY initiates an initial calibration for all ranks enabled in the PC Initial Calibration Config0 Register. When this bit is written to 0b, no action is taken by the DDR PHY. When read, this bit always returns the last value written.
61	RW	START_PER_CAL: When this bit is written to 1b, the DDR PHY initiates a single periodic calibration (equivalent to a periodic timer pop). When this bit is written to 0b, no action is taken by the DDR PHY. When read, this bit always returns the last value written.
62	RW	ABORT_ON_ERR_EN: Periodic calibration abort on error enable. 1 = Enable the detection of the pc_errn_in. 0 = Disable the detection of the pc_errn_in.
63	RW	DD2_FIX_DIS: 1 = Disable CDD2 fixes. 0 = Normal operation.

Register Name	PC Configuration 0 Register
Mnemonic	IOM0.DDRPHY_PC_CONFIG0_P0
Address	8000C00C0701103F (SCOM)
Description	This register contains global configuration information that describes the characteristics of the memory modules and characteristics of the system design.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	PDA_ENABLE_OVERRIDE: Enables PDA mode on a rank pair basis by overriding the snooped value of bit 4 in the PC Mode 3 Register (MR3). Required in certain DIMM configurations. Bit 48 overrides rank pair 0 MR3 bit 4 PDA enable. Bit 49 overrides rank pair 1 MR3 bit 4 PDA enable. Bit 50 overrides rank pair 2 MR3 bit 4 PDA enable. Bit 51 overrides rank pair 3 MR3 bit 4 PDA enable. 0 = PDA under MR3 bit 4 control. 1 = PDA enable.
52	RW	2TCK_PREAMBLE_ENABLE: 0 = 1tCK preamble for write and read traffic. 1 = 2tCK preamble for write and read traffic. **Note:** Calibration steps always use 1tCK preamble.

Bits	SCOM	Field Mnemonic: Description
53	RW	PBA_ENABLE: LRDIMM PBA enable. 0 = Disable per-buffer addressability (PBA). 1 = Enable PBA, which snoops buffer control word (BCW) writes and drives DQ/DQS.
54	RW	DDR4_CMD_SIG_REDUCTION: In DDR4, to enable the DDR4 command/address signal-reduction feature, this value must be set to 1b. 0 = The PHY does not decode the ACT# DDR command signal. 1 = The PHY monitors and drives the DDR4 ACT# (activate) signal. Address pins A15, A14, and A13 are not monitored. When the DDR PHY drives an activate command, A15, A14, and A13 are driven onto RAS#, CAS#, and WE#.
55	RW	SYSCLK_2X_MEMINTCLKO: 0 = The internal SYSCLK frequency equals the memory interface clock (MEMINTCLKO) frequency. 1 = Not supported.
56	RW	RANK_OVERRIDE: Rank override mode. 0 = The DDR PHY uses the rank number (chip select) provided by the memory controller on the MEMCTL interface to determine the rank pair and hence the configuration registers for each read or write command. 1 = The DDR PHY uses the rank number provided in the RANK_OVERRIDE_VALUE field of this register to determine the rank pair and hence the configuration registers for all read/write commands regardless of the rank number (chip select) provided by the memory controller on the MEMCTL interface. When this bit is 1b, the following assumptions and restrictions apply: All ranks must be of the same configuration. (That is, all x4 or all x8.) Only the rank specified in RANK_OVERRIDE_VALUE can be calibrated. Calibrating other ranks causes an undefined behavior.
57:59	RW	RANK_OVERRIDE_VALUE: Rank override value. 000 = Rank 0 001 = Rank 1 010 = Rank 2 011 = Rank 3 All other settings are reserved.
60	RW	LOW_LATENCY: 0 = Early read start (ERS) mode on/off is determined by the CL value. When CL = 5 or 6, ERS mode is automatically off. Otherwise, ERS mode is automatically on. 1 = Force ERS mode off.
61	RW	DDR4_IPW_LOOP_DIS: When the MEMORY_TYPE field in the PC Configuration 1 Register equals 1XXX (for example, DDR4 RDIMM), initial pattern write (IPW) to Multipurpose Register (MPR) requires that Side A and Side B DRAMs be written separately. IPW loops to write both sides for this memory type. This bit can disable this behavior, in which case Side A/B selection can be manually controlled in the SEQ Configuration 0 Register. 0 = Normal operation. IPW loops over both sides. 1 = IPW loop behavior is disabled. This bit must be set to 1 if the FORCE_RESERVED bit is set in the SEQ Configuration 0 Register. This bit is not used for other memory types.
62	RW	DDR4_VLEVEL_BANK_GROUP: Must be set to `1'b. 0 = Disable voltage level and bank group arch. 1 = Enable voltage level and bank group arch.
63	RW	VPROTH_PSEL_MODE: Controls power state of drivers. 0 = Normal power. 1 = Reduced power.

Register Name	PC Configuration 0 Register
Mnemonic	IOM0.DDRPHY_PC_CONFIG0_P1
Address	8000C00C0701143F (SCOM)
Description	This register contains global configuration information that describes the characteristics of the memory modules and characteristics of the system design.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	PDA_ENABLE_OVERRIDE: Enables PDA mode on a rank pair basis by overriding the snooped value of bit 4 in the PC Mode 3 Register (MR3). Required in certain DIMM configurations. Bit 48 overrides rank pair 0 MR3 bit 4 PDA enable. Bit 49 overrides rank pair 1 MR3 bit 4 PDA enable. Bit 50 overrides rank pair 2 MR3 bit 4 PDA enable. Bit 51 overrides rank pair 3 MR3 bit 4 PDA enable. 0 = PDA under MR3 bit 4 control. 1 = PDA enable.
52	RW	2TCK_PREAMBLE_ENABLE: 0 = 1tCK preamble for write and read traffic. 1 = 2tCK preamble for write and read traffic. **Note:** Calibration steps always use 1tCK preamble.
53	RW	PBA_ENABLE: LRDIMM PBA enable. 0 = Disable PBA. 1 = Enable PBA, which snoops BCW writes and drives DQ/DQS.
54	RW	DDR4_CMD_SIG_REDUCTION: In DDR4, to enable the DDR4 command/address signal-reduction feature, this value must be set to 1b. 0 = The PHY does not decode the ACT# DDR command signal. 1 = The PHY monitors and drives the DDR4 ACT# (activate) signal. Address pins A15, A14, and A13 are not monitored. When the DDR PHY drives an activate command, A15, A14, and A13 are driven onto RAS#, CAS#, and WE#.
55	RW	SYSCLK_2X_MEMINTCLKO: 0 = The internal SYSCLK frequency equals the memory interface clock (MEMINTCLKO) frequency. 1 = Not supported.
56	RW	RANK_OVERRIDE: Rank override mode. 0 = The DDR PHY uses the rank number (chip select) provided by the memory controller on the MEMCTL interface to determine the rank pair and hence the configuration registers for each read or write command. 1 = The DDR PHY uses the rank number provided in the RANK_OVERRIDE_VALUE field of this register to determine the rank pair and hence the configuration registers for all read/write commands regardless of the rank number (chip select) provided by the memory controller on the MEMCTL interface. When this bit is 1b, the following assumptions and restrictions apply: All ranks must be of the same configuration. (That is, all x4 or all x8.) Only the rank specified in RANK_OVERRIDE_VALUE can be calibrated. Calibrating other ranks causes an undefined behavior.
57:59	RW	RANK_OVERRIDE_VALUE: Rank override value. 000 = Rank 0 001 = Rank 1 010 = Rank 2 011 = Rank 3 All other settings are reserved.
60	RW	LOW_LATENCY: 0 = ERS mode on/off is determined by the CL value. When CL = 5 or 6, ERS mode is automatically off. Otherwise, ERS mode is automatically on. 1 = Force ERS mode off.

Bits	SCOM	Field Mnemonic: Description
61	RW	DDR4_IPW_LOOP_DIS: When the MEMORY_TYPE field in the PC Configuration 1 Register equals 1XXX (for example, DDR4 RDIMM), IPW to MPR requires that Side A and Side B DRAMs be written separately. IPW loops to write both sides for this memory type. This bit can disable this behavior, in which case Side A/B selection can be manually controlled in the SEQ Configuration 0 Register. 0 = Normal operation. IPW loops over both sides. 1 = IPW loop behavior is disabled. This bit must be set to 1 if the FORCE_RESERVED bit is set in the SEQ Configuration 0 Register. This bit is not used for other memory types.
62	RW	DDR4_VLEVEL_BANK_GROUP: Must be set to `1'b. 0 = Disable voltage level and bank group arch. 1 = Enable voltage level and bank group arch.
63	RW	VPROTH_PSEL_MODE: Controls power state of drivers. 0 = Normal power. 1 = Reduced power.

Register Name	PC Configuration 0 Register
Mnemonic	IOM0.DDRPHY_PC_CONFIG0_P2
Address	8000C00C0701183F (SCOM)
Description	This register contains global configuration information that describes the characteristics of the memory modules and characteristics of the system design.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	PDA_ENABLE_OVERRIDE: Enables PDA mode on a rank pair basis by overriding the snooped value of bit 4 in the PC Mode 3 Register (MR3). Required in certain DIMM configurations. Bit 48 overrides rank pair 0 MR3 bit 4 PDA enable. Bit 49 overrides rank pair 1 MR3 bit 4 PDA enable. Bit 50 overrides rank pair 2 MR3 bit 4 PDA enable. Bit 51 overrides rank pair 3 MR3 bit 4 PDA enable. 0 = PDA under MR3 bit 4 control. 1 = PDA enable.
52	RW	2TCK_PREAMBLE_ENABLE: 0 = 1tCK preamble for write and read traffic. 1 = 2tCK preamble for write and read traffic. **Note:** Calibration steps always use 1tCK preamble.
53	RW	PBA_ENABLE: LRDIMM PBA enable. 0 = Disable PBA. 1 = Enable PBA, which snoops BCW writes and drives DQ/DQS.
54	RW	DDR4_CMD_SIG_REDUCTION: In DDR4, to enable the DDR4 command/address signal-reduction feature, this value must be set to 1b. 0 = The PHY does not decode the ACT# DDR command signal. 1 = The PHY monitors and drives the DDR4 ACT# (activate) signal. Address pins A15, A14, and A13 are not monitored. When the DDR PHY drives an activate command, A15, A14, and A13 are driven onto RAS#, CAS#, and WE#.
55	RW	SYSCLK_2X_MEMINTCLKO: 0 = The internal SYSCLK frequency equals the memory interface clock (MEMINTCLKO) frequency. 1 = Not supported.

Bits	SCOM	Field Mnemonic: Description
56	RW	RANK_OVERRIDE: Rank override mode. 0 = The DDR PHY uses the rank number (chip select) provided by the memory controller on the MEMCTL interface to determine the rank pair and hence the configuration registers for each read or write command. 1 = The DDR PHY uses the rank number provided in the RANK_OVERRIDE_VALUE field of this register to determine the rank pair and hence the configuration registers for all read/write commands regardless of the rank number (chip select) provided by the memory controller on the MEMCTL interface. When this bit is 1b, the following assumptions and restrictions apply: All ranks must be of the same configuration. (That is, all x4 or all x8.) Only the rank specified in RANK_OVERRIDE_VALUE can be calibrated. Calibrating other ranks causes an undefined behavior.
57:59	RW	RANK_OVERRIDE_VALUE: Rank override value. 000 = Rank 0 001 = Rank 1 010 = Rank 2 011 = Rank 3 All other settings are reserved.
60	RW	LOW_LATENCY: 0 = ERS mode on/off is determined by the CL value. When CL = 5 or 6, ERS mode is automatically off. Otherwise, ERS mode is automatically on. 1 = Force ERS mode off.
61	RW	DDR4_IPW_LOOP_DIS: When the MEMORY_TYPE field in the PC Configuration 1 Register equals 1XXX (for example, DDR4 RDIMM), IPW to MPR requires that Side A and Side B DRAMs be written separately. IPW loops to write both sides for this memory type. This bit can disable this behavior, in which case Side A/B selection can be manually controlled in the SEQ Configuration 0 Register. 0 = Normal operation. IPW loops over both sides. 1 = IPW loop behavior is disabled. This bit must be set to 1 if the FORCE_RESERVED bit is set in the SEQ Configuration 0 Register. This bit is not used for other memory types.
62	RW	DDR4_VLEVEL_BANK_GROUP: Must be set to `1'b. 0 = Disable voltage level and bank group arch. 1 = Enable voltage level and bank group arch.
63	RW	VPROTH_PSEL_MODE: Controls power state of drivers. 0 = Normal power. 1 = Reduced power.

Register Name	PC Configuration 0 Register
Mnemonic	IOM0.DDRPHY_PC_CONFIG0_P3
Address	8000C00C07011C3F (SCOM)
Description	This register contains global configuration information that describes the characteristics of the memory modules and characteristics of the system design.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	PDA_ENABLE_OVERRIDE: Enables PDA mode on a rank pair basis by overriding the snooped value of bit 4 in the PC Mode 3 Register (MR3). Required in certain DIMM configurations. Bit 48 overrides rank pair 0 MR3 bit 4 PDA enable. Bit 49 overrides rank pair 1 MR3 bit 4 PDA enable. Bit 50 overrides rank pair 2 MR3 bit 4 PDA enable. Bit 51 overrides rank pair 3 MR3 bit 4 PDA enable. 0 = PDA under MR3 bit 4 control. 1 = PDA enable.

Bits	SCOM	Field Mnemonic: Description
52	RW	2TCK_PREAMBLE_ENABLE: 0 = 1tCK preamble for write and read traffic. 1 = 2tCK preamble for write and read traffic. **Note:** Calibration steps always use 1tCK preamble.
53	RW	PBA_ENABLE: LRDIMM PBA enable. 0 = Disable PBA. 1 = Enable PBA, which snoops BCW writes and drives DQ/DQS.
54	RW	DDR4_CMD_SIG_REDUCTION: In DDR4, to enable the DDR4 command/address signal-reduction feature, this value must be set to 1b. 0 = The PHY does not decode the ACT# DDR command signal. 1 = The PHY monitors and drives the DDR4 ACT# (activate) signal. Address pins A15, A14, and A13 are not monitored. When the DDR PHY drives an activate command, A15, A14, and A13 are driven onto RAS#, CAS#, and WE#.
55	RW	SYSCLK_2X_MEMINTCLKO: 0 = The internal SYSCLK frequency equals the memory interface clock (MEMINTCLKO) frequency. 1 = Not supported.
56	RW	RANK_OVERRIDE: Rank override mode. 0 = The DDR PHY uses the rank number (chip select) provided by the memory controller on the MEMCTL interface to determine the rank pair and hence the configuration registers for each read or write command. 1 = The DDR PHY uses the rank number provided in the RANK_OVERRIDE_VALUE field of this register to determine the rank pair and hence the configuration registers for all read/write commands regardless of the rank number (chip select) provided by the memory controller on the MEMCTL interface. When this bit is 1b, the following assumptions and restrictions apply: All ranks must be of the same configuration. (That is, all x4 or all x8.) Only the rank specified in RANK_OVERRIDE_VALUE can be calibrated. Calibrating other ranks causes an undefined behavior.
57:59	RW	RANK_OVERRIDE_VALUE: Rank override value. 000 = Rank 0 001 = Rank 1 010 = Rank 2 011 = Rank 3 All other settings are reserved.
60	RW	LOW_LATENCY: 0 = ERS mode on/off is determined by the CL value. When CL = 5 or 6, ERS mode is automatically off. Otherwise, ERS mode is automatically on. 1 = Force ERS mode off.
61	RW	DDR4_IPW_LOOP_DIS: When the MEMORY_TYPE field in the PC Configuration 1 Register equals 1XXX (for example, DDR4 RDIMM), IPW to MPR requires that Side A and Side B DRAMs be written separately. IPW loops to write both sides for this memory type. This bit can disable this behavior, in which case Side A/B selection can be manually controlled in the SEQ Configuration 0 Register. 0 = Normal operation. IPW loops over both sides. 1 = IPW loop behavior is disabled. This bit must be set to 1 if the FORCE_RESERVED bit is set in the SEQ Configuration 0 Register. This bit is not used for other memory types.
62	RW	DDR4_VLEVEL_BANK_GROUP: Must be set to `1'b. 0 = Disable voltage level and bank group arch. 1 = Enable voltage level and bank group arch.
63	RW	VPROTH_PSEL_MODE: Controls power state of drivers. 0 = Normal power. 1 = Reduced power.

Register Name	PC Configuration 1 Register
Mnemonic	IOM0.DDRPHY_PC_CONFIG1_P0
Address	8000C00D0701103F (SCOM)
Description	This register contains global configuration information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:51	RW	WRITE_LATENCY_OFFSET: Write latency offset (WLO) is used to adjust the delay through the internal write command FIFO. RDIMM support might require this field to be set to a nonzero value to account for register clock driver (RCD) latency. Certain board latencies might require the WLO to be set to a negative number. Changes to the WLO are accompanied by changes to the memory controller's wr_data_dly setting. For instance, if WLO moves from 0 to -1, wr_data_delay must be increased by +1. This value is twos complement, with a range of '-8'd to '7'd memory clock cycles. Determination of the WLO is based on hardware characterization, which takes into account all system delays.
52:55	RW	READ_LATENCY_OFFSET: Read latency offset (RLO) is used to adjust the delay through the internal read command FIFO. RDIMM support might require this field to be set to a nonzero value to account for RCD latency. This value is a twos compliment, with a range of -8d to 7d memory clock cycles. The value for this field must be: RLO ≤ min{RoundDown(System_Delay)} where: System_Delay is the round-trip delay in the memory system: System_Delay = (((ADR_DELAY - '64'd) + {wire delay from the PHY memory clock output to the DRAM module converted to units of 1/128th of a MEMINTCLKO clock cycle} + {delay of DQS at the memory module pin relative to memory clock at the memory module pin introduced by the memory module (that is, tDQSCK) converted to units of 1/128th of a MEMINTCLKO clock cycle} + {wire delay from the DRAM DQS output to the PHY converted to units of 1/128th of a MEMINTCLKO clock cycle}) / 128) max{RoundUp(System_Delay)} is the largest System_Delay in the memory system across all data bits and all ranks rounded up to the next integer memory clock cycle period value. min{RoundDown(System_Delay)} is the smallest System_Delay in the memory system across all data bits and all ranks rounded down to the next integer memory clock cycle period value. The recommended values for RLO are: RLO = 3 for RDIMMs RLO = 4 for LRDIMMs Long board wire lengths might require an increase in the RLO.
56	RW	MEMCTL_CIC_FAST: 0 = memctl_cic_o is de-asserted (0b) in response to memctl_cis_i being asserted (1b) and remains de-asserted until the calibration completes. 1 = memctl_cic_o is de-asserted (0b) in response to memctl_cis_i being asserted (1b) and is asserted (1b) in response to memctl_cis_i being de-asserted (0b).
57	RW	MEMCTL_CTRN_IGNORE: 0 = DDR PHY responds to the memctl_ctrn_i input. 1 = DDR PHY does not respond to the memctl_ctrn_i input. The memctl_ctrn_i input value is a don't care.
58	RW	DISABLE_MEMCTL_CAL: Reserved. This bit must be 0b. When set to 1b, the DDR PHY interface bus (DFI) request/ACK handshaking is disabled. The DDR PHY does not wait for an acknowledgment (ACK). This is a debug aid.
59:61	RW	MEMORY_TYPE: 101 = DDR4 RDIMM. 111 = DDR4 LRDIMM. Other values are reserved.
62	RW	DDR4_LATENCY_SW: 0 = Standard DDR4 CL range (MR0 A6:A4, A2). 1 = Extended DDR4/3DS CL range (MR0 A12, A6:A4, A2).

Bits	SCOM	Field Mnemonic: Description
63	RW	RETRAIN_PERCAL_SW: Retrain the periodic-calibration mode switch. This bit affects the behavior of memctl_cup_o during periodic read calibrations. 0 = The rank is the requested rank and might not be the rank that was executed. 1 = The rank is the next rank that requires calibration.

Register Name	PC Configuration 1 Register
Mnemonic	IOM0.DDRPHY_PC_CONFIG1_P1
Address	8000C00D0701143F (SCOM)
Description	This register contains global configuration information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	WRITE_LATENCY_OFFSET: Write latency offset (WLO) is used to adjust the delay through the internal write command FIFO. RDIMM support might require this field to be set to a nonzero value to account for RCD latency. Certain board latencies might require the WLO to be set to a negative number. Changes to the WLO are accompanied by changes to the memory controller's wr_data_dly setting. For instance, if WLO moves from 0 to -1, wr_data_delay must be increased by +1. This value is twos complement, with a range of '-8'd to '7'd memory clock cycles. Determination of the WLO is based on hardware characterization, which takes into account all system delays.
52:55	RW	READ_LATENCY_OFFSET: Read latency offset (RLO) is used to adjust the delay through the internal read command FIFO. RDIMM support might require this field to be set to a nonzero value to account for RCD latency. This value is a twos compliment, with a range of -8d to 7d memory clock cycles. The value for this field must be: RLO ≤ min{RoundDown(System_Delay)} where: System_Delay is the round-trip delay in the memory system: System_Delay = (((ADR_DELAY - '64'd) + {wire delay from the PHY memory clock output to the DRAM module converted to units of 1/128th of a MEMINTCLKO clock cycle} + {delay of DQS at the memory module pin relative to memory clock at the memory module pin introduced by the memory module (that is, tDQSCK) converted to units of 1/128th of a MEMINTCLKO clock cycle} + {wire delay from the DRAM DQS output to the PHY converted to units of 1/128th of a MEMINTCLKO clock cycle}) / 128) max{RoundUp(System_Delay)} is the largest System_Delay in the memory system across all data bits and all ranks rounded up to the next integer memory clock cycle period value. min{RoundDown(System_Delay)} is the smallest System_Delay in the memory system across all data bits and all ranks rounded down to the next integer memory clock cycle period value. The recommended values for RLO are: RLO = 3 for RDIMMs RLO = 4 for LRDIMMs Long board wire lengths might require an increase in the RLO.
56	RW	MEMCTL_CIC_FAST: 0 = memctl_cic_o is de-asserted (0b) in response to memctl_cis_i being asserted (1b) and remains de-asserted until the calibration completes. 1 = memctl_cic_o is de-asserted (0b) in response to memctl_cis_i being asserted (1b) and is asserted (1b) in response to memctl_cis_i being de-asserted (0b).
57	RW	MEMCTL_CTRN_IGNORE: 0 = DDR PHY responds to the memctl_ctrn_i input. 1 = DDR PHY does not respond to the memctl_ctrn_i input. The memctl_ctrn_i input value is a don't care.
58	RW	DISABLE_MEMCTL_CAL: Reserved. This bit must be 0b. When set to 1b, the DFI request/ACK handshaking is disabled. The DDR PHY does not wait for an ACK. This is a debug aid.

Bits	SCOM	Field Mnemonic: Description
59:61	RW	MEMORY_TYPE: 101 = DDR4 RDIMM. 111 = DDR4 LRDIMM. Other values are reserved.
62	RW	DDR4_LATENCY_SW: 0 = Standard DDR4 CL range (MR0 A6:A4, A2). 1 = Extended DDR4/3DS CL range (MR0 A12, A6:A4, A2).
63	RW	RETRAIN_PERCAL_SW: Retrain the periodic-calibration mode switch. This bit affects the behavior of memctl_cup_o during periodic read calibrations. 0 = The rank is the requested rank and might not be the rank that was executed. 1 = The rank is the next rank that requires calibration.

Register Name	PC Configuration 1 Register
Mnemonic	IOM0.DDRPHY_PC_CONFIG1_P2
Address	8000C00D0701183F (SCOM)
Description	This register contains global configuration information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	WRITE_LATENCY_OFFSET: Write latency offset (WLO) is used to adjust the delay through the internal write command FIFO. RDIMM support might require this field to be set to a nonzero value to account for RCD latency. Certain board latencies might require the WLO to be set to a negative number. Changes to the WLO are accompanied by changes to the memory controller's wr_data_dly setting. For instance, if WLO moves from 0 to -1, wr_data_delay must be increased by +1. This value is twos complement, with a range of '-8'd to '7'd memory clock cycles. Determination of the WLO is based on hardware characterization, which takes into account all system delays.
52:55	RW	READ_LATENCY_OFFSET: Read latency offset (RLO) is used to adjust the delay through the internal read command FIFO. RDIMM support might require this field to be set to a nonzero value to account for RCD latency. This value is a twos compliment, with a range of -8d to 7d memory clock cycles. The value for this field must be: RLO ≤ min{RoundDown(System_Delay)} where: System_Delay is the round-trip delay in the memory system: System_Delay = (((ADR_DELAY - '64'd) + {wire delay from the PHY memory clock output to the DRAM module converted to units of 1/128th of a MEMINTCLKO clock cycle} + {delay of DQS at the memory module pin relative to memory clock at the memory module pin introduced by the memory module (that is, tDQSCK) converted to units of 1/128th of a MEMINTCLKO clock cycle} + {wire delay from the DRAM DQS output to the PHY converted to units of 1/128th of a MEMINTCLKO clock cycle}) / 128) max{RoundUp(System_Delay)} is the largest System_Delay in the memory system across all data bits and all ranks rounded up to the next integer memory clock cycle period value. min{RoundDown(System_Delay)} is the smallest System_Delay in the memory system across all data bits and all ranks rounded down to the next integer memory clock cycle period value. The recommended values for RLO are: RLO = 3 for RDIMMs RLO = 4 for LRDIMMs Long board wire lengths might require an increase in the RLO.
56	RW	MEMCTL_CIC_FAST: 0 = memctl_cic_o is de-asserted (0b) in response to memctl_cis_i being asserted (1b) and remains de-asserted until the calibration completes. 1 = memctl_cic_o is de-asserted (0b) in response to memctl_cis_i being asserted (1b) and is asserted (1b) in response to memctl_cis_i being de-asserted (0b).

Bits	SCOM	Field Mnemonic: Description
57	RW	MEMCTL_CTRN_IGNORE: 0 = DDR PHY responds to the memctl_ctrn_i input. 1 = DDR PHY does not respond to the memctl_ctrn_i input. The memctl_ctrn_i input value is a don't care.
58	RW	DISABLE_MEMCTL_CAL: Reserved. This bit must be 0b. When set to 1b, the DFI request/ACK handshaking is disabled. The DDR PHY does not wait for an ACK. This is a debug aid.
59:61	RW	MEMORY_TYPE: 101 = DDR4 RDIMM. 111 = DDR4 LRDIMM. Other values are reserved.
62	RW	DDR4_LATENCY_SW: 0 = Standard DDR4 CL range (MR0 A6:A4, A2). 1 = Extended DDR4/3DS CL range (MR0 A12, A6:A4, A2).
63	RW	RETRAIN_PERCAL_SW: Retrain the periodic-calibration mode switch. This bit affects the behavior of memctl_cup_o during periodic read calibrations. 0 = The rank is the requested rank and might not be the rank that was executed. 1 = The rank is the next rank that requires calibration.

Register Name	PC Configuration 1 Register
Mnemonic	IOM0.DDRPHY_PC_CONFIG1_P3
Address	8000C00D07011C3F (SCOM)
Description	This register contains global configuration information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	WRITE_LATENCY_OFFSET: Write latency offset (WLO) is used to adjust the delay through the internal write command FIFO. RDIMM support might require this field to be set to a nonzero value to account for RCD latency. Certain board latencies might require the WLO to be set to a negative number. Changes to the WLO are accompanied by changes to the memory controller's wr_data_dly setting. For instance, if WLO moves from 0 to -1, wr_data_delay must be increased by +1. This value is twos complement, with a range of '-8'd to '7'd memory clock cycles. Determination of the WLO is based on hardware characterization, which takes into account all system delays.

Bits	SCOM	Field Mnemonic: Description
52:55	RW	READ_LATENCY_OFFSET: Read latency offset (RLO) is used to adjust the delay through the internal read command FIFO. RDIMM support might require this field to be set to a nonzero value to account for RCD latency. This value is a twos compliment, with a range of -8d to 7d memory clock cycles. The value for this field must be: RLO ≤ min{RoundDown(System_Delay)} where: System_Delay is the round-trip delay in the memory system: System_Delay = (((ADR_DELAY - '64'd) + {wire delay from the PHY memory clock output to the DRAM module converted to units of 1/128th of a MEMINTCLKO clock cycle} + {delay of DQS at the memory module pin relative to memory clock at the memory module pin introduced by the memory module (that is, tDQSCK) converted to units of 1/128th of a MEMINTCLKO clock cycle} + {wire delay from the DRAM DQS output to the PHY converted to units of 1/128th of a MEMINTCLKO clock cycle}) / 128) max{RoundUp(System_Delay)} is the largest System_Delay in the memory system across all data bits and all ranks rounded up to the next integer memory clock cycle period value. min{RoundDown(System_Delay)} is the smallest System_Delay in the memory system across all data bits and all ranks rounded down to the next integer memory clock cycle period value. The recommended values for RLO are: RLO = 3 for RDIMMs RLO = 4 for LRDIMMs Long board wire lengths might require an increase in the RLO.
56	RW	MEMCTL_CIC_FAST: 0 = memctl_cic_o is de-asserted (0b) in response to memctl_cis_i being asserted (1b) and remains de-asserted until the calibration completes. 1 = memctl_cic_o is de-asserted (0b) in response to memctl_cis_i being asserted (1b) and is asserted (1b) in response to memctl_cis_i being de-asserted (0b).
57	RW	MEMCTL_CTRN_IGNORE: 0 = DDR PHY responds to the memctl_ctrn_i input. 1 = DDR PHY does not respond to the memctl_ctrn_i input. The memctl_ctrn_i input value is a don't care.
58	RW	DISABLE_MEMCTL_CAL: Reserved. This bit must be 0b. When set to 1b, the DFI request/ACK handshaking is disabled. The DDR PHY does not wait for an ACK. This is a debug aid.
59:61	RW	MEMORY_TYPE: 101 = DDR4 RDIMM. 111 = DDR4 LRDIMM. Other values are reserved.
62	RW	DDR4_LATENCY_SW: 0 = Standard DDR4 CL range (MR0 A6:A4, A2). 1 = Extended DDR4/3DS CL range (MR0 A12, A6:A4, A2).
63	RW	RETRAIN_PERCAL_SW: Retrain the periodic-calibration mode switch. This bit affects the behavior of memctl_cup_o during periodic read calibrations. 0 = The rank is the requested rank and might not be the rank that was executed. 1 = The rank is the next rank that requires calibration.

Register Name	PC Resets Register
Mnemonic	IOM0.DDRPHY_PC_RESETS_P0
Address	8000C00E0701103F (SCOM)
Description	This register provides the capability to initiate resets in the hard cores.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b0000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49	RO	SYSCLK_RESET: 1 = Reset all logic in the internal SYSCLK domain.
50	RO	PVT_OVERRIDE: 0 = All drivers are updated with the PVTP and PVTN values from the internal impedance calibration state machine. 1 = All drivers are updated with the PVTP and PVTN override values from the PC IO PVT N/P FET Driver Control Register.
51	RO	ENABLE_ZCAL: ENABLE_ZCAL must be toggled for the internal impedance calibration values to be updated. The required sequence is as follows: 1. Set this bit to 0b. 2. Set this bit to 1b. 3. Wait for the ZCAL_DONE bit in the PC DLL / ZCAL Calibration Status Register to go to 1b. 0 = Disable the internal impedance controller. 1 = Enable the internal impedance controller.
52	RO	VREF_85PER: 0 = Voltage protect high (VPROTH) regulators at 70%. 1 = VPROTH regulators at 85%.
53:55	RO	Reserved.
56	RO	DD2_WR_PRE_DLY_EXT: This bit is used to extend the range of the WR_PRE_DLY parameter in the WC Configuration 1 Register. WR_PRE_DLY has a range limitation of 0:63. For 2666 speeds and beyond, 63 might not be a sufficient delay, and the actual range of the delay can be extended using DD2_WR_PRE_DLY_EXT. 0 = WC Configuration 1, WR_PRE_DLY range is 0:63 (DD1 function). 1 = WC Configuration 1, WR_PRE_DLY range is extended to 64:127.
57	RO	DD2_ADR_CG_DISABLE: 0 = Enable DD2 enhanced clock gating on ADR registers. 1 = Enable DD1 function.
58	RO	DD2_WC_CA_ERROR_DISABLE: 0 = Enable DD2 recording of write control (WRCNTL) errors propagating during coarse alignment. 1 = Enable DD1 function.
59	RO	DD2_CAL_REG_CG_DISABLE: 0 = Enable DD2 enhanced clock gating on calibration registers. 1 = Enable DD1 function.
60	RO	DD2_CMDS_REG_CG_DISABLE: 0 = Enable DD2 enhanced clock gating on command FIFOs and mode register set (MRS) snoop registers. 1 = Enable DD1 function.
61	RO	PBA_CW_F0RC06_DISABLE: 0 = Enable PBA support for BCWs written using CW F0RC06. 1 = Disable this function.
62	RO	DD2_RESET_READ_FIX_DISABLE: 0 = Enable DD2 function to remove the register reset on read feature on status registers. 1 = Enable DD1 function.
63	RO	DD2_BABG_INV_FIX_DISABLE: 0 = Enable DD2 function for interpreting bank address (BA) and bank group (BG) polarity on inverted Mode Register 7 (MR7) control words. 1 = Enable DD1 function.

Register Name	PC Resets Register
Mnemonic	IOM0.DDRPHY_PC_RESETS_P1
Address	8000C00E0701143F (SCOM)
Description	This register provides the capability to initiate resets in the hard cores.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b0000000000000000000000000000000000000000000000000
49	RO	SYSCLK_RESET: 1 = Reset all logic in the internal system clock (SYSCLK) domain.
50	RO	PVT_OVERRIDE: 0 = All drivers are updated with the process voltage temperature (PVTP and PVTN) values from the internal impedance calibration state machine. 1 = All drivers are updated with the PVTP and PVTN override values from the PC IO PVT N/P FET Driver Control Register.
51	RO	ENABLE_ZCAL: ENABLE_ZCAL must be toggled for the internal impedance calibration values to be updated. The required sequence is as follows: 1. Set this bit to 0b. 2. Set this bit to 1b. 3. Wait for the ZCAL_DONE bit in the PC DLL / ZCAL Calibration Status Register to go to 1b. 0 = Disable the internal impedance controller. 1 = Enable the internal impedance controller.
52	RO	VREF_85PER: 0 = VPROTH regulators at 70%. 1 = VPROTH regulators at 85%.
53:55	RO	Reserved.
56	RO	DD2_WR_PRE_DLY_EXT: This bit is used to extend the range of the WR_PRE_DLY parameter in the WC Configuration 1 Register. WR_PRE_DLY has a range limitation of 0:63. For 2666 speeds and beyond, 63 might not be a sufficient delay, and the actual range of the delay can be extended using DD2_WR_PRE_DLY_EXT. 0 = WC Configuration 1, WR_PRE_DLY range is 0:63 (DD1 function). 1 = WC Configuration 1, WR_PRE_DLY range is extended to 64:127.
57	RO	DD2_ADR_CG_DISABLE: 0 = Enable DD2 enhanced clock gating on ADR registers. 1 = Enable DD1 function.
58	RO	DD2_WC_CA_ERROR_DISABLE: 0 = Enable DD2 recording of WRCNTL errors propagating during coarse alignment. 1 = Enable DD1 function.
59	RO	DD2_CAL_REG_CG_DISABLE: 0 = Enable DD2 enhanced clock gating on calibration registers. 1 = Enable DD1 function.
60	RO	DD2_CMDS_REG_CG_DISABLE: 0 = Enable DD2 enhanced clock gating on command FIFOs and MRS snoop registers. 1 = Enable DD1 function.
61	RO	PBA_CW_F0RC06_DISABLE: 0 = Enable PBA support for BCWs written using CW F0RC06. 1 = Disable this function.
62	RO	DD2_RESET_READ_FIX_DISABLE: 0 = Enable DD2 function to remove the register reset on read feature on status registers. 1 = Enable DD1 function.

Bits	SCOM	Field Mnemonic: Description
63	RO	DD2_BABG_INV_FIX_DISABLE: 0 = Enable DD2 function for interpreting BA and BG polarity on inverted MR7 control words. 1 = Enable DD1 function.

Register Name	PC Resets Register
Mnemonic	IOM0.DDRPHY_PC_RESETS_P2
Address	8000C00E0701183F (SCOM)
Description	This register provides the capability to initiate resets in the hard cores.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49	RO	SYSCLK_RESET: 1 = Reset all logic in the internal SYSCLK domain.
50	RO	PVT_OVERRIDE: 0 = All drivers are updated with the PVTP and PVTN values from the internal impedance calibration state machine. 1 = All drivers are updated with the PVTP and PVTN override values from the PC IO PVT N/P FET Driver Control Register.
51	RO	ENABLE_ZCAL: ENABLE_ZCAL must be toggled for the internal impedance calibration values to be updated. The required sequence is as follows: 1. Set this bit to 0b. 2. Set this bit to 1b. 3. Wait for the ZCAL_DONE bit in the PC DLL / ZCAL Calibration Status Register to go to 1b. 0 = Disable the internal impedance controller. 1 = Enable the internal impedance controller.
52	RO	VREF_85PER: 0 = VPROTH regulators at 70%. 1 = VPROTH regulators at 85%.
53:55	RO	Reserved.
56	RO	DD2_WR_PRE_DLY_EXT: This bit is used to extend the range of the WR_PRE_DLY parameter in the WC Configuration 1 Register. WR_PRE_DLY has a range limitation of 0:63. For 2666 speeds and beyond, 63 might not be a sufficient delay, and the actual range of the delay can be extended using DD2_WR_PRE_DLY_EXT. 0 = WC Configuration 1, WR_PRE_DLY range is 0:63 (DD1 function). 1 = WC Configuration 1, WR_PRE_DLY range is extended to 64:127.
57	RO	DD2_ADR_CG_DISABLE: 0 = Enable DD2 enhanced clock gating on ADR registers. 1 = Enable DD1 function.
58	RO	DD2_WC_CA_ERROR_DISABLE: 0 = Enable DD2 recording of WRCNTL errors propagating during coarse alignment. 1 = Enable DD1 function.
59	RO	DD2_CAL_REG_CG_DISABLE: 0 = Enable DD2 enhanced clock gating on calibration registers. 1 = Enable DD1 function.
60	RO	DD2_CMDS_REG_CG_DISABLE: 0 = Enable DD2 enhanced clock gating on command FIFOs and MRS snoop registers. 1 = Enable DD1 function.

Bits	SCOM	Field Mnemonic: Description
61	RO	PBA_CW_F0RC06_DISABLE: 0 = Enable PBA support for BCWs written using CW F0RC06. 1 = Disable this function.
62	RO	DD2_RESET_READ_FIX_DISABLE: 0 = Enable DD2 function to remove the register reset on read feature on status registers. 1 = Enable DD1 function.
63	RO	DD2_BABG_INV_FIX_DISABLE: 0 = Enable DD2 function for interpreting BA and BG polarity on inverted MR7 control words. 1 = Enable DD1 function.

Register Name	PC Resets Register
Mnemonic	IOM0.DDRPHY_PC_RESETS_P3
Address	8000C00E07011C3F (SCOM)
Description	This register provides the capability to initiate resets in the hard cores.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49	RO	SYSCLK_RESET: 1 = Reset all logic in the internal SYSCLK domain.
50	RO	PVT_OVERRIDE: 0 = All drivers are updated with the PVTP and PVTN values from the internal impedance calibration state machine. 1 = All drivers are updated with the PVTP and PVTN override values from the PC IO PVT N/P FET Driver Control Register.
51	RO	ENABLE_ZCAL: ENABLE_ZCAL must be toggled for the internal impedance calibration values to be updated. The required sequence is as follows: 1. Set this bit to 0b. 2. Set this bit to 1b. 3. Wait for the ZCAL_DONE bit in the PC DLL / ZCAL Calibration Status Register to go to 1b. 0 = Disable the internal impedance controller. 1 = Enable the internal impedance controller.
52	RO	VREF_85PER: 0 = VPROTH regulators at 70%. 1 = VPROTH regulators at 85%.
53:55	RO	Reserved.
56	RO	DD2_WR_PRE_DLY_EXT: This bit is used to extend the range of the WR_PRE_DLY parameter in the WC Configuration 1 Register. WR_PRE_DLY has a range limitation of 0:63. For 2666 speeds and beyond, 63 might not be a sufficient delay, and the actual range of the delay can be extended using DD2_WR_PRE_DLY_EXT. 0 = WC Configuration 1, WR_PRE_DLY range is 0:63 (DD1 function). 1 = WC Configuration 1, WR_PRE_DLY range is extended to 64:127.
57	RO	DD2_ADR_CG_DISABLE: 0 = Enable DD2 enhanced clock gating on ADR registers. 1 = Enable DD1 function.
58	RO	DD2_WC_CA_ERROR_DISABLE: 0 = Enable DD2 recording of WRCNTL errors propagating during coarse alignment. 1 = Enable DD1 function.

Bits	SCOM	Field Mnemonic: Description
59	RO	DD2_CAL_REG_CG_DISABLE: 0 = Enable DD2 enhanced clock gating on calibration registers. 1 = Enable DD1 function.
60	RO	DD2_CMDS_REG_CG_DISABLE: 0 = Enable DD2 enhanced clock gating on command FIFOs and MRS snoop registers. 1 = Enable DD1 function.
61	RO	PBA_CW_F0RC06_DISABLE: 0 = Enable PBA support for BCWs written using CW F0RC06. 1 = Disable this function.
62	RO	DD2_RESET_READ_FIX_DISABLE: 0 = Enable DD2 function to remove the register reset on read feature on status registers. 1 = Enable DD1 function.
63	RO	DD2_BABG_INV_FIX_DISABLE: 0 = Enable DD2 function for interpreting BA and BG polarity on inverted MR7 control words. 1 = Enable DD1 function.

Register Name	**PC Periodic Z-Cal Configuration Register**
Mnemonic	IOM0.DDRPHY_PC_PER_ZCAL_CONFIG_P0
Address	8000C00F0701103F (SCOM)
Description	This register controls the periodic external impedance calibration logic. When enabled, the PHY periodically issues ZQ calibration commands to the external memory.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:55	RWX	PER_ZCAL_ENA_RANK: 1b indicates that periodic external impedance calibration is enabled. 0b indicates that periodic external impedance calibration is disabled. Bit 0 contains the enable bit for rank 0. Bit 1 contains the enable bit for rank 1. Bit 2 contains the enable bit for rank 2. Bit 3 contains the enable bit for rank 3. Bit 4 is reserved. Bit 5 is reserved. Bit 6 is reserved. Bit 7 is reserved.
56:58	RWX	PER_ZCAL_NEXT_RANK: Indicates which rank is scheduled for the next periodic external impedance calibration operation. This field is updated by the PHY as it sequences through periodic impedance calibrations on each enabled rank. 000 = rank_0 is the next rank scheduled to run ZCAL. 001 = rank_1 is the next rank scheduled to run ZCAL. 010 = rank_2 is the next rank scheduled to run ZCAL. 011 = rank_3 is the next rank scheduled to run ZCAL. All other settings are reserved.
59	RWX	START_PER_ZCAL: When this bit is written to 1b, the DDR PHY initiate a single periodic external impedance calibration (equivalent to a periodic ZCAL timer pop). When this bit is written to 0b, no action is taken by the DDR PHY. When read, this bit always returns the last value written.
60:63	RO	Constant = 0b0000

Register Name	PC Periodic Z-Cal Configuration Register
Mnemonic	IOM0.DDRPHY_PC_PER_ZCAL_CONFIG_P1
Address	8000C00F0701143F (SCOM)
Description	This register controls the periodic external impedance calibration logic. When enabled, the PHY periodically issues ZQ calibration commands to the external memory.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:55	RWX	PER_ZCAL_ENA_RANK: 1b indicates that periodic external impedance calibration is enabled. 0b indicates that periodic external impedance calibration is disabled. Bit 0 contains the enable bit for rank 0. Bit 1 contains the enable bit for rank 1. Bit 2 contains the enable bit for rank 2. Bit 3 contains the enable bit for rank 3. Bit 4 is reserved. Bit 5 is reserved. Bit 6 is reserved. Bit 7 is reserved.
56:58	RWX	PER_ZCAL_NEXT_RANK: Indicates which rank is scheduled for the next periodic external impedance calibration operation. This field is updated by the PHY as it sequences through periodic impedance calibrations on each enabled rank. 000 = rank_0 is the next rank scheduled to run ZCAL. 001 = rank_1 is the next rank scheduled to run ZCAL. 010 = rank_2 is the next rank scheduled to run ZCAL. 011 = rank_3 is the next rank scheduled to run ZCAL. All other settings are reserved.
59	RWX	START_PER_ZCAL: When this bit is written to 1b, the DDR PHY initiate a single periodic external impedance calibration (equivalent to a periodic ZCAL timer pop). When this bit is written to 0b, no action is taken by the DDR PHY. When read, this bit always returns the last value written.
60:63	RO	Constant = 0b0000

Register Name	PC Periodic Z-Cal Configuration Register
Mnemonic	IOM0.DDRPHY_PC_PER_ZCAL_CONFIG_P2
Address	8000C00F0701183F (SCOM)
Description	This register controls the periodic external impedance calibration logic. When enabled, the PHY periodically issues ZQ calibration commands to the external memory.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RWX	PER_ZCAL_ENA_RANK: 1b indicates that periodic external impedance calibration is enabled. 0b indicates that periodic external impedance calibration is disabled. Bit 0 contains the enable bit for rank 0. Bit 1 contains the enable bit for rank 1. Bit 2 contains the enable bit for rank 2. Bit 3 contains the enable bit for rank 3. Bit 4 is reserved. Bit 5 is reserved. Bit 6 is reserved. Bit 7 is reserved.
56:58	RWX	PER_ZCAL_NEXT_RANK: Indicates which rank is scheduled for the next periodic external impedance calibration operation. This field is updated by the PHY as it sequences through periodic impedance calibrations on each enabled rank. 000 = rank_0 is the next rank scheduled to run ZCAL. 001 = rank_1 is the next rank scheduled to run ZCAL. 010 = rank_2 is the next rank scheduled to run ZCAL. 011 = rank_3 is the next rank scheduled to run ZCAL. All other settings are reserved.
59	RWX	START_PER_ZCAL: When this bit is written to 1b, the DDR PHY initiate a single periodic external impedance calibration (equivalent to a periodic ZCAL timer pop). When this bit is written to 0b, no action is taken by the DDR PHY. When read, this bit always returns the last value written.
60:63	RO	Constant = 0b0000

Register Name	PC Periodic Z-Cal Configuration Register
Mnemonic	IOM0.DDRPHY_PC_PER_ZCAL_CONFIG_P3
Address	8000C00F07011C3F (SCOM)
Description	This register controls the periodic external impedance calibration logic. When enabled, the PHY periodically issues ZQ calibration commands to the external memory.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	PER_ZCAL_ENA_RANK: 1b indicates that periodic external impedance calibration is enabled. 0b indicates that periodic external impedance calibration is disabled. Bit 0 contains the enable bit for rank 0. Bit 1 contains the enable bit for rank 1. Bit 2 contains the enable bit for rank 2. Bit 3 contains the enable bit for rank 3. Bit 4 is reserved. Bit 5 is reserved. Bit 6 is reserved. Bit 7 is reserved.
56:58	RWX	PER_ZCAL_NEXT_RANK: Indicates which rank is scheduled for the next periodic external impedance calibration operation. This field is updated by the PHY as it sequences through periodic impedance calibrations on each enabled rank. 000 = rank_0 is the next rank scheduled to run ZCAL. 001 = rank_1 is the next rank scheduled to run ZCAL. 010 = rank_2 is the next rank scheduled to run ZCAL. 011 = rank_3 is the next rank scheduled to run ZCAL. All other settings are reserved.

Bits	SCOM	Field Mnemonic: Description
59	RWX	START_PER_ZCAL: When this bit is written to 1b, the DDR PHY initiate a single periodic external impedance calibration (equivalent to a periodic ZCAL timer pop). When this bit is written to 0b, no action is taken by the DDR PHY. When read, this bit always returns the last value written.
60:63	RO	Constant = 0b0000

Register Name	PC Power Down 1 Register
Mnemonic	IOM0.DDRPHY_PC_POWERDOWN_1_P0
Address	8000C0100701103F (SCOM)
Description	This register provides control of the power-down modes of the DDR PHY.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	RW	MASTER_POWERDOWN: Master power-down control. 0 = Normal operation. The DDR port is in functional mode regardless of Power Down Register 1 bits {49:63}. 1 = The power-down status of the DDR port is determined by Power Down Register 1 bits {49:63}.
49	RW	DLL_POWERDOWN: 0 = Normal operation. 1 = Shuts off the VCC voltage regulator in the DLL.
50	RW	DLL_CLOCK_GATE: 0 = Normal operation. 1 = Disables the DLL clocks. Valid only when DLL_POWERDOWN = 0.
51	RW	DQS_POWERDOWN: 0 = Normal operation. 1 = Disables the internal dqsaclk and dqsbclk signals.
52	RW	VPROTH_POWERDOWN: 0 = Normal operation. 1 = Puts the VPROTH regulators into a reduced power mode.
53	RW	KPRIME_POWERDOWN: 0 = Normal operation. 1 = Disables the KPRIME reference circuit. (KPRIME is a macro embedded in the hierarchy.) Note that this renders the VCC regulators inoperative.
54	RW	PORTPOWERDOWN: 0 = Normal operation. 1 = Forces internal signals on the regulated VCC supplies to known states. Typically used in conjunction with DLL_POWERDOWN and VREG_S_POWERDOWN.
55	RW	ANALOG_INPUT_STAB: 0 = Normal operation. 1 = Forces the even and odd data (EDAT/ODAT) inputs to the analog macros to a known state.
56	RW	ZCAL_POWERDOWN: 0 = Normal operation. 1 = Disables the internal impedance calibration circuits.
57	RW	DELAY_LINE_CTL_OVERRIDE: 0 = Normal operation. 1 = Enables only the 0^{o} delay line phase into the read clock (RDCLK) phase rotators (PRs).
58	RW	WR_FIFO_STAB: 0 = Normal operation. 1 = All write FIFO clocks are disabled, and flush mode is set.

Bits	SCOM	Field Mnemonic: Description
59	RW	Reserved.
60	RW	RX_POWERDOWN: 0 = Normal operation. 1 = Disables all DQ and DQS receivers.
61	RW	DP_TX_TRISTATE: 0 = Normal operation. 1 = Puts DQ and DQS drivers into a tri-state (high-impedance) state.
62	RW	ADR_TX_TRISTATE: 0 = Normal operation. 1 = ADR driver tri-state (high-impedance) becomes controllable by Power Down Register 2 (PDR2).
63	RW	VREG_S_POWERDOWN: 0 = Normal operation. 1 = Shuts off the VCC voltage regulator for all circuits other than the DLL.

Register Name	PC Power Down 1 Register
Mnemonic	IOM0.DDRPHY_PC_POWERDOWN_1_P1
Address	8000C0100701143F (SCOM)
Description	This register provides control of the power-down modes of the DDR PHY.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	MASTER_POWERDOWN: Master power-down control. 0 = Normal operation. The DDR port is in functional mode regardless of Power Down Register 1 bits {49:63}. 1 = The power-down status of the DDR port is determined by Power Down Register 1 bits {49:63}.
49	RW	DLL_POWERDOWN: 0 = Normal operation. 1 = Shuts off the VCC voltage regulator in the DLL.
50	RW	DLL_CLOCK_GATE: 0 = Normal operation. 1 = Disables the DLL clocks. Valid only when DLL_POWERDOWN = 0.
51	RW	DQS_POWERDOWN: 0 = Normal operation. 1 = Disables the internal dqsaclk and dqsbclk signals.
52	RW	VPROTH_POWERDOWN: 0 = Normal operation. 1 = Puts the VPROTH regulators into a reduced power mode.
53	RW	KPRIME_POWERDOWN: 0 = Normal operation. 1 = Disables the KPRIME reference circuit. (KPRIME is a macro embedded in the hierarchy.) Note that this renders the VCC regulators inoperative.
54	RW	PORTPOWERDOWN: 0 = Normal operation. 1 = Forces internal signals on the regulated VCC supplies to known states. Typically used in conjunction with DLL_POWERDOWN and VREG_S_POWERDOWN.
55	RW	ANALOG_INPUT_STAB: 0 = Normal operation. 1 = Forces the EDAT/ODAT inputs to the analog macros to a known state.

Bits	SCOM	Field Mnemonic: Description
56	RW	ZCAL_POWERDOWN: 0 = Normal operation. 1 = Disables the internal impedance calibration circuits.
57	RW	DELAY_LINE_CTL_OVERRIDE: 0 = Normal operation. 1 = Enables only the 0º delay line phase into the RDCLK PRs.
58	RW	WR_FIFO_STAB: 0 = Normal operation. 1 = All write FIFO clocks are disabled, and flush mode is set.
59	RW	Reserved.
60	RW	RX_POWERDOWN: 0 = Normal operation. 1 = Disables all DQ and DQS receivers.
61	RW	DP_TX_TRISTATE: 0 = Normal operation. 1 = Puts DQ and DQS drivers into a tri-state (high-impedance) state.
62	RW	ADR_TX_TRISTATE: 0 = Normal operation. 1 = ADR driver tri-state (high-impedance) becomes controllable by PDR2.
63	RW	VREG_S_POWERDOWN: 0 = Normal operation. 1 = Shuts off the VCC voltage regulator for all circuits other than the DLL.

Register Name	PC Power Down 1 Register
Mnemonic	IOM0.DDRPHY_PC_POWERDOWN_1_P2
Address	8000C0100701183F (SCOM)
Description	This register provides control of the power-down modes of the DDR PHY.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	MASTER_POWERDOWN: Master power-down control. 0 = Normal operation. The DDR port is in functional mode regardless of Power Down Register 1 bits {49:63}. 1 = The power-down status of the DDR port is determined by Power Down Register 1 bits {49:63}.
49	RW	DLL_POWERDOWN: 0 = Normal operation. 1 = Shuts off the VCC voltage regulator in the DLL.
50	RW	DLL_CLOCK_GATE: 0 = Normal operation. 1 = Disables the DLL clocks. Valid only when DLL_POWERDOWN = 0.
51	RW	DQS_POWERDOWN: 0 = Normal operation. 1 = Disables the internal dqsaclk and dqsbclk signals.
52	RW	VPROTH_POWERDOWN: 0 = Normal operation. 1 = Puts the VPROTH regulators into a reduced power mode.

Bits	SCOM	Field Mnemonic: Description
53	RW	KPRIME_POWERDOWN: 0 = Normal operation. 1 = Disables the KPRIME reference circuit. (KPRIME is a macro embedded in the hierarchy.) Note that this renders the VCC regulators inoperative.
54	RW	PORTPOWERDOWN: 0 = Normal operation. 1 = Forces internal signals on the regulated VCC supplies to known states. Typically used in conjunction with DLL_POWERDOWN and VREG_S_POWERDOWN.
55	RW	ANALOG_INPUT_STAB: 0 = Normal operation. 1 = Forces the EDAT/ODAT inputs to the analog macros to a known state.
56	RW	ZCAL_POWERDOWN: 0 = Normal operation. 1 = Disables the internal impedance calibration circuits.
57	RW	DELAY_LINE_CTL_OVERRIDE: 0 = Normal operation. 1 = Enables only the 0^{o} delay line phase into the RDCLK PRs.
58	RW	WR_FIFO_STAB: 0 = Normal operation. 1 = All write FIFO clocks are disabled, and flush mode is set.
59	RW	Reserved.
60	RW	RX_POWERDOWN: 0 = Normal operation. 1 = Disables all DQ and DQS receivers.
61	RW	DP_TX_TRISTATE: 0 = Normal operation. 1 = Puts DQ and DQS drivers into a tri-state (high-impedance) state.
62	RW	ADR_TX_TRISTATE: 0 = Normal operation. 1 = ADR driver tri-state (high-impedance) becomes controllable by PDR2.
63	RW	VREG_S_POWERDOWN: 0 = Normal operation. 1 = Shuts off the VCC voltage regulator for all circuits other than the DLL.

Register Name	PC Power Down 1 Register
Mnemonic	IOM0.DDRPHY_PC_POWERDOWN_1_P3
Address	8000C01007011C3F (SCOM)
Description	This register provides control of the power-down modes of the DDR PHY.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	MASTER_POWERDOWN: Master power-down control. 0 = Normal operation. The DDR port is in functional mode regardless of Power Down Register 1 bits {49:63}. 1 = The power-down status of the DDR port is determined by Power Down Register 1 bits {49:63}.
49	RW	DLL_POWERDOWN: 0 = Normal operation. 1 = Shuts off the VCC voltage regulator in the DLL.

Bits	SCOM	Field Mnemonic: Description
50	RW	DLL_CLOCK_GATE: 0 = Normal operation. 1 = Disables the DLL clocks. Valid only when DLL_POWERDOWN = 0.
51	RW	DQS_POWERDOWN: 0 = Normal operation. 1 = Disables the internal dqsaclk and dqsbclk signals.
52	RW	VPROTH_POWERDOWN: 0 = Normal operation. 1 = Puts the VPROTH regulators into a reduced power mode.
53	RW	KPRIME_POWERDOWN: 0 = Normal operation. 1 = Disables the KPRIME reference circuit. (KPRIME is a macro embedded in the hierarchy.) Note that this renders the VCC regulators inoperative.
54	RW	PORTPOWERDOWN: 0 = Normal operation. 1 = Forces internal signals on the regulated VCC supplies to known states. Typically used in conjunction with DLL_POWERDOWN and VREG_S_POWERDOWN.
55	RW	ANALOG_INPUT_STAB: 0 = Normal operation. 1 = Forces the EDAT/ODAT inputs to the analog macros to a known state.
56	RW	ZCAL_POWERDOWN: 0 = Normal operation. 1 = Disables the internal impedance calibration circuits.
57	RW	DELAY_LINE_CTL_OVERRIDE: 0 = Normal operation. 1 = Enables only the 0^{o} delay line phase into the RDCLK PRs.
58	RW	WR_FIFO_STAB: 0 = Normal operation. 1 = All write FIFO clocks are disabled, and flush mode is set.
59	RW	Reserved.
60	RW	RX_POWERDOWN: 0 = Normal operation. 1 = Disables all DQ and DQS receivers.
61	RW	DP_TX_TRISTATE: 0 = Normal operation. 1 = Puts DQ and DQS drivers into a tri-state (high-impedance) state.
62	RW	ADR_TX_TRISTATE: 0 = Normal operation. 1 = ADR driver tri-state (high-impedance) becomes controllable by PDR2.
63	RW	VREG_S_POWERDOWN: 0 = Normal operation. 1 = Shuts off the VCC voltage regulator for all circuits other than the DLL.

Register Name	**PC Mirror Configuration Register**
Mnemonic	IOM0.DDRPHY_PC_MIRROR_CONFIG_P0
Address	8000C0110701103F (SCOM)
Description	This register provides control of the rank groups.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	ADDR_MIRROR_RP0_PRI: 1 = Enable address mirroring rank pair 0 primary.
49	RW	ADDR_MIRROR_RP0_SEC: 1 = Enable address mirroring rank pair 0 secondary.
50	RW	ADDR_MIRROR_RP1_PRI: 1 = Enable address mirroring rank pair 1 primary.
51	RW	ADDR_MIRROR_RP1_SEC: 1 = Enable address mirroring rank pair 1 secondary.
52	RW	ADDR_MIRROR_RP2_PRI: 1 = Enable address mirroring rank pair 2 primary.
53	RW	ADDR_MIRROR_RP2_SEC: 1 = Enable address mirroring rank pair 2 secondary.
54	RW	ADDR_MIRROR_RP3_PRI: 1 = Enable address mirroring rank pair 3 primary.
55	RW	ADDR_MIRROR_RP3_SEC: 1 = Enable address mirroring rank pair 3 secondary.
56:57	RW	Reserved,
58	RW	ADDR_MIRROR_A3_A4: 1 = Mirror A3 and A4 signals on mirrored ranks.
59	RW	ADDR_MIRROR_A5_A6: 1 = Mirror A5 and A6 signals on mirrored ranks.
60	RW	ADDR_MIRROR_A7_A8: 1 = Mirror A7 and A8 signals on mirrored ranks.
61	RW	ADDR_MIRROR_A11_A13: 1 = Mirror A11 and A13 signals on mirrored ranks.
62	RW	ADDR_MIRROR_BA0_BA1: 1 = Mirror BA0 and BA1 signals on mirrored ranks.
63	RW	ADDR_MIRROR_BG0_BG1: 1 = Mirror BG0 and BG1 signals on mirrored ranks.

Register Name	PC Mirror Configuration Register
Mnemonic	IOM0.DDRPHY_PC_MIRROR_CONFIG_P1
Address	8000C0110701143F (SCOM)
Description	This register provides control of the rank groups.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	ADDR_MIRROR_RP0_PRI: 1 = Enable address mirroring of rank pair 0 primary.
49	RW	ADDR_MIRROR_RP0_SEC: 1 = Enable address mirroring of rank pair 0 secondary.
50	RW	ADDR_MIRROR_RP1_PRI: 1 = Enable address mirroring of rank pair 1 primary.
51	RW	ADDR_MIRROR_RP1_SEC: 1 = Enable address mirroring of rank pair 1 secondary.
52	RW	ADDR_MIRROR_RP2_PRI: 1 = Enable address mirroring of rank pair 2 primary.
53	RW	ADDR_MIRROR_RP2_SEC: 1 = Enable address mirroring of rank pair 2 secondary.
54	RW	ADDR_MIRROR_RP3_PRI: 1 = Enable address mirroring of rank pair 3 primary.
55	RW	ADDR_MIRROR_RP3_SEC: 1 = Enable address mirroring of rank pair 3 secondary.
56:57	RW	Reserved,
58	RW	ADDR_MIRROR_A3_A4: 1 = Mirror A3 and A4 signals on mirrored ranks.
59	RW	ADDR_MIRROR_A5_A6: 1 = Mirror A5 and A6 signals on mirrored ranks.
60	RW	ADDR_MIRROR_A7_A8: 1 = Mirror A7 and A8 signals on mirrored ranks.
61	RW	ADDR_MIRROR_A11_A13: 1 = Mirror A11 and A13 signals on mirrored ranks.
62	RW	ADDR_MIRROR_BA0_BA1: 1 = Mirror BA0 and BA1 signals on mirrored ranks.
63	RW	ADDR_MIRROR_BG0_BG1: 1 = Mirror BG0 and BG1 signals on mirrored ranks.

Register Name	PC Mirror Configuration Register
Mnemonic	IOM0.DDRPHY_PC_MIRROR_CONFIG_P2
Address	8000C0110701183F (SCOM)
Description	This register provides control of the rank groups.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	ADDR_MIRROR_RP0_PRI: 1 = Enable address mirroring of rank pair 0 primary.
49	RW	ADDR_MIRROR_RP0_SEC: 1 = Enable address mirroring of rank pair 0 secondary.
50	RW	ADDR_MIRROR_RP1_PRI: 1 = Enable address mirroring of rank pair 1 primary.
51	RW	ADDR_MIRROR_RP1_SEC: 1 = Enable address mirroring of rank pair 1 secondary.
52	RW	ADDR_MIRROR_RP2_PRI: 1 = Enable address mirroring of rank pair 2 primary.
53	RW	ADDR_MIRROR_RP2_SEC: 1 = Enable address mirroring of rank pair 2 secondary.
54	RW	ADDR_MIRROR_RP3_PRI: 1 = Enable address mirroring of rank pair 3 primary.
55	RW	ADDR_MIRROR_RP3_SEC: 1 = Enable address mirroring of rank pair 3 secondary.
56:57	RW	Reserved,
58	RW	ADDR_MIRROR_A3_A4: 1 = Mirror A3 and A4 signals on mirrored ranks.
59	RW	ADDR_MIRROR_A5_A6: 1 = Mirror A5 and A6 signals on mirrored ranks.
60	RW	ADDR_MIRROR_A7_A8: 1 = Mirror A7 and A8 signals on mirrored ranks.
61	RW	ADDR_MIRROR_A11_A13: 1 = Mirror A11 and A13 signals on mirrored ranks.
62	RW	ADDR_MIRROR_BA0_BA1: 1 = Mirror BA0 and BA1 signals on mirrored ranks.
63	RW	ADDR_MIRROR_BG0_BG1: 1 = Mirror BG0 and BG1 signals on mirrored ranks.

Register Name	PC Mirror Configuration Register
Mnemonic	IOM0.DDRPHY_PC_MIRROR_CONFIG_P3
Address	8000C01107011C3F (SCOM)
Description	This register provides control of the rank groups.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	ADDR_MIRROR_RP0_PRI: 1 = Enable address mirroring of rank pair 0 primary.
49	RW	ADDR_MIRROR_RP0_SEC: 1 = Enable address mirroring of rank pair 0 secondary.
50	RW	ADDR_MIRROR_RP1_PRI: 1 = Enable address mirroring of rank pair 1 primary.
51	RW	ADDR_MIRROR_RP1_SEC: 1 = Enable address mirroring of rank pair 1 secondary.
52	RW	ADDR_MIRROR_RP2_PRI: 1 = Enable address mirroring of rank pair 2 primary.
53	RW	ADDR_MIRROR_RP2_SEC: 1 = Enable address mirroring of rank pair 2 secondary.
54	RW	ADDR_MIRROR_RP3_PRI: 1 = Enable address mirroring of rank pair 3 primary.
55	RW	ADDR_MIRROR_RP3_SEC: 1 = Enable address mirroring of rank pair 3 secondary.
56:57	RW	Reserved,

Bits	SCOM	Field Mnemonic: Description
58	RW	ADDR_MIRROR_A3_A4: 1 = Mirror A3 and A4 signals on mirrored ranks.
59	RW	ADDR_MIRROR_A5_A6: 1 = Mirror A5 and A6 signals on mirrored ranks.
60	RW	ADDR_MIRROR_A7_A8: 1 = Mirror A7 and A8 signals on mirrored ranks.
61	RW	ADDR_MIRROR_A11_A13: 1 = Mirror A11 and A13 signals on mirrored ranks.
62	RW	ADDR_MIRROR_BA0_BA1: 1 = Mirror BA0 and BA1 signals on mirrored ranks.
63	RW	ADDR_MIRROR_BG0_BG1: 1 = Mirror BG0 and BG1 signals on mirrored ranks.

Register Name	**PC Error Status 0 Register**
Mnemonic	IOM0.DDRPHY_PC_ERROR_STATUS0_P0
Address	8000C0120701103F (SCOM)
Description	This register is the top-level error reporting register. When a bit in this register is set, and it is not masked in the PC Error Mask 0 Register, the pc_memctl_error_o/pc_memctl_errorb_o output of the DDR PHY core is asserted.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RWX	RC_ERROR: 1 = Error in read control logic.
49	RWX	WC_ERROR: 1 = Error in write control logic.
50	RWX	SEQ_ERROR: 1 = Error in sequencer control logic.
51	RWX	Reserved.
52	RWX	APB_ERROR: 1 = Error in register interface logic.
53	RWX	PC_ERROR: 1 = Error in PHY control logic.
54:63	RO	Constant = 0b0000000000

Register Name	**PC Error Status 0 Register**
Mnemonic	IOM0.DDRPHY_PC_ERROR_STATUS0_P1
Address	8000C0120701143F (SCOM)
Description	This register is the top-level error reporting register. When a bit in this register is set, and it is not masked in the PC Error Mask 0 Register, the pc_memctl_error_o/pc_memctl_errorb_o output of the DDR PHY core is asserted.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RWX	RC_ERROR: 1 = Error in read control logic.
49	RWX	WC_ERROR: 1 = Error in write control logic.
50	RWX	SEQ_ERROR: 1 = Error in sequencer control logic.
51	RWX	Reserved
52	RWX	APB_ERROR: 1 = Error in register interface logic.
53	RWX	PC_ERROR: 1 = Error in PHY control logic.
54:63	RO	Constant = 0b0000000000

Register Name	PC Error Status 0 Register
Mnemonic	IOM0.DDRPHY_PC_ERROR_STATUS0_P2
Address	8000C0120701183F (SCOM)
Description	This register is the top-level error reporting register. When a bit in this register is set, and it is not masked in the PC Error Mask 0 Register, the pc_memctl_error_o/pc_memctl_errorb_o output of the DDR PHY core is asserted.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RWX	RC_ERROR: 1 = Error in read control logic.
49	RWX	WC_ERROR: 1 = Error in write control logic.
50	RWX	SEQ_ERROR: 1 = Error in sequencer control logic.
51	RWX	Reserved.
52	RWX	APB_ERROR: 1 = Error in register interface logic.
53	RWX	PC_ERROR: 1 = Error in PHY control logic.
54:63	RO	Constant = 0b0000000000

Register Name	PC Error Status 0 Register
Mnemonic	IOM0.DDRPHY_PC_ERROR_STATUS0_P3
Address	8000C01207011C3F (SCOM)
Description	This register is the top-level error reporting register. When a bit in this register is set, and it is not masked in the PC Error Mask 0 Register, the pc_memctl_error_o/pc_memctl_errorb_o output of the DDR PHY core is asserted.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RWX	RC_ERROR: 1 = Error in read control logic.
49	RWX	WC_ERROR: 1 = Error in write control logic.
50	RWX	SEQ_ERROR: 1 = Error in sequencer control logic.
51	RWX	Reserved.
52	RWX	APB_ERROR: 1 = Error in register interface logic.
53	RWX	PC_ERROR: 1 = Error in PHY control logic.
54:63	RO	Constant = 0b0000000000

Register Name	PC Error Mask 0 Register
Mnemonic	IOM0.DDRPHY_PC_ERROR_MASK0_P0
Address	8000C0130701103F (SCOM)
Description	This register masks errors in the PC Error Status 0 Register. Thus, it prevents the assertion of the pc_memctl_error_o/pc_memctl_errorb_o output.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	RC_ERROR_MASK: 1 = Mask errors in read control logic.
49	RW	WC_ERROR_MASK: 1 = Mask errors in write control logic.
50	RW	SEQ_ERROR_MASK: 1 = Mask errors in sequencer control logic.
51	RW	Reserved.
52	RW	APB_ERROR_MASK: 1 = Mask errors in register interface logic.
53	RW	PC_ERROR_MASK: 1 = Mask errors in PHY control logic.
54:63	RO	Constant = 0b0000000000

Register Name	PC Error Mask 0 Register
Mnemonic	IOM0.DDRPHY_PC_ERROR_MASK0_P1
Address	8000C0130701143F (SCOM)
Description	This register masks errors in the PC Error Status 0 Register. Thus, it prevents the assertion of the pc_memctl_error_o/pc_memctl_errorb_o output.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	RC_ERROR_MASK: 1 = Mask errors in read control logic.
49	RW	WC_ERROR_MASK: 1 = Mask errors in write control logic.
50	RW	SEQ_ERROR_MASK: 1 = Mask errors in sequencer control logic.
51	RW	Reserved.
52	RW	APB_ERROR_MASK: 1 = Mask errors in register interface logic.
53	RW	PC_ERROR_MASK: 1 = Mask errors in PHY control logic.
54:63	RO	Constant = 0b0000000000

Register Name	PC Error Mask 0 Register
Mnemonic	IOM0.DDRPHY_PC_ERROR_MASK0_P2
Address	8000C0130701183F (SCOM)
Description	This register masks errors in the PC Error Status 0 Register. Thus, it prevents the assertion of the pc_memctl_error_o/pc_memctl_errorb_o output.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	RC_ERROR_MASK: 1 = Mask errors in read control logic.
49	RW	WC_ERROR_MASK: 1 = Mask errors in write control logic.
50	RW	SEQ_ERROR_MASK: 1 = Mask errors in sequencer control logic.
51	RW	Reserved.
52	RW	APB_ERROR_MASK: 1 = Mask errors in register interface logic.
53	RW	PC_ERROR_MASK: 1 = Mask errors in PHY control logic.
54:63	RO	Constant = 0b0000000000

Register Name	PC Error Mask 0 Register
Mnemonic	IOM0.DDRPHY_PC_ERROR_MASK0_P3
Address	8000C01307011C3F (SCOM)
Description	This register masks errors in the PC Error Status 0 Register. Thus, it prevents the assertion of the pc_memctl_error_o/pc_memctl_errorb_o output.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48	RW	RC_ERROR_MASK: 1 = Mask errors in read control logic.
49	RW	WC_ERROR_MASK: 1 = Mask errors in write control logic.
50	RW	SEQ_ERROR_MASK: 1 = Mask errors in sequencer control logic.
51	RW	Reserved.
52	RW	APB_ERROR_MASK: 1 = Mask errors in register interface logic.
53	RW	PC_ERROR_MASK: 1 = Mask errors in PHY control logic.
54:63	RO	Constant = 0b0000000000

Register Name	PC IO PVT N/P FET Driver Control Register
Mnemonic	IOM0.DDRPHY_PC_IO_PVT_FET_CONTROL_P0
Address	8000C0140701103F (SCOM)
Description	This register overrides the values coming into the DDR PHY core from the internal impedance controller, and controls the impedance controller connected to the interface.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48	RW	PVTPB: Positive field-effect transistor (PFET) binary driver PVTP value to send to all output drivers when PVT_OVERRIDE is set.
49:55	RW	PVTPL: PFET linear driver PVTP value to send to all output drivers when PVT_OVERRIDE is set.
56	RW	PVTNB: Negative field-effect transistor (NFET) binary driver PVTN value to send to all output drivers when PVT_OVERRIDE is set.
57:63	RW	PVTNL: NFET linear driver PVTN value to send to all output drivers when PVT_OVERRIDE is set.

Register Name	PC IO PVT N/P FET Driver Control Register
Mnemonic	IOM0.DDRPHY_PC_IO_PVT_FET_CONTROL_P1
Address	8000C0140701143F (SCOM)
Description	This register overrides the values coming into the DDR PHY core from the internal impedance controller, and controls the impedance controller connected to the interface.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48	RW	PVTPB: PFET binary driver PVTP value to send to all output drivers when PVT_OVERRIDE is set.
49:55	RW	PVTPL: PFET linear driver PVTP value to send to all output drivers when PVT_OVERRIDE is set.

Bits	SCOM	Field Mnemonic: Description
56	RW	PVTNB: NFET binary driver PVTN value to send to all output drivers when PVT_OVERRIDE is set.
57:63	RW	PVTNL: NFET linear driver PVTN value to send to all output drivers when PVT_OVERRIDE is set.

Register Name	PC IO PVT N/P FET Driver Control Register
Mnemonic	IOM0.DDRPHY_PC_IO_PVT_FET_CONTROL_P2
Address	8000C0140701183F (SCOM)
Description	This register overrides the values coming into the DDR PHY core from the internal impedance controller, and controls the impedance controller connected to the interface.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	PVTPB: PFET binary driver PVTP value to send to all output drivers when PVT_OVERRIDE is set.
49:55	RW	PVTPL: PFET linear driver PVTP value to send to all output drivers when PVT_OVERRIDE is set.
56	RW	PVTNB: NFET binary driver PVTN value to send to all output drivers when PVT_OVERRIDE is set.
57:63	RW	PVTNL: NFET linear driver PVTN value to send to all output drivers when PVT_OVERRIDE is set.

Register Name	PC IO PVT N/P FET Driver Control Register
Mnemonic	IOM0.DDRPHY_PC_IO_PVT_FET_CONTROL_P3
Address	8000C01407011C3F (SCOM)
Description	This register overrides the values coming into the DDR PHY core from the internal impedance controller, and controls the impedance controller connected to the interface.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	PVTPB: PFET binary driver PVTP value to send to all output drivers when PVT_OVERRIDE is set.
49:55	RW	PVTPL: PFET linear driver PVTP value to send to all output drivers when PVT_OVERRIDE is set.
56	RW	PVTNB: NFET binary driver PVTN value to send to all output drivers when PVT_OVERRIDE is set.
57:63	RW	PVTNL: NFET linear driver PVTN value to send to all output drivers when PVT_OVERRIDE is set.

Register Name	PC PBA Control Register
Mnemonic	IOM0.DDRPHY_PC_PBA_CONTROL_P0
Address	8000C0150701103F (SCOM)
Description	This register is used for per-buffer addressability (PBA) mode control settings.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Reserved.
48	RWX	SNOOPED_F0RC4X_BIT4: Snooped value of bit 4 from the F0RC4X RCD control word write to LRDIMM CSN0, representing A12 of CW data control word writes.
49:50	RWX	PHY_CSN_MAP: Actual PHY CSN that is mapped to LRDIMM CSN0. Required to determine which CSN should be snooped for the F0RC4X bit 4 value. Only LRDIMM CSN0 is valid.

Bits	SCOM	Field Mnemonic: Description
51:63	RO	Reserved.

Register Name	PC PBA Control Register
Mnemonic	IOM0.DDRPHY_PC_PBA_CONTROL_P1
Address	8000C0150701143F (SCOM)
Description	This register is used for per-buffer addressability (PBA) mode control settings.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Reserved.
48	RWX	SNOOPED_F0RC4X_BIT4: Snooped value of bit 4 from the F0RC4X register clock driver (RCD) control word write to LRDIMM CSN0, representing A12 of CW data control word writes.
49:50	RWX	PHY_CSN_MAP: Actual PHY CSN that is mapped to LRDIMM CSN0. Required to determine which CSN should be snooped for the F0RC4X bit 4 value. Only LRDIMM CSN0 is valid.
51:63	RO	Reserved.

Register Name	PC PBA Control Register
Mnemonic	IOM0.DDRPHY_PC_PBA_CONTROL_P2
Address	8000C0150701183F (SCOM)
Description	This register is used for per-buffer addressability (PBA) mode control settings.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Reserved.
48	RWX	SNOOPED_F0RC4X_BIT4: Snooped value of bit 4 from the F0RC4X RCD control word write to LRDIMM CSN0, representing A12 of CW data control word writes.
49:50	RWX	PHY_CSN_MAP: Actual PHY CSN that is mapped to LRDIMM CSN0. Required to determine which CSN should be snooped for the F0RC4X bit 4 value. Only LRDIMM CSN0 is valid.
51:63	RO	Reserved.

Register Name	PC PBA Control Register
Mnemonic	IOM0.DDRPHY_PC_PBA_CONTROL_P3
Address	8000C01507011C3F (SCOM)
Description	This register is used for per-buffer addressability (PBA) mode control settings.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Reserved.
48	RWX	SNOOPED_F0RC4X_BIT4: Snooped value of bit 4 from the F0RC4X RCD control word write to LRDIMM CSN0, representing A12 of CW data control word writes.
49:50	RWX	PHY_CSN_MAP: Actual PHY CSN that is mapped to LRDIMM CSN0. Required to determine which CSN should be snooped for the F0RC4X bit 4 value. Only LRDIMM CSN0 is valid.
51:63	RO	Reserved.

Register Name	PC Initial Calibration Config0 Register
Mnemonic	IOM0.DDRPHY_PC_INIT_CAL_CONFIG0_P0
Address	8000C0160701103F (SCOM)
Description	This register controls the initial calibration sequence performed by the PHY. This register specifies which calibration routines and algorithms are run. When more than one calibration routine or algorithm is selected, they are executed sequentially from the lowest-bit-numbered to the highest-bit-numbered enabled routine or algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	ENA_WR_LEVEL: Enable write leveling during initial calibration.
49	RW	ENA_INITIAL_PAT_WR: Enable an initial-pattern write during initial calibration. This bit must be set when performing read centering or write centering on memory devices that do not generate an MPR pattern. This bit must be set when performing custom read centering or custom write centering. If custom read centering or custom write centering was performed, an initial-pattern write of 5555 hex, the reset value of the SEQ Read/Write Data {0-1} Registers, must be performed before any periodic calibration routines are performed.
50	RW	ENA_DQS_ALIGN: Enable DQS (read) alignment during initial calibration.
51	RW	ENA_RDCLK_ALIGN: Enable the alignment of the internal SYSCLK to the read clock during initial calibration. This calibration step requires the DQS (read) alignment calibration step to have been performed.
52	RW	ENA_READ_CTR: Enable read centering during initial calibration. This calibration step requires the SYSCLK-to-read-clock alignment to have been performed. This bit must also be set to allow the read VREF to be enabled in the RC Read VREF Configuration 1 Register. The read VREF is required for read centering.
53	RW	ENA_WRITE_CTR: Enable write centering during initial calibration. This calibration step requires the read centering calibration step to have been performed.
54	RW	ENA_INITIAL_COARSE_WR: Enable an initial coarse pattern write during initial calibration. This calibration step requires the write centering calibration step to have been performed.
55	RW	ENA_COARSE_RD: Enable coarse read centering during initial calibration. This calibration step requires the initial coarse pattern write calibration step to have been performed.
56	RW	ENA_CUSTOM_RD: Enable the use of a custom read pattern during initial calibration. This algorithm is not required to be run to calibrate the PHY. If it is run, it must be performed after the coarse read algorithm has been run. When this bit is set, bit 49 must be set and bits 48, 50, 51, 52, 53, 54, and 55 must be reset. This bit is reserved. It must be written to zero for correct operation.
57	RW	ENA_CUSTOM_WR: Enable the use of a custom write pattern during initial calibration. This algorithm is not required to be run to calibrate the PHY. If it is run, it must be performed after the coarse read algorithm has been run. When this bit is set, bit 49 must be set and bits 48, 50, 51, 52, 53, 54, and 55 must be reset. This bit is reserved. It must be written to zero for correct operation.
58	RW	ABORT_ON_CAL_ERROR: Stop the initial calibration sequence if an error occurs. If more than one calibration algorithm is enabled and an error occurs before the last calibration algorithm is started, the PHY does not perform any calibration algorithm after the errant calibration algorithm completes. The one exception is write leveling. If there is an error in any initial calibration step, the PHY continues to execute write leveling on the remaining ranks in the rank group. This can result in multiple error bits getting set.
59	RW	ENA_DIGITAL_EYE: Enable the internal digital eye characterization assist logic. Do not run this algorithm during normal calibration.
60:63	RW	ENA_RANK_PAIR: Enable rank pair. 1 = Enabled. 0 = Disabled. Bit 60 contains the enable for rank pair 0. Bit 61 contains the enable for rank pair 1. Bit 62 contains the enable for rank pair 2. Bit 63 contains the enable for rank pair 3.

Register Name	PC Initial Calibration Config0 Register
Mnemonic	IOM0.DDRPHY_PC_INIT_CAL_CONFIG0_P1
Address	8000C0160701143F (SCOM)
Description	This register controls the initial calibration sequence performed by the PHY. This register specifies which calibration routines and algorithms are run. When more than one calibration routine or algorithm is selected, they are executed sequentially from the lowest-bit-numbered to the highest-bit-numbered enabled routine or algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	ENA_WR_LEVEL: Enable write leveling during initial calibration.
49	RW	ENA_INITIAL_PAT_WR: Enable an initial-pattern write during initial calibration. This bit must be set when performing read centering or write centering on memory devices that do not generate an MPR pattern. This bit must be set when performing custom read centering or custom write centering. If custom read centering or custom write centering was performed, an initial-pattern write of 5555 hex, the reset value of the SEQ Read/Write Data {0-1} Registers, must be performed before any periodic calibration routines are performed.
50	RW	ENA_DQS_ALIGN: Enable DQS (read) alignment during initial calibration.
51	RW	ENA_RDCLK_ALIGN: Enable the alignment of the internal SYSCLK to the read clock during initial calibration. This calibration step requires the DQS (read) alignment calibration step to have been performed.
52	RW	ENA_READ_CTR: Enable read centering during initial calibration. This calibration step requires the SYSCLK-to-read-clock alignment to have been performed. This bit must also be set to allow the read VREF to be enabled in the RC Read VREF Configuration 1 Register. The read VREF is required for read centering.
53	RW	ENA_INITIAL_COARSE_WR: Enable an initial coarse pattern write during initial calibration. This calibration step requires the write centering calibration step to have been performed
54	RW	ENA_INITIAL_COARSE_WR: Enable an initial coarse pattern write during initial calibration. This calibration step requires the write centering calibration step to have been performed.
55	RW	ENA_COARSE_RD: Enable coarse read centering during initial calibration. This calibration step requires the initial coarse pattern write calibration step to have been performed.
56	RW	ENA_CUSTOM_RD: Enable the use of a custom read pattern during initial calibration. This algorithm is not required to be run to calibrate the PHY. If it is run, it must be performed after the coarse read algorithm has been run. When this bit is set, bit 49 must be set and bits 48, 50, 51, 52, 53, 54, and 55 must be reset. This bit is reserved. It must be written to zero for correct operation.
57	RW	ENA_CUSTOM_WR: Enable the use of a custom write pattern during initial calibration. This algorithm is not required to be run to calibrate the PHY. If it is run, it must be performed after the coarse read algorithm has been run. When this bit is set, bit 49 must be set and bits 48, 50, 51, 52, 53, 54, and 55 must be reset. This bit is reserved. It must be written to zero for correct operation.
58	RW	ABORT_ON_CAL_ERROR: Stop the initial calibration sequence if an error occurs. If more than one calibration algorithm is enabled and an error occurs before the last calibration algorithm is started, the PHY does not perform any calibration algorithm after the errant calibration algorithm completes. The one exception is write leveling. If there is an error in any initial calibration step, the PHY continues to execute write leveling on the remaining ranks in the rank group. This can result in multiple error bits getting set.
59	RW	ENA_DIGITAL_EYE: Enable the internal digital eye characterization assist logic. Do not run this algorithm during normal calibration.

Bits	SCOM	Field Mnemonic: Description
60:63	RW	ENA_RANK_PAIR: Enable rank pair. 1 = Enabled. 0 = Disabled. Bit 60 contains the enable for rank pair 0. Bit 61 contains the enable for rank pair 1. Bit 62 contains the enable for rank pair 2. Bit 63 contains the enable for rank pair 3.

Register Name	**PC Initial Calibration Config0 Register**
Mnemonic	IOM0.DDRPHY_PC_INIT_CAL_CONFIG0_P2
Address	8000C0160701183F (SCOM)
Description	This register controls the initial calibration sequence performed by the PHY. This register specifies which calibration routines and algorithms are run. When more than one calibration routine or algorithm is selected, they are executed sequentially from the lowest-bit-numbered to the highest-bit-numbered enabled routine or algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	ENA_WR_LEVEL: Enable write leveling during initial calibration.
49	RW	ENA_INITIAL_PAT_WR: Enable an initial-pattern write during initial calibration. This bit must be set when performing read centering or write centering on memory devices that do not generate an MPR pattern. This bit must be set when performing custom read centering or custom write centering. If custom read centering or custom write centering was performed, an initial-pattern write of 5555 hex, the reset value of the SEQ Read/Write Data {0-1} Registers, must be performed before any periodic calibration routines are performed.
50	RW	ENA_DQS_ALIGN: Enable DQS (read) alignment during initial calibration.
51	RW	ENA_RDCLK_ALIGN: Enable the alignment of the internal SYSCLK to the read clock during initial calibration. This calibration step requires the DQS (read) alignment calibration step to have been performed.
52	RW	ENA_READ_CTR: Enable read centering during initial calibration. This calibration step requires the SYSCLK-to-read-clock alignment to have been performed. This bit must also be set to allow the read VREF to be enabled in the RC Read VREF Configuration 1 Register. The read VREF is required for read centering.
53	RW	ENA_INITIAL_COARSE_WR: Enable an initial coarse pattern write during initial calibration. This calibration step requires the write centering calibration step to have been performed
54	RW	ENA_INITIAL_COARSE_WR: Enable an initial coarse pattern write during initial calibration. This calibration step requires the write centering calibration step to have been performed.
55	RW	ENA_COARSE_RD: Enable coarse read centering during initial calibration. This calibration step requires the initial coarse pattern write calibration step to have been performed.
56	RW	ENA_CUSTOM_RD: Enable the use of a custom read pattern during initial calibration. This algorithm is not required to be run to calibrate the PHY. If it is run, it must be performed after the coarse read algorithm has been run. When this bit is set, bit 49 must be set and bits 48, 50, 51, 52, 53, 54, and 55 must be reset. This bit is reserved. It must be written to zero for correct operation.
57	RW	ENA_CUSTOM_WR: Enable the use of a custom write pattern during initial calibration. This algorithm is not required to be run to calibrate the PHY. If it is run, it must be performed after the coarse read algorithm has been run. When this bit is set, bit 49 must be set and bits 48, 50, 51, 52, 53, 54, and 55 must be reset. This bit is reserved. It must be written to zero for correct operation.

Bits	SCOM	Field Mnemonic: Description
58	RW	ABORT_ON_CAL_ERROR: Stop the initial calibration sequence if an error occurs. If more than one calibration algorithm is enabled and an error occurs before the last calibration algorithm is started, the PHY does not perform any calibration algorithm after the errant calibration algorithm completes. The one exception is write leveling. If there is an error in any initial calibration step, the PHY continues to execute write leveling on the remaining ranks in the rank group. This can result in multiple error bits getting set.
59	RW	ENA_DIGITAL_EYE: Enable the internal digital eye characterization assist logic. Do not run this algorithm during normal calibration.
60:63	RW	ENA_RANK_PAIR: Enable rank pair. 1 = Enabled. 0 = Disabled. Bit 60 contains the enable for rank pair 0. Bit 61 contains the enable for rank pair 1. Bit 62 contains the enable for rank pair 2. Bit 63 contains the enable for rank pair 3.

Register Name	PC Initial Calibration Config0 Register
Mnemonic	IOM0.DDRPHY_PC_INIT_CAL_CONFIG0_P3
Address	8000C01607011C3F (SCOM)
Description	This register controls the initial calibration sequence performed by the PHY. This register specifies which calibration routines and algorithms are run. When more than one calibration routine or algorithm is selected, they are executed sequentially from the lowest-bit-numbered to the highest-bit-numbered enabled routine or algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	ENA_WR_LEVEL: Enable write leveling during initial calibration.
49	RW	ENA_INITIAL_PAT_WR: Enable an initial-pattern write during initial calibration. This bit must be set when performing read centering or write centering on memory devices that do not generate an MPR pattern. This bit must be set when performing custom read centering or custom write centering. If custom read centering or custom write centering was performed, an initial-pattern write of 5555 hex, the reset value of the SEQ Read/Write Data {0-1} Registers, must be performed before any periodic calibration routines are performed.
50	RW	ENA_DQS_ALIGN: Enable DQS (read) alignment during initial calibration.
51	RW	ENA_RDCLK_ALIGN: Enable the alignment of the internal SYSCLK to the read clock during initial calibration. This calibration step requires the DQS (read) alignment calibration step to have been performed.
52	RW	ENA_READ_CTR: Enable read centering during initial calibration. This calibration step requires the SYSCLK-to-read-clock alignment to have been performed. This bit must also be set to allow the read VREF to be enabled in the RC Read VREF Configuration 1 Register. The read VREF is required for read centering.
53	RW	ENA_INITIAL_COARSE_WR: Enable an initial coarse pattern write during initial calibration. This calibration step requires the write centering calibration step to have been performed
54	RW	ENA_INITIAL_COARSE_WR: Enable an initial coarse pattern write during initial calibration. This calibration step requires the write centering calibration step to have been performed.
55	RW	ENA_COARSE_RD: Enable coarse read centering during initial calibration. This calibration step requires the initial coarse pattern write calibration step to have been performed.
56	RW	ENA_CUSTOM_RD: Enable the use of a custom read pattern during initial calibration. This algorithm is not required to be run to calibrate the PHY. If it is run, it must be performed after the coarse read algorithm has been run. When this bit is set, bit 49 must be set and bits 48, 50, 51, 52, 53, 54, and 55 must be reset. This bit is reserved. It must be written to zero for correct operation.

Bits	SCOM	Field Mnemonic: Description
57	RW	ENA_CUSTOM_WR: Enable the use of a custom write pattern during initial calibration. This algorithm is not required to be run to calibrate the PHY. If it is run, it must be performed after the coarse read algorithm has been run. When this bit is set, bit 49 must be set and bits 48, 50, 51, 52, 53, 54, and 55 must be reset. This bit is reserved. It must be written to zero for correct operation.
58	RW	ABORT_ON_CAL_ERROR: Stop the initial calibration sequence if an error occurs. If more than one calibration algorithm is enabled and an error occurs before the last calibration algorithm is started, the PHY does not perform any calibration algorithm after the errant calibration algorithm completes. The one exception is write leveling. If there is an error in any initial calibration step, the PHY continues to execute write leveling on the remaining ranks in the rank group. This can result in multiple error bits getting set.
59	RW	ENA_DIGITAL_EYE: Enable the internal digital eye characterization assist logic. Do not run this algorithm during normal calibration.
60:63	RW	ENA_RANK_PAIR: Enable rank pair. 1 = Enabled. 0 = Disabled. Bit 60 contains the enable for rank pair 0. Bit 61 contains the enable for rank pair 1. Bit 62 contains the enable for rank pair 2. Bit 63 contains the enable for rank pair 3.

Register Name	PC Initial Calibration Config1 Register
Mnemonic	IOM0.DDRPHY_PC_INIT_CAL_CONFIG1_P0
Address	8000C0170701103F (SCOM)
Description	This register controls the initial calibration sequence performed by the PHY.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	REFRESH_COUNT: The refresh count specifies the number of refresh commands to insert at the start of an initial calibration. The value zero causes no refresh commands to be sent when an initial calibration begins.
52:53	RW	REFRESH_CONTROL: This field is used to control the refresh logic during initial calibration: 00 = Refresh commands are only sent at start of initial calibration, based on the value in the REFRESH_COUNT field. 01 = Use the internal refresh interval timer to determine when refresh commands are sent. Allow refreshes to occur between calibration routines. 10 = Reserved. 11 = Use the internal refresh interval timer to determine when refresh commands should be sent. In addition to allowing refresh commands to be issued between calibration routines, also allow refreshes to interrupt each calibration routine (as required). This is the recommended setting when refreshes are required during initial calibration.
54	RW	REFRESH_ALL_RANKS: 0 = One refresh command is sent to the rank currently being calibrated. 1 = All ranks are refreshed during initial calibration. One refresh command is sent to each rank sequentially to refresh all ranks.
55	RW	CMD_SNOOP_DIS: 0 = Normal operation. 1 = Disable PHY control command snoop.
56	RW	MRS_SNOOP_DIS: 0 = Normal operation. 1 = Disable MRS write snooping.

Bits	SCOM	Field Mnemonic: Description
57:63	RW	REFRESH_INTERVAL: This refresh interval value times 256 is the number of MEMINTCLKO cycles to wait between sending refresh commands to the memory (tREFI). This value is used when the REFRESH_CONTROL field is configured to use the internal refresh interval timer. 0000001 (minimum value) = 256 MEMINTCLKO cycles between refreshes. 1111111 (maximum value) = 32,512 MEMINTCLKO cycle between refreshes. For example, for a DDR:1600 system running with an 800 MHz memory controller clock frequency, the value 24 (0011000b) provides a tREFI setting of 7.68 µs (that is, 24 x 256 cycles x 1.25 ns period yields = 7.68 µs). The minimum value for this field is 6. If a value less than 6 is written to this field, this field is set to 6 by hardware. When the refresh interval counter expires, an internal pending refresh counter is incremented to count the number of pending refreshes. When refresh commands are issued during initial calibration, all pending refreshes are issued and the internal counter is decremented to zero. The internal pending refresh counter is a 4-bit counter with a maximum value of 15d. An error bit sets the PC_ERROR bit in the PC Error Status 0 Register if the internal pending refresh counter overflows.

Register Name	PC Initial Calibration Config1 Register
Mnemonic	IOM0.DDRPHY_PC_INIT_CAL_CONFIG1_P1
Address	8000C0170701143F (SCOM)
Description	This register controls the initial calibration sequence performed by the PHY.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	REFRESH_COUNT: The refresh count specifies the number of refresh commands to insert at the start of an initial calibration. The value zero causes no refresh commands to be sent when an initial calibration begins.
52:53	RW	REFRESH_CONTROL: This field is used to control the refresh logic during initial calibration: 00 = Refresh commands are only sent at start of initial calibration, based on the value in the REFRESH_COUNT field. 01 = Use the internal refresh interval timer to determine when refresh commands are sent. Allow refreshes to occur between calibration routines. 10 = Reserved. 11 = Use the internal refresh interval timer to determine when refresh commands should be sent. In addition to allowing refresh commands to be issued between calibration routines, also allow refreshes to interrupt each calibration routine (as required). This is the recommended setting when refreshes are required during initial calibration.
54	RW	REFRESH_ALL_RANKS: 0 = One refresh command is sent to the rank currently being calibrated. 1 = All ranks are refreshed during initial calibration. One refresh command is sent to each rank sequentially to refresh all ranks.
55	RW	CMD_SNOOP_DIS: 0 = Normal operation. 1 = Disable PHY control command snoop.
56	RW	MRS_SNOOP_DIS: 0 = Normal operation. 1 = Disable MRS write snooping.

Bits	SCOM	Field Mnemonic: Description
57:63	RW	REFRESH_INTERVAL: This refresh interval value times 256 is the number of MEMINTCLKO cycles to wait between sending refresh commands to the memory (tREFI). This value is used when the REFRESH_CONTROL field is configured to use the internal refresh interval timer. 0000001 (minimum value) = 256 MEMINTCLKO cycles between refreshes. 1111111 (maximum value) = 32,512 MEMINTCLKO cycle between refreshes. For example, for a DDR:1600 system running with an 800 MHz memory controller clock frequency, the value 24 (0011000b) provides a tREFI setting of 7.68 µs (that is, 24 x 256 cycles x 1.25 ns period yields = 7.68 µs). The minimum value for this field is 6. If a value less than 6 is written to this field, this field is set to 6 by hardware. When the refresh interval counter expires, an internal pending refresh counter is incremented to count the number of pending refreshes. When refresh commands are issued during initial calibration, all pending refreshes are issued and the internal counter is decremented to zero. The internal pending refresh counter is a 4-bit counter with a maximum value of 15d. An error bit sets the PC_ERROR bit in the PC Error Status 0 Register if the internal pending refresh counter overflows.

Register Name	PC Initial Calibration Config1 Register
Mnemonic	IOM0.DDRPHY_PC_INIT_CAL_CONFIG1_P2
Address	8000C0170701183F (SCOM)
Description	This register controls the initial calibration sequence performed by the PHY.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	REFRESH_COUNT: The refresh count specifies the number of refresh commands to insert at the start of an initial calibration. The value zero causes no refresh commands to be sent when an initial calibration begins.
52:53	RW	REFRESH_CONTROL: This field is used to control the refresh logic during initial calibration: 00 = Refresh commands are only sent at start of initial calibration, based on the value in the REFRESH_COUNT field. 01 = Use the internal refresh interval timer to determine when refresh commands are sent. Allow refreshes to occur between calibration routines. 10 = Reserved. 11 = Use the internal refresh interval timer to determine when refresh commands should be sent. In addition to allowing refresh commands to be issued between calibration routines, also allow refreshes to interrupt each calibration routine (as required). This is the recommended setting when refreshes are required during initial calibration.
54	RW	REFRESH_ALL_RANKS: 0 = One refresh command is sent to the rank currently being calibrated. 1 = All ranks are refreshed during initial calibration. One refresh command is sent to each rank sequentially to refresh all ranks.
55	RW	CMD_SNOOP_DIS: 0 = Normal operation. 1 = Disable PHY control command snoop.
56	RW	MRS_SNOOP_DIS: 0 = Normal operation. 1 = Disable MRS write snooping.

Bits	SCOM	Field Mnemonic: Description
57:63	RW	REFRESH_INTERVAL: This refresh interval value times 256 is the number of MEMINTCLKO cycles to wait between sending refresh commands to the memory (tREFI). This value is used when the REFRESH_CONTROL field is configured to use the internal refresh interval timer. 0000001 (minimum value) = 256 MEMINTCLKO cycles between refreshes. 1111111 (maximum value) = 32,512 MEMINTCLKO cycle between refreshes. For example, for a DDR:1600 system running with an 800 MHz memory controller clock frequency, the value 24 (0011000b) provides a tREFI setting of 7.68 µs (that is, 24 x 256 cycles x 1.25 ns period yields = 7.68 µs). The minimum value for this field is 6. If a value less than 6 is written to this field, this field is set to 6 by hardware. When the refresh interval counter expires, an internal pending refresh counter is incremented to count the number of pending refreshes. When refresh commands are issued during initial calibration, all pending refreshes are issued and the internal counter is decremented to zero. The internal pending refresh counter is a 4-bit counter with a maximum value of 15d. An error bit sets the PC_ERROR bit in the PC Error Status 0 Register if the internal pending refresh counter overflows.

Register Name	PC Initial Calibration Config1 Register
Mnemonic	IOM0.DDRPHY_PC_INIT_CAL_CONFIG1_P3
Address	8000C01707011C3F (SCOM)
Description	This register controls the initial calibration sequence performed by the PHY.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	REFRESH_COUNT: The refresh count specifies the number of refresh commands to insert at the start of an initial calibration. The value zero causes no refresh commands to be sent when an initial calibration begins.
52:53	RW	REFRESH_CONTROL: This field is used to control the refresh logic during initial calibration: 00 = Refresh commands are only sent at start of initial calibration, based on the value in the REFRESH_COUNT field. 01 = Use the internal refresh interval timer to determine when refresh commands are sent. Allow refreshes to occur between calibration routines. 10 = Reserved. 11 = Use the internal refresh interval timer to determine when refresh commands should be sent. In addition to allowing refresh commands to be issued between calibration routines, also allow refreshes to interrupt each calibration routine (as required). This is the recommended setting when refreshes are required during initial calibration.
54	RW	REFRESH_ALL_RANKS: 0 = One refresh command is sent to the rank currently being calibrated. 1 = All ranks are refreshed during initial calibration. One refresh command is sent to each rank sequentially to refresh all ranks.
55	RW	CMD_SNOOP_DIS: 0 = Normal operation. 1 = Disable PHY control command snoop.
56	RW	MRS_SNOOP_DIS: 0 = Normal operation. 1 = Disable MRS write snooping.

Bits	SCOM	Field Mnemonic: Description
57:63	RW	REFRESH_INTERVAL: This refresh interval value times 256 is the number of MEMINTCLKO cycles to wait between sending refresh commands to the memory (tREFI). This value is used when the REFRESH_CONTROL field is configured to use the internal refresh interval timer. 0000001 (minimum value) = 256 MEMINTCLKO cycles between refreshes. 1111111 (maximum value) = 32,512 MEMINTCLKO cycle between refreshes. For example, for a DDR:1600 system running with an 800 MHz memory controller clock frequency, the value 24 (0011000b) provides a tREFI setting of 7.68 µs (that is, 24 x 256 cycles x 1.25 ns period yields = 7.68 µs). The minimum value for this field is 6. If a value less than 6 is written to this field, this field is set to 6 by hardware. When the refresh interval counter expires, an internal pending refresh counter is incremented to count the number of pending refreshes. When refresh commands are issued during initial calibration, all pending refreshes are issued and the internal counter is decremented to zero. The internal pending refresh counter is a 4-bit counter with a maximum value of 15d. An error bit sets the PC_ERROR bit in the PC Error Status 0 Register if the internal pending refresh counter overflows.

Register Name	PC Initial Calibration Error Register
Mnemonic	IOM0.DDRPHY_PC_INIT_CAL_ERROR_P0
Address	8000C0180701103F (SCOM)
Description	This register provides error and status information associated with initial calibration. The errors reported in this register are maskable by the PC Initial Calibration Mask Register. The error bits in this register are set by hardware. When one or more of the error bits in this register are set and they are not masked: The pc_memctl_err_o output is asserted if in non-TDM mode or if this PC is on side A in TDM mode. The pc_memctl_err_ob output is asserted if this PC is on side B in TDM mode. Before writing this register to 0, the following registers, if set, must be written to 0: DDRPHY_PC_ERROR_STATUS0 DDRPHY_WC_ERROR_STATUS0 DDRPHY_RC_ERROR_STATUS0 DDRPHY_SEQ_ERROR_STATUS0 DDRPHY_APB_ERROR_STATUS0

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	RWX	ERROR_WR_LEVEL: A write-leveling error occurred during initial calibration.
49	RWX	ERROR_INITIAL_PAT_WRITE: An initial-pattern write error occurred during the initial calibration. This calibration step does not report errors. Therefore, this bit is always read as 0b.
50	RWX	ERROR_DQS_ALIGN: A DQS alignment error occurred during initial calibration.
51	RWX	ERROR_RDCLK_ALIGN: A RDCLK-to-SYSCLK alignment error occurred during initial calibration.
52	RWX	ERROR_READ_CTR: A read-centering error occurred during initial calibration.
53	RWX	ERROR_WRITE_CTR: A write-centering error occurred during initial calibration.
54	RWX	ERROR_INITIAL_COARSE_WR: An initial coarse pattern write error occurred during initial calibration. This calibration step does not report errors. Therefore, this bit is always read as 0b.
55	RWX	ERROR_COARSE_RD: A coarse read-centering error occurred during initial calibration.
56	RWX	ERROR_CUSTOM_RD: A custom pattern read-centering error occurred during initial calibration.
57	RWX	ERROR_CUSTOM_WR: A custom pattern write-centering error occurred during initial calibration.
58	RWX	ERROR_DIGITAL_EYE: A digital eye error occurred during initial calibration.
59	RWX	ERROR_VREF: A read or write VREF error occurred during initial calibration.

Bits	SCOM	Field Mnemonic: Description
60:63	RWX	ERROR_RANK_PAIR: This field indicates which rank pairs encountered an error during initial calibration. Bit 60 reflects the status of rank pair 0. Bit 61 reflects the status of rank pair 1. Bit 62 reflects the status of rank pair 2. Bit 63 reflects the status of rank pair 3.

Register Name	**PC Initial Calibration Error Register**
Mnemonic	IOM0.DDRPHY_PC_INIT_CAL_ERROR_P1
Address	8000C0180701143F (SCOM)
Description	This register provides error and status information associated with initial calibration. The errors reported in this register are maskable by the PC Initial Calibration Mask Register. The error bits in this register are set by hardware. When one or more of the error bits in this register are set and they are not masked: The pc_memctl_err_o output is asserted if in non-TDM mode or if this PC is on side A in TDM mode. The pc_memctl_err_ob output is asserted if this PC is on side B in TDM mode. Before writing this register to 0, the following registers, if set, must be written to 0: DDRPHY_PC_ERROR_STATUS0 DDRPHY_WC_ERROR_STATUS0 DDRPHY_RC_ERROR_STATUS0 DDRPHY_SEQ_ERROR_STATUS0 DDRPHY_APB_ERROR_STATUS0

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RWX	ERROR_WR_LEVEL: A write-leveling error occurred during initial calibration.
49	RWX	ERROR_INITIAL_PAT_WRITE: An initial-pattern write error occurred during the initial calibration. This calibration step does not report errors. Therefore, this bit is always read as 0b.
50	RWX	ERROR_DQS_ALIGN: A DQS alignment error occurred during initial calibration.
51	RWX	ERROR_RDCLK_ALIGN: A RDCLK-to-SYSCLK alignment error occurred during initial calibration.
52	RWX	ERROR_READ_CTR: A read-centering error occurred during initial calibration.
53	RWX	ERROR_WRITE_CTR: A write-centering error occurred during initial calibration.
54	RWX	ERROR_INITIAL_COARSE_WR: An initial coarse pattern write error occurred during initial calibration. This calibration step does not report errors. Therefore, this bit is always read as 0b.
55	RWX	ERROR_COARSE_RD: A coarse read-centering error occurred during initial calibration.
56	RWX	ERROR_CUSTOM_RD: A custom pattern read-centering error occurred during initial calibration.
57	RWX	ERROR_CUSTOM_WR: A custom pattern write-centering error occurred during initial calibration.
58	RWX	ERROR_DIGITAL_EYE: A digital eye error occurred during initial calibration.
59	RWX	ERROR_VREF: A read or write VREF error occurred during initial calibration.
60:63	RWX	ERROR_RANK_PAIR: This field indicates which rank pairs encountered an error during initial calibration. Bit 60 reflects the status of rank pair 0. Bit 61 reflects the status of rank pair 1. Bit 62 reflects the status of rank pair 2. Bit 63 reflects the status of rank pair 3.

Register Name	PC Initial Calibration Error Register
Mnemonic	IOM0.DDRPHY_PC_INIT_CAL_ERROR_P2
Address	8000C0180701183F (SCOM)
Description	This register provides error and status information associated with initial calibration. The errors reported in this register are maskable by the PC Initial Calibration Mask Register. The error bits in this register are set by hardware. When one or more of the error bits in this register are set and they are not masked: The pc_memctl_err_o output is asserted if in non-TDM mode or if this PC is on side A in TDM mode. The pc_memctl_err_ob output is asserted if this PC is on side B in TDM mode. Before writing this register to 0, the following registers, if set, must be written to 0: DDRPHY_PC_ERROR_STATUS0 DDRPHY_WC_ERROR_STATUS0 DDRPHY_RC_ERROR_STATUS0 DDRPHY_SEQ_ERROR_STATUS0 DDRPHY_APB_ERROR_STATUS0

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RWX	ERROR_WR_LEVEL: A write-leveling error occurred during initial calibration.
49	RWX	ERROR_INITIAL_PAT_WRITE: An initial-pattern write error occurred during the initial calibration. This calibration step does not report errors. Therefore, this bit is always read as 0b.
50	RWX	ERROR_DQS_ALIGN: A DQS alignment error occurred during initial calibration.
51	RWX	ERROR_RDCLK_ALIGN: A RDCLK-to-SYSCLK alignment error occurred during initial calibration.
52	RWX	ERROR_READ_CTR: A read-centering error occurred during initial calibration.
53	RWX	ERROR_WRITE_CTR: A write-centering error occurred during initial calibration.
54	RWX	ERROR_INITIAL_COARSE_WR: An initial coarse pattern write error occurred during initial calibration. This calibration step does not report errors. Therefore, this bit is always read as 0b.
55	RWX	ERROR_COARSE_RD: A coarse read-centering error occurred during initial calibration.
56	RWX	ERROR_CUSTOM_RD: A custom pattern read-centering error occurred during initial calibration.
57	RWX	ERROR_CUSTOM_WR: A custom pattern write-centering error occurred during initial calibration.
58	RWX	ERROR_DIGITAL_EYE: A digital eye error occurred during initial calibration.
59	RWX	ERROR_VREF: A read or write VREF error occurred during initial calibration.
60:63	RWX	ERROR_RANK_PAIR: This field indicates which rank pairs encountered an error during initial calibration. Bit 60 reflects the status of rank pair 0. Bit 61 reflects the status of rank pair 1. Bit 62 reflects the status of rank pair 2. Bit 63 reflects the status of rank pair 3.

Register Name	PC Initial Calibration Error Register
Mnemonic	IOM0.DDRPHY_PC_INIT_CAL_ERROR_P3
Address	8000C01807011C3F (SCOM)
Description	This register provides error and status information associated with initial calibration. The errors reported in this register are maskable by the PC Initial Calibration Mask Register. The error bits in this register are set by hardware. When one or more of the error bits in this register are set and they are not masked: The pc_memctl_err_o output is asserted if in non-TDM mode or if this PC is on side A in TDM mode. The pc_memctl_err_ob output is asserted if this PC is on side B in TDM mode. Before writing this register to 0, the following registers, if set, must be written to 0: DDRPHY_PC_ERROR_STATUS0 DDRPHY_WC_ERROR_STATUS0 DDRPHY_RC_ERROR_STATUS0 DDRPHY_SEQ_ERROR_STATUS0 DDRPHY_APB_ERROR_STATUS0

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RWX	ERROR_WR_LEVEL: A write-leveling error occurred during initial calibration.
49	RWX	ERROR_INITIAL_PAT_WRITE: An initial-pattern write error occurred during the initial calibration. This calibration step does not report errors. Therefore, this bit is always read as 0b.
50	RWX	ERROR_DQS_ALIGN: A DQS alignment error occurred during initial calibration.
51	RWX	ERROR_RDCLK_ALIGN: A RDCLK-to-SYSCLK alignment error occurred during initial calibration.
52	RWX	ERROR_READ_CTR: A read-centering error occurred during initial calibration.
53	RWX	ERROR_WRITE_CTR: A write-centering error occurred during initial calibration.
54	RWX	ERROR_INITIAL_COARSE_WR: An initial coarse pattern write error occurred during initial calibration. This calibration step does not report errors. Therefore, this bit is always read as 0b.
55	RWX	ERROR_COARSE_RD: A coarse read-centering error occurred during initial calibration.
56	RWX	ERROR_CUSTOM_RD: A custom pattern read-centering error occurred during initial calibration.
57	RWX	ERROR_CUSTOM_WR: A custom pattern write-centering error occurred during initial calibration.
58	RWX	ERROR_DIGITAL_EYE: A digital eye error occurred during initial calibration.
59	RWX	ERROR_VREF: A read or write VREF error occurred during initial calibration.
60:63	RWX	ERROR_RANK_PAIR: This field indicates which rank pairs encountered an error during initial calibration. Bit 60 reflects the status of rank pair 0. Bit 61 reflects the status of rank pair 1. Bit 62 reflects the status of rank pair 2. Bit 63 reflects the status of rank pair 3.

Register Name	PC Initial Calibration Status Register
Mnemonic	IOM0.DDRPHY_PC_INIT_CAL_STATUS_P0
Address	8000C0190701103F (SCOM)
Description	This register provides status information associated with initial calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RWX	INIT_CAL_COMPLETE: This field indicates which rank pairs have completed initial calibration. 1b indicates that the rank pair has completed an initial calibration sequence. Bit 48 reflects the status of rank pair 0. Bit 49 reflects the status of rank pair 1. Bit 50 reflects the status of rank pair 2. Bit 51 reflects the status of rank pair 3.
52:55	ROX	DFI_REQ_STATE: This field indicates the current state of the DFI request state machine, which controls the handshaking to control calibration. For debug use only.
56	RWX	PER_PEND_OVRFLW: 1 = Overflow of refresh pending counter. For debug used only. If this overflow causes an error, the error is captured in an error register.
57	RWX	PER_CAL_ABORT: Periodic calibration abort. This bit is set by hardware when the pc_errn_in transitions from high to low, a periodic calibration is in progress, and the ABORT_ON_ERR_EN bit is set in the PC Periodic Calibration Configuration Register. This bit is reset at the start of every new calibration. For debug use only.
58	ROX	Reserved.
59:63	ROX	ICAL_STATE: This field indicates the current state of the initial calibration state machine. For debug use only.

Register Name	PC Initial Calibration Status Register
Mnemonic	IOM0.DDRPHY_PC_INIT_CAL_STATUS_P1
Address	8000C0190701143F (SCOM)
Description	This register provides status information associated with initial calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:51	RWX	INIT_CAL_COMPLETE: This field indicates which rank pairs have completed initial calibration. 1b indicates that the rank pair has completed an initial calibration sequence. Bit 48 reflects the status of rank pair 0. Bit 49 reflects the status of rank pair 1. Bit 50 reflects the status of rank pair 2. Bit 51 reflects the status of rank pair 3.
52:55	ROX	DFI_REQ_STATE: This field indicates the current state of the DFI request state machine, which controls the handshaking to control calibration. For debug use only.
56	RWX	PER_PEND_OVRFLW: 1 = Overflow of refresh pending counter. For debug used only. If this overflow causes an error, the error is captured in an error register.
57	RWX	PER_CAL_ABORT: Periodic calibration abort. This bit is set by hardware when the pc_errn_in transitions from high to low, a periodic calibration is in progress, and the ABORT_ON_ERR_EN bit is set in the PC Periodic Calibration Configuration Register. This bit is reset at the start of every new calibration. For debug use only.
58	ROX	Reserved.
59:63	ROX	ICAL_STATE: This field indicates the current state of the initial calibration state machine. For debug use only.

Register Name	PC Initial Calibration Status Register
Mnemonic	IOM0.DDRPHY_PC_INIT_CAL_STATUS_P2
Address	8000C0190701183F (SCOM)
Description	This register provides status information associated with initial calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:51	RWX	INIT_CAL_COMPLETE: This field indicates which rank pairs have completed initial calibration. 1b indicates that the rank pair has completed an initial calibration sequence. Bit 48 reflects the status of rank pair 0. Bit 49 reflects the status of rank pair 1. Bit 50 reflects the status of rank pair 2. Bit 51 reflects the status of rank pair 3.
52:55	ROX	DFI_REQ_STATE: This field indicates the current state of the DFI request state machine, which controls the handshaking to control calibration. For debug use only.
56	RWX	PER_PEND_OVRFLW: 1 = Overflow of refresh pending counter. For debug used only. If this overflow causes an error, the error is captured in an error register.
57	RWX	PER_CAL_ABORT: Periodic calibration abort. This bit is set by hardware when the pc_errn_in transitions from high to low, a periodic calibration is in progress, and the ABORT_ON_ERR_EN bit is set in the PC Periodic Calibration Configuration Register. This bit is reset at the start of every new calibration. For debug use only.
58	ROX	Reserved.
59:63	ROX	ICAL_STATE: This field indicates the current state of the initial calibration state machine. For debug use only.

Register Name	PC Initial Calibration Status Register
Mnemonic	IOM0.DDRPHY_PC_INIT_CAL_STATUS_P3
Address	8000C01907011C3F (SCOM)
Description	This register provides status information associated with initial calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:51	RWX	INIT_CAL_COMPLETE: This field indicates which rank pairs have completed initial calibration. 1b indicates that the rank pair has completed an initial calibration sequence. Bit 48 reflects the status of rank pair 0. Bit 49 reflects the status of rank pair 1. Bit 50 reflects the status of rank pair 2. Bit 51 reflects the status of rank pair 3.
52:55	ROX	DFI_REQ_STATE: This field indicates the current state of the DFI request state machine, which controls the handshaking to control calibration. For debug use only.
56	RWX	PER_PEND_OVRFLW: 1 = Overflow of refresh pending counter. For debug used only. If this overflow causes an error, the error is captured in an error register.
57	RWX	PER_CAL_ABORT: Periodic calibration abort. This bit is set by hardware when the pc_errn_in transitions from high to low, a periodic calibration is in progress, and the ABORT_ON_ERR_EN bit is set in the PC Periodic Calibration Configuration Register. This bit is reset at the start of every new calibration. For debug use only.
58	ROX	Reserved.

Bits	SCOM	Field Mnemonic: Description
59:63	ROX	ICAL_STATE: This field indicates the current state of the initial calibration state machine. For debug use only.

Register Name	PC Initial Calibration Mask Register
Mnemonic	IOM0.DDRPHY_PC_INIT_CAL_MASK_P0
Address	8000C01A0701103F (SCOM)
Description	This register masks error bits in the PC Initial Calibration Error Register from asserting: The pc_memctl_err_o output if in non-TDM mode or if this PC is on side A in TDM mode. The pc_memctl_err_ob output if this PC is on side B in TDM mode.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	ERROR_WR_LEVEL_MASK: Mask write-leveling error.
49	RW	ERROR_INITIAL_PAT_WRITE_MASK: Mask initial-pattern write error.
50	RW	ERROR_DQS_ALIGN_MASK: Mask DQS alignment error.
51	RW	ERROR_RDCLK_ALIGN_MASK: Mask RDCLK-to-SYSCLK alignment error.
52	RW	ERROR_READ_CTR_MASK: Mask read-centering error.
53	RW	ERROR_WRITE_CTR_MASK: Mask write-centering error.
54	RW	ERROR_INITIAL_COARSE_WR_MASK: Mask initial coarse pattern write-centering error.
55	RW	ERROR_COARSE_RD_MASK: Mask coarse read-centering error.
56	RW	ERROR_CUSTOM_RD_MASK: Mask custom pattern read-centering error.
57	RW	ERROR_CUSTOM_WR_MASK: Mask custom pattern write-centering error.
58	RW	ERROR_DIGITAL_EYE_MASK: Mask digital eye error.
59	RW	ERROR_VREF_MASK: Mask read and write VREF error.
60:63	RO	Constant = 0b0000

Register Name	PC Initial Calibration Mask Register
Mnemonic	IOM0.DDRPHY_PC_INIT_CAL_MASK_P1
Address	8000C01A0701143F (SCOM)
Description	This register masks error bits in the PC Initial Calibration Error Register from asserting: The pc_memctl_err_o output if in non-TDM mode or if this PC is on side A in TDM mode The pc_memctl_err_ob output if this PC is on side B in TDM mode.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	ERROR_WR_LEVEL_MASK: Mask write-leveling error.
49	RW	ERROR_INITIAL_PAT_WRITE_MASK: Mask initial-pattern write error.
50	RW	ERROR_DQS_ALIGN_MASK: Mask DQS alignment error.
51	RW	ERROR_RDCLK_ALIGN_MASK: Mask RDCLK-to-SYSCLK alignment error.
52	RW	ERROR_READ_CTR_MASK: Mask read-centering error.
53	RW	ERROR_WRITE_CTR_MASK: Mask write-centering error.

Bits	SCOM	Field Mnemonic: Description
54	RW	ERROR_INITIAL_COARSE_WR_MASK: Mask initial coarse pattern write-centering error.
55	RW	ERROR_COARSE_RD_MASK: Mask coarse read-centering error.
56	RW	ERROR_CUSTOM_RD_MASK: Mask custom pattern read-centering error.
57	RW	ERROR_CUSTOM_WR_MASK: Mask custom pattern write-centering error.
58	RW	ERROR_DIGITAL_EYE_MASK: Mask digital eye error.
59	RW	ERROR_VREF_MASK: Mask read and write VREF error.
60:63	RO	Constant = 0b0000

Register Name	PC Initial Calibration Mask Register
Mnemonic	IOM0.DDRPHY_PC_INIT_CAL_MASK_P2
Address	8000C01A0701183F (SCOM)
Description	This register masks error bits in the PC Initial Calibration Error Register from asserting: The pc_memctl_err_o output if in non-TDM mode or if this PC is on side A in TDM mode The pc_memctl_err_ob output if this PC is on side B in TDM mode.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48	RW	ERROR_WR_LEVEL_MASK: Mask write-leveling error.
49	RW	ERROR_INITIAL_PAT_WRITE_MASK: Mask initial-pattern write error.
50	RW	ERROR_DQS_ALIGN_MASK: Mask DQS alignment error.
51	RW	ERROR_RDCLK_ALIGN_MASK: Mask RDCLK-to-SYSCLK alignment error.
52	RW	ERROR_READ_CTR_MASK: Mask read-centering error.
53	RW	ERROR_WRITE_CTR_MASK: Mask write-centering error.
54	RW	ERROR_INITIAL_COARSE_WR_MASK: Mask initial coarse pattern write-centering error.
55	RW	ERROR_COARSE_RD_MASK: Mask coarse read-centering error.
56	RW	ERROR_CUSTOM_RD_MASK: Mask custom pattern read-centering error.
57	RW	ERROR_CUSTOM_WR_MASK: Mask custom pattern write-centering error.
58	RW	ERROR_DIGITAL_EYE_MASK: Mask digital eye error.
59	RW	ERROR_VREF_MASK: Mask read and write VREF error.
60:63	RO	Constant = 0b0000

Register Name	PC Initial Calibration Mask Register
Mnemonic	IOM0.DDRPHY_PC_INIT_CAL_MASK_P3
Address	8000C01A07011C3F (SCOM)
Description	This register masks error bits in the PC Initial Calibration Error Register from asserting: The pc_memctl_err_o output if in non-TDM mode or if this PC is on side A in TDM mode The pc_memctl_err_ob output if this PC is on side B in TDM mode.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RW	ERROR_WR_LEVEL_MASK: Mask write-leveling error.
49	RW	ERROR_INITIAL_PAT_WRITE_MASK: Mask initial-pattern write error.
50	RW	ERROR_DQS_ALIGN_MASK: Mask DQS alignment error.
51	RW	ERROR_RDCLK_ALIGN_MASK: Mask RDCLK-to-SYSCLK alignment error.
52	RW	ERROR_READ_CTR_MASK: Mask read-centering error.
53	RW	ERROR_WRITE_CTR_MASK: Mask write-centering error.
54	RW	ERROR_INITIAL_COARSE_WR_MASK: Mask initial coarse pattern write-centering error.
55	RW	ERROR_COARSE_RD_MASK: Mask coarse read-centering error.
56	RW	ERROR_CUSTOM_RD_MASK: Mask custom pattern read-centering error.
57	RW	ERROR_CUSTOM_WR_MASK: Mask custom pattern write-centering error.
58	RW	ERROR_DIGITAL_EYE_MASK: Mask digital eye error.
59	RW	ERROR_VREF_MASK: Mask read and write VREF error.
60:63	RO	Constant = 0b0000

Register Name	**PC IO PVT N/P FET Driver Status Register**
Mnemonic	IOM0.DDRPHY_PC_IO_PVT_FET_STATUS_P0
Address	8000C01B0701103F (SCOM)
Description	This register reports the values coming into the DDR PHY core from the internal impedance controller core (external to the DDR PHY core). Reading this register is asynchronous to the value updates from the internal impedance controller. To ensure a valid read value, read this register multiple times until two consecutive reads return the same value.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	ROX	PVTPB: PFET binary driver PVTP value observed. This is the value calculated by the internal impedance calibration macro external to the DDR PHY.
49:55	ROX	PVTPL: PFET linear driver PVTP value observed. This is the value calculated by the internal impedance calibration macro external to the DDR PHY.
56	ROX	PVTNB: NFET binary driver PVTN value observed. This is the value calculated by the internal impedance calibration macro external to the DDR PHY.
57:63	ROX	PVTNL: NFET linear driver PVTN value observed. This is the value calculated by the internal impedance calibration macro external to the DDR PHY.

Register Name	**PC IO PVT N/P FET Driver Status Register**
Mnemonic	IOM0.DDRPHY_PC_IO_PVT_FET_STATUS_P1
Address	8000C01B0701143F (SCOM)
Description	This register reports the values coming into the DDR PHY core from the internal impedance controller core (external to the DDR PHY core). Reading this register is asynchronous to the value updates from the internal impedance controller. To ensure a valid read value, read this register multiple times until two consecutive reads return the same value.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	ROX	PVTPB: PFET binary driver PVTP value observed. This is the value calculated by the internal impedance calibration macro external to the DDR PHY.
49:55	ROX	PVTPL: PFET linear driver PVTP value observed. This is the value calculated by the internal impedance calibration macro external to the DDR PHY.
56	ROX	PVTNB: NFET binary driver PVTN value observed. This is the value calculated by the internal impedance calibration macro external to the DDR PHY.
57:63	ROX	PVTNL: NFET linear driver PVTN value observed. This is the value calculated by the internal impedance calibration macro external to the DDR PHY.

Register Name	**PC IO PVT N/P FET Driver Status Register**
Mnemonic	IOM0.DDRPHY_PC_IO_PVT_FET_STATUS_P2
Address	8000C01B0701183F (SCOM)
Description	This register reports the values coming into the DDR PHY core from the internal impedance controller core (external to the DDR PHY core). Reading this register is asynchronous to the value updates from the internal impedance controller. To ensure a valid read value, read this register multiple times until two consecutive reads return the same value.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	ROX	PVTPB: PFET binary driver PVTP value observed. This is the value calculated by the internal impedance calibration macro external to the DDR PHY.
49:55	ROX	PVTPL: PFET linear driver PVTP value observed. This is the value calculated by the internal impedance calibration macro external to the DDR PHY.
56	ROX	PVTNB: NFET binary driver PVTN value observed. This is the value calculated by the internal impedance calibration macro external to the DDR PHY.
57:63	ROX	PVTNL: NFET linear driver PVTN value observed. This is the value calculated by the internal impedance calibration macro external to the DDR PHY.

Register Name	**PC IO PVT N/P FET Driver Status Register**
Mnemonic	IOM0.DDRPHY_PC_IO_PVT_FET_STATUS_P3
Address	8000C01B07011C3F (SCOM)
Description	This register reports the values coming into the DDR PHY core from the internal impedance controller core (external to the DDR PHY core). Reading this register is asynchronous to the value updates from the internal impedance controller. To ensure a valid read value, read this register multiple times until two consecutive reads return the same value.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	ROX	PVTPB: PFET binary driver PVTP value observed. This is the value calculated by the internal impedance calibration macro external to the DDR PHY.
49:55	ROX	PVTPL: PFET linear driver PVTP value observed. This is the value calculated by the internal impedance calibration macro external to the DDR PHY.
56	ROX	PVTNB: NFET binary driver PVTN value observed. This is the value calculated by the internal impedance calibration macro external to the DDR PHY.

Bits	SCOM	Field Mnemonic: Description
57:63	ROX	PVTNL: NFET linear driver PVTN value observed. This is the value calculated by the internal impedance calibration macro external to the DDR PHY.

Register Name	PC Mode 0 RP0 Register
Mnemonic	IOM0.DDRPHY_PC_MR0_RP0_P0
Address	8000C01C0701103F (SCOM)
Description	The value in this register reflects Mode Register 0 (MR0) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value that is intended for MR0 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Register registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_0_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 0 RP0 Register
Mnemonic	IOM0.DDRPHY_PC_MR0_RP0_P1
Address	8000C01C0701143F (SCOM)
Description	The value in this register reflects Mode Register 0 (MR0) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value that is intended for MR0 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_0_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 0 RP0 Register
Mnemonic	IOM0.DDRPHY_PC_MR0_RP0_P2
Address	8000C01C0701183F (SCOM)
Description	The value in this register reflects Mode Register 0 (MR0) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value that is intended for MR0 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_0_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 0 RP0 Register
Mnemonic	IOM0.DDRPHY_PC_MR0_RP0_P3
Address	8000C01C07011C3F (SCOM)
Description	The value in this register reflects Mode Register 0 (MR0) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value that is intended for MR0 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_0_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 1 RP0 Register
Mnemonic	IOM0.DDRPHY_PC_MR1_RP0_P0
Address	8000C01D0701103F (SCOM)
Description	The value in this register reflects Mode Register 1 (MR1) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR1 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_1_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	**PC Mode 1 RP0 Register**
Mnemonic	IOM0.DDRPHY_PC_MR1_RP0_P1
Address	8000C01D0701143F (SCOM)
Description	The value in this register reflects Mode Register 1 (MR1) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR1 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_1_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	**PC Mode 1 RP0 Register**
Mnemonic	IOM0.DDRPHY_PC_MR1_RP0_P2
Address	8000C01D0701183F (SCOM)
Description	The value in this register reflects Mode Register 1 (MR1) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR1 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_1_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 1 RP0 Register
Mnemonic	IOM0.DDRPHY_PC_MR1_RP0_P3
Address	8000C01D07011C3F (SCOM)
Description	The value in this register reflects Mode Register 1 (MR1) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR1 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_1_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 2 RP0 Register
Mnemonic	IOM0.DDRPHY_PC_MR2_RP0_P0
Address	8000C01E0701103F (SCOM)
Description	The value in this register reflects Mode Register 2 (MR2) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR2 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY core snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_2_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 2 RP0 Register
Mnemonic	IOM0.DDRPHY_PC_MR2_RP0_P1
Address	8000C01E0701143F (SCOM)
Description	The value in this register reflects Mode Register 2 (MR2) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR2 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY core snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_2_VALUE:

Register Name	PC Mode 2 RP0 Register
Mnemonic	IOM0.DDRPHY_PC_MR2_RP0_P2
Address	8000C01E0701183F (SCOM)
Description	The value in this register reflects Mode Register 2 (MR2) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR2 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY core snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_2_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 2 RP0 Register
Mnemonic	IOM0.DDRPHY_PC_MR2_RP0_P3
Address	8000C01E07011C3F (SCOM)
Description	The value in this register reflects Mode Register 2 (MR2) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR2 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY core snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_2_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 3 RP0 Register
Mnemonic	IOM0.DDRPHY_PC_MR3_RP0_P0
Address	8000C01F0701103F (SCOM)
Description	The value in this register reflects Mode Register 3 (MR3) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_3_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 3 RP0 Register
Mnemonic	IOM0.DDRPHY_PC_MR3_RP0_P1
Address	8000C01F0701143F (SCOM)
Description	The value in this register reflects Mode Register 3 (MR3) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_3_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 3 RP0 Register
Mnemonic	IOM0.DDRPHY_PC_MR3_RP0_P2
Address	8000C01F0701183F (SCOM)
Description	The value in this register reflects Mode Register 3 (MR3) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Registerprogramming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_3_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	**PC Mode 3 RP0 Register**
Mnemonic	IOM0.DDRPHY_PC_MR3_RP0_P3
Address	8000C01F07011C3F (SCOM)
Description	The value in this register reflects Mode Register 3 (MR3) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_3_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	**PC Mode 4 RP0 Register**
Mnemonic	IOM0.DDRPHY_PC_MR4_RP0_P0
Address	8000C0200701103F (SCOM)
Description	The value in this register reflects Mode Register 4 (MR4) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_4_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 4 RP0 Register
Mnemonic	IOM0.DDRPHY_PC_MR4_RP0_P1
Address	8000C0200701143F (SCOM)
Description	The value in this register reflects Mode Register 4 (MR4) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_4_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 4 RP0 Register
Mnemonic	IOM0.DDRPHY_PC_MR4_RP0_P2
Address	8000C0200701183F (SCOM)
Description	The value in this register reflects Mode Register 4 (MR4) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_4_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 4 RP0 Register
Mnemonic	IOM0.DDRPHY_PC_MR4_RP0_P3
Address	8000C02007011C3F (SCOM)
Description	The value in this register reflects Mode Register 4 (MR4) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_4_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	**PC Mode 5 RP0 Register**
Mnemonic	IOM0.DDRPHY_PC_MR5_RP0_P0
Address	8000C0210701103F (SCOM)
Description	The value in this register reflects Mode Register 5 (MR5) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_5_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	**PC Mode 5 RP0 Register**
Mnemonic	IOM0.DDRPHY_PC_MR5_RP0_P1
Address	8000C0210701143F (SCOM)
Description	The value in this register reflects Mode Register 5 (MR5) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_5_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 5 RP0 Register
Mnemonic	IOM0.DDRPHY_PC_MR5_RP0_P2
Address	8000C0210701183F (SCOM)
Description	The value in this register reflects Mode Register 5 (MR5) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_5_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 5 RP0 Register
Mnemonic	IOM0.DDRPHY_PC_MR5_RP0_P3
Address	8000C02107011C3F (SCOM)
Description	The value in this register reflects Mode Register 5 (MR5) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_5_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 6 RP0 Register
Mnemonic	IOM0.DDRPHY_PC_MR6_RP0_P0
Address	8000C0220701103F (SCOM)
Description	The value in this register reflects Mode Register 6 (MR6) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_6_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	**PC Mode 6 RP0 Register**
Mnemonic	IOM0.DDRPHY_PC_MR6_RP0_P1
Address	8000C0220701143F (SCOM)
Description	The value in this register reflects Mode Register 6 (MR6) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_6_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	**PC Mode 6 RP0 Register**
Mnemonic	IOM0.DDRPHY_PC_MR6_RP0_P2
Address	8000C0220701183F (SCOM)
Description	The value in this register reflects Mode Register 6 (MR6) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_6_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 6 RP0 Register
Mnemonic	IOM0.DDRPHY_PC_MR6_RP0_P3
Address	8000C02207011C3F (SCOM)
Description	The value in this register reflects Mode Register 6 (MR6) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_6_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 7 RP0 Register
Mnemonic	IOM0.DDRPHY_PC_MR7_RP0_P0
Address	8000C0230701103F (SCOM)
Description	This register is provided solely for debugging firmware. It reflects the value that was snooped on the last mode register set (MRS) command sent to the DRAM. The PHY uses only the information contained in the PC Mode X Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_7_VALUE: Reserved.

Register Name	PC Mode 7 RP0 Register
Mnemonic	IOM0.DDRPHY_PC_MR7_RP0_P1
Address	8000C0230701143F (SCOM)
Description	This register is provided solely for debugging firmware. It reflects the value that was snooped on the last mode register set (MRS) command sent to the DRAM. The PHY uses only the information contained in the PC Mode X Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_7_VALUE: Reserved.

Register Name	PC Mode 7 RP0 Register
Mnemonic	IOM0.DDRPHY_PC_MR7_RP0_P2
Address	8000C0230701183F (SCOM)
Description	This register is provided solely for debugging firmware. It reflects the value that was snooped on the last mode register set (MRS) command sent to the DRAM. The PHY uses only the information contained in the PC Mode X Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_7_VALUE: Reserved.

Register Name	PC Mode 7 RP0 Register
Mnemonic	IOM0.DDRPHY_PC_MR7_RP0_P3
Address	8000C02307011C3F (SCOM)
Description	This register is provided solely for debugging firmware. It reflects the value that was snooped on the last mode register set (MRS) command sent to the DRAM. The PHY uses only the information contained in the PC Mode X Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_7_VALUE: Reserved.

Register Name	PC Rank Pair 2 Register
Mnemonic	IOM0.DDRPHY_PC_RANK_PAIR2_P0
Address	8000C0300701103F (SCOM)
Description	These four registers assign rank numbers to the rank groups. The DDR PHY supports up to four ranks. Ranks in a rank group must have the same system timing and delay characteristics. The DDR PHY core calibrates the primary rank in the rank group, and uses the delay settings when any rank in the rank group is accessed. In the DDR PHY core, all parameters that are rank dependent are stored in one of four rank group (or rank pair) register sets. By configuring these registers, one to four ranks can be assigned to a rank group. When a rank is accessed, the parameter values used are determined by the configuration of this rank pair association register. Assigning one rank to multiple rank groups causes indeterminate behavior of the DDR PHY core.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	RANK_PAIR0_TER: Tertiary rank of rank pair 0. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
51	RW	RANK_PAIR0_TER_V: The value in the RANK_PAIR0_TER field is valid. If this bit is set, the RANK_PAIR0_SEC_V bit must be set in the PC Rank Pair 0 Register.
52:54	RW	RANK_PAIR0_QUA: Quaternary rank of rank pair 0. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
55	RW	RANK_PAIR0_QUA_V: The value in the RANK_PAIR0_QUA field is valid. If this bit is set, the RANK_PAIR0_TER_V bit must be set.
56:58	RW	RANK_PAIR1_TER: Tertiary rank of rank pair 1. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).

Bits	SCOM	Field Mnemonic: Description
59	RW	RANK_PAIR1_TER_V: The value in the RANK_PAIR1_TER field is valid. If this bit is set, the RANK_PAIR1_SEC_V bit must be set in the PC Rank Pair 0 Register.
60:62	RW	RANK_PAIR1_QUA: Quaternary rank of rank pair 1. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
63	RW	RANK_PAIR1_QUA_V: The value in the RANK_PAIR1_QUA field is valid. If this bit is set, the RANK_PAIR1_TER_V bit must be set.

Register Name	PC Rank Pair 2 Register
Mnemonic	IOM0.DDRPHY_PC_RANK_PAIR2_P1
Address	8000C0300701143F (SCOM)
Description	These four registers assign rank numbers to the rank groups. The DDR PHY supports up to four ranks. Ranks in a rank group must have the same system timing and delay characteristics. The DDR PHY core calibrates the primary rank in the rank group, and uses the delay settings when any rank in the rank group is accessed. In the DDR PHY core, all parameters that are rank dependent are stored in one of four rank group (or rank pair) register sets. By configuring these registers, one to four ranks can be assigned to a rank group. When a rank is accessed, the parameter values used are determined by the configuration of this rank pair association register. Assigning one rank to multiple rank groups causes indeterminate behavior of the DDR PHY core.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	RANK_PAIR0_TER: Tertiary rank of rank pair 0. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
51	RW	RANK_PAIR0_TER_V: The value in the RANK_PAIR0_TER field is valid. If this bit is set, the RANK_PAIR0_SEC_V bit must be set in the PC Rank Pair 0 Register.
52:54	RW	RANK_PAIR0_QUA: Quaternary rank of rank pair 0. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
55	RW	RANK_PAIR0_QUA_V: The value in the RANK_PAIR0_QUA field is valid. If this bit is set, the RANK_PAIR0_TER_V bit must be set.
56:58	RW	RANK_PAIR1_TER: Tertiary rank of rank pair 1. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
59	RW	RANK_PAIR1_TER_V: The value in the RANK_PAIR1_TER field is valid. If this bit is set, the RANK_PAIR1_SEC_V bit must be set in the PC Rank Pair 0 Register.
60:62	RW	RANK_PAIR1_QUA: Quaternary rank of rank pair 1. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
63	RW	RANK_PAIR1_QUA_V: The value in the RANK_PAIR1_QUA field is valid. If this bit is set, the RANK_PAIR1_TER_V bit must be set.

Register Name	PC Rank Pair 2 Register
Mnemonic	IOM0.DDRPHY_PC_RANK_PAIR2_P2
Address	8000C0300701183F (SCOM)
Description	These four registers assign rank numbers to the rank groups. The DDR PHY supports up to four ranks. Ranks in a rank group must have the same system timing and delay characteristics. The DDR PHY core calibrates the primary rank in the rank group, and uses the delay settings when any rank in the rank group is accessed. In the DDR PHY core, all parameters that are rank dependent are stored in one of four rank group (or rank pair) register sets. By configuring these registers, one to four ranks can be assigned to a rank group. When a rank is accessed, the parameter values used are determined by the configuration of this rank pair association register. Assigning one rank to multiple rank groups causes indeterminate behavior of the DDR PHY core.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	RANK_PAIR0_TER: Tertiary rank of rank pair 0. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
51	RW	RANK_PAIR0_TER_V: The value in the RANK_PAIR0_TER field is valid. If this bit is set, the RANK_PAIR0_SEC_V bit must be set in the PC Rank Pair 0 Register.
52:54	RW	RANK_PAIR0_QUA: Quaternary rank of rank pair 0. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
55	RW	RANK_PAIR0_QUA_V: The value in the RANK_PAIR0_QUA field is valid. If this bit is set, the RANK_PAIR0_TER_V bit must be set.
56:58	RW	RANK_PAIR1_TER: Tertiary rank of rank pair 1. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
59	RW	RANK_PAIR1_TER_V: The value in the RANK_PAIR1_TER field is valid. If this bit is set, the RANK_PAIR1_SEC_V bit must be set in the PC Rank Pair 0 Register.
60:62	RW	RANK_PAIR1_QUA: Quaternary rank of rank pair 1. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
63	RW	RANK_PAIR1_QUA_V: The value in the RANK_PAIR1_QUA field is valid. If this bit is set, the RANK_PAIR1_TER_V bit must be set.

Register Name	PC Rank Pair 2 Register
Mnemonic	IOM0.DDRPHY_PC_RANK_PAIR2_P3
Address	8000C03007011C3F (SCOM)
Description	These four registers assign rank numbers to the rank groups. The DDR PHY supports up to four ranks. Ranks in a rank group must have the same system timing and delay characteristics. The DDR PHY core calibrates the primary rank in the rank group, and uses the delay settings when any rank in the rank group is accessed. In the DDR PHY core, all parameters that are rank dependent are stored in one of four rank group (or rank pair) register sets. By configuring these registers, one to four ranks can be assigned to a rank group. When a rank is accessed, the parameter values used are determined by the configuration of this rank pair association register. Assigning one rank to multiple rank groups causes indeterminate behavior of the DDR PHY core.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	RANK_PAIR0_TER: Tertiary rank of rank pair 0. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
51	RW	RANK_PAIR0_TER_V: The value in the RANK_PAIR0_TER field is valid. If this bit is set, the RANK_PAIR0_SEC_V bit must be set in the PC Rank Pair 0 Register.

Bits	SCOM	Field Mnemonic: Description
52:54	RW	RANK_PAIR0_QUA: Quaternary rank of rank pair 0. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
55	RW	RANK_PAIR0_QUA_V: The value in the RANK_PAIR0_QUA field is valid. If this bit is set, the RANK_PAIR0_TER_V bit must be set.
56:58	RW	RANK_PAIR1_TER: Tertiary rank of rank pair 1. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
59	RW	RANK_PAIR1_TER_V: The value in the RANK_PAIR1_TER field is valid. If this bit is set, the RANK_PAIR1_SEC_V bit must be set in the PC Rank Pair 0 Register.
60:62	RW	RANK_PAIR1_QUA: Quaternary rank of rank pair 1. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
63	RW	RANK_PAIR1_QUA_V: The value in the RANK_PAIR1_QUA field is valid. If this bit is set, the RANK_PAIR1_TER_V bit must be set.

Register Name	**PC Rank Pair 3 Register**
Mnemonic	IOM0.DDRPHY_PC_RANK_PAIR3_P0
Address	8000C0310701103F (SCOM)
Description	These four registers assign rank numbers to the rank groups. The DDR PHY supports up to four ranks. Ranks in a rank group must have the same system timing and delay characteristics. The DDR PHY core calibrates the primary rank in the rank group, and uses the delay settings when any rank in the rank group is accessed. In the DDR PHY core, all parameters that are rank dependent are stored in one of four rank group (or rank pair) register sets. By configuring these registers, one to four ranks can be assigned to a rank group. When a rank is accessed, the parameter values used are determined by the configuration of this rank pair association register. Assigning one rank to multiple rank groups causes indeterminate behavior of the DDR PHY core.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	RANK_PAIR2_TER: Tertiary rank of rank pair 2. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
51	RW	RANK_PAIR2_TER_V: The value in the RANK_PAIR2_TER field is valid. If this bit is set, the RANK_PAIR2_SEC_V bit must be set in the PC Rank Pair 1 Register.
52:54	RW	RANK_PAIR2_QUA: Quaternary rank of rank pair 2. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
55	RW	RANK_PAIR2_QUA_V: The value in the RANK_PAIR2_QUA field is valid. If this bit is set, the RANK_PAIR0_TER_V bit must be set.
56:58	RW	RANK_PAIR3_TER: Tertiary rank of rank pair 3. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
59	RW	RANK_PAIR3_TER_V: The value in the RANK_PAIR3_TER field is valid. If this bit is set, the RANK_PAIR3_SEC_V bit must be set in the PC Rank Pair 1 Register.
60:62	RW	RANK_PAIR3_QUA: Quaternary rank of rank pair 3. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
63	RW	RANK_PAIR3_QUA_V: The value in the RANK_PAIR3_QUA field is valid. If this bit is set, the RANK_PAIR3_TER_V bit must be set.

Register Name	PC Rank Pair 3 Register
Mnemonic	IOM0.DDRPHY_PC_RANK_PAIR3_P1
Address	8000C0310701143F (SCOM)
Description	These four registers assign rank numbers to the rank groups. The DDR PHY supports up to four ranks. Ranks in a rank group must have the same system timing and delay characteristics. The DDR PHY core calibrates the primary rank in the rank group, and uses the delay settings when any rank in the rank group is accessed. In the DDR PHY core, all parameters that are rank dependent are stored in one of four rank group (or rank pair) register sets. By configuring these registers, one to four ranks can be assigned to a rank group. When a rank is accessed, the parameter values used are determined by the configuration of this rank pair association register. Assigning one rank to multiple rank groups causes indeterminate behavior of the DDR PHY core.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	RANK_PAIR2_TER: Tertiary rank of rank pair 2. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
51	RW	RANK_PAIR2_TER_V: The value in the RANK_PAIR2_TER field is valid. If this bit is set, the RANK_PAIR2_SEC_V bit must be set in the PC Rank Pair 1 Register.
52:54	RW	RANK_PAIR2_QUA: Quaternary rank of rank pair 2. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
55	RW	RANK_PAIR2_QUA_V: The value in the RANK_PAIR2_QUA field is valid. If this bit is set, the RANK_PAIR0_TER_V bit must be set.
56:58	RW	RANK_PAIR3_TER: Tertiary rank of rank pair 3. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
59	RW	RANK_PAIR3_TER_V: The value in the RANK_PAIR3_TER field is valid. If this bit is set, the RANK_PAIR3_SEC_V bit must be set in the PC Rank Pair 1 Register.
60:62	RW	RANK_PAIR3_QUA: Quaternary rank of rank pair 3. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
63	RW	RANK_PAIR3_QUA_V: The value in the RANK_PAIR3_QUA field is valid. If this bit is set, the RANK_PAIR3_TER_V bit must be set.

Register Name	PC Rank Pair 3 Register
Mnemonic	IOM0.DDRPHY_PC_RANK_PAIR3_P2
Address	8000C0310701183F (SCOM)
Description	These four registers assign rank numbers to the rank groups. The DDR PHY supports up to four ranks. Ranks in a rank group must have the same system timing and delay characteristics. The DDR PHY core calibrates the primary rank in the rank group, and uses the delay settings when any rank in the rank group is accessed. In the DDR PHY core, all parameters that are rank dependent are stored in one of four rank group (or rank pair) register sets. By configuring these registers, one to four ranks can be assigned to a rank group. When a rank is accessed, the parameter values used are determined by the configuration of this rank pair association register. Assigning one rank to multiple rank groups causes indeterminate behavior of the DDR PHY core.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	RANK_PAIR2_TER: Tertiary rank of rank pair 2. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
51	RW	RANK_PAIR2_TER_V: The value in the RANK_PAIR2_TER field is valid. If this bit is set, the RANK_PAIR2_SEC_V bit must be set in the PC Rank Pair 1 Register.

Bits	SCOM	Field Mnemonic: Description
52:54	RW	RANK_PAIR2_QUA: Quaternary rank of rank pair 2. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
55	RW	RANK_PAIR2_QUA_V: The value in the RANK_PAIR2_QUA field is valid. If this bit is set, the RANK_PAIR0_TER_V bit must be set.
56:58	RW	RANK_PAIR3_TER: Tertiary rank of rank pair 3. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
59	RW	RANK_PAIR3_TER_V: The value in the RANK_PAIR3_TER field is valid. If this bit is set, the RANK_PAIR3_SEC_V bit must be set in the PC Rank Pair 1 Register.
60:62	RW	RANK_PAIR3_QUA: Quaternary rank of rank pair 3. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
63	RW	RANK_PAIR3_QUA_V: The value in the RANK_PAIR3_QUA field is valid. If this bit is set, the RANK_PAIR3_TER_V bit must be set.

Register Name	**PC Rank Pair 3 Register**
Mnemonic	IOM0.DDRPHY_PC_RANK_PAIR3_P3
Address	8000C03107011C3F (SCOM)
Description	These four registers assign rank numbers to the rank groups. The DDR PHY supports up to four ranks. Ranks in a rank group must have the same system timing and delay characteristics. The DDR PHY core calibrates the primary rank in the rank group, and uses the delay settings when any rank in the rank group is accessed. In the DDR PHY core, all parameters that are rank dependent are stored in one of four rank group (or rank pair) register sets. By configuring these registers, one to four ranks can be assigned to a rank group. When a rank is accessed, the parameter values used are determined by the configuration of this rank pair association register. Assigning one rank to multiple rank groups causes indeterminate behavior of the DDR PHY core.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	RANK_PAIR2_TER: Tertiary rank of rank pair 2. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
51	RW	RANK_PAIR2_TER_V: The value in the RANK_PAIR2_TER field is valid. If this bit is set, the RANK_PAIR2_SEC_V bit must be set in the PC Rank Pair 1 Register.
52:54	RW	RANK_PAIR2_QUA: Quaternary rank of rank pair 2. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
55	RW	RANK_PAIR2_QUA_V: The value in the RANK_PAIR2_QUA field is valid. If this bit is set, the RANK_PAIR0_TER_V bit must be set.
56:58	RW	RANK_PAIR3_TER: Tertiary rank of rank pair 3. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
59	RW	RANK_PAIR3_TER_V: The value in the RANK_PAIR3_TER field is valid. If this bit is set, the RANK_PAIR3_SEC_V bit must be set in the PC Rank Pair 1 Register.
60:62	RW	RANK_PAIR3_QUA: Quaternary rank of rank pair 3. Valid ranks are rank 0 (0b000), rank 1 (0b001), rank 2 (0b010), and rank 3 (0b011).
63	RW	RANK_PAIR3_QUA_V: The value in the RANK_PAIR3_QUA field is valid. If this bit is set, the RANK_PAIR3_TER_V bit must be set.

Register Name	PC Chip Select ID Configuration Register
Mnemonic	IOM0.DDRPHY_PC_CSID_CFG_P0
Address	8000C0330701103F (SCOM)
Description	This register controls the value of chip select (CS) signals not selected by any of the PC Rank Pair Registers during initial calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	CS0_INIT_CAL_VALUE: If CS0 is not selected by any of the Rank Pair Registers, CS0 is driven to this value during initial calibration. If CS0 is a chip select ID (CSID) bit, set this value to select the rank to be calibrated. Otherwise this bit is a "don't care".
49	RW	CS1_INIT_CAL_VALUE: If CS1 is not selected by any of the Rank Pair Registers, CS1 is driven to this value during initial calibration. If CS1 is a CSID bit, set this value to select the rank to be calibrated. Otherwise this bit is a "don't care".
50	RW	CS2_INIT_CAL_VALUE: If CS2 is not selected by any of the Rank Pair Registers, CS2 is driven to this value during initial calibration. If CS2 is a CSID bit, set this value to select the rank to be calibrated. Otherwise this bit is a "don't care".
51	RW	CS3_INIT_CAL_VALUE: If CS3 is not selected by any of the Rank Pair Registers, CS3 is driven to this value during initial calibration. If CS3 is a CSID bit, set this value to select the rank to be calibrated. Otherwise this bit is a "don't care".
52:63	RO	Reserved.

Register Name	PC Chip Select ID Configuration Register
Mnemonic	IOM0.DDRPHY_PC_CSID_CFG_P1
Address	8000C0330701143F (SCOM)
Description	This register controls the value of chip select (CS) signals not selected by any of the PC Rank Pair Registers during initial calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	CS0_INIT_CAL_VALUE: If CS0 is not selected by any of the Rank Pair Registers, CS0 is driven to this value during initial calibration. If CS0 is a CSID bit, set this value to select the rank to be calibrated. Otherwise this bit is a "don't care".
49	RW	CS1_INIT_CAL_VALUE: If CS1 is not selected by any of the Rank Pair Registers, CS1 is driven to this value during initial calibration. If CS1 is a CSID bit, set this value to select the rank to be calibrated. Otherwise this bit is a "don't care".
50	RW	CS2_INIT_CAL_VALUE: If CS2 is not selected by any of the Rank Pair Registers, CS2 is driven to this value during initial calibration. If CS2 is a CSID bit, set this value to select the rank to be calibrated. Otherwise this bit is a "don't care".
51	RW	CS3_INIT_CAL_VALUE: If CS3 is not selected by any of the Rank Pair Registers, CS3 is driven to this value during initial calibration. If CS3 is a CSID bit, set this value to select the rank to be calibrated. Otherwise this bit is a "don't care".
52:63	RO	Reserved.

Register Name	PC Chip Select ID Configuration Register
Mnemonic	IOM0.DDRPHY_PC_CSID_CFG_P2
Address	8000C0330701183F (SCOM)
Description	This register controls the value of chip select (CS) signals not selected by any of the PC Rank Pair Registers during initial calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	CS0_INIT_CAL_VALUE: If CS0 is not selected by any of the Rank Pair Registers, CS0 is driven to this value during initial calibration. If CS0 is a CSID bit, set this value to select the rank to be calibrated. Otherwise this bit is a "don't care".
49	RW	CS1_INIT_CAL_VALUE: If CS1 is not selected by any of the Rank Pair Registers, CS1 is driven to this value during initial calibration. If CS1 is a CSID bit, set this value to select the rank to be calibrated. Otherwise this bit is a "don't care".
50	RW	CS2_INIT_CAL_VALUE: If CS2 is not selected by any of the Rank Pair Registers, CS2 is driven to this value during initial calibration. If CS2 is a CSID bit, set this value to select the rank to be calibrated. Otherwise this bit is a "don't care".
51	RW	CS3_INIT_CAL_VALUE: If CS3 is not selected by any of the Rank Pair Registers, CS3 is driven to this value during initial calibration. If CS3 is a CSID bit, set this value to select the rank to be calibrated. Otherwise this bit is a "don't care".
52:63	RO	Reserved.

Register Name	PC Chip Select ID Configuration Register
Mnemonic	IOM0.DDRPHY_PC_CSID_CFG_P3
Address	8000C03307011C3F (SCOM)
Description	This register controls the value of chip select (CS) signals not selected by any of the PC Rank Pair Registers during initial calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	CS0_INIT_CAL_VALUE: If CS0 is not selected by any of the Rank Pair Registers, CS0 is driven to this value during initial calibration. If CS0 is a CSID bit, set this value to select the rank to be calibrated. Otherwise this bit is a "don't care".
49	RW	CS1_INIT_CAL_VALUE: If CS1 is not selected by any of the Rank Pair Registers, CS1 is driven to this value during initial calibration. If CS1 is a CSID bit, set this value to select the rank to be calibrated. Otherwise this bit is a "don't care".
50	RW	CS2_INIT_CAL_VALUE: If CS2 is not selected by any of the Rank Pair Registers, CS2 is driven to this value during initial calibration. If CS2 is a CSID bit, set this value to select the rank to be calibrated. Otherwise this bit is a "don't care".
51	RW	CS3_INIT_CAL_VALUE: If CS3 is not selected by any of the Rank Pair Registers, CS3 is driven to this value during initial calibration. If CS3 is a CSID bit, set this value to select the rank to be calibrated. Otherwise this bit is a "don't care".
52:63	RO	Reserved.

Register Name	PC Rank Group Extension Register
Mnemonic	IOM0.DDRPHY_PC_RANK_GROUP_EXT_P0
Address	8000C0350701103F (SCOM)
Description	This register provides control of the rank groups.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	ADDR_MIRROR_RP0_TER: 1 = Enable address mirroring of rank pair 0 tertiary.
49	RW	ADDR_MIRROR_RP0_QUA: 1 = Enable address mirroring of rank pair 0 quaternary.
50	RW	ADDR_MIRROR_RP1_TER: 1 = Enable address mirroring of rank pair 1 tertiary.
51	RW	ADDR_MIRROR_RP1_QUA: 1 = Enable address mirroring of rank pair 1 quaternary.
52	RW	ADDR_MIRROR_RP2_TER: 1 = Enable address mirroring of rank pair 2 tertiary.
53	RW	ADDR_MIRROR_RP2_QUA: 1 = Enable address mirroring of rank pair 2 quaternary.
54	RW	ADDR_MIRROR_RP3_TER: 1 = Enable address mirroring of rank pair 3 tertiary.
55	RW	ADDR_MIRROR_RP3_QUA: 1 = Enable address mirroring of rank pair 3 quaternary.
56:63	RO	Constant = 0b00000000

Register Name	PC Rank Group Extension Register
Mnemonic	IOM0.DDRPHY_PC_RANK_GROUP_EXT_P1
Address	8000C0350701143F (SCOM)
Description	This register provides control of the rank groups.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	ADDR_MIRROR_RP0_TER: 1 = Enable address mirroring of rank pair 0 tertiary.
49	RW	ADDR_MIRROR_RP0_QUA: 1 = Enable address mirroring of rank pair 0 quaternary.
50	RW	ADDR_MIRROR_RP1_TER: 1 = Enable address mirroring of rank pair 1 tertiary.
51	RW	ADDR_MIRROR_RP1_QUA: 1 = Enable address mirroring of rank pair 1 quaternary.
52	RW	ADDR_MIRROR_RP2_TER: 1 = Enable address mirroring of rank pair 2 tertiary.
53	RW	ADDR_MIRROR_RP2_QUA: 1 = Enable address mirroring of rank pair 2 quaternary.
54	RW	ADDR_MIRROR_RP3_TER: 1 = Enable address mirroring of rank pair 3 tertiary.
55	RW	ADDR_MIRROR_RP3_QUA: 1 = Enable address mirroring of rank pair 3 quaternary.
56:63	RO	Constant = 0b00000000

Register Name	PC Rank Group Extension Register
Mnemonic	IOM0.DDRPHY_PC_RANK_GROUP_EXT_P2
Address	8000C0350701183F (SCOM)
Description	This register provides control of the rank groups.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	ADDR_MIRROR_RP0_TER: 1 = Enable address mirroring of rank pair 0 tertiary.
49	RW	ADDR_MIRROR_RP0_QUA: 1 = Enable address mirroring of rank pair 0 quaternary.
50	RW	ADDR_MIRROR_RP1_TER: 1 = Enable address mirroring of rank pair 1 tertiary.
51	RW	ADDR_MIRROR_RP1_QUA: 1 = Enable address mirroring of rank pair 1 quaternary.
52	RW	ADDR_MIRROR_RP2_TER: 1 = Enable address mirroring of rank pair 2 tertiary.
53	RW	ADDR_MIRROR_RP2_QUA: 1 = Enable address mirroring of rank pair 2 quaternary.
54	RW	ADDR_MIRROR_RP3_TER: 1 = Enable address mirroring of rank pair 3 tertiary.
55	RW	ADDR_MIRROR_RP3_QUA: 1 = Enable address mirroring of rank pair 3 quaternary.
56:63	RO	Constant = 0b00000000

Register Name	**PC Rank Group Extension Register**
Mnemonic	IOM0.DDRPHY_PC_RANK_GROUP_EXT_P3
Address	8000C03507011C3F (SCOM)
Description	This register provides control of the rank groups.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	ADDR_MIRROR_RP0_TER: 1 = Enable address mirroring of rank pair 0 tertiary.
49	RW	ADDR_MIRROR_RP0_QUA: 1 = Enable address mirroring of rank pair 0 quaternary.
50	RW	ADDR_MIRROR_RP1_TER: 1 = Enable address mirroring of rank pair 1 tertiary.
51	RW	ADDR_MIRROR_RP1_QUA: 1 = Enable address mirroring of rank pair 1 quaternary.
52	RW	ADDR_MIRROR_RP2_TER: 1 = Enable address mirroring of rank pair 2 tertiary.
53	RW	ADDR_MIRROR_RP2_QUA: 1 = Enable address mirroring of rank pair 2 quaternary.
54	RW	ADDR_MIRROR_RP3_TER: 1 = Enable address mirroring of rank pair 3 tertiary.
55	RW	ADDR_MIRROR_RP3_QUA: 1 = Enable address mirroring of rank pair 3 quaternary.
56:63	RO	Constant = 0b00000000

Register Name	**PC Mode 0 RP1 Register**
Mnemonic	IOM0.DDRPHY_PC_MR0_RP1_P0
Address	8000C11C0701103F (SCOM)
Description	The value in this register reflects Mode Register 0 (MR0) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value that is intended for MR0 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). In multiple rank systems, the read latency and write latency values (that is CL, AL, and CWL) must be equal in all ranks. The values used by the DDR PHY are from the Rank Pair 0 Register for all read/write accesses.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	MODE_REGISTER_0_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 0 RP1 Register
Mnemonic	IOM0.DDRPHY_PC_MR0_RP1_P1
Address	8000C11C0701143F (SCOM)
Description	The value in this register reflects Mode Register 0 (MR0) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value that is intended for MR0 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). In multiple rank systems, the read latency and write latency values (that is CL, AL, and CWL) must be equal in all ranks. The values used by the DDR PHY are from the Rank Pair 0 Register for all read/write accesses.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_0_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 0 RP1 Register
Mnemonic	IOM0.DDRPHY_PC_MR0_RP1_P2
Address	8000C11C0701183F (SCOM)
Description	The value in this register reflects Mode Register 0 (MR0) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value that is intended for MR0 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). In multiple rank systems, the read latency and write latency values (that is CL, AL, and CWL) must be equal in all ranks. The values used by the DDR PHY are from the Rank Pair 0 Register for all read/write accesses.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_0_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 0 RP1 Register
Mnemonic	IOM0.DDRPHY_PC_MR0_RP1_P3
Address	8000C11C07011C3F (SCOM)
Description	The value in this register reflects Mode Register 0 (MR0) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value that is intended for MR0 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). In multiple rank systems, the read latency and write latency values (that is CL, AL, and CWL) must be equal in all ranks. The values used by the DDR PHY are from the Rank Pair 0 Register for all read/write accesses.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_0_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 1 RP1 Register
Mnemonic	IOM0.DDRPHY_PC_MR1_RP1_P0
Address	8000C11D0701103F (SCOM)
Description	The value in this register reflects Mode Register 1 (MR1) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR1 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_1_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 1 RP1 Register
Mnemonic	IOM0.DDRPHY_PC_MR1_RP1_P1
Address	8000C11D0701143F (SCOM)
Description	The value in this register reflects Mode Register 1 (MR1) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR1 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_1_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 1 RP1 Register
Mnemonic	IOM0.DDRPHY_PC_MR1_RP1_P2
Address	8000C11D0701183F (SCOM)
Description	The value in this register reflects Mode Register 1 (MR1) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR1 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_1_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 1 RP1 Register
Mnemonic	IOM0.DDRPHY_PC_MR1_RP1_P3
Address	8000C11D07011C3F (SCOM)
Description	The value in this register reflects Mode Register 1 (MR1) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR1 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_1_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 2 RP1 Register
Mnemonic	IOM0.DDRPHY_PC_MR2_RP1_P0
Address	8000C11E0701103F (SCOM)
Description	The value in this register reflects Mode Register 2 (MR2) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR2 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY core snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_2_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 2 RP1 Register
Mnemonic	IOM0.DDRPHY_PC_MR2_RP1_P1
Address	8000C11E0701143F (SCOM)
Description	The value in this register reflects Mode Register 2 (MR2) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR2 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY core snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_2_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 2 RP1 Register
Mnemonic	IOM0.DDRPHY_PC_MR2_RP1_P2
Address	8000C11E0701183F (SCOM)
Description	The value in this register reflects Mode Register 2 (MR2) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR2 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY core snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_2_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 2 RP1 Register
Mnemonic	IOM0.DDRPHY_PC_MR2_RP1_P3
Address	8000C11E07011C3F (SCOM)
Description	The value in this register reflects Mode Register 2 (MR2) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR2 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY core snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_2_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 3 RP1 Register
Mnemonic	IOM0.DDRPHY_PC_MR3_RP1_P0
Address	8000C11F0701103F (SCOM)
Description	The value in this register reflects Mode Register 3 (MR3) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_3_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 3 RP1 Register
Mnemonic	IOM0.DDRPHY_PC_MR3_RP1_P1
Address	8000C11F0701143F (SCOM)
Description	The value in this register reflects Mode Register 3 (MR3) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_3_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 3 RP1 Register
Mnemonic	IOM0.DDRPHY_PC_MR3_RP1_P2
Address	8000C11F0701183F (SCOM)
Description	The value in this register reflects Mode Register 3 (MR3) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_3_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 3 RP1 Register
Mnemonic	IOM0.DDRPHY_PC_MR3_RP1_P3
Address	8000C11F07011C3F (SCOM)
Description	The value in this register reflects Mode Register 3 (MR3) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_3_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 4 RP1 Register
Mnemonic	IOM0.DDRPHY_PC_MR4_RP1_P0
Address	8000C1200701103F (SCOM)
Description	The value in this register reflects Mode Register 4 (MR4) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_4_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 4 RP1 Register
Mnemonic	IOM0.DDRPHY_PC_MR4_RP1_P1
Address	8000C1200701143F (SCOM)
Description	The value in this register reflects Mode Register 4 (MR4) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_4_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 4 RP1 Register
Mnemonic	IOM0.DDRPHY_PC_MR4_RP1_P2
Address	8000C1200701183F (SCOM)
Description	The value in this register reflects Mode Register 4 (MR4) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Registerprogramming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_4_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	**PC Mode 4 RP1 Register**
Mnemonic	IOM0.DDRPHY_PC_MR4_RP1_P3
Address	8000C12007011C3F (SCOM)
Description	The value in this register reflects Mode Register 4 (MR4) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_4_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	**PC Mode 5 RP1 Register**
Mnemonic	IOM0.DDRPHY_PC_MR5_RP1_P0
Address	8000C1210701103F (SCOM)
Description	The value in this register reflects Mode Register 5 (MR5) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_5_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 5 RP1 Register
Mnemonic	IOM0.DDRPHY_PC_MR5_RP1_P1
Address	8000C1210701143F (SCOM)
Description	The value in this register reflects Mode Register 5 (MR5) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_5_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 5 RP1 Register
Mnemonic	IOM0.DDRPHY_PC_MR5_RP1_P2
Address	8000C1210701183F (SCOM)
Description	The value in this register reflects Mode Register 5 (MR5) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_5_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 5 RP1 Register
Mnemonic	IOM0.DDRPHY_PC_MR5_RP1_P3
Address	8000C12107011C3F (SCOM)
Description	The value in this register reflects Mode Register 5 (MR5) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_5_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 6 RP1 Register
Mnemonic	IOM0.DDRPHY_PC_MR6_RP1_P0
Address	8000C1220701103F (SCOM)
Description	The value in this register reflects Mode Register 6 (MR6) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_6_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 6 RP1 Register
Mnemonic	IOM0.DDRPHY_PC_MR6_RP1_P1
Address	8000C1220701143F (SCOM)
Description	The value in this register reflects Mode Register 6 (MR6) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_6_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 6 RP1 Register
Mnemonic	IOM0.DDRPHY_PC_MR6_RP1_P2
Address	8000C1220701183F (SCOM)
Description	The value in this register reflects Mode Register 6 (MR6) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_6_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 6 RP1 Register
Mnemonic	IOM0.DDRPHY_PC_MR6_RP1_P3
Address	8000C12207011C3F (SCOM)
Description	The value in this register reflects Mode Register 6 (MR6) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_6_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 7 RP1 Register
Mnemonic	IOM0.DDRPHY_PC_MR7_RP1_P0
Address	8000C1230701103F (SCOM)
Description	This register is provided solely for debugging firmware. It reflects the value that was snooped on the last mode register set (MRS) command sent to the DRAM. The PHY uses only the information contained in the PC Mode X Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_7_VALUE: Reserved.

Register Name	PC Mode 7 RP1 Register
Mnemonic	IOM0.DDRPHY_PC_MR7_RP1_P1
Address	8000C1230701143F (SCOM)
Description	This register is provided solely for debugging firmware. It reflects the value that was snooped on the last mode register set (MRS) command sent to the DRAM. The PHY uses only the information contained in the PC Mode X Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_7_VALUE: Reserved.

Register Name	PC Mode 7 RP1 Register
Mnemonic	IOM0.DDRPHY_PC_MR7_RP1_P2
Address	8000C1230701183F (SCOM)
Description	This register is provided solely for debugging firmware. It reflects the value that was snooped on the last mode register set (MRS) command sent to the DRAM. The PHY uses only the information contained in the PC Mode X Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_7_VALUE: Reserved.

Register Name	PC Mode 7 RP1 Register
Mnemonic	IOM0.DDRPHY_PC_MR7_RP1_P3
Address	8000C12307011C3F (SCOM)
Description	This register is provided solely for debugging firmware. It reflects the value that was snooped on the last mode register set (MRS) command sent to the DRAM. The PHY uses only the information contained in the PC Mode X Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_7_VALUE: Reserved.

Register Name	PC Mode 0 RP2 Register
Mnemonic	IOM0.DDRPHY_PC_MR0_RP2_P0
Address	8000C21C0701103F (SCOM)
Description	The value in this register reflects Mode Register 0 (MR0) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value that is intended for MR0 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). In multiple rank systems, the read latency and write latency values (that is CL, AL, and CWL) must be equal in all ranks. The values used by the DDR PHY are from the Rank Pair 0 Register for all read/write accesses.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_0_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 0 RP2 Register
Mnemonic	IOM0.DDRPHY_PC_MR0_RP2_P1
Address	8000C21C0701143F (SCOM)
Description	The value in this register reflects Mode Register 0 (MR0) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value that is intended for MR0 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). In multiple rank systems, the read latency and write latency values (that is CL, AL, and CWL) must be equal in all ranks. The values used by the DDR PHY are from the Rank Pair 0 Register for all read/write accesses.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_0_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 0 RP2 Register
Mnemonic	IOM0.DDRPHY_PC_MR0_RP2_P2
Address	8000C21C0701183F (SCOM)
Description	The value in this register reflects Mode Register 0 (MR0) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value that is intended for MR0 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). In multiple rank systems, the read latency and write latency values (that is CL, AL, and CWL) must be equal in all ranks. The values used by the DDR PHY are from the Rank Pair 0 Register for all read/write accesses.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_0_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 0 RP2 Register
Mnemonic	IOM0.DDRPHY_PC_MR0_RP2_P3
Address	8000C21C07011C3F (SCOM)
Description	The value in this register reflects Mode Register 0 (MR0) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value that is intended for MR0 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). In multiple rank systems, the read latency and write latency values (that is CL, AL, and CWL) must be equal in all ranks. The values used by the DDR PHY are from the Rank Pair 0 Register for all read/write accesses.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_0_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 1 RP2 Register
Mnemonic	IOM0.DDRPHY_PC_MR1_RP2_P0
Address	8000C21D0701103F (SCOM)
Description	The value in this register reflects Mode Register 1 (MR1) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR1 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_1_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 1 RP2 Register
Mnemonic	IOM0.DDRPHY_PC_MR1_RP2_P1
Address	8000C21D0701143F (SCOM)
Description	The value in this register reflects Mode Register 1 (MR1) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR1 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_1_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 1 RP2 Register
Mnemonic	IOM0.DDRPHY_PC_MR1_RP2_P2
Address	8000C21D0701183F (SCOM)
Description	The value in this register reflects Mode Register 1 (MR1) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR1 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_1_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 1 RP2 Register
Mnemonic	IOM0.DDRPHY_PC_MR1_RP2_P3
Address	8000C21D07011C3F (SCOM)
Description	The value in this register reflects Mode Register 1 (MR1) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR1 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_1_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 2 RP2 Register
Mnemonic	IOM0.DDRPHY_PC_MR2_RP2_P0
Address	8000C21E0701103F (SCOM)
Description	The value in this register reflects Mode Register 2 (MR2) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR2 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY core snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_2_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 2 RP2 Register
Mnemonic	IOM0.DDRPHY_PC_MR2_RP2_P1
Address	8000C21E0701143F (SCOM)
Description	The value in this register reflects Mode Register 2 (MR2) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR2 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY core snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_2_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 2 RP2 Register
Mnemonic	IOM0.DDRPHY_PC_MR2_RP2_P2
Address	8000C21E0701183F (SCOM)
Description	The value in this register reflects Mode Register 2 (MR2) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR2 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY core snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_2_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 2 RP2 Register
Mnemonic	IOM0.DDRPHY_PC_MR2_RP2_P3
Address	8000C21E07011C3F (SCOM)
Description	The value in this register reflects Mode Register 2 (MR2) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR2 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY core snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_2_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 3 RP2 Register
Mnemonic	IOM0.DDRPHY_PC_MR3_RP2_P0
Address	8000C21F0701103F (SCOM)
Description	The value in this register reflects Mode Register 3 (MR3) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_3_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 3 RP2 Register
Mnemonic	IOM0.DDRPHY_PC_MR3_RP2_P1
Address	8000C21F0701143F (SCOM)
Description	The value in this register reflects Mode Register 3 (MR3) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_3_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 3 RP2 Register
Mnemonic	IOM0.DDRPHY_PC_MR3_RP2_P2
Address	8000C21F0701183F (SCOM)
Description	The value in this register reflects Mode Register 3 (MR3) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_3_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 3 RP2 Register
Mnemonic	IOM0.DDRPHY_PC_MR3_RP2_P3
Address	8000C21F07011C3F (SCOM)
Description	The value in this register reflects Mode Register 3 (MR3) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_3_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 4 RP2 Register
Mnemonic	IOM0.DDRPHY_PC_MR4_RP2_P0
Address	8000C2200701103F (SCOM)
Description	The value in this register reflects Mode Register 4 (MR4) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_4_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 4 RP2 Register
Mnemonic	IOM0.DDRPHY_PC_MR4_RP2_P1
Address	8000C2200701143F (SCOM)
Description	The value in this register reflects Mode Register 4 (MR4) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_4_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 4 RP2 Register
Mnemonic	IOM0.DDRPHY_PC_MR4_RP2_P2
Address	8000C2200701183F (SCOM)
Description	The value in this register reflects Mode Register 4 (MR4) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_4_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	**PC Mode 4 RP2 Register**
Mnemonic	IOM0.DDRPHY_PC_MR4_RP2_P3
Address	8000C22007011C3F (SCOM)
Description	The value in this register reflects Mode Register 4 (MR4) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_4_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	**PC Mode 5 RP2 Register**
Mnemonic	IOM0.DDRPHY_PC_MR5_RP2_P0
Address	8000C2210701103F (SCOM)
Description	The value in this register reflects Mode Register 5 (MR5) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_5_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 5 RP2 Register
Mnemonic	IOM0.DDRPHY_PC_MR5_RP2_P1
Address	8000C2210701143F (SCOM)
Description	The value in this register reflects Mode Register 5 (MR5) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_5_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 5 RP2 Register
Mnemonic	IOM0.DDRPHY_PC_MR5_RP2_P2
Address	8000C2210701183F (SCOM)
Description	The value in this register reflects Mode Register 5 (MR5) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_5_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 5 RP2 Register
Mnemonic	IOM0.DDRPHY_PC_MR5_RP2_P3
Address	8000C22107011C3F (SCOM)
Description	The value in this register reflects Mode Register 5 (MR5) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_5_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 6 RP2 Register
Mnemonic	IOM0.DDRPHY_PC_MR6_RP2_P0
Address	8000C2220701103F (SCOM)
Description	The value in this register reflects Mode Register 6 (MR6) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_6_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 6 RP2 Register
Mnemonic	IOM0.DDRPHY_PC_MR6_RP2_P1
Address	8000C2220701143F (SCOM)
Description	The value in this register reflects Mode Register 6 (MR6) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_6_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 6 RP2 Register
Mnemonic	IOM0.DDRPHY_PC_MR6_RP2_P2
Address	8000C2220701183F (SCOM)
Description	The value in this register reflects Mode Register 6 (MR6) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_6_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 6 RP2 Register
Mnemonic	IOM0.DDRPHY_PC_MR6_RP2_P3
Address	8000C22207011C3F (SCOM)
Description	The value in this register reflects Mode Register 6 (MR6) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_6_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 7 RP2 Register
Mnemonic	IOM0.DDRPHY_PC_MR7_RP2_P0
Address	8000C2230701103F (SCOM)
Description	This register is provided solely for debugging firmware. It reflects the value that was snooped on the last mode register set (MRS) command sent to the DRAM. The PHY uses only the information contained in the PC Mode X Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_7_VALUE: Reserved.

Register Name	PC Mode 7 RP2 Register
Mnemonic	IOM0.DDRPHY_PC_MR7_RP2_P1
Address	8000C2230701143F (SCOM)
Description	This register is provided solely for debugging firmware. It reflects the value that was snooped on the last mode register set (MRS) command sent to the DRAM. The PHY uses only the information contained in the PC Mode X Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_7_VALUE: Reserved.

Register Name	PC Mode 7 RP2 Register
Mnemonic	IOM0.DDRPHY_PC_MR7_RP2_P2
Address	8000C2230701183F (SCOM)
Description	This register is provided solely for debugging firmware. It reflects the value that was snooped on the last mode register set (MRS) command sent to the DRAM. The PHY uses only the information contained in the PC Mode X Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_7_VALUE: Reserved.

Register Name	PC Mode 7 RP2 Register
Mnemonic	IOM0.DDRPHY_PC_MR7_RP2_P3
Address	8000C22307011C3F (SCOM)
Description	This register is provided solely for debugging firmware. It reflects the value that was snooped on the last mode register set (MRS) command sent to the DRAM. The PHY uses only the information contained in the PC Mode X Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_7_VALUE: Reserved.

Register Name	PC Mode 0 RP3 Register
Mnemonic	IOM0.DDRPHY_PC_MR0_RP3_P0
Address	8000C31C0701103F (SCOM)
Description	The value in this register reflects Mode Register 0 (MR0) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value that is intended for MR0 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). In multiple rank systems, the read latency and write latency values (that is CL, AL, and CWL) must be equal in all ranks. The values used by the DDR PHY are from the Rank Pair 0 Register for all read/write accesses.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_0_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 0 RP3 Register
Mnemonic	IOM0.DDRPHY_PC_MR0_RP3_P1
Address	8000C31C0701143F (SCOM)
Description	The value in this register reflects Mode Register 0 (MR0) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value that is intended for MR0 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). In multiple rank systems, the read latency and write latency values (that is CL, AL, and CWL) must be equal in all ranks. The values used by the DDR PHY are from the Rank Pair 0 Register for all read/write accesses.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_0_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 0 RP3 Register
Mnemonic	IOM0.DDRPHY_PC_MR0_RP3_P2
Address	8000C31C0701183F (SCOM)
Description	The value in this register reflects Mode Register 0 (MR0) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value that is intended for MR0 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). In multiple rank systems, the read latency and write latency values (that is CL, AL, and CWL) must be equal in all ranks. The values used by the DDR PHY are from the Rank Pair 0 Register for all read/write accesses.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_0_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 0 RP3 Register
Mnemonic	IOM0.DDRPHY_PC_MR0_RP3_P3
Address	8000C31C07011C3F (SCOM)
Description	The value in this register reflects Mode Register 0 (MR0) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value that is intended for MR0 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). In multiple rank systems, the read latency and write latency values (that is CL, AL, and CWL) must be equal in all ranks. The values used by the DDR PHY are from the Rank Pair 0 Register for all read/write accesses.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_0_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 1 RP3 Register
Mnemonic	IOM0.DDRPHY_PC_MR1_RP3_P0
Address	8000C31D0701103F (SCOM)
Description	The value in this register reflects Mode Register 1 (MR1) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR1 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_1_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 1 RP3 Register
Mnemonic	IOM0.DDRPHY_PC_MR1_RP3_P1
Address	8000C31D0701143F (SCOM)
Description	The value in this register reflects Mode Register 1 (MR1) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR1 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_1_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 1 RP3 Register
Mnemonic	IOM0.DDRPHY_PC_MR1_RP3_P2
Address	8000C31D0701183F (SCOM)
Description	The value in this register reflects Mode Register 1 (MR1) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR1 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_1_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 1 RP3 Register
Mnemonic	IOM0.DDRPHY_PC_MR1_RP3_P3
Address	8000C31D07011C3F (SCOM)
Description	The value in this register reflects Mode Register 1 (MR1) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR1 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_1_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 2 RP3 Register
Mnemonic	IOM0.DDRPHY_PC_MR2_RP3_P0
Address	8000C31E0701103F (SCOM)
Description	The value in this register reflects Mode Register 2 (MR2) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR2 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY core snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_2_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 2 RP3 Register
Mnemonic	IOM0.DDRPHY_PC_MR2_RP3_P1
Address	8000C31E0701143F (SCOM)
Description	The value in this register reflects Mode Register 2 (MR2) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR2 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY core snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_2_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 2 RP3 Register
Mnemonic	IOM0.DDRPHY_PC_MR2_RP3_P2
Address	8000C31E0701183F (SCOM)
Description	The value in this register reflects Mode Register 2 (MR2) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR2 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY core snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_2_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 2 RP3 Register
Mnemonic	IOM0.DDRPHY_PC_MR2_RP3_P3
Address	8000C31E07011C3F (SCOM)
Description	The value in this register reflects Mode Register 2 (MR2) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR2 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY core snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_2_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 3 RP3 Register
Mnemonic	IOM0.DDRPHY_PC_MR3_RP3_P0
Address	8000C31F0701103F (SCOM)
Description	The value in this register reflects Mode Register 3 (MR3) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_3_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 3 RP3 Register
Mnemonic	IOM0.DDRPHY_PC_MR3_RP3_P1
Address	8000C31F0701143F (SCOM)
Description	The value in this register reflects Mode Register 3 (MR3) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_3_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 3 RP3 Register
Mnemonic	IOM0.DDRPHY_PC_MR3_RP3_P2
Address	8000C31F0701183F (SCOM)
Description	The value in this register reflects Mode Register 3 (MR3) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_3_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 3 RP3 Register
Mnemonic	IOM0.DDRPHY_PC_MR3_RP3_P3
Address	8000C31F07011C3F (SCOM)
Description	The value in this register reflects Mode Register 3 (MR3) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_3_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 4 RP3 Register
Mnemonic	IOM0.DDRPHY_PC_MR4_RP3_P0
Address	8000C3200701103F (SCOM)
Description	The value in this register reflects Mode Register 4 (MR4) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_4_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 4 RP3 Register
Mnemonic	IOM0.DDRPHY_PC_MR4_RP3_P1
Address	8000C3200701143F (SCOM)
Description	The value in this register reflects Mode Register 4 (MR4) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_4_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 4 RP3 Register
Mnemonic	IOM0.DDRPHY_PC_MR4_RP3_P2
Address	8000C3200701183F (SCOM)
Description	The value in this register reflects Mode Register 4 (MR4) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_4_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 4 RP3 Register
Mnemonic	IOM0.DDRPHY_PC_MR4_RP3_P3
Address	8000C32007011C3F (SCOM)
Description	The value in this register reflects Mode Register 4 (MR4) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_4_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 5 RP3 Register
Mnemonic	IOM0.DDRPHY_PC_MR5_RP3_P0
Address	8000C3210701103F (SCOM)
Description	The value in this register reflects Mode Register 5 (MR5) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_5_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 5 RP3 Register
Mnemonic	IOM0.DDRPHY_PC_MR5_RP3_P1
Address	8000C3210701143F (SCOM)
Description	The value in this register reflects Mode Register 5 (MR5) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_5_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 5 RP3 Register
Mnemonic	IOM0.DDRPHY_PC_MR5_RP3_P2
Address	8000C3210701183F (SCOM)
Description	The value in this register reflects Mode Register 5 (MR5) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_5_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 5 RP3 Register
Mnemonic	IOM0.DDRPHY_PC_MR5_RP3_P3
Address	8000C32107011C3F (SCOM)
Description	The value in this register reflects Mode Register 5 (MR5) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_5_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 6 RP3 Register
Mnemonic	IOM0.DDRPHY_PC_MR6_RP3_P0
Address	8000C3220701103F (SCOM)
Description	The value in this register reflects Mode Register 6 (MR6) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_6_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 6 RP3 Register
Mnemonic	IOM0.DDRPHY_PC_MR6_RP3_P1
Address	8000C3220701143F (SCOM)
Description	The value in this register reflects Mode Register 6 (MR6) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_6_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 6 RP3 Register
Mnemonic	IOM0.DDRPHY_PC_MR6_RP3_P2
Address	8000C3220701183F (SCOM)
Description	The value in this register reflects Mode Register 6 (MR6) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_6_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 6 RP3 Register
Mnemonic	IOM0.DDRPHY_PC_MR6_RP3_P3
Address	8000C32207011C3F (SCOM)
Description	The value in this register reflects Mode Register 6 (MR6) for the primary rank of the targeted rank pair as defined in PC rank pair 0 and PC rank pair 1. The value in this register must reflect the operational value intended for MR3 of the targeted rank of memory. The contents of this register are updated when written, or when a mode register set (MRS) command is sent from the memory controller (that is, the DDR PHY snoops the command as it is sent to the memory). Snooped Mode Register programming for RP0 primary is used to configure PHY latencies for all ranks. Therefore, the RP0 primary rank Mode Registers must be correctly programmed for proper PHY functionality. In multiple rank systems, the read latency and write latency values (that is, CL, AL, CWL, and PL) must be consistent in all ranks and rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_6_VALUE: The values in this register must match the values in the DRAM. Refer to the JEDEC DDR4 standard for details of the contents.

Register Name	PC Mode 7 RP3 Register
Mnemonic	IOM0.DDRPHY_PC_MR7_RP3_P0
Address	8000C3230701103F (SCOM)
Description	This register is provided solely for debugging firmware. It reflects the value that was snooped on the last mode register set (MRS) command sent to the DRAM. The PHY uses only the information contained in the PC Mode X Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_7_VALUE: Reserved.

Register Name	PC Mode 7 RP3 Register
Mnemonic	IOM0.DDRPHY_PC_MR7_RP3_P1
Address	8000C3230701143F (SCOM)
Description	This register is provided solely for debugging firmware. It reflects the value that was snooped on the last mode register set (MRS) command sent to the DRAM. The PHY uses only the information contained in the PC Mode X Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_7_VALUE: Reserved.

Register Name	PC Mode 7 RP3 Register
Mnemonic	IOM0.DDRPHY_PC_MR7_RP3_P2
Address	8000C3230701183F (SCOM)
Description	This register is provided solely for debugging firmware. It reflects the value that was snooped on the last mode register set (MRS) command sent to the DRAM. The PHY uses only the information contained in the PC Mode X Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_7_VALUE: Reserved.

Register Name	PC Mode 7 RP3 Register
Mnemonic	IOM0.DDRPHY_PC_MR7_RP3_P3
Address	8000C32307011C3F (SCOM)
Description	This register is provided solely for debugging firmware. It reflects the value that was snooped on the last mode register set (MRS) command sent to the DRAM. The PHY uses only the information contained in the PC Mode X Registers.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	MODE_REGISTER_7_VALUE: Reserved.

8. DDRPHY: RC Registers

This section contains the registers located in the read control (RC) logic. The RC registers are listed alphabetically by mnemonic in the following address table.

The RC registers are listed in the following tables.

Register Name	RC Configuration 0 Register
Mnemonic	IOM0.DDRPHY_RC_CONFIG0_P0
Address	8000C8000701103F (SCOM)
Description	This register contains global configuration information to control the read control logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:51	RW	**Note:** This field is not used functionally in the POWER9 design. However, it must be programmed correctly to load the debug bus into the trace array and to compute the rdtag_dly value used by the memory controller. GLOBAL_PHY_OFFSET: Global PHY Offset (GPO). This field is the number of memory clock cycles added to the total read latency in the PHY. GPO = 7 + System_delay + tDQSCK + RCD_Delay + DB_Delay Where: System_delay is the round-trip delay in the memory system and includes: • The delay from the POWER9 memory clock output pin to the DRAM input pin • The delay from the DRAM DQS output pin to the POWER9 DQS input pin tDQSCK is taken from the JEDEC DDR4 specification. RCD_Delay is the clock delay through the RCD device. DB_Delay is the DQS delay through the data buffer device (LRDIMMs only). Using typical board wiring and the DRAM specification for RDIMMs, the GPO is: • 12 at 1866 Gbps • 12 at 2133 Gbps • 13 at 2400 Gbps • 13 at 2666 Gbps
52	RW	Reserved.
53	RW	PER_DUTY_CYCLE_SW: Set to 0 for normal function. Read commands are generated during periodic calibration with a 50% duty cycle. When set to 1, periodic calibration issues read commands continuously.
54:56	RW	NUM_PERIODIC_CAL: Each time a periodic calibration request occurs, each enabled periodic calibration routine is executed NUM_PERIODIC_CAL + 1 times. This applies to the SysClk/RdClk alignment, DQS alignment, and read-centering periodic calibration routines.
57:61	RO	Reserved.
62	RW	PERFORM_RDCLK_ALIGN: This bit must be set to 1b in hardware. This bit provides a method for behavioral simulations to skip the SysClk/RdClk alignment calibration step. 1 = The SysClk/RdClk alignment calibration must be performed for correct operation. 0 = In a zero wire delay behavioral simulation, the RTL ignores the register settings associated with SysClk/RdClk alignment. Values in the DP16 DQS Read Phase Select Register have no effect. The SysClk/RdClk alignment calibration fails if it is run.
63	RW	STAGGERED_PATTERN: 0 = A[12:11], MPR Read Format, of the Mode Register 3 (MR3) register in DDR4 memory modules is set to serial mode by the DDR PHY during custom read centering or initial pattern write. 1 = A[12:11], MPR Read Format, of the MR3 register in DDR4 memory modules is set to staggered mode by the DDR PHY during custom read centering or initial pattern write. **Note:** The A bits represent bit positions 15:0 in the mode register.

Register Name	**RC Configuration 0 Register**
Mnemonic	IOM0.DDRPHY_RC_CONFIG0_P1
Address	8000C8000701143F (SCOM)
Description	This register contains global configuration information to control the read control logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:51	RW	**Note:** This field is not used functionally in the POWER9 design. However, it must be programmed correctly to load the debug bus into the trace array and to compute the rdtag_dly value used by the memory controller. GLOBAL_PHY_OFFSET: Global PHY Offset (GPO). This field is the number of memory clock cycles added to the total read latency in the PHY. GPO = 7 + System_delay + tDQSCK + RCD_Delay + DB_Delay Where: System_delay is the round-trip delay in the memory system and includes: • The delay from the POWER9 memory clock output pin to the DRAM input pin • The delay from the DRAM DQS output pin to the POWER9 DQS input pin tDQSCK is taken from the JEDEC DDR4 specification. RCD_Delay is the clock delay through the RCD device. DB_Delay is the DQS delay through the data buffer device (LRDIMMs only). Using typical board wiring and the DRAM specification for RDIMMs, the GPO is: • 12 at 1866 Gbps • 12 at 2133 Gbps • 13 at 2400 Gbps • 13 at 2666 Gbps
52	RW	Reserved.
53	RW	PER_DUTY_CYCLE_SW: Set to 0 for normal function. Read commands are generated during periodic calibration with a 50% duty cycle. When set to 1, periodic calibration issues read commands continuously.
54:56	RW	NUM_PERIODIC_CAL: Each time a periodic calibration request occurs, each enabled periodic calibration routine is executed NUM_PERIODIC_CAL + 1 times. This applies to the SysClk/RdClk alignment, DQS alignment, and read-centering periodic calibration routines.
57:61	RO	Reserved.
62	RW	PERFORM_RDCLK_ALIGN: This bit must be set to 1b in hardware. This bit provides a method for behavioral simulations to skip the SysClk/RdClk alignment calibration step. 1 = The SysClk/RdClk alignment calibration must be performed for correct operation. 0 = In a zero wire delay behavioral simulation, the RTL ignores the register settings associated with SysClk/RdClk alignment. Values in the DP16 DQS Read Phase Select Register have no effect. The SysClk/RdClk alignment calibration fails if it is run.
63	RW	STAGGERED_PATTERN: 0 = A[12:11], MPR Read Format, of the MR3 register in DDR4 memory modules is set to serial mode by the DDR PHY during custom read centering or initial pattern write. 1 = A[12:11], MPR Read Format, of the MR3 register in DDR4 memory modules is set to staggered mode by the DDR PHY during custom read centering or initial pattern write. **Note:** The A bits represent bit positions 15:0 in the mode register.

Register Name	RC Configuration 0 Register
Mnemonic	IOM0.DDRPHY_RC_CONFIG0_P2
Address	8000C8000701183F (SCOM)
Description	This register contains global configuration information to control the read control logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:51	RW	**Note:** This field is not used functionally in the POWER9 design. However, it must be programmed correctly to load the debug bus into the trace array and to compute the rdtag_dly value used by the memory controller. GLOBAL_PHY_OFFSET: Global PHY Offset (GPO). This field is the number of memory clock cycles added to the total read latency in the PHY. GPO = 7 + System_delay + tDQSCK + RCD_Delay + DB_Delay Where: System_delay is the round-trip delay in the memory system and includes: • The delay from the POWER9 memory clock output pin to the DRAM input pin • The delay from the DRAM DQS output pin to the POWER9 DQS input pin tDQSCK is taken from the JEDEC DDR4 specification. RCD_Delay is the clock delay through the RCD device. DB_Delay is the DQS delay through the data buffer device (LRDIMMs only). Using typical board wiring and the DRAM specification for RDIMMs, the GPO is: • 12 at 1866 Gbps • 12 at 2133 Gbps • 13 at 2400 Gbps • 13 at 2666 Gbps
52	RW	Reserved.
53	RW	PER_DUTY_CYCLE_SW: Set to 0 for normal function. Read commands are generated during periodic calibration with a 50% duty cycle. When set to 1, periodic calibration issues read commands continuously.
54:56	RW	NUM_PERIODIC_CAL: Each time a periodic calibration request occurs, each enabled periodic calibration routine is executed NUM_PERIODIC_CAL + 1 times. This applies to the SysClk/RdClk alignment, DQS alignment, and read-centering periodic calibration routines.
57:61	RO	Reserved.
62	RW	PERFORM_RDCLK_ALIGN: This bit must be set to 1b in hardware. This bit provides a method for behavioral simulations to skip the SysClk/RdClk alignment calibration step. 1 = The SysClk/RdClk alignment calibration must be performed for correct operation. 0 = In a zero wire delay behavioral simulation, the RTL ignores the register settings associated with SysClk/RdClk alignment. Values in the DP16 DQS Read Phase Select Register have no effect. The SysClk/RdClk alignment calibration fails if it is run.
63	RW	STAGGERED_PATTERN: 0 = A[12:11], MPR Read Format, of the MR3 register in DDR4 memory modules is set to serial mode by the DDR PHY during custom read centering or initial pattern write. 1 = A[12:11], MPR Read Format, of the MR3 register in DDR4 memory modules is set to staggered mode by the DDR PHY during custom read centering or initial pattern write. **Note:** The A bits represent bit positions 15:0 in the mode register.

Register Name	RC Configuration 0 Register
Mnemonic	IOM0.DDRPHY_RC_CONFIG0_P3
Address	8000C80007011C3F (SCOM)
Description	This register contains global configuration information to control the read control logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:51	RW	**Note:** This field is not used functionally in the POWER9 design. However, it must be programmed correctly to load the debug bus into the trace array and to compute the rdtag_dly value used by the memory controller. GLOBAL_PHY_OFFSET: Global PHY Offset (GPO). This field is the number of memory clock cycles added to the total read latency in the PHY. GPO = 7 + System_delay + tDQSCK + RCD_Delay + DB_Delay Where: System_delay is the round-trip delay in the memory system and includes: • The delay from the POWER9 memory clock output pin to the DRAM input pin • The delay from the DRAM DQS output pin to the POWER9 DQS input pin tDQSCK is taken from the JEDEC DDR4 specification. RCD_Delay is the clock delay through the RCD device. DB_Delay is the DQS delay through the data buffer device (LRDIMMs only). Using typical board wiring and the DRAM specification for RDIMMs, the GPO is: • 12 at 1866 Gbps • 12 at 2133 Gbps • 13 at 2400 Gbps • 13 at 2666 Gbps
52	RW	Reserved.
53	RW	PER_DUTY_CYCLE_SW: Set to 0 for normal function. Read commands are generated during periodic calibration with a 50% duty cycle. When set to 1, periodic calibration issues read commands continuously.
54:56	RW	NUM_PERIODIC_CAL: Each time a periodic calibration request occurs, each enabled periodic calibration routine is executed NUM_PERIODIC_CAL + 1 times. This applies to the SysClk/RdClk alignment, DQS alignment, and read-centering periodic calibration routines.
57:61	RO	Reserved.
62	RW	PERFORM_RDCLK_ALIGN: This bit must be set to 1b in hardware. This bit provides a method for behavioral simulations to skip the SysClk/RdClk alignment calibration step. 1 = The SysClk/RdClk alignment calibration must be performed for correct operation. 0 = In a zero wire delay behavioral simulation, the RTL ignores the register settings associated with SysClk/RdClk alignment. Values in the DP16 DQS Read Phase Select Register have no effect. The SysClk/RdClk alignment calibration fails if it is run.
63	RW	STAGGERED_PATTERN: 0 = A[12:11], MPR Read Format, of the MR3 register in DDR4 memory modules is set to serial mode by the DDR PHY during custom read centering or initial pattern write. 1 = A[12:11], MPR Read Format, of the MR3 register in DDR4 memory modules is set to staggered mode by the DDR PHY during custom read centering or initial pattern write. **Note:** The A bits represent bit positions 15:0 in the mode register.

Register Name	RC Configuration 1 Register
Mnemonic	IOM0.DDRPHY_RC_CONFIG1_P0
Address	8000C8010701103F (SCOM)
Description	This register contains global configuration information to control the read control logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:61	RW	OUTER_LOOP_CNT: This field must remain at the reset value for normal mainline operation. It provides the outer loop iteration count for the "digital eye." This field must be loaded with the required number of outer loop iterations before starting the digital eye function.
62:63	RO	Constant = 0b00

Register Name	RC Configuration 1 Register
Mnemonic	IOM0.DDRPHY_RC_CONFIG1_P1
Address	8000C8010701143F (SCOM)
Description	This register contains global configuration information to control the read control logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:61	RW	OUTER_LOOP_CNT: This field must remain at the reset value for normal mainline operation. It provides the outer loop iteration count for the "digital eye." This field must be loaded with the required number of outer loop iterations before starting the digital eye function.
62:63	RO	Constant = 0b00

Register Name	RC Configuration 1 Register
Mnemonic	IOM0.DDRPHY_RC_CONFIG1_P2
Address	8000C8010701183F (SCOM)
Description	This register contains global configuration information to control the read control logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:61	RW	OUTER_LOOP_CNT: This field must remain at the reset value for normal mainline operation. It provides the outer loop iteration count for the "digital eye." This field must be loaded with the required number of outer loop iterations before starting the digital eye function.
62:63	RO	Constant = 0b00

Register Name	RC Configuration 1 Register
Mnemonic	IOM0.DDRPHY_RC_CONFIG1_P3
Address	8000C80107011C3F (SCOM)
Description	This register contains global configuration information to control the read control logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:61	RW	OUTER_LOOP_CNT: This field must remain at the reset value for normal mainline operation. It provides the outer loop iteration count for the "digital eye." This field must be loaded with the required number of outer loop iterations before starting the digital eye function.
62:63	RO	Constant = 0b00

Register Name	RC Configuration 2 Register
Mnemonic	IOM0.DDRPHY_RC_CONFIG2_P0
Address	8000C8020701103F (SCOM)
Description	This register contains global configuration information to control the read control logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:52	RW	CONSEC_PASS: When DIGITAL_EYE_EN is 0b in the DP16 DFT Digital Eye Register, this field specifies the number of consecutive passes required when determining the left edge of the data eye when stepping the read strobe/clock through the phase rotator. This field must be set to minimum value of 6 when sampling 8 beats of data, and to a minimum value of 12 when sampling 4 beats of data. When DIGITAL_EYE_EN is 1b in the DP16 DFT Digital Eye Register, this field specifies the minimum number of cycles between outer loop iterations of the "digital eye" (0 - 31 tCK cycles).
53:58	RO	Constant = 0b000000
59	RW	ALLOW_RD_FIFO_AUTO_RESET: Automatic reset control for the read FIFO. 0 = Allow the RD FIFO to auto reset pointers on the rank switch. 1 = Prevent the RD FIFO auto reset of pointers on the rank switch.
60:63	RO	Constant = 0b0000

Register Name	RC Configuration 2 Register
Mnemonic	IOM0.DDRPHY_RC_CONFIG2_P1
Address	8000C8020701143F (SCOM)
Description	This register contains global configuration information to control the read control logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:52	RW	CONSEC_PASS: When DIGITAL_EYE_EN is 0b in the DP16 DFT Digital Eye Register, this field specifies the number of consecutive passes required when determining the left edge of the data eye when stepping the read strobe/clock through the phase rotator. This field must be set to minimum value of 6 when sampling 8 beats of data, and to a minimum value of 12 when sampling 4 beats of data. When DIGITAL_EYE_EN is 1b in the DP16 DFT Digital Eye Register, this field specifies the minimum number of cycles between outer loop iterations of the "digital eye" (0 - 31 tCK cycles).
53:58	RO	Constant = 0b000000
59	RW	ALLOW_RD_FIFO_AUTO_RESET: Automatic reset control for the read FIFO. 0 = Allow the RD FIFO to auto reset pointers on the rank switch. 1 = Prevent the RD FIFO auto reset of pointers on the rank switch.
60:63	RO	Constant = 0b0000

Register Name	RC Configuration 2 Register
Mnemonic	IOM0.DDRPHY_RC_CONFIG2_P2
Address	8000C8020701183F (SCOM)
Description	This register contains global configuration information to control the read control logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:52	RW	CONSEC_PASS: When DIGITAL_EYE_EN is 0b in the DP16 DFT Digital Eye Register, this field specifies the number of consecutive passes required when determining the left edge of the data eye when stepping the read strobe/clock through the phase rotator. This field must be set to minimum value of 6 when sampling 8 beats of data, and to a minimum value of 12 when sampling 4 beats of data. When DIGITAL_EYE_EN is 1b in the DP16 DFT Digital Eye Register, this field specifies the minimum number of cycles between outer loop iterations of the "digital eye" (0 - 31 tCK cycles).
53:58	RO	Constant = 0b000000
59	RW	ALLOW_RD_FIFO_AUTO_RESET: Automatic reset control for the read FIFO. 0 = Allow the RD FIFO to auto reset pointers on the rank switch. 1 = Prevent the RD FIFO auto reset of pointers on the rank switch.
60:63	RO	Constant = 0b0000

Register Name	RC Configuration 2 Register
Mnemonic	IOM0.DDRPHY_RC_CONFIG2_P3
Address	8000C80207011C3F (SCOM)
Description	This register contains global configuration information to control the read control logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:52	RW	CONSEC_PASS: When DIGITAL_EYE_EN is 0b in the DP16 DFT Digital Eye Register, this field specifies the number of consecutive passes required when determining the left edge of the data eye when stepping the read strobe/clock through the phase rotator. This field must be set to minimum value of 6 when sampling 8 beats of data, and to a minimum value of 12 when sampling 4 beats of data. When DIGITAL_EYE_EN is 1b in the DP16 DFT Digital Eye Register, this field specifies the minimum number of cycles between outer loop iterations of the "digital eye" (0 - 31 tCK cycles).
53:58	RO	Constant = 0b000000
59	RW	ALLOW_RD_FIFO_AUTO_RESET: Automatic reset control for the read FIFO. 0 = Allow the RD FIFO to auto reset pointers on the rank switch. 1 = Prevent the RD FIFO auto reset of pointers on the rank switch.
60:63	RO	Constant = 0b0000

Register Name	RC Error Status 0 Register
Mnemonic	IOM0.DDRPHY_RC_ERROR_STATUS0_P0
Address	8000C8050701103F (SCOM)
Description	This register contains error information about the read control logic. It contains composite error information from the DP16 logic blocks regarding read calibration algorithms. Before writing this register to 0b, DDRPHY_DP16_RD_STATUS0, if set, must be written to 0b.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	RD_ERROR: 1 = Read control (RC) error.
49	RW	DP16_ERROR: 1 = An error from DP16 was detected. See the DP16 Read Status 0 Register for more information.
50	RW	CNTR_UNDERFLOW_ERROR: 1 = An error from counter underflow was detected.
51	RW	CNTR_OVERFLOW_ERROR: 1 = An error from counter overflow was detected.
52:63	RO	Constant = 0b0000000000000000

Register Name	RC Error Status 0 Register
Mnemonic	IOM0.DDRPHY_RC_ERROR_STATUS0_P1
Address	8000C8050701143F (SCOM)
Description	This register contains error information about the read control logic. It contains composite error information from the DP16 logic blocks regarding read calibration algorithms. Before writing this register to 0b, DDRPHY_DP16_RD_STATUS0, if set, must be written to 0b.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	RD_ERROR: 1 = Read control (RC) error.
49	RW	DP16_ERROR: 1 = An error from DP16 was detected. See the DP16 Read Status 0 Register for more information.
50	RW	CNTR_UNDERFLOW_ERROR: 1 = An error from counter underflow was detected.
51	RW	CNTR_OVERFLOW_ERROR: 1 = An error from counter overflow was detected.
52:63	RO	Constant = 0b0000000000000000

Register Name	RC Error Status 0 Register
Mnemonic	IOM0.DDRPHY_RC_ERROR_STATUS0_P2
Address	8000C8050701183F (SCOM)
Description	This register contains error information about the read control logic. It contains composite error information from the DP16 logic blocks regarding read calibration algorithms. Before writing this register to 0b, DDRPHY_DP16_RD_STATUS0, if set, must be written to 0b.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	RD_ERROR: 1 = Read control (RC) error.
49	RW	DP16_ERROR: 1 = An error from DP16 was detected. See the DP16 Read Status 0 Register for more information.
50	RW	CNTR_UNDERFLOW_ERROR: 1 = An error from counter underflow was detected.
51	RW	CNTR_OVERFLOW_ERROR: 1 = An error from counter overflow was detected.
52:63	RO	Constant = 0b0000000000000000

Register Name	RC Error Status 0 Register
Mnemonic	IOM0.DDRPHY_RC_ERROR_STATUS0_P3
Address	8000C80507011C3F (SCOM)
Description	This register contains error information about the read control logic. It contains composite error information from the DP16 logic blocks regarding read calibration algorithms. Before writing this register to 0b, DDRPHY_DP16_RD_STATUS0, if set, must be written to 0b.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	RD_ERROR: 1 = Read control (RC) error.
49	RW	DP16_ERROR: 1 = An error from DP16 was detected. See the DP16 Read Status 0 Register for more information.
50	RW	CNTR_UNDERFLOW_ERROR: 1 = An error from counter underflow was detected.
51	RW	CNTR_OVERFLOW_ERROR: 1 = An error from counter overflow was detected.
52:63	RO	Constant = 0b0000000000000000

Register Name	RC Error Mask 0 Register
Mnemonic	IOM0.DDRPHY_RC_ERROR_MASK0_P0
Address	8000C80607011O3F (SCOM)
Description	This register masks errors in the RC Error Status 0 Register. It prevents the RC_ERROR bit from being set in the PC Error Status 0 Register and the appropriate bit from being set in PC Initial Calibration Error Register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	RD_ERROR_MASK: 1 = Mask RD_ERROR.
49:63	RO	Constant = 0b0000000000000000

Register Name	RC Error Mask 0 Register
Mnemonic	IOM0.DDRPHY_RC_ERROR_MASK0_P1
Address	8000C8060701143F (SCOM)
Description	This register masks errors in the RC Error Status 0 Register. It prevents the RC_ERROR bit from being set in the PC Error Status 0 Register and the appropriate bit from being set in PC Initial Calibration Error Register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	RD_ERROR_MASK: 1 = Mask RD_ERROR.
49:63	RO	Constant = 0b000000000000000

Register Name	RC Error Mask 0 Register
Mnemonic	IOM0.DDRPHY_RC_ERROR_MASK0_P2
Address	8000C8060701183F (SCOM)
Description	This register masks errors in the RC Error Status 0 Register. It prevents the RC_ERROR bit from being set in the PC Error Status 0 Register and the appropriate bit from being set in PC Initial Calibration Error Register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	RD_ERROR_MASK: 1 = Mask RD_ERROR.
49:63	RO	Constant = 0b000000000000000

Register Name	RC Error Mask 0 Register
Mnemonic	IOM0.DDRPHY_RC_ERROR_MASK0_P3
Address	8000C80607011C3F (SCOM)
Description	This register masks errors in the RC Error Status 0 Register. It prevents the RC_ERROR bit from being set in the PC Error Status 0 Register and the appropriate bit from being set in PC Initial Calibration Error Register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	RD_ERROR_MASK: 1 = Mask RD_ERROR.
49:63	RO	Constant = 0b000000000000000

Register Name	RC Configuration 3 Register
Mnemonic	IOM0.DDRPHY_RC_CONFIG3_P0
Address	8000C8070701103F (SCOM)
Description	This register contains global configuration information to control the read control logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:50	RW	FINE_CAL_STEP_SIZE: Fine calibration step size: 000 = 1/128. 001 = 1/64. 010 = 3/128. 011 = 1/32. 100 = 5/128. 101 = 3/64. 110 = 7/128. 111 = 1/16.
51:54	RW	COARSE_CAL_STEP_SIZE: Coarse calibration step size: 0000 = 1/128. 0001 = 1/64. 0010 = 3/128. 0011 = 1/32. 0100 = 5/128. 0101 = 3/64. 0110 = 7/128. 0111 = 1/161. 1000 - 1111 = Reserved. When DIGITAL_EYE_EN is 1b in the DP16 DFT Digital Eye Register: bit 51:52: Reserved. bit 53: DIGEYE_16_NOT_1: 1 = A block of 16 BL8s is issued during each outer loop iteration of "digital eye." 0 = One BL8 read is issued during each outer loop iteration of "digital eye." bit 54: DIGEYE_REFRESH: 1 = Issues a precharge and refresh during every outer loop iteration of "digital eye." 0 = Issues a precharge and refresh at least once every 16 outer loop iterations of "digital eye."
55:56	RWX	DQ_SEL_QUAD: The quadrant within the DP16 being calibrated (read calibrations). Can also be set statically for "digital eye." This field must not be modified while the calibration is running. This field is part of a counter that automatically increments during some types of calibrations.
57:59	RWX	DQ_SEL_LANE: The data bit within the DP16 being calibrated (read calibrations). Can also be set statically for "digital eye." This field must not be modified while the calibration is running. This field is part of a counter that automatically increments during some types of calibrations.
60:63	RO	Constant = 0b0000

Register Name	RC Configuration 3 Register
Mnemonic	IOM0.DDRPHY_RC_CONFIG3_P1
Address	8000C8070701143F (SCOM)
Description	This register contains global configuration information to control the read control logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:50	RW	FINE_CAL_STEP_SIZE: Fine calibration step size: 000 = 1/128. 001 = 1/64. 010 = 3/128. 011 = 1/32. 100 = 5/128. 101 = 3/64. 110 = 7/128. 111 = 1/16.

Bits	SCOM	Field Mnemonic: Description
51:54	RW	COARSE_CAL_STEP_SIZE: Coarse calibration step size: 0000 = 1/128. 0001 = 1/64. 0010 = 3/128. 0011 = 1/32. 0100 = 5/128. 0101 = 3/64. 0110 = 7/128. 0111 = 1/161. 1000 - 1111 = Reserved. When DIGITAL_EYE_EN is 1b in the DP16 DFT Digital Eye Register: bit 51:52: Reserved. bit 53: DIGEYE_16_NOT_1: 1 = A block of 16 BL8s is issued during each outer loop iteration of "digital eye." 0 = One BL8 read is issued during each outer loop iteration of "digital eye." bit 54: DIGEYE_REFRESH: 1 = Issues a precharge and refresh during every outer loop iteration of "digital eye." 0 = Issues a precharge and refresh at least once every 16 outer loop iterations of "digital eye."
55:56	RWX	DQ_SEL_QUAD: The quadrant within the DP16 being calibrated (read calibrations). Can also be set statically for "digital eye." This field must not be modified while the calibration is running. This field is part of a counter that automatically increments during some types of calibrations.
57:59	RWX	DQ_SEL_LANE: The data bit within the DP16 being calibrated (read calibrations). Can also be set statically for "digital eye." This field must not be modified while the calibration is running. This field is part of a counter that automatically increments during some types of calibrations.
60:63	RO	Constant = 0b0000

Register Name	RC Configuration 3 Register
Mnemonic	IOM0.DDRPHY_RC_CONFIG3_P2
Address	8000C8070701183F (SCOM)
Description	This register contains global configuration information to control the read control logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	FINE_CAL_STEP_SIZE: Fine calibration step size: 000 = 1/128. 001 = 1/64. 010 = 3/128. 011 = 1/32. 100 = 5/128. 101 = 3/64. 110 = 7/128. 111 = 1/16.

Bits	SCOM	Field Mnemonic: Description
51:54	RW	COARSE_CAL_STEP_SIZE: Coarse calibration step size: 0000 = 1/128. 0001 = 1/64. 0010 = 3/128. 0011 = 1/32. 0100 = 5/128. 0101 = 3/64. 0110 = 7/128. 0111 = 1/161. 1000 - 1111 = Reserved. When DIGITAL_EYE_EN is 1b in the DP16 DFT Digital Eye Register: bit 51:52: Reserved. bit 53: DIGEYE_16_NOT_1: 1 = A block of 16 BL8s is issued during each outer loop iteration of "digital eye." 0 = One BL8 read is issued during each outer loop iteration of "digital eye." bit 54: DIGEYE_REFRESH: 1 = Issues a precharge and refresh during every outer loop iteration of "digital eye." 0 = Issues a precharge and refresh at least once every 16 outer loop iterations of "digital eye."
55:56	RWX	DQ_SEL_QUAD: The quadrant within the DP16 being calibrated (read calibrations). Can also be set statically for "digital eye." This field must not be modified while the calibration is running. This field is part of a counter that automatically increments during some types of calibrations.
57:59	RWX	DQ_SEL_LANE: The data bit within the DP16 being calibrated (read calibrations). Can also be set statically for "digital eye." This field must not be modified while the calibration is running. This field is part of a counter that automatically increments during some types of calibrations.
60:63	RO	Constant = 0b0000

Register Name	RC Configuration 3 Register
Mnemonic	IOM0.DDRPHY_RC_CONFIG3_P3
Address	8000C80707011C3F (SCOM)
Description	This register contains global configuration information to control the read control logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	FINE_CAL_STEP_SIZE: Fine calibration step size: 000 = 1/128. 001 = 1/64. 010 = 3/128. 011 = 1/32. 100 = 5/128. 101 = 3/64. 110 = 7/128. 111 = 1/16.

Bits	SCOM	Field Mnemonic: Description
51:54	RW	COARSE_CAL_STEP_SIZE: Coarse calibration step size: 0000 = 1/128. 0001 = 1/64. 0010 = 3/128. 0011 = 1/32. 0100 = 5/128. 0101 = 3/64. 0110 = 7/128. 0111 = 1/161. 1000 - 1111 = Reserved. When DIGITAL_EYE_EN is 1b in the DP16 DFT Digital Eye Register: bit 51:52: Reserved. bit 53: DIGEYE_16_NOT_1: 1 = A block of 16 BL8s is issued during each outer loop iteration of "digital eye." 0 = One BL8 read is issued during each outer loop iteration of "digital eye." bit 54: DIGEYE_REFRESH: 1 = Issues a precharge and refresh during every outer loop iteration of "digital eye." 0 = Issues a precharge and refresh at least once every 16 outer loop iterations of "digital eye."
55:56	RWX	DQ_SEL_QUAD: The quadrant within the DP16 being calibrated (read calibrations). Can also be set statically for "digital eye." This field must not be modified while the calibration is running. This field is part of a counter that automatically increments during some types of calibrations.
57:59	RWX	DQ_SEL_LANE: The data bit within the DP16 being calibrated (read calibrations). Can also be set statically for "digital eye." This field must not be modified while the calibration is running. This field is part of a counter that automatically increments during some types of calibrations.
60:63	RO	Constant = 0b0000

Register Name	RC Read VREF Configuration 0 Register
Mnemonic	IOM0.DDRPHY_RC_RDVREF_CONFIG0_P0
Address	8000C8090701103F (SCOM)
Description	This register controls the read VREF calibration logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	WAIT_TIME: This 16-bit integer denotes the number of memory clock cycles to wait for the analog D/A converter to settle to a value. The digital value in the D/A converter can change every 500 KHz, so the frequency of dphy_gckn divided by the number in this register must be less than 500 KHz. Due to changing state machine states happening during this period, it is recommended to ensure that the value used slightly exceeds the 500 KHz threshold. For example, a 1333 MHz clock must have a value that is slightly more than 1333 MHz / 500 KHz = 2,666 MT/s, rounded up to a final value of 2,700 MT/s. Set to ‘0B74’h for 2666 MT/s. Set to ‘0A50’h for 2400 MT/s. Set to ‘092A’h for 2133 MT/s. Set to ‘0804’h for 1866 MT/s.

Register Name	RC Read VREF Configuration 0 Register
Mnemonic	IOM0.DDRPHY_RC_RDVREF_CONFIG0_P1
Address	8000C8090701143F (SCOM)
Description	This register controls the read VREF calibration logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	WAIT_TIME: This 16-bit integer denotes the number of memory clock cycles to wait for the analog D/A converter to settle to a value. The digital value in the D/A converter can change every 500 KHz, so the frequency of dphy_gckn divided by the number in this register must be less than 500 KHz. Due to changing state machine states happening during this period, it is recommended to ensure that the value used slightly exceeds the 500 KHz threshold. For example, a 1333 MHz clock must have a value that is slightly more than 1333 MHz / 500 KHz = 2,666 MT/s, rounded up to a final value of 2,700 MT/s. Set to ‘0B74’h for 2666 MT/s. Set to ‘0A50’h for 2400 MT/s. Set to ‘092A’h for 2133 MT/s. Set to ‘0804’h for 1866 MT/s.

Register Name	RC Read VREF Configuration 0 Register
Mnemonic	IOM0.DDRPHY_RC_RDVREF_CONFIG0_P2
Address	8000C8090701183F (SCOM)
Description	This register controls the read VREF calibration logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	WAIT_TIME: This 16-bit integer denotes the number of memory clock cycles to wait for the analog D/A converter to settle to a value. The digital value in the D/A converter can change every 500 KHz, so the frequency of dphy_gckn divided by the number in this register must be less than 500 KHz. Due to changing state machine states happening during this period, it is recommended to ensure that the value used slightly exceeds the 500 KHz threshold. For example, a 1333 MHz clock must have a value that is slightly more than 1333 MHz / 500 KHz = 2,666 MT/s, rounded up to a final value of 2,700 MT/s. Set to ‘0B74’h for 2666 MT/s. Set to ‘0A50’h for 2400 MT/s. Set to ‘092A’h for 2133 MT/s. Set to ‘0804’h for 1866 MT/s.

Register Name	RC Read VREF Configuration 0 Register
Mnemonic	IOM0.DDRPHY_RC_RDVREF_CONFIG0_P3
Address	8000C80907011C3F (SCOM)
Description	This register controls the read VREF calibration logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	WAIT_TIME: This 16-bit integer denotes the number of memory clock cycles to wait for the analog D/A converter to settle to a value. The digital value in the D/A converter can change every 500 KHz, so the frequency of dphy_gckn divided by the number in this register must be less than 500 KHz. Due to changing state machine states happening during this period, it is recommended to ensure that the value used slightly exceeds the 500 KHz threshold. For example, a 1333 MHz clock must have a value that is slightly more than 1333 MHz / 500 KHz = 2,666 MT/s, rounded up to a final value of 2,700 MT/s. Set to '0B74'h for 2666 MT/s. Set to '0A50'h for 2400 MT/s. Set to '092A'h for 2133 MT/s. Set to '0804'h for 1866 MT/s.

Register Name	RC Read VREF Configuration 1 Register
Mnemonic	IOM0.DDRPHY_RC_RDVREF_CONFIG1_P0
Address	8000C80A0701103F (SCOM)
Description	This register controls the read VREF calibration logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:55	RW	CMD_PRECEDE_TIME: This 8-bit integer denotes the number of cycles the read command is sent to the memory before the D/A converter is sampled. The recommended setting is (Additive Latency + CAS Latency + 12).
56:59	RW	MPR_LOCATION: This field configures which MPR location holds all the MPR patterns used in read calibrations. Bits 56:57 are the location used in read VREF, and must be all zeros. Bits 58:59 are the location used in read centering, and must be alternating 1s and 0s.
60	RW	CALIBRATION_ENABLE: When 1, read VREF calibration is run before read centering. For this to have an effect, read centering must be enabled in the PC Initial Calibration Config0 Register. When 0, read VREF calibration is not run and the pre-existing values in the DP16 configuration registers are used as the VREF threshold.
61	RW	SKIP_RDCENTERING: When 1, when read VREF calibration is finished, the calibration algorithm inside the RC is immediately finished. Read centering does not run. This allows the user to only run the read VREF calibration step. When 0, the read-centering calibration algorithm is run after read VREF. Note that if CALIBRATION_ENABLE = 0, this bit has no effect and read centering runs as configured.
62:63	RO	Constant = 0b00

Register Name	RC Read VREF Configuration 1 Register
Mnemonic	IOM0.DDRPHY_RC_RDVREF_CONFIG1_P1
Address	8000C80A0701143F (SCOM)
Description	This register controls the read VREF calibration logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:55	RW	CMD_PRECEDE_TIME: This 8-bit integer denotes the number of cycles the read command is sent to the memory before the D/A converter is sampled. The recommended setting is (Additive Latency + CAS Latency + 12).

Bits	SCOM	Field Mnemonic: Description
56:59	RW	MPR_LOCATION: This field configures which MPR location holds all the MPR patterns used in read calibrations. Bits 56:57 are the location used in read VREF, and must be all zeros. Bits 58:59 are the location used in read centering, and must be alternating 1s and 0s.
60	RW	CALIBRATION_ENABLE: When 1, read VREF calibration is run before read centering. For this to have an effect, read centering must be enabled in the PC Initial Calibration Config0 Register. When 0, read VREF calibration is not run and the pre-existing values in the DP16 configuration registers are used as the VREF threshold.
61	RW	SKIP_RDCENTERING: When 1, when read VREF calibration is finished, the calibration algorithm inside the RC is immediately finished. Read centering does not run. This allows the user to only run the read VREF calibration step. When 0, the read-centering calibration algorithm is run after read VREF. Note that if CALIBRATION_ENABLE = 0, this bit has no effect and read centering runs as configured.
62:63	RO	Constant = 0b00

Register Name	RC Read VREF Configuration 1 Register
Mnemonic	IOM0.DDRPHY_RC_RDVREF_CONFIG1_P2
Address	8000C80A0701183F (SCOM)
Description	This register controls the read VREF calibration logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:55	RW	CMD_PRECEDE_TIME: This 8-bit integer denotes the number of cycles the read command is sent to the memory before the D/A converter is sampled. The recommended setting is (Additive Latency + CAS Latency + 12).
56:59	RW	MPR_LOCATION: This field configures which MPR location holds all the MPR patterns used in read calibrations. Bits 56:57 are the location used in read VREF, and must be all zeros. Bits 58:59 are the location used in read centering, and must be alternating 1s and 0s.
60	RW	CALIBRATION_ENABLE: When 1, read VREF calibration is run before read centering. For this to have an effect, read centering must be enabled in the PC Initial Calibration Config0 Register. When 0, read VREF calibration is not run and the pre-existing values in the DP16 configuration registers are used as the VREF threshold.
61	RW	SKIP_RDCENTERING: When 1, when read VREF calibration is finished, the calibration algorithm inside the RC is immediately finished. Read centering does not run. This allows the user to only run the read VREF calibration step. When 0, the read-centering calibration algorithm is run after read VREF. Note that if CALIBRATION_ENABLE = 0, this bit has no effect and read centering runs as configured.
62:63	RO	Constant = 0b00

Register Name	RC Read VREF Configuration 1 Register
Mnemonic	IOM0.DDRPHY_RC_RDVREF_CONFIG1_P3
Address	8000C80A07011C3F (SCOM)
Description	This register controls the read VREF calibration logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	CMD_PRECEDE_TIME: This 8-bit integer denotes the number of cycles the read command is sent to the memory before the D/A converter is sampled. The recommended setting is (Additive Latency + CAS Latency + 12).
56:59	RW	MPR_LOCATION: This field configures which MPR location holds all the MPR patterns used in read calibrations. Bits 56:57 are the location used in read VREF, and must be all zeros. Bits 58:59 are the location used in read centering, and must be alternating 1s and 0s.
60	RW	CALIBRATION_ENABLE: When 1, read VREF calibration is run before read centering. For this to have an effect, read centering must be enabled in the PC Initial Calibration Config0 Register. When 0, read VREF calibration is not run and the pre-existing values in the DP16 configuration registers are used as the VREF threshold.
61	RW	SKIP_RDCENTERING: When 1, when read VREF calibration is finished, the calibration algorithm inside the RC is immediately finished. Read centering does not run. This allows the user to only run the read VREF calibration step. When 0, the read-centering calibration algorithm is run after read VREF. Note that if CALIBRATION_ENABLE = 0, this bit has no effect and read centering runs as configured.
62:63	RO	Constant = 0b00

9. DDRPHY: SEQ Registers

Ths section contains the registers that are located in the sequencer (SEQ) logic. The SEQ registers are listed alphabetically by mnemonic in the following address table.

Mnemonic	Address	Page
IOM0.DDRPHY_SEQ_ODT_DEFAULT_CONFIG_P2	0x8000C4240701183F	945
IOM0.DDRPHY_SEQ_ODT_DEFAULT_CONFIG_P3	0x8000C42407011C3F	946
IOM0.DDRPHY_SEQ_ODT_RD_CONFIG0_P0	0x8000C40E0701103F	921
IOM0.DDRPHY_SEQ_ODT_RD_CONFIG0_P1	0x8000C40E0701143F	922
IOM0.DDRPHY_SEQ_ODT_RD_CONFIG0_P2	0x8000C40E0701183F	922
IOM0.DDRPHY_SEQ_ODT_RD_CONFIG0_P3	0x8000C40E07011C3F	922
IOM0.DDRPHY_SEQ_ODT_RD_CONFIG1_P0	0x8000C40F0701103F	923
IOM0.DDRPHY_SEQ_ODT_RD_CONFIG1_P1	0x8000C40F0701143F	923
IOM0.DDRPHY_SEQ_ODT_RD_CONFIG1_P2	0x8000C40F0701183F	924
IOM0.DDRPHY_SEQ_ODT_RD_CONFIG1_P3	0x8000C40F07011C3F	924
IOM0.DDRPHY_SEQ_ODT_WR_CONFIG0_P0	0x8000C40A0701103F	918
IOM0.DDRPHY_SEQ_ODT_WR_CONFIG0_P1	0x8000C40A0701143F	919
IOM0.DDRPHY_SEQ_ODT_WR_CONFIG0_P2	0x8000C40A0701183F	919
IOM0.DDRPHY_SEQ_ODT_WR_CONFIG0_P3	0x8000C40A07011C3F	920
IOM0.DDRPHY_SEQ_ODT_WR_CONFIG1_P0	0x8000C40B0701103F	920
IOM0.DDRPHY_SEQ_ODT_WR_CONFIG1_P1	0x8000C40B0701143F	920
IOM0.DDRPHY_SEQ_ODT_WR_CONFIG1_P2	0x8000C40B0701183F	921
IOM0.DDRPHY_SEQ_ODT_WR_CONFIG1_P3	0x8000C40B07011C3F	921
IOM0.DDRPHY_SEQ_RD_WR_DATA0_P0	0x8000C4000701103F	895
IOM0.DDRPHY_SEQ_RD_WR_DATA0_P1	0x8000C4000701143F	896
IOM0.DDRPHY_SEQ_RD_WR_DATA0_P2	0x8000C4000701183F	897
IOM0.DDRPHY_SEQ_RD_WR_DATA0_P3	0x8000C40007011C3F	897
IOM0.DDRPHY_SEQ_RD_WR_DATA1_P0	0x8000C4010701103F	898
IOM0.DDRPHY_SEQ_RD_WR_DATA1_P1	0x8000C4010701143F	899
IOM0.DDRPHY_SEQ_RD_WR_DATA1_P2	0x8000C4010701183F	899
IOM0.DDRPHY_SEQ_RD_WR_DATA1_P3	0x8000C40107011C3F	900
IOM0.DDRPHY_SEQ_RESERVED_ADDR0_P0	0x8000C4030701103F	906
IOM0.DDRPHY_SEQ_RESERVED_ADDR0_P1	0x8000C4030701143F	906
IOM0.DDRPHY_SEQ_RESERVED_ADDR0_P2	0x8000C4030701183F	907
IOM0.DDRPHY_SEQ_RESERVED_ADDR0_P3	0x8000C40307011C3F	907
IOM0.DDRPHY_SEQ_RESERVED_ADDR1_P0	0x8000C4040701103F	907
IOM0.DDRPHY_SEQ_RESERVED_ADDR1_P1	0x8000C4040701143F	908
IOM0.DDRPHY_SEQ_RESERVED_ADDR1_P2	0x8000C4040701183F	908
IOM0.DDRPHY_SEQ_RESERVED_ADDR1_P3	0x8000C40407011C3F	908
IOM0.DDRPHY_SEQ_RESERVED_ADDR2_P0	0x8000C4050701103F	908
IOM0.DDRPHY_SEQ_RESERVED_ADDR2_P1	0x8000C4050701143F	909
IOM0.DDRPHY_SEQ_RESERVED_ADDR2_P2	0x8000C4050701183F	910
IOM0.DDRPHY_SEQ_RESERVED_ADDR2_P3	0x8000C40507011C3F	911
IOM0.DDRPHY_SEQ_RESERVED_ADDR3_P0	0x8000C4060701103F	912
IOM0.DDRPHY_SEQ_RESERVED_ADDR3_P1	0x8000C4060701143F	912
IOM0.DDRPHY_SEQ_RESERVED_ADDR3_P2	0x8000C4060701183F	913
IOM0.DDRPHY_SEQ_RESERVED_ADDR3_P3	0x8000C40607011C3F	913
IOM0.DDRPHY_SEQ_RESERVED_ADDR4_P0	0x8000C4070701103F	913

The SEQ registers are listed in the following tables.

Register Name	**SEQ Read/Write Data 0 Register**
Mnemonic	IOM0.DDRPHY_SEQ_RD_WR_DATA0_P0
Address	8000C4000701103F (SCOM)
Description	The data in these registers is used to write the custom training pattern into a specified memory location during calibration operations. The data in these registers is also used as comparison data during calibration operations that perform a read operation that requires the incoming read data to be compared. This register must be programmed to the predefined pattern for protocols that provide a predefined pattern for read calibrations. For the most robust centering solution, custom patterns for data strobe (DQS) centering must have data transitions at all beats. Each bit lane can have a different pattern, but the composite pattern must have transitions at each beat. This register contains the test pattern that is wrapped through the address (ADR) and data path 16 (DP16) pins during a design for test (DFT) wrap test.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	RD_WR_DATA_REG0: These registers define the values written to memory modules during initial pattern write and custom write centering when CUSTOM_INIT_WRITE = 1. These registers also define the expected data used during custom read centering and custom write centering. Custom write centering always uses reserved memory and does not use multipurpose registers (MPRs). During initial pattern write when CUSTOM_INIT_WRITE equals 1b: Bits 48:55 of the SEQ Read/Write Data 0 Register are written to MPR0. Bits 56:63 of the SEQ Read/Write Data 0 Register are written to MPR1. Bits 48:55 of the SEQ Read/Write Data 1 Register are written to MPR2. Bits 56:63 of the SEQ Read/Write Data 1 Register are written to MPR3. During custom read centering and custom write centering: The READ_CENTERING_MODE field of the DP16 IO RX Configuration 0 Register is set to 11b for DDR4 custom read centering, and is set to 00b otherwise.

Register Name	SEQ Read/Write Data 0 Register
Mnemonic	IOM0.DDRPHY_SEQ_RD_WR_DATA0_P1
Address	8000C4000701143F (SCOM)
Description	The data in these registers is used to write the custom training pattern into a specified memory location during calibration operations. The data in these registers is also used as comparison data during calibration operations that perform a read operation that requires the incoming read data to be compared. This register must be programmed to the predefined pattern for protocols that provide a predefined pattern for read calibrations. For the most robust centering solution, custom patterns for DQS centering must have data transitions at all beats. Each bit lane can have a different pattern, but the composite pattern must have transitions at each beat. This register contains the test pattern that is wrapped through the ADR and DP16 pins during a DFT wrap test.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	RD_WR_DATA_REG0: These registers define the values written to memory modules during initial pattern write and custom write centering when CUSTOM_INIT_WRITE = 1. These registers also define the expected data used during custom read centering and custom write centering. Custom write centering always uses reserved memory and does not use MPR registers. During initial pattern write when CUSTOM_INIT_WRITE equals 1b: Bits 48:55 of the SEQ Read/Write Data 0 Register are written to MPR0. Bits 56:63 of the SEQ Read/Write Data 0 Register are written to MPR1. Bits 48:55 of the SEQ Read/Write Data 1 Register are written to MPR2. Bits 56:63 of the SEQ Read/Write Data 1 Register are written to MPR3. During custom read centering and custom write centering: The READ_CENTERING_MODE field of the DP16 IO RX Configuration 0 Register is set to 11b for DDR4 custom read centering, and is set to 00b otherwise.

Register Name	SEQ Read/Write Data 0 Register
Mnemonic	IOM0.DDRPHY_SEQ_RD_WR_DATA0_P2
Address	8000C4000701183F (SCOM)
Description	The data in these registers is used to write the custom training pattern into a specified memory location during calibration operations. The data in these registers is also used as comparison data during calibration operations that perform a read operation that requires the incoming read data to be compared. This register must be programmed to the predefined pattern for protocols that provide a predefined pattern for read calibrations. For the most robust centering solution, custom patterns for DQS centering must have data transitions at all beats. Each bit lane can have a different pattern, but the composite pattern must have transitions at each beat. This register contains the test pattern that is wrapped through the ADR and DP16 pins during a DFT wrap test.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	RD_WR_DATA_REG0: These registers define the values written to memory modules during initial pattern write and custom write centering when CUSTOM_INIT_WRITE = 1. These registers also define the expected data used during custom read centering and custom write centering. Custom write centering always uses reserved memory and does not use MPR registers. During initial pattern write when CUSTOM_INIT_WRITE equals 1b: Bits 48:55 of the SEQ Read/Write Data 0 Register are written to MPR0. Bits 56:63 of the SEQ Read/Write Data 0 Register are written to MPR1. Bits 48:55 of the SEQ Read/Write Data 1 Register are written to MPR2. Bits 56:63 of the SEQ Read/Write Data 1 Register are written to MPR3. During custom read centering and custom write centering: The READ_CENTERING_MODE field of the DP16 IO RX Configuration 0 Register is set to 11b for DDR4 custom read centering, and is set to 00b otherwise.

Register Name	SEQ Read/Write Data 0 Register
Mnemonic	IOM0.DDRPHY_SEQ_RD_WR_DATA0_P3
Address	8000C40007011C3F (SCOM)
Description	The data in these registers is used to write the custom training pattern into a specified memory location during calibration operations. The data in these registers is also used as comparison data during calibration operations that perform a read operation that requires the incoming read data to be compared. This register must be programmed to the predefined pattern for protocols that provide a predefined pattern for read calibrations. For the most robust centering solution, custom patterns for DQS centering must have data transitions at all beats. Each bit lane can have a different pattern, but the composite pattern must have transitions at each beat. This register contains the test pattern that is wrapped through the ADR and DP16 pins during a DFT wrap test.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	RD_WR_DATA_REG0: These registers define the values written to memory modules during initial pattern write and custom write centering when CUSTOM_INIT_WRITE = 1. These registers also define the expected data used during custom read centering and custom write centering. Custom write centering always uses reserved memory and does not use MPR registers. During initial pattern write when CUSTOM_INIT_WRITE equals 1b: Bits 48:55 of the SEQ Read/Write Data 0 Register are written to MPR0. Bits 56:63 of the SEQ Read/Write Data 0 Register are written to MPR1. Bits 48:55 of the SEQ Read/Write Data 1 Register are written to MPR2. Bits 56:63 of the SEQ Read/Write Data 1 Register are written to MPR3. During custom read centering and custom write centering: The READ_CENTERING_MODE field of the DP16 IO RX Configuration 0 Register is set to 11b for DDR4 custom read centering, and is set to 00b otherwise.

Register Name	SEQ Read/Write Data 1 Register
Mnemonic	IOM0.DDRPHY_SEQ_RD_WR_DATA1_P0
Address	8000C4010701103F (SCOM)
Description	The data in these registers is used to write the custom training pattern into a specified memory location during calibration operations. The data in these registers is also used as comparison data during calibration operations that perform a read operation that requires the incoming read data to be compared. This register must be programmed to the predefined pattern for protocols that provide a predefined pattern for read calibrations. For the most robust centering solution, custom patterns for DQS centering must have data transitions at all beats. Each bit lane can have a different pattern, but the composite pattern must have transitions at each beat. This register contains the test pattern that is wrapped through the ADR and DP16 pins during a DFT wrap test.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	RD_WR_DATA_REG1: These registers define the values written to memory modules during initial pattern write and custom write centering when CUSTOM_INIT_WRITE = 1. These registers also define the expected data used during custom read centering and custom write centering. Custom write centering always uses reserved memory and does not use MPR registers. During initial pattern write when CUSTOM_INIT_WRITE equals 1b: Bits 48:55 of the SEQ Read/Write Data 0 Register are written to MPR0. Bits 56:63 of the SEQ Read/Write Data 0 Register are written to MPR1. Bits 48:55 of the SEQ Read/Write Data 1 Register are written to MPR2. Bits 56:63 of the SEQ Read/Write Data 1 Register are written to MPR3. During custom read centering and custom write centering: The READ_CENTERING_MODE field of the DP16 IO RX Configuration 0 Register is set to 11b for DDR4 custom read centering, and is set to 00b otherwise.

Register Name	SEQ Read/Write Data 1 Register
Mnemonic	IOM0.DDRPHY_SEQ_RD_WR_DATA1_P1
Address	8000C4010701143F (SCOM)
Description	The data in these registers is used to write the custom training pattern into a specified memory location during calibration operations. The data in these registers is also used as comparison data during calibration operations that perform a read operation that requires the incoming read data to be compared. This register must be programmed to the predefined pattern for protocols that provide a predefined pattern for read calibrations. For the most robust centering solution, custom patterns for DQS centering must have data transitions at all beats. Each bit lane can have a different pattern, but the composite pattern must have transitions at each beat. This register contains the test pattern that is wrapped through the ADR and DP16 pins during a DFT wrap test.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	RD_WR_DATA_REG1: These registers define the values written to memory modules during initial pattern write and custom write centering when CUSTOM_INIT_WRITE = 1. These registers also define the expected data used during custom read centering and custom write centering. Custom write centering always uses reserved memory and does not use MPR registers. During initial pattern write when CUSTOM_INIT_WRITE equals 1b: Bits 48:55 of the SEQ Read/Write Data 0 Register are written to MPR0. Bits 56:63 of the SEQ Read/Write Data 0 Register are written to MPR1. Bits 48:55 of the SEQ Read/Write Data 1 Register are written to MPR2. Bits 56:63 of the SEQ Read/Write Data 1 Register are written to MPR3. During custom read centering and custom write centering: The READ_CENTERING_MODE field of the DP16 IO RX Configuration 0 Register is set to 11b for DDR4 custom read centering, and is set to 00b otherwise.

Register Name	SEQ Read/Write Data 1 Register
Mnemonic	IOM0.DDRPHY_SEQ_RD_WR_DATA1_P2
Address	8000C4010701183F (SCOM)
Description	The data in these registers is used to write the custom training pattern into a specified memory location during calibration operations. The data in these registers is also used as comparison data during calibration operations that perform a read operation that requires the incoming read data to be compared. This register must be programmed to the predefined pattern for protocols that provide a predefined pattern for read calibrations. For the most robust centering solution, custom patterns for DQS centering must have data transitions at all beats. Each bit lane can have a different pattern, but the composite pattern must have transitions at each beat. This register contains the test pattern that is wrapped through the ADR and DP16 pins during a DFT wrap test.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	RD_WR_DATA_REG1: These registers define the values written to memory modules during initial pattern write and custom write centering when CUSTOM_INIT_WRITE = 1. These registers also define the expected data used during custom read centering and custom write centering. During initial pattern write when CUSTOM_INIT_WRITE equals 1b: Bits 48:55 of the SEQ Read/Write Data 0 Register are written to MPR0. Bits 56:63 of the SEQ Read/Write Data 0 Register are written to MPR1. Bits 48:55 of the SEQ Read/Write Data 1 Register are written to MPR2. Bits 56:63 of the SEQ Read/Write Data 1 Register are written to MPR3. During custom read centering and custom write centering: The READ_CENTERING_MODE field of the DP16 IO RX Configuration 0 Register is set to 11b for DDR4 custom read centering, and is set to 00b otherwise.

Register Name	SEQ Read/Write Data 1 Register
Mnemonic	IOM0.DDRPHY_SEQ_RD_WR_DATA1_P3
Address	8000C40107011C3F (SCOM)
Description	The data in these registers is used to write the custom training pattern into a specified memory location during calibration operations. The data in these registers is also used as comparison data during calibration operations that perform a read operation that requires the incoming read data to be compared. This register must be programmed to the predefined pattern for protocols that provide a predefined pattern for read calibrations. For the most robust centering solution, custom patterns for DQS centering must have data transitions at all beats. Each bit lane can have a different pattern, but the composite pattern must have transitions at each beat. This register contains the test pattern that is wrapped through the ADR and DP16 pins during a DFT wrap test.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	RD_WR_DATA_REG1: These registers define the values written to memory modules during initial pattern write and custom write centering when CUSTOM_INIT_WRITE = 1. These registers also define the expected data used during custom read centering and custom write centering. During initial pattern write when CUSTOM_INIT_WRITE equals 1b: Bits 48:55 of the SEQ Read/Write Data 0 Register are written to MPR0. Bits 56:63 of the SEQ Read/Write Data 0 Register are written to MPR1. Bits 48:55 of the SEQ Read/Write Data 1 Register are written to MPR2. Bits 56:63 of the SEQ Read/Write Data 1 Register are written to MPR3. During custom read centering and custom write centering: The READ_CENTERING_MODE field of the DP16 IO RX Configuration 0 Register is set to 11b for DDR4 custom read centering, and is set to 00b otherwise.

Register Name	SEQ Configuration 0 Register
Mnemonic	IOM0.DDRPHY_SEQ_CONFIG0_P0
Address	8000C4020701103F (SCOM)
Description	This register contains the configuration settings for the sequencer (SEQ) logic block.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RW	MPR_PATTERN_BIT: Read and write calibration algorithms are based on 8-beat bursts. This register controls the read/write burst data pattern. For write data: The MPR_PATTERN_BIT value is available on all bit lanes of beats 1, 3, 5, and 7, and the inverse of the MPR_PATTERN_BIT on all bit lanes of beats 2, 4, 6, and 8. This ensures that all bit lanes toggle consecutive beats. If the protocol requires a burst length longer than eight beats, the pattern in this register is repeated until all data beats are defined. For read data: Bit 48 is brought out as output of the sequencer, and DP16 composes the expected pattern from this output.
49	RW	TWO_CYCLE_ADDR_EN: 1 = During calibrations, the address and command are driven onto the address/cmd bus for two memory clock cycles, while the appropriate chip selects are active only during the second memory clock cycle of the command. 0 = During calibration, the address and command and chip selects are driven and active for one memory clock cycle.
50:53	RW	MR_MASK_EN: PC Mode Register mask enable. This register masks, or disables, the PC Mode Register access by the calibration algorithms. Bits 50 - 53 map to PC Mode Registers 0 - 3.
54	RW	DELAYED_PAR: 1 = During calibration algorithms, the parity bit is driven one cycle after the command is driven on the memory command bus. 0 = During calibration algorithms, the parity bit is driven the same cycle the command is driven on the memory command bus.
55	RW	LRDIMM_CONTEXT: The value of the context bit to be used during F[0]RC12 LRDIMM control word commands.
56	RW	FORCE_RESERVED: 0 = When the PROTOCOL field in the PC Configuration 0 Register equals DDR4, custom read centering and the initial pattern write use the DDR4 MPR registers. 1 = When the PROTOCOL field in the PC Configuration 0 Register equals DDR4, custom read centering and the initial pattern write use the reserved location in memory. If the PROTOCOL field in the PC Configuration 0 Register does not equal DDR4, this bit is not used and is a don't care.
57	RW	HALT_ROTATION: 0 = When the PROTOCOL field in the PC Configuration 0 Register equals DDR4, custom read centering and the initial pattern write rotate through the use of all four MPR registers by changing BA[0:1] during the calibration. 1 = When the PROTOCOL field in the PC Configuration 0 Register equals DDR4, custom read centering and the initial pattern write set BA[0:1] = 00b. The same 8 beats are read repeatedly on a particular DQ lane. The expected data is not rotated through the 4 bytes of the SEQ Read/Write Data {0-1} Register every 8 beats. If the PROTOCOL field in the PC Configuration 0 Register does not equal DDR4, this bit is not used and is a don't care. If this bit is 1b, STAGGERED_PATTERN must be 0b in the RC Configuration 0 Register.
58:59	RW	Reserved.
60	RW	PAR_INVERT: 0 = Normal operation. 1 = For DDR4 registered dual in-line memory module (RDIMM) systems where CID2:0 has been configured to a nonzero value for calibrations, set this bit to the value of CID2 XOR CID1 XOR CID0.
61	RW	IPW_SIDEAB_SEL: 0 = Initial pattern write (IPW) is performed to MPRs on side A DRAMs. 1 = IPW is performed to MPRs on side B DRAMs. (This bit is only used in DDR4 when the MEMORY_TYPE field in the PC Configuration 1 Register equals 1XXX.)
62	RW	PAR_A17_MASK: 0 = The A17 bit is used to generate parity. 1 = The A17 bit is excluded from parity generation. This bit is used for DDR4 only.

Bits	SCOM	Field Mnemonic: Description
63	RW	CW_MIRROR: 0 = Address mirroring is not applied to LRDIMM control words. 1 = Address mirroring is applied to LRDIMM control words if enabled for the rank.

Register Name	SEQ Configuration 0 Register
Mnemonic	IOM0.DDRPHY_SEQ_CONFIG0_P1
Address	8000C4020701143F (SCOM)
Description	This register contains the configuration settings for the SEQ logic block.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	MPR_PATTERN_BIT: Read and write calibration algorithms are based on 8-beat bursts. This register controls the read/write burst data pattern. For write data: The MPR_PATTERN_BIT value is available on all bit lanes of beats 1, 3, 5, and 7, and the inverse of the MPR_PATTERN_BIT on all bit lanes of beats 2, 4, 6, and 8. This ensures that all bit lanes toggle consecutive beats. If the protocol requires a burst length longer than eight beats, the pattern in this register is repeated until all data beats are defined. For read data: Bit 48 is brought out as output of the sequencer, and DP16 composes the expected pattern from this output.
49	RW	TWO_CYCLE_ADDR_EN: 1 = During calibrations, the address and command are driven onto the address/cmd bus for two memory clock cycles, while the appropriate chip selects are active only during the second memory clock cycle of the command. 0 = During calibration, the address and command and chip selects are driven and active for one memory clock cycle.
50:53	RW	MR_MASK_EN: PC Mode Register mask enable. This register masks, or disables, the PC Mode Register access by the calibration algorithms. Bits 50 - 53 map to PC Mode Registers 0 - 3.
54	RW	DELAYED_PAR: 1 = During calibration algorithms, the parity bit is driven one cycle after the command is driven on the memory command bus. 0 = During calibration algorithms, the parity bit is driven the same cycle the command is driven on the memory command bus.
55	RW	LRDIMM_CONTEXT: The value of the context bit to be used during F[0]RC12 LRDIMM control word commands.
56	RW	FORCE_RESERVED: 0 = When the PROTOCOL field in the PC Configuration 0 Register equals DDR4, custom read centering and the initial pattern write use the DDR4 MPR registers. 1 = When the PROTOCOL field in the PC Configuration 0 Register equals DDR4, custom read centering and the initial pattern write use the reserved location in memory. If the PROTOCOL field in the PC Configuration 0 Register does not equal DDR4, this bit is not used and is a don't care.

Bits	SCOM	Field Mnemonic: Description
57	RW	HALT_ROTATION: 0 = When the PROTOCOL field in the PC Configuration 0 Register equals DDR4, custom read centering and the initial pattern write rotate through the use of all four MPR registers by changing BA[0:1] during the calibration. 1 = When the PROTOCOL field in the PC Configuration 0 Register equals DDR4, custom read centering and the initial pattern write set BA[0:1] = 00b. The same 8 beats are read repeatedly on a particular DQ lane. The expected data is not rotated through the 4 bytes of the SEQ Read/Write Data {0-1} Register every 8 beats. If the PROTOCOL field in the PC Configuration 0 Register does not equal DDR4, this bit is not used and is a don't care. If this bit is 1b, STAGGERED_PATTERN must be 0b in the RC Configuration 0 Register.
58:59	RW	Reserved.
60	RW	PAR_INVERT: 0 = Normal operation. 1 = For DDR4 RDIMM systems where CID2:0 has been configured to a nonzero value for calibrations, set this bit to the value of CID2 XOR CID1 XOR CID0.
61	RW	IPW_SIDEAB_SEL: 0 = IPW is performed to MPRs on side A DRAMs. 1 = IPW is performed to MPRs on side B DRAMs. (This bit is only used in DDR4 when the MEMORY_TYPE field in the PC Configuration 1 Register equals 1XXX.)
62	RW	PAR_A17_MASK: 0 = The A17 bit is used to generate parity. 1 = The A17 bit is excluded from parity generation. This bit is used for DDR4 only.
63	RW	CW_MIRROR: 0 = Address mirroring is not applied to LRDIMM control words. 1 = Address mirroring is applied to LRDIMM control words if enabled for the rank.

Register Name	SEQ Configuration 0 Register
Mnemonic	IOM0.DDRPHY_SEQ_CONFIG0_P2
Address	8000C4020701183F (SCOM)
Description	This register contains the configuration settings for the SEQ logic block.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	MPR_PATTERN_BIT: Read and write calibration algorithms are based on 8-beat bursts. This register controls the read/write burst data pattern. For write data: The MPR_PATTERN_BIT value is available on all bit lanes of beats 1, 3, 5, and 7, and the inverse of the MPR_PATTERN_BIT on all bit lanes of beats 2, 4, 6, and 8. This ensures that all bit lanes toggle consecutive beats. If the protocol requires a burst length longer than eight beats, the pattern in this register is repeated until all data beats are defined. For read data: Bit 48 is brought out as output of the sequencer, and DP16 composes the expected pattern from this output.
49	RW	TWO_CYCLE_ADDR_EN: 1 = During calibrations, the address and command are driven onto the address/cmd bus for two memory clock cycles, while the appropriate chip selects are active only during the second memory clock cycle of the command. 0 = During calibration, the address and command and chip selects are driven and active for one memory clock cycle.
50:53	RW	MR_MASK_EN: PC Mode Register mask enable. This register masks, or disables, the PC Mode Register access by the calibration algorithms. Bits 50 - 53 map to PC Mode Registers 0 - 3.

Bits	SCOM	Field Mnemonic: Description
54	RW	DELAYED_PAR: 1 = During calibration algorithms, the parity bit is driven one cycle after the command is driven on the memory command bus. 0 = During calibration algorithms, the parity bit is driven the same cycle the command is driven on the memory command bus.
55	RW	LRDIMM_CONTEXT: The value of the context bit to be used during F[0]RC12 LRDIMM control word commands.
56	RW	FORCE_RESERVED: 0 = When the PROTOCOL field in the PC Configuration 0 Register equals DDR4, custom read centering and the initial pattern write use the DDR4 MPR registers. 1 = When the PROTOCOL field in the PC Configuration 0 Register equals DDR4, custom read centering and the initial pattern write use the reserved location in memory. If the PROTOCOL field in the PC Configuration 0 Register does not equal DDR4, this bit is not used and is a don't care.
57	RW	HALT_ROTATION: 0 = When the PROTOCOL field in the PC Configuration 0 Register equals DDR4, custom read centering and the initial pattern write rotate through the use of all four MPR registers by changing BA[0:1] during the calibration. 1 = When the PROTOCOL field in the PC Configuration 0 Register equals DDR4, custom read centering and the initial pattern write set BA[0:1] = 00b. The same 8 beats are read repeatedly on a particular DQ lane. The expected data is not rotated through the 4 bytes of the SEQ Read/Write Data {0-1} Register every 8 beats. If the PROTOCOL field in the PC Configuration 0 Register does not equal DDR4, this bit is not used and is a don't care. If this bit is 1b, STAGGERED_PATTERN must be 0b in the RC Configuration 0 Register.
58:59	RW	Reserved.
60	RW	PAR_INVERT: 0 = Normal operation. 1 = For DDR4 RDIMM systems where CID2:0 has been configured to a nonzero value for calibrations, set this bit to the value of CID2 XOR CID1 XOR CID0.
61	RW	IPW_SIDEAB_SEL: 0 = IPW is performed to MPRs on side A DRAMs. 1 = IPW is performed to MPRs on side B DRAMs. (This bit is only used in DDR4 when the MEMORY_TYPE field in the PC Configuration 1 Register equals 1XXX.)
62	RW	PAR_A17_MASK: 0 = The A17 bit is used to generate parity. 1 = The A17 bit is excluded from parity generation. This bit is used for DDR4 only.
63	RW	CW_MIRROR: 0 = Address mirroring is not applied to LRDIMM control words. 1 = Address mirroring is applied to LRDIMM control words if enabled for the rank.

Register Name	SEQ Configuration 0 Register
Mnemonic	IOM0.DDRPHY_SEQ_CONFIG0_P3
Address	8000C40207011C3F (SCOM)
Description	This register contains the configuration settings for the SEQ logic block.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RW	MPR_PATTERN_BIT: Read and write calibration algorithms are based on 8-beat bursts. This register controls the read/write burst data pattern. For write data: The MPR_PATTERN_BIT value is available on all bit lanes of beats 1, 3, 5, and 7, and the inverse of the MPR_PATTERN_BIT on all bit lanes of beats 2, 4, 6, and 8. This ensures that all bit lanes toggle consecutive beats. If the protocol requires a burst length longer than eight beats, the pattern in this register is repeated until all data beats are defined. For read data: Bit 48 is brought out as output of the sequencer, and DP16 composes the expected pattern from this output.
49	RW	TWO_CYCLE_ADDR_EN: 1 = During calibrations, the address and command are driven onto the address/cmd bus for two memory clock cycles, while the appropriate chip selects are active only during the second memory clock cycle of the command. 0 = During calibration, the address and command and chip selects are driven and active for one memory clock cycle.
50:53	RW	MR_MASK_EN: PC Mode Register mask enable. This register masks, or disables, the PC Mode Register access by the calibration algorithms. Bits 50 - 53 map to PC Mode Registers 0 - 3.
54	RW	DELAYED_PAR: 1 = During calibration algorithms, the parity bit is driven one cycle after the command is driven on the memory command bus. 0 = During calibration algorithms, the parity bit is driven the same cycle the command is driven on the memory command bus.
55	RW	LRDIMM_CONTEXT: The value of the context bit to be used during F[0]RC12 LRDIMM control word commands.
56	RW	FORCE_RESERVED: 0 = When the PROTOCOL field in the PC Configuration 0 Register equals DDR4, custom read centering and the initial pattern write use the DDR4 MPR registers. 1 = When the PROTOCOL field in the PC Configuration 0 Register equals DDR4, custom read centering and the initial pattern write use the reserved location in memory. If the PROTOCOL field in the PC Configuration 0 Register does not equal DDR4, this bit is not used and is a don't care.
57	RW	HALT_ROTATION: 0 = When the PROTOCOL field in the PC Configuration 0 Register equals DDR4, custom read centering and the initial pattern write rotate through the use of all four MPR registers by changing BA[0:1] during the calibration. 1 = When the PROTOCOL field in the PC Configuration 0 Register equals DDR4, custom read centering and the initial pattern write set BA[0:1] = 00b. The same 8 beats are read repeatedly on a particular DQ lane. The expected data is not rotated through the 4 bytes of the SEQ Read/Write Data {0-1} Register every 8 beats. If the PROTOCOL field in the PC Configuration 0 Register does not equal DDR4, this bit is not used and is a don't care. If this bit is 1b, STAGGERED_PATTERN must be 0b in the RC Configuration 0 Register.
58:59	RW	Reserved.
60	RW	PAR_INVERT: 0 = Normal operation. 1 = For DDR4 RDIMM systems where CID2:0 has been configured to a nonzero value for calibrations, set this bit to the value of CID2 XOR CID1 XOR CID0.
61	RW	IPW_SIDEAB_SEL: 0 = IPW is performed to MPRs on side A DRAMs. 1 = IPW is performed to MPRs on side B DRAMs. (This bit is only used in DDR4 when the MEMORY_TYPE field in the PC Configuration 1 Register equals 1XXX.)
62	RW	PAR_A17_MASK: 0 = The A17 bit is used to generate parity. 1 = The A17 bit is excluded from parity generation. This bit is used for DDR4 only.

Bits	SCOM	Field Mnemonic: Description
63	RW	CW_MIRROR: 0 = Address mirroring is not applied to LRDIMM control words. 1 = Address mirroring is applied to LRDIMM control words if enabled for the rank.

Register Name	SEQ Reserved Address 0 Register
Mnemonic	IOM0.DDRPHY_SEQ_RESERVED_ADDR0_P0
Address	8000C4030701103F (SCOM)
Description	This register contains the reserved address to be used during calibration algorithms in the memory devices. This address is used within all primary ranks of rank pairs. Each read or write access by the DDR PHY during calibration algorithms receives or sends eight beats of data, starting at the address defined by the SEQ Reserved Address Registers. Bank addressing: For a single read or write command, the bank address is defined by the SEQ Reserved Address Registers. For a series of multiple back-to-back read or write commands, the first read or write is to the bank address defined by the SEQ Reserved Address Registers. The bank address is incremented by 1 for each subsequent read or write command.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	RESERVED_ADDR0: Reserved address field 0. Bits 48 - 63 map to A0 - A15. The lower 2 bytes of the row address are used. **Note:** A7:A0 must be less than or equal to ‘F8’h. Therefore, if bits 51:55 = ‘11111’b, bits 48:50 must be ‘000’b.

Register Name	SEQ Reserved Address 0 Register
Mnemonic	IOM0.DDRPHY_SEQ_RESERVED_ADDR0_P1
Address	8000C4030701143F (SCOM)
Description	This register contains the reserved address to be used during calibration algorithms in the memory devices. This address is used within all primary ranks of rank pairs. Each read or write access by the DDR PHY during calibration algorithms receives or sends eight beats of data, starting at the address defined by the SEQ Reserved Address Registers. Bank addressing: For a single read or write command, the bank address is defined by the SEQ Reserved Address Registers. For a series of multiple back-to-back read or write commands, the first read or write is to the bank address defined by the SEQ Reserved Address Registers. The bank address is incremented by 1 for each subsequent read or write command.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	RESERVED_ADDR0: Reserved address field 0. Bits 48 - 63 map to A0 - A15. The lower 2 bytes of the row address are used. **Note:** A7:A0 must be less than or equal to ‘F8’h. Therefore, if bits 51:55 = ‘11111’b, bits 48:50 must be ‘000’b.

Register Name	SEQ Reserved Address 0 Register
Mnemonic	IOM0.DDRPHY_SEQ_RESERVED_ADDR0_P2
Address	8000C4030701183F (SCOM)
Description	This register contains the reserved address to be used during calibration algorithms in the memory devices. This address is used within all primary ranks of rank pairs. Each read or write access by the DDR PHY during calibration algorithms receives or sends eight beats of data, starting at the address defined by the SEQ Reserved Address Registers. Bank addressing: For a single read or write command, the bank address is defined by the SEQ Reserved Address Registers. For a series of multiple back-to-back read or write commands, the first read or write is to the bank address defined by the SEQ Reserved Address Registers. The bank address is incremented by 1 for each subsequent read or write command.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	RESERVED_ADDR0: Reserved address field 0. Bits 48 - 63 map to A0 - A15. The lower 2 bytes of the row address are used. **Note:** A7:A0 must be less than or equal to ‘F8’h. Therefore, if bits 51:55 = ‘11111’b, bits 48:50 must be ‘000’b.

Register Name	SEQ Reserved Address 0 Register
Mnemonic	IOM0.DDRPHY_SEQ_RESERVED_ADDR0_P3
Address	8000C40307011C3F (SCOM)
Description	This register contains the reserved address to be used during calibration algorithms in the memory devices. This address is used within all primary ranks of rank pairs. Each read or write access by the DDR PHY during calibration algorithms receives or sends eight beats of data, starting at the address defined by the SEQ Reserved Address Registers. Bank addressing: For a single read or write command, the bank address is defined by the SEQ Reserved Address Registers. For a series of multiple back-to-back read or write commands, the first read or write is to the bank address defined by the SEQ Reserved Address Registers. The bank address is incremented by 1 for each subsequent read or write command.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	RESERVED_ADDR0: Reserved address field 0. Bits 48 - 63 map to A0 - A15. The lower 2 bytes of the row address are used. **Note:** A7:A0 must be less than or equal to ‘F8’h. Therefore, if bits 51:55 = ‘11111’b, bits 48:50 must be ‘000’b.

Register Name	SEQ Reserved Address 1 Register
Mnemonic	IOM0.DDRPHY_SEQ_RESERVED_ADDR1_P0
Address	8000C4040701103F (SCOM)
Description	This register contains the reserved address to be used during calibration algorithms in the memory devices. This address is used within all primary ranks of rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	RESERVED_ADDR1: Reserved address field 1. Bits 48 - 52 map to A16 - A20; bits 53 - 63 are reserved. This protocol uses the upper bit of the row address.

Register Name	SEQ Reserved Address 1 Register
Mnemonic	IOM0.DDRPHY_SEQ_RESERVED_ADDR1_P1
Address	8000C4040701143F (SCOM)
Description	This register contains the reserved address to be used during calibration algorithms in the memory devices. This address is used within all primary ranks of rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	RESERVED_ADDR1: Reserved address field 1. Bits 48 - 52 map to A16 - A20; bits 53 - 63 are reserved. This protocol uses the upper bit of the row address.

Register Name	SEQ Reserved Address 1 Register
Mnemonic	IOM0.DDRPHY_SEQ_RESERVED_ADDR1_P2
Address	8000C4040701183F (SCOM)
Description	This register contains the reserved address to be used during calibration algorithms in the memory devices. This address is used within all primary ranks of rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	RESERVED_ADDR1: Reserved address field 1. Bits 48 - 52 map to A16 - A20; bits 53 - 63 are reserved. This protocol uses the upper bit of the row address.

Register Name	SEQ Reserved Address 1 Register
Mnemonic	IOM0.DDRPHY_SEQ_RESERVED_ADDR1_P3
Address	8000C40407011C3F (SCOM)
Description	This register contains the reserved address to be used during calibration algorithms in the memory devices. This address is used within all primary ranks of rank pairs.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	RESERVED_ADDR1: Reserved address field 1. Bits 48 - 52 map to A16 - A20; bits 53 - 63 are reserved. This protocol uses the upper bit of the row address.

Register Name	SEQ Reserved Address 2 Register
Mnemonic	IOM0.DDRPHY_SEQ_RESERVED_ADDR2_P0
Address	8000C4050701103F (SCOM)
Description	This register contains the reserved address to be used during calibration algorithms in the memory devices. This address is used within all primary ranks of rank pairs. Address mirroring, if enabled, does not alter the address bit mapping of this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	RESERVED_ADDR2: Reserved address field 2. This register controls the lower 2 bytes of the column address. Some address pins depend upon the value of DDR4_CMD_SIG_REDUCTION in the PC Configuration 0 Register. Writes with DDR4_CMD_SIG_REDUCTION = 1b: A15 (CAS_n) = 0b. A14 (WE_n) = 0b (for write). A13 = bit 61. A12 (BL8) = 1b. A11 = bit 59. A10 (AP) = 0b. A0:A9 = bits 48:57. Reads with DDR4_CMD_SIG_REDUCTION = 1b: A15 (CAS_n) = 0b. A14 (WE_n) = 1b (for read). A13 = bit 61. A12 (BL8) = 1b. A11 = bit 59. A10 (AP) = 0b. A3:A9 = bits 51:57. A0:A2 = 000b. Refresh: A11:A15 = bits 59:63. A10 (AP) = 1b. A0:A9 = bits 48:57.

Register Name	SEQ Reserved Address 2 Register
Mnemonic	IOM0.DDRPHY_SEQ_RESERVED_ADDR2_P1
Address	8000C4050701143F (SCOM)
Description	This register contains the reserved address to be used during calibration algorithms in the memory devices. This address is used within all primary ranks of rank pairs. Address mirroring, if enabled, does not alter the address bit mapping of this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	RESERVED_ADDR2: Reserved address field 2. This register controls the lower 2 bytes of the column address. Some address pins depend upon the value of DDR4_CMD_SIG_REDUCTION in the PC Configuration 0 Register. Writes with DDR4_CMD_SIG_REDUCTION = 1b: A15 (CAS_n) = 0b. A14 (WE_n) = 0b (for write). A13 = bit 61. A12 (BL8) = 1b. A11 = bit 59. A10 (AP) = 0b. A0:A9 = bits 48:57. Reads with DDR4_CMD_SIG_REDUCTION = 1b: A15 (CAS_n) = 0b. A14 (WE_n) = 1b (for read). A13 = bit 61. A12 (BL8) = 1b. A11 = bit 59. A10 (AP) = 0b. A3:A9 = bits 51:57. A0:A2 = 000b. Refresh: A11:A15 = bits 59:63. A10 (AP) = 1b. A0:A9 = bits 48:57.

Register Name	SEQ Reserved Address 2 Register
Mnemonic	IOM0.DDRPHY_SEQ_RESERVED_ADDR2_P2
Address	8000C4050701183F (SCOM)
Description	This register contains the reserved address to be used during calibration algorithms in the memory devices. This address is used within all primary ranks of rank pairs. Address mirroring, if enabled, does not alter the address bit mapping of this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	RESERVED_ADDR2: Reserved address field 2. This register controls the lower 2 bytes of the column address. Some address pins depend upon the value of DDR4_CMD_SIG_REDUCTION in the PC Configuration 0 Register. Writes with DDR4_CMD_SIG_REDUCTION = 1b: A15 (CAS_n) = 0b. A14 (WE_n) = 0b (for write). A13 = bit 61. A12 (BL8) = 1b. A11 = bit 59. A10 (AP) = 0b. A0:A9 = bits 48:57. Reads with DDR4_CMD_SIG_REDUCTION = 1b: A15 (CAS_n) = 0b. A14 (WE_n) = 1b (for read). A13 = bit 61. A12 (BL8) = 1b. A11 = bit 59. A10 (AP) = 0b. A3:A9 = bits 51:57. A0:A2 = 000b. Refresh: A11:A15 = bits 59:63. A10 (AP) = 1b. A0:A9 = bits 48:57.

Register Name	SEQ Reserved Address 2 Register
Mnemonic	IOM0.DDRPHY_SEQ_RESERVED_ADDR2_P3
Address	8000C40507011C3F (SCOM)
Description	This register contains the reserved address to be used during calibration algorithms in the memory devices. This address is used within all primary ranks of rank pairs. Address mirroring, if enabled, does not alter the address bit mapping of this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	RESERVED_ADDR2: Reserved address field 2. This register controls the lower 2 bytes of the column address. Some address pins depend upon the value of DDR4_CMD_SIG_REDUCTION in the PC Configuration 0 Register. Writes with DDR4_CMD_SIG_REDUCTION = 1b: A15 (CAS_n) = 0b. A14 (WE_n) = 0b (for write). A13 = bit 61. A12 (BL8) = 1b. A11 = bit 59. A10 (AP) = 0b. A0:A9 = bits 48:57. Reads with DDR4_CMD_SIG_REDUCTION = 1b: A15 (CAS_n) = 0b. A14 (WE_n) = 1b (for read). A13 = bit 61. A12 (BL8) = 1b. A11 = bit 59. A10 (AP) = 0b. A3:A9 = bits 51:57. A0:A2 = 000b. Refresh: A11:A15 = bits 59:63. A10 (AP) = 1b. A0:A9 = bits 48:57.

Register Name	SEQ Reserved Address 3 Register
Mnemonic	IOM0.DDRPHY_SEQ_RESERVED_ADDR3_P0
Address	8000C4060701103F (SCOM)
Description	This register contains the reserved address to be used during calibration algorithms in the memory devices. This address is used within all primary ranks of rank pairs. Address mirroring, if enabled, does not alter the address bit mapping of this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	RESERVED_ADDR3: Reserved address field 3.

Register Name	SEQ Reserved Address 3 Register
Mnemonic	IOM0.DDRPHY_SEQ_RESERVED_ADDR3_P1
Address	8000C4060701143F (SCOM)
Description	This register contains the reserved address to be used during calibration algorithms in the memory devices. This address is used within all primary ranks of rank pairs. Address mirroring, if enabled, does not alter the address bit mapping of this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	RESERVED_ADDR3: Reserved address field 3.

Register Name	SEQ Reserved Address 3 Register
Mnemonic	IOM0.DDRPHY_SEQ_RESERVED_ADDR3_P2
Address	8000C4060701183F (SCOM)
Description	This register contains the reserved address to be used during calibration algorithms in the memory devices. This address is used within all primary ranks of rank pairs. Address mirroring, if enabled, does not alter the address bit mapping of this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	RESERVED_ADDR3: Reserved address field 3.

Register Name	SEQ Reserved Address 3 Register
Mnemonic	IOM0.DDRPHY_SEQ_RESERVED_ADDR3_P3
Address	8000C40607011C3F (SCOM)
Description	This register contains the reserved address to be used during calibration algorithms in the memory devices. This address is used within all primary ranks of rank pairs. Address mirroring, if enabled, does not alter the address bit mapping of this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	RESERVED_ADDR3: Reserved address field 3.

Register Name	SEQ Reserved Address 4 Register
Mnemonic	IOM0.DDRPHY_SEQ_RESERVED_ADDR4_P0
Address	8000C4070701103F (SCOM)
Description	This register contains the reserved address to be used during calibration algorithms in the memory devices. This address is used within all primary ranks of rank pairs. Address mirroring, if enabled, does not alter the address bit mapping of this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	RESERVED_ADDR4: Reserved address field 4. Bank address. Bits 48 - 49 map to BA0 - BA1, and bits 50 - 51 map to BG0 - BG1. Bits 52 - 63 are reserved. MPR reads performed by the internal calibration routines: BA0 - BA1 are forced to 00b to access MPR0. Reads performed by the internal calibration routines: BG1 is toggled (both values of BG1 are used/reserved) and all banks are accessed (all BA0 - BA1 are addressed used/reserved).

Register Name	SEQ Reserved Address 4 Register
Mnemonic	IOM0.DDRPHY_SEQ_RESERVED_ADDR4_P1
Address	8000C4070701143F (SCOM)
Description	This register contains the reserved address to be used during calibration algorithms in the memory devices. This address is used within all primary ranks of rank pairs. Address mirroring, if enabled, does not alter the address bit mapping of this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	RESERVED_ADDR4: Reserved address field 4. Bank address. Bits 48 - 49 map to BA0 - BA1, and bits 50 - 51 map to BG0 - BG1. Bits 52 - 63 are reserved. MPR reads performed by the internal calibration routines: BA0 - BA1 are forced to 00b to access MPR0. Reads performed by the internal calibration routines: BG1 is toggled (both values of BG1 are used/reserved) and all banks are accessed (all BA0 - BA1 are addressed used/reserved).

Register Name	SEQ Reserved Address 4 Register
Mnemonic	IOM0.DDRPHY_SEQ_RESERVED_ADDR4_P2
Address	8000C4070701183F (SCOM)
Description	This register contains the reserved address to be used during calibration algorithms in the memory devices. This address is used within all primary ranks of rank pairs. Address mirroring, if enabled, does not alter the address bit mapping of this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	RESERVED_ADDR4: Reserved address field 4. Bank address. Bits 48 - 49 map to BA0 - BA1, and bits 50 - 51 map to BG0 - BG1. Bits 52 - 63 are reserved. MPR reads performed by the internal calibration routines: BA0 - BA1 are forced to 00b to access MPR0. Reads performed by the internal calibration routines: BG1 is toggled (both values of BG1 are used/reserved) and all banks are accessed (all BA0 - BA1 are addressed used/reserved).

Register Name	SEQ Reserved Address 4 Register
Mnemonic	IOM0.DDRPHY_SEQ_RESERVED_ADDR4_P3
Address	8000C40707011C3F (SCOM)
Description	This register contains the reserved address to be used during calibration algorithms in the memory devices. This address is used within all primary ranks of rank pairs. Address mirroring, if enabled, does not alter the address bit mapping of this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	RESERVED_ADDR4: Reserved address field 4. Bank address. Bits 48 - 49 map to BA0 - BA1, and bits 50 - 51 map to BG0 - BG1. Bits 52 - 63 are reserved. MPR reads performed by the internal calibration routines: BA0 - BA1 are forced to 00b to access MPR0. Reads performed by the internal calibration routines: BG1 is toggled (both values of BG1 are used/reserved) and all banks are accessed (all BA0 - BA1 are addressed used/reserved).

Register Name	SEQ Error Status 0 Register
Mnemonic	IOM0.DDRPHY_SEQ_ERROR_STATUS0_P0
Address	8000C4080701103F (SCOM)
Description	This register contains error and status information about the sequencer logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	MULTIPLE_REQ_ERROR: 1 = Error: Multiple requests received at the same time.
49	RWX	INVALID_REQTYPE_ERROR: 1 = Error: In the current state, this request is not expected.
50	RWX	EARLY_REQ_ERROR: 1 = Error: A new request arrived before acknowledgment of the previous request.
51:53	RWX	MULTIPLE_REQ_SOURCE: If MULTIPLE_REQ_ERROR is flagged, the source of the request is indicated by these bits. Bits 51:53 = {PC_REQ, RC_REQ, WC_REQ}.
54:57	RWX	INVALID_REQTYPE: If INVALID_REQTYPE_ERROR is flagged, the type of request is indicated by this register.
58:60	RWX	INVALID_REQ_SOURCE: If INVALID_REQ_ERROR is flagged, the source of the request is indicated by these bits. Bits 58:60 = {PC_REQ, RC_REQ, WC_REQ}.
61:63	RWX	EARLY_REQ_SOURCE: If EARLY_REQ_ERROR is flagged, the source of the request is indicated by these bits. Bits 61:63 = {PC_REQ, RC_REQ, WC_REQ}.

Register Name	SEQ Error Status 0 Register
Mnemonic	IOM0.DDRPHY_SEQ_ERROR_STATUS0_P1
Address	8000C4080701143F (SCOM)
Description	This register contains error and status information about the sequencer logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	RWX	MULTIPLE_REQ_ERROR: 1 = Error: Multiple requests received at the same time.
49	RWX	INVALID_REQTYPE_ERROR: 1 = Error: In the current state, this request is not expected.
50	RWX	EARLY_REQ_ERROR: 1 = Error: A new request arrived before acknowledgment of the previous request.
51:53	RWX	MULTIPLE_REQ_SOURCE: If MULTIPLE_REQ_ERROR is flagged, the source of the request is indicated by these bits. Bits 51:53 = {PC_REQ, RC_REQ, WC_REQ}.
54:57	RWX	INVALID_REQTYPE: If INVALID_REQTYPE_ERROR is flagged, the type of request is indicated by this register.
58:60	RWX	INVALID_REQ_SOURCE: If INVALID_REQ_ERROR is flagged, the source of the request is indicated by these bits. Bits 58:60 = {PC_REQ, RC_REQ, WC_REQ}.
61:63	RWX	EARLY_REQ_SOURCE: If EARLY_REQ_ERROR is flagged, the source of the request is indicated by these bits. Bits 61:63 = {PC_REQ, RC_REQ, WC_REQ}.

Register Name	SEQ Error Status 0 Register
Mnemonic	IOM0.DDRPHY_SEQ_ERROR_STATUS0_P2
Address	8000C4080701183F (SCOM)
Description	This register contains error and status information about the sequencer logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RWX	MULTIPLE_REQ_ERROR: 1 = Error: Multiple requests received at the same time.
49	RWX	INVALID_REQTYPE_ERROR: 1 = Error: In the current state, this request is not expected.
50	RWX	EARLY_REQ_ERROR: 1 = Error: A new request arrived before acknowledgment of the previous request.
51:53	RWX	MULTIPLE_REQ_SOURCE: If MULTIPLE_REQ_ERROR is flagged, the source of the request is indicated by these bits. Bits 51:53 = {PC_REQ, RC_REQ, WC_REQ}.
54:57	RWX	INVALID_REQTYPE: If INVALID_REQTYPE_ERROR is flagged, the type of request is indicated by this register.
58:60	RWX	INVALID_REQ_SOURCE: If INVALID_REQ_ERROR is flagged, the source of the request is indicated by these bits. Bits 58:60 = {PC_REQ, RC_REQ, WC_REQ}.
61:63	RWX	EARLY_REQ_SOURCE: If EARLY_REQ_ERROR is flagged, the source of the request is indicated by these bits. Bits 61:63 = {PC_REQ, RC_REQ, WC_REQ}.

Register Name	SEQ Error Status 0 Register
Mnemonic	IOM0.DDRPHY_SEQ_ERROR_STATUS0_P3
Address	8000C40807011C3F (SCOM)
Description	This register contains error and status information about the sequencer logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RWX	MULTIPLE_REQ_ERROR: 1 = Error: Multiple requests received at the same time.
49	RWX	INVALID_REQTYPE_ERROR: 1 = Error: In the current state, this request is not expected.
50	RWX	EARLY_REQ_ERROR: 1 = Error: A new request arrived before acknowledgment of the previous request.
51:53	RWX	MULTIPLE_REQ_SOURCE: If MULTIPLE_REQ_ERROR is flagged, the source of the request is indicated by these bits. Bits 51:53 = {PC_REQ, RC_REQ, WC_REQ}.
54:57	RWX	INVALID_REQTYPE: If INVALID_REQTYPE_ERROR is flagged, the type of request is indicated by this register.
58:60	RWX	INVALID_REQ_SOURCE: If INVALID_REQ_ERROR is flagged, the source of the request is indicated by these bits. Bits 58:60 = {PC_REQ, RC_REQ, WC_REQ}.

Bits	SCOM	Field Mnemonic: Description
61:63	RWX	EARLY_REQ_SOURCE: If EARLY_REQ_ERROR is flagged, the source of the request is indicated by these bits. Bits 61:63 = {PC_REQ, RC_REQ, WC_REQ}.

Register Name	SEQ Error Mask 0 Register
Mnemonic	IOM0.DDRPHY_SEQ_ERROR_MASK0_P0
Address	8000C4090701103F (SCOM)
Description	This register masks errors in the SEQ Error Status 0 Register. It also prevents the SEQ_ERROR bit from being set in the PC Error Status 0 Register and the appropriate bit from being set in the PC Initial Calibration Error Register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	MULT_REQ_ERR_MASK: 1 = Prevent the MULTIPLE_REQ_ERROR bit from being set in the SEQ Error Status 0 Register. 0 = Allow the MULTIPLE_REQ_ERROR bit to be set.
49	RW	INVALID_REQTYPE_ERR_MASK: 1 = Prevent the INVALID_REQTYPE_ERROR bit from being set in the SEQ Error Status 0 Register. 0 = Allow the INVALID_REQTYPE_ERROR bit to be set.
50	RW	EARLY_REQ_ERR_MASK: 1 = Prevent the EARLY_REQ_ERROR bit from being set in the SEQ Error Status 0 Register. 0 = Allow the EARLY_REQ_ERROR bit to be set.
51:63	RW	Reserved.

Register Name	SEQ Error Mask 0 Register
Mnemonic	IOM0.DDRPHY_SEQ_ERROR_MASK0_P1
Address	8000C4090701143F (SCOM)
Description	This register masks errors in the SEQ Error Status 0 Register. It also prevents the SEQ_ERROR bit from being set in the PC Error Status 0 Register and the appropriate bit from being set in the PC Initial Calibration Error Register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	MULT_REQ_ERR_MASK: 1 = Prevent the MULTIPLE_REQ_ERROR bit from being set in the SEQ Error Status 0 Register. 0 = Allow the MULTIPLE_REQ_ERROR bit to be set.
49	RW	INVALID_REQTYPE_ERR_MASK: 1 = Prevent the INVALID_REQTYPE_ERROR bit from being set in the SEQ Error Status 0 Register. 0 = Allow the INVALID_REQTYPE_ERROR bit to be set.
50	RW	EARLY_REQ_ERR_MASK: 1 = Prevent the EARLY_REQ_ERROR bit from being set in the SEQ Error Status 0 Register. 0 = Allow the EARLY_REQ_ERROR bit to be set.
51:63	RW	Reserved.

Register Name	SEQ Error Mask 0 Register
Mnemonic	IOM0.DDRPHY_SEQ_ERROR_MASK0_P2
Address	8000C4090701183F (SCOM)
Description	This register masks errors in the SEQ Error Status 0 Register. It also prevents the SEQ_ERROR bit from being set in the PC Error Status 0 Register and the appropriate bit from being set in the PC Initial Calibration Error Register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	MULT_REQ_ERR_MASK: 1 = Prevent the MULTIPLE_REQ_ERROR bit from being set in the SEQ Error Status 0 Register. 0 = Allow the MULTIPLE_REQ_ERROR bit to be set.
49	RW	INVALID_REQTYPE_ERR_MASK: 1 = Prevent the INVALID_REQTYPE_ERROR bit from being set in the SEQ Error Status 0 Register. 0 = Allow the INVALID_REQTYPE_ERROR bit to be set.
50	RW	EARLY_REQ_ERR_MASK: 1 = Prevent the EARLY_REQ_ERROR bit from being set in the SEQ Error Status 0 Register. 0 = Allow the EARLY_REQ_ERROR bit to be set.
51:63	RW	Reserved.

Register Name	SEQ Error Mask 0 Register
Mnemonic	IOM0.DDRPHY_SEQ_ERROR_MASK0_P3
Address	8000C40907011C3F (SCOM)
Description	This register masks errors in the SEQ Error Status 0 Register. It also prevents the SEQ_ERROR bit from being set in the PC Error Status 0 Register and the appropriate bit from being set in the PC Initial Calibration Error Register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	MULT_REQ_ERR_MASK: 1 = Prevent the MULTIPLE_REQ_ERROR bit from being set in the SEQ Error Status 0 Register. 0 = Allow the MULTIPLE_REQ_ERROR bit to be set.
49	RW	INVALID_REQTYPE_ERR_MASK: 1 = Prevent the INVALID_REQTYPE_ERROR bit from being set in the SEQ Error Status 0 Register. 0 = Allow the INVALID_REQTYPE_ERROR bit to be set.
50	RW	EARLY_REQ_ERR_MASK: 1 = Prevent the EARLY_REQ_ERROR bit from being set in the SEQ Error Status 0 Register. 0 = Allow the EARLY_REQ_ERROR bit to be set.
51:63	RW	Reserved.

Register Name	SEQ ODT Write Configuration 0 Register
Mnemonic	IOM0.DDRPHY_SEQ_ODT_WR_CONFIG0_P0
Address	8000C40A0701103F (SCOM)
Description	This register determines the on-die termination (ODT) values that are sent to all ranks when the given rank is written during calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:51	RW	ODT_WR_VALUES0: This 4-bit value is driven on ODT pins 0:3 when rank {0-1} × 2 is written. This field corresponds to the even rank.
52:55	RW	Reserved.
56:59	RW	ODT_WR_VALUES1: This 4-bit value is driven on ODT pins 0:3 when rank {0-1} × 2 + 1 is written. This field corresponds to the odd rank.
60:63	RW	Reserved.

Register Name	SEQ ODT Write Configuration 0 Register
Mnemonic	IOM0.DDRPHY_SEQ_ODT_WR_CONFIG0_P1
Address	8000C40A0701143F (SCOM)
Description	This register determines the ODT values that are sent to all ranks when the given rank is written during calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:51	RW	ODT_WR_VALUES0: This 4-bit value is driven on ODT pins 0:3 when rank {0-1} × 2 is written. This field corresponds to the even rank.
52:55	RW	Reserved.
56:59	RW	ODT_WR_VALUES1: This 4-bit value is driven on ODT pins 0:3 when rank {0-1} × 2 + 1 is written. This field corresponds to the odd rank.
60:63	RW	Reserved.

Register Name	SEQ ODT Write Configuration 0 Register
Mnemonic	IOM0.DDRPHY_SEQ_ODT_WR_CONFIG0_P2
Address	8000C40A0701183F (SCOM)
Description	This register determines the ODT values that are sent to all ranks when the given rank is written during calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:51	RW	ODT_WR_VALUES0: This 4-bit value is driven on ODT pins 0:3 when rank {0-1} × 2 is written. This field corresponds to the even rank.
52:55	RW	Reserved.
56:59	RW	ODT_WR_VALUES1: This 4-bit value is driven on ODT pins 0:3 when rank {0-1} × 2 + 1 is written. This field corresponds to the odd rank.
60:63	RW	Reserved.

Register Name	SEQ ODT Write Configuration 0 Register
Mnemonic	IOM0.DDRPHY_SEQ_ODT_WR_CONFIG0_P3
Address	8000C40A07011C3F (SCOM)
Description	This register determines the ODT values that are sent to all ranks when the given rank is written during calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	ODT_WR_VALUES0: This 4-bit value is driven on ODT pins 0:3 when rank {0-1} × 2 is written. This field corresponds to the even rank.
52:55	RW	Reserved.
56:59	RW	ODT_WR_VALUES1: This 4-bit value is driven on ODT pins 0:3 when rank {0-1} × 2 + 1 is written. This field corresponds to the odd rank.
60:63	RW	Reserved.

Register Name	SEQ ODT Write Configuration 1 Register
Mnemonic	IOM0.DDRPHY_SEQ_ODT_WR_CONFIG1_P0
Address	8000C40B0701103F (SCOM)
Description	This register determines the ODT values that are sent to all ranks when the given rank is written during calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	ODT_WR_VALUES2: This 4-bit value is driven on ODT pins 0:3 when rank {0-1} × 2 is written. This field corresponds to the even rank.
52:55	RW	Reserved.
56:59	RW	ODT_WR_VALUES3: This 4-bit value is driven on ODT pins 0:3 when rank {0-1} × 2 + 1 is written. This field corresponds to the odd rank.
60:63	RW	Reserved.

Register Name	SEQ ODT Write Configuration 1 Register
Mnemonic	IOM0.DDRPHY_SEQ_ODT_WR_CONFIG1_P1
Address	8000C40B0701143F (SCOM)
Description	This register determines the ODT values that are sent to all ranks when the given rank is written during calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	ODT_WR_VALUES2: This 4-bit value is driven on ODT pins 0:3 when rank {0-1} × 2 is written. This field corresponds to the even rank.
52:55	RW	Reserved.
56:59	RW	ODT_WR_VALUES3: This 4-bit value is driven on ODT pins 0:3 when rank {0-1} × 2 + 1 is written. This field corresponds to the odd rank.

Bits	SCOM	Field Mnemonic: Description
60:63	RW	Reserved.

Register Name	SEQ ODT Write Configuration 1 Register
Mnemonic	IOM0.DDRPHY_SEQ_ODT_WR_CONFIG1_P2
Address	8000C40B0701183F (SCOM)
Description	This register determines the ODT values that are sent to all ranks when the given rank is written during calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	ODT_WR_VALUES2: This 4-bit value is driven on ODT pins 0:3 when rank {0-1} × 2 is written. This field corresponds to the even rank.
52:55	RW	Reserved.
56:59	RW	ODT_WR_VALUES3: This 4-bit value is driven on ODT pins 0:3 when rank {0-1} × 2 + 1 is written. This field corresponds to the odd rank.
60:63	RW	Reserved.

Register Name	SEQ ODT Write Configuration 1 Register
Mnemonic	IOM0.DDRPHY_SEQ_ODT_WR_CONFIG1_P3
Address	8000C40B07011C3F (SCOM)
Description	This register determines the ODT values that are sent to all ranks when the given rank is written during calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	ODT_WR_VALUES2: This 4-bit value is driven on ODT pins 0:3 when rank {0-1} × 2 is written. This field corresponds to the even rank.
52:55	RW	Reserved.
56:59	RW	ODT_WR_VALUES3: This 4-bit value is driven on ODT pins 0:3 when rank {0-1} × 2 + 1 is written. This field corresponds to the odd rank.
60:63	RW	Reserved.

Register Name	SEQ ODT Read Configuration 0 Register
Mnemonic	IOM0.DDRPHY_SEQ_ODT_RD_CONFIG0_P0
Address	8000C40E0701103F (SCOM)
Description	This register determines the ODT values that are sent to all ranks when the given rank is read during calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	ODT_RD_VALUES0: This 4-bit value is driven on ODT pins 0:3 when rank {0-1} × 2 is read. This field corresponds to the even rank.

Bits	SCOM	Field Mnemonic: Description
52:55	RW	Reserved.
56:59	RW	ODT_RD_VALUES1: This 4-bit value is driven on ODT pins 0:3 when rank {0-1} × 2 + 1 is read. This field corresponds to the odd rank.
60:63	RW	Reserved.

Register Name	SEQ ODT Read Configuration 0 Register
Mnemonic	IOM0.DDRPHY_SEQ_ODT_RD_CONFIG0_P1
Address	8000C40E0701143F (SCOM)
Description	This register determines the ODT values that are sent to all ranks when the given rank is read during calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	ODT_RD_VALUES0: This 4-bit value is driven on ODT pins 0:3 when rank {0-1} × 2 is read. This field corresponds to the even rank.
52:55	RW	Reserved.
56:59	RW	ODT_RD_VALUES1: This 4-bit value is driven on ODT pins 0:3 when rank {0-1} × 2 + 1 is read. This field corresponds to the odd rank.
60:63	RW	Reserved.

Register Name	SEQ ODT Read Configuration 0 Register
Mnemonic	IOM0.DDRPHY_SEQ_ODT_RD_CONFIG0_P2
Address	8000C40E0701183F (SCOM)
Description	This register determines the ODT values that are sent to all ranks when the given rank is read during calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	ODT_RD_VALUES0: This 4-bit value is driven on ODT pins 0:3 when rank {0-1} × 2 is read. This field corresponds to the even rank.
52:55	RW	Reserved.
56:59	RW	ODT_RD_VALUES1: This 4-bit value is driven on ODT pins 0:3 when rank {0-1} × 2 + 1 is read. This field corresponds to the odd rank.
60:63	RW	Reserved.

Register Name	SEQ ODT Read Configuration 0 Register
Mnemonic	IOM0.DDRPHY_SEQ_ODT_RD_CONFIG0_P3
Address	8000C40E07011C3F (SCOM)
Description	This register determines the ODT values that are sent to all ranks when the given rank is read during calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:51	RW	ODT_RD_VALUES0: This 4-bit value is driven on ODT pins 0:3 when rank {0-1} × 2 is read. This field corresponds to the even rank.
52:55	RW	Reserved.
56:59	RW	ODT_RD_VALUES1: This 4-bit value is driven on ODT pins 0:3 when rank {0-1} × 2 + 1 is read. This field corresponds to the odd rank.
60:63	RW	Reserved.

Register Name	SEQ ODT Read Configuration 1 Register
Mnemonic	IOM0.DDRPHY_SEQ_ODT_RD_CONFIG1_P0
Address	8000C40F0701103F (SCOM)
Description	This register determines the ODT values that are sent to all ranks when the given rank is read during calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:51	RW	ODT_RD_VALUES2: This 4-bit value is driven on ODT pins 0:3 when rank {0-1} × 2 is read. This field corresponds to the even rank.
52:55	RW	Reserved.
56:59	RW	ODT_RD_VALUES3: This 4-bit value is driven on ODT pins 0:3 when rank {0-1} × 2 + 1 is read. This field corresponds to the odd rank.
60:63	RW	Reserved.

Register Name	SEQ ODT Read Configuration 1 Register
Mnemonic	IOM0.DDRPHY_SEQ_ODT_RD_CONFIG1_P1
Address	8000C40F0701143F (SCOM)
Description	This register determines the ODT values that are sent to all ranks when the given rank is read during calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:51	RW	ODT_RD_VALUES2: This 4-bit value is driven on ODT pins 0:3 when rank {0-1} × 2 is read. This field corresponds to the even rank.
52:55	RW	Reserved.
56:59	RW	ODT_RD_VALUES3: This 4-bit value is driven on ODT pins 0:3 when rank {0-1} × 2 + 1 is read. This field corresponds to the odd rank.
60:63	RW	Reserved.

Register Name	SEQ ODT Read Configuration 1 Register
Mnemonic	IOM0.DDRPHY_SEQ_ODT_RD_CONFIG1_P2
Address	8000C40F0701183F (SCOM)
Description	This register determines the ODT values that are sent to all ranks when the given rank is read during calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	ODT_RD_VALUES2: This 4-bit value is driven on ODT pins 0:3 when rank {0-1} × 2 is read. This field corresponds to the even rank.
52:55	RW	Reserved.
56:59	RW	ODT_RD_VALUES3: This 4-bit value is driven on ODT pins 0:3 when rank {0-1} × 2 + 1 is read. This field corresponds to the odd rank.
60:63	RW	Reserved.

Register Name	SEQ ODT Read Configuration 1 Register
Mnemonic	IOM0.DDRPHY_SEQ_ODT_RD_CONFIG1_P3
Address	8000C40F07011C3F (SCOM)
Description	This register determines the ODT values that are sent to all ranks when the given rank is read during calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	ODT_RD_VALUES2: This 4-bit value is driven on ODT pins 0:3 when rank {0-1} × 2 is read. This field corresponds to the even rank.
52:55	RW	Reserved.
56:59	RW	ODT_RD_VALUES3: This 4-bit value is driven on ODT pins 0:3 when rank {0-1} × 2 + 1 is read. This field corresponds to the odd rank.
60:63	RW	Reserved.

Register Name	SEQ Memory Timing Parameter 0 Register
Mnemonic	IOM0.DDRPHY_SEQ_MEM_TIMING_PARAM0_P0
Address	8000C4120701103F (SCOM)
Description	This register determines the memory timing parameters to be used during calibration. Each nibble is used as an exponent of 2, to calculate the number of MEMINTCLKO clock cycles. For example, if TMOD_CYCLES[0:3] = 5, the internal timers use the value 25 = 32 MEMINTCLKO clock cycles. The maximum value per nibble is Ah.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	TMOD_CYCLES: max(tMRD, tMOD).
52:55	RW	TRCD_CYCLES: tRCD.
56:59	RW	TRP_CYCLES: tRP.

Bits	SCOM	Field Mnemonic: Description
60:63	RW	TRFC_CYCLES: tRFC.

Register Name	SEQ Memory Timing Parameter 0 Register
Mnemonic	IOM0.DDRPHY_SEQ_MEM_TIMING_PARAM0_P1
Address	8000C4120701143F (SCOM)
Description	This register determines the memory timing parameters to be used during calibration. Each nibble is used as an exponent of 2, to calculate the number of MEMINTCLKO clock cycles. For example, if TMOD_CYCLES[0:3] = 5, the internal timers use the value 25 = 32 MEMINTCLKO clock cycles. The maximum value per nibble is Ah.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	TMOD_CYCLES: max(tMRD, tMOD).
52:55	RW	TRCD_CYCLES: tRCD.
56:59	RW	TRP_CYCLES: tRP.
60:63	RW	TRFC_CYCLES: tRFC.

Register Name	SEQ Memory Timing Parameter 0 Register
Mnemonic	IOM0.DDRPHY_SEQ_MEM_TIMING_PARAM0_P2
Address	8000C4120701183F (SCOM)
Description	This register determines the memory timing parameters to be used during calibration. Each nibble is used as an exponent of 2, to calculate the number of MEMINTCLKO clock cycles. For example, if TMOD_CYCLES[0:3] = 5, the internal timers use the value 25 = 32 MEMINTCLKO clock cycles. The maximum value per nibble is Ah.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	TMOD_CYCLES: max(tMRD, tMOD).
52:55	RW	TRCD_CYCLES: tRCD.
56:59	RW	TRP_CYCLES: tRP.
60:63	RW	TRFC_CYCLES: tRFC.

Register Name	SEQ Memory Timing Parameter 0 Register
Mnemonic	IOM0.DDRPHY_SEQ_MEM_TIMING_PARAM0_P3
Address	8000C41207011C3F (SCOM)
Description	This register determines the memory timing parameters to be used during calibration. Each nibble is used as an exponent of 2, to calculate the number of MEMINTCLKO clock cycles. For example, if TMOD_CYCLES[0:3] = 5, the internal timers use the value 25 = 32 MEMINTCLKO clock cycles. The maximum value per nibble is Ah.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	TMOD_CYCLES: max(tMRD, tMOD).
52:55	RW	TRCD_CYCLES: tRCD.
56:59	RW	TRP_CYCLES: tRP.
60:63	RW	TRFC_CYCLES: tRFC.

Register Name	SEQ Memory Timing Parameter 1 Register
Mnemonic	IOM0.DDRPHY_SEQ_MEM_TIMING_PARAM1_P0
Address	8000C4130701103F (SCOM)
Description	This register determines the memory timing parameters to be used during calibration. Each nibble is used as an exponent of 2, to calculate the number of MEMINTCLKO clock cycles, For example, if TMOD_CYCLES[0:3] = 5, the internal timers use the value 25 = 32 MEMINTCLKO clock cycles. The maximum value per nibble is Ah.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	TZQINIT_CYCLES: max(tZQINIT,tZQOPER).
52:55	RW	TZQCS_CYCLES: tZQCS.
56:59	RW	TWLDQSEN_CYCLES: tWLDQSEN.
60:63	RW	TWRMRD_CYCLES: tWLMRD.

Register Name	SEQ Memory Timing Parameter 1 Register
Mnemonic	IOM0.DDRPHY_SEQ_MEM_TIMING_PARAM1_P1
Address	8000C4130701143F (SCOM)
Description	This register determines the memory timing parameters to be used during calibration. Each nibble is used as an exponent of 2, to calculate the number of MEMINTCLKO clock cycles, For example, if TMOD_CYCLES[0:3] = 5, the internal timers use the value 25 = 32 MEMINTCLKO clock cycles. The maximum value per nibble is Ah.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	TZQINIT_CYCLES: max(tZQINIT,tZQOPER).
52:55	RW	TZQCS_CYCLES: tZQCS.
56:59	RW	TWLDQSEN_CYCLES: tWLDQSEN.
60:63	RW	TWRMRD_CYCLES: tWLMRD.

Register Name	SEQ Memory Timing Parameter 1 Register
Mnemonic	IOM0.DDRPHY_SEQ_MEM_TIMING_PARAM1_P2
Address	8000C4130701183F (SCOM)
Description	This register determines the memory timing parameters to be used during calibration. Each nibble is used as an exponent of 2, to calculate the number of MEMINTCLKO clock cycles, For example, if TMOD_CYCLES[0:3] = 5, the internal timers use the value 25 = 32 MEMINTCLKO clock cycles. The maximum value per nibble is Ah.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	TZQINIT_CYCLES: max(tZQINIT,tZQOPER).
52:55	RW	TZQCS_CYCLES: tZQCS.
56:59	RW	TWLDQSEN_CYCLES: tWLDQSEN.
60:63	RW	TWRMRD_CYCLES: tWLMRD.

Register Name	SEQ Memory Timing Parameter 1 Register
Mnemonic	IOM0.DDRPHY_SEQ_MEM_TIMING_PARAM1_P3
Address	8000C41307011C3F (SCOM)
Description	This register determines the memory timing parameters to be used during calibration. Each nibble is used as an exponent of 2, to calculate the number of MEMINTCLKO clock cycles, For example, if TMOD_CYCLES[0:3] = 5, the internal timers use the value 25 = 32 MEMINTCLKO clock cycles. The maximum value per nibble is Ah.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	TZQINIT_CYCLES: max(tZQINIT,tZQOPER).
52:55	RW	TZQCS_CYCLES: tZQCS.
56:59	RW	TWLDQSEN_CYCLES: tWLDQSEN.
60:63	RW	TWRMRD_CYCLES: tWLMRD.

Register Name	SEQ Memory Timing Parameter 2 Register
Mnemonic	IOM0.DDRPHY_SEQ_MEM_TIMING_PARAM2_P0
Address	8000C4140701103F (SCOM)
Description	This register determines the memory timing parameters to be used during calibration. Each nibble is used as an exponent of 2, to calculate the number of MEMINTCLKO clock cycles. That is, if TMOD_CYCLES[0:3] = 5, the internal timers use the value 25 = 32 MEMINTCLKO clock cycles. The maximum allowed value per nibble is Ah.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	TODTLON_OFF_CYCLES: max(ODTLon, ODTLoff). When the ODT values change during a calibration algorithm, the PHY waits TODTLON_OFF_CYCLES 2 memory clock cycles before changing the ODT values. The ODT values might change because of a rank change, or a change from read ODT values to write ODT values, or because a mode register set (MRS) command is issued. For more information, see SEQ ODT Write Configuration {0-3} Registers and SEQ ODT Read Configuration {0-3} Registers. The ODT pins must be forced to zero during MRS commands when RTT_Nom is enabled via MR1. This is independent of the values stored in the SEQ ODT Write/Read Configuration {0-3} Registers. Before issuing the MRS command, the DDR PHY checks if the ODT pin was recently changed within the window. It waits for the tODTLOFF cycles to expire. When tODTLOFF expires, the ODT value is forced to zero, and the DDR PHY again waits for tODTLOFF cycles. After this, the MRS command is issued. The DDR PHY waits for tMOD cycles, and then restores the ODT pins to their prior state.
52:63	RW	Reserved.

Register Name	SEQ Memory Timing Parameter 2 Register
Mnemonic	IOM0.DDRPHY_SEQ_MEM_TIMING_PARAM2_P1
Address	8000C4140701143F (SCOM)
Description	This register determines the memory timing parameters to be used during calibration. Each nibble is used as an exponent of 2, to calculate the number of MEMINTCLKO clock cycles. That is, if TMOD_CYCLES[0:3] = 5, the internal timers use the value 25 = 32 MEMINTCLKO clock cycles. The maximum allowed value per nibble is Ah.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	TODTLON_OFF_CYCLES: max(ODTLon, ODTLoff). When the ODT values change during a calibration algorithm, the PHY waits TODTLON_OFF_CYCLES 2 memory clock cycles before changing the ODT values. The ODT values might change because of a rank change, or a change from read ODT values to write ODT values, or because an MRS command is issued. For more information, see SEQ ODT Write Configuration {0-3} Registers and SEQ ODT Read Configuration {0-3} Registers. The ODT pins must be forced to zero during MRS commands when RTT_Nom is enabled via MR1. This is independent of the values stored in the SEQ ODT Write/Read Configuration {0-3} Registers. Before issuing the MRS command, the DDR PHY checks if the ODT pin was recently changed within the window. It waits for the tODTLOFF cycles to expire. When tODTLOFF expires, the ODT value is forced to zero, and the DDR PHY again waits for tODTLOFF cycles. After this, the MRS command is issued. The DDR PHY waits for tMOD cycles, and then restores the ODT pins to their prior state.
52:63	RW	Reserved.

Register Name	SEQ Memory Timing Parameter 2 Register
Mnemonic	IOM0.DDRPHY_SEQ_MEM_TIMING_PARAM2_P2
Address	8000C4140701183F (SCOM)
Description	This register determines the memory timing parameters to be used during calibration. Each nibble is used as an exponent of 2, to calculate the number of MEMINTCLKO clock cycles. That is, if TMOD_CYCLES[0:3] = 5, the internal timers use the value 25 = 32 MEMINTCLKO clock cycles. The maximum allowed value per nibble is Ah.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	TODTLON_OFF_CYCLES: max(ODTLon, ODTLoff). When the ODT values change during a calibration algorithm, the PHY waits TODTLON_OFF_CYCLES 2 memory clock cycles before changing the ODT values. The ODT values might change because of a rank change, or a change from read ODT values to write ODT values, or because an MRS command is issued. For more information, see SEQ ODT Write Configuration {0-3} Registers and SEQ ODT Read Configuration {0-3} Registers. The ODT pins must be forced to zero during MRS commands when RTT_Nom is enabled via MR1. This is independent of the values stored in the SEQ ODT Write/Read Configuration {0-3} Registers. Before issuing the MRS command, the DDR PHY checks if the ODT pin was recently changed within the window. It waits for the tODTLOFF cycles to expire. When tODTLOFF expires, the ODT value is forced to zero, and the DDR PHY again waits for tODTLOFF cycles. After this, the MRS command is issued. The DDR PHY waits for tMOD cycles, and then restores the ODT pins to their prior state.
52:63	RW	Reserved.

Register Name	SEQ Memory Timing Parameter 2 Register
Mnemonic	IOM0.DDRPHY_SEQ_MEM_TIMING_PARAM2_P3
Address	8000C41407011C3F (SCOM)
Description	This register determines the memory timing parameters to be used during calibration. Each nibble is used as an exponent of 2, to calculate the number of MEMINTCLKO clock cycles. That is, if TMOD_CYCLES[0:3] = 5, the internal timers use the value 25 = 32 MEMINTCLKO clock cycles. The maximum allowed value per nibble is Ah.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	TODTLON_OFF_CYCLES: max(ODTLon, ODTLoff). When the ODT values change during a calibration algorithm, the PHY waits TODTLON_OFF_CYCLES 2 memory clock cycles before changing the ODT values. The ODT values might change because of a rank change, or a change from read ODT values to write ODT values, or because an MRS command is issued. For more information, see SEQ ODT Write Configuration {0-3} Registers and SEQ ODT Read Configuration {0-3} Registers. The ODT pins must be forced to zero during MRS commands when RTT_Nom is enabled via MR1. This is independent of the values stored in the SEQ ODT Write/Read Configuration {0-3} Registers. Before issuing the MRS command, the DDR PHY checks if the ODT pin was recently changed within the window. It waits for the tODTLOFF cycles to expire. When tODTLOFF expires, the ODT value is forced to zero, and the DDR PHY again waits for tODTLOFF cycles. After this, the MRS command is issued. The DDR PHY waits for tMOD cycles, and then restores the ODT pins to their prior state.
52:63	RW	Reserved.

Register Name	SEQ Low Power Termination Address 2 Register
Mnemonic	IOM0.DDRPHY_SEQ_LPT_ADDR2_P0
Address	8000C4170701103F (SCOM)
Description	This register corresponds to the SEQ Reserved Address {2-4} Register for DDR4 bit mapping.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	LPT_ADDR2: The bit positions and mapping of the bit positions to the Address/BA/BG pins in DDR4 of the SEQ Low Power Termination Address{2-4} Registers correspond to the bit positions and mapping of the bit positions to the Address/BA/BG pins in the SEQ Reserved Address{2-4} Registers. The content of these registers that corresponds to: BA(0:1), BG(0), A(0:9), A(11), A(13), A(17), BG(1) is driven onto the Address/BA/BG pins during idle bus cycles during periodic calibration. Register bits within these registers that correspond to Address/BA/BG not listed above are reserved. A(0:9) = LPT_ADDR2(48:57). A(11) = LPT_ADDR2(59). A(13) = LPT_ADDR2(61). A(17) = LPT_ADDR3(49). BA(0:1) = LPT_ADDR4(48:49). BG(0:1) = LPT_ADDR4(50:51). All other register bit positions are reserved.

Register Name	SEQ Low Power Termination Address 2 Register
Mnemonic	IOM0.DDRPHY_SEQ_LPT_ADDR2_P1
Address	8000C4170701143F (SCOM)
Description	This register corresponds to the SEQ Reserved Address {2-4} Register for DDR4 bit mapping.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	LPT_ADDR2: The bit positions and mapping of the bit positions to the Address/BA/BG pins in DDR4 of the SEQ Low Power Termination Address{2-4} Registers correspond to the bit positions and mapping of the bit positions to the Address/BA/BG pins in the SEQ Reserved Address{2-4} registers. The content of these registers that corresponds to: BA(0:1), BG(0), A(0:9), A(11), A(13), A(17), BG(1) is driven onto the Address/BA/BG pins during idle bus cycles during periodic calibration. Register bits within these registers that correspond to Address/BA/BG not listed above are reserved. A(0:9) = LPT_ADDR2(48:57). A(11) = LPT_ADDR2(59). A(13) = LPT_ADDR2(61). A(17) = LPT_ADDR3(49). BA(0:1) = LPT_ADDR4(48:49). BG(0:1) = LPT_ADDR4(50:51). All other register bit positions are reserved.

Register Name	SEQ Low Power Termination Address 2 Register
Mnemonic	IOM0.DDRPHY_SEQ_LPT_ADDR2_P2
Address	8000C4170701183F (SCOM)
Description	This register corresponds to the SEQ Reserved Address {2-4} Register for DDR4 bit mapping.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	LPT_ADDR2: The bit positions and mapping of the bit positions to the Address/BA/BG pins in DDR4 of the SEQ Low Power Termination Address{2-4} Registers correspond to the bit positions and mapping of the bit positions to the Address/BA/BG pins in the SEQ Reserved Address{2-4} registers. The content of these registers that corresponds to: BA(0:1), BG(0), A(0:9), A(11), A(13), A(17), BG(1) is driven onto the Address/BA/BG pins during idle bus cycles during periodic calibration. Register bits within these registers that correspond to Address/BA/BG not listed above are reserved. A(0:9) = LPT_ADDR2(48:57). A(11) = LPT_ADDR2(59). A(13) = LPT_ADDR2(61). A(17) = LPT_ADDR3(49). BA(0:1) = LPT_ADDR4(48:49). BG(0:1) = LPT_ADDR4(50:51). All other register bit positions are reserved.

Register Name	SEQ Low Power Termination Address 2 Register
Mnemonic	IOM0.DDRPHY_SEQ_LPT_ADDR2_P3
Address	8000C41707011C3F (SCOM)
Description	This register corresponds to the SEQ Reserved Address {2-4} Register for DDR4 bit mapping.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	LPT_ADDR2: The bit positions and mapping of the bit positions to the Address/BA/BG pins in DDR4 of the SEQ Low Power Termination Address{2-4} Registers correspond to the bit positions and mapping of the bit positions to the Address/BA/BG pins in the SEQ Reserved Address{2-4} registers. The content of these registers that corresponds to: BA(0:1), BG(0), A(0:9), A(11), A(13), A(17), BG(1) is driven onto the Address/BA/BG pins during idle bus cycles during periodic calibration. Register bits within these registers that correspond to Address/BA/BG not listed above are reserved. A(0:9) = LPT_ADDR2(48:57). A(11) = LPT_ADDR2(59). A(13) = LPT_ADDR2(61). A(17) = LPT_ADDR3(49). BA(0:1) = LPT_ADDR4(48:49). BG(0:1) = LPT_ADDR4(50:51). All other register bit positions are reserved.

Register Name	SEQ Low Power Termination Address 3 Register
Mnemonic	IOM0.DDRPHY_SEQ_LPT_ADDR3_P0
Address	8000C4180701103F (SCOM)
Description	This register corresponds to the SEQ Reserved Address {2-4} Register for DDR4 bit mapping.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	LPT_ADDR3: The bit positions and mapping of the bit positions to the Address/BA/BG pins in DDR4 of the SEQ Low Power Termination Address{2-4} Registers correspond to the bit positions and mapping of the bit positions to the Address/BA/BG pins in the SEQ Reserved Address{2-4} registers. The content of these registers that corresponds to: BA(0:1), BG(0), A(0:9), A(11), A(13), A(17), BG(1) is driven onto the Address/BA/BG pins during idle bus cycles during periodic calibration. Register bits within these registers that correspond to Address/BA/BG not listed above are reserved. A(0:9) = LPT_ADDR2(48:57). A(11) = LPT_ADDR2(59). A(13) = LPT_ADDR2(61). A(17) = LPT_ADDR3(49). BA(0:1) = LPT_ADDR4(48:49). BG(0:1) = LPT_ADDR4(50:51). All other register bit positions are reserved.

Register Name	SEQ Low Power Termination Address 3 Register
Mnemonic	IOM0.DDRPHY_SEQ_LPT_ADDR3_P1
Address	8000C4180701143F (SCOM)
Description	This register corresponds to the SEQ Reserved Address {2-4} Register for DDR4 bit mapping.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	LPT_ADDR3: The bit positions and mapping of the bit positions to the Address/BA/BG pins in DDR4 of the SEQ Low Power Termination Address{2-4} Registers correspond to the bit positions and mapping of the bit positions to the Address/BA/BG pins in the SEQ Reserved Address{2-4} registers. The content of these registers that corresponds to: BA(0:1), BG(0), A(0:9), A(11), A(13), A(17), BG(1) is driven onto the Address/BA/BG pins during idle bus cycles during periodic calibration. Register bits within these registers that correspond to Address/BA/BG not listed above are reserved. A(0:9) = LPT_ADDR2(48:57). A(11) = LPT_ADDR2(59). A(13) = LPT_ADDR2(61). A(17) = LPT_ADDR3(49). BA(0:1) = LPT_ADDR4(48:49). BG(0:1) = LPT_ADDR4(50:51). All other register bit positions are reserved.

Register Name	SEQ Low Power Termination Address 3 Register
Mnemonic	IOM0.DDRPHY_SEQ_LPT_ADDR3_P2
Address	8000C4180701183F (SCOM)
Description	This register corresponds to the SEQ Reserved Address {2-4} Register for DDR4 bit mapping.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	LPT_ADDR3: The bit positions and mapping of the bit positions to the Address/BA/BG pins in DDR4 of the SEQ Low Power Termination Address{2-4} Registers correspond to the bit positions and mapping of the bit positions to the Address/BA/BG pins in the SEQ Reserved Address{2-4} registers. The content of these registers that corresponds to: BA(0:1), BG(0), A(0:9), A(11), A(13), A(17), BG(1) is driven onto the Address/BA/BG pins during idle bus cycles during periodic calibration. Register bits within these registers that correspond to Address/BA/BG not listed above are reserved. A(0:9) = LPT_ADDR2(48:57). A(11) = LPT_ADDR2(59). A(13) = LPT_ADDR2(61). A(17) = LPT_ADDR3(49). BA(0:1) = LPT_ADDR4(48:49). BG(0:1) = LPT_ADDR4(50:51). All other register bit positions are reserved.

Register Name	SEQ Low Power Termination Address 3 Register
Mnemonic	IOM0.DDRPHY_SEQ_LPT_ADDR3_P3
Address	8000C41807011C3F (SCOM)
Description	This register corresponds to the SEQ Reserved Address {2-4} Register for DDR4 bit mapping.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48:63	RW	LPT_ADDR3: The bit positions and mapping of the bit positions to the Address/BA/BG pins in DDR4 of the SEQ Low Power Termination Address{2-4} Registers correspond to the bit positions and mapping of the bit positions to the Address/BA/BG pins in the SEQ Reserved Address{2-4} registers. The content of these registers that corresponds to: BA(0:1), BG(0), A(0:9), A(11), A(13), A(17), BG(1) is driven onto the Address/BA/BG pins during idle bus cycles during periodic calibration. Register bits within these registers that correspond to Address/BA/BG not listed above are reserved. A(0:9) = LPT_ADDR2(48:57). A(11) = LPT_ADDR2(59). A(13) = LPT_ADDR2(61). A(17) = LPT_ADDR3(49). BA(0:1) = LPT_ADDR4(48:49). BG(0:1) = LPT_ADDR4(50:51). All other register bit positions are reserved.

Register Name	SEQ Low Power Termination Address 4 Register
Mnemonic	IOM0.DDRPHY_SEQ_LPT_ADDR4_P0
Address	8000C4190701103F (SCOM)
Description	This register corresponds to the SEQ Reserved Address {2-4} Register for DDR4 bit mapping.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	LPT_ADDR4: The bit positions and mapping of the bit positions to the Address/BA/BG pins in DDR4 of the SEQ Low Power Termination Address{2-4} Registers correspond to the bit positions and mapping of the bit positions to the Address/BA/BG pins in the SEQ Reserved Address{2-4} registers. The content of these registers that corresponds to: BA(0:1), BG(0), A(0:9), A(11), A(13), A(17), BG(1) is driven onto the Address/BA/BG pins during idle bus cycles during periodic calibration. Register bits within these registers that correspond to Address/BA/BG not listed above are reserved. A(0:9) = LPT_ADDR2(48:57). A(11) = LPT_ADDR2(59). A(13) = LPT_ADDR2(61). A(17) = LPT_ADDR3(49). BA(0:1) = LPT_ADDR4(48:49). BG(0:1) = LPT_ADDR4(50:51). All other register bit positions are reserved.

Register Name	SEQ Low Power Termination Address 4 Register
Mnemonic	IOM0.DDRPHY_SEQ_LPT_ADDR4_P1
Address	8000C4190701143F (SCOM)
Description	This register corresponds to the SEQ Reserved Address {2-4} Register for DDR4 bit mapping.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	LPT_ADDR4: The bit positions and mapping of the bit positions to the Address/BA/BG pins in DDR4 of the SEQ Low Power Termination Address{2-4} Registers correspond to the bit positions and mapping of the bit positions to the Address/BA/BG pins in the SEQ Reserved Address{2-4} registers. The content of these registers that corresponds to: BA(0:1), BG(0), A(0:9), A(11), A(13), A(17), BG(1) is driven onto the Address/BA/BG pins during idle bus cycles during periodic calibration. Register bits within these registers that correspond to Address/BA/BG not listed above are reserved. A(0:9) = LPT_ADDR2(48:57). A(11) = LPT_ADDR2(59). A(13) = LPT_ADDR2(61). A(17) = LPT_ADDR3(49). BA(0:1) = LPT_ADDR4(48:49). BG(0:1) = LPT_ADDR4(50:51). All other register bit positions are reserved.

Register Name	SEQ Low Power Termination Address 4 Register
Mnemonic	IOM0.DDRPHY_SEQ_LPT_ADDR4_P2
Address	8000C4190701183F (SCOM)
Description	This register corresponds to the SEQ Reserved Address {2-4} Register for DDR4 bit mapping.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	LPT_ADDR4: The bit positions and mapping of the bit positions to the Address/BA/BG pins in DDR4 of the SEQ Low Power Termination Address{2-4} Registers correspond to the bit positions and mapping of the bit positions to the Address/BA/BG pins in the SEQ Reserved Address{2-4} registers. The content of these registers that corresponds to: BA(0:1), BG(0), A(0:9), A(11), A(13), A(17), BG(1) is driven onto the Address/BA/BG pins during idle bus cycles during periodic calibration. Register bits within these registers that correspond to Address/BA/BG not listed above are reserved. A(0:9) = LPT_ADDR2(48:57). A(11) = LPT_ADDR2(59). A(13) = LPT_ADDR2(61). A(17) = LPT_ADDR3(49). BA(0:1) = LPT_ADDR4(48:49). BG(0:1) = LPT_ADDR4(50:51). All other register bit positions are reserved.

Register Name	SEQ Low Power Termination Address 4 Register
Mnemonic	IOM0.DDRPHY_SEQ_LPT_ADDR4_P3
Address	8000C41907011C3F (SCOM)
Description	This register corresponds to the SEQ Reserved Address {2-4} Register for DDR4 bit mapping.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48:63	RW	LPT_ADDR4: The bit positions and mapping of the bit positions to the Address/BA/BG pins in DDR4 of the SEQ Low Power Termination Address{2-4} Registers correspond to the bit positions and mapping of the bit positions to the Address/BA/BG pins in the SEQ Reserved Address{2-4} registers. The content of these registers that corresponds to: BA(0:1), BG(0), A(0:9), A(11), A(13), A(17), BG(1) is driven onto the Address/BA/BG pins during idle bus cycles during periodic calibration. Register bits within these registers that correspond to Address/BA/BG not listed above are reserved. A(0:9) = LPT_ADDR2(48:57). A(11) = LPT_ADDR2(59). A(13) = LPT_ADDR2(61). A(17) = LPT_ADDR3(49). BA(0:1) = LPT_ADDR4(48:49). BG(0:1) = LPT_ADDR4(50:51). All other register bit positions are reserved.

Register Name	SEQ ZQCal Encoded Rank Control 0 Register
Mnemonic	IOM0.DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG0_P0
Address	8000C41A0701103F (SCOM)
Description	This register modifies the external I/O impedance calibration (ZQCal) execution performed by the SEQ state machine. The SEQ ZQCal Encoded Rank Control 0 Register contains the configuration for rank groups 0 and 1. The SEQ ZQCal Encoded Rank Control 1 Register contains the configuration for rank groups 2 and 3.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48	RW	ZQCAL_ENC_0: 1 = Enable dual ZQCal for rank group {0,2}.

Bits	SCOM	Field Mnemonic: Description
49	RW	ZQCAL_SEL_TYPE_0: 0 = The encoded chip select (CS) bit for ZQCal is on an inverted chip select (CSN). 1 = The encoded CS bit for ZQCal is on an ODT.
50:52	RW	Reserved.
53:55	RW	ZQCAL_SEL_0: Selects which CSN or ODT is used for the CS bit for ZQCal on rank group {0,2}.
56	RW	ZQCAL_ENC_1: 1 = Enable dual ZQCal for rank group {1,3}.
57	RW	ZQCAL_SEL_TYPE_1: 0 = The encoded CS bit for ZQCal is on a CSN. 1 = The encoded CS bit for ZQCal is on an ODT.
58:60	RW	Reserved.
61:63	RW	ZQCAL_SEL_1: Selects which CSN or ODT is used for the CS bit for ZQCal on rank group {1,3}.

Register Name	SEQ ZQCal Encoded Rank Control 0 Register
Mnemonic	IOM0.DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG0_P1
Address	8000C41A0701143F (SCOM)
Description	This register modifies the external ZQCal execution performed by the SEQ state machine. The SEQ ZQCal Encoded Rank Control 0 Register contains the configuration for rank groups 0 and 1. The SEQ ZQCal Encoded Rank Control 1 Register contains the configuration for rank groups 2 and 3.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	ZQCAL_ENC_0: 1 = Enable dual ZQCal for rank group {0,2}.
49	RW	ZQCAL_SEL_TYPE_0: 0 = The encoded CS bit for ZQCal is on a CSN. 1 = The encoded CS bit for ZQCal is on an ODT.
50:52	RW	Reserved.
53:55	RW	ZQCAL_SEL_0: Selects which CSN or ODT is used for the CS bit for ZQCal on rank group {0,2}.
56	RW	ZQCAL_ENC_1: 1 = Enable dual ZQCal for rank group {1,3}.
57	RW	ZQCAL_SEL_TYPE_1: 0 = The encoded CS bit for ZQCal is on a CSN. 1 = The encoded CS bit for ZQCal is on an ODT.
58:60	RW	Reserved.
61:63	RW	ZQCAL_SEL_1: Selects which CSN or ODT is used for the CS bit for ZQCal on rank group {1,3}.

Register Name	SEQ ZQCal Encoded Rank Control 0 Register
Mnemonic	IOM0.DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG0_P2
Address	8000C41A0701183F (SCOM)
Description	This register modifies the external ZQCal execution performed by the SEQ state machine. The SEQ ZQCal Encoded Rank Control 0 Register contains the configuration for rank groups 0 and 1. The SEQ ZQCal Encoded Rank Control 1 Register contains the configuration for rank groups 2 and 3.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	ZQCAL_ENC_0: 1 = Enable dual ZQCal for rank group {0,2}.
49	RW	ZQCAL_SEL_TYPE_0: 0 = The encoded CS bit for ZQCal is on a CSN. 1 = The encoded CS bit for ZQCal is on an ODT.
50:52	RW	Reserved.
53:55	RW	ZQCAL_SEL_0: Selects which CSN or ODT is used for the CS bit for ZQCal on rank group {0,2}.
56	RW	ZQCAL_ENC_1: 1 = Enable dual ZQCal for rank group {1,3}.
57	RW	ZQCAL_SEL_TYPE_1: 0 = The encoded CS bit for ZQCal is on a CSN. 1 = The encoded CS bit for ZQCal is on an ODT.
58:60	RW	Reserved.
61:63	RW	ZQCAL_SEL_1: Selects which CSN or ODT is used for the CS bit for ZQCal on rank group {1,3}.

Register Name	SEQ ZQCal Encoded Rank Control 0 Register
Mnemonic	IOM0.DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG0_P3
Address	8000C41A07011C3F (SCOM)
Description	This register modifies the external ZQCal execution performed by the SEQ state machine. The SEQ ZQCal Encoded Rank Control 0 Register contains the configuration for rank groups 0 and 1. The SEQ ZQCal Encoded Rank Control 1 Register contains the configuration for rank groups 2 and 3.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	ZQCAL_ENC_0: 1 = Enable dual ZQCal for rank group {0,2}.
49	RW	ZQCAL_SEL_TYPE_0: 0 = The encoded CS bit for ZQCal is on a CSN. 1 = The encoded CS bit for ZQCal is on an ODT.
50:52	RW	Reserved.
53:55	RW	ZQCAL_SEL_0: Selects which CSN or ODT is used for the CS bit for ZQCal on rank group {0,2}.
56	RW	ZQCAL_ENC_1: 1 = Enable dual ZQCal for rank group {1,3}.
57	RW	ZQCAL_SEL_TYPE_1: 0 = The encoded CS bit for ZQCal is on a CSN. 1 = The encoded CS bit for ZQCal is on an ODT.
58:60	RW	Reserved.
61:63	RW	ZQCAL_SEL_1: Selects which CSN or ODT is used for the CS bit for ZQCal on rank group {1,3}.

Register Name	SEQ ZQCal Encoded Rank Control 1 Register
Mnemonic	IOM0.DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG1_P0
Address	8000C41B0701103F (SCOM)
Description	This register modifies the external ZQCal execution performed by the SEQ state machine. The SEQ ZQCal Encoded Rank Control 0 Register contains the configuration for rank groups 0 and 1. The SEQ ZQCal Encoded Rank Control 1 Register contains the configuration for rank groups 2 and 3.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	ZQCAL_ENC_2: 1 = Enable dual ZQCal for rank group {0,2}.
49	RW	ZQCAL_SEL_TYPE_2: 0 = The encoded CS bit for ZQCal is on a CSN. 1 = The encoded CS bit for ZQCal is on an ODT.
50:52	RW	Reserved.
53:55	RW	ZQCAL_SEL_2: Selects which CSN or ODT is used for the CS bit for ZQCal on rank group {0,2}.
56	RW	ZQCAL_ENC_3: 1 = Enable dual ZQCal for rank group {1,3}.
57	RW	ZQCAL_SEL_TYPE_3: 0 = The encoded CS bit for ZQCal is on a CSN. 1 = The encoded CS bit for ZQCal is on an ODT.
58:60	RW	Reserved.
61:63	RW	ZQCAL_SEL_3: Selects which CSN or ODT is used for the CS bit for ZQCal on rank group {1,3}.

Register Name	SEQ ZQCal Encoded Rank Control 1 Register
Mnemonic	IOM0.DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG1_P1
Address	8000C41B0701143F (SCOM)
Description	This register modifies the external ZQCal execution performed by the SEQ state machine. The SEQ ZQCal Encoded Rank Control 0 Register contains the configuration for rank groups 0 and 1. The SEQ ZQCal Encoded Rank Control 1 Register contains the configuration for rank groups 2 and 3.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	ZQCAL_ENC_2: 1 = Enable dual ZQCal for rank group {0,2}.
49	RW	ZQCAL_SEL_TYPE_2: 0 = The encoded CS bit for ZQCal is on a CSN. 1 = The encoded CS bit for ZQCal is on an ODT.
50:52	RW	Reserved.
53:55	RW	ZQCAL_SEL_2: Selects which CSN or ODT is used for the CS bit for ZQCal on rank group {0,2}.
56	RW	ZQCAL_ENC_3: 1 = Enable dual ZQCal for rank group {1,3}.
57	RW	ZQCAL_SEL_TYPE_3: 0 = The encoded CS bit for ZQCal is on a CSN. 1 = The encoded CS bit for ZQCal is on an ODT.
58:60	RW	Reserved.

Bits	SCOM	Field Mnemonic: Description
61:63	RW	ZQCAL_SEL_3: Selects which CSN or ODT is used for the CS bit for ZQCal on rank group {1,3}.

Register Name	SEQ ZQCal Encoded Rank Control 1 Register
Mnemonic	IOM0.DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG1_P2
Address	8000C41B0701183F (SCOM)
Description	This register modifies the external ZQCal execution performed by the SEQ state machine. The SEQ ZQCal Encoded Rank Control 0 Register contains the configuration for rank groups 0 and 1. The SEQ ZQCal Encoded Rank Control 1 Register contains the configuration for rank groups 2 and 3.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	ZQCAL_ENC_2: 1 = Enable dual ZQCal for rank group {0,2}.
49	RW	ZQCAL_SEL_TYPE_2: 0 = The encoded CS bit for ZQCal is on a CSN. 1 = The encoded CS bit for ZQCal is on an ODT.
50:52	RW	Reserved.
53:55	RW	ZQCAL_SEL_2: Selects which CSN or ODT is used for the CS bit for ZQCal on rank group {0,2}.
56	RW	ZQCAL_ENC_3: 1 = Enable dual ZQCal for rank group {1,3}.
57	RW	ZQCAL_SEL_TYPE_3: 0 = The encoded CS bit for ZQCal is on a CSN. 1 = The encoded CS bit for ZQCal is on an ODT.
58:60	RW	Reserved.
61:63	RW	ZQCAL_SEL_3: Selects which CSN or ODT is used for the CS bit for ZQCal on rank group {1,3}.

Register Name	SEQ ZQCal Encoded Rank Control 1 Register
Mnemonic	IOM0.DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG1_P3
Address	8000C41B07011C3F (SCOM)
Description	This register modifies the external ZQCal execution performed by the SEQ state machine. The SEQ ZQCal Encoded Rank Control 0 Register contains the configuration for rank groups 0 and 1. The SEQ ZQCal Encoded Rank Control 1 Register contains the configuration for rank groups 2 and 3.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	ZQCAL_ENC_2: 1 = Enable dual ZQCal for rank group {0,2}.
49	RW	ZQCAL_SEL_TYPE_2: 0 = The encoded CS bit for ZQCal is on a CSN. 1 = The encoded CS bit for ZQCal is on an ODT.
50:52	RW	Reserved.
53:55	RW	ZQCAL_SEL_2: Selects which CSN or ODT is used for the CS bit for ZQCal on rank group {0,2}.
56	RW	ZQCAL_ENC_3: 1 = Enable dual ZQCal for rank group {1,3}.

Bits	SCOM	Field Mnemonic: Description
57	RW	ZQCAL_SEL_TYPE_3: 0 = The encoded CS bit for ZQCal is on a CSN. 1 = The encoded CS bit for ZQCal is on an ODT.
58:60	RW	Reserved.
61:63	RW	ZQCAL_SEL_3: Selects which CSN or ODT is used for the CS bit for ZQCal on rank group {1,3}.

Register Name	SEQ RTT Write Term Swap 0 Register
Mnemonic	IOM0.DDRPHY_SEQ_WR_TERM_SWAP0_P0
Address	8000C41D0701103F (SCOM)
Description	This register contains the conversion from RTT_WR settings to RTT_NOM settings corresponding to JEDEC Mode Register settings.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	RTT_WR0_NOM_VALUE: Value for RTT_NOM if RTT_WR contains a 0 value: bit 48 → A10. bit 49 → A9. bit 50 → A8.
51:53	RW	RTT_WR1_NOM_VALUE: Value for RTT_NOM if RTT_WR contains a 1 value: bit 51 → A10. bit 52 → A9. bit 53 → A8.
54:56	RW	RTT_WR2_NOM_VALUE: Value for RTT_NOM if RTT_WR contains a 2 value: bit 54 → A10. bit 55 → A9. bit 56 → A8.
57:59	RW	RTT_WR3_NOM_VALUE: Value for RTT_NOM if RTT_WR contains a 3 value: bit 57 → A10. bit 58 → A9. bit 59 → A8.
60:62	RW	RTT_WR4_NOM_VALUE: Value for RTT_NOM if RTT_WR contains a 4 value: bit 60 → A10. bit 61 → A9. bit 62 → A8.
63	RW	DD2_WR_VREF_FIX_DISABLE: 0 = Enable the DD2 function for the write reference voltage (VREF) algorithm. 1 = Enable the DD1 function.

Register Name	SEQ RTT Write Term Swap 0 Register
Mnemonic	IOM0.DDRPHY_SEQ_WR_TERM_SWAP0_P1
Address	8000C41D0701143F (SCOM)
Description	This register contains the conversion from RTT_WR settings to RTT_NOM settings corresponding to JEDEC Mode Register settings.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RW	RTT_WR0_NOM_VALUE: Value for RTT_NOM if RTT_WR contains a 0 value: bit 48 → A10. bit 49 → A9. bit 50 → A8.
51:53	RW	RTT_WR1_NOM_VALUE: Value for RTT_NOM if RTT_WR contains a 1 value: bit 51 → A10. bit 52 → A9. bit 53 → A8.
54:56	RW	RTT_WR2_NOM_VALUE: Value for RTT_NOM if RTT_WR contains a 2 value: bit 54 → A10. bit 55 → A9. bit 56 → A8.
57:59	RW	RTT_WR3_NOM_VALUE: Value for RTT_NOM if RTT_WR contains a 3 value: bit 57 → A10. bit 58 → A9. bit 59 → A8.
60:62	RW	RTT_WR4_NOM_VALUE: Value for RTT_NOM if RTT_WR contains a 4 value: bit 60 → A10. bit 61 → A9. bit 62 → A8.
63	RW	DD2_WR_VREF_FIX_DISABLE: 0 = Enable the DD2 function for the write VREF algorithm. 1 = Enable the DD1 function.

Register Name	SEQ RTT Write Term Swap 0 Register
Mnemonic	IOM0.DDRPHY_SEQ_WR_TERM_SWAP0_P2
Address	8000C41D0701183F (SCOM)
Description	This register contains the conversion from RTT_WR settings to RTT_NOM settings corresponding to JEDEC Mode Register settings.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	RTT_WR0_NOM_VALUE: Value for RTT_NOM if RTT_WR contains a 0 value: bit 48 → A10. bit 49 → A9. bit 50 → A8.
51:53	RW	RTT_WR1_NOM_VALUE: Value for RTT_NOM if RTT_WR contains a 1 value: bit 51 → A10. bit 52 → A9. bit 53 → A8.
54:56	RW	RTT_WR2_NOM_VALUE: Value for RTT_NOM if RTT_WR contains a 2 value: bit 54 → A10. bit 55 → A9. bit 56 → A8.
57:59	RW	RTT_WR3_NOM_VALUE: Value for RTT_NOM if RTT_WR contains a 3 value: bit 57 → A10. bit 58 → A9. bit 59 → A8.

Bits	SCOM	Field Mnemonic: Description
60:62	RW	RTT_WR4_NOM_VALUE: Value for RTT_NOM if RTT_WR contains a 4 value: bit 60 → A10. bit 61 → A9. bit 62 → A8.
63	RW	DD2_WR_VREF_FIX_DISABLE: 0 = Enable the DD2 function for the write VREF algorithm. 1 = Enable the DD1 function.

Register Name	SEQ RTT Write Term Swap 0 Register
Mnemonic	IOM0.DDRPHY_SEQ_WR_TERM_SWAP0_P3
Address	8000C41D07011C3F (SCOM)
Description	This register contains the conversion from RTT_WR settings to RTT_NOM settings corresponding to JEDEC Mode Register settings.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	RTT_WR0_NOM_VALUE: Value for RTT_NOM if RTT_WR contains a 0 value: bit 48 → A10. bit 49 → A9. bit 50 → A8.
51:53	RW	RTT_WR1_NOM_VALUE: Value for RTT_NOM if RTT_WR contains a 1 value: bit 51 → A10. bit 52 → A9. bit 53 → A8.
54:56	RW	RTT_WR2_NOM_VALUE: Value for RTT_NOM if RTT_WR contains a 2 value: bit 54 → A10. bit 55 → A9. bit 56 → A8.
57:59	RW	RTT_WR3_NOM_VALUE: Value for RTT_NOM if RTT_WR contains a 3 value: bit 57 → A10. bit 58 → A9. bit 59 → A8.
60:62	RW	RTT_WR4_NOM_VALUE: Value for RTT_NOM if RTT_WR contains a 4 value: bit 60 → A10. bit 61 → A9. bit 62 → A8.
63	RW	DD2_WR_VREF_FIX_DISABLE: 0 = Enable the DD2 function for the write VREF algorithm. 1 = Enable the DD1 function.

Register Name	SEQ RTT Write Term Swap 1 Register
Mnemonic	IOM0.DDRPHY_SEQ_WR_TERM_SWAP1_P0
Address	8000C41E0701103F (SCOM)
Description	This register contains the conversion from RTT_WR settings to RTT_NOM settings corresponding to JEDEC Mode Register settings.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	RTT_WR5_NOM_VALUE: Value for RTT_NOM if RTT_WR contains a 5 value: bit 48 → A10. bit 49 → A9. bit 50 → A8.
51:53	RW	RTT_WR6_NOM_VALUE: Value for RTT_NOM if RTT_WR contains a 6 value: bit 51 → A10. bit 52 → A9. bit 52 → A8.
54:56	RW	RTT_WR7_NOM_VALUE: Value for RTT_NOM if RTT_WR contains a 7 value: bit 54 → A10. bit 55 → A9. bit 56 → A8.
57:63	RW	Reserved.

Register Name	SEQ RTT Write Term Swap 1 Register
Mnemonic	IOM0.DDRPHY_SEQ_WR_TERM_SWAP1_P1
Address	8000C41E0701143F (SCOM)
Description	This register contains the conversion from RTT_WR settings to RTT_NOM settings corresponding to JEDEC Mode Register settings.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	RTT_WR5_NOM_VALUE: Value for RTT_NOM if RTT_WR contains a 5 value: bit 48 → A10. bit 49 → A9. bit 50 → A8.
51:53	RW	RTT_WR6_NOM_VALUE: Value for RTT_NOM if RTT_WR contains a 6 value: bit 51 → A10. bit 52 → A9. bit 52 → A8.
54:56	RW	RTT_WR7_NOM_VALUE: Value for RTT_NOM if RTT_WR contains a 7 value: bit 54 → A10. bit 55 → A9. bit 56 → A8.
57:63	RW	Reserved.

Register Name	SEQ RTT Write Term Swap 1 Register
Mnemonic	IOM0.DDRPHY_SEQ_WR_TERM_SWAP1_P2
Address	8000C41E0701183F (SCOM)
Description	This register contains the conversion from RTT_WR settings to RTT_NOM settings corresponding to JEDEC Mode Register settings.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RW	RTT_WR5_NOM_VALUE: Value for RTT_NOM if RTT_WR contains a 5 value: bit 48 → A10. bit 49 → A9. bit 50 → A8.
51:53	RW	RTT_WR6_NOM_VALUE: Value for RTT_NOM if RTT_WR contains a 6 value: bit 51 → A10. bit 52 → A9. bit 52 → A8.
54:56	RW	RTT_WR7_NOM_VALUE: Value for RTT_NOM if RTT_WR contains a 7 value: bit 54 → A10. bit 55 → A9. bit 56 → A8.
57:63	RW	Reserved.

Register Name	SEQ RTT Write Term Swap 1 Register
Mnemonic	IOM0.DDRPHY_SEQ_WR_TERM_SWAP1_P3
Address	8000C41E07011C3F (SCOM)
Description	This register contains the conversion from RTT_WR settings to RTT_NOM settings corresponding to JEDEC Mode Register settings.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	RTT_WR5_NOM_VALUE: Value for RTT_NOM if RTT_WR contains a 5 value: bit 48 → A10. bit 49 → A9. bit 50 → A8.
51:53	RW	RTT_WR6_NOM_VALUE: Value for RTT_NOM if RTT_WR contains a 6 value: bit 51 → A10. bit 52 → A9. bit 52 → A8.
54:56	RW	RTT_WR7_NOM_VALUE: Value for RTT_NOM if RTT_WR contains a 7 value: bit 54 → A10. bit 55 → A9. bit 56 → A8.
57:63	RW	Reserved.

Register Name	SEQ ODT Default Configuration Register
Mnemonic	IOM0.DDRPHY_SEQ_ODT_DEFAULT_CONFIG_P0
Address	8000C4240701103F (SCOM)
Description	This register determines the ODT values sent to all ranks during MRS commands.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	ODT_DEF_VALUES: The four ODT values in this register are driven to the ODT pins during MRS commands. Typically, the ODT value must be set to all zeros during MRS commands. Where: bit 0 = ODT value for ODT pin 0 during MRS command. bit 1 = ODT value for ODT pin 1 during MRS command. bit 2 = ODT value for ODT pin 2 during MRS command. bit 3 = ODT value for ODT pin 3 during MRS command.
52:63	RW	Reserved.

Register Name	SEQ ODT Default Configuration Register
Mnemonic	IOM0.DDRPHY_SEQ_ODT_DEFAULT_CONFIG_P1
Address	8000C4240701143F (SCOM)
Description	This register determines the ODT values sent to all ranks during MRS commands.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:51	RW	ODT_DEF_VALUES: The four ODT values in this register are driven to the ODT pins during MRS commands. Typically, the ODT value must be set to all zeros during MRS commands. Where: bit 0 = ODT value for ODT pin 0 during MRS command. bit 1 = ODT value for ODT pin 1 during MRS command. bit 2 = ODT value for ODT pin 2 during MRS command. bit 3 = ODT value for ODT pin 3 during MRS command.
52:63	RW	Reserved.

Register Name	SEQ ODT Default Configuration Register
Mnemonic	IOM0.DDRPHY_SEQ_ODT_DEFAULT_CONFIG_P2
Address	8000C4240701183F (SCOM)
Description	This register determines the ODT values sent to all ranks during MRS commands.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:51	RW	ODT_DEF_VALUES: The four ODT values in this register are driven to the ODT pins during MRS commands. Typically, the ODT value must be set to all zeros during MRS commands. Where: bit 0 = ODT value for ODT pin 0 during MRS command. bit 1 = ODT value for ODT pin 1 during MRS command. bit 2 = ODT value for ODT pin 2 during MRS command. bit 3 = ODT value for ODT pin 3 during MRS command.
52:63	RW	Reserved.

Register Name	SEQ ODT Default Configuration Register
Mnemonic	IOM0.DDRPHY_SEQ_ODT_DEFAULT_CONFIG_P3
Address	8000C42407011C3F (SCOM)
Description	This register determines the ODT values sent to all ranks during MRS commands.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:51	RW	ODT_DEF_VALUES: The four ODT values in this register are driven to the ODT pins during MRS commands. Typically, the ODT value must be set to all zeros during MRS commands. Where: bit 0 = ODT value for ODT pin 0 during MRS command. bit 1 = ODT value for ODT pin 1 during MRS command. bit 2 = ODT value for ODT pin 2 during MRS command. bit 3 = ODT value for ODT pin 3 during MRS command.
52:63	RW	Reserved.

10. DDRPHY: WC Registers

This section contains the registers located in the write control (WC) logic. The WC registers are listed alphabetically by mnemonic in the following address table.

The WC registers are listed in the following tables.

Register Name	WC Configuration 0 Register
Mnemonic	IOM0.DDRPHY_WC_CONFIG0_P0
Address	8000CC000701103F (SCOM)
Description	This register contains global configuration information to control the write control logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:55	RW	TWLO_TWLOE: This field contains the number of memory clock cycles that equal: 12 + {The greater of (tWLDQSEN - tMOD) converted to and rounded up to the nearest integer number of memory clock cycles or (tWLO + tWLOE) converted to and rounded up to the nearest integer number of memory clock cycles.} + {The longest DQS wire delay converted to and rounded up to the nearest integer number of memory clock cycles.} + {The longest DQ wire delay converted to and rounded up to the nearest integer number of memory clock cycles.}. This field is used during write leveling.
56	RW	WL_ONE_DQS_PULSE: 0 = Continuous data strobe (DQS) pulses during write leveling. Thirty-two continuous pulses are sent. 1 = One DQS pulse during each write-leveling adjustment.
57:62	RW	FW_WR_RD: This field contains the number of memory clock cycles to wait between the write and read command pairs during write centering.
63	RW	CUSTOM_INIT_WRITE: 1 = Write the data pattern in the SEQ Read/Write Data {0-1} Registers during the initial-pattern-write algorithm. 0 = Write the MPR-like pattern defined by the MPR_PATTERN_BIT field in the SEQ Configuration 0 Register during the initial-pattern-write algorithm.

Register Name	WC Configuration 0 Register
Mnemonic	IOM0.DDRPHY_WC_CONFIG0_P1
Address	8000CC000701143F (SCOM)
Description	This register contains global configuration information to control the write control logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:55	RW	TWLO_TWLOE: This field contains the number of memory clock cycles that equal: 12 + {The greater of (tWLDQSEN - tMOD) converted to and rounded up to the nearest integer number of memory clock cycles or (tWLO + tWLOE) converted to and rounded up to the nearest integer number of memory clock cycles.} + {The longest DQS wire delay converted to and rounded up to the nearest integer number of memory clock cycles.} + {The longest DQ wire delay converted to and rounded up to the nearest integer number of memory clock cycles.}. This field is used during write leveling.
56	RW	WL_ONE_DQS_PULSE: 0 = Continuous DQS pulses during write leveling. Thirty-two continuous pulses are sent. 1 = One DQS pulse during each write-leveling adjustment.
57:62	RW	FW_WR_RD: This field contains the number of memory clock cycles to wait between the write and read command pairs during write centering.

Bits	SCOM	Field Mnemonic: Description
63	RW	CUSTOM_INIT_WRITE: 1 = Write the data pattern in the SEQ Read/Write Data {0-1} Registers during the initial-pattern-write algorithm. 0 = Write the MPR-like pattern defined by the MPR_PATTERN_BIT field in the SEQ Configuration 0 Register during the initial-pattern-write algorithm.

Register Name	WC Configuration 0 Register
Mnemonic	IOM0.DDRPHY_WC_CONFIG0_P2
Address	8000CC000701183F (SCOM)
Description	This register contains global configuration information to control the write control logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:55	RW	TWLO_TWLOE: This field contains the number of memory clock cycles that equal: 12 + {The greater of (tWLDQSEN - tMOD) converted to and rounded up to the nearest integer number of memory clock cycles or (tWLO + tWLOE) converted to and rounded up to the nearest integer number of memory clock cycles.} + {The longest DQS wire delay converted to and rounded up to the nearest integer number of memory clock cycles.} + {The longest DQ wire delay converted to and rounded up to the nearest integer number of memory clock cycles.}. This field is used during write leveling.
56	RW	WL_ONE_DQS_PULSE: 0 = Continuous DQS pulses during write leveling. Thirty-two continuous pulses are sent. 1 = One DQS pulse during each write-leveling adjustment.
57:62	RW	FW_WR_RD: This field contains the number of memory clock cycles to wait between the write and read command pairs during write centering.
63	RW	CUSTOM_INIT_WRITE: 1 = Write the data pattern in the SEQ Read/Write Data {0-1} Registers during the initial-pattern-write algorithm. 0 = Write the MPR-like pattern defined by the MPR_PATTERN_BIT field in the SEQ Configuration 0 Register during the initial-pattern-write algorithm.

Register Name	WC Configuration 0 Register
Mnemonic	IOM0.DDRPHY_WC_CONFIG0_P3
Address	8000CC0007011C3F (SCOM)
Description	This register contains global configuration information to control the write control logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	TWLO_TWLOE: This field contains the number of memory clock cycles that equal: 12 + {The greater of (tWLDQSEN - tMOD) converted to and rounded up to the nearest integer number of memory clock cycles or (tWLO + tWLOE) converted to and rounded up to the nearest integer number of memory clock cycles.} + {The longest DQS wire delay converted to and rounded up to the nearest integer number of memory clock cycles.} + {The longest DQ wire delay converted to and rounded up to the nearest integer number of memory clock cycles.}. This field is used during write leveling.
56	RW	WL_ONE_DQS_PULSE: 0 = Continuous DQS pulses during write leveling. Thirty-two continuous pulses are sent. 1 = One DQS pulse during each write-leveling adjustment.
57:62	RW	FW_WR_RD: This field contains the number of memory clock cycles to wait between the write and read command pairs during write centering.
63	RW	CUSTOM_INIT_WRITE: 1 = Write the data pattern in the SEQ Read/Write Data {0-1} Registers during the initial-pattern-write algorithm. 0 = Write the MPR-like pattern defined by the MPR_PATTERN_BIT field in the SEQ Configuration 0 Register during the initial-pattern-write algorithm.

Register Name	**WC Configuration 1 Register**
Mnemonic	IOM0.DDRPHY_WC_CONFIG1_P0
Address	8000CC010701103F (SCOM)
Description	This register contains global configuration information to control the write control logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48:51	RW	BIG_STEP: This field indicates the amount the phase rotator value is adjusted during a big step in the write-leveling and write-centering algorithms. The amount of the adjustment is (BIG_STEP + 1) / 128th of a memory clock.
52:54	RW	SMALL_STEP: This field indicates the amount the phase rotator value is adjusted during a small step in the write-leveling and write-centering algorithms. The amount of the adjustment is (SMALL_STEP + 1) / 128th of a memory clock. **Note:** The write-leveling and write-centering algorithms achieve the most accurate results when this field is set to zero.
55:60	RW	WR_PRE_DLY: This field indicates the number of dphy_gckn cycles between a write command and a precharge command in the coarse initial-pattern-write, initial-write, and write-centering calibration algorithms. This value has a range limitation of 0:63. For 2666 Mbps speeds and beyond, 63 might not be a sufficient delay. The range of the delay can be extended by using the DD2_WR_PRE_DLY_EXT bit in the PC Resets Register.
61:63	RO	Constant = 0b000

Register Name	**WC Configuration 1 Register**
Mnemonic	IOM0.DDRPHY_WC_CONFIG1_P1
Address	8000CC010701143F (SCOM)
Description	This register contains global configuration information to control the write control logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	BIG_STEP: This field indicates the amount the phase rotator value is adjusted during a big step in the write-leveling and write-centering algorithms. The amount of the adjustment is (BIG_STEP + 1) / 128th of a memory clock.
52:54	RW	SMALL_STEP: This field indicates the amount the phase rotator value is adjusted during a small step in the write-leveling and write-centering algorithms. The amount of the adjustment is (SMALL_STEP + 1) / 128th of a memory clock. **Note:** The write-leveling and write-centering algorithms achieve the most accurate results when this field is set to zero.
55:60	RW	WR_PRE_DLY: This field indicates the number of dphy_gckn cycles between a write command and a precharge command in the coarse initial-pattern-write, initial-write, and write-centering calibration algorithms. This value has a range limitation of 0:63. For 2666 Mbps speeds and beyond, 63 might not be a sufficient delay. The range of the delay can be extended by using the DD2_WR_PRE_DLY_EXT bit in the PC Resets Register.
61:63	RO	Constant = 0b000

Register Name	WC Configuration 1 Register
Mnemonic	IOM0.DDRPHY_WC_CONFIG1_P2
Address	8000CC010701183F (SCOM)
Description	This register contains global configuration information to control the write control logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	BIG_STEP: This field indicates the amount the phase rotator value is adjusted during a big step in the write-leveling and write-centering algorithms. The amount of the adjustment is (BIG_STEP + 1) / 128th of a memory clock.
52:54	RW	SMALL_STEP: This field indicates the amount the phase rotator value is adjusted during a small step in the write-leveling and write-centering algorithms. The amount of the adjustment is (SMALL_STEP + 1) / 128th of a memory clock. **Note:** The write-leveling and write-centering algorithms achieve the most accurate results when this field is set to zero.
55:60	RW	WR_PRE_DLY: This field indicates the number of dphy_gckn cycles between a write command and a precharge command in the coarse initial-pattern-write, initial-write, and write-centering calibration algorithms. This value has a range limitation of 0:63. For 2666 Mbps speeds and beyond, 63 might not be a sufficient delay. The range of the delay can be extended by using the DD2_WR_PRE_DLY_EXT bit in the PC Resets Register.
61:63	RO	Constant = 0b000

Register Name	WC Configuration 1 Register
Mnemonic	IOM0.DDRPHY_WC_CONFIG1_P3
Address	8000CC0107011C3F (SCOM)
Description	This register contains global configuration information to control the write control logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	BIG_STEP: This field indicates the amount the phase rotator value is adjusted during a big step in the write-leveling and write-centering algorithms. The amount of the adjustment is (BIG_STEP + 1) / 128th of a memory clock.
52:54	RW	SMALL_STEP: This field indicates the amount the phase rotator value is adjusted during a small step in the write-leveling and write-centering algorithms. The amount of the adjustment is (SMALL_STEP + 1) / 128th of a memory clock. **Note:** The write-leveling and write-centering algorithms achieve the most accurate results when this field is set to zero.
55:60	RW	WR_PRE_DLY: This field indicates the number of dphy_gckn cycles between a write command and a precharge command in the coarse initial-pattern-write, initial-write, and write-centering calibration algorithms. This value has a range limitation of 0:63. For 2666 Mbps speeds and beyond, 63 might not be a sufficient delay. The range of the delay can be extended by using the DD2_WR_PRE_DLY_EXT bit in the PC Resets Register.
61:63	RO	Constant = 0b000

Register Name	**WC Configuration 2 Register**
Mnemonic	IOM0.DDRPHY_WC_CONFIG2_P0
Address	8000CC020701103F (SCOM)
Description	This register contains global configuration information to control the write control logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	NUM_VALID_SAMPLES: The write-leveling and write-centering algorithms require NUM_VALID_SAMPLES + 1 samples at one delay to determine that the delay setting returns valid data. One invalid sample at any time causes an invalid sample. The write-leveling algorithm performs the second-to-last sample at the current sample point plus 1/2 unit interval (UI) to ensure that the current sample point is at the 0b-to-1b transition. **Caution:** The minimum value for this field is 2.
52:57	RW	FW_RD_WR: This delay value is used in two places in the write-centering algorithm. This value sets the delay between a read and write command in memory clock cycles. This value must be a minimum of 11 plus the spacing required by DDR4. For example, DDR4 specifies this spacing as tWTR. The second place this delay value is used is to set the delay between the read and the precharge command in memory clock cycles. This value must be a minimum of 3 plus the spacing required by DDR4. For example, DDR4 specifies this spacing as additive latency (AL) + tRTP. This field must be set to the larger of the two values in number of memory clock cycles. FW_RD_WR = max(tWTR + 11, AL + tRTP + 3).
58:61	RW	IPW_WR_WR: This delay value is used to separate write commands during an initial pattern write. When writing a pattern to DDR4 MPRs, this must be set to meet tWR_MPR. Otherwise, this should be set to 0h. The number of clock cycles between write commands is (IPW_WR_WR + 1) x 4.
62	RW	CDD2_FIX_DIS: 0 = Enable the POWER8 DD2 function. 1 = Enable the POWER8 DD1 function.
63	RW	EN_RESET_WR_DELAY_WL: 1 = The DP16 Write Delay Value {0-23} Registers are reset at the start of the write-leveling calibration algorithm for rank pair 0. 0 = The DP16 Write Delay Value {0-23} Registers are not reset at the start of the write-leveling calibration algorithm.

Register Name	WC Configuration 2 Register
Mnemonic	IOM0.DDRPHY_WC_CONFIG2_P1
Address	8000CC020701143F (SCOM)
Description	This register contains global configuration information to control the write control logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	NUM_VALID_SAMPLES: The write-leveling and write-centering algorithms require NUM_VALID_SAMPLES + 1 samples at one delay to determine that the delay setting returns valid data. One invalid sample at any time causes an invalid sample. The write-leveling algorithm performs the second-to-last sample at the current sample point plus 1/2 UI to ensure that the current sample point is at the 0b-to-1b transition. **Caution:** The minimum value for this field is 2.
52:57	RW	FW_RD_WR: This delay value is used in two places in the write-centering algorithm. This value sets the delay between a read and write command in memory clock cycles. This value must be a minimum of 11 plus the spacing required by DDR4. For example, DDR4 specifies this spacing as tWTR. The second place this delay value is used is to set the delay between the read and the precharge command in memory clock cycles. This value must be a minimum of 3 plus the spacing required by DDR4. For example, DDR4 specifies this spacing as additive latency (AL) + tRTP. This field must be set to the larger of the two values in number of memory clock cycles. FW_RD_WR = max(tWTR + 11, AL + tRTP + 3).
58:61	RW	IPW_WR_WR: This delay value is used to separate write commands during an initial pattern write. When writing a pattern to DDR4 MPRs, this must be set to meet tWR_MPR. Otherwise, this should be set to 0h. The number of clock cycles between write commands is (IPW_WR_WR + 1) x 4.
62	RW	CDD2_FIX_DIS: 0 = Enable the POWER8 DD2 function. 1 = Enable the POWER8 DD1 function.
63	RW	EN_RESET_WR_DELAY_WL: 1 = The DP16 Write Delay Value {0-23} Registers are reset at the start of the write-leveling calibration algorithm for rank pair 0. 0 = The DP16 Write Delay Value {0-23} Registers are not reset at the start of the write-leveling calibration algorithm.

Register Name	WC Configuration 2 Register
Mnemonic	IOM0.DDRPHY_WC_CONFIG2_P2
Address	8000CC020701183F (SCOM)
Description	This register contains global configuration information to control the write control logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	NUM_VALID_SAMPLES: The write-leveling and write-centering algorithms require NUM_VALID_SAMPLES + 1 samples at one delay to determine that the delay setting returns valid data. One invalid sample at any time causes an invalid sample. The write-leveling algorithm performs the second-to-last sample at the current sample point plus 1/2 UI to ensure that the current sample point is at the 0b-to-1b transition. **Caution:** The minimum value for this field is 2.

Bits	SCOM	Field Mnemonic: Description
52:57	RW	FW_RD_WR: This delay value is used in two places in the write-centering algorithm. This value sets the delay between a read and write command in memory clock cycles. This value must be a minimum of 11 plus the spacing required by DDR4. For example, DDR4 specifies this spacing as tWTR. The second place this delay value is used is to set the delay between the read and the precharge command in memory clock cycles. This value must be a minimum of 3 plus the spacing required by DDR4. For example, DDR4 specifies this spacing as additive latency (AL) + tRTP. This field must be set to the larger of the two values in number of memory clock cycles. FW_RD_WR = max(tWTR + 11, AL + tRTP + 3).
58:61	RW	IPW_WR_WR: This delay value is used to separate write commands during an initial pattern write. When writing a pattern to DDR4 MPRs, this must be set to meet tWR_MPR. Otherwise, this should be set to 0h. The number of clock cycles between write commands is (IPW_WR_WR + 1) x 4.
62	RW	CDD2_FIX_DIS: 0 = Enable the POWER8 DD2 function. 1 = Enable the POWER8 DD1 function.
63	RW	EN_RESET_WR_DELAY_WL: 1 = The DP16 Write Delay Value {0-23} Registers are reset at the start of the write-leveling calibration algorithm for rank pair 0. 0 = The DP16 Write Delay Value {0-23} Registers are not reset at the start of the write-leveling calibration algorithm.

Register Name	**WC Configuration 2 Register**
Mnemonic	IOM0.DDRPHY_WC_CONFIG2_P3
Address	8000CC0207011C3F (SCOM)
Description	This register contains global configuration information to control the write control logic.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	NUM_VALID_SAMPLES: The write-leveling and write-centering algorithms require NUM_VALID_SAMPLES + 1 samples at one delay to determine that the delay setting returns valid data. One invalid sample at any time causes an invalid sample. The write-leveling algorithm performs the second-to-last sample at the current sample point plus 1/2 UI to ensure that the current sample point is at the 0b-to-1b transition. **Caution:** The minimum value for this field is 2.
52:57	RW	FW_RD_WR: This delay value is used in two places in the write-centering algorithm. This value sets the delay between a read and write command in memory clock cycles. This value must be a minimum of 11 plus the spacing required by DDR4. For example, DDR4 specifies this spacing as tWTR. The second place this delay value is used is to set the delay between the read and the precharge command in memory clock cycles. This value must be a minimum of 3 plus the spacing required by DDR4. For example, DDR4 specifies this spacing as additive latency (AL) + tRTP. This field must be set to the larger of the two values in number of memory clock cycles. FW_RD_WR = max(tWTR + 11, AL + tRTP + 3).
58:61	RW	IPW_WR_WR: This delay value is used to separate write commands during an initial pattern write. When writing a pattern to DDR4 MPRs, this must be set to meet tWR_MPR. Otherwise, this should be set to 0h. The number of clock cycles between write commands is (IPW_WR_WR + 1) x 4.
62	RW	CDD2_FIX_DIS: 0 = Enable the POWER8 DD2 function. 1 = Enable the POWER8 DD1 function.

Bits	SCOM	Field Mnemonic: Description
63	RW	EN_RESET_WR_DELAY_WL: 1 = The DP16 Write Delay Value {0-23} Registers are reset at the start of the write-leveling calibration algorithm for rank pair 0. 0 = The DP16 Write Delay Value {0-23} Registers are not reset at the start of the write-leveling calibration algorithm.

Register Name	**WC Error Status 0 Register**
Mnemonic	IOM0.DDRPHY_WC_ERROR_STATUS0_P0
Address	8000CC030701103F (SCOM)
Description	This register contains error information about the write control logic. It contains composite error information from the DP16 logic block that is about write calibration algorithms. Before writing this register to ‘0’b, DDRPHY_DP16_WR_ERROR0, if set, must be written to ‘0’b.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	WR_CNTL_ERROR: 1 = Write control error. See the DP16 Write Error 0 Register for more information.
49:63	RO	Constant = 0b000000000000000

Register Name	**WC Error Status 0 Register**
Mnemonic	IOM0.DDRPHY_WC_ERROR_STATUS0_P1
Address	8000CC030701143F (SCOM)
Description	This register contains error information about the write control logic. It contains composite error information from the DP16 logic block that is about write calibration algorithms. Before writing this register to ‘0’b, DDRPHY_DP16_WR_ERROR0, if set, must be written to ‘0’b.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	WR_CNTL_ERROR: 1 = Write control error. See the DP16 Write Error 0 Register for more information.
49:63	RO	Constant = 0b000000000000000

Register Name	**WC Error Status 0 Register**
Mnemonic	IOM0.DDRPHY_WC_ERROR_STATUS0_P2
Address	8000CC030701183F (SCOM)
Description	This register contains error information about the write control logic. It contains composite error information from the DP16 logic block that is about write calibration algorithms. Before writing this register to ‘0’b, DDRPHY_DP16_WR_ERROR0, if set, must be written to ‘0’b.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	WR_CNTL_ERROR: 1 = Write control error. See the DP16 Write Error 0 Register for more information.
49:63	RO	Constant = 0b000000000000000

Register Name	WC Error Status 0 Register
Mnemonic	IOM0.DDRPHY_WC_ERROR_STATUS0_P3
Address	8000CC0307011C3F (SCOM)
Description	This register contains error information about the write control logic. It contains composite error information from the DP16 logic block that is about write calibration algorithms. Before writing this register to ‘0’b, DDRPHY_DP16_WR_ERROR0, if set, must be written to ‘0’b.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	RW	WR_CNTL_ERROR: 1 = Write control error. See the DP16 Write Error 0 Register for more information.
49:63	RO	Constant = 0b000000000000000

Register Name	WC Error Mask 0 Register
Mnemonic	IOM0.DDRPHY_WC_ERROR_MASK0_P0
Address	8000CC040701103F (SCOM)
Description	This register masks errors in the WC Error Status 0 Register. It prevents the WC_ERROR bit from being set in the PC Error Status 0 Register and the appropriate bit from being set in PC Initial Calibration Error Register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	RW	WR_CNTL_ERROR_MASK: 1 = Mask WR_CNTL_ERROR.
49:63	RO	Constant = 0b000000000000000

Register Name	WC Error Mask 0 Register
Mnemonic	IOM0.DDRPHY_WC_ERROR_MASK0_P1
Address	8000CC040701143F (SCOM)
Description	This register masks errors in the WC Error Status 0 Register. It prevents the WC_ERROR bit from being set in the PC Error Status 0 Register and the appropriate bit from being set in PC Initial Calibration Error Register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	RW	WR_CNTL_ERROR_MASK: 1 = Mask WR_CNTL_ERROR.
49:63	RO	Constant = 0b000000000000000

Register Name	WC Error Mask 0 Register
Mnemonic	IOM0.DDRPHY_WC_ERROR_MASK0_P2
Address	8000CC040701183F (SCOM)
Description	This register masks errors in the WC Error Status 0 Register. It prevents the WC_ERROR bit from being set in the PC Error Status 0 Register and the appropriate bit from being set in PC Initial Calibration Error Register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	WR_CNTL_ERROR_MASK: 1 = Mask WR_CNTL_ERROR.
49:63	RO	Constant = 0b000000000000000

Register Name	WC Error Mask 0 Register
Mnemonic	IOM0.DDRPHY_WC_ERROR_MASK0_P3
Address	8000CC0407011C3F (SCOM)
Description	This register masks errors in the WC Error Status 0 Register. It prevents the WC_ERROR bit from being set in the PC Error Status 0 Register and the appropriate bit from being set in PC Initial Calibration Error Register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	WR_CNTL_ERROR_MASK: 1 = Mask WR_CNTL_ERROR.
49:63	RO	Constant = 0b000000000000000

Register Name	WC Configuration 3 Register
Mnemonic	IOM0.DDRPHY_WC_CONFIG3_P0
Address	8000CC050701103F (SCOM)
Description	This register contains global configuration information to control per DRAM address (PDA) mode MRS commands. The DQ and DQS are required to be driven in PDA mode. This register must be set to enable driving DQ/DQS (for DDR4), and to start and stop driving DQ/DQS such that timing expectations of the JEDEC standard are met at the DRAM. **Note:** PHY logic can only track one MRS PDA command at a time. The minimum spacing between MRS commands is MRS_CMD_DQ_ON + MRS_CMD_DQ_OFF + 8 when this mode is used.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	PDA_RANKDELAY_ENABLE: This bit enables the use of rank-pair-specific calibrated delays. It must be set to 1 when using PDA.
49:54	RW	MRS_CMD_DQ_ON: MRS_CMD_DQ_ON determines the WL_per_DRAM_addr time. It is used for both PDA and PBA modes. WL_per_DRAM_addr = 8 + MRS_CMD_DQ_ON memory clock cycles in 2:1 mode. The PHY starts to drive I/O after WL_per_DRAM_addr cycles, as measured from the MRS command. The value that must be programmed for MRS_CMD_DQ_ON is determined by the latencies programmed in the DRAM Mode Registers as well as the Write Latency Offset in the PC Configuration 1 Register. The cycle on which I/O is driven is independent of the DP16 Write Delay Value {0-23} Registers. Therefore, it might be necessary to pad when the I/O turns on/off to account for wire delays.

Bits	SCOM	Field Mnemonic: Description
55:60	RW	MRS_CMD_DQ_OFF is the number of memory clock cycles that the write DQ/DQS are driven after MRS_CMD_DQ_ON before returning to high impedance. It is used for both PDA and PBA modes.
61:63	RO	Constant = 0b000

Register Name	WC Configuration 3 Register
Mnemonic	IOM0.DDRPHY_WC_CONFIG3_P1
Address	8000CC050701143F (SCOM)
Description	This register contains global configuration information to control per DRAM address (PDA) mode MRS commands. The DQ and DQS are required to be driven in PDA mode. This register must be set to enable driving DQ/DQS (for DDR4), and to start and stop driving DQ/DQS such that timing expectations of the JEDEC standard are met at the DRAM. **Note:** PHY logic can only track one MRS PDA command at a time. The minimum spacing between MRS commands is MRS_CMD_DQ_ON + MRS_CMD_DQ_OFF + 8 when this mode is used.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	PDA_RANKDELAY_ENABLE: This bit enables the use of rank-pair-specific calibrated delays. It must be set to 1 when using PDA.
49:54	RW	MRS_CMD_DQ_ON: MRS_CMD_DQ_ON determines the WL_per_DRAM_addr time. It is used for both PDA and PBA modes. WL_per_DRAM_addr = 8 + MRS_CMD_DQ_ON memory clock cycles in 2:1 mode. The PHY starts to drive I/O after WL_per_DRAM_addr cycles, as measured from the MRS command. The value that must be programmed for MRS_CMD_DQ_ON is determined by the latencies programmed in the DRAM Mode Registers as well as the Write Latency Offset in the PC Configuration 1 Register. The cycle on which I/O is driven is independent of the DP16 Write Delay Value {0-23} Registers. Therefore, it might be necessary to pad when the I/O turns on/off to account for wire delays.
55:60	RW	MRS_CMD_DQ_OFF is the number of memory clock cycles that the write DQ/DQS are driven after MRS_CMD_DQ_ON before returning to high impedance. It is used for both PDA and PBA modes.
61:63	RO	Constant = 0b000

Register Name	WC Configuration 3 Register
Mnemonic	IOM0.DDRPHY_WC_CONFIG3_P2
Address	8000CC050701183F (SCOM)
Description	This register contains global configuration information to control per DRAM address (PDA) mode MRS commands. The DQ and DQS are required to be driven in PDA mode. This register must be set to enable driving DQ/DQS (for DDR4), and to start and stop driving DQ/DQS such that timing expectations of the JEDEC standard are met at the DRAM. **Note:** PHY logic can only track one MRS PDA command at a time. The minimum spacing between MRS commands is MRS_CMD_DQ_ON + MRS_CMD_DQ_OFF + 8 when this mode is used.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	PDA_RANKDELAY_ENABLE: This bit enables the use of rank-pair-specific calibrated delays. It must be set to 1 when using PDA.

Bits	SCOM	Field Mnemonic: Description
49:54	RW	MRS_CMD_DQ_ON: MRS_CMD_DQ_ON determines the WL_per_DRAM_addr time. It is used for both PDA and PBA modes. WL_per_DRAM_addr = 8 + MRS_CMD_DQ_ON memory clock cycles in 2:1 mode. The PHY starts to drive I/O after WL_per_DRAM_addr cycles, as measured from the MRS command. The value that must be programmed for MRS_CMD_DQ_ON is determined by the latencies programmed in the DRAM Mode Registers as well as the Write Latency Offset in the PC Configuration 1 Register. The cycle on which I/O is driven is independent of the DP16 Write Delay Value {0-23} Registers. Therefore, it might be necessary to pad when the I/O turns on/off to account for wire delays.
55:60	RW	MRS_CMD_DQ_OFF is the number of memory clock cycles that the write DQ/DQS are driven after MRS_CMD_DQ_ON before returning to high impedance. It is used for both PDA and PBA modes.
61:63	RO	Constant = 0b000

Register Name	WC Configuration 3 Register
Mnemonic	IOM0.DDRPHY_WC_CONFIG3_P3
Address	8000CC0507011C3F (SCOM)
Description	This register contains global configuration information to control per DRAM address (PDA) mode MRS commands. The DQ and DQS are required to be driven in PDA mode. This register must be set to enable driving DQ/DQS (for DDR4), and to start and stop driving DQ/DQS such that timing expectations of the JEDEC standard are met at the DRAM. **Note:** PHY logic can only track one MRS PDA command at a time. The minimum spacing between MRS commands is MRS_CMD_DQ_ON + MRS_CMD_DQ_OFF + 8 when this mode is used.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	PDA_RANKDELAY_ENABLE: This bit enables the use of rank-pair-specific calibrated delays. It must be set to 1 when using PDA.
49:54	RW	MRS_CMD_DQ_ON: MRS_CMD_DQ_ON determines the WL_per_DRAM_addr time. It is used for both PDA and PBA modes. WL_per_DRAM_addr = 8 + MRS_CMD_DQ_ON memory clock cycles in 2:1 mode. The PHY starts to drive I/O after WL_per_DRAM_addr cycles, as measured from the MRS command. The value that must be programmed for MRS_CMD_DQ_ON is determined by the latencies programmed in the DRAM Mode Registers as well as the Write Latency Offset in the PC Configuration 1 Register. The cycle on which I/O is driven is independent of the DP16 Write Delay Value {0-23} Registers. Therefore, it might be necessary to pad when the I/O turns on/off to account for wire delays.
55:60	RW	MRS_CMD_DQ_OFF is the number of memory clock cycles that the write DQ/DQS are driven after MRS_CMD_DQ_ON before returning to high impedance. It is used for both PDA and PBA modes.
61:63	RO	Constant = 0b000

Register Name	WC RTT Write Swap Enable Register
Mnemonic	IOM0.DDRPHY_WC_RTT_WR_SWAP_ENABLE_P0
Address	8000CC060701103F (SCOM)
Description	This register enables hardware mode switches, allowing for RTT_WR to be swapped into RTT_NOM for PDA in write centering or for write leveling.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RW	WL_ENABLE_RTT_SWAP: This bit enables the swapping of RTT_WR values into RTT_NOM for the write-leveling calibration step.
49	RW	WR_CTR_ENABLE_RTT_SWAP: This bit enables the swapping of RTT_WR values into RTT_NOM for the write-centering VREF calibration step before and after VREF changes.
50:59	RW	WR_CTR_VREF_COUNTER_RESET_VAL: This field resets the VREF wait state counter to a predefined user value. This must be computed according to the JEDEC time of the VREF wait divided by the command clock time.
60:63	RO	Constant = 0b0000

Register Name	**WC RTT Write Swap Enable Register**
Mnemonic	IOM0.DDRPHY_WC_RTT_WR_SWAP_ENABLE_P1
Address	8000CC060701143F (SCOM)
Description	This register enables hardware mode switches, allowing for RTT_WR to be swapped into RTT_NOM for PDA in write centering or for write leveling.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	WL_ENABLE_RTT_SWAP: This bit enables the swapping of RTT_WR values into RTT_NOM for the write-leveling calibration step.
49	RW	WR_CTR_ENABLE_RTT_SWAP: This bit enables the swapping of RTT_WR values into RTT_NOM for the write-centering VREF calibration step before and after VREF changes.
50:59	RW	WR_CTR_VREF_COUNTER_RESET_VAL: This field resets the VREF wait state counter to a predefined user value. This must be computed according to the JEDEC time of the VREF wait divided by the command clock time.
60:63	RO	Constant = 0b0000

Register Name	**WC RTT Write Swap Enable Register**
Mnemonic	IOM0.DDRPHY_WC_RTT_WR_SWAP_ENABLE_P2
Address	8000CC060701183F (SCOM)
Description	This register enables hardware mode switches, allowing for RTT_WR to be swapped into RTT_NOM for PDA in write centering or for write leveling.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	WL_ENABLE_RTT_SWAP: This bit enables the swapping of RTT_WR values into RTT_NOM for the write-leveling calibration step.
49	RW	WR_CTR_ENABLE_RTT_SWAP: This bit enables the swapping of RTT_WR values into RTT_NOM for the write-centering VREF calibration step before and after VREF changes.
50:59	RW	WR_CTR_VREF_COUNTER_RESET_VAL: This field resets the VREF wait state counter to a predefined user value. This must be computed according to the JEDEC time of the VREF wait divided by the command clock time.
60:63	RO	Constant = 0b0000

Register Name	WC RTT Write Swap Enable Register
Mnemonic	IOM0.DDRPHY_WC_RTT_WR_SWAP_ENABLE_P3
Address	8000CC0607011C3F (SCOM)
Description	This register enables hardware mode switches, allowing for RTT_WR to be swapped into RTT_NOM for PDA in write centering or for write leveling.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	WL_ENABLE_RTT_SWAP: This bit enables the swapping of RTT_WR values into RTT_NOM for the write-leveling calibration step.
49	RW	WR_CTR_ENABLE_RTT_SWAP: This bit enables the swapping of RTT_WR values into RTT_NOM for the write-centering VREF calibration step before and after VREF changes.
50:59	RW	WR_CTR_VREF_COUNTER_RESET_VAL: This field resets the VREF wait state counter to a predefined user value. This must be computed according to the JEDEC time of the VREF wait divided by the command clock time.
60:63	RO	Constant = 0b0000

11. DDRPHY: DP16 Registers

This section contains the addressable registers in data path 16 (DP16). The DP16 registers are listed alphabetically by mnemonic in the following address table.

Mnemonic	Address	Page
IOM0.DDRPHY_DP16_DELAY_LINE_PWR_CTL_P1_[n]	0x8000006F0701143F	1217
IOM0.DDRPHY_DP16_DELAY_LINE_PWR_CTL_P2_[n]	0x8000006F0701183F	1217
IOM0.DDRPHY_DP16_DELAY_LINE_PWR_CTL_P3_[n]	0x8000006F07011C3F	1217
IOM0.DDRPHY_DP16_DFT_DIG_EYE_P0_[n]	0x800000080701103F	1025
IOM0.DDRPHY_DP16_DFT_DIG_EYE_P1_[n]	0x800000080701143F	1026
IOM0.DDRPHY_DP16_DFT_DIG_EYE_P2_[n]	0x800000080701183F	1026
IOM0.DDRPHY_DP16_DFT_DIG_EYE_P3_[n]	0x8000000807011C3F	1027
IOM0.DDRPHY_DP16_DFT_PDA_CONTROL_P0_[n]	0x800000010701103F	992
IOM0.DDRPHY_DP16_DFT_PDA_CONTROL_P1_[n]	0x800000010701143F	993
IOM0.DDRPHY_DP16_DFT_PDA_CONTROL_P2_[n]	0x800000010701183F	994
IOM0.DDRPHY_DP16_DFT_PDA_CONTROL_P3_[n]	0x8000000107011C3F	995
IOM0.DDRPHY_DP16_DFT_WRAP_STATUS_P0_[n]	0x8000001D0701103F	1073
IOM0.DDRPHY_DP16_DFT_WRAP_STATUS_P1_[n]	0x8000001D0701143F	1074
IOM0.DDRPHY_DP16_DFT_WRAP_STATUS_P2_[n]	0x8000001D0701183F	1074
IOM0.DDRPHY_DP16_DFT_WRAP_STATUS_P3_[n]	0x8000001D07011C3F	1075
IOM0.DDRPHY_DP16_DLL_CNTL0_P0_[n]	0x800000240701103F	1091
IOM0.DDRPHY_DP16_DLL_CNTL0_P1_[n]	0x800000240701143F	1092
IOM0.DDRPHY_DP16_DLL_CNTL0_P2_[n]	0x800000240701183F	1093
IOM0.DDRPHY_DP16_DLL_CNTL0_P3_[n]	0x8000002407011C3F	1094
IOM0.DDRPHY_DP16_DLL_CNTL1_P0_[n]	0x800000250701103F	1095
IOM0.DDRPHY_DP16_DLL_CNTL1_P1_[n]	0x800000250701143F	1096
IOM0.DDRPHY_DP16_DLL_CNTL1_P2_[n]	0x800000250701183F	1097
IOM0.DDRPHY_DP16_DLL_CNTL1_P3_[n]	0x8000002507011C3F	1098
IOM0.DDRPHY_DP16_DLL_CONFIG1_P0_[n]	0x800000770701103F	1229
IOM0.DDRPHY_DP16_DLL_CONFIG1_P1_[n]	0x800000770701143F	1230
IOM0.DDRPHY_DP16_DLL_CONFIG1_P2_[n]	0x800000770701183F	1230
IOM0.DDRPHY_DP16_DLL_CONFIG1_P3_[n]	0x8000007707011C3F	1231
IOM0.DDRPHY_DP16_DLL_DAC_LOWER0_P0_[n]	0x800000260701103F	1099
IOM0.DDRPHY_DP16_DLL_DAC_LOWER0_P1_[n]	0x800000260701143F	1099
IOM0.DDRPHY_DP16_DLL_DAC_LOWER0_P2_[n]	0x800000260701183F	1099
IOM0.DDRPHY_DP16_DLL_DAC_LOWER0_P3_[n]	0x8000002607011C3F	1100
IOM0.DDRPHY_DP16_DLL_DAC_LOWER1_P0_[n]	0x800000270701103F	1100
IOM0.DDRPHY_DP16_DLL_DAC_LOWER1_P1_[n]	0x800000270701143F	1101
IOM0.DDRPHY_DP16_DLL_DAC_LOWER1_P2_[n]	0x800000270701183F	1101
IOM0.DDRPHY_DP16_DLL_DAC_LOWER1_P3_[n]	0x8000002707011C3F	1101
IOM0.DDRPHY_DP16_DLL_DAC_UPPER0_P0_[n]	0x800000280701103F	1102
IOM0.DDRPHY_DP16_DLL_DAC_UPPER0_P1_[n]	0x800000280701143F	1102
IOM0.DDRPHY_DP16_DLL_DAC_UPPER0_P2_[n]	0x800000280701183F	1102
IOM0.DDRPHY_DP16_DLL_DAC_UPPER0_P3_[n]	0x8000002807011C3F	1103
IOM0.DDRPHY_DP16_DLL_DAC_UPPER1_P0_[n]	0x800000290701103F	1103
IOM0.DDRPHY_DP16_DLL_DAC_UPPER1_P1_[n]	0x800000290701143F	1103
IOM0.DDRPHY_DP16_DLL_DAC_UPPER1_P2_[n]	0x800000290701183F	1104
IOM0.DDRPHY_DP16_DLL_DAC_UPPER1_P3_[n]	0x8000002907011C3F	1104

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IOM0.DDRPHY_DP16_DLL_EXTRA0_P0_[n]	0x800000AC0701103F	1269
IOM0.DDRPHY_DP16_DLL_EXTRA0_P1_[n]	0x800000AC0701143F	1269
IOM0.DDRPHY_DP16_DLL_EXTRA0_P2_[n]	0x800000AC0701183F	1270
IOM0.DDRPHY_DP16_DLL_EXTRA0_P3_[n]	0x800000AC07011C3F	1270
IOM0.DDRPHY_DP16_DLL_EXTRA1_P0_[n]	0x800000AD0701103F	1271
IOM0.DDRPHY_DP16_DLL_EXTRA1_P1_[n]	0x800000AD0701143F	1271
IOM0.DDRPHY_DP16_DLL_EXTRA1_P2_[n]	0x800000AD0701183F	1272
IOM0.DDRPHY_DP16_DLL_EXTRA1_P3_[n]	0x800000AD07011C3F	1272
IOM0.DDRPHY_DP16_DLL_SLAVE_VREG_LOWER0_P0_[n]	0x800000A80701103F	1264
IOM0.DDRPHY_DP16_DLL_SLAVE_VREG_LOWER0_P1_[n]	0x800000A80701143F	1264
IOM0.DDRPHY_DP16_DLL_SLAVE_VREG_LOWER0_P2_[n]	0x800000A80701183F	1265
IOM0.DDRPHY_DP16_DLL_SLAVE_VREG_LOWER0_P3_[n]	0x800000A807011C3F	1265
IOM0.DDRPHY_DP16_DLL_SLAVE_VREG_LOWER1_P0_[n]	0x800000A90701103F	1265
IOM0.DDRPHY_DP16_DLL_SLAVE_VREG_LOWER1_P1_[n]	0x800000A90701143F	1266
IOM0.DDRPHY_DP16_DLL_SLAVE_VREG_LOWER1_P2_[n]	0x800000A90701183F	1266
IOM0.DDRPHY_DP16_DLL_SLAVE_VREG_LOWER1_P3_[n]	0x800000A907011C3F	1266
IOM0.DDRPHY_DP16_DLL_SLAVE_VREG_UPPER0_P0_[n]	0x800000AA0701103F	1267
IOM0.DDRPHY_DP16_DLL_SLAVE_VREG_UPPER0_P1_[n]	0x800000AA0701143F	1267
IOM0.DDRPHY_DP16_DLL_SLAVE_VREG_UPPER0_P2_[n]	0x800000AA0701183F	1267
IOM0.DDRPHY_DP16_DLL_SLAVE_VREG_UPPER0_P3_[n]	0x800000AA07011C3F	1267
IOM0.DDRPHY_DP16_DLL_SLAVE_VREG_UPPER1_P0_[n]	0x800000AB0701103F	1268
IOM0.DDRPHY_DP16_DLL_SLAVE_VREG_UPPER1_P1_[n]	0x800000AB0701143F	1268
IOM0.DDRPHY_DP16_DLL_SLAVE_VREG_UPPER1_P2_[n]	0x800000AB0701183F	1268
IOM0.DDRPHY_DP16_DLL_SLAVE_VREG_UPPER1_P3_[n]	0x800000AB07011C3F	1269
IOM0.DDRPHY_DP16_DLL_SW_CONTROL0_P0_[n]	0x800000A60701103F	1256
IOM0.DDRPHY_DP16_DLL_SW_CONTROL0_P1_[n]	0x800000A60701143F	1257
IOM0.DDRPHY_DP16_DLL_SW_CONTROL0_P2_[n]	0x800000A60701183F	1258
IOM0.DDRPHY_DP16_DLL_SW_CONTROL0_P3_[n]	0x800000A607011C3F	1259
IOM0.DDRPHY_DP16_DLL_SW_CONTROL1_P0_[n]	0x800000A70701103F	1260
IOM0.DDRPHY_DP16_DLL_SW_CONTROL1_P1_[n]	0x800000A70701143F	1261
IOM0.DDRPHY_DP16_DLL_SW_CONTROL1_P2_[n]	0x800000A70701183F	1262
IOM0.DDRPHY_DP16_DLL_SW_CONTROL1_P3_[n]	0x800000A707011C3F	1263
IOM0.DDRPHY_DP16_DLL_VREG_COARSE0_P0_[n]	0x8000002C0701103F	1110
IOM0.DDRPHY_DP16_DLL_VREG_COARSE0_P1_[n]	0x8000002C0701143F	1110
IOM0.DDRPHY_DP16_DLL_VREG_COARSE0_P2_[n]	0x8000002C0701183F	1111
IOM0.DDRPHY_DP16_DLL_VREG_COARSE0_P3_[n]	0x8000002C07011C3F	1111
IOM0.DDRPHY_DP16_DLL_VREG_COARSE1_P0_[n]	0x8000002D0701103F	1112
IOM0.DDRPHY_DP16_DLL_VREG_COARSE1_P1_[n]	0x8000002D0701143F	1112
IOM0.DDRPHY_DP16_DLL_VREG_COARSE1_P2_[n]	0x8000002D0701183F	1113
IOM0.DDRPHY_DP16_DLL_VREG_COARSE1_P3_[n]	0x8000002D07011C3F	1113
IOM0.DDRPHY_DP16_DLL_VREG_CONTROL0_P0_[n]	0x8000002A0701103F	1104
IOM0.DDRPHY_DP16_DLL_VREG_CONTROL0_P1_[n]	0x8000002A0701143F	1105
IOM0.DDRPHY_DP16_DLL_VREG_CONTROL0_P2_[n]	0x8000002A0701183F	1106

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IOM0.DDRPHY_DP16_DLL_VREG_CONTROL0_P3_[n]	0x8000002A07011C3F	1106
IOM0.DDRPHY_DP16_DLL_VREG_CONTROL1_P0_[n]	0x8000002B0701103F	1107
IOM0.DDRPHY_DP16_DLL_VREG_CONTROL1_P1_[n]	0x8000002B0701143F	1108
IOM0.DDRPHY_DP16_DLL_VREG_CONTROL1_P2_[n]	0x8000002B0701183F	1108
IOM0.DDRPHY_DP16_DLL_VREG_CONTROL1_P3_[n]	0x8000002B07011C3F	1109
IOM0.DDRPHY_DP16_DQSCLK_OFFSET_P0_[n]	0x800000370701103F	1126
IOM0.DDRPHY_DP16_DQSCLK_OFFSET_P1_[n]	0x800000370701143F	1126
IOM0.DDRPHY_DP16_DQSCLK_OFFSET_P2_[n]	0x800000370701183F	1127
IOM0.DDRPHY_DP16_DQSCLK_OFFSET_P3_[n]	0x8000003707011C3F	1127
IOM0.DDRPHY_DP16_DQSCLK_PR0_RANK_PAIR0_P0_[n]	0x800000300701103F	1116
IOM0.DDRPHY_DP16_DQSCLK_PR0_RANK_PAIR0_P1_[n]	0x800000300701143F	1116
IOM0.DDRPHY_DP16_DQSCLK_PR0_RANK_PAIR0_P2_[n]	0x800000300701183F	1117
IOM0.DDRPHY_DP16_DQSCLK_PR0_RANK_PAIR0_P3_[n]	0x8000003007011C3F	1117
IOM0.DDRPHY_DP16_DQSCLK_PR0_RANK_PAIR1_P0_[n]	0x800001300701103F	1329
IOM0.DDRPHY_DP16_DQSCLK_PR0_RANK_PAIR1_P1_[n]	0x800001300701143F	1330
IOM0.DDRPHY_DP16_DQSCLK_PR0_RANK_PAIR1_P2_[n]	0x800001300701183F	1330
IOM0.DDRPHY_DP16_DQSCLK_PR0_RANK_PAIR1_P3_[n]	0x8000013007011C3F	1331
IOM0.DDRPHY_DP16_DQSCLK_PR0_RANK_PAIR2_P0_[n]	0x800002300701103F	1446
IOM0.DDRPHY_DP16_DQSCLK_PR0_RANK_PAIR2_P1_[n]	0x800002300701143F	1447
IOM0.DDRPHY_DP16_DQSCLK_PR0_RANK_PAIR2_P2_[n]	0x800002300701183F	1447
IOM0.DDRPHY_DP16_DQSCLK_PR0_RANK_PAIR2_P3_[n]	0x8000023007011C3F	1448
IOM0.DDRPHY_DP16_DQSCLK_PR0_RANK_PAIR3_P0_[n]	0x800003300701103F	1563
IOM0.DDRPHY_DP16_DQSCLK_PR0_RANK_PAIR3_P1_[n]	0x800003300701143F	1564
IOM0.DDRPHY_DP16_DQSCLK_PR0_RANK_PAIR3_P2_[n]	0x800003300701183F	1564
IOM0.DDRPHY_DP16_DQSCLK_PR0_RANK_PAIR3_P3_[n]	0x8000033007011C3F	1565
IOM0.DDRPHY_DP16_DQSCLK_PR1_RANK_PAIR0_P0_[n]	0x800000310701103F	1117
IOM0.DDRPHY_DP16_DQSCLK_PR1_RANK_PAIR0_P1_[n]	0x800000310701143F	1118
IOM0.DDRPHY_DP16_DQSCLK_PR1_RANK_PAIR0_P2_[n]	0x800000310701183F	1118
IOM0.DDRPHY_DP16_DQSCLK_PR1_RANK_PAIR0_P3_[n]	0x8000003107011C3F	1119
IOM0.DDRPHY_DP16_DQSCLK_PR1_RANK_PAIR1_P0_[n]	0x800001310701103F	1331
IOM0.DDRPHY_DP16_DQSCLK_PR1_RANK_PAIR1_P1_[n]	0x800001310701143F	1331
IOM0.DDRPHY_DP16_DQSCLK_PR1_RANK_PAIR1_P2_[n]	0x800001310701183F	1332
IOM0.DDRPHY_DP16_DQSCLK_PR1_RANK_PAIR1_P3_[n]	0x8000013107011C3F	1332
IOM0.DDRPHY_DP16_DQSCLK_PR1_RANK_PAIR2_P0_[n]	0x800002310701103F	1448
IOM0.DDRPHY_DP16_DQSCLK_PR1_RANK_PAIR2_P1_[n]	0x800002310701143F	1448
IOM0.DDRPHY_DP16_DQSCLK_PR1_RANK_PAIR2_P2_[n]	0x800002310701183F	1449
IOM0.DDRPHY_DP16_DQSCLK_PR1_RANK_PAIR2_P3_[n]	0x8000023107011C3F	1449
IOM0.DDRPHY_DP16_DQSCLK_PR1_RANK_PAIR3_P0_[n]	0x800003310701103F	1565
IOM0.DDRPHY_DP16_DQSCLK_PR1_RANK_PAIR3_P1_[n]	0x800003310701143F	1565
IOM0.DDRPHY_DP16_DQSCLK_PR1_RANK_PAIR3_P2_[n]	0x800003310701183F	1566
IOM0.DDRPHY_DP16_DQSCLK_PR1_RANK_PAIR3_P3_[n]	0x8000033107011C3F	1566
IOM0.DDRPHY_DP16_DQS_BIT_DISABLE_RP0_P0_[n]	0x8000007D0701103F	1239
IOM0.DDRPHY_DP16_DQS_BIT_DISABLE_RP0_P1_[n]	0x8000007D0701143F	1239

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IOM0.DDRPHY_DP16_DQS_BIT_DISABLE_RP0_P2_[n]	0x8000007D0701183F	1240
IOM0.DDRPHY_DP16_DQS_BIT_DISABLE_RP0_P3_[n]	0x8000007D07011C3F	1241
IOM0.DDRPHY_DP16_DQS_BIT_DISABLE_RP1_P0_[n]	0x8000017D0701103F	1416
IOM0.DDRPHY_DP16_DQS_BIT_DISABLE_RP1_P1_[n]	0x8000017D0701143F	1417
IOM0.DDRPHY_DP16_DQS_BIT_DISABLE_RP1_P2_[n]	0x8000017D0701183F	1418
IOM0.DDRPHY_DP16_DQS_BIT_DISABLE_RP1_P3_[n]	0x8000017D07011C3F	1418
IOM0.DDRPHY_DP16_DQS_BIT_DISABLE_RP2_P0_[n]	0x8000027D0701103F	1533
IOM0.DDRPHY_DP16_DQS_BIT_DISABLE_RP2_P1_[n]	0x8000027D0701143F	1534
IOM0.DDRPHY_DP16_DQS_BIT_DISABLE_RP2_P2_[n]	0x8000027D0701183F	1535
IOM0.DDRPHY_DP16_DQS_BIT_DISABLE_RP2_P3_[n]	0x8000027D07011C3F	1535
IOM0.DDRPHY_DP16_DQS_BIT_DISABLE_RP3_P0_[n]	0x8000037D0701103F	1650
IOM0.DDRPHY_DP16_DQS_BIT_DISABLE_RP3_P1_[n]	0x8000037D0701143F	1651
IOM0.DDRPHY_DP16_DQS_BIT_DISABLE_RP3_P2_[n]	0x8000037D0701183F	1652
IOM0.DDRPHY_DP16_DQS_BIT_DISABLE_RP3_P3_[n]	0x8000037D07011C3F	1652
IOM0.DDRPHY_DP16_DQS_GATE_DELAY_RP0_P0_[n]	0x800000130701103F	1042
IOM0.DDRPHY_DP16_DQS_GATE_DELAY_RP0_P1_[n]	0x800000130701143F	1043
IOM0.DDRPHY_DP16_DQS_GATE_DELAY_RP0_P2_[n]	0x800000130701183F	1044
IOM0.DDRPHY_DP16_DQS_GATE_DELAY_RP0_P3_[n]	0x8000001307011C3F	1044
IOM0.DDRPHY_DP16_DQS_GATE_DELAY_RP1_P0_[n]	0x800001130701103F	1327
IOM0.DDRPHY_DP16_DQS_GATE_DELAY_RP1_P1_[n]	0x800001130701143F	1327
IOM0.DDRPHY_DP16_DQS_GATE_DELAY_RP1_P2_[n]	0x800001130701183F	1328
IOM0.DDRPHY_DP16_DQS_GATE_DELAY_RP1_P3_[n]	0x8000011307011C3F	1329
IOM0.DDRPHY_DP16_DQS_GATE_DELAY_RP2_P0_[n]	0x800002130701103F	1444
IOM0.DDRPHY_DP16_DQS_GATE_DELAY_RP2_P1_[n]	0x800002130701143F	1444
IOM0.DDRPHY_DP16_DQS_GATE_DELAY_RP2_P2_[n]	0x800002130701183F	1445
IOM0.DDRPHY_DP16_DQS_GATE_DELAY_RP2_P3_[n]	0x8000021307011C3F	1446
IOM0.DDRPHY_DP16_DQS_GATE_DELAY_RP3_P0_[n]	0x800003130701103F	1561
IOM0.DDRPHY_DP16_DQS_GATE_DELAY_RP3_P1_[n]	0x800003130701143F	1561
IOM0.DDRPHY_DP16_DQS_GATE_DELAY_RP3_P2_[n]	0x800003130701183F	1562
IOM0.DDRPHY_DP16_DQS_GATE_DELAY_RP3_P3_[n]	0x8000031307011C3F	1563
IOM0.DDRPHY_DP16_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_[n]	0x800000090701103F	1027
IOM0.DDRPHY_DP16_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_[n]	0x800000090701143F	1028
IOM0.DDRPHY_DP16_DQS_RD_PHASE_SELECT_RANK_PAIR0_P2_[n]	0x800000090701183F	1029
IOM0.DDRPHY_DP16_DQS_RD_PHASE_SELECT_RANK_PAIR0_P3_[n]	0x8000000907011C3F	1029
IOM0.DDRPHY_DP16_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_[n]	0x800001090701103F	1320
IOM0.DDRPHY_DP16_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_[n]	0x800001090701143F	1321
IOM0.DDRPHY_DP16_DQS_RD_PHASE_SELECT_RANK_PAIR1_P2_[n]	0x800001090701183F	1322
IOM0.DDRPHY_DP16_DQS_RD_PHASE_SELECT_RANK_PAIR1_P3_[n]	0x8000010907011C3F	1322
IOM0.DDRPHY_DP16_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_[n]	0x800002090701103F	1437
IOM0.DDRPHY_DP16_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_[n]	0x800002090701143F	1438
IOM0.DDRPHY_DP16_DQS_RD_PHASE_SELECT_RANK_PAIR2_P2_[n]	0x800002090701183F	1439
IOM0.DDRPHY_DP16_DQS_RD_PHASE_SELECT_RANK_PAIR2_P3_[n]	0x8000020907011C3F	1439
IOM0.DDRPHY_DP16_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_[n]	0x800003090701103F	1554

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IOM0.DDRPHY_DP16_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_[n]	0x800003090701143F	1555
IOM0.DDRPHY_DP16_DQS_RD_PHASE_SELECT_RANK_PAIR3_P2_[n]	0x800003090701183F	1556
IOM0.DDRPHY_DP16_DQS_RD_PHASE_SELECT_RANK_PAIR3_P3_[n]	0x8000030907011C3F	1556
IOM0.DDRPHY_DP16_DQ_BIT_DISABLE_RP0_P0_[n]	0x8000007C0701103F	1237
IOM0.DDRPHY_DP16_DQ_BIT_DISABLE_RP0_P1_[n]	0x8000007C0701143F	1238
IOM0.DDRPHY_DP16_DQ_BIT_DISABLE_RP0_P2_[n]	0x8000007C0701183F	1238
IOM0.DDRPHY_DP16_DQ_BIT_DISABLE_RP0_P3_[n]	0x8000007C07011C3F	1238
IOM0.DDRPHY_DP16_DQ_BIT_DISABLE_RP1_P0_[n]	0x8000017C0701103F	1415
IOM0.DDRPHY_DP16_DQ_BIT_DISABLE_RP1_P1_[n]	0x8000017C0701143F	1415
IOM0.DDRPHY_DP16_DQ_BIT_DISABLE_RP1_P2_[n]	0x8000017C0701183F	1415
IOM0.DDRPHY_DP16_DQ_BIT_DISABLE_RP1_P3_[n]	0x8000017C07011C3F	1416
IOM0.DDRPHY_DP16_DQ_BIT_DISABLE_RP2_P0_[n]	0x8000027C0701103F	1532
IOM0.DDRPHY_DP16_DQ_BIT_DISABLE_RP2_P1_[n]	0x8000027C0701143F	1532
IOM0.DDRPHY_DP16_DQ_BIT_DISABLE_RP2_P2_[n]	0x8000027C0701183F	1532
IOM0.DDRPHY_DP16_DQ_BIT_DISABLE_RP2_P3_[n]	0x8000027C07011C3F	1533
IOM0.DDRPHY_DP16_DQ_BIT_DISABLE_RP3_P0_[n]	0x8000037C0701103F	1649
IOM0.DDRPHY_DP16_DQ_BIT_DISABLE_RP3_P1_[n]	0x8000037C0701143F	1649
IOM0.DDRPHY_DP16_DQ_BIT_DISABLE_RP3_P2_[n]	0x8000037C0701183F	1649
IOM0.DDRPHY_DP16_DQ_BIT_DISABLE_RP3_P3_[n]	0x8000037C07011C3F	1650
IOM0.DDRPHY_DP16_DQ_BIT_ENABLE0_P0_[n]	0x800000000701103F	990
IOM0.DDRPHY_DP16_DQ_BIT_ENABLE0_P1_[n]	0x800000000701143F	991
IOM0.DDRPHY_DP16_DQ_BIT_ENABLE0_P3_[n]	0x8000000007011C3F	992
IOM0.DDRPHY_DP16_DQ_WR_OFFSET_RP0_P0_[n]	0x8000007E0701103F	1241
IOM0.DDRPHY_DP16_DQ_WR_OFFSET_RP0_P1_[n]	0x8000007E0701143F	1242
IOM0.DDRPHY_DP16_DQ_WR_OFFSET_RP0_P2_[n]	0x8000007E0701183F	1243
IOM0.DDRPHY_DP16_DQ_WR_OFFSET_RP0_P3_[n]	0x8000007E07011C3F	1244
IOM0.DDRPHY_DP16_DQ_WR_OFFSET_RP1_P0_[n]	0x8000017E0701103F	1419
IOM0.DDRPHY_DP16_DQ_WR_OFFSET_RP1_P1_[n]	0x8000017E0701143F	1420
IOM0.DDRPHY_DP16_DQ_WR_OFFSET_RP1_P2_[n]	0x8000017E0701183F	1421
IOM0.DDRPHY_DP16_DQ_WR_OFFSET_RP1_P3_[n]	0x8000017E07011C3F	1422
IOM0.DDRPHY_DP16_DQ_WR_OFFSET_RP2_P0_[n]	0x8000027E0701103F	1536
IOM0.DDRPHY_DP16_DQ_WR_OFFSET_RP2_P1_[n]	0x8000027E0701143F	1537
IOM0.DDRPHY_DP16_DQ_WR_OFFSET_RP2_P2_[n]	0x8000027E0701183F	1538
IOM0.DDRPHY_DP16_DQ_WR_OFFSET_RP2_P3_[n]	0x8000027E07011C3F	1539
IOM0.DDRPHY_DP16_DQ_WR_OFFSET_RP3_P0_[n]	0x8000037E0701103F	1653
IOM0.DDRPHY_DP16_DQ_WR_OFFSET_RP3_P1_[n]	0x8000037E0701143F	1654
IOM0.DDRPHY_DP16_DQ_WR_OFFSET_RP3_P2_[n]	0x8000037E0701183F	1655
IOM0.DDRPHY_DP16_DQ_WR_OFFSET_RP3_P3_[n]	0x8000037E07011C3F	1656
IOM0.DDRPHY_DP16_DRIFT_LIMITS_P0_[n]	0x8000000A0701103F	1030
IOM0.DDRPHY_DP16_DRIFT_LIMITS_P1_[n]	0x8000000A0701143F	1030
IOM0.DDRPHY_DP16_DRIFT_LIMITS_P2_[n]	0x8000000A0701183F	1031
IOM0.DDRPHY_DP16_DRIFT_LIMITS_P3_[n]	0x8000000A07011C3F	1031
IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN0_RANK_PAIR0_P0_[n]	0x8000005C0701103F	1178

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IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN0_RANK_PAIR0_P1_[n]	0x8000005C0701143F	1179
IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN0_RANK_PAIR0_P2_[n]	0x8000005C0701183F	1179
IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN0_RANK_PAIR0_P3_[n]	0x8000005C07011C3F	1179
IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN0_RANK_PAIR1_P0_[n]	0x8000015C0701103F	1383
IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN0_RANK_PAIR1_P1_[n]	0x8000015C0701143F	1383
IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN0_RANK_PAIR1_P2_[n]	0x8000015C0701183F	1384
IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN0_RANK_PAIR1_P3_[n]	0x8000015C07011C3F	1384
IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN0_RANK_PAIR2_P0_[n]	0x8000025C0701103F	1500
IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN0_RANK_PAIR2_P1_[n]	0x8000025C0701143F	1500
IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN0_RANK_PAIR2_P2_[n]	0x8000025C0701183F	1501
IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN0_RANK_PAIR2_P3_[n]	0x8000025C07011C3F	1501
IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN0_RANK_PAIR3_P0_[n]	0x8000035C0701103F	1617
IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN0_RANK_PAIR3_P1_[n]	0x8000035C0701143F	1617
IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN0_RANK_PAIR3_P2_[n]	0x8000035C0701183F	1618
IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN0_RANK_PAIR3_P3_[n]	0x8000035C07011C3F	1618
IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN1_RANK_PAIR0_P0_[n]	0x8000005D0701103F	1180
IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN1_RANK_PAIR0_P1_[n]	0x8000005D0701143F	1180
IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN1_RANK_PAIR0_P2_[n]	0x8000005D0701183F	1181
IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN1_RANK_PAIR0_P3_[n]	0x8000005D07011C3F	1181
IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN1_RANK_PAIR1_P0_[n]	0x8000015D0701103F	1384
IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN1_RANK_PAIR1_P1_[n]	0x8000015D0701143F	1385
IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN1_RANK_PAIR1_P2_[n]	0x8000015D0701183F	1385
IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN1_RANK_PAIR1_P3_[n]	0x8000015D07011C3F	1386
IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN1_RANK_PAIR2_P0_[n]	0x8000025D0701103F	1501
IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN1_RANK_PAIR2_P1_[n]	0x8000025D0701143F	1502
IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN1_RANK_PAIR2_P2_[n]	0x8000025D0701183F	1502
IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN1_RANK_PAIR2_P3_[n]	0x8000025D07011C3F	1503
IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN1_RANK_PAIR3_P0_[n]	0x8000035D0701103F	1618
IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN1_RANK_PAIR3_P1_[n]	0x8000035D0701143F	1619
IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN1_RANK_PAIR3_P2_[n]	0x8000035D0701183F	1619
IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN1_RANK_PAIR3_P3_[n]	0x8000035D07011C3F	1620
IOM0.DDRPHY_DP16_IO_TX_CONFIG0_P0_[n]	0x800000750701103F	1226
IOM0.DDRPHY_DP16_IO_TX_CONFIG0_P1_[n]	0x800000750701143F	1227
IOM0.DDRPHY_DP16_IO_TX_CONFIG0_P2_[n]	0x800000750701183F	1227
IOM0.DDRPHY_DP16_IO_TX_CONFIG0_P3_[n]	0x8000007507011C3F	1227
IOM0.DDRPHY_DP16_IO_TX_FET_SLICE_P0_[n]	0x800000780701103F	1231
IOM0.DDRPHY_DP16_IO_TX_FET_SLICE_P1_[n]	0x800000780701143F	1232
IOM0.DDRPHY_DP16_IO_TX_FET_SLICE_P2_[n]	0x800000780701183F	1232
IOM0.DDRPHY_DP16_IO_TX_FET_SLICE_P3_[n]	0x8000007807011C3F	1233
IOM0.DDRPHY_DP16_IO_TX_PFET_TERM_P0_[n]	0x8000007B0701103F	1236
IOM0.DDRPHY_DP16_IO_TX_PFET_TERM_P1_[n]	0x8000007B0701143F	1236
IOM0.DDRPHY_DP16_IO_TX_PFET_TERM_P2_[n]	0x8000007B0701183F	1236
IOM0.DDRPHY_DP16_IO_TX_PFET_TERM_P3_[n]	0x8000007B07011C3F	1237

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IOM0.DDRPHY_DP16_LO_PROBE_SELECT_P0_[n]	0x800000790701103F	1233
IOM0.DDRPHY_DP16_LO_PROBE_SELECT_P1_[n]	0x800000790701143F	1234
IOM0.DDRPHY_DP16_LO_PROBE_SELECT_P2_[n]	0x800000790701183F	1234
IOM0.DDRPHY_DP16_LO_PROBE_SELECT_P3_[n]	0x8000007907011C3F	1234
IOM0.DDRPHY_DP16_PATTERN_POS_0_P0_[n]	0x800000320701103F	1119
IOM0.DDRPHY_DP16_PATTERN_POS_0_P1_[n]	0x800000320701143F	1120
IOM0.DDRPHY_DP16_PATTERN_POS_0_P2_[n]	0x800000320701183F	1120
IOM0.DDRPHY_DP16_PATTERN_POS_0_P3_[n]	0x8000003207011C3F	1121
IOM0.DDRPHY_DP16_PATTERN_POS_1_P0_[n]	0x800000330701103F	1121
IOM0.DDRPHY_DP16_PATTERN_POS_1_P1_[n]	0x800000330701143F	1122
IOM0.DDRPHY_DP16_PATTERN_POS_1_P2_[n]	0x800000330701183F	1122
IOM0.DDRPHY_DP16_PATTERN_POS_1_P3_[n]	0x8000003307011C3F	1123
IOM0.DDRPHY_DP16_RD_DIA_CONFIG0_P0_[n]	0x8000001E0701103F	1076
IOM0.DDRPHY_DP16_RD_DIA_CONFIG0_P1_[n]	0x8000001E0701143F	1076
IOM0.DDRPHY_DP16_RD_DIA_CONFIG0_P2_[n]	0x8000001E0701183F	1076
IOM0.DDRPHY_DP16_RD_DIA_CONFIG0_P3_[n]	0x8000001E07011C3F	1077
IOM0.DDRPHY_DP16_RD_DIA_CONFIG1_P0_[n]	0x800000350701103F	1123
IOM0.DDRPHY_DP16_RD_DIA_CONFIG1_P1_[n]	0x800000350701143F	1123
IOM0.DDRPHY_DP16_RD_DIA_CONFIG1_P2_[n]	0x800000350701183F	1124
IOM0.DDRPHY_DP16_RD_DIA_CONFIG1_P3_[n]	0x8000003507011C3F	1124
IOM0.DDRPHY_DP16_RD_DIA_CONFIG2_P0_[n]	0x800000360701103F	1124
IOM0.DDRPHY_DP16_RD_DIA_CONFIG2_P1_[n]	0x800000360701143F	1125
IOM0.DDRPHY_DP16_RD_DIA_CONFIG2_P2_[n]	0x800000360701183F	1125
IOM0.DDRPHY_DP16_RD_DIA_CONFIG2_P3_[n]	0x8000003607011C3F	1126
IOM0.DDRPHY_DP16_RD_DIA_CONFIG3_P0_[n]	0x8000006D0701103F	1213
IOM0.DDRPHY_DP16_RD_DIA_CONFIG3_P1_[n]	0x8000006D0701143F	1214
IOM0.DDRPHY_DP16_RD_DIA_CONFIG3_P2_[n]	0x8000006D0701183F	1214
IOM0.DDRPHY_DP16_RD_DIA_CONFIG3_P3_[n]	0x8000006D07011C3F	1215
IOM0.DDRPHY_DP16_RD_DIA_CONFIG4_P0_[n]	0x8000006E0701103F	1215
IOM0.DDRPHY_DP16_RD_DIA_CONFIG4_P1_[n]	0x8000006E0701143F	1215
IOM0.DDRPHY_DP16_RD_DIA_CONFIG4_P2_[n]	0x8000006E0701183F	1216
IOM0.DDRPHY_DP16_RD_DIA_CONFIG4_P3_[n]	0x8000006E07011C3F	1216
IOM0.DDRPHY_DP16_RD_DIA_CONFIG5_P0_[n]	0x800000120701103F	1039
IOM0.DDRPHY_DP16_RD_DIA_CONFIG5_P1_[n]	0x800000120701143F	1040
IOM0.DDRPHY_DP16_RD_DIA_CONFIG5_P2_[n]	0x800000120701183F	1041
IOM0.DDRPHY_DP16_RD_DIA_CONFIG5_P3_[n]	0x8000001207011C3F	1042
IOM0.DDRPHY_DP16_RD_ERROR_MASK0_P0_[n]	0x800000150701103F	1052
IOM0.DDRPHY_DP16_RD_ERROR_MASK0_P1_[n]	0x800000150701143F	1053
IOM0.DDRPHY_DP16_RD_ERROR_MASK0_P2_[n]	0x800000150701183F	1053
IOM0.DDRPHY_DP16_RD_ERROR_MASK0_P3_[n]	0x8000001507011C3F	1054
IOM0.DDRPHY_DP16_RD_LVL_STATUS0_P0_[n]	0x8000000E0701103F	1037
IOM0.DDRPHY_DP16_RD_LVL_STATUS0_P1_[n]	0x8000000E0701143F	1037
IOM0.DDRPHY_DP16_RD_LVL_STATUS0_P2_[n]	0x8000000E0701183F	1038

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IOM0.DDRPHY_DP16_RD_LVL_STATUS0_P3_[n]	0x8000000E07011C3F	1038
IOM0.DDRPHY_DP16_RD_LVL_STATUS2_P0_[n]	0x800000100701103F	1038
IOM0.DDRPHY_DP16_RD_LVL_STATUS2_P1_[n]	0x800000100701143F	1038
IOM0.DDRPHY_DP16_RD_LVL_STATUS2_P2_[n]	0x800000100701183F	1039
IOM0.DDRPHY_DP16_RD_LVL_STATUS2_P3_[n]	0x8000001007011C3F	1039
IOM0.DDRPHY_DP16_RD_STATUS0_P0_[n]	0x800000140701103F	1045
IOM0.DDRPHY_DP16_RD_STATUS0_P1_[n]	0x800000140701143F	1047
IOM0.DDRPHY_DP16_RD_STATUS0_P2_[n]	0x800000140701183F	1048
IOM0.DDRPHY_DP16_RD_STATUS0_P3_[n]	0x8000001407011C3F	1050
IOM0.DDRPHY_DP16_RD_VREF_CAL_EN_P0_[n]	0x800000760701103F	1228
IOM0.DDRPHY_DP16_RD_VREF_CAL_EN_P1_[n]	0x800000760701143F	1228
IOM0.DDRPHY_DP16_RD_VREF_CAL_EN_P2_[n]	0x800000760701183F	1229
IOM0.DDRPHY_DP16_RD_VREF_CAL_EN_P3_[n]	0x8000007607011C3F	1229
IOM0.DDRPHY_DP16_RD_VREF_CAL_ERROR_P0_[n]	0x8000007A0701103F	1235
IOM0.DDRPHY_DP16_RD_VREF_CAL_ERROR_P1_[n]	0x8000007A0701143F	1235
IOM0.DDRPHY_DP16_RD_VREF_CAL_ERROR_P2_[n]	0x8000007A0701183F	1235
IOM0.DDRPHY_DP16_RD_VREF_CAL_ERROR_P3_[n]	0x8000007A07011C3F	1235
IOM0.DDRPHY_DP16_RD_VREF_DAC_0_P0_[n]	0x800000160701103F	1055
IOM0.DDRPHY_DP16_RD_VREF_DAC_0_P1_[n]	0x800000160701143F	1056
IOM0.DDRPHY_DP16_RD_VREF_DAC_0_P2_[n]	0x800000160701183F	1056
IOM0.DDRPHY_DP16_RD_VREF_DAC_0_P3_[n]	0x8000001607011C3F	1057
IOM0.DDRPHY_DP16_RD_VREF_DAC_1_P0_[n]	0x8000001F0701103F	1077
IOM0.DDRPHY_DP16_RD_VREF_DAC_1_P1_[n]	0x8000001F0701143F	1077
IOM0.DDRPHY_DP16_RD_VREF_DAC_1_P2_[n]	0x8000001F0701183F	1078
IOM0.DDRPHY_DP16_RD_VREF_DAC_1_P3_[n]	0x8000001F07011C3F	1079
IOM0.DDRPHY_DP16_RD_VREF_DAC_2_P0_[n]	0x800000C00701103F	1282
IOM0.DDRPHY_DP16_RD_VREF_DAC_2_P1_[n]	0x800000C00701143F	1283
IOM0.DDRPHY_DP16_RD_VREF_DAC_2_P2_[n]	0x800000C00701183F	1283
IOM0.DDRPHY_DP16_RD_VREF_DAC_2_P3_[n]	0x800000C007011C3F	1284
IOM0.DDRPHY_DP16_RD_VREF_DAC_3_P0_[n]	0x800000C10701103F	1284
IOM0.DDRPHY_DP16_RD_VREF_DAC_3_P1_[n]	0x800000C10701143F	1284
IOM0.DDRPHY_DP16_RD_VREF_DAC_3_P2_[n]	0x800000C10701183F	1285
IOM0.DDRPHY_DP16_RD_VREF_DAC_3_P3_[n]	0x800000C107011C3F	1285
IOM0.DDRPHY_DP16_RD_VREF_DAC_4_P0_[n]	0x800000C20701103F	1286
IOM0.DDRPHY_DP16_RD_VREF_DAC_4_P1_[n]	0x800000C20701143F	1286
IOM0.DDRPHY_DP16_RD_VREF_DAC_4_P2_[n]	0x800000C20701183F	1286
IOM0.DDRPHY_DP16_RD_VREF_DAC_4_P3_[n]	0x800000C207011C3F	1287
IOM0.DDRPHY_DP16_RD_VREF_DAC_5_P0_[n]	0x800000C30701103F	1287
IOM0.DDRPHY_DP16_RD_VREF_DAC_5_P1_[n]	0x800000C30701143F	1288
IOM0.DDRPHY_DP16_RD_VREF_DAC_5_P2_[n]	0x800000C30701183F	1288
IOM0.DDRPHY_DP16_RD_VREF_DAC_5_P3_[n]	0x800000C307011C3F	1289
IOM0.DDRPHY_DP16_RD_VREF_DAC_6_P0_[n]	0x800000C40701103F	1289
IOM0.DDRPHY_DP16_RD_VREF_DAC_6_P1_[n]	0x800000C40701143F	1289

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IOM0.DDRPHY_DP16_RD_VREF_DAC_6_P2_[n]	0x800000C40701183F	1290
IOM0.DDRPHY_DP16_RD_VREF_DAC_6_P3_[n]	0x800000C407011C3F	1290
IOM0.DDRPHY_DP16_RD_VREF_DAC_7_P0_[n]	0x800000C50701103F	1291
IOM0.DDRPHY_DP16_RD_VREF_DAC_7_P1_[n]	0x800000C50701143F	1291
IOM0.DDRPHY_DP16_RD_VREF_DAC_7_P2_[n]	0x800000C50701183F	1291
IOM0.DDRPHY_DP16_RD_VREF_DAC_7_P3_[n]	0x800000C507011C3F	1292
IOM0.DDRPHY_DP16_RD_VREF_DAC_COMP_OUT_P0_[n]	0x800000F60701103F	1294
IOM0.DDRPHY_DP16_RD_VREF_DAC_COMP_OUT_P1_[n]	0x800000F60701143F	1295
IOM0.DDRPHY_DP16_RD_VREF_DAC_COMP_OUT_P2_[n]	0x800000F60701183F	1295
IOM0.DDRPHY_DP16_RD_VREF_DAC_COMP_OUT_P3_[n]	0x800000F607011C3F	1296
IOM0.DDRPHY_DP16_READ_CLOCK_RANK_PAIR0_P0_[n]	0x800000040701103F	1001
IOM0.DDRPHY_DP16_READ_CLOCK_RANK_PAIR0_P1_[n]	0x800000040701143F	1003
IOM0.DDRPHY_DP16_READ_CLOCK_RANK_PAIR0_P2_[n]	0x800000040701183F	1004
IOM0.DDRPHY_DP16_READ_CLOCK_RANK_PAIR0_P3_[n]	0x8000000407011C3F	1006
IOM0.DDRPHY_DP16_READ_CLOCK_RANK_PAIR1_P0_[n]	0x800001040701103F	1306
IOM0.DDRPHY_DP16_READ_CLOCK_RANK_PAIR1_P1_[n]	0x800001040701143F	1307
IOM0.DDRPHY_DP16_READ_CLOCK_RANK_PAIR1_P2_[n]	0x800001040701183F	1309
IOM0.DDRPHY_DP16_READ_CLOCK_RANK_PAIR1_P3_[n]	0x8000010407011C3F	1311
IOM0.DDRPHY_DP16_READ_CLOCK_RANK_PAIR2_P0_[n]	0x800002040701103F	1423
IOM0.DDRPHY_DP16_READ_CLOCK_RANK_PAIR2_P1_[n]	0x800002040701143F	1425
IOM0.DDRPHY_DP16_READ_CLOCK_RANK_PAIR2_P2_[n]	0x800002040701183F	1427
IOM0.DDRPHY_DP16_READ_CLOCK_RANK_PAIR2_P3_[n]	0x8000020407011C3F	1428
IOM0.DDRPHY_DP16_READ_CLOCK_RANK_PAIR3_P0_[n]	0x800003040701103F	1540
IOM0.DDRPHY_DP16_READ_CLOCK_RANK_PAIR3_P1_[n]	0x800003040701143F	1542
IOM0.DDRPHY_DP16_READ_CLOCK_RANK_PAIR3_P2_[n]	0x800003040701183F	1544
IOM0.DDRPHY_DP16_READ_CLOCK_RANK_PAIR3_P3_[n]	0x8000030407011C3F	1545
IOM0.DDRPHY_DP16_READ_DELAY0_RANK_PAIR0_P0_[n]	0x800000500701103F	1160
IOM0.DDRPHY_DP16_READ_DELAY0_RANK_PAIR0_P1_[n]	0x800000500701143F	1161
IOM0.DDRPHY_DP16_READ_DELAY0_RANK_PAIR0_P2_[n]	0x800000500701183F	1161
IOM0.DDRPHY_DP16_READ_DELAY0_RANK_PAIR0_P3_[n]	0x8000005007011C3F	1162
IOM0.DDRPHY_DP16_READ_DELAY0_RANK_PAIR1_P0_[n]	0x800001500701103F	1365
IOM0.DDRPHY_DP16_READ_DELAY0_RANK_PAIR1_P1_[n]	0x800001500701143F	1365
IOM0.DDRPHY_DP16_READ_DELAY0_RANK_PAIR1_P2_[n]	0x800001500701183F	1366
IOM0.DDRPHY_DP16_READ_DELAY0_RANK_PAIR1_P3_[n]	0x8000015007011C3F	1366
IOM0.DDRPHY_DP16_READ_DELAY0_RANK_PAIR2_P0_[n]	0x800002500701103F	1482
IOM0.DDRPHY_DP16_READ_DELAY0_RANK_PAIR2_P1_[n]	0x800002500701143F	1482
IOM0.DDRPHY_DP16_READ_DELAY0_RANK_PAIR2_P2_[n]	0x800002500701183F	1483
IOM0.DDRPHY_DP16_READ_DELAY0_RANK_PAIR2_P3_[n]	0x8000025007011C3F	1483
IOM0.DDRPHY_DP16_READ_DELAY0_RANK_PAIR3_P0_[n]	0x800003500701103F	1599
IOM0.DDRPHY_DP16_READ_DELAY0_RANK_PAIR3_P1_[n]	0x800003500701143F	1599
IOM0.DDRPHY_DP16_READ_DELAY0_RANK_PAIR3_P2_[n]	0x800003500701183F	1600
IOM0.DDRPHY_DP16_READ_DELAY0_RANK_PAIR3_P3_[n]	0x8000035007011C3F	1600
IOM0.DDRPHY_DP16_READ_DELAY1_RANK_PAIR0_P0_[n]	0x800000510701103F	1162

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IOM0.DDRPHY_DP16_READ_DELAY1_RANK_PAIR0_P1_[n]	0x800000510701143F	1163
IOM0.DDRPHY_DP16_READ_DELAY1_RANK_PAIR0_P2_[n]	0x800000510701183F	1163
IOM0.DDRPHY_DP16_READ_DELAY1_RANK_PAIR0_P3_[n]	0x8000005107011C3F	1164
IOM0.DDRPHY_DP16_READ_DELAY1_RANK_PAIR1_P0_[n]	0x800001510701103F	1367
IOM0.DDRPHY_DP16_READ_DELAY1_RANK_PAIR1_P1_[n]	0x800001510701143F	1367
IOM0.DDRPHY_DP16_READ_DELAY1_RANK_PAIR1_P2_[n]	0x800001510701183F	1368
IOM0.DDRPHY_DP16_READ_DELAY1_RANK_PAIR1_P3_[n]	0x8000015107011C3F	1369
IOM0.DDRPHY_DP16_READ_DELAY1_RANK_PAIR2_P0_[n]	0x800002510701103F	1484
IOM0.DDRPHY_DP16_READ_DELAY1_RANK_PAIR2_P1_[n]	0x800002510701143F	1484
IOM0.DDRPHY_DP16_READ_DELAY1_RANK_PAIR2_P2_[n]	0x800002510701183F	1485
IOM0.DDRPHY_DP16_READ_DELAY1_RANK_PAIR2_P3_[n]	0x8000025107011C3F	1486
IOM0.DDRPHY_DP16_READ_DELAY1_RANK_PAIR3_P0_[n]	0x800003510701103F	1601
IOM0.DDRPHY_DP16_READ_DELAY1_RANK_PAIR3_P1_[n]	0x800003510701143F	1601
IOM0.DDRPHY_DP16_READ_DELAY1_RANK_PAIR3_P2_[n]	0x800003510701183F	1602
IOM0.DDRPHY_DP16_READ_DELAY1_RANK_PAIR3_P3_[n]	0x8000035107011C3F	1603
IOM0.DDRPHY_DP16_READ_DELAY2_RANK_PAIR0_P0_[n]	0x800000520701103F	1165
IOM0.DDRPHY_DP16_READ_DELAY2_RANK_PAIR0_P1_[n]	0x800000520701143F	1165
IOM0.DDRPHY_DP16_READ_DELAY2_RANK_PAIR0_P2_[n]	0x800000520701183F	1166
IOM0.DDRPHY_DP16_READ_DELAY2_RANK_PAIR0_P3_[n]	0x8000005207011C3F	1166
IOM0.DDRPHY_DP16_READ_DELAY2_RANK_PAIR1_P0_[n]	0x800001520701103F	1369
IOM0.DDRPHY_DP16_READ_DELAY2_RANK_PAIR1_P1_[n]	0x800001520701143F	1370
IOM0.DDRPHY_DP16_READ_DELAY2_RANK_PAIR1_P2_[n]	0x800001520701183F	1370
IOM0.DDRPHY_DP16_READ_DELAY2_RANK_PAIR1_P3_[n]	0x8000015207011C3F	1371
IOM0.DDRPHY_DP16_READ_DELAY2_RANK_PAIR2_P0_[n]	0x800002520701103F	1486
IOM0.DDRPHY_DP16_READ_DELAY2_RANK_PAIR2_P1_[n]	0x800002520701143F	1487
IOM0.DDRPHY_DP16_READ_DELAY2_RANK_PAIR2_P2_[n]	0x800002520701183F	1487
IOM0.DDRPHY_DP16_READ_DELAY2_RANK_PAIR2_P3_[n]	0x8000025207011C3F	1488
IOM0.DDRPHY_DP16_READ_DELAY2_RANK_PAIR3_P0_[n]	0x800003520701103F	1603
IOM0.DDRPHY_DP16_READ_DELAY2_RANK_PAIR3_P1_[n]	0x800003520701143F	1604
IOM0.DDRPHY_DP16_READ_DELAY2_RANK_PAIR3_P2_[n]	0x800003520701183F	1604
IOM0.DDRPHY_DP16_READ_DELAY2_RANK_PAIR3_P3_[n]	0x8000035207011C3F	1605
IOM0.DDRPHY_DP16_READ_DELAY3_RANK_PAIR0_P0_[n]	0x800000530701103F	1167
IOM0.DDRPHY_DP16_READ_DELAY3_RANK_PAIR0_P1_[n]	0x800000530701143F	1167
IOM0.DDRPHY_DP16_READ_DELAY3_RANK_PAIR0_P2_[n]	0x800000530701183F	1168
IOM0.DDRPHY_DP16_READ_DELAY3_RANK_PAIR0_P3_[n]	0x8000005307011C3F	1169
IOM0.DDRPHY_DP16_READ_DELAY3_RANK_PAIR1_P0_[n]	0x800001530701103F	1371
IOM0.DDRPHY_DP16_READ_DELAY3_RANK_PAIR1_P1_[n]	0x800001530701143F	1372
IOM0.DDRPHY_DP16_READ_DELAY3_RANK_PAIR1_P2_[n]	0x800001530701183F	1373
IOM0.DDRPHY_DP16_READ_DELAY3_RANK_PAIR1_P3_[n]	0x8000015307011C3F	1373
IOM0.DDRPHY_DP16_READ_DELAY3_RANK_PAIR2_P0_[n]	0x800002530701103F	1488
IOM0.DDRPHY_DP16_READ_DELAY3_RANK_PAIR2_P1_[n]	0x800002530701143F	1489
IOM0.DDRPHY_DP16_READ_DELAY3_RANK_PAIR2_P2_[n]	0x800002530701183F	1490
IOM0.DDRPHY_DP16_READ_DELAY3_RANK_PAIR2_P3_[n]	0x8000025307011C3F	1490

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IOM0.DDRPHY_DP16_READ_DELAY3_RANK_PAIR3_P0_[n]	0x800003530701103F	1605
IOM0.DDRPHY_DP16_READ_DELAY3_RANK_PAIR3_P1_[n]	0x800003530701143F	1606
IOM0.DDRPHY_DP16_READ_DELAY3_RANK_PAIR3_P2_[n]	0x800003530701183F	1607
IOM0.DDRPHY_DP16_READ_DELAY3_RANK_PAIR3_P3_[n]	0x8000035307011C3F	1607
IOM0.DDRPHY_DP16_READ_DELAY4_RANK_PAIR0_P0_[n]	0x800000540701103F	1169
IOM0.DDRPHY_DP16_READ_DELAY4_RANK_PAIR0_P1_[n]	0x800000540701143F	1170
IOM0.DDRPHY_DP16_READ_DELAY4_RANK_PAIR0_P2_[n]	0x800000540701183F	1170
IOM0.DDRPHY_DP16_READ_DELAY4_RANK_PAIR0_P3_[n]	0x8000005407011C3F	1171
IOM0.DDRPHY_DP16_READ_DELAY4_RANK_PAIR1_P0_[n]	0x800001540701103F	1374
IOM0.DDRPHY_DP16_READ_DELAY4_RANK_PAIR1_P1_[n]	0x800001540701143F	1374
IOM0.DDRPHY_DP16_READ_DELAY4_RANK_PAIR1_P2_[n]	0x800001540701183F	1375
IOM0.DDRPHY_DP16_READ_DELAY4_RANK_PAIR1_P3_[n]	0x8000015407011C3F	1375
IOM0.DDRPHY_DP16_READ_DELAY4_RANK_PAIR2_P0_[n]	0x800002540701103F	1491
IOM0.DDRPHY_DP16_READ_DELAY4_RANK_PAIR2_P1_[n]	0x800002540701143F	1491
IOM0.DDRPHY_DP16_READ_DELAY4_RANK_PAIR2_P2_[n]	0x800002540701183F	1492
IOM0.DDRPHY_DP16_READ_DELAY4_RANK_PAIR2_P3_[n]	0x8000025407011C3F	1492
IOM0.DDRPHY_DP16_READ_DELAY4_RANK_PAIR3_P0_[n]	0x800003540701103F	1608
IOM0.DDRPHY_DP16_READ_DELAY4_RANK_PAIR3_P1_[n]	0x800003540701143F	1608
IOM0.DDRPHY_DP16_READ_DELAY4_RANK_PAIR3_P2_[n]	0x800003540701183F	1609
IOM0.DDRPHY_DP16_READ_DELAY4_RANK_PAIR3_P3_[n]	0x8000035407011C3F	1609
IOM0.DDRPHY_DP16_READ_DELAY5_RANK_PAIR0_P0_[n]	0x800000550701103F	1171
IOM0.DDRPHY_DP16_READ_DELAY5_RANK_PAIR0_P1_[n]	0x800000550701143F	1172
IOM0.DDRPHY_DP16_READ_DELAY5_RANK_PAIR0_P2_[n]	0x800000550701183F	1173
IOM0.DDRPHY_DP16_READ_DELAY5_RANK_PAIR0_P3_[n]	0x8000005507011C3F	1173
IOM0.DDRPHY_DP16_READ_DELAY5_RANK_PAIR1_P0_[n]	0x800001550701103F	1376
IOM0.DDRPHY_DP16_READ_DELAY5_RANK_PAIR1_P1_[n]	0x800001550701143F	1377
IOM0.DDRPHY_DP16_READ_DELAY5_RANK_PAIR1_P2_[n]	0x800001550701183F	1377
IOM0.DDRPHY_DP16_READ_DELAY5_RANK_PAIR1_P3_[n]	0x8000015507011C3F	1378
IOM0.DDRPHY_DP16_READ_DELAY5_RANK_PAIR2_P0_[n]	0x800002550701103F	1493
IOM0.DDRPHY_DP16_READ_DELAY5_RANK_PAIR2_P1_[n]	0x800002550701143F	1494
IOM0.DDRPHY_DP16_READ_DELAY5_RANK_PAIR2_P2_[n]	0x800002550701183F	1494
IOM0.DDRPHY_DP16_READ_DELAY5_RANK_PAIR2_P3_[n]	0x8000025507011C3F	1495
IOM0.DDRPHY_DP16_READ_DELAY5_RANK_PAIR3_P0_[n]	0x800003550701103F	1610
IOM0.DDRPHY_DP16_READ_DELAY5_RANK_PAIR3_P1_[n]	0x800003550701143F	1611
IOM0.DDRPHY_DP16_READ_DELAY5_RANK_PAIR3_P2_[n]	0x800003550701183F	1611
IOM0.DDRPHY_DP16_READ_DELAY5_RANK_PAIR3_P3_[n]	0x8000035507011C3F	1612
IOM0.DDRPHY_DP16_READ_DELAY6_RANK_PAIR0_P0_[n]	0x800000560701103F	1174
IOM0.DDRPHY_DP16_READ_DELAY6_RANK_PAIR0_P1_[n]	0x800000560701143F	1174
IOM0.DDRPHY_DP16_READ_DELAY6_RANK_PAIR0_P2_[n]	0x800000560701183F	1175
IOM0.DDRPHY_DP16_READ_DELAY6_RANK_PAIR0_P3_[n]	0x8000005607011C3F	1175
IOM0.DDRPHY_DP16_READ_DELAY6_RANK_PAIR1_P0_[n]	0x800001560701103F	1378
IOM0.DDRPHY_DP16_READ_DELAY6_RANK_PAIR1_P1_[n]	0x800001560701143F	1379
IOM0.DDRPHY_DP16_READ_DELAY6_RANK_PAIR1_P2_[n]	0x800001560701183F	1379

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IOM0.DDRPHY_DP16_READ_DELAY6_RANK_PAIR1_P3_[n]	0x8000015607011C3F	1380
IOM0.DDRPHY_DP16_READ_DELAY6_RANK_PAIR2_P0_[n]	0x800002560701103F	1495
IOM0.DDRPHY_DP16_READ_DELAY6_RANK_PAIR2_P1_[n]	0x800002560701143F	1496
IOM0.DDRPHY_DP16_READ_DELAY6_RANK_PAIR2_P2_[n]	0x800002560701183F	1496
IOM0.DDRPHY_DP16_READ_DELAY6_RANK_PAIR2_P3_[n]	0x8000025607011C3F	1497
IOM0.DDRPHY_DP16_READ_DELAY6_RANK_PAIR3_P0_[n]	0x800003560701103F	1612
IOM0.DDRPHY_DP16_READ_DELAY6_RANK_PAIR3_P1_[n]	0x800003560701143F	1613
IOM0.DDRPHY_DP16_READ_DELAY6_RANK_PAIR3_P2_[n]	0x800003560701183F	1613
IOM0.DDRPHY_DP16_READ_DELAY6_RANK_PAIR3_P3_[n]	0x8000035607011C3F	1614
IOM0.DDRPHY_DP16_READ_DELAY7_RANK_PAIR0_P0_[n]	0x800000570701103F	1176
IOM0.DDRPHY_DP16_READ_DELAY7_RANK_PAIR0_P1_[n]	0x800000570701143F	1177
IOM0.DDRPHY_DP16_READ_DELAY7_RANK_PAIR0_P2_[n]	0x800000570701183F	1177
IOM0.DDRPHY_DP16_READ_DELAY7_RANK_PAIR0_P3_[n]	0x8000005707011C3F	1178
IOM0.DDRPHY_DP16_READ_DELAY7_RANK_PAIR1_P0_[n]	0x800001570701103F	1381
IOM0.DDRPHY_DP16_READ_DELAY7_RANK_PAIR1_P1_[n]	0x800001570701143F	1381
IOM0.DDRPHY_DP16_READ_DELAY7_RANK_PAIR1_P2_[n]	0x800001570701183F	1382
IOM0.DDRPHY_DP16_READ_DELAY7_RANK_PAIR1_P3_[n]	0x8000015707011C3F	1382
IOM0.DDRPHY_DP16_READ_DELAY7_RANK_PAIR2_P0_[n]	0x800002570701103F	1498
IOM0.DDRPHY_DP16_READ_DELAY7_RANK_PAIR2_P1_[n]	0x800002570701143F	1498
IOM0.DDRPHY_DP16_READ_DELAY7_RANK_PAIR2_P2_[n]	0x800002570701183F	1499
IOM0.DDRPHY_DP16_READ_DELAY7_RANK_PAIR2_P3_[n]	0x8000025707011C3F	1499
IOM0.DDRPHY_DP16_READ_DELAY7_RANK_PAIR3_P0_[n]	0x800003570701103F	1615
IOM0.DDRPHY_DP16_READ_DELAY7_RANK_PAIR3_P1_[n]	0x800003570701143F	1615
IOM0.DDRPHY_DP16_READ_DELAY7_RANK_PAIR3_P2_[n]	0x800003570701183F	1616
IOM0.DDRPHY_DP16_READ_DELAY7_RANK_PAIR3_P3_[n]	0x8000035707011C3F	1616
IOM0.DDRPHY_DP16_READ_DELAY_OFFSET0_RANK_PAIR0_P0_[n]	0x8000000C0701103F	1033
IOM0.DDRPHY_DP16_READ_DELAY_OFFSET0_RANK_PAIR0_P1_[n]	0x8000000C0701143F	1034
IOM0.DDRPHY_DP16_READ_DELAY_OFFSET0_RANK_PAIR0_P2_[n]	0x8000000C0701183F	1034
IOM0.DDRPHY_DP16_READ_DELAY_OFFSET0_RANK_PAIR0_P3_[n]	0x8000000C07011C3F	1035
IOM0.DDRPHY_DP16_READ_DELAY_OFFSET0_RANK_PAIR1_P0_[n]	0x8000010C0701103F	1323
IOM0.DDRPHY_DP16_READ_DELAY_OFFSET0_RANK_PAIR1_P1_[n]	0x8000010C0701143F	1323
IOM0.DDRPHY_DP16_READ_DELAY_OFFSET0_RANK_PAIR1_P2_[n]	0x8000010C0701183F	1324
IOM0.DDRPHY_DP16_READ_DELAY_OFFSET0_RANK_PAIR1_P3_[n]	0x8000010C07011C3F	1324
IOM0.DDRPHY_DP16_READ_DELAY_OFFSET0_RANK_PAIR2_P0_[n]	0x8000020C0701103F	1440
IOM0.DDRPHY_DP16_READ_DELAY_OFFSET0_RANK_PAIR2_P1_[n]	0x8000020C0701143F	1440
IOM0.DDRPHY_DP16_READ_DELAY_OFFSET0_RANK_PAIR2_P2_[n]	0x8000020C0701183F	1441
IOM0.DDRPHY_DP16_READ_DELAY_OFFSET0_RANK_PAIR2_P3_[n]	0x8000020C07011C3F	1441
IOM0.DDRPHY_DP16_READ_DELAY_OFFSET0_RANK_PAIR3_P0_[n]	0x8000030C0701103F	1557
IOM0.DDRPHY_DP16_READ_DELAY_OFFSET0_RANK_PAIR3_P1_[n]	0x8000030C0701143F	1557
IOM0.DDRPHY_DP16_READ_DELAY_OFFSET0_RANK_PAIR3_P2_[n]	0x8000030C0701183F	1558
IOM0.DDRPHY_DP16_READ_DELAY_OFFSET0_RANK_PAIR3_P3_[n]	0x8000030C07011C3F	1558
IOM0.DDRPHY_DP16_READ_DELAY_OFFSET1_RANK_PAIR0_P0_[n]	0x8000000D0701103F	1035
IOM0.DDRPHY_DP16_READ_DELAY_OFFSET1_RANK_PAIR0_P1_[n]	0x8000000D0701143F	1036

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IOM0.DDRPHY_DP16_READ_DELAY_OFFSET1_RANK_PAIR0_P2_[n]	0x8000000D0701183F	1036
IOM0.DDRPHY_DP16_READ_DELAY_OFFSET1_RANK_PAIR0_P3_[n]	0x8000000D07011C3F	1037
IOM0.DDRPHY_DP16_READ_DELAY_OFFSET1_RANK_PAIR1_P0_[n]	0x8000010D0701103F	1325
IOM0.DDRPHY_DP16_READ_DELAY_OFFSET1_RANK_PAIR1_P1_[n]	0x8000010D0701143F	1325
IOM0.DDRPHY_DP16_READ_DELAY_OFFSET1_RANK_PAIR1_P2_[n]	0x8000010D0701183F	1326
IOM0.DDRPHY_DP16_READ_DELAY_OFFSET1_RANK_PAIR1_P3_[n]	0x8000010D07011C3F	1326
IOM0.DDRPHY_DP16_READ_DELAY_OFFSET1_RANK_PAIR2_P0_[n]	0x8000020D0701103F	1442
IOM0.DDRPHY_DP16_READ_DELAY_OFFSET1_RANK_PAIR2_P1_[n]	0x8000020D0701143F	1442
IOM0.DDRPHY_DP16_READ_DELAY_OFFSET1_RANK_PAIR2_P2_[n]	0x8000020D0701183F	1443
IOM0.DDRPHY_DP16_READ_DELAY_OFFSET1_RANK_PAIR2_P3_[n]	0x8000020D07011C3F	1443
IOM0.DDRPHY_DP16_READ_DELAY_OFFSET1_RANK_PAIR3_P0_[n]	0x8000030D0701103F	1559
IOM0.DDRPHY_DP16_READ_DELAY_OFFSET1_RANK_PAIR3_P1_[n]	0x8000030D0701143F	1559
IOM0.DDRPHY_DP16_READ_DELAY_OFFSET1_RANK_PAIR3_P2_[n]	0x8000030D0701183F	1560
IOM0.DDRPHY_DP16_READ_DELAY_OFFSET1_RANK_PAIR3_P3_[n]	0x8000030D07011C3F	1560
IOM0.DDRPHY_DP16_READ_DQS_TIMING_REFERENCE_P0_[n]	0x800000720701103F	1221
IOM0.DDRPHY_DP16_READ_DQS_TIMING_REFERENCE_P1_[n]	0x800000720701143F	1221
IOM0.DDRPHY_DP16_READ_DQS_TIMING_REFERENCE_P2_[n]	0x800000720701183F	1221
IOM0.DDRPHY_DP16_READ_DQS_TIMING_REFERENCE_P3_[n]	0x8000007207011C3F	1222
IOM0.DDRPHY_DP16_READ_EYE_SIZE0_RANK_PAIR0_P0_[n]	0x800000600701103F	1186
IOM0.DDRPHY_DP16_READ_EYE_SIZE0_RANK_PAIR0_P1_[n]	0x800000600701143F	1187
IOM0.DDRPHY_DP16_READ_EYE_SIZE0_RANK_PAIR0_P2_[n]	0x800000600701183F	1187
IOM0.DDRPHY_DP16_READ_EYE_SIZE0_RANK_PAIR0_P3_[n]	0x8000006007011C3F	1188
IOM0.DDRPHY_DP16_READ_EYE_SIZE0_RANK_PAIR1_P0_[n]	0x800001600701103F	1391
IOM0.DDRPHY_DP16_READ_EYE_SIZE0_RANK_PAIR1_P1_[n]	0x800001600701143F	1391
IOM0.DDRPHY_DP16_READ_EYE_SIZE0_RANK_PAIR1_P2_[n]	0x800001600701183F	1392
IOM0.DDRPHY_DP16_READ_EYE_SIZE0_RANK_PAIR1_P3_[n]	0x8000016007011C3F	1392
IOM0.DDRPHY_DP16_READ_EYE_SIZE0_RANK_PAIR2_P0_[n]	0x800002600701103F	1508
IOM0.DDRPHY_DP16_READ_EYE_SIZE0_RANK_PAIR2_P1_[n]	0x800002600701143F	1508
IOM0.DDRPHY_DP16_READ_EYE_SIZE0_RANK_PAIR2_P2_[n]	0x800002600701183F	1509
IOM0.DDRPHY_DP16_READ_EYE_SIZE0_RANK_PAIR2_P3_[n]	0x8000026007011C3F	1509
IOM0.DDRPHY_DP16_READ_EYE_SIZE0_RANK_PAIR3_P0_[n]	0x800003600701103F	1625
IOM0.DDRPHY_DP16_READ_EYE_SIZE0_RANK_PAIR3_P1_[n]	0x800003600701143F	1625
IOM0.DDRPHY_DP16_READ_EYE_SIZE0_RANK_PAIR3_P2_[n]	0x800003600701183F	1626
IOM0.DDRPHY_DP16_READ_EYE_SIZE0_RANK_PAIR3_P3_[n]	0x8000036007011C3F	1626
IOM0.DDRPHY_DP16_READ_EYE_SIZE10_RANK_PAIR0_P0_[n]	0x8000006A0701103F	1206
IOM0.DDRPHY_DP16_READ_EYE_SIZE10_RANK_PAIR0_P1_[n]	0x8000006A0701143F	1207
IOM0.DDRPHY_DP16_READ_EYE_SIZE10_RANK_PAIR0_P2_[n]	0x8000006A0701183F	1207
IOM0.DDRPHY_DP16_READ_EYE_SIZE10_RANK_PAIR0_P3_[n]	0x8000006A07011C3F	1208
IOM0.DDRPHY_DP16_READ_EYE_SIZE10_RANK_PAIR1_P0_[n]	0x8000016A0701103F	1411
IOM0.DDRPHY_DP16_READ_EYE_SIZE10_RANK_PAIR1_P1_[n]	0x8000016A0701143F	1411
IOM0.DDRPHY_DP16_READ_EYE_SIZE10_RANK_PAIR1_P2_[n]	0x8000016A0701183F	1412
IOM0.DDRPHY_DP16_READ_EYE_SIZE10_RANK_PAIR1_P3_[n]	0x8000016A07011C3F	1412
IOM0.DDRPHY_DP16_READ_EYE_SIZE10_RANK_PAIR2_P0_[n]	0x8000026A0701103F	1528

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IOM0.DDRPHY_DP16_READ_EYE_SIZE10_RANK_PAIR2_P1_[n]	0x8000026A0701143F	1528
IOM0.DDRPHY_DP16_READ_EYE_SIZE10_RANK_PAIR2_P2_[n]	0x8000026A0701183F	1529
IOM0.DDRPHY_DP16_READ_EYE_SIZE10_RANK_PAIR2_P3_[n]	0x8000026A07011C3F	1529
IOM0.DDRPHY_DP16_READ_EYE_SIZE10_RANK_PAIR3_P0_[n]	0x8000036A0701103F	1645
IOM0.DDRPHY_DP16_READ_EYE_SIZE10_RANK_PAIR3_P1_[n]	0x8000036A0701143F	1645
IOM0.DDRPHY_DP16_READ_EYE_SIZE10_RANK_PAIR3_P2_[n]	0x8000036A0701183F	1646
IOM0.DDRPHY_DP16_READ_EYE_SIZE10_RANK_PAIR3_P3_[n]	0x8000036A07011C3F	1646
IOM0.DDRPHY_DP16_READ_EYE_SIZE11_RANK_PAIR0_P0_[n]	0x8000006B0701103F	1208
IOM0.DDRPHY_DP16_READ_EYE_SIZE11_RANK_PAIR0_P1_[n]	0x8000006B0701143F	1209
IOM0.DDRPHY_DP16_READ_EYE_SIZE11_RANK_PAIR0_P2_[n]	0x8000006B0701183F	1209
IOM0.DDRPHY_DP16_READ_EYE_SIZE11_RANK_PAIR0_P3_[n]	0x8000006B07011C3F	1210
IOM0.DDRPHY_DP16_READ_EYE_SIZE11_RANK_PAIR1_P0_[n]	0x8000016B0701103F	1413
IOM0.DDRPHY_DP16_READ_EYE_SIZE11_RANK_PAIR1_P1_[n]	0x8000016B0701143F	1413
IOM0.DDRPHY_DP16_READ_EYE_SIZE11_RANK_PAIR1_P2_[n]	0x8000016B0701183F	1414
IOM0.DDRPHY_DP16_READ_EYE_SIZE11_RANK_PAIR1_P3_[n]	0x8000016B07011C3F	1414
IOM0.DDRPHY_DP16_READ_EYE_SIZE11_RANK_PAIR2_P0_[n]	0x8000026B0701103F	1530
IOM0.DDRPHY_DP16_READ_EYE_SIZE11_RANK_PAIR2_P1_[n]	0x8000026B0701143F	1530
IOM0.DDRPHY_DP16_READ_EYE_SIZE11_RANK_PAIR2_P2_[n]	0x8000026B0701183F	1531
IOM0.DDRPHY_DP16_READ_EYE_SIZE11_RANK_PAIR2_P3_[n]	0x8000026B07011C3F	1531
IOM0.DDRPHY_DP16_READ_EYE_SIZE11_RANK_PAIR3_P0_[n]	0x8000036B0701103F	1647
IOM0.DDRPHY_DP16_READ_EYE_SIZE11_RANK_PAIR3_P1_[n]	0x8000036B0701143F	1647
IOM0.DDRPHY_DP16_READ_EYE_SIZE11_RANK_PAIR3_P2_[n]	0x8000036B0701183F	1648
IOM0.DDRPHY_DP16_READ_EYE_SIZE11_RANK_PAIR3_P3_[n]	0x8000036B07011C3F	1648
IOM0.DDRPHY_DP16_READ_EYE_SIZE1_RANK_PAIR0_P0_[n]	0x800000610701103F	1188
IOM0.DDRPHY_DP16_READ_EYE_SIZE1_RANK_PAIR0_P1_[n]	0x800000610701143F	1189
IOM0.DDRPHY_DP16_READ_EYE_SIZE1_RANK_PAIR0_P2_[n]	0x800000610701183F	1189
IOM0.DDRPHY_DP16_READ_EYE_SIZE1_RANK_PAIR0_P3_[n]	0x8000006107011C3F	1190
IOM0.DDRPHY_DP16_READ_EYE_SIZE1_RANK_PAIR1_P0_[n]	0x800001610701103F	1393
IOM0.DDRPHY_DP16_READ_EYE_SIZE1_RANK_PAIR1_P1_[n]	0x800001610701143F	1393
IOM0.DDRPHY_DP16_READ_EYE_SIZE1_RANK_PAIR1_P2_[n]	0x800001610701183F	1394
IOM0.DDRPHY_DP16_READ_EYE_SIZE1_RANK_PAIR1_P3_[n]	0x8000016107011C3F	1394
IOM0.DDRPHY_DP16_READ_EYE_SIZE1_RANK_PAIR2_P0_[n]	0x800002610701103F	1510
IOM0.DDRPHY_DP16_READ_EYE_SIZE1_RANK_PAIR2_P1_[n]	0x800002610701143F	1510
IOM0.DDRPHY_DP16_READ_EYE_SIZE1_RANK_PAIR2_P2_[n]	0x800002610701183F	1511
IOM0.DDRPHY_DP16_READ_EYE_SIZE1_RANK_PAIR2_P3_[n]	0x8000026107011C3F	1511
IOM0.DDRPHY_DP16_READ_EYE_SIZE1_RANK_PAIR3_P0_[n]	0x800003610701103F	1627
IOM0.DDRPHY_DP16_READ_EYE_SIZE1_RANK_PAIR3_P1_[n]	0x800003610701143F	1627
IOM0.DDRPHY_DP16_READ_EYE_SIZE1_RANK_PAIR3_P2_[n]	0x800003610701183F	1628
IOM0.DDRPHY_DP16_READ_EYE_SIZE1_RANK_PAIR3_P3_[n]	0x8000036107011C3F	1628
IOM0.DDRPHY_DP16_READ_EYE_SIZE2_RANK_PAIR0_P0_[n]	0x800000620701103F	1190
IOM0.DDRPHY_DP16_READ_EYE_SIZE2_RANK_PAIR0_P1_[n]	0x800000620701143F	1191
IOM0.DDRPHY_DP16_READ_EYE_SIZE2_RANK_PAIR0_P2_[n]	0x800000620701183F	1191
IOM0.DDRPHY_DP16_READ_EYE_SIZE2_RANK_PAIR0_P3_[n]	0x8000006207011C3F	1192

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IOM0.DDRPHY_DP16_READ_EYE_SIZE2_RANK_PAIR1_P0_[n]	0x800001620701103F	1395
IOM0.DDRPHY_DP16_READ_EYE_SIZE2_RANK_PAIR1_P1_[n]	0x800001620701143F	1395
IOM0.DDRPHY_DP16_READ_EYE_SIZE2_RANK_PAIR1_P2_[n]	0x800001620701183F	1396
IOM0.DDRPHY_DP16_READ_EYE_SIZE2_RANK_PAIR1_P3_[n]	0x8000016207011C3F	1396
IOM0.DDRPHY_DP16_READ_EYE_SIZE2_RANK_PAIR2_P0_[n]	0x800002620701103F	1512
IOM0.DDRPHY_DP16_READ_EYE_SIZE2_RANK_PAIR2_P1_[n]	0x800002620701143F	1512
IOM0.DDRPHY_DP16_READ_EYE_SIZE2_RANK_PAIR2_P2_[n]	0x800002620701183F	1513
IOM0.DDRPHY_DP16_READ_EYE_SIZE2_RANK_PAIR2_P3_[n]	0x8000026207011C3F	1513
IOM0.DDRPHY_DP16_READ_EYE_SIZE2_RANK_PAIR3_P0_[n]	0x800003620701103F	1629
IOM0.DDRPHY_DP16_READ_EYE_SIZE2_RANK_PAIR3_P1_[n]	0x800003620701143F	1629
IOM0.DDRPHY_DP16_READ_EYE_SIZE2_RANK_PAIR3_P2_[n]	0x800003620701183F	1630
IOM0.DDRPHY_DP16_READ_EYE_SIZE2_RANK_PAIR3_P3_[n]	0x8000036207011C3F	1630
IOM0.DDRPHY_DP16_READ_EYE_SIZE3_RANK_PAIR0_P0_[n]	0x800000630701103F	1192
IOM0.DDRPHY_DP16_READ_EYE_SIZE3_RANK_PAIR0_P1_[n]	0x800000630701143F	1193
IOM0.DDRPHY_DP16_READ_EYE_SIZE3_RANK_PAIR0_P2_[n]	0x800000630701183F	1193
IOM0.DDRPHY_DP16_READ_EYE_SIZE3_RANK_PAIR0_P3_[n]	0x8000006307011C3F	1194
IOM0.DDRPHY_DP16_READ_EYE_SIZE3_RANK_PAIR1_P0_[n]	0x800001630701103F	1397
IOM0.DDRPHY_DP16_READ_EYE_SIZE3_RANK_PAIR1_P1_[n]	0x800001630701143F	1397
IOM0.DDRPHY_DP16_READ_EYE_SIZE3_RANK_PAIR1_P2_[n]	0x800001630701183F	1398
IOM0.DDRPHY_DP16_READ_EYE_SIZE3_RANK_PAIR1_P3_[n]	0x8000016307011C3F	1398
IOM0.DDRPHY_DP16_READ_EYE_SIZE3_RANK_PAIR2_P0_[n]	0x800002630701103F	1514
IOM0.DDRPHY_DP16_READ_EYE_SIZE3_RANK_PAIR2_P1_[n]	0x800002630701143F	1514
IOM0.DDRPHY_DP16_READ_EYE_SIZE3_RANK_PAIR2_P2_[n]	0x800002630701183F	1515
IOM0.DDRPHY_DP16_READ_EYE_SIZE3_RANK_PAIR2_P3_[n]	0x8000026307011C3F	1515
IOM0.DDRPHY_DP16_READ_EYE_SIZE3_RANK_PAIR3_P0_[n]	0x800003630701103F	1631
IOM0.DDRPHY_DP16_READ_EYE_SIZE3_RANK_PAIR3_P1_[n]	0x800003630701143F	1631
IOM0.DDRPHY_DP16_READ_EYE_SIZE3_RANK_PAIR3_P2_[n]	0x800003630701183F	1632
IOM0.DDRPHY_DP16_READ_EYE_SIZE3_RANK_PAIR3_P3_[n]	0x8000036307011C3F	1632
IOM0.DDRPHY_DP16_READ_EYE_SIZE4_RANK_PAIR0_P0_[n]	0x800000640701103F	1194
IOM0.DDRPHY_DP16_READ_EYE_SIZE4_RANK_PAIR0_P1_[n]	0x800000640701143F	1195
IOM0.DDRPHY_DP16_READ_EYE_SIZE4_RANK_PAIR0_P2_[n]	0x800000640701183F	1195
IOM0.DDRPHY_DP16_READ_EYE_SIZE4_RANK_PAIR0_P3_[n]	0x8000006407011C3F	1196
IOM0.DDRPHY_DP16_READ_EYE_SIZE4_RANK_PAIR1_P0_[n]	0x800001640701103F	1399
IOM0.DDRPHY_DP16_READ_EYE_SIZE4_RANK_PAIR1_P1_[n]	0x800001640701143F	1399
IOM0.DDRPHY_DP16_READ_EYE_SIZE4_RANK_PAIR1_P2_[n]	0x800001640701183F	1400
IOM0.DDRPHY_DP16_READ_EYE_SIZE4_RANK_PAIR1_P3_[n]	0x8000016407011C3F	1400
IOM0.DDRPHY_DP16_READ_EYE_SIZE4_RANK_PAIR2_P0_[n]	0x800002640701103F	1516
IOM0.DDRPHY_DP16_READ_EYE_SIZE4_RANK_PAIR2_P1_[n]	0x800002640701143F	1516
IOM0.DDRPHY_DP16_READ_EYE_SIZE4_RANK_PAIR2_P2_[n]	0x800002640701183F	1517
IOM0.DDRPHY_DP16_READ_EYE_SIZE4_RANK_PAIR2_P3_[n]	0x8000026407011C3F	1517
IOM0.DDRPHY_DP16_READ_EYE_SIZE4_RANK_PAIR3_P0_[n]	0x800003640701103F	1633
IOM0.DDRPHY_DP16_READ_EYE_SIZE4_RANK_PAIR3_P1_[n]	0x800003640701143F	1633
IOM0.DDRPHY_DP16_READ_EYE_SIZE4_RANK_PAIR3_P2_[n]	0x800003640701183F	1634

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IOM0.DDRPHY_DP16_READ_EYE_SIZE4_RANK_PAIR3_P3_[n]	0x8000036407011C3F	1634
IOM0.DDRPHY_DP16_READ_EYE_SIZE5_RANK_PAIR0_P0_[n]	0x800000650701103F	1196
IOM0.DDRPHY_DP16_READ_EYE_SIZE5_RANK_PAIR0_P1_[n]	0x800000650701143F	1197
IOM0.DDRPHY_DP16_READ_EYE_SIZE5_RANK_PAIR0_P2_[n]	0x800000650701183F	1197
IOM0.DDRPHY_DP16_READ_EYE_SIZE5_RANK_PAIR0_P3_[n]	0x8000006507011C3F	1198
IOM0.DDRPHY_DP16_READ_EYE_SIZE5_RANK_PAIR1_P0_[n]	0x800001650701103F	1401
IOM0.DDRPHY_DP16_READ_EYE_SIZE5_RANK_PAIR1_P1_[n]	0x800001650701143F	1401
IOM0.DDRPHY_DP16_READ_EYE_SIZE5_RANK_PAIR1_P2_[n]	0x800001650701183F	1402
IOM0.DDRPHY_DP16_READ_EYE_SIZE5_RANK_PAIR1_P3_[n]	0x8000016507011C3F	1402
IOM0.DDRPHY_DP16_READ_EYE_SIZE5_RANK_PAIR2_P0_[n]	0x800002650701103F	1518
IOM0.DDRPHY_DP16_READ_EYE_SIZE5_RANK_PAIR2_P1_[n]	0x800002650701143F	1518
IOM0.DDRPHY_DP16_READ_EYE_SIZE5_RANK_PAIR2_P2_[n]	0x800002650701183F	1519
IOM0.DDRPHY_DP16_READ_EYE_SIZE5_RANK_PAIR2_P3_[n]	0x8000026507011C3F	1519
IOM0.DDRPHY_DP16_READ_EYE_SIZE5_RANK_PAIR3_P0_[n]	0x800003650701103F	1635
IOM0.DDRPHY_DP16_READ_EYE_SIZE5_RANK_PAIR3_P1_[n]	0x800003650701143F	1635
IOM0.DDRPHY_DP16_READ_EYE_SIZE5_RANK_PAIR3_P2_[n]	0x800003650701183F	1636
IOM0.DDRPHY_DP16_READ_EYE_SIZE5_RANK_PAIR3_P3_[n]	0x8000036507011C3F	1636
IOM0.DDRPHY_DP16_READ_EYE_SIZE6_RANK_PAIR0_P0_[n]	0x800000660701103F	1198
IOM0.DDRPHY_DP16_READ_EYE_SIZE6_RANK_PAIR0_P1_[n]	0x800000660701143F	1199
IOM0.DDRPHY_DP16_READ_EYE_SIZE6_RANK_PAIR0_P2_[n]	0x800000660701183F	1199
IOM0.DDRPHY_DP16_READ_EYE_SIZE6_RANK_PAIR0_P3_[n]	0x8000006607011C3F	1200
IOM0.DDRPHY_DP16_READ_EYE_SIZE6_RANK_PAIR1_P0_[n]	0x800001660701103F	1403
IOM0.DDRPHY_DP16_READ_EYE_SIZE6_RANK_PAIR1_P1_[n]	0x800001660701143F	1403
IOM0.DDRPHY_DP16_READ_EYE_SIZE6_RANK_PAIR1_P2_[n]	0x800001660701183F	1404
IOM0.DDRPHY_DP16_READ_EYE_SIZE6_RANK_PAIR1_P3_[n]	0x8000016607011C3F	1404
IOM0.DDRPHY_DP16_READ_EYE_SIZE6_RANK_PAIR2_P0_[n]	0x800002660701103F	1520
IOM0.DDRPHY_DP16_READ_EYE_SIZE6_RANK_PAIR2_P1_[n]	0x800002660701143F	1520
IOM0.DDRPHY_DP16_READ_EYE_SIZE6_RANK_PAIR2_P2_[n]	0x800002660701183F	1521
IOM0.DDRPHY_DP16_READ_EYE_SIZE6_RANK_PAIR2_P3_[n]	0x8000026607011C3F	1521
IOM0.DDRPHY_DP16_READ_EYE_SIZE6_RANK_PAIR3_P0_[n]	0x800003660701103F	1637
IOM0.DDRPHY_DP16_READ_EYE_SIZE6_RANK_PAIR3_P1_[n]	0x800003660701143F	1637
IOM0.DDRPHY_DP16_READ_EYE_SIZE6_RANK_PAIR3_P2_[n]	0x800003660701183F	1638
IOM0.DDRPHY_DP16_READ_EYE_SIZE6_RANK_PAIR3_P3_[n]	0x8000036607011C3F	1638
IOM0.DDRPHY_DP16_READ_EYE_SIZE7_RANK_PAIR0_P0_[n]	0x800000670701103F	1200
IOM0.DDRPHY_DP16_READ_EYE_SIZE7_RANK_PAIR0_P1_[n]	0x800000670701143F	1201
IOM0.DDRPHY_DP16_READ_EYE_SIZE7_RANK_PAIR0_P2_[n]	0x800000670701183F	1201
IOM0.DDRPHY_DP16_READ_EYE_SIZE7_RANK_PAIR0_P3_[n]	0x8000006707011C3F	1202
IOM0.DDRPHY_DP16_READ_EYE_SIZE7_RANK_PAIR1_P0_[n]	0x800001670701103F	1405
IOM0.DDRPHY_DP16_READ_EYE_SIZE7_RANK_PAIR1_P1_[n]	0x800001670701143F	1405
IOM0.DDRPHY_DP16_READ_EYE_SIZE7_RANK_PAIR1_P2_[n]	0x800001670701183F	1406
IOM0.DDRPHY_DP16_READ_EYE_SIZE7_RANK_PAIR1_P3_[n]	0x8000016707011C3F	1406
IOM0.DDRPHY_DP16_READ_EYE_SIZE7_RANK_PAIR2_P0_[n]	0x800002670701103F	1522
IOM0.DDRPHY_DP16_READ_EYE_SIZE7_RANK_PAIR2_P1_[n]	0x800002670701143F	1522

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IOM0.DDRPHY_DP16_READ_EYE_SIZE7_RANK_PAIR2_P2_[n]	0x800002670701183F	1523
IOM0.DDRPHY_DP16_READ_EYE_SIZE7_RANK_PAIR2_P3_[n]	0x8000026707011C3F	1523
IOM0.DDRPHY_DP16_READ_EYE_SIZE7_RANK_PAIR3_P0_[n]	0x800003670701103F	1639
IOM0.DDRPHY_DP16_READ_EYE_SIZE7_RANK_PAIR3_P1_[n]	0x800003670701143F	1639
IOM0.DDRPHY_DP16_READ_EYE_SIZE7_RANK_PAIR3_P2_[n]	0x800003670701183F	1640
IOM0.DDRPHY_DP16_READ_EYE_SIZE7_RANK_PAIR3_P3_[n]	0x8000036707011C3F	1640
IOM0.DDRPHY_DP16_READ_EYE_SIZE8_RANK_PAIR0_P0_[n]	0x800000680701103F	1202
IOM0.DDRPHY_DP16_READ_EYE_SIZE8_RANK_PAIR0_P1_[n]	0x800000680701143F	1203
IOM0.DDRPHY_DP16_READ_EYE_SIZE8_RANK_PAIR0_P2_[n]	0x800000680701183F	1203
IOM0.DDRPHY_DP16_READ_EYE_SIZE8_RANK_PAIR0_P3_[n]	0x8000006807011C3F	1204
IOM0.DDRPHY_DP16_READ_EYE_SIZE8_RANK_PAIR1_P0_[n]	0x800001680701103F	1407
IOM0.DDRPHY_DP16_READ_EYE_SIZE8_RANK_PAIR1_P1_[n]	0x800001680701143F	1407
IOM0.DDRPHY_DP16_READ_EYE_SIZE8_RANK_PAIR1_P2_[n]	0x800001680701183F	1408
IOM0.DDRPHY_DP16_READ_EYE_SIZE8_RANK_PAIR1_P3_[n]	0x8000016807011C3F	1408
IOM0.DDRPHY_DP16_READ_EYE_SIZE8_RANK_PAIR2_P0_[n]	0x800002680701103F	1524
IOM0.DDRPHY_DP16_READ_EYE_SIZE8_RANK_PAIR2_P1_[n]	0x800002680701143F	1524
IOM0.DDRPHY_DP16_READ_EYE_SIZE8_RANK_PAIR2_P2_[n]	0x800002680701183F	1525
IOM0.DDRPHY_DP16_READ_EYE_SIZE8_RANK_PAIR2_P3_[n]	0x8000026807011C3F	1525
IOM0.DDRPHY_DP16_READ_EYE_SIZE8_RANK_PAIR3_P0_[n]	0x800003680701103F	1641
IOM0.DDRPHY_DP16_READ_EYE_SIZE8_RANK_PAIR3_P1_[n]	0x800003680701143F	1641
IOM0.DDRPHY_DP16_READ_EYE_SIZE8_RANK_PAIR3_P2_[n]	0x800003680701183F	1642
IOM0.DDRPHY_DP16_READ_EYE_SIZE8_RANK_PAIR3_P3_[n]	0x8000036807011C3F	1642
IOM0.DDRPHY_DP16_READ_EYE_SIZE9_RANK_PAIR0_P0_[n]	0x800000690701103F	1204
IOM0.DDRPHY_DP16_READ_EYE_SIZE9_RANK_PAIR0_P1_[n]	0x800000690701143F	1205
IOM0.DDRPHY_DP16_READ_EYE_SIZE9_RANK_PAIR0_P2_[n]	0x800000690701183F	1205
IOM0.DDRPHY_DP16_READ_EYE_SIZE9_RANK_PAIR0_P3_[n]	0x8000006907011C3F	1206
IOM0.DDRPHY_DP16_READ_EYE_SIZE9_RANK_PAIR1_P0_[n]	0x800001690701103F	1409
IOM0.DDRPHY_DP16_READ_EYE_SIZE9_RANK_PAIR1_P1_[n]	0x800001690701143F	1409
IOM0.DDRPHY_DP16_READ_EYE_SIZE9_RANK_PAIR1_P2_[n]	0x800001690701183F	1410
IOM0.DDRPHY_DP16_READ_EYE_SIZE9_RANK_PAIR1_P3_[n]	0x8000016907011C3F	1410
IOM0.DDRPHY_DP16_READ_EYE_SIZE9_RANK_PAIR2_P0_[n]	0x800002690701103F	1526
IOM0.DDRPHY_DP16_READ_EYE_SIZE9_RANK_PAIR2_P1_[n]	0x800002690701143F	1526
IOM0.DDRPHY_DP16_READ_EYE_SIZE9_RANK_PAIR2_P2_[n]	0x800002690701183F	1527
IOM0.DDRPHY_DP16_READ_EYE_SIZE9_RANK_PAIR2_P3_[n]	0x8000026907011C3F	1527
IOM0.DDRPHY_DP16_READ_EYE_SIZE9_RANK_PAIR3_P0_[n]	0x800003690701103F	1643
IOM0.DDRPHY_DP16_READ_EYE_SIZE9_RANK_PAIR3_P1_[n]	0x800003690701143F	1643
IOM0.DDRPHY_DP16_READ_EYE_SIZE9_RANK_PAIR3_P2_[n]	0x800003690701183F	1644
IOM0.DDRPHY_DP16_READ_EYE_SIZE9_RANK_PAIR3_P3_[n]	0x8000036907011C3F	1644
IOM0.DDRPHY_DP16_READ_TIMING_REFERENCE0_P0_[n]	0x800000700701103F	1218
IOM0.DDRPHY_DP16_READ_TIMING_REFERENCE0_P1_[n]	0x800000700701143F	1218
IOM0.DDRPHY_DP16_READ_TIMING_REFERENCE0_P2_[n]	0x800000700701183F	1218
IOM0.DDRPHY_DP16_READ_TIMING_REFERENCE0_P3_[n]	0x8000007007011C3F	1219
IOM0.DDRPHY_DP16_READ_TIMING_REFERENCE1_P0_[n]	0x800000710701103F	1219

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IOM0.DDRPHY_DP16_READ_TIMING_REFERENCE1_P1_[n]	0x800000710701143F	1220
IOM0.DDRPHY_DP16_READ_TIMING_REFERENCE1_P2_[n]	0x800000710701183F	1220
IOM0.DDRPHY_DP16_READ_TIMING_REFERENCE1_P3_[n]	0x8000007107011C3F	1220
IOM0.DDRPHY_DP16_RX_CONFIG0_P0_[n]	0x800000060701103F	1015
IOM0.DDRPHY_DP16_RX_CONFIG0_P1_[n]	0x800000060701143F	1017
IOM0.DDRPHY_DP16_RX_CONFIG0_P2_[n]	0x800000060701183F	1018
IOM0.DDRPHY_DP16_RX_CONFIG0_P3_[n]	0x8000000607011C3F	1019
IOM0.DDRPHY_DP16_SYSCLK_PR0_P0_[n]	0x800000070701103F	1020
IOM0.DDRPHY_DP16_SYSCLK_PR0_P1_[n]	0x800000070701143F	1022
IOM0.DDRPHY_DP16_SYSCLK_PR0_P2_[n]	0x800000070701183F	1023
IOM0.DDRPHY_DP16_SYSCLK_PR0_P3_[n]	0x8000000707011C3F	1024
IOM0.DDRPHY_DP16_SYSCLK_PR1_P0_[n]	0x8000007F0701103F	1245
IOM0.DDRPHY_DP16_SYSCLK_PR1_P1_[n]	0x8000007F0701143F	1247
IOM0.DDRPHY_DP16_SYSCLK_PR1_P2_[n]	0x8000007F0701183F	1248
IOM0.DDRPHY_DP16_SYSCLK_PR1_P3_[n]	0x8000007F07011C3F	1249
IOM0.DDRPHY_DP16_SYSCLK_PR_VALUE_P0_[n]	0x800000730701103F	1222
IOM0.DDRPHY_DP16_SYSCLK_PR_VALUE_P1_[n]	0x800000730701143F	1223
IOM0.DDRPHY_DP16_SYSCLK_PR_VALUE_P2_[n]	0x800000730701183F	1223
IOM0.DDRPHY_DP16_SYSCLK_PR_VALUE_P3_[n]	0x8000007307011C3F	1224
IOM0.DDRPHY_DP16_WRCLK_EN_RP0_P0_[n]	0x800000050701103F	1008
IOM0.DDRPHY_DP16_WRCLK_EN_RP0_P1_[n]	0x800000050701143F	1010
IOM0.DDRPHY_DP16_WRCLK_EN_RP0_P2_[n]	0x800000050701183F	1012
IOM0.DDRPHY_DP16_WRCLK_EN_RP0_P3_[n]	0x8000000507011C3F	1014
IOM0.DDRPHY_DP16_WRCLK_EN_RP1_P0_[n]	0x800001050701103F	1313
IOM0.DDRPHY_DP16_WRCLK_EN_RP1_P1_[n]	0x800001050701143F	1315
IOM0.DDRPHY_DP16_WRCLK_EN_RP1_P2_[n]	0x800001050701183F	1317
IOM0.DDRPHY_DP16_WRCLK_EN_RP1_P3_[n]	0x8000010507011C3F	1319
IOM0.DDRPHY_DP16_WRCLK_EN_RP2_P0_[n]	0x800002050701103F	1430
IOM0.DDRPHY_DP16_WRCLK_EN_RP2_P1_[n]	0x800002050701143F	1432
IOM0.DDRPHY_DP16_WRCLK_EN_RP2_P2_[n]	0x800002050701183F	1434
IOM0.DDRPHY_DP16_WRCLK_EN_RP2_P3_[n]	0x8000020507011C3F	1436
IOM0.DDRPHY_DP16_WRCLK_EN_RP3_P0_[n]	0x800003050701103F	1547
IOM0.DDRPHY_DP16_WRCLK_EN_RP3_P1_[n]	0x800003050701143F	1549
IOM0.DDRPHY_DP16_WRCLK_EN_RP3_P2_[n]	0x800003050701183F	1551
IOM0.DDRPHY_DP16_WRCLK_EN_RP3_P3_[n]	0x8000030507011C3F	1553
IOM0.DDRPHY_DP16_WRCLK_PR_P0_[n]	0x800000740701103F	1225
IOM0.DDRPHY_DP16_WRCLK_PR_P1_[n]	0x800000740701143F	1225
IOM0.DDRPHY_DP16_WRCLK_PR_P2_[n]	0x800000740701183F	1225
IOM0.DDRPHY_DP16_WRCLK_PR_P3_[n]	0x8000007407011C3F	1226
IOM0.DDRPHY_DP16_WR_CNTR_STATUS0_P0_[n]	0x800000180701103F	1060
IOM0.DDRPHY_DP16_WR_CNTR_STATUS0_P1_[n]	0x800000180701143F	1061
IOM0.DDRPHY_DP16_WR_CNTR_STATUS0_P2_[n]	0x800000180701183F	1062
IOM0.DDRPHY_DP16_WR_CNTR_STATUS0_P3_[n]	0x8000001807011C3F	1063

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IOM0.DDRPHY_DP16_WR_CNTR_STATUS1_P0_[n]	0x800000190701103F	1064
IOM0.DDRPHY_DP16_WR_CNTR_STATUS1_P1_[n]	0x800000190701143F	1064
IOM0.DDRPHY_DP16_WR_CNTR_STATUS1_P2_[n]	0x800000190701183F	1064
IOM0.DDRPHY_DP16_WR_CNTR_STATUS1_P3_[n]	0x8000001907011C3F	1065
IOM0.DDRPHY_DP16_WR_CNTR_STATUS2_P0_[n]	0x8000001A0701103F	1065
IOM0.DDRPHY_DP16_WR_CNTR_STATUS2_P1_[n]	0x8000001A0701143F	1065
IOM0.DDRPHY_DP16_WR_CNTR_STATUS2_P2_[n]	0x8000001A0701183F	1066
IOM0.DDRPHY_DP16_WR_CNTR_STATUS2_P3_[n]	0x8000001A07011C3F	1066
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_0_RP0_REG_P0_[n]	0x800000380701103F	1128
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_0_RP0_REG_P1_[n]	0x800000380701143F	1128
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_0_RP0_REG_P2_[n]	0x800000380701183F	1129
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_0_RP0_REG_P3_[n]	0x8000003807011C3F	1129
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_0_RP1_REG_P0_[n]	0x800001380701103F	1333
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_0_RP1_REG_P1_[n]	0x800001380701143F	1333
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_0_RP1_REG_P2_[n]	0x800001380701183F	1333
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_0_RP1_REG_P3_[n]	0x8000013807011C3F	1334
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_0_RP2_REG_P0_[n]	0x800002380701103F	1450
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_0_RP2_REG_P1_[n]	0x800002380701143F	1450
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_0_RP2_REG_P2_[n]	0x800002380701183F	1450
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_0_RP2_REG_P3_[n]	0x8000023807011C3F	1451
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_0_RP3_REG_P0_[n]	0x800003380701103F	1567
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_0_RP3_REG_P1_[n]	0x800003380701143F	1567
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_0_RP3_REG_P2_[n]	0x800003380701183F	1567
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_0_RP3_REG_P3_[n]	0x8000033807011C3F	1568
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_10_RP0_REG_P0_[n]	0x800000420701103F	1144
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_10_RP0_REG_P1_[n]	0x800000420701143F	1144
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_10_RP0_REG_P2_[n]	0x800000420701183F	1145
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_10_RP0_REG_P3_[n]	0x8000004207011C3F	1145
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_10_RP1_REG_P0_[n]	0x800001420701103F	1349
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_10_RP1_REG_P1_[n]	0x800001420701143F	1349
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_10_RP1_REG_P2_[n]	0x800001420701183F	1349
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_10_RP1_REG_P3_[n]	0x8000014207011C3F	1350
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_10_RP2_REG_P0_[n]	0x800002420701103F	1466
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_10_RP2_REG_P1_[n]	0x800002420701143F	1466
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_10_RP2_REG_P2_[n]	0x800002420701183F	1466
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_10_RP2_REG_P3_[n]	0x8000024207011C3F	1467
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_10_RP3_REG_P0_[n]	0x800003420701103F	1583
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_10_RP3_REG_P1_[n]	0x800003420701143F	1583
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_10_RP3_REG_P2_[n]	0x800003420701183F	1583
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_10_RP3_REG_P3_[n]	0x8000034207011C3F	1584
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_11_RP0_REG_P0_[n]	0x800000430701103F	1146
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_11_RP0_REG_P1_[n]	0x800000430701143F	1146
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_11_RP0_REG_P2_[n]	0x800000430701183F	1146

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IOM0.DDRPHY_DP16_WR_DELAY_VALUE_11_RP0_REG_P3_[n]	0x8000004307011C3F	1147
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_11_RP1_REG_P0_[n]	0x800001430701103F	1350
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_11_RP1_REG_P1_[n]	0x800001430701143F	1351
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_11_RP1_REG_P2_[n]	0x800001430701183F	1351
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_11_RP1_REG_P3_[n]	0x8000014307011C3F	1351
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_11_RP2_REG_P0_[n]	0x800002430701103F	1467
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_11_RP2_REG_P1_[n]	0x800002430701143F	1468
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_11_RP2_REG_P2_[n]	0x800002430701183F	1468
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_11_RP2_REG_P3_[n]	0x8000024307011C3F	1468
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_11_RP3_REG_P0_[n]	0x800003430701103F	1584
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_11_RP3_REG_P1_[n]	0x800003430701143F	1585
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_11_RP3_REG_P2_[n]	0x800003430701183F	1585
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_11_RP3_REG_P3_[n]	0x8000034307011C3F	1585
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_12_RP0_REG_P0_[n]	0x800000440701103F	1147
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_12_RP0_REG_P1_[n]	0x800000440701143F	1148
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_12_RP0_REG_P2_[n]	0x800000440701183F	1148
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_12_RP0_REG_P3_[n]	0x8000004407011C3F	1148
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_12_RP1_REG_P0_[n]	0x800001440701103F	1352
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_12_RP1_REG_P1_[n]	0x800001440701143F	1352
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_12_RP1_REG_P2_[n]	0x800001440701183F	1353
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_12_RP1_REG_P3_[n]	0x8000014407011C3F	1353
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_12_RP2_REG_P0_[n]	0x800002440701103F	1469
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_12_RP2_REG_P1_[n]	0x800002440701143F	1469
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_12_RP2_REG_P2_[n]	0x800002440701183F	1470
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_12_RP2_REG_P3_[n]	0x8000024407011C3F	1470
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_12_RP3_REG_P0_[n]	0x800003440701103F	1586
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_12_RP3_REG_P1_[n]	0x800003440701143F	1586
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_12_RP3_REG_P2_[n]	0x800003440701183F	1587
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_12_RP3_REG_P3_[n]	0x8000034407011C3F	1587
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_13_RP0_REG_P0_[n]	0x800000450701103F	1149
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_13_RP0_REG_P1_[n]	0x800000450701143F	1149
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_13_RP0_REG_P2_[n]	0x800000450701183F	1150
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_13_RP0_REG_P3_[n]	0x8000004507011C3F	1150
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_13_RP1_REG_P0_[n]	0x800001450701103F	1353
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_13_RP1_REG_P1_[n]	0x800001450701143F	1354
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_13_RP1_REG_P2_[n]	0x800001450701183F	1354
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_13_RP1_REG_P3_[n]	0x8000014507011C3F	1355
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_13_RP2_REG_P0_[n]	0x800002450701103F	1470
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_13_RP2_REG_P1_[n]	0x800002450701143F	1471
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_13_RP2_REG_P2_[n]	0x800002450701183F	1471
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_13_RP2_REG_P3_[n]	0x8000024507011C3F	1472
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_13_RP3_REG_P0_[n]	0x800003450701103F	1587
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_13_RP3_REG_P1_[n]	0x800003450701143F	1588

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IOM0.DDRPHY_DP16_WR_DELAY_VALUE_13_RP3_REG_P2_[n]	0x800003450701183F	1588
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_13_RP3_REG_P3_[n]	0x8000034507011C3F	1589
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_14_RP0_REG_P0_[n]	0x800000460701103F	1150
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_14_RP0_REG_P1_[n]	0x800000460701143F	1151
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_14_RP0_REG_P2_[n]	0x800000460701183F	1151
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_14_RP0_REG_P3_[n]	0x8000004607011C3F	1152
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_14_RP1_REG_P0_[n]	0x800001460701103F	1355
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_14_RP1_REG_P1_[n]	0x800001460701143F	1355
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_14_RP1_REG_P2_[n]	0x800001460701183F	1356
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_14_RP1_REG_P3_[n]	0x8000014607011C3F	1356
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_14_RP2_REG_P0_[n]	0x800002460701103F	1472
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_14_RP2_REG_P1_[n]	0x800002460701143F	1472
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_14_RP2_REG_P2_[n]	0x800002460701183F	1473
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_14_RP2_REG_P3_[n]	0x8000024607011C3F	1473
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_14_RP3_REG_P0_[n]	0x800003460701103F	1589
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_14_RP3_REG_P1_[n]	0x800003460701143F	1589
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_14_RP3_REG_P2_[n]	0x800003460701183F	1590
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_14_RP3_REG_P3_[n]	0x8000034607011C3F	1590
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_15_RP0_REG_P0_[n]	0x800000470701103F	1152
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_15_RP0_REG_P1_[n]	0x800000470701143F	1152
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_15_RP0_REG_P2_[n]	0x800000470701183F	1153
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_15_RP0_REG_P3_[n]	0x8000004707011C3F	1153
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_15_RP1_REG_P0_[n]	0x800001470701103F	1357
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_15_RP1_REG_P1_[n]	0x800001470701143F	1357
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_15_RP1_REG_P2_[n]	0x800001470701183F	1357
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_15_RP1_REG_P3_[n]	0x8000014707011C3F	1358
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_15_RP2_REG_P0_[n]	0x800002470701103F	1474
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_15_RP2_REG_P1_[n]	0x800002470701143F	1474
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_15_RP2_REG_P2_[n]	0x800002470701183F	1474
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_15_RP2_REG_P3_[n]	0x8000024707011C3F	1475
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_15_RP3_REG_P0_[n]	0x800003470701103F	1591
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_15_RP3_REG_P1_[n]	0x800003470701143F	1591
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_15_RP3_REG_P2_[n]	0x800003470701183F	1591
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_15_RP3_REG_P3_[n]	0x8000034707011C3F	1592
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_16_RP0_REG_P0_[n]	0x800000480701103F	1154
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_16_RP0_REG_P1_[n]	0x800000480701143F	1154
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_16_RP0_REG_P2_[n]	0x800000480701183F	1154
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_16_RP0_REG_P3_[n]	0x8000004807011C3F	1155
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_16_RP1_REG_P0_[n]	0x800001480701103F	1358
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_16_RP1_REG_P1_[n]	0x800001480701143F	1359
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_16_RP1_REG_P2_[n]	0x800001480701183F	1359
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_16_RP1_REG_P3_[n]	0x8000014807011C3F	1359
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_16_RP2_REG_P0_[n]	0x800002480701103F	1475

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IOM0.DDRPHY_DP16_WR_DELAY_VALUE_16_RP2_REG_P1_[n]	0x800002480701143F	1476
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_16_RP2_REG_P2_[n]	0x800002480701183F	1476
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_16_RP2_REG_P3_[n]	0x8000024807011C3F	1476
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_16_RP3_REG_P0_[n]	0x800003480701103F	1592
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_16_RP3_REG_P1_[n]	0x800003480701143F	1593
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_16_RP3_REG_P2_[n]	0x800003480701183F	1593
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_16_RP3_REG_P3_[n]	0x8000034807011C3F	1593
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_18_RP0_REG_P0_[n]	0x8000004A0701103F	1155
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_18_RP0_REG_P1_[n]	0x8000004A0701143F	1156
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_18_RP0_REG_P2_[n]	0x8000004A0701183F	1156
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_18_RP0_REG_P3_[n]	0x8000004A07011C3F	1156
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_18_RP1_REG_P0_[n]	0x8000014A0701103F	1360
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_18_RP1_REG_P1_[n]	0x8000014A0701143F	1360
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_18_RP1_REG_P2_[n]	0x8000014A0701183F	1361
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_18_RP1_REG_P3_[n]	0x8000014A07011C3F	1361
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_18_RP2_REG_P0_[n]	0x8000024A0701103F	1477
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_18_RP2_REG_P1_[n]	0x8000024A0701143F	1477
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_18_RP2_REG_P2_[n]	0x8000024A0701183F	1478
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_18_RP2_REG_P3_[n]	0x8000024A07011C3F	1478
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_18_RP3_REG_P0_[n]	0x8000034A0701103F	1594
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_18_RP3_REG_P1_[n]	0x8000034A0701143F	1594
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_18_RP3_REG_P2_[n]	0x8000034A0701183F	1595
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_18_RP3_REG_P3_[n]	0x8000034A07011C3F	1595
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_1_RP0_REG_P0_[n]	0x800000390701103F	1130
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_1_RP0_REG_P1_[n]	0x800000390701143F	1130
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_1_RP0_REG_P2_[n]	0x800000390701183F	1130
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_1_RP0_REG_P3_[n]	0x8000003907011C3F	1131
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_1_RP1_REG_P0_[n]	0x800001390701103F	1334
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_1_RP1_REG_P1_[n]	0x800001390701143F	1335
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_1_RP1_REG_P2_[n]	0x800001390701183F	1335
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_1_RP1_REG_P3_[n]	0x8000013907011C3F	1335
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_1_RP2_REG_P0_[n]	0x800002390701103F	1451
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_1_RP2_REG_P1_[n]	0x800002390701143F	1452
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_1_RP2_REG_P2_[n]	0x800002390701183F	1452
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_1_RP2_REG_P3_[n]	0x8000023907011C3F	1452
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_1_RP3_REG_P0_[n]	0x800003390701103F	1568
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_1_RP3_REG_P1_[n]	0x800003390701143F	1569
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_1_RP3_REG_P2_[n]	0x800003390701183F	1569
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_1_RP3_REG_P3_[n]	0x8000033907011C3F	1569
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_20_RP0_REG_P0_[n]	0x8000004C0701103F	1157
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_20_RP0_REG_P1_[n]	0x8000004C0701143F	1157
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_20_RP0_REG_P2_[n]	0x8000004C0701183F	1158
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_20_RP0_REG_P3_[n]	0x8000004C07011C3F	1158

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IOM0.DDRPHY_DP16_WR_DELAY_VALUE_20_RP1_REG_P0_[n]	0x8000014C0701103F	1361
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_20_RP1_REG_P1_[n]	0x8000014C0701143F	1362
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_20_RP1_REG_P2_[n]	0x8000014C0701183F	1362
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_20_RP1_REG_P3_[n]	0x8000014C07011C3F	1363
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_20_RP2_REG_P0_[n]	0x8000024C0701103F	1478
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_20_RP2_REG_P1_[n]	0x8000024C0701143F	1479
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_20_RP2_REG_P2_[n]	0x8000024C0701183F	1479
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_20_RP2_REG_P3_[n]	0x8000024C07011C3F	1480
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_20_RP3_REG_P0_[n]	0x8000034C0701103F	1595
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_20_RP3_REG_P1_[n]	0x8000034C0701143F	1596
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_20_RP3_REG_P2_[n]	0x8000034C0701183F	1596
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_20_RP3_REG_P3_[n]	0x8000034C07011C3F	1597
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_22_RP0_REG_P0_[n]	0x8000004E0701103F	1158
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_22_RP0_REG_P1_[n]	0x8000004E0701143F	1159
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_22_RP0_REG_P2_[n]	0x8000004E0701183F	1159
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_22_RP0_REG_P3_[n]	0x8000004E07011C3F	1160
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_22_RP1_REG_P0_[n]	0x8000014E0701103F	1363
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_22_RP1_REG_P1_[n]	0x8000014E0701143F	1363
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_22_RP1_REG_P2_[n]	0x8000014E0701183F	1364
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_22_RP1_REG_P3_[n]	0x8000014E07011C3F	1364
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_22_RP2_REG_P0_[n]	0x8000024E0701103F	1480
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_22_RP2_REG_P1_[n]	0x8000024E0701143F	1480
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_22_RP2_REG_P2_[n]	0x8000024E0701183F	1481
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_22_RP2_REG_P3_[n]	0x8000024E07011C3F	1481
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_22_RP3_REG_P0_[n]	0x8000034E0701103F	1597
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_22_RP3_REG_P1_[n]	0x8000034E0701143F	1597
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_22_RP3_REG_P2_[n]	0x8000034E0701183F	1598
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_22_RP3_REG_P3_[n]	0x8000034E07011C3F	1598
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_2_RP0_REG_P0_[n]	0x8000003A0701103F	1131
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_2_RP0_REG_P1_[n]	0x8000003A0701143F	1132
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_2_RP0_REG_P2_[n]	0x8000003A0701183F	1132
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_2_RP0_REG_P3_[n]	0x8000003A07011C3F	1132
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_2_RP1_REG_P0_[n]	0x8000013A0701103F	1336
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_2_RP1_REG_P1_[n]	0x8000013A0701143F	1336
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_2_RP1_REG_P2_[n]	0x8000013A0701183F	1337
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_2_RP1_REG_P3_[n]	0x8000013A07011C3F	1337
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_2_RP2_REG_P0_[n]	0x8000023A0701103F	1453
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_2_RP2_REG_P1_[n]	0x8000023A0701143F	1453
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_2_RP2_REG_P2_[n]	0x8000023A0701183F	1454
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_2_RP2_REG_P3_[n]	0x8000023A07011C3F	1454
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_2_RP3_REG_P0_[n]	0x8000033A0701103F	1570
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_2_RP3_REG_P1_[n]	0x8000033A0701143F	1570
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_2_RP3_REG_P2_[n]	0x8000033A0701183F	1571

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IOM0.DDRPHY_DP16_WR_DELAY_VALUE_2_RP3_REG_P3_[n]	0x8000033A07011C3F	1571
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_3_RP0_REG_P0_[n]	0x8000003B0701103F	1133
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_3_RP0_REG_P1_[n]	0x8000003B0701143F	1133
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_3_RP0_REG_P2_[n]	0x8000003B0701183F	1134
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_3_RP0_REG_P3_[n]	0x8000003B07011C3F	1134
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_3_RP1_REG_P0_[n]	0x8000013B0701103F	1337
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_3_RP1_REG_P1_[n]	0x8000013B0701143F	1338
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_3_RP1_REG_P2_[n]	0x8000013B0701183F	1338
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_3_RP1_REG_P3_[n]	0x8000013B07011C3F	1339
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_3_RP2_REG_P0_[n]	0x8000023B0701103F	1454
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_3_RP2_REG_P1_[n]	0x8000023B0701143F	1455
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_3_RP2_REG_P2_[n]	0x8000023B0701183F	1455
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_3_RP2_REG_P3_[n]	0x8000023B07011C3F	1456
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_3_RP3_REG_P0_[n]	0x8000033B0701103F	1571
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_3_RP3_REG_P1_[n]	0x8000033B0701143F	1572
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_3_RP3_REG_P2_[n]	0x8000033B0701183F	1572
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_3_RP3_REG_P3_[n]	0x8000033B07011C3F	1573
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_4_RP0_REG_P0_[n]	0x8000003C0701103F	1134
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_4_RP0_REG_P1_[n]	0x8000003C0701143F	1135
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_4_RP0_REG_P2_[n]	0x8000003C0701183F	1135
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_4_RP0_REG_P3_[n]	0x8000003C07011C3F	1136
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_4_RP1_REG_P0_[n]	0x8000013C0701103F	1339
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_4_RP1_REG_P1_[n]	0x8000013C0701143F	1339
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_4_RP1_REG_P2_[n]	0x8000013C0701183F	1340
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_4_RP1_REG_P3_[n]	0x8000013C07011C3F	1340
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_4_RP2_REG_P0_[n]	0x8000023C0701103F	1456
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_4_RP2_REG_P1_[n]	0x8000023C0701143F	1456
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_4_RP2_REG_P2_[n]	0x8000023C0701183F	1457
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_4_RP2_REG_P3_[n]	0x8000023C07011C3F	1457
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_4_RP3_REG_P0_[n]	0x8000033C0701103F	1573
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_4_RP3_REG_P1_[n]	0x8000033C0701143F	1573
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_4_RP3_REG_P2_[n]	0x8000033C0701183F	1574
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_4_RP3_REG_P3_[n]	0x8000033C07011C3F	1574
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_5_RP0_REG_P0_[n]	0x8000003D0701103F	1136
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_5_RP0_REG_P1_[n]	0x8000003D0701143F	1136
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_5_RP0_REG_P2_[n]	0x8000003D0701183F	1137
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_5_RP0_REG_P3_[n]	0x8000003D07011C3F	1137
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_5_RP1_REG_P0_[n]	0x8000013D0701103F	1341
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_5_RP1_REG_P1_[n]	0x8000013D0701143F	1341
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_5_RP1_REG_P2_[n]	0x8000013D0701183F	1341
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_5_RP1_REG_P3_[n]	0x8000013D07011C3F	1342
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_5_RP2_REG_P0_[n]	0x8000023D0701103F	1458
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_5_RP2_REG_P1_[n]	0x8000023D0701143F	1458

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IOM0.DDRPHY_DP16_WR_DELAY_VALUE_5_RP2_REG_P2_[n]	0x8000023D0701183F	1458
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_5_RP2_REG_P3_[n]	0x8000023D07011C3F	1459
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_5_RP3_REG_P0_[n]	0x8000033D0701103F	1575
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_5_RP3_REG_P1_[n]	0x8000033D0701143F	1575
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_5_RP3_REG_P2_[n]	0x8000033D0701183F	1575
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_5_RP3_REG_P3_[n]	0x8000033D07011C3F	1576
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_6_RP0_REG_P0_[n]	0x8000003E0701103F	1138
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_6_RP0_REG_P1_[n]	0x8000003E0701143F	1138
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_6_RP0_REG_P2_[n]	0x8000003E0701183F	1138
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_6_RP0_REG_P3_[n]	0x8000003E07011C3F	1139
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_6_RP1_REG_P0_[n]	0x8000013E0701103F	1342
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_6_RP1_REG_P1_[n]	0x8000013E0701143F	1343
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_6_RP1_REG_P2_[n]	0x8000013E0701183F	1343
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_6_RP1_REG_P3_[n]	0x8000013E07011C3F	1343
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_6_RP2_REG_P0_[n]	0x8000023E0701103F	1459
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_6_RP2_REG_P1_[n]	0x8000023E0701143F	1460
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_6_RP2_REG_P2_[n]	0x8000023E0701183F	1460
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_6_RP2_REG_P3_[n]	0x8000023E07011C3F	1460
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_6_RP3_REG_P0_[n]	0x8000033E0701103F	1576
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_6_RP3_REG_P1_[n]	0x8000033E0701143F	1577
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_6_RP3_REG_P2_[n]	0x8000033E0701183F	1577
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_6_RP3_REG_P3_[n]	0x8000033E07011C3F	1577
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_7_RP0_REG_P0_[n]	0x8000003F0701103F	1139
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_7_RP0_REG_P1_[n]	0x8000003F0701143F	1140
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_7_RP0_REG_P2_[n]	0x8000003F0701183F	1140
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_7_RP0_REG_P3_[n]	0x8000003F07011C3F	1140
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_7_RP1_REG_P0_[n]	0x8000013F0701103F	1344
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_7_RP1_REG_P1_[n]	0x8000013F0701143F	1344
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_7_RP1_REG_P2_[n]	0x8000013F0701183F	1345
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_7_RP1_REG_P3_[n]	0x8000013F07011C3F	1345
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_7_RP2_REG_P0_[n]	0x8000023F0701103F	1461
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_7_RP2_REG_P1_[n]	0x8000023F0701143F	1461
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_7_RP2_REG_P2_[n]	0x8000023F0701183F	1462
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_7_RP2_REG_P3_[n]	0x8000023F07011C3F	1462
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_7_RP3_REG_P0_[n]	0x8000033F0701103F	1578
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_7_RP3_REG_P1_[n]	0x8000033F0701143F	1578
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_7_RP3_REG_P2_[n]	0x8000033F0701183F	1579
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_7_RP3_REG_P3_[n]	0x8000033F07011C3F	1579
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_8_RP0_REG_P0_[n]	0x800000400701103F	1141
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_8_RP0_REG_P1_[n]	0x800000400701143F	1141
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_8_RP0_REG_P2_[n]	0x800000400701183F	1142
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_8_RP0_REG_P3_[n]	0x8000004007011C3F	1142
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_8_RP1_REG_P0_[n]	0x800001400701103F	1345

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IOM0.DDRPHY_DP16_WR_DELAY_VALUE_8_RP1_REG_P1_[n]	0x800001400701143F	1346
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_8_RP1_REG_P2_[n]	0x800001400701183F	1346
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_8_RP1_REG_P3_[n]	0x8000014007011C3F	1347
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_8_RP2_REG_P0_[n]	0x800002400701103F	1462
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_8_RP2_REG_P1_[n]	0x800002400701143F	1463
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_8_RP2_REG_P2_[n]	0x800002400701183F	1463
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_8_RP2_REG_P3_[n]	0x8000024007011C3F	1464
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_8_RP3_REG_P0_[n]	0x800003400701103F	1579
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_8_RP3_REG_P1_[n]	0x800003400701143F	1580
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_8_RP3_REG_P2_[n]	0x800003400701183F	1580
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_8_RP3_REG_P3_[n]	0x8000034007011C3F	1581
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_9_RP0_REG_P0_[n]	0x800000410701103F	1142
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_9_RP0_REG_P1_[n]	0x800000410701143F	1143
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_9_RP0_REG_P2_[n]	0x800000410701183F	1143
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_9_RP0_REG_P3_[n]	0x8000004107011C3F	1144
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_9_RP1_REG_P0_[n]	0x800001410701103F	1347
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_9_RP1_REG_P1_[n]	0x800001410701143F	1347
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_9_RP1_REG_P2_[n]	0x800001410701183F	1348
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_9_RP1_REG_P3_[n]	0x8000014107011C3F	1348
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_9_RP2_REG_P0_[n]	0x800002410701103F	1464
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_9_RP2_REG_P1_[n]	0x800002410701143F	1464
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_9_RP2_REG_P2_[n]	0x800002410701183F	1465
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_9_RP2_REG_P3_[n]	0x8000024107011C3F	1465
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_9_RP3_REG_P0_[n]	0x800003410701103F	1581
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_9_RP3_REG_P1_[n]	0x800003410701143F	1581
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_9_RP3_REG_P2_[n]	0x800003410701183F	1582
IOM0.DDRPHY_DP16_WR_DELAY_VALUE_9_RP3_REG_P3_[n]	0x8000034107011C3F	1582
IOM0.DDRPHY_DP16_WR_ERROR0_P0_[n]	0x8000001B0701103F	1066
IOM0.DDRPHY_DP16_WR_ERROR0_P1_[n]	0x8000001B0701143F	1067
IOM0.DDRPHY_DP16_WR_ERROR0_P2_[n]	0x8000001B0701183F	1068
IOM0.DDRPHY_DP16_WR_ERROR0_P3_[n]	0x8000001B07011C3F	1069
IOM0.DDRPHY_DP16_WR_ERROR_MASK0_P0_[n]	0x8000001C0701103F	1070
IOM0.DDRPHY_DP16_WR_ERROR_MASK0_P1_[n]	0x8000001C0701143F	1071
IOM0.DDRPHY_DP16_WR_ERROR_MASK0_P2_[n]	0x8000001C0701183F	1072
IOM0.DDRPHY_DP16_WR_ERROR_MASK0_P3_[n]	0x8000001C07011C3F	1073
IOM0.DDRPHY_DP16_WR_LVL_STATUS0_P0_[n]	0x800000170701103F	1058
IOM0.DDRPHY_DP16_WR_LVL_STATUS0_P1_[n]	0x800000170701143F	1058
IOM0.DDRPHY_DP16_WR_LVL_STATUS0_P2_[n]	0x800000170701183F	1059
IOM0.DDRPHY_DP16_WR_LVL_STATUS0_P3_[n]	0x8000001707011C3F	1060
IOM0.DDRPHY_DP16_WR_VREF_CONFIG0_P0_[n]	0x8000006C0701103F	1210
IOM0.DDRPHY_DP16_WR_VREF_CONFIG0_P1_[n]	0x8000006C0701143F	1211
IOM0.DDRPHY_DP16_WR_VREF_CONFIG0_P2_[n]	0x8000006C0701183F	1212
IOM0.DDRPHY_DP16_WR_VREF_CONFIG0_P3_[n]	0x8000006C07011C3F	1212

Mnemonic	Address	Page
IOM0.DDRPHY_DP16_WR_VREF_CONFIG1_P0_[n]	0x800000EC0701103F	1292
IOM0.DDRPHY_DP16_WR_VREF_CONFIG1_P1_[n]	0x800000EC0701143F	1293
IOM0.DDRPHY_DP16_WR_VREF_CONFIG1_P2_[n]	0x800000EC0701183F	1293
IOM0.DDRPHY_DP16_WR_VREF_CONFIG1_P3_[n]	0x800000EC07011C3F	1294
IOM0.DDRPHY_DP16_WR_VREF_ERROR0_P0_[n]	0x800000AE0701103F	1273
IOM0.DDRPHY_DP16_WR_VREF_ERROR0_P1_[n]	0x800000AE0701143F	1274
IOM0.DDRPHY_DP16_WR_VREF_ERROR0_P2_[n]	0x800000AE0701183F	1275
IOM0.DDRPHY_DP16_WR_VREF_ERROR0_P3_[n]	0x800000AE07011C3F	1276
IOM0.DDRPHY_DP16_WR_VREF_ERROR1_P0_[n]	0x800000AF0701103F	1278
IOM0.DDRPHY_DP16_WR_VREF_ERROR1_P1_[n]	0x800000AF0701143F	1279
IOM0.DDRPHY_DP16_WR_VREF_ERROR1_P2_[n]	0x800000AF0701183F	1280
IOM0.DDRPHY_DP16_WR_VREF_ERROR1_P3_[n]	0x800000AF07011C3F	1281
IOM0.DDRPHY_DP16_WR_VREF_ERROR_MASK0_P0_[n]	0x800000FB0701103F	1301
IOM0.DDRPHY_DP16_WR_VREF_ERROR_MASK0_P1_[n]	0x800000FB0701143F	1302
IOM0.DDRPHY_DP16_WR_VREF_ERROR_MASK0_P2_[n]	0x800000FB0701183F	1303
IOM0.DDRPHY_DP16_WR_VREF_ERROR_MASK0_P3_[n]	0x800000FB07011C3F	1304
IOM0.DDRPHY_DP16_WR_VREF_ERROR_MASK1_P0_[n]	0x800000FA0701103F	1296
IOM0.DDRPHY_DP16_WR_VREF_ERROR_MASK1_P1_[n]	0x800000FA0701143F	1297
IOM0.DDRPHY_DP16_WR_VREF_ERROR_MASK1_P2_[n]	0x800000FA0701183F	1298
IOM0.DDRPHY_DP16_WR_VREF_ERROR_MASK1_P3_[n]	0x800000FA07011C3F	1299
IOM0.DDRPHY_DP16_WR_VREF_STATUS0_P0_[n]	0x8000002E0701103F	1114
IOM0.DDRPHY_DP16_WR_VREF_STATUS0_P1_[n]	0x8000002E0701143F	1114
IOM0.DDRPHY_DP16_WR_VREF_STATUS0_P2_[n]	0x8000002E0701183F	1114
IOM0.DDRPHY_DP16_WR_VREF_STATUS0_P3_[n]	0x8000002E07011C3F	1114
IOM0.DDRPHY_DP16_WR_VREF_STATUS1_P0_[n]	0x8000002F0701103F	1115
IOM0.DDRPHY_DP16_WR_VREF_STATUS1_P1_[n]	0x8000002F0701143F	1115
IOM0.DDRPHY_DP16_WR_VREF_STATUS1_P2_[n]	0x8000002F0701183F	1115
IOM0.DDRPHY_DP16_WR_VREF_STATUS1_P3_[n]	0x8000002F07011C3F	1116
IOM0.DDRPHY_DP16_WR_VREF_VALUE0_RANK_PAIR0_P0_[n]	0x8000005E0701103F	1181
IOM0.DDRPHY_DP16_WR_VREF_VALUE0_RANK_PAIR0_P1_[n]	0x8000005E0701143F	1182
IOM0.DDRPHY_DP16_WR_VREF_VALUE0_RANK_PAIR0_P2_[n]	0x8000005E0701183F	1183
IOM0.DDRPHY_DP16_WR_VREF_VALUE0_RANK_PAIR0_P3_[n]	0x8000005E07011C3F	1183
IOM0.DDRPHY_DP16_WR_VREF_VALUE0_RANK_PAIR1_P0_[n]	0x8000015E0701103F	1386
IOM0.DDRPHY_DP16_WR_VREF_VALUE0_RANK_PAIR1_P1_[n]	0x8000015E0701143F	1387
IOM0.DDRPHY_DP16_WR_VREF_VALUE0_RANK_PAIR1_P2_[n]	0x8000015E0701183F	1387
IOM0.DDRPHY_DP16_WR_VREF_VALUE0_RANK_PAIR1_P3_[n]	0x8000015E07011C3F	1388
IOM0.DDRPHY_DP16_WR_VREF_VALUE0_RANK_PAIR2_P0_[n]	0x8000025E0701103F	1503
IOM0.DDRPHY_DP16_WR_VREF_VALUE0_RANK_PAIR2_P1_[n]	0x8000025E0701143F	1504
IOM0.DDRPHY_DP16_WR_VREF_VALUE0_RANK_PAIR2_P2_[n]	0x8000025E0701183F	1504
IOM0.DDRPHY_DP16_WR_VREF_VALUE0_RANK_PAIR2_P3_[n]	0x8000025E07011C3F	1505
IOM0.DDRPHY_DP16_WR_VREF_VALUE0_RANK_PAIR3_P0_[n]	0x8000035E0701103F	1620
IOM0.DDRPHY_DP16_WR_VREF_VALUE0_RANK_PAIR3_P1_[n]	0x8000035E0701143F	1621
IOM0.DDRPHY_DP16_WR_VREF_VALUE0_RANK_PAIR3_P2_[n]	0x8000035E0701183F	1621

The DP16 registers are listed in the following tables.

Register Name	**DP16 DQ Bit Enable 0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQ_BIT_ENABLE0_P0_[n]
Address	800000000701103F (SCOM), +0x0400_0000_0000
Description	A DP16 has 16 possible single-ended data pins that can send or receive data. This register is used to enable and disable each of the 16 pins for data sending or receiving. Any pins on the DP16 that are used as strobes or clocks to capture the data must not be marked as enabled in this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DATA_BIT_ENABLE_0_15: 1 = Indicates that the DP16 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. 0 = Indicates that the DP16 bit is not used to send or receive data. Bit 48 controls MEMINTD00B(n). Bit 49 controls MEMINTD01B(n). Bit 50 controls MEMINTD02B(n). ... Bit 63 controls MEMINTD15B(n). where n is the DP16 instance number. Note: For correct operation of the coarse read alignment algorithm, a minimum of 3 bidirectional data bits must be enabled (and not disabled) in each nibble (0 - 3, 4 - 7, 8 - 11, and 12 - 15) to be calibrated.

Register Name	DP16 DQ Bit Enable 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQ_BIT_ENABLE0_P1_[n]
Address	800000000701143F (SCOM), +0x0400_0000_0000
Description	A DP16 has 16 possible single-ended data pins that can send or receive data. This register is used to enable and disable each of the 16 pins for data sending or receiving. Any pins on the DP16 that are used as strobes or clocks to capture the data must not be marked as enabled in this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DATA_BIT_ENABLE_0_15: 1 = Indicates that the DP16 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. 0 = Indicates that the DP16 bit is not used to send or receive data. Bit 48 controls MEMINTD00B(n). Bit 49 controls MEMINTD01B(n). Bit 50 controls MEMINTD02B(n). ... Bit 63 controls MEMINTD15B(n). where n is the DP16 instance number. Note: For correct operation of the coarse read alignment algorithm, a minimum of 3 bidirectional data bits must be enabled (and not disabled) in each nibble (0 - 3, 4 - 7, 8 - 11, and 12 - 15) to be calibrated.

Register Name	DP16 DQ Bit Enable 0 Register [n] (n=0:4)
Mnemonic	IOM0. DDRPHY_DP16_DQ_BIT_ENABLE0_P2_[n]
Address	800000000701183F (SCOM), +0x0400_0000_0000
Description	A DP16 has 16 possible single-ended data pins that can send or receive data. This register is used to enable and disable each of the 16 pins for data sending or receiving. Any pins on the DP16 that are used as strobes or clocks to capture the data must not be marked as enabled in this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DATA_BIT_ENABLE_0_15: 1 = Indicates that the DP16 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. 0 = Indicates that the DP16 bit is not used to send or receive data. Bit 48 controls MEMINTD00B(n). Bit 49 controls MEMINTD01B(n). Bit 50 controls MEMINTD02B(n). ... Bit 63 controls MEMINTD15B(n). where n is the DP16 instance number. Note: For correct operation of the coarse read alignment algorithm, a minimum of 3 bidirectional data bits must be enabled (and not disabled) in each nibble (0 - 3, 4 - 7, 8 - 11, and 12 - 15) to be calibrated.

Register Name	**DP16 DQ Bit Enable 0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQ_BIT_ENABLE0_P3_[n]
Address	8000000007011C3F (SCOM), +0x0400_0000_0000
Description	A DP16 has 16 possible single-ended data pins that can send or receive data. This register is used to enable and disable each of the 16 pins for data sending or receiving. Any pins on the DP16 that are used as strobes or clocks to capture the data must not be marked as enabled in this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	DATA_BIT_ENABLE_0_15: 1 = Indicates that the DP16 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. 0 = Indicates that the DP16 bit is not used to send or receive data. Bit 48 controls MEMINTD00B(n). Bit 49 controls MEMINTD01B(n). Bit 50 controls MEMINTD02B(n). ... Bit 63 controls MEMINTD15B(n). where n is the DP16 instance number. Note: For correct operation of the coarse read alignment algorithm, a minimum of 3 bidirectional data bits must be enabled (and not disabled) in each nibble (0 - 3, 4 - 7, 8 - 11, and 12 - 15) to be calibrated.

Register Name	**DP16 DFT/PDA Control Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DFT_PDA_CONTROL_P0_[n]
Address	800000010701103F (SCOM), +0x0400_0000_0000
Description	This register provides design for test (DFT) and per DRAM addressability (PDA) controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:55	RW	Reserved. This field must remain at the reset value.
56	RW	DFT_FORCE_OUTPUTS: 1 = The 24 outputs of the DP16 are forced to a low-impedance state when the corresponding DATA_BIT_ENABLE bit is 1b. They are forced to a high-impedance state when the corresponding DATA_BIT_ENABLE bit is 0b. When a DP16 output is forced to a low-impedance state, the value driven out, 1b or 0b, is determined by the corresponding bit value in the DP16 DQ Force Outputs and DP16 Configuration 0 Registers. 0 = The 24 outputs of the DP16 are not forced.
57	RW	DFT_PRBS7_GEN_EN: 1 = The 24 outputs of the DP16 are forced to a low-impedance state when the corresponding DATA_BIT_ENABLE bit is 1b or when enabled as a write clock in the DP16 Write Clock Enable and Clock Selection Register. An output is forced to a high-impedance state when the corresponding DATA_BIT_ENABLE bit is 0b and not enabled as a write clock. When a pin is enabled via the corresponding DATA_BIT_ENABLE bit, the PRBS7 pattern is driven out. When a pin is enabled as a clock, a free running clock is driven out. Note: When a clock is enabled as differential, both outputs drive out the same free running clock. The two clocks are in-phase, synchronous clocks; they are edge-aligned clocks, and are not differential. 0 = The 24 outputs of the DP16 are not forced.
58	RW	WRAPSEL: This bit is connected directly to the S0WRAPSEL and S1WRAPSEL input pins of the analog core. This bit is used during wrap tests of the analog core. This bit must be 0b for proper functional operation.
59	RW	Reserved.

Bits	SCOM	Field Mnemonic: Description
60	RW	MRS_CMD_DATA_N0: This is the value that is driven by MEMINT_D00_B - MEMINT_D03_B when a double data rate 4 (DDR4) mode register set (MRS) command is detected, and PDA mode is enabled, in the PC Mode 3 Register bit A4. This represents an MR3 register of the primary rank within a rank group that has been programmed to enable PDA mode. It is also used in PBA mode.
61	RW	MRS_CMD_DATA_N1: This is the value that is driven by MEMINT_D04_B - MEMINT_D07_B when a DDR4 MRS command is detected, and PDA mode is enabled, in the PC Mode 3 Register bit A4. This represents an MR3 register of the primary rank within a rank group that has been programmed to enable PDA mode. It is also used in PBA mode.
62	RW	MRS_CMD_DATA_N2: This is the value that is driven by MEMINT_D08_B - MEMINT_D11_B when a DDR4 MRS command is detected, and PDA mode is enabled, in the PC Mode 3 Register bit A4. This represents an MR3 register of the primary rank within a rank group that has been programmed to enable PDA mode. It is also used in PBA mode.
63	RW	MRS_CMD_DATA_N3: This is the value that is driven by MEMINT_D12_B - MEMINT_D15_B when a DDR4 MRS command is detected, and PDA mode is enabled, in the PC Mode 3 Register bit A4. This represents an MR3 register of the primary rank within a rank group that has been programmed to enable PDA mode. It is also used in PBA mode.

Register Name	DP16 DFT/PDA Control Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DFT_PDA_CONTROL_P1_[n]
Address	800000010701143F (SCOM), +0x0400_0000_0000
Description	This register provides DFT and PDA controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:55	RW	Reserved. This field must remain at the reset value.
56	RW	DFT_FORCE_OUTPUTS: 1 = The 24 outputs of the DP16 are forced to a low-impedance state when the corresponding DATA_BIT_ENABLE bit is 1b. They are forced to a high-impedance state when the corresponding DATA_BIT_ENABLE bit is 0b. When a DP16 output is forced to a low-impedance state, the value driven out, 1b or 0b, is determined by the corresponding bit value in the DP16 DQ Force Outputs and DP16 Config0 Registers. 0 = The 24 outputs of the DP16 are not forced.
57	RW	DFT_PRBS7_GEN_EN: 1 = The 24 outputs of the DP16 are forced to a low-impedance state when the corresponding DATA_BIT_ENABLE bit is 1b or when enabled as a write clock in the DP16 Write Clock Enable and Clock Selection Register. An output is forced to a high-impedance state when the corresponding DATA_BIT_ENABLE bit is 0b and not enabled as a write clock. When a pin is enabled via the corresponding DATA_BIT_ENABLE bit, the PRBS7 pattern is driven out. When a pin is enabled as a clock, a free running clock is driven out. Note: When a clock is enabled as differential, both outputs drive out the same free running clock. The two clocks are in-phase, synchronous clocks; they are edge-aligned clocks, and are not differential. 0 = The 24 outputs of the DP16 are not forced.
58	RW	WRAPSEL: This bit is connected directly to the S0WRAPSEL and S1WRAPSEL input pins of the analog core. This bit is used during wrap tests of the analog core. This bit must be 0b for proper functional operation.
59	RW	Reserved.
60	RW	MRS_CMD_DATA_N0: This is the value that is driven by MEMINT_D00_B - MEMINT_D03_B when a DDR4 MRS command is detected, and PDA mode is enabled, in the PC Mode 3 Register bit A4. This represents an MR3 register of the primary rank within a rank group that has been programmed to enable PDA mode. It is also used in PBA mode.

Bits	SCOM	Field Mnemonic: Description
61	RW	MRS_CMD_DATA_N1: This is the value that is driven by MEMINT_D04_B - MEMINT_D07_B when a DDR4 MRS command is detected, and PDA mode is enabled, in the PC Mode 3 Register bit A4. This represents an MR3 register of the primary rank within a rank group that has been programmed to enable PDA mode. It is also used in PBA mode.
62	RW	MRS_CMD_DATA_N2: This is the value that is driven by MEMINT_D08_B - MEMINT_D11_B when a DDR4 MRS command is detected, and PDA mode is enabled, in the PC Mode 3 Register bit A4. This represents an MR3 register of the primary rank within a rank group that has been programmed to enable PDA mode. It is also used in PBA mode.
63	RW	MRS_CMD_DATA_N3: This is the value that is driven by MEMINT_D12_B - MEMINT_D15_B when a DDR4 MRS command is detected, and PDA mode is enabled, in the PC Mode 3 Register bit A4. This represents an MR3 register of the primary rank within a rank group that has been programmed to enable PDA mode. It is also used in PBA mode.

Register Name	**DP16 DFT/PDA Control Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DFT_PDA_CONTROL_P2_[n]
Address	800000010701183F (SCOM), +0x0400_0000_0000
Description	This register provides DFT and PDA controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:55	RW	Reserved. This field must remain at the reset value.
56	RW	DFT_FORCE_OUTPUTS: 1 = The 24 outputs of the DP16 are forced to a low-impedance state when the corresponding DATA_BIT_ENABLE bit is 1b. They are forced to a high-impedance state when the corresponding DATA_BIT_ENABLE bit is 0b. When a DP16 output is forced to a low-impedance state, the value driven out, 1b or 0b, is determined by the corresponding bit value in the DP16 DQ Force Outputs and DP16 Configuration 0 Registers. 0 = The 24 outputs of the DP16 are not forced.
57	RW	DFT_PRBS7_GEN_EN: 1 = The 24 outputs of the DP16 are forced to a low-impedance state when the corresponding DATA_BIT_ENABLE bit is 1b or when enabled as a write clock in the DP16 Write Clock Enable and Clock Selection Register. An output is forced to a high-impedance state when the corresponding DATA_BIT_ENABLE bit is 0b and not enabled as a write clock. When a pin is enabled via the corresponding DATA_BIT_ENABLE bit, the PRBS7 pattern is driven out. When a pin is enabled as a clock, a free running clock is driven out. Note: When a clock is enabled as differential, both outputs drive out the same free running clock. The two clocks are in-phase, synchronous clocks; they are edge-aligned clocks, and are not differential. 0 = The 24 outputs of the DP16 are not forced.
58	RW	WRAPSEL: This bit is connected directly to the S0WRAPSEL and S1WRAPSEL input pins of the analog core. This bit is used during wrap tests of the analog core. This bit must be 0b for proper functional operation.
59	RW	Reserved.
60	RW	MRS_CMD_DATA_N0: This is the value that is driven by MEMINT_D00_B - MEMINT_D03_B when a DDR4 MRS command is detected, and PDA mode is enabled, in the PC Mode 3 Register bit A4. This represents an MR3 register of the primary rank within a rank group that has been programmed to enable PDA mode. It is also used in PBA mode.
61	RW	MRS_CMD_DATA_N1: This is the value that is driven by MEMINT_D04_B - MEMINT_D07_B when a DDR4 MRS command is detected, and PDA mode is enabled, in the PC Mode 3 Register bit A4. This represents an MR3 register of the primary rank within a rank group that has been programmed to enable PDA mode. It is also used in PBA mode.

Bits	SCOM	Field Mnemonic: Description
62	RW	MRS_CMD_DATA_N2: This is the value that is driven by MEMINT_D08_B - MEMINT_D11_B when a DDR4 MRS command is detected, and PDA mode is enabled, in the PC Mode 3 Register bit A4. This represents an MR3 register of the primary rank within a rank group that has been programmed to enable PDA mode. It is also used in PBA mode.
63	RW	MRS_CMD_DATA_N3: This is the value that is driven by MEMINT_D12_B - MEMINT_D15_B when a DDR4 MRS command is detected, and PDA mode is enabled, in the PC Mode 3 Register bit A4. This represents an MR3 register of the primary rank within a rank group that has been programmed to enable PDA mode. It is also used in PBA mode.

Register Name	**DP16 DFT/PDA Control Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DFT_PDA_CONTROL_P3_[n]
Address	8000000107011C3F (SCOM), +0x0400_0000_0000
Description	This register provides DFT and PDA controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48:55	RW	Reserved. This field must remain at the reset value.
56	RW	DFT_FORCE_OUTPUTS: 1 = The 24 outputs of the DP16 are forced to a low-impedance state when the corresponding DATA_BIT_ENABLE bit is 1b. They are forced to a high-impedance state when the corresponding DATA_BIT_ENABLE bit is 0b. When a DP16 output is forced to a low-impedance state, the value driven out, 1b or 0b, is determined by the corresponding bit value in the DP16 DQ Force Outputs and DP16 Configuration 0 Registers. 0 = The 24 outputs of the DP16 are not forced.
57	RW	DFT_PRBS7_GEN_EN: 1 = The 24 outputs of the DP16 are forced to a low-impedance state when the corresponding DATA_BIT_ENABLE bit is 1b or when enabled as a write clock in the DP16 Write Clock Enable and Clock Selection Register. An output is forced to a high-impedance state when the corresponding DATA_BIT_ENABLE bit is 0b and not enabled as a write clock. When a pin is enabled via the corresponding DATA_BIT_ENABLE bit, the PRBS7 pattern is driven out. When a pin is enabled as a clock, a free running clock is driven out. Note: When a clock is enabled as differential, both outputs drive out the same free running clock. The two clocks are in-phase, synchronous clocks; they are edge-aligned clocks, and are not differential. 0 = The 24 outputs of the DP16 are not forced.
58	RW	WRAPSEL: This bit is connected directly to the S0WRAPSEL and S1WRAPSEL input pins of the analog core. This bit is used during wrap tests of the analog core. This bit must be 0b for proper functional operation.
59	RW	Reserved.
60	RW	MRS_CMD_DATA_N0: This is the value that is driven by MEMINT_D00_B - MEMINT_D03_B when a DDR4 MRS command is detected, and PDA mode is enabled, in the PC Mode 3 Register bit A4. This represents an MR3 register of the primary rank within a rank group that has been programmed to enable PDA mode. It is also used in PBA mode.
61	RW	MRS_CMD_DATA_N1: This is the value that is driven by MEMINT_D04_B - MEMINT_D07_B when a DDR4 MRS command is detected, and PDA mode is enabled, in the PC Mode 3 Register bit A4. This represents an MR3 register of the primary rank within a rank group that has been programmed to enable PDA mode. It is also used in PBA mode.
62	RW	MRS_CMD_DATA_N2: This is the value that is driven by MEMINT_D08_B - MEMINT_D11_B when a DDR4 MRS command is detected, and PDA mode is enabled, in the PC Mode 3 Register bit A4. This represents an MR3 register of the primary rank within a rank group that has been programmed to enable PDA mode. It is also used in PBA mode.

Bits	SCOM	Field Mnemonic: Description
63	RW	MRS_CMD_DATA_N3: This is the value that is driven by MEMINT_D12_B - MEMINT_D15_B when a DDR4 MRS command is detected, and PDA mode is enabled, in the PC Mode 3 Register bit A4. This represents an MR3 register of the primary rank within a rank group that has been programmed to enable PDA mode. It is also used in PBA mode.

Register Name	DP16 DQ Force Outputs Register [n] (n=0:4)
Mnemonic	DDRPHY_DP16_DQ_FORCE_OUTPUTS_P0_[n]
Address	800000020701103F (SCOM), +0x0400_0000_0000
Description	This register is used for diagnostic purposes only. It defines the voltage levels to be driven out of the data (DQ) bits when DFT_FORCE_OUTPUTS = 1 in the DP16 DFT/PDA Control Register [n] (n=0:4).

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	DQ_FORCE_VALUE_0_15: When set to '0', a low voltage is driven out of the associated DQ pin if DFT_FORCE_OUTPUTS = 1 in the DP16 DFT/PDA Control Register [n] (n=0:4). When set to '1', a high voltage is driven out of the associated DQ pin if DFT_FORCE_OUTPUTS = 1 in the DP16 DFT/PDA Control Register [n] (n=0:4).

Register Name	DP16 DQ Force Outputs Register [n] (n=0:4)
Mnemonic	DDRPHY_DP16_DQ_FORCE_OUTPUTS_P1_[n]
Address	800000020701143F (SCOM), +0x0400_0000_0000
Description	It defines the voltage levels to be driven out of the DQ bits when DFT_FORCE_OUTPUTS = 1 in the DP16 DFT/PDA Control Register [n] (n=0:4).

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	DQ_FORCE_VALUE_0_15: When set to '0', a low voltage is driven out of the associated DQ pin if DFT_FORCE_OUTPUTS = 1 in the DP16 DFT/PDA Control Register [n] (n=0:4). When set to '1', a high voltage is driven out of the associated DQ pin if DFT_FORCE_OUTPUTS = 1 in the DP16 DFT/PDA Control Register [n] (n=0:4).

Register Name	DP16 DQ Force Outputs Register [n] (n=0:4)
Mnemonic	DDRPHY_DP16_DQ_FORCE_OUTPUTS_P2_[n]
Address	800000020701183F (SCOM), +0x0400_0000_0000
Description	It defines the voltage levels to be driven out of the DQ bits when DFT_FORCE_OUTPUTS = 1 in the DP16 DFT/PDA Control Register [n] (n=0:4).

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	DQ_FORCE_VALUE_0_15: When set to ‘0’, a low voltage is driven out of the associated DQ pin if DFT_FORCE_OUTPUTS = 1 in the DP16 DFT/PDA Control Register [n] (n=0:4). When set to ‘1’, a high voltage is driven out of the associated DQ pin if DFT_FORCE_OUTPUTS = 1 in the DP16 DFT/PDA Control Register [n] (n=0:4).

Register Name	**DP16 DQ Force Outputs Register [n] (n=0:4)**
Mnemonic	DDRPHY_DP16_DQ_FORCE_OUTPUTS_P3_[n]
Address	8000000207011C3F (SCOM), +0x0400_0000_0000
Description	It defines the voltage levels to be driven out of the DQ bits when DFT_FORCE_OUTPUTS = 1 in the DP16 DFT/PDA Control Register [n] (n=0:4).

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	DQ_FORCE_VALUE_0_15: When set to ‘0’, a low voltage is driven out of the associated DQ pin if DFT_FORCE_OUTPUTS = 1 in the DP16 DFT/PDA Control Register [n] (n=0:4). When set to ‘1’, a high voltage is driven out of the associated DQ pin if DFT_FORCE_OUTPUTS = 1 in the DP16 DFT/PDA Control Register [n] (n=0:4).

Register Name	**DP16 Configuration 0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_CONFIG0_P0_[n]
Address	800000030701103F (SCOM), +0x0400_0000_0000
Description	This is the DP16 configuration register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	DD2_COARSE_OF_DISABLE: 0 = Enable the DD2 function for reporting of write delay overflow errors in coarse alignment. 1 = Enable the DD1 function.
49	RW	DD2_DBDIS_DQS_DISABLE: 0 = Enable the DD2 function to allow setting data strobe (DQS) disable bits when DQS calibration is detected. 1 = Enable the DD1 function.
50	RW	DD2_SPARE_L2SFF_CG_DISABLE: 0 = Enable the DD2 function of clock gating on spare L2 flip flop (L2SFF) latches. 1 = Enable the DD1 function.
51	RW	FLUSH: Manufacturing macro test control for ANALOG. This bit controls whether the transmit FIFO is flushed or not. When flushed, half-rate data is no longer valid.
52	RW	DQS_FORCE_VALUE: This bit is relevant only when DFT_FORCE_OUTPUTS = 1 in the DP16 DFT/PDA Control Register [n] (n=0:4). 0 = A low voltage is driven on all eight DQS pins. 1 = A high voltage is driven on all eight DQS pins.
53	RW	P8_DD2_FIX_DIS: 0 = Enable POWER8 DD2 function. 1 = Enable POWER8 DD1 function.

Bits	SCOM	Field Mnemonic: Description
54	RW	INIT_IO: Enables the DC level translator in front of the TX output stages, which initialize the top-plate voltage of the fly cap in the AC level translator at start up. This must be applied for a minimum of five clock cycles after startup, and before the I/Os can be used. This requirement also applies to all manufacturing test modes.
55	RW	ADVANCE_PING_PONG: This bit must be set to 1b due to the timing requirements of the analog core. 0 = The DQS (write strobe) phase rotator multiplex select is not advanced. 1 = The DQS (write strobe) phase rotator multiplex select switches one system clock (SysClk) clock cycle early.
56	RW	WL_ADVANCE_DISABLE: 0 = Enable the 1/2 unit interval (UI) advance of the second-to-last sample in the write-leveling calibration algorithm. 1 = Disable the 1/2 UI advance of the second-to-last sample in the write-leveling calibration algorithm.
57	RW	DISABLE_PING_PONG: Reserved. This bit must always be written to zero. 0 = The DQS (write strobe) write phase rotator values toggle between the two possible phase rotator values when the rank pair written is not the same as the last rank pair that was written. 1 = The DQS (write strobe) write phase rotator values do not toggle. Each DQS (write strobe) output uses the corresponding phase rotator.
58	RW	DELAY_PING_PONG_HALF: This bit must be set to 1b due to the timing requirements of the analog core. 0 = The DQS (write strobe) phase rotator multiplex select is not delayed. 1 = The DQS (write strobe) phase rotator multiplex select is not 1/2 SysClk clock cycle later. When this bit is set to 1b, and the ADVANCE_PING_PONG bit is set to 1b, the phase rotator multiplex select switches 1/2 a SysClk clock cycle early.
59:63	RW	ATESTSEL_0_4: Lowest level of analog test pin (ATEST) multiplex selection.

Register Name	DP16 Configuration 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_CONFIG0_P1_[n]
Address	800000030701143F (SCOM), +0x0400_0000_0000
Description	This is the DP16 configuration register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	DD2_COARSE_OF_DISABLE: 0 = Enable the DD2 function for reporting of write delay overflow errors in coarse alignment. 1 = Enable the DD1 function.
49	RW	DD2_DBDIS_DQS_DISABLE: 0 = Enable the DD2 function to allow setting DQS disable bits when DQS calibration is detected. 1 = Enable the DD1 function.
50	RW	DD2_SPARE_L2SFF_CG_DISABLE: 0 = Enable the DD2 function of clock gating on spare L2SFF latches. 1 = Enable the DD1 function.
51	RW	FLUSH: Manufacturing macro test control for ANALOG. This bit controls whether the transmit FIFO is flushed or not. When flushed, half-rate data is no longer valid.
52	RW	DQS_FORCE_VALUE: This bit is relevant only when DFT_FORCE_OUTPUTS = 1 in the DP16 DFT/PDA Control Register [n] (n=0:4). 0 = A low voltage is driven on all eight DQS pins. 1 = A high voltage is driven on all eight DQS pins.
53	RW	P8_DD2_FIX_DIS: 0 = Enable POWER8 DD2 function. 1 = Enable POWER8 DD1 function.

Bits	SCOM	Field Mnemonic: Description
54	RW	INIT_IO: Enables the DC level translator in front of the TX output stages, which initialize the top-plate voltage of the fly cap in the AC level translator at start up. This must be applied for a minimum of five clock cycles after startup, and before the I/Os can be used. This requirement also applies to all manufacturing test modes.
55	RW	ADVANCE_PING_PONG: This bit must be set to 1b due to the timing requirements of the analog core. 0 = The DQS (write strobe) phase rotator multiplex select is not advanced. 1 = The DQS (write strobe) phase rotator multiplex select switches one SysClk clock cycle early.
56	RW	WL_ADVANCE_DISABLE: 0 = Enable the 1/2 UI advance of the second-to-last sample in the write-leveling calibration algorithm. 1 = Disable the 1/2 UI advance of the second-to-last sample in the write-leveling calibration algorithm.
57	RW	DISABLE_PING_PONG: Reserved. This bit must always be written to zero. 0 = The DQS (write strobe) write phase rotator values toggle between the two possible phase rotator values when the rank pair written is not the same as the last rank pair that was written. 1 = The DQS (write strobe) write phase rotator values do not toggle. Each DQS (write strobe) output uses the corresponding phase rotator.
58	RW	DELAY_PING_PONG_HALF: This bit must be set to 1b due to the timing requirements of the analog core. 0 = The DQS (write strobe) phase rotator multiplex select is not delayed. 1 = The DQS (write strobe) phase rotator multiplex select is not 1/2 SysClk clock cycle later. When this bit is set to 1b, and the ADVANCE_PING_PONG bit is set to 1b, the phase rotator multiplex select switches 1/2 a SysClk clock cycle early.
59:63	RW	ATESTSEL_0_4: Lowest level of ATEST multiplex selection.

Register Name	**DP16 Configuration 0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_CONFIG0_P2_[n]
Address	800000030701183F (SCOM), +0x0400_0000_0000
Description	This is the DP16 configuration register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	DD2_COARSE_OF_DISABLE: 0 = Enable the DD2 function for reporting of write delay overflow errors in coarse alignment. 1 = Enable the DD1 function.
49	RW	DD2_DBDIS_DQS_DISABLE: 0 = Enable the DD2 function to allow setting DQS disable bits when DQS calibration is detected. 1 = Enable the DD1 function.
50	RW	DD2_SPARE_L2SFF_CG_DISABLE: 0 = Enable the DD2 function of clock gating on spare L2SFF latches. 1 = Enable the DD1 function.
51	RW	FLUSH: Manufacturing macro test control for ANALOG. This bit controls whether the transmit FIFO is flushed or not. When flushed, half-rate data is no longer valid.
52	RW	DQS_FORCE_VALUE: This bit is relevant only when DFT_FORCE_OUTPUTS = 1 in the DP16 DFT/PDA Control Register [n] (n=0:4). 0 = A low voltage is driven on all eight DQS pins. 1 = A high voltage is driven on all eight DQS pins.
53	RW	P8_DD2_FIX_DIS: 0 = Enable POWER8 DD2 function. 1 = Enable POWER8 DD1 function.
54	RW	INIT_IO: Enables the DC level translator in front of the TX output stages, which initialize the top-plate voltage of the fly cap in the AC level translator at start up. This must be applied for a minimum of five clock cycles after startup, and before the I/Os can be used. This requirement also applies to all manufacturing test modes.

Bits	SCOM	Field Mnemonic: Description
55	RW	ADVANCE_PING_PONG: This bit must be set to 1b due to the timing requirements of the analog core. 0 = The DQS (write strobe) phase rotator multiplex select is not advanced. 1 = The DQS (write strobe) phase rotator multiplex select switches one SysClk clock cycle early.
56	RW	WL_ADVANCE_DISABLE: 0 = Enable the 1/2 UI advance of the second-to-last sample in the write-leveling calibration algorithm. 1 = Disable the 1/2 UI advance of the second-to-last sample in the write-leveling calibration algorithm.
57	RW	DISABLE_PING_PONG: Reserved. This bit must always be written to zero. 0 = The DQS (write strobe) write phase rotator values toggle between the two possible phase rotator values when the rank pair written is not the same as the last rank pair that was written. 1 = The DQS (write strobe) write phase rotator values do not toggle. Each DQS (write strobe) output uses the corresponding phase rotator.
58	RW	DELAY_PING_PONG_HALF: This bit must be set to 1b due to the timing requirements of the analog core. 0 = The DQS (write strobe) phase rotator multiplex select is not delayed. 1 = The DQS (write strobe) phase rotator multiplex select is not 1/2 SysClk clock cycle later. When this bit is set to 1b, and the ADVANCE_PING_PONG bit is set to 1b, the phase rotator multiplex select switches 1/2 a SysClk clock cycle early.
59:63	RW	ATESTSEL_0_4: Lowest level of ATEST multiplex selection.

Register Name	DP16 Configuration 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_CONFIG0_P3_[n]
Address	8000000307011C3F (SCOM), +0x0400_0000_0000
Description	This is the DP16 configuration register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	DD2_COARSE_OF_DISABLE: 0 = Enable the DD2 function for reporting of write delay overflow errors in coarse alignment. 1 = Enable the DD1 function.
49	RW	DD2_DBDIS_DQS_DISABLE: 0 = Enable the DD2 function to allow setting DQS disable bits when DQS calibration is detected. 1 = Enable the DD1 function.
50	RW	DD2_SPARE_L2SFF_CG_DISABLE: 0 = Enable the DD2 function of clock gating on spare L2SFF latches. 1 = Enable the DD1 function.
51	RW	FLUSH: Manufacturing macro test control for ANALOG. This bit controls whether the transmit FIFO is flushed or not. When flushed, half-rate data is no longer valid.
52	RW	DQS_FORCE_VALUE: This bit is relevant only when DFT_FORCE_OUTPUTS = 1 in the DP16 DFT/PDA Control Register [n] (n=0:4). 0 = A low voltage is driven on all eight DQS pins. 1 = A high voltage is driven on all eight DQS pins.
53	RW	P8_DD2_FIX_DIS: 0 = Enable POWER8 DD2 function. 1 = Enable POWER8 DD1 function.
54	RW	INIT_IO: Enables the DC level translator in front of the TX output stages, which initialize the top-plate voltage of the fly cap in the AC level translator at start up. This must be applied for a minimum of five clock cycles after startup, and before the I/Os can be used. This requirement also applies to all manufacturing test modes.
55	RW	ADVANCE_PING_PONG: This bit must be set to 1b due to the timing requirements of the analog core. 0 = The DQS (write strobe) phase rotator multiplex select is not advanced. 1 = The DQS (write strobe) phase rotator multiplex select switches one SysClk clock cycle early.

Bits	SCOM	Field Mnemonic: Description
56	RW	WL_ADVANCE_DISABLE: 0 = Enable the 1/2 UI advance of the second-to-last sample in the write-leveling calibration algorithm. 1 = Disable the 1/2 UI advance of the second-to-last sample in the write-leveling calibration algorithm.
57	RW	DISABLE_PING_PONG: Reserved. This bit must always be written to zero. 0 = The DQS (write strobe) write phase rotator values toggle between the two possible phase rotator values when the rank pair written is not the same as the last rank pair that was written. 1 = The DQS (write strobe) write phase rotator values do not toggle. Each DQS (write strobe) output uses the corresponding phase rotator.
58	RW	DELAY_PING_PONG_HALF: This bit must be set to 1b due to the timing requirements of the analog core. 0 = The DQS (write strobe) phase rotator multiplex select is not delayed. 1 = The DQS (write strobe) phase rotator multiplex select is not 1/2 SysClk clock cycle later. When this bit is set to 1b, and the ADVANCE_PING_PONG bit is set to 1b, the phase rotator multiplex select switches 1/2 a SysClk clock cycle early.
59:63	RW	ATESTSEL_0_4: Lowest level of ATEST multiplex selection.

Register Name	DP16 Read Clock Enable and Selection RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_CLOCK_RANK_PAIR0_P0_[n]
Address	800000040701103F (SCOM), +0x0400_0000_0000
Description	This register configures which input pins on the DP16 are used as strobes to capture incoming data on which data pins. This register must be configured the same as the DP16 Write Clock Enable and Selection Register. The following are legal configurations on POWER9 for bits 48:53: 110000 = By-8 memory using CLK16. 000011 = By-8 memory using CLK18. 100001 = By-4 memory, not cross-coupled. 010010 = By-4 memory, cross-coupled. 000000 = Byte is not used. Other values are reserved. The following are legal configurations on POWER9 for bits 54:57: 1100 = By-8 memory using CLK20. 0011 = By-8 memory using CLK22. 1001 = By-4 memory, not cross-coupled. 0110 = By-4 memory, cross-coupled. 0000 = Byte is not used. Other values are reserved.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	QUAD0_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an incoming clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
49	RW	QUAD1_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an incoming clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.

Bits	SCOM	Field Mnemonic: Description
50:51	RO	Reserved.
52	RW	QUAD0_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an incoming clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
53	RW	QUAD1_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an incoming clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
54	RW	QUAD2_CLK20: 1 = MEMINTD20B(n) and MEMINTD21B(n) are used as an incoming clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
55	RW	QUAD3_CLK20: 1 = MEMINTD20B(n) and MEMINTD21B(n) are used as an incoming clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
56	RW	QUAD2_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an incoming clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
57	RW	QUAD3_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an incoming clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
58:63	RO	Reserved.

Register Name	**DP16 Read Clock Enable and Selection RP0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_CLOCK_RANK_PAIR0_P1_[n]
Address	800000040701143F (SCOM), +0x0400_0000_0000
Description	This register configures which input pins on the DP16 are used as strobes to capture incoming data on which data pins. This register must be configured the same as the DP16 Write Clock Enable and Selection Register. The following are legal configurations on POWER9 for bits 48:53: 110000 = By-8 memory using CLK16. 000011 = By-8 memory using CLK18. 100001 = By-4 memory, not cross-coupled. 010010 = By-4 memory, cross-coupled. 000000 = Byte is not used. Other values are reserved. The following are legal configurations on POWER9 for bits 54:57: 1100 = By-8 memory using CLK20. 0011 = By-8 memory using CLK22. 1001 = By-4 memory, not cross-coupled. 0110 = By-4 memory, cross-coupled. 0000 = Byte is not used. Other values are reserved.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	QUAD0_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an incoming clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
49	RW	QUAD1_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an incoming clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
50:51	RO	Reserved.
52	RW	QUAD0_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an incoming clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
53	RW	QUAD1_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an incoming clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.

Bits	SCOM	Field Mnemonic: Description
54	RW	QUAD2_CLK20: 1 = MEMINTD20B(n) and MEMINTD21B(n) are used as an incoming clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
55	RW	QUAD3_CLK20: 1 = MEMINTD20B(n) and MEMINTD21B(n) are used as an incoming clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
56	RW	QUAD2_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an incoming clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
57	RW	QUAD3_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an incoming clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
58:63	RO	Reserved.

Register Name	**DP16 Read Clock Enable and Selection RP0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_CLOCK_RANK_PAIR0_P2_[n]
Address	800000040701183F (SCOM), +0x0400_0000_0000
Description	This register configures which input pins on the DP16 are used as strobes to capture incoming data on which data pins. This register must be configured the same as the DP16 Write Clock Enable and Selection Register. The following are legal configurations on POWER9 for bits 48:53: 110000 = By-8 memory using CLK16. 000011 = By-8 memory using CLK18. 100001 = By-4 memory, not cross-coupled. 010010 = By-4 memory, cross-coupled. 000000 = Byte is not used. Other values are reserved. The following are legal configurations on POWER9 for bits 54:57: 1100 = By-8 memory using CLK20. 0011 = By-8 memory using CLK22. 1001 = By-4 memory, not cross-coupled. 0110 = By-4 memory, cross-coupled. 0000 = Byte is not used. Other values are reserved.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	QUAD0_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an incoming clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
49	RW	QUAD1_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an incoming clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
50:51	RO	Reserved.
52	RW	QUAD0_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an incoming clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
53	RW	QUAD1_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an incoming clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
54	RW	QUAD2_CLK20: 1 = MEMINTD20B(n) and MEMINTD21B(n) are used as an incoming clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
55	RW	QUAD3_CLK20: 1 = MEMINTD20B(n) and MEMINTD21B(n) are used as an incoming clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.

Bits	SCOM	Field Mnemonic: Description
56	RW	QUAD2_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an incoming clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
57	RW	QUAD3_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an incoming clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
58:63	RO	Reserved.

Register Name	**DP16 Read Clock Enable and Selection RP0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_CLOCK_RANK_PAIR0_P3_[n]
Address	8000000407011C3F (SCOM), +0x0400_0000_0000
Description	This register configures which input pins on the DP16 are used as strobes to capture incoming data on which data pins. This register must be configured the same as the DP16 Write Clock Enable and Selection Register. The following are legal configurations on POWER9 for bits 48:53: 110000 = By-8 memory using CLK16. 000011 = By-8 memory using CLK18. 100001 = By-4 memory, not cross-coupled. 010010 = By-4 memory, cross-coupled. 000000 = Byte is not used. Other values are reserved. The following are legal configurations on POWER9 for bits 54:57: 1100 = By-8 memory using CLK20. 0011 = By-8 memory using CLK22. 1001 = By-4 memory, not cross-coupled. 0110 = By-4 memory, cross-coupled. 0000 = Byte is not used. Other values are reserved.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	QUAD0_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an incoming clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.

Bits	SCOM	Field Mnemonic: Description
49	RW	QUAD1_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an incoming clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
50:51	RO	Reserved.
52	RW	QUAD0_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an incoming clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
53	RW	QUAD1_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an incoming clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
54	RW	QUAD2_CLK20: 1 = MEMINTD20B(n) and MEMINTD21B(n) are used as an incoming clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
55	RW	QUAD3_CLK20: 1 = MEMINTD20B(n) and MEMINTD21B(n) are used as an incoming clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
56	RW	QUAD2_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an incoming clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.

Bits	SCOM	Field Mnemonic: Description
57	RW	QUAD3_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an incoming clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
58:63	RO	Reserved.

Register Name	DP16 Write Clock Enable and Selection RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WRCLK_EN_RP0_P0_[n]
Address	800000050701103F (SCOM), +0x0400_0000_0000
Description	This register configures which output pins on the DP16 are used as clocks or strobes to capture outgoing data on which data pins. This register must be configured exactly the same as the DP16 Read Clock Enable and Selection Register. The following are legal configurations for bits 48:53: 110000 = by-8 memory using CLK16 000011 = by-8 memory using CLK18 100001 = by-4 memory, not cross-coupled 010010 = by-4 memory, cross-coupled 000000 = Byte is not used. Other values are reserved. The following are legal configurations for bits 54:57: 1100 = by-8 memory using CLK20 0011 = by-8 memory using CLK22 1001 = by-4 memory, not cross-coupled 0110 = by-4 memory, cross-coupled 0000 = Byte is not used. Other values are reserved. The same configuration should be loaded for all active ranks.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	QUAD0_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
49	RW	QUAD1_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
50:51	RW	Reserved.

Bits	SCOM	Field Mnemonic: Description
52	RW	QUAD0_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
53	RW	QUAD1_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
54	RW	QUAD2_CLK20: 1 = MEMINTD20B(n) and MEMINTD21B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
55	RW	QUAD3_CLK20: 1 = MEMINTD20B(n) and MEMINTD21B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
56	RW	QUAD2_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
57	RW	QUAD3_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
58:63	RW	Reserved.

Register Name	DP16 Write Clock Enable and Selection RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WRCLK_EN_RP0_P1_[n]
Address	800000050701143F (SCOM), +0x0400_0000_0000
Description	This register configures which output pins on the DP16 are used as clocks or strobes to capture outgoing data on which data pins. This register must be configured exactly the same as the DP16 Read Clock Enable and Selection Register. The following are legal configurations for bits 48:53: 110000 = by-8 memory using CLK16 000011 = by-8 memory using CLK18 100001 = by-4 memory, not cross-coupled 010010 = by-4 memory, cross-coupled 000000 = Byte is not used. Other values are reserved. The following are legal configurations for bits 54:57: 1100 = by-8 memory using CLK20 0011 = by-8 memory using CLK22 1001 = by-4 memory, not cross-coupled 0110 = by-4 memory, cross-coupled 0000 = Byte is not used. Other values are reserved. The same configuration should be loaded for all active ranks.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	QUAD0_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an outgoing clock to capture data on the following pins when the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
49	RW	QUAD1_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an outgoing clock to capture data on the following pins when the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
50:51	RW	Reserved.
52	RW	QUAD0_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.

Bits	SCOM	Field Mnemonic: Description
53	RW	QUAD1_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
54	RW	QUAD2_CLK20: 1 = MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
55	RW	QUAD3_CLK20: 1 = MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
56	RW	QUAD2_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
57	RW	QUAD3_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
58:63	RW	Reserved.

Register Name	DP16 Write Clock Enable and Selection RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WRCLK_EN_RP0_P2_[n]
Address	800000050701183F (SCOM), +0x0400_0000_0000
Description	This register configures which output pins on the DP16 are used as clocks or strobes to capture outgoing data on which data pins. This register must be configured exactly the same as the DP16 Read Clock Enable and Selection Register. The following are legal configurations for bits 48:53: 110000 = by-8 memory using CLK16 000011 = by-8 memory using CLK18 100001 = by-4 memory, not cross-coupled 010010 = by-4 memory, cross-coupled 000000 = Byte is not used. Other values are reserved. The following are legal configurations for bits 54:57: 1100 = by-8 memory using CLK20 0011 = by-8 memory using CLK22 1001 = by-4 memory, not cross-coupled 0110 = by-4 memory, cross-coupled 0000 = Byte is not used. Other values are reserved. The same configuration should be loaded for all active ranks.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	QUAD0_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an outgoing clock to capture data on the following pins when the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
49	RW	QUAD1_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an outgoing clock to capture data on the following pins when the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
50:51	RW	Reserved.
52	RW	QUAD0_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.

Bits	SCOM	Field Mnemonic: Description
53	RW	QUAD1_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
54	RW	QUAD2_CLK20: 1 = MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
55	RW	QUAD3_CLK20: 1 = MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
56	RW	QUAD2_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
57	RW	QUAD3_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
58:63	RW	Reserved.

Register Name	DP16 Write Clock Enable and Selection RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WRCLK_EN_RP0_P3_[n]
Address	8000000507011C3F (SCOM), +0x0400_0000_0000
Description	This register configures which output pins on the DP16 are used as clocks or strobes to capture outgoing data on which data pins. This register must be configured exactly the same as the DP16 Read Clock Enable and Selection Register. The following are legal configurations for bits 48:53: 110000 = by-8 memory using CLK16 000011 = by-8 memory using CLK18 100001 = by-4 memory, not cross-coupled 010010 = by-4 memory, cross-coupled 000000 = Byte is not used. Other values are reserved. The following are legal configurations for bits 54:57: 1100 = by-8 memory using CLK20 0011 = by-8 memory using CLK22 1001 = by-4 memory, not cross-coupled 0110 = by-4 memory, cross-coupled 0000 = Byte is not used. Other values are reserved. The same configuration should be loaded for all active ranks.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	QUAD0_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an outgoing clock to capture data on the following pins when the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
49	RW	QUAD1_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an outgoing clock to capture data on the following pins when the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
50:51	RW	Reserved.
52	RW	QUAD0_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.

Bits	SCOM	Field Mnemonic: Description
53	RW	QUAD1_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
54	RW	QUAD2_CLK20: 1 = MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
55	RW	QUAD3_CLK20: 1 = MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
56	RW	QUAD2_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
57	RW	QUAD3_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
58:63	RW	Reserved.

Register Name	DP16 IO RX Configuration 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RX_CONFIG0_P0_[n]
Address	800000060701103F (SCOM), +0x0400_0000_0000
Description	This register contains the receiver configuration for the DP16.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	NIB0TCFLIP_DC: Reverse the polarity of the differential pair on DQS0 (lane 16/17). 0 = Normal wiring of true and complement. 1 = Reverse usage of true and complement.

Bits	SCOM	Field Mnemonic: Description
49	RW	NIB1TCFLIP_DC: Reverse the polarity of the differential pair on DQS1 (lane 18/19). 0 = Normal wiring of true and complement. 1 = Reverse usage of true and complement.
50	RW	NIB2TCFLIP_DC: Reverse the polarity of the differential pair on DQS2 (lane 20/21). 0 = Normal wiring of true and complement. 1 = Reverse usage of true and complement.
51	RW	NIB3TCFLIP_DC: Reverse the polarity of the differential pair on DQS3 (lane 22/23). 0 = Normal wiring of true and complement. 1 = Reverse usage of true and complement.
52	RW	DD2_MCTERM_FIX_DISABLE: 0 = Enable the DD2 function for suppressing an extraneous pulse on MCTERM. 1 = Enable the DD1 function.
53	RW	DD2_COARSE_ALN_FIX_DISABLE: 0 = Enable the DD2 function for coarse alignment not recognizing out-of-range latency adjustments. 1 = Enable the DD1 function.
54	RW	DD2_RESET_READ_FIX_DISABLE: 0 = Enable the DD2 function to remove the register reset on read feature on status registers. 1 = Enable the DD1 function.
55	RW	DD2_RDFIFO_CG_DISABLE: 0 = Enable DD2 enhanced clock gating on read FIFO registers. 1 = Enable the DD1 function.
56	RW	DD2_RDCNTL_CG_DISABLE: 0 = Enable DD2 enhanced clock gating on read control registers. 1 = Enable the DD1 function.
57	RW	DD2_WRCNTL_CG_DISABLE 0 = Enable DD2 enhanced clock gating on write control registers. 1 = Enable the DD1 function.
58	RW	DD2_PARERROR_FIX_DISABLE: 0 = Enable the DD2 fix for parity errors on the VREF Calibration Error Registers. 1 = Enable the DD1 function.
59:60	RW	Reserved.
61	RW	DISABLE_TERMINATION: 0 = The termination resistors for data and strobe pins are turned on during read data transfer. 1 = The termination resistors for data and strobe pins are always off.
62:63	RW	READ_CENTERING_MODE: 00 = Data read from memory is compared to the value of the SEQ Read/Write Data 0 - 1 Registers. The specific bits used by each lane are determined by the DP16 Pattern Position 0 - 2 Registers. This mode is used for custom read centering. 01 = Read back the read FIFO for DDR4 load-reduced dual in-line memory module (LRDIMM) calibration. Do not use for custom calibration. 10 = Reserved. Do not execute custom read centering with this value. 11 = Data read from memory is compared to the value of the SEQ Read/Write Data 0 - 1 Registers. The specific bits used by each lane are determined dynamically based on traffic. This mode is used for DDR4 custom read centering for either the Multipurpose Register (MPR) serial or MPR staggered mode. (MPR parallel mode is supported with a firmware assist, but must not be used for calibration.) These bits are used if custom read centering is enabled. These bits are not used during periodic read centering. The expected read data is always an alternating 01010101 pattern during periodic read centering. The value of the reserved location in DDR4 devices, and the value of the MPR registers in DDR4 memories, is written during initial pattern write. See the CUSTOM_INIT_WRITE field in the WC Configuration 0 Register. For reference, the alternating 01010101 pattern used during initial read centering and periodic read centering is typically read from the MPR0 register of DDR4 devices. The first bit of the expected 01010101 data pattern is controlled by the MPR_PATTERN_BIT of the SEQ Configuration 0 Register.

Register Name	DP16 IO RX Configuration 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RX_CONFIG0_P1_[n]
Address	800000060701143F (SCOM), +0x0400_0000_0000
Description	This register contains the receiver configuration for the DP16.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	NIB0TCFLIP_DC: Reverse the polarity of the differential pair on DQS0 (lane 16/17). 0 = Normal wiring of true and complement. 1 = Reverse usage of true and complement.
49	RW	NIB1TCFLIP_DC: Reverse the polarity of the differential pair on DQS1 (lane 18/19). 0 = Normal wiring of true and complement. 1 = Reverse usage of true and complement.
50	RW	NIB2TCFLIP_DC: Reverse the polarity of the differential pair on DQS2 (lane 20/21). 0 = Normal wiring of true and complement. 1 = Reverse usage of true and complement.
51	RW	NIB3TCFLIP_DC: Reverse the polarity of the differential pair on DQS3 (lane 22/23). 0 = Normal wiring of true and complement. 1 = Reverse usage of true and complement.
52	RW	DD2_MCTERM_FIX_DISABLE: 0 = Enable the DD2 function for suppressing an extraneous pulse on MCTERM. 1 = Enable the DD1 function.
53	RW	DD2_COARSE_ALN_FIX_DISABLE: 0 = Enable the DD2 function for coarse alignment not recognizing out-of-range latency adjustments. 1 = Enable the DD1 function.
54	RW	DD2_RESET_READ_FIX_DISABLE: 0 = Enable the DD2 function to remove the register reset on read feature on status registers. 1 = Enable the DD1 function.
55	RW	DD2_RDFIFO_CG_DISABLE: 0 = Enable DD2 enhanced clock gating on read FIFO registers. 1 = Enable the DD1 function.
56	RW	DD2_RDCNTL_CG_DISABLE: 0 = Enable DD2 enhanced clock gating on read control registers. 1 = Enable the DD1 function.
57	RW	DD2_WRCNTL_CG_DISABLE 0 = Enable DD2 enhanced clock gating on write control registers. 1 = Enable the DD1 function.
58	RW	DD2_PARERROR_FIX_DISABLE: 0 = Enable the DD2 fix for parity errors on the VREF Calibration Error Registers. 1 = Enable the DD1 function.
59:60	RW	Reserved.
61	RW	DISABLE_TERMINATION: 0 = The termination resistors for data and strobe pins are turned on during read data transfer. 1 = The termination resistors for data and strobe pins are always off.

Bits	SCOM	Field Mnemonic: Description
62:63	RW	READ_CENTERING_MODE: 00 = Data read from memory is compared to the value of the SEQ Read/Write Data 0 - 1 Registers. The specific bits used by each lane are determined by the DP16 Pattern Position 0 - 2 Registers. This mode is used for custom read centering. 01 = Read back the read FIFO for DDR4 LRDIMM calibration. Do not use for custom calibration. 10 = Reserved. Do not execute custom read centering with this value. 11 = Data read from memory is compared to the value of the SEQ Read/Write Data 0 - 1 Registers. The specific bits used by each lane are determined dynamically based on traffic. This mode is used for DDR4 custom read centering for either the MPR serial or MPR staggered mode. (MPR parallel mode is supported with a firmware assist, but must not be used for calibration.) These bits are used if custom read centering is enabled. These bits are not used during periodic read centering. The expected read data is always an alternating 01010101 pattern during periodic read centering. The value of the reserved location in DDR4 devices, and the value of the MPR registers in DDR4 memories, is written during initial pattern write. See the CUSTOM_INIT_WRITE field in the WC Configuration 0 Register. For reference, the alternating 01010101 pattern used during initial read centering and periodic read centering is typically read from the MPR0 register of DDR4 devices. The first bit of the expected 01010101 data pattern is controlled by the MPR_PATTERN_BIT of the SEQ Configuration 0 Register.

Register Name	DP16 IO RX Configuration 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RX_CONFIG0_P2_[n]
Address	800000060701183F (SCOM), +0x0400_0000_0000
Description	This register contains the receiver configuration for the DP16.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	NIB0TCFLIP_DC: Reverse the polarity of the differential pair on DQS0 (lane 16/17). 0 = Normal wiring of true and complement. 1 = Reverse usage of true and complement.
49	RW	NIB1TCFLIP_DC: Reverse the polarity of the differential pair on DQS1 (lane 18/19). 0 = Normal wiring of true and complement. 1 = Reverse usage of true and complement.
50	RW	NIB2TCFLIP_DC: Reverse the polarity of the differential pair on DQS2 (lane 20/21). 0 = Normal wiring of true and complement. 1 = Reverse usage of true and complement.
51	RW	NIB3TCFLIP_DC: Reverse the polarity of the differential pair on DQS3 (lane 22/23). 0 = Normal wiring of true and complement. 1 = Reverse usage of true and complement.
52	RW	DD2_MCTERM_FIX_DISABLE: 0 = Enable the DD2 function for suppressing an extraneous pulse on MCTERM. 1 = Enable the DD1 function.
53	RW	DD2_COARSE_ALN_FIX_DISABLE: 0 = Enable the DD2 function for coarse alignment not recognizing out-of-range latency adjustments. 1 = Enable the DD1 function.
54	RW	DD2_RESET_READ_FIX_DISABLE: 0 = Enable the DD2 function to remove the register reset on read feature on status registers. 1 = Enable the DD1 function.
55	RW	DD2_RDFIFO_CG_DISABLE: 0 = Enable DD2 enhanced clock gating on read FIFO registers. 1 = Enable the DD1 function.

Bits	SCOM	Field Mnemonic: Description
56	RW	DD2_RDCNTL_CG_DISABLE: 0 = Enable DD2 enhanced clock gating on read control registers. 1 = Enable the DD1 function.
57	RW	DD2_WRCNTL_CG_DISABLE 0 = Enable DD2 enhanced clock gating on write control registers. 1 = Enable the DD1 function.
58	RW	DD2_PARERROR_FIX_DISABLE: 0 = Enable the DD2 fix for parity errors on the VREF Calibration Error Registers. 1 = Enable the DD1 function.
59:60	RW	Reserved.
61	RW	DISABLE_TERMINATION: 0 = The termination resistors for data and strobe pins are turned on during read data transfer. 1 = The termination resistors for data and strobe pins are always off.
62:63	RW	READ_CENTERING_MODE: 00 = Data read from memory is compared to the value of the SEQ Read/Write Data 0 - 1 Registers. The specific bits used by each lane are determined by the DP16 Pattern Position 0 - 2 Registers. This mode is used for custom read centering. 01 = Read back the read FIFO for DDR4 LRDIMM calibration. Do not use for custom calibration. 10 = Reserved. Do not execute custom read centering with this value. 11 = Data read from memory is compared to the value of the SEQ Read/Write Data 0 - 1 Registers. The specific bits used by each lane are determined dynamically based on traffic. This mode is used for DDR4 custom read centering for either the MPR serial or MPR staggered mode. (MPR parallel mode is supported with a firmware assist, but must not be used for calibration.) These bits are used if custom read centering is enabled. These bits are not used during periodic read centering. The expected read data is always an alternating 01010101 pattern during periodic read centering. The value of the reserved location in DDR4 devices, and the value of the MPR registers in DDR4 memories, is written during initial pattern write. See the CUSTOM_INIT_WRITE field in the WC Configuration 0 Register. For reference, the alternating 01010101 pattern used during initial read centering and periodic read centering is typically read from the MPR0 register of DDR4 devices. The first bit of the expected 01010101 data pattern is controlled by the MPR_PATTERN_BIT of the SEQ Configuration 0 Register.

Register Name	DP16 IO RX Configuration 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RX_CONFIG0_P3_[n]
Address	8000000607011C3F (SCOM), +0x0400_0000_0000
Description	This register contains the receiver configuration for the DP16.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	NIB0TCFLIP_DC: Reverse the polarity of the differential pair on DQS0 (lane 16/17). 0 = Normal wiring of true and complement. 1 = Reverse usage of true and complement.
49	RW	NIB1TCFLIP_DC: Reverse the polarity of the differential pair on DQS1 (lane 18/19). 0 = Normal wiring of true and complement. 1 = Reverse usage of true and complement.
50	RW	NIB2TCFLIP_DC: Reverse the polarity of the differential pair on DQS2 (lane 20/21). 0 = Normal wiring of true and complement. 1 = Reverse usage of true and complement.
51	RW	NIB3TCFLIP_DC: Reverse the polarity of the differential pair on DQS3 (lane 22/23). 0 = Normal wiring of true and complement. 1 = Reverse usage of true and complement.

Bits	SCOM	Field Mnemonic: Description
52	RW	DD2_MCTERM_FIX_DISABLE: 0 = Enable the DD2 function for suppressing an extraneous pulse on MCTERM. 1 = Enable the DD1 function.
53	RW	DD2_COARSE_ALN_FIX_DISABLE: 0 = Enable the DD2 function for coarse alignment not recognizing out-of-range latency adjustments. 1 = Enable the DD1 function.
54	RW	DD2_RESET_READ_FIX_DISABLE: 0 = Enable the DD2 function to remove the register reset on read feature on status registers. 1 = Enable the DD1 function.
55	RW	DD2_RDFIFO_CG_DISABLE: 0 = Enable DD2 enhanced clock gating on read FIFO registers. 1 = Enable the DD1 function.
56	RW	DD2_RDCNTL_CG_DISABLE: 0 = Enable DD2 enhanced clock gating on read control registers. 1 = Enable the DD1 function.
57	RW	DD2_WRCNTL_CG_DISABLE 0 = Enable DD2 enhanced clock gating on write control registers. 1 = Enable the DD1 function.
58	RW	DD2_PARERROR_FIX_DISABLE: 0 = Enable the DD2 fix for parity errors on the VREF Calibration Error Registers. 1 = Enable the DD1 function.
59:60	RW	Reserved.
61	RW	DISABLE_TERMINATION: 0 = The termination resistors for data and strobe pins are turned on during read data transfer. 1 = The termination resistors for data and strobe pins are always off.
62:63	RW	READ_CENTERING_MODE: 00 = Data read from memory is compared to the value of the SEQ Read/Write Data 0 - 1 Registers. The specific bits used by each lane are determined by the DP16 Pattern Position 0 - 2 Registers. This mode is used for custom read centering. 01 = Read back the read FIFO for DDR4 LRDIMM calibration. Do not use for custom calibration. 10 = Reserved. Do not execute custom read centering with this value. 11 = Data read from memory is compared to the value of the SEQ Read/Write Data 0 - 1 Registers. The specific bits used by each lane are determined dynamically based on traffic. This mode is used for DDR4 custom read centering for either the MPR serial or MPR staggered mode. (MPR parallel mode is supported with a firmware assist, but must not be used for calibration.) These bits are used if custom read centering is enabled. These bits are not used during periodic read centering. The expected read data is always an alternating 01010101 pattern during periodic read centering. The value of the reserved location in DDR4 devices, and the value of the MPR registers in DDR4 memories, is written during initial pattern write. See the CUSTOM_INIT_WRITE field in the WC Configuration 0 Register. For reference, the alternating 01010101 pattern used during initial read centering and periodic read centering is typically read from the MPR0 register of DDR4 devices. The first bit of the expected 01010101 data pattern is controlled by the MPR_PATTERN_BIT of the SEQ Configuration 0 Register.

Register Name	**DP16 SysClk 0 Phase Rotator Control Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_SYSCLK_PR0_P0_[n]
Address	800000070701103F (SCOM), +0x0400_0000_0000
Description	This register controls the circuit that aligns the internal SysClk 0 to the incoming dphy_gckn clock clock.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RW	Reserved.
49:55	RW	SYSCLK_ROT_OVERRIDE: System clock (SysClk) phase rotator override value. This field has a dual purpose: override control and lock control. When SYSCLK_ROT_OVERRIDE_EN = 1b, this field is in override control mode. When SYSCLK_ROT_OVERRIDE_EN = 0b, this field is in lock control mode. For override control: The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by four dphy_gckn clock cycles. Back-to-back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field in the DP16 SysClk 1 Phase Rotator Control Register is reserved. For lock control: Write this field to all zeros unless instructed otherwise by your IBM representative. Bit 50: Lock select: Selects between lock status and sticky lock. 0 = Selects the status of the lock. When the dphy_gckn detects that it has reached alignment between the dphy_gckn and SysClk, the BB_LOCK field in the DP16 SysClk 1 Phase Rotator Control Register is asserted. 1 = Selects the sticky lock to the BB_LOCK field in the DP16 SysClk 1 Phase Rotator Control Register. The sticky lock is controlled by bit 52, sticky lock enable. After the sticky lock is set, it remains set. Bit 52: Sticky lock enable. Bits 53:55 000 = At most, a 1-count increment or decrement occurs to indicate a lock. 001 = At most, a 2-count increment or decrement occurs to indicate a lock. 010 = At most, a 3-count increment or decrement occurs to indicate a lock. 011 = At most, a 4-count increment or decrement occurs to indicate a lock. 100 = At most, a 5-count increment or decrement occurs to indicate a lock.
56	RW	SYSCLK_ROT_OVERRIDE_EN: This field enables the use of the SYSCLK_ROT_OVERRIDE field rather than the internally calculated SYSCLK_ROT value when set to 1b. The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by four dphy_gckn clock cycles. Back-to-back APB write operations to this register provide the required separation. When this bit is written to 0b and was 1b, the SYSCLK_ROT value in the DP16 SysClk 1 Phase Rotator Control Register resets to zero.
57	RW	SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_gckn, the SysClk phase alignment controller. Must be asserted after the phase-locked loop (PLL) locks, and must be active for at least five SysClk cycles.
58	RW	SYSCLK_PHASE_CNTL_EN: Alignment enable to dphy_gckn, the SysClk phase alignment controller Must be asserted low at least 25 SysClk cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.
59	RW	SYSCLK_PHASE_DEFAULT_EN: This field enables default startup values to be output by dphy_gckn, the SysClk phase alignment controller. This bit must be asserted during system reset and de-asserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	SYSCLK_POS_EDGE_ALIGN: This field must be 0b for proper functional operation. It is an edge-alignment strap to dphy_gckn, the SysClk phase alignment controller. 0 = Negative edge alignment of the SysClk to the positive edge of dphy_gckn. 1 = Positive edge alignment of the SysClk to the positive edge of dphy_gckn.
61	RW	CONTINUOUS_UPDATE: 0 = The dphy_gckn, the SysClk phase alignment controller, is only updated periodically under hardware control when an update does not interfere with the physical layer (PHY) functional operations. 1 = The dphy_gckn, the SysClk phase alignment controller, runs continuously. Thus, it continuously aligns the dphy_gckn clock to the internal SysClk clock.
62:63	RO	Constant = 0b00

Register Name	DP16 SysClk 0 Phase Rotator Control Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_SYSCLK_PR0_P1_[n]
Address	800000070701143F (SCOM), +0x0400_0000_0000
Description	This register controls the circuit that aligns the internal SysClk 0 to the incoming dphy_gckn clock clock.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	SYSCLK_ROT_OVERRIDE: System clock (SysClk) phase rotator override value. This field has a dual purpose: override control and lock control. When SYSCLK_ROT_OVERRIDE_EN = 1b, this field is in override control mode. When SYSCLK_ROT_OVERRIDE_EN = 0b, this field is in lock control mode. For override control: The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by four dphy_gckn clock cycles. Back-to-back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field in the DP16 SysClk 1 Phase Rotator Control Register is reserved. For lock control: Write this field to all zeros unless instructed otherwise by your IBM representative. Bit 50: Lock select: Selects between lock status and sticky lock. 0 = Selects the status of the lock. When the dphy_gckn detects that it has reached alignment between the dphy_gckn and SysClk, the BB_LOCK field in the DP16 SysClk 1 Phase Rotator Control Register is asserted. 1 = Selects the sticky lock to the BB_LOCK field in the DP16 SysClk 1 Phase Rotator Control Register. The sticky lock is controlled by bit 52, sticky lock enable. After the sticky lock is set, it remains set. Bit 52: Sticky lock enable. Bits 53:55 000 = At most, a 1-count increment or decrement occurs to indicate a lock. 001 = At most, a 2-count increment or decrement occurs to indicate a lock. 010 = At most, a 3-count increment or decrement occurs to indicate a lock. 011 = At most, a 4-count increment or decrement occurs to indicate a lock. 100 = At most, a 5-count increment or decrement occurs to indicate a lock.
56	RW	SYSCLK_ROT_OVERRIDE_EN: This field enables the use of the SYSCLK_ROT_OVERRIDE field rather than the internally calculated SYSCLK_ROT value when set to 1b. The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by four dphy_gckn clock cycles. Back-to-back APB write operations to this register provide the required separation. When this bit is written to 0b and was 1b, the SYSCLK_ROT value in the DP16 SysClk 1 Phase Rotator Control Register resets to zero.
57	RW	SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_gckn, the SysClk phase alignment controller. Must be asserted after the PLL locks, and must be active for at least five SysClk cycles.
58	RW	SYSCLK_PHASE_CNTL_EN: Alignment enable to dphy_gckn, the SysClk phase alignment controller. Must be asserted low at least 25 SysClk cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.
59	RW	SYSCLK_PHASE_DEFAULT_EN: This field enables default startup values to be output by dphy_gckn, the SysClk phase alignment controller. This bit must be asserted during system reset and de-asserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	SYSCLK_POS_EDGE_ALIGN: This field must be 0b for proper functional operation. It is an edge-alignment strap to dphy_gckn, the SysClk phase alignment controller. 0 = Negative edge alignment of the SysClk to the positive edge of dphy_gckn. 1 = Positive edge alignment of the SysClk to the positive edge of dphy_gckn.

Bits	SCOM	Field Mnemonic: Description
61	RW	CONTINUOUS_UPDATE: 0 = The dphy_gckn, the SysClk phase alignment controller, is only updated periodically under hardware control when an update does not interfere with the PHY functional operations. 1 = The dphy_gckn, the SysClk phase alignment controller, runs continuously. Thus, it continuously aligns the dphy_gckn clock to the internal SysClk clock.
62:63	RO	Constant = 0b00

Register Name	DP16 SysClk 0 Phase Rotator Control Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_SYSCLK_PR0_P2_[n]
Address	800000070701183F (SCOM), +0x0400_0000_0000
Description	This register controls the circuit that aligns the internal SysClk 0 to the incoming dphy_gckn clock clock.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	SYSCLK_ROT_OVERRIDE: System clock (SysClk) phase rotator override value. This field has a dual purpose: override control and lock control. When SYSCLK_ROT_OVERRIDE_EN = 1b, this field is in override control mode. When SYSCLK_ROT_OVERRIDE_EN = 0b, this field is in lock control mode. For override control: The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by four dphy_gckn clock cycles. Back-to-back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field in the DP16 SysClk 1 Phase Rotator Control Register is reserved. For lock control: Write this field to all zeros unless instructed otherwise by your IBM representative. Bit 50: Lock select: Selects between lock status and sticky lock. 0 = Selects the status of the lock. When the dphy_gckn detects that it has reached alignment between the dphy_gckn and SysClk, the BB_LOCK field in the DP16 SysClk 1 Phase Rotator Control Register is asserted. 1 = Selects the sticky lock to the BB_LOCK field in the DP16 SysClk 1 Phase Rotator Control Register. The sticky lock is controlled by bit 52, sticky lock enable. After the sticky lock is set, it remains set. Bit 52: Sticky lock enable. Bits 53:55 000 = At most, a 1-count increment or decrement occurs to indicate a lock. 001 = At most, a 2-count increment or decrement occurs to indicate a lock. 010 = At most, a 3-count increment or decrement occurs to indicate a lock. 011 = At most, a 4-count increment or decrement occurs to indicate a lock. 100 = At most, a 5-count increment or decrement occurs to indicate a lock.
56	RW	SYSCLK_ROT_OVERRIDE_EN: This field enables the use of the SYSCLK_ROT_OVERRIDE field, rather than the internally calculated SYSCLK_ROT value, when set to 1b. The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by four dphy_gckn clock cycles. Back-to-back APB write operations to this register provide the required separation. When this bit is written to 0b and was 1b, the SYSCLK_ROT value in the DP16 SysClk 1 Phase Rotator Control Register resets to zero.
57	RW	SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_gckn, the SysClk phase alignment controller. Must be asserted after the PLL locks, and must be active for at least five SysClk cycles.
58	RW	SYSCLK_PHASE_CNTL_EN: Alignment enable to dphy_gckn, the SysClk phase alignment controller. Must be asserted low at least 25 SysClk cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.

Bits	SCOM	Field Mnemonic: Description
59	RW	SYSCLK_PHASE_DEFAULT_EN: This field enables default startup values to be output by dphy_gckn, the SysClk phase alignment controller. This bit must be asserted during system reset and de-asserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	SYSCLK_POS_EDGE_ALIGN: This field must be 0b for proper functional operation. It is an edge-alignment strap to dphy_gckn, the SysClk phase alignment controller. 0 = Negative edge alignment of the SysClk to the positive edge of dphy_gckn. 1 = Positive edge alignment of the SysClk to the positive edge of dphy_gckn.
61	RW	CONTINUOUS_UPDATE: 0 = The dphy_gckn, the SysClk phase alignment controller, is only updated periodically under hardware control when an update does not interfere with the PHY functional operations. 1 = The dphy_gckn, the SysClk phase alignment controller, runs continuously. Thus, it continuously aligns the dphy_gckn clock to the internal SysClk clock.
62:63	RO	Constant = 0b00

Register Name	DP16 SysClk 0 Phase Rotator Control Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_SYSCLK_PR0_P3_[n]
Address	8000000707011C3F (SCOM), +0x0400_0000_0000
Description	This register controls the circuit that aligns the internal SysClk 0 to the incoming dphy_gckn clock clock.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	SYSCLK_ROT_OVERRIDE: System clock (SysClk) phase rotator override value. This field has a dual purpose: override control and lock control. When SYSCLK_ROT_OVERRIDE_EN = 1b, this field is in override control mode. When SYSCLK_ROT_OVERRIDE_EN = 0b, this field is in lock control mode. For override control: The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by four dphy_gckn clock cycles. Back-to-back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field in the DP16 SysClk 1 Phase Rotator Control Register is reserved. For lock control: Write this field to all zeros unless instructed otherwise by your IBM representative. Bit 50: Lock select: Selects between lock status and sticky lock. 0 = Selects the status of the lock. When the dphy_gckn detects that it has reached alignment between the dphy_gckn and SysClk, the BB_LOCK field in the DP16 SysClk 1 Phase Rotator Control Register is asserted. 1 = Selects the sticky lock to the BB_LOCK field in the DP16 SysClk 1 Phase Rotator Control Register. The sticky lock is controlled by bit 52, sticky lock enable. After the sticky lock is set, it remains set. Bit 52: Sticky lock enable. Bits 53:55 000 = At most, a 1-count increment or decrement occurs to indicate a lock. 001 = At most, a 2-count increment or decrement occurs to indicate a lock. 010 = At most, a 3-count increment or decrement occurs to indicate a lock. 011 = At most, a 4-count increment or decrement occurs to indicate a lock. 100 = At most, a 5-count increment or decrement occurs to indicate a lock.

Bits	SCOM	Field Mnemonic: Description
56	RW	SYSCLK_ROT_OVERRIDE_EN: This field enables the use of the SYSCLK_ROT_OVERRIDE field rather than the internally calculated SYSCLK_ROT value when set to 1b. The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by four dphy_gckn clock cycles. Back-to-back APB write operations to this register provide the required separation. When this bit is written to 0b and was 1b, the SYSCLK_ROT value in the DP16 SysClk 1 Phase Rotator Control Register resets to zero.
57	RW	SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_gckn, the SysClk phase alignment controller. Must be asserted after the PLL locks, and must be active for at least five SysClk cycles.
58	RW	SYSCLK_PHASE_CNTL_EN: Alignment enable to dphy_gckn, the SysClk phase alignment controller Must be asserted low at least 25 SysClk cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.
59	RW	SYSCLK_PHASE_DEFAULT_EN: This field enables default startup values to be output by dphy_gckn, the SysClk phase alignment controller. This bit must be asserted during system reset and de-asserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	SYSCLK_POS_EDGE_ALIGN: This field must be 0b for proper functional operation. It is an edge-alignment strap to dphy_gckn, the SysClk phase alignment controller. 0 = Negative edge alignment of the SysClk to the positive edge of dphy_gckn. 1 = Positive edge alignment of the SysClk to the positive edge of dphy_gckn.
61	RW	CONTINUOUS_UPDATE: 0 = The dphy_gckn, the SysClk phase alignment controller, is only updated periodically under hardware control when an update does not interfere with the PHY functional operations. 1 = The dphy_gckn, the SysClk phase alignment controller, runs continuously. Thus, it continuously aligns the dphy_gckn clock to the internal SysClk clock.
62:63	RO	Constant = 0b00

Register Name	DP16 DFT Digital Eye Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DFT_DIG_EYE_P0_[n]
Address	800000080701103F (SCOM), +0x0400_0000_0000
Description	This register controls the digital eye state machine and provides the result of running the digital eye state machine. This register must remain at the reset values for correct mainline function of the DDR PHY. Contact your IBM representative for more information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RWX	DIGITAL_EYE_EN: 0 = Normal operation. 1 = Digital eye function is enabled.
49	RWX	BUMP: When written to 1b, capture the next beat every period (bump to the next bit in the pattern). When read, this bit always returns 0b.
50	RWX	TRIG_PERIOD: 0 = Trigger every 8 beats of data. 1 = Trigger every 128 beats of data.
51	RWX	CNTL_POL: When the eyedac is controlled by hardware, this bit controls the polarity of the feedback to the eyedac. This bit should be left at 0 for normal operation.
52:54	RO	Constant = 0b000

Bits	SCOM	Field Mnemonic: Description
55	RWX	CNTL_SRC: 0 = The control source is from the register. 1 = The control source is a hardware algorithm.
56:63	RO	Constant = 0b00000000

Register Name	DP16 DFT Digital Eye Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DFT_DIG_EYE_P1_[n]
Address	8000000807011 43F (SCOM), +0x0400_0000_0000
Description	This register controls the digital eye state machine and provides the result of running the digital eye state machine. This register must remain at the reset values for correct mainline function of the DDR PHY. Contact your IBM representative for more information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RWX	DIGITAL_EYE_EN: 0 = Normal operation. 1 = Digital eye function is enabled.
49	RWX	BUMP: When written to 1b, capture the next beat every period (bump to the next bit in the pattern). When read, this bit always returns 0b.
50	RWX	TRIG_PERIOD: 0 = Trigger every 8 beats of data. 1 = Trigger every 128 beats of data.
51	RWX	CNTL_POL: When the eyedac is controlled by hardware, this bit controls the polarity of the feedback to the eyedac. This bit should be left at 0 for normal operation.
52:54	RO	Constant = 0b000
55	RWX	CNTL_SRC: 0 = The control source is from the register. 1 = The control source is a hardware algorithm.
56:63	RO	Constant = 0b00000000

Register Name	DP16 DFT Digital Eye Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DFT_DIG_EYE_P2_[n]
Address	8000000807011 83F (SCOM), +0x0400_0000_0000
Description	This register controls the digital eye state machine and provides the result of running the digital eye state machine. This register must remain at the reset values for correct mainline function of the DDR PHY. Contact your IBM representative for more information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RWX	DIGITAL_EYE_EN: 0 = Normal operation. 1 = Digital eye function is enabled.
49	RWX	BUMP: When written to 1b, capture the next beat every period (bump to the next bit in the pattern). When read, this bit always returns 0b.

Bits	SCOM	Field Mnemonic: Description
50	RWX	TRIG_PERIOD: 0 = Trigger every 8 beats of data. 1 = Trigger every 128 beats of data.
51	RWX	CNTL_POL: When the eyedac is controlled by hardware, this bit controls the polarity of the feedback to the eyedac. This bit should be left at 0 for normal operation.
52:54	RO	Constant = 0b000
55	RWX	CNTL_SRC: 0 = The control source is from the register. 1 = The control source is a hardware algorithm.
56:63	RO	Constant = 0b00000000

Register Name	**DP16 DFT Digital Eye Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DFT_DIG_EYE_P3_[n]
Address	8000000807011C3F (SCOM), +0x0400_0000_0000
Description	This register controls the digital eye state machine and provides the result of running the digital eye state machine. This register must remain at the reset values for correct mainline function of the DDR PHY. Contact your IBM representative for more information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RWX	DIGITAL_EYE_EN: 0 = Normal operation. 1 = Digital eye function is enabled.
49	RWX	BUMP: When written to 1b, capture the next beat every period (bump to the next bit in the pattern). When read, this bit always returns 0b.
50	RWX	TRIG_PERIOD: 0 = Trigger every 8 beats of data. 1 = Trigger every 128 beats of data.
51	RWX	CNTL_POL: When the eyedac is controlled by hardware, this bit controls the polarity of the feedback to the eyedac. This bit should be left at 0 for normal operation.
52:54	RO	Constant = 0b000
55	RWX	CNTL_SRC: 0 = The control source is from the register. 1 = The control source is a hardware algorithm.
56:63	RO	Constant = 0b00000000

Register Name	**DP16 DQS Read Phase Select RP0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_[n]
Address	8000000907011O3F (SCOM), +0x0400_0000_0000
Description	This register contains a dynamic value that represents the phase differences between the memory clock, strobes, and the receiver clocks. Hardware determines these values during initial calibration and maintains them during periodic calibrations. One register stores phase selects for each rank pair for a total of four registers. This register is provided for diagnostic use. Do not use software to write to this register during normal use.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:49	RW	DQSCLK_SELECT0: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03.
50:51	RW	RDCLK_SELECT0: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03.
52:53	RW	DQSCLK_SELECT1: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07.
54:55	RW	RDCLK_SELECT1: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07.
56:57	RW	DQSCLK_SELECT2: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11.
58:59	RW	RDCLK_SELECT2: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11.
60:61	RW	DQSCLK_SELECT3: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15.
62:63	RW	RDCLK_SELECT3: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15.

Register Name	**DP16 DQS Read Phase Select RP0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_[n]
Address	800000090701143F (SCOM), +0x0400_0000_0000
Description	This register contains a dynamic value that represents the phase differences between the memory clock, strobes, and the receiver clocks. Hardware determines these values during initial calibration and maintains them during periodic calibrations. One register stores phase selects for each rank pair for a total of four registers. This register is provided for diagnostic use. Do not use software to write to this register during normal use.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:49	RW	DQSCLK_SELECT0: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03.
50:51	RW	RDCLK_SELECT0: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03.
52:53	RW	DQSCLK_SELECT1: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07.
54:55	RW	RDCLK_SELECT1: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07.
56:57	RW	DQSCLK_SELECT2: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11.
58:59	RW	RDCLK_SELECT2: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11.
60:61	RW	DQSCLK_SELECT3: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15.
62:63	RW	RDCLK_SELECT3: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15.

Register Name	DP16 DQS Read Phase Select RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQS_RD_PHASE_SELECT_RANK_PAIR0_P2_[n]
Address	800000090701183F (SCOM), +0x0400_0000_0000
Description	This register contains a dynamic value that represents the phase differences between the memory clock, strobes, and the receiver clocks. Hardware determines these values during initial calibration and maintains them during periodic calibrations. One register stores phase selects for each rank pair for a total of four registers. This register is provided for diagnostic use. Do not use software to write to this register during normal use.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:49	RW	DQSCLK_SELECT0: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03.
50:51	RW	RDCLK_SELECT0: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03.
52:53	RW	DQSCLK_SELECT1: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07.
54:55	RW	RDCLK_SELECT1: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07.
56:57	RW	DQSCLK_SELECT2: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11.
58:59	RW	RDCLK_SELECT2: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11.
60:61	RW	DQSCLK_SELECT3: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15.
62:63	RW	RDCLK_SELECT3: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15.

Register Name	DP16 DQS Read Phase Select RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQS_RD_PHASE_SELECT_RANK_PAIR0_P3_[n]
Address	8000000907011C3F (SCOM), +0x0400_0000_0000
Description	This register contains a dynamic value that represents the phase differences between the memory clock, strobes, and the receiver clocks. Hardware determines these values during initial calibration and maintains them during periodic calibrations. One register stores phase selects for each rank pair for a total of four registers. This register is provided for diagnostic use. Do not use software to write to this register during normal use.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:49	RW	DQSCLK_SELECT0: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03.
50:51	RW	RDCLK_SELECT0: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03.
52:53	RW	DQSCLK_SELECT1: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07.
54:55	RW	RDCLK_SELECT1: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07.

Bits	SCOM	Field Mnemonic: Description
56:57	RW	DQSCLK_SELECT2: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11.
58:59	RW	RDCLK_SELECT2: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11.
60:61	RW	DQSCLK_SELECT3: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15.
62:63	RW	RDCLK_SELECT3: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15.

Register Name	**DP16 Drift Limits Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DRIFT_LIMITS_P0_[n]
Address	8000000A0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the limits for periodic drift of the data eye and the received strobe.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:49	RW	DD2_BLUE_EXTEND_RANGE: 00 = The RDCLK_SELECT range is 0 - 3 (DD1 function). 01 = The RDCLK_SELECT range is 1 - 4. 10 = Invalid. 11 = The RDCLK_SELECT range is 2 – 5. **Note:** RDCLK_SELECTis defined in the DP16 DQS Read Phase Select Register.
50:55	RW	MIN_RD_EYE_SIZE: This is the minimum allowable read eye size for any data bit measured in the same units as RD_EYE_SIZE.
56	RW	DD2_SPARE_L2SFF_CG_DISABLE: 0 = Enable the DD2 function of clock gating on spare L2SFF latches. 1 = Enable the DD1 function.
57	RW	DD2_PERRDCTR_FIX_DISABLE: 0 = Enable the DD2 periodic read centering fix. 1 = Enable the DD1 function.
58:63	RW	MAX_DQS_DRIFT: This is the maximum acceptable drift of any received DQS either earlier or later than the DQS arrival time determined during initial DQS alignment. A value of 0 disables this check.

Register Name	**DP16 Drift Limits Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DRIFT_LIMITS_P1_[n]
Address	8000000A0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the limits for periodic drift of the data eye and the received strobe.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RW	DD2_BLUE_EXTEND_RANGE: 00 = The RDCLK_SELECT range is 0 - 3 (DD1 function). 01 = The RDCLK_SELECT range is 1 - 4. 10 = Invalid. 11 = The RDCLK_SELECT range is 2 – 5. **Note:** RDCLK_SELECTis defined in the DP16 DQS Read Phase Select Register.
50:55	RW	MIN_RD_EYE_SIZE: This is the minimum allowable read eye size for any data bit measured in the same units as RD_EYE_SIZE.
56	RW	DD2_SPARE_L2SFF_CG_DISABLE: 0 = Enable the DD2 function of clock gating on spare L2SFF latches. 1 = Enable the DD1 function.
57	RW	DD2_PERRDCTR_FIX_DISABLE: 0 = Enable the DD2 periodic read centering fix. 1 = Enable the DD1 function.
58:63	RW	MAX_DQS_DRIFT: This is the maximum acceptable drift of any received DQS either earlier or later than the DQS arrival time determined during initial DQS alignment. A value of 0 disables this check.

Register Name	**DP16 Drift Limits Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DRIFT_LIMITS_P2_[n]
Address	8000000A0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the limits for periodic drift of the data eye and the received strobe.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:49	RW	DD2_BLUE_EXTEND_RANGE: 00 = The RDCLK_SELECT range is 0 - 3 (DD1 function). 01 = The RDCLK_SELECT range is 1 - 4. 10 = Invalid. 11 = The RDCLK_SELECT range is 2 – 5. **Note:** RDCLK_SELECTis defined in the DP16 DQS Read Phase Select Register.
50:55	RW	MIN_RD_EYE_SIZE: This is the minimum allowable read eye size for any data bit measured in the same units as RD_EYE_SIZE.
56	RW	DD2_SPARE_L2SFF_CG_DISABLE: 0 = Enable the DD2 function of clock gating on spare L2SFF latches. 1 = Enable the DD1 function.
57	RW	DD2_PERRDCTR_FIX_DISABLE: 0 = Enable the DD2 periodic read centering fix. 1 = Enable the DD1 function.
58:63	RW	MAX_DQS_DRIFT: This is the maximum acceptable drift of any received DQS either earlier or later than the DQS arrival time determined during initial DQS alignment. A value of 0 disables this check.

Register Name	**DP16 Drift Limits Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DRIFT_LIMITS_P3_[n]
Address	8000000A07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the limits for periodic drift of the data eye and the received strobe.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:49	RW	DD2_BLUE_EXTEND_RANGE: 00 = The RDCLK_SELECT range is 0 - 3 (DD1 function). 01 = The RDCLK_SELECT range is 1 - 4. 10 = Invalid. 11 = The RDCLK_SELECT range is 2 – 5. **Note:** RDCLK_SELECTis defined in the DP16 DQS Read Phase Select Register.
50:55	RW	MIN_RD_EYE_SIZE: This is the minimum allowable read eye size for any data bit measured in the same units as RD_EYE_SIZE.
56	RW	DD2_SPARE_L2SFF_CG_DISABLE: 0 = Enable the DD2 function of clock gating on spare L2SFF latches. 1 = Enable the DD1 function.
57	RW	DD2_PERRDCTR_FIX_DISABLE: 0 = Enable the DD2 periodic read centering fix. 1 = Enable the DD1 function.
58:63	RW	MAX_DQS_DRIFT: This is the maximum acceptable drift of any received DQS either earlier or later than the DQS arrival time determined during initial DQS alignment. A value of 0 disables this check.

Register Name	**DP16 Debug Bus Select Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DEBUG_SEL_P0_[n]
Address	8000000B0701103F (SCOM), +0x0400_0000_0000
Description	This register is used for the diagnosis and characterization of the DP16 core. For correct functional mainline operation, this register must not be written. Contact your IBM representative before changing the value of this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:53	RW	HS_PROBE_A_SEL: High-speed probe A select.
54:59	RW	HS_PROBE_B_SEL: High-speed probe B select.
60:63	RW	RD_DEBUG_SEL: Selects signals that drive the 44-bit debug bus output of DP16.

Register Name	**DP16 Debug Bus Select Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DEBUG_SEL_P1_[n]
Address	8000000B0701143F (SCOM), +0x0400_0000_0000
Description	This register is used for the diagnosis and characterization of the DP16 core. For correct functional mainline operation, this register must not be written. Contact your IBM representative before changing the value of this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:53	RW	HS_PROBE_A_SEL: High-speed probe A select.
54:59	RW	HS_PROBE_B_SEL: High-speed probe B select.
60:63	RW	RD_DEBUG_SEL: Selects signals that drive the 44-bit debug bus output of DP16.

Register Name	DP16 Debug Bus Select Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DEBUG_SEL_P2_[n]
Address	8000000B0701183F (SCOM), +0x0400_0000_0000
Description	This register is used for the diagnosis and characterization of the DP16 core. For correct functional mainline operation, this register must not be written. Contact your IBM representative before changing the value of this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:53	RW	HS_PROBE_A_SEL: High-speed probe A select.
54:59	RW	HS_PROBE_B_SEL: High-speed probe B select.
60:63	RW	RD_DEBUG_SEL: Selects signals that drive the 44-bit debug bus output of DP16.

Register Name	DP16 Debug Bus Select Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DEBUG_SEL_P3_[n]
Address	8000000B07011C3F (SCOM), +0x0400_0000_0000
Description	This register is used for the diagnosis and characterization of the DP16 core. For correct functional mainline operation, this register must not be written. Contact your IBM representative before changing the value of this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:53	RW	HS_PROBE_A_SEL: High-speed probe A select.
54:59	RW	HS_PROBE_B_SEL: High-speed probe B select.
60:63	RW	RD_DEBUG_SEL: Selects signals that drive the 44-bit debug bus output of DP16.

Register Name	DP16 Read Delay Offset 0 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY_OFFSET0_RANK_PAIR0_P0_[n]
Address	8000000C0701103F (SCOM), +0x0400_0000_0000
Description	Each register field holds the read delay offsets for four of the MEMINTDnnB pins for one rank pair in the DP16.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000000000000
49:55	RW	OFFSET0: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03 and nn{1} = 08, 09, 10, 11. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.
56	RO	Constant = 0b0

Bits	SCOM	Field Mnemonic: Description
57:63	RW	OFFSET1: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07 and nn{1} = 12, 13, 14, 15. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.

Register Name	**DP16 Read Delay Offset 0 RP0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY_OFFSET0_RANK_PAIR0_P1_[n]
Address	8000000C0701143F (SCOM), +0x0400_0000_0000
Description	Each register field holds the read delay offsets for four of the MEMINTDnnB pins for one rank pair in the DP16.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	OFFSET0: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03 and nn{1} = 08, 09, 10, 11. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.
56	RO	Constant = 0b0
57:63	RW	OFFSET1: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07 and nn{1} = 12, 13, 14, 15. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.

Register Name	**DP16 Read Delay Offset 0 RP0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY_OFFSET0_RANK_PAIR0_P2_[n]
Address	8000000C0701183F (SCOM), +0x0400_0000_0000
Description	Each register field holds the read delay offsets for four of the MEMINTDnnB pins for one rank pair in the DP16.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	OFFSET0: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03 and nn{1} = 08, 09, 10, 11. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.
56	RO	Constant = 0b0

Bits	SCOM	Field Mnemonic: Description
57:63	RW	OFFSET1: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07 and nn{1} = 12, 13, 14, 15. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.

Register Name	**DP16 Read Delay Offset 0 RP0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY_OFFSET0_RANK_PAIR0_P3_[n]
Address	8000000C07011C3F (SCOM), +0x0400_0000_0000
Description	Each register field holds the read delay offsets for four of the MEMINTDnnB pins for one rank pair in the DP16.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	OFFSET0: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03 and nn{1} = 08, 09, 10, 11. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.
56	RO	Constant = 0b0
57:63	RW	OFFSET1: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07 and nn{1} = 12, 13, 14, 15. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.

Register Name	**DP16 Read Delay Offset 1 RP0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY_OFFSET1_RANK_PAIR0_P0_[n]
Address	8000000D0701103F (SCOM), +0x0400_0000_0000
Description	Each register field holds the read delay offsets for four of the MEMINTDnnB pins for one rank pair in the DP16.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	OFFSET2: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03 and nn{1} = 08, 09, 10, 11. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.
56	RO	Constant = 0b0

Bits	SCOM	Field Mnemonic: Description
57:63	RW	OFFSET3: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07 and nn{1} = 12, 13, 14, 15. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.

Register Name	**DP16 Read Delay Offset 1 RP0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY_OFFSET1_RANK_PAIR0_P1_[n]
Address	8000000D0701143F (SCOM), +0x0400_0000_0000
Description	Each register field holds the read delay offsets for four of the MEMINTDnnB pins for one rank pair in the DP16.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	OFFSET2: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03 and nn{1} = 08, 09, 10, 11. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.
56	RO	Constant = 0b0
57:63	RW	OFFSET3: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07 and nn{1} = 12, 13, 14, 15. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.

Register Name	**DP16 Read Delay Offset 1 RP0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY_OFFSET1_RANK_PAIR0_P2_[n]
Address	8000000D0701183F (SCOM), +0x0400_0000_0000
Description	Each register field holds the read delay offsets for four of the MEMINTDnnB pins for one rank pair in the DP16.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	OFFSET2: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03 and nn{1} = 08, 09, 10, 11. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.
56	RO	Constant = 0b0

Bits	SCOM	Field Mnemonic: Description
57:63	RW	OFFSET3: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07 and nn{1} = 12, 13, 14, 15. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.

Register Name	DP16 Read Delay Offset 1 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY_OFFSET1_RANK_PAIR0_P3_[n]
Address	8000000D07011C3F (SCOM), +0x0400_0000_0000
Description	Each register field holds the read delay offsets for four of the MEMINTDnnB pins for one rank pair in the DP16.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	OFFSET2: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03 and nn{1} = 08, 09, 10, 11. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.
56	RO	Constant = 0b0
57:63	RW	OFFSET3: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07 and nn{1} = 12, 13, 14, 15. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.

Register Name	DP16 Read Centering Status 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_LVL_STATUS0_P0_[n]
Address	8000000E0701103F (SCOM), +0x0400_0000_0000
Description	This register contains status information about read calibrations.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RO	LEADING_EDGE_NOT_FOUND_0_15: The leading-edge (left side) transition of the data eye was not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	DP16 Read Centering Status 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_LVL_STATUS0_P1_[n]
Address	8000000E0701143F (SCOM), +0x0400_0000_0000
Description	This register contains status information about read calibrations.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RO	LEADING_EDGE_NOT_FOUND_0_15: The leading-edge (left side) transition of the data eye was not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	DP16 Read Centering Status 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_LVL_STATUS0_P2_[n]
Address	8000000E0701183F (SCOM), +0x0400_0000_0000
Description	This register contains status information about read calibrations.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RO	LEADING_EDGE_NOT_FOUND_0_15: The leading-edge (left side) transition of the data eye was not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	DP16 Read Centering Status 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_LVL_STATUS0_P3_[n]
Address	8000000E07011C3F (SCOM), +0x0400_0000_0000
Description	This register contains status information about read calibrations.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RO	LEADING_EDGE_NOT_FOUND_0_15: The leading-edge (left side) transition of the data eye was not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	DP16 Read Centering Status 2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_LVL_STATUS2_P0_[n]
Address	800000100701103F (SCOM), +0x0400_0000_0000
Description	This register contains status information about read calibrations.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RO	TRAILING_EDGE_NOT_FOUND_0_15: The trailing-edge (right side) transition of the data eye was not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	DP16 Read Centering Status 2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_LVL_STATUS2_P1_[n]
Address	800000100701143F (SCOM), +0x0400_0000_0000
Description	This register contains status information about read calibrations.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RO	TRAILING_EDGE_NOT_FOUND_0_15: The trailing-edge (right side) transition of the data eye was not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	DP16 Read Centering Status 2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_LVL_STATUS2_P2_[n]
Address	800000100701183F (SCOM), +0x0400_0000_0000
Description	This register contains status information about read calibrations.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RO	TRAILING_EDGE_NOT_FOUND_0_15: The trailing-edge (right side) transition of the data eye was not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	DP16 Read Centering Status 2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_LVL_STATUS2_P3_[n]
Address	8000001007011C3F (SCOM), +0x0400_0000_0000
Description	This register contains status information about read calibrations.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RO	TRAILING_EDGE_NOT_FOUND_0_15: The trailing-edge (right side) transition of the data eye was not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	DP16 Read Diagnostic Configuration 5 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_DIA_CONFIG5_P0_[n]
Address	800000120701103F (SCOM), +0x0400_0000_0000
Description	This register is used for the diagnosis and characterization of the read function within the DP16. For correct functional mainline operation, this register must not be written. Contact your IBM representative before changing the value of this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	DYN_POWER_CNTL_EN: Dynamic power control enable: 0 = Normal operation with mode disabled. Seven delay stages are powered on per quad. 1 = Mode enabled. The number of delay stages powered on is based on the read delay values determined by initial read centering. If this mode is enabled, initial read centering must be run on rank group 0 and all other rank groups that are populated.
49	RW	DYN_MCTERM_CNTL_EN: Dynamic termination control enable. This bit must be set to 1 for normal operation.
50	RW	DYN_RX_GATE_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
51	RW	CALGATE_ON: Reserved. This bit must be set to 0 for normal operation.

Bits	SCOM	Field Mnemonic: Description
52	RW	PER_CAL_UPDATE_DISABLE: Reserved. This bit must be set to 0 for normal operation.
53:54	RW	DQS_PIPE_FIX_DIS: Reserved. These bits must be set to 00 for normal operation.
55	RW	CDD2_DQS_FIX_DIS: Reserved. This bit must be set to 0 for normal operation.
56	RW	DL_FORCE_ON: Reserved. This bit must be set to 0 for normal operation.
57	RW	BLFIFO_DIS: Reserved. This bit must be set to 0 for normal operation.
58	RW	WTRFL_AVE_DIS: Reserved. This bit must be set to 0 for normal operation.
59	RW	PERCAL_PWR_DIS: 0 = Run DQS alignment when doing periodic calibration for each bit. 1 = Run DQS alignment when doing periodic calibration for bit 0 only.
60	RW	LOOPBACK_FIX_EN: Set this bit to 1 for improved loopback reliability.
61	RW	LOOPBACK_DLY12: If LOOPBACK_FIX_EN = 1, this bit controls the loopback start delay.
62	RW	CDD2_WTRFL_SYNC_DIS: Reserved. This bit must be set to 0 for normal operation.
63	RW	FORCE_FIFO_CAPTURE: 0 = Normal operation. 1 = Force DQ capture in the read FIFO to support DDR4 LRDIMM calibration.

Register Name	**DP16 Read Diagnostic Configuration 5 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_RD_DIA_CONFIG5_P1_[n]
Address	800000120701143F (SCOM), +0x0400_0000_0000
Description	This register is used for the diagnosis and characterization of the read function within the DP16. For correct functional mainline operation, this register must not be written. Contact your IBM representative before changing the value of this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	DYN_POWER_CNTL_EN: Dynamic power control enable: 0 = Normal operation with mode disabled. Seven delay stages are powered on per quad. 1 = Mode enabled. The number of delay stages powered on is based on the read delay values determined by initial read centering. If this mode is enabled, initial read centering must be run on rank group 0 and all other rank groups that are populated.
49	RW	DYN_MCTERM_CNTL_EN: Dynamic termination control enable. This bit must be set to 1 for normal operation.
50	RW	DYN_RX_GATE_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
51	RW	CALGATE_ON: Reserved. This bit must be set to 0 for normal operation.
52	RW	PER_CAL_UPDATE_DISABLE: Reserved. This bit must be set to 0 for normal operation.
53:54	RW	DQS_PIPE_FIX_DIS: Reserved. These bits must be set to 00 for normal operation.
55	RW	CDD2_DQS_FIX_DIS: Reserved. This bit must be set to 0 for normal operation.
56	RW	DL_FORCE_ON: Reserved. This bit must be set to 0 for normal operation.
57	RW	BLFIFO_DIS: Reserved. This bit must be set to 0 for normal operation.
58	RW	WTRFL_AVE_DIS: Reserved. This bit must be set to 0 for normal operation.
59	RW	PERCAL_PWR_DIS: 0 = Run DQS alignment when doing periodic calibration for each bit. 1 = Run DQS alignment when doing periodic calibration for bit 0 only.

Bits	SCOM	Field Mnemonic: Description
60	RW	LOOPBACK_FIX_EN: Set this bit to 1 for improved loopback reliability.
61	RW	LOOPBACK_DLY12: If LOOPBACK_FIX_EN = 1, this bit controls the loopback start delay.
62	RW	CDD2_WTRFL_SYNC_DIS: Reserved. This bit must be set to 0 for normal operation.
63	RW	FORCE_FIFO_CAPTURE: 0 = Normal operation. 1 = Force DQ capture in the read FIFO to support DDR4 LRDIMM calibration.

Register Name	**DP16 Read Diagnostic Configuration 5 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_RD_DIA_CONFIG5_P2_[n]
Address	800000120701183F (SCOM), +0x0400_0000_0000
Description	This register is used for the diagnosis and characterization of the read function within the DP16. For correct functional mainline operation, this register must not be written. Contact your IBM representative before changing the value of this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48	RW	DYN_POWER_CNTL_EN: Dynamic power control enable: 0 = Normal operation with mode disabled. Seven delay stages are powered on per quad. 1 = Mode enabled. The number of delay stages powered on is based on the read delay values determined by initial read centering. If this mode is enabled, initial read centering must be run on rank group 0 and all other rank groups that are populated.
49	RW	DYN_MCTERM_CNTL_EN: Dynamic termination control enable. This bit must be set to 1 for normal operation.
50	RW	DYN_RX_GATE_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
51	RW	CALGATE_ON: Reserved. This bit must be set to 0 for normal operation.
52	RW	PER_CAL_UPDATE_DISABLE: Reserved. This bit must be set to 0 for normal operation.
53:54	RW	DQS_PIPE_FIX_DIS: Reserved. These bits must be set to 00 for normal operation.
55	RW	CDD2_DQS_FIX_DIS: Reserved. This bit must be set to 0 for normal operation.
56	RW	DL_FORCE_ON: Reserved. This bit must be set to 0 for normal operation.
57	RW	BLFIFO_DIS: Reserved. This bit must be set to 0 for normal operation.
58	RW	WTRFL_AVE_DIS: Reserved. This bit must be set to 0 for normal operation.
59	RW	PERCAL_PWR_DIS: 0 = Run DQS alignment when doing periodic calibration for each bit. 1 = Run DQS alignment when doing periodic calibration for bit 0 only.
60	RW	LOOPBACK_FIX_EN: Set this bit to 1 for improved loopback reliability.
61	RW	LOOPBACK_DLY12: If LOOPBACK_FIX_EN = 1, this bit controls the loopback start delay.
62	RW	CDD2_WTRFL_SYNC_DIS: Reserved. This bit must be set to 0 for normal operation.
63	RW	FORCE_FIFO_CAPTURE: 0 = Normal operation. 1 = Force DQ capture in the read FIFO to support DDR4 LRDIMM calibration.

Register Name	DP16 Read Diagnostic Configuration 5 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_DIA_CONFIG5_P3_[n]
Address	8000001207011C3F (SCOM), +0x0400_0000_0000
Description	This register is used for the diagnosis and characterization of the read function within the DP16. For correct functional mainline operation, this register must not be written. Contact your IBM representative before changing the value of this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	DYN_POWER_CNTL_EN: Dynamic power control enable: 0 = Normal operation with mode disabled. Seven delay stages are powered on per quad. 1 = Mode enabled. The number of delay stages powered on is based on the read delay values determined by initial read centering. If this mode is enabled, initial read centering must be run on rank group 0 and all other rank groups that are populated.
49	RW	DYN_MCTERM_CNTL_EN: Dynamic termination control enable. This bit must be set to 1 for normal operation.
50	RW	DYN_RX_GATE_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
51	RW	CALGATE_ON: Reserved. This bit must be set to 0 for normal operation.
52	RW	PER_CAL_UPDATE_DISABLE: Reserved. This bit must be set to 0 for normal operation.
53:54	RW	DQS_PIPE_FIX_DIS: Reserved. These bits must be set to 00 for normal operation.
55	RW	CDD2_DQS_FIX_DIS: Reserved. This bit must be set to 0 for normal operation.
56	RW	DL_FORCE_ON: Reserved. This bit must be set to 0 for normal operation.
57	RW	BLFIFO_DIS: Reserved. This bit must be set to 0 for normal operation.
58	RW	WTRFL_AVE_DIS: Reserved. This bit must be set to 0 for normal operation.
59	RW	PERCAL_PWR_DIS: 0 = Run DQS alignment when doing periodic calibration for each bit. 1 = Run DQS alignment when doing periodic calibration for bit 0 only.
60	RW	LOOPBACK_FIX_EN: Set this bit to 1 for improved loopback reliability.
61	RW	LOOPBACK_DLY12: If LOOPBACK_FIX_EN = 1, this bit controls the loopback start delay.
62	RW	CDD2_WTRFL_SYNC_DIS: Reserved. This bit must be set to 0 for normal operation.
63	RW	FORCE_FIFO_CAPTURE: 0 = Normal operation. 1 = Force DQ capture in the read FIFO to support DDR4 LRDIMM calibration.

Register Name	DP16 DQS Gate Delay RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQS_GATE_DELAY_RP0_P0_[n]
Address	800000130701103F (SCOM), +0x0400_0000_0000
Description	This register contains the DQS gate delay settings for each incoming read clock. One register exists for each rank pair. This register must be reset or written to its reset value before running or rerunning initial calibration.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b0000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:51	RW	DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00 - DQ03 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
52	RO	Constant = 0b0
53:55	RW	DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04 - DQ07 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
56	RO	Constant = 0b0
57:59	RW	DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08 - DQ11 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
60	RO	Constant = 0b0
61:63	RW	DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12 - DQ15 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.

Register Name	**DP16 DQS Gate Delay RP0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQS_GATE_DELAY_RP0_P1_[n]
Address	800000130701143F (SCOM), +0x0400_0000_0000
Description	This register contains the DQS gate delay settings for each incoming read clock. One register exists for each rank pair. This register must be reset or written to its reset value before running or rerunning initial calibration.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:51	RW	DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00 - DQ03 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
52	RO	Constant = 0b0
53:55	RW	DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04 - DQ07 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
56	RO	Constant = 0b0
57:59	RW	DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08 - DQ11 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.

Bits	SCOM	Field Mnemonic: Description
60	RO	Constant = 0b0
61:63	RW	DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12 - DQ15 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.

Register Name	**DP16 DQS Gate Delay RP0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQS_GATE_DELAY_RP0_P2_[n]
Address	800000130701183F (SCOM), +0x0400_0000_0000
Description	This register contains the DQS gate delay settings for each incoming read clock. One register exists for each rank pair. This register must be reset or written to its reset value before running or rerunning initial calibration.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:51	RW	DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00 - DQ03 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
52	RO	Constant = 0b0
53:55	RW	DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04 - DQ07 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
56	RO	Constant = 0b0
57:59	RW	DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08 - DQ11 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
60	RO	Constant = 0b0
61:63	RW	DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12 - DQ15 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.

Register Name	**DP16 DQS Gate Delay RP0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQS_GATE_DELAY_RP0_P3_[n]
Address	8000001307011C3F (SCOM), +0x0400_0000_0000
Description	This register contains the DQS gate delay settings for each incoming read clock. One register exists for each rank pair. This register must be reset or written to its reset value before running or rerunning initial calibration.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:51	RW	DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00 - DQ03 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
52	RO	Constant = 0b0
53:55	RW	DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04 - DQ07 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
56	RO	Constant = 0b0
57:59	RW	DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08 - DQ11 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
60	RO	Constant = 0b0
61:63	RW	DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12 - DQ15 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.

Register Name	**DP16 Read Status 0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_RD_STATUS0_P0_[n]
Address	800000140701103F (SCOM), +0x0400_0000_0000
Description	This register contains status information about read calibrations. The bits in this register can only be set by hardware when the corresponding mask bit is not set in the DP16 Read Error Mask 0 Register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RWX	NO_EYE_DETECTED: Read centering error. No eye was detected on at least one of the data pins by one of the DP16 logic blocks.
49	RWX	LEADING_EDGE_NOT_FOUND: Read centering error. This bit is set when at least one of the leading edges of the data eyes of the data bits are not found during a calibration.
50	RWX	TRAILING_EDGE_NOT_FOUND: Read centering error. This bit is set when at least one of the trailing edges of the data eyes of the data bits are not found during a calibration.
51	RWX	INCOMPLETE_RD_CAL_N0: Read centering/DQS alignment/coarse read alignment error. This bit is set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD00B - MEMINTD03B.
52	RWX	INCOMPLETE_RD_CAL_N1: Read centering/DQS alignment/coarse read alignment error. This bit is set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD04B - MEMINTD07B.
53	RWX	INCOMPLETE_RD_CAL_N2: Read centering/DQS alignment/coarse read alignment error. This bit is set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a a read calibration operation on pins MEMINTD08B - MEMINTD11B.

Bits	SCOM	Field Mnemonic: Description
54	RWX	INCOMPLETE_RD_CAL_N3: Read centering/DQS alignment/coarse read alignment error. This bit is set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD12B - MEMINTD15B.
55	RWX	COARSE_PATTERN_ERR_N0: Coarse read alignment error. This bit is set when the coarse read alignment algorithm does not receive a valid pattern fragment on pins MEMINTD00B - MEMINTD03B.
56	RWX	COARSE_PATTERN_ERR_N1: Coarse read alignment error. This bit is set when the coarse read alignment algorithm does not receive a valid pattern fragment on pins MEMINTD04B - MEMINTD07B.
57	RWX	COARSE_PATTERN_ERR_N2: Coarse read alignment error. This bit is set when the coarse read alignment algorithm does not receive a valid pattern fragment on pins MEMINTD08B - MEMINTD11B.
58	RWX	COARSE_PATTERN_ERR_N3: Coarse read alignment error. This bit is set when the coarse read alignment algorithm does not receive a valid pattern fragment on pins MEMINTD12B - MEMINTD15B.
59	RWX	EYE_CLIPPING: Read centering error/status. This bit activates whenever the eye center is out of the range of the strobe delay line. This is an expected condition for negative values of Trdqsdq (DQ arrives before DQS). The DDR PHY is usually capable of compensating for this. In a typical configuration, the EYE_CLIPPLING_MASK bit must be set to 1b so that this condition is not reported as an error. When EYE_CLIPPING_MASK is 1b, the read centering algorithm continues calibration by using an adjacent DQS edge to perform centering. This configures normal operation of the DDR PHY in most cases, with the margin for inter-symbol interference, and random noise is reduced. The extent of margin reduction is dependent on jitter and the duty cycle distortion (DCD) characteristics of the DRAM.
60	RWX	NO_DQS: DQS alignment error/status. This bit is set when a strobe edge was not detected during DQS alignment calibration. If a strobe is stuck or broken, its location cannot be determined. Thus, it is not possible to guarantee that rank-to-rank switching delays differ by no more than 1/2 UI. Therefore, an extra cycle of gap on rank-to-rank switching must be maintained. You can use the firmware to recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings that are associated with stuck or broken strobes to maintain the 1/2 UI rank-to-rank compression rule.
61	RWX	NO_LOCK: DQS alignment error and status. This bit is set when a phase rotator lock could not be attained on a strobe during DQS alignment calibration. The No Lock error detect circuit detects a DQS strobe that is always 1b or always 0b. When a DQS strobe is always 1b or 0b, it is considered missing or stuck. The No Lock circuit sets this bit when: It does not have a valid strobe for more than 30 samples (that is, 30 samples x 27 tCK per sample = 810 tCK) and The strobe then goes missing or stuck for at least 13 samples (that is, 13 samples x 27 tCK per sample = 351 tCK). If a strobe is stuck or broken, its location cannot be determined. Thus, it is not possible to guarantee that rank-to-rank switching delays differ by no more than 1/2 UI. Therefore, an extra cycle of gap on rank-to-rank switching must be maintained. Firmware can optionally recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings associated with stuck/broken strobes in a way that maintains the 1/2 UI rank-to-rank compression rule.
62	RWX	DRIFT_ERROR: Periodic read calibration error/status: This bit is set when a DQS signal has drifted further than the limit set in the MAX_DQS_DRIFT field of the DP16 Drift Limits Register. The drift limit can be configured very tightly, in which case the activation of this bit is typically informational. Alternatively, it can be configured to a larger value that might indicate rank-to-rank switching is unreliable. Even in such a case, it can be ignored if the application uses a parity of error correction code (ECC) as the final arbiter.

Bits	SCOM	Field Mnemonic: Description
63	RWX	MIN_EYE: Periodic read calibration error/status: This bit is set when a data eye has closed to a value less than the value set in the MIN_RD_EYE_SIZE field of the DP16 Drift Limits Register. The minimum eye size can be configured to a value that is informational, or it can be configured to a limit that reflects a customer's maximum tolerance for errors. In that case, it can be considered to be an error.

Register Name	**DP16 Read Status 0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_RD_STATUS0_P1_[n]
Address	800000140701143F (SCOM), +0x0400_0000_0000
Description	This register contains status information about read calibrations. The bits in this register can only be set by hardware when the corresponding mask bit is not set in the DP16 Read Error Mask 0 Register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RWX	NO_EYE_DETECTED: Read centering error. No eye was detected on at least one of the data pins by one of the DP16 logic blocks.
49	RWX	LEADING_EDGE_NOT_FOUND: Read centering error. This bit is set when at least one of the leading edges of the data eyes of the data bits are not found during a calibration.
50	RWX	TRAILING_EDGE_NOT_FOUND: Read centering error. This bit is set when at least one of the trailing edges of the data eyes of the data bits are not found during a calibration.
51	RWX	INCOMPLETE_RD_CAL_N0: Read centering/DQS alignment/coarse read alignment error. This bit is set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD00B - MEMINTD03B.
52	RWX	INCOMPLETE_RD_CAL_N1: Read centering/DQS alignment/coarse read alignment error. This bit is set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD04B - MEMINTD07B.
53	RWX	INCOMPLETE_RD_CAL_N2: Read centering/DQS alignment/coarse read alignment error. This bit is set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a a read calibration operation on pins MEMINTD08B - MEMINTD11B.
54	RWX	INCOMPLETE_RD_CAL_N3: Read centering/DQS alignment/coarse read alignment error. This bit is set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD12B - MEMINTD15B.
55	RWX	COARSE_PATTERN_ERR_N0: Coarse read alignment error. This bit is set when the coarse read alignment algorithm does not receive a valid pattern fragment on pins MEMINTD00B - MEMINTD03B.
56	RWX	COARSE_PATTERN_ERR_N1: Coarse read alignment error. This bit is set when the coarse read alignment algorithm does not receive a valid pattern fragment on pins MEMINTD04B - MEMINTD07B.
57	RWX	COARSE_PATTERN_ERR_N2: Coarse read alignment error. This bit is set when the coarse read alignment algorithm does not receive a valid pattern fragment on pins MEMINTD08B - MEMINTD11B.
58	RWX	COARSE_PATTERN_ERR_N3: Coarse read alignment error. This bit is set when the coarse read alignment algorithm does not receive a valid pattern fragment on pins MEMINTD12B - MEMINTD15B.

Bits	SCOM	Field Mnemonic: Description
59	RWX	EYE_CLIPPING: Read centering error/status. This bit activates whenever the eye center is out of the range of the strobe delay line. This is an expected condition for negative values of Trdqsdq (DQ arrives before DQS). The DDR PHY is usually capable of compensating for this. In a typical configuration, the EYE_CLIPPLING_MASK bit must be set to 1b so that this condition is not reported as an error. When EYE_CLIPPING_MASK is 1b, the read centering algorithm continues calibration by using an adjacent DQS edge to perform centering. This configures normal operation of the DDR PHY in most cases, with the margin for inter-symbol interference, and random noise is reduced. The extent of margin reduction is dependent on jitter and the DCD characteristics of the DRAM.
60	RWX	NO_DQS: DQS alignment error/status. This bit is set when a strobe edge was not detected during DQS alignment calibration. If a strobe is stuck or broken, its location cannot be determined. Thus, it is not possible to guarantee that rank-to-rank switching delays differ by no more than 1/2 UI. Therefore, an extra cycle of gap on rank-to-rank switching must be maintained. You can use the firmware to recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings that are associated with stuck or broken strobes to maintain the 1/2 UI rank-to-rank compression rule.
61	RWX	NO_LOCK: DQS alignment error and status. This bit is set when a phase rotator lock could not be attained on a strobe during DQS alignment calibration. The No Lock error detect circuit detects a DQS strobe that is always 1b or always 0b. When a DQS strobe is always 1b or 0b, it is considered missing or stuck. The No Lock circuit sets this bit when: It does not have a valid strobe for more than 30 samples (that is, 30 samples x 27 tCK per sample = 810 tCK) and The strobe then goes missing or stuck for at least 13 samples (that is, 13 samples x 27 tCK per sample = 351 tCK). If a strobe is stuck or broken, its location cannot be determined. Thus, it is not possible to guarantee that rank-to-rank switching delays differ by no more than 1/2 UI. Therefore, an extra cycle of gap on rank-to-rank switching must be maintained. Firmware can optionally recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings associated with stuck/broken strobes in a way that maintains the 1/2 UI rank-to-rank compression rule.
62	RWX	DRIFT_ERROR: Periodic read calibration error/status: This bit is set when a DQS signal has drifted further than the limit set in the MAX_DQS_DRIFT field of the DP16 Drift Limits Register. The drift limit can be configured very tightly, in which case the activation of this bit is typically informational. Alternatively, it can be configured to a larger value that might indicate rank-to-rank switching is unreliable. Even in such a case, it can be ignored if the application uses a parity of ECC code as the final arbiter.
63	RWX	MIN_EYE: Periodic read calibration error/status: This bit is set when a data eye has closed to a value less than the value set in the MIN_RD_EYE_SIZE field of the DP16 Drift Limits Register. The minimum eye size can be configured to a value that is informational, or it can be configured to a limit that reflects a customer's maximum tolerance for errors. In that case, it can be considered to be an error.

Register Name	**DP16 Read Status 0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_RD_STATUS0_P2_[n]
Address	800000140701183F (SCOM), +0x0400_0000_0000
Description	This register contains status information about read calibrations. The bits in this register can only be set by hardware when the corresponding mask bit is not set in the DP16 Read Error Mask 0 Register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RWX	NO_EYE_DETECTED: Read centering error. No eye was detected on at least one of the data pins by one of the DP16 logic blocks.

Bits	SCOM	Field Mnemonic: Description
49	RWX	LEADING_EDGE_NOT_FOUND: Read centering error. This bit is set when at least one of the leading edges of the data eyes of the data bits are not found during a calibration.
50	RWX	TRAILING_EDGE_NOT_FOUND: Read centering error. This bit is set when at least one of the trailing edges of the data eyes of the data bits are not found during a calibration.
51	RWX	INCOMPLETE_RD_CAL_N0: Read centering/DQS alignment/coarse read alignment error. This bit is set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD00B - MEMINTD03B.
52	RWX	INCOMPLETE_RD_CAL_N1: Read centering/DQS alignment/coarse read alignment error. This bit is set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD04B - MEMINTD07B.
53	RWX	INCOMPLETE_RD_CAL_N2: Read centering/DQS alignment/coarse read alignment error. This bit is set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a a read calibration operation on pins MEMINTD08B - MEMINTD11B.
54	RWX	INCOMPLETE_RD_CAL_N3: Read centering/DQS alignment/coarse read alignment error. This bit is set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD12B - MEMINTD15B.
55	RWX	COARSE_PATTERN_ERR_N0: Coarse read alignment error. This bit is set when the coarse read alignment algorithm does not receive a valid pattern fragment on pins MEMINTD00B - MEMINTD03B.
56	RWX	COARSE_PATTERN_ERR_N1: Coarse read alignment error. This bit is set when the coarse read alignment algorithm does not receive a valid pattern fragment on pins MEMINTD04B - MEMINTD07B.
57	RWX	COARSE_PATTERN_ERR_N2: Coarse read alignment error. This bit is set when the coarse read alignment algorithm does not receive a valid pattern fragment on pins MEMINTD08B - MEMINTD11B.
58	RWX	COARSE_PATTERN_ERR_N3: Coarse read alignment error. This bit is set when the coarse read alignment algorithm does not receive a valid pattern fragment on pins MEMINTD12B - MEMINTD15B.
59	RWX	EYE_CLIPPING: Read centering error/status. This bit activates whenever the eye center is out of the range of the strobe delay line. This is an expected condition for negative values of Trdqsdq (DQ arrives before DQS). The DDR PHY is usually capable of compensating for this. In a typical configuration, the EYE_CLIPPLING_MASK bit must be set to 1b so that this condition is not reported as an error. When EYE_CLIPPING_MASK is 1b, the read centering algorithm continues calibration by using an adjacent DQS edge to perform centering. This configures normal operation of the DDR PHY in most cases, with the margin for inter-symbol interference, and random noise is reduced. The extent of margin reduction is dependent on jitter and the DCD characteristics of the DRAM.
60	RWX	NO_DQS: DQS alignment error/status. This bit is set when a strobe edge was not detected during DQS alignment calibration. If a strobe is stuck or broken, its location cannot be determined. Thus, it is not possible to guarantee that rank-to-rank switching delays differ by no more than 1/2 UI. Therefore, an extra cycle of gap on rank-to-rank switching must be maintained. You can use the firmware to recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings that are associated with stuck or broken strobes to maintain the 1/2 UI rank-to-rank compression rule.

Bits	SCOM	Field Mnemonic: Description
61	RWX	NO_LOCK: DQS alignment error and status. This bit is set when a phase rotator lock could not be attained on a strobe during DQS alignment calibration. The No Lock error detect circuit detects a DQS strobe that is always 1b or always 0b. When a DQS strobe is always 1b or 0b, it is considered missing or stuck. The No Lock circuit sets this bit when: It does not have a valid strobe for more than 30 samples (that is, 30 samples x 27 tCK per sample = 810 tCK) and The strobe then goes missing or stuck for at least 13 samples (that is, 13 samples x 27 tCK per sample = 351 tCK). If a strobe is stuck or broken, its location cannot be determined. Thus, it is not possible to guarantee that rank-to-rank switching delays differ by no more than 1/2 UI. Therefore, an extra cycle of gap on rank-to-rank switching must be maintained. Firmware can optionally recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings associated with stuck/broken strobes in a way that maintains the 1/2 UI rank-to-rank compression rule.
62	RWX	DRIFT_ERROR: Periodic read calibration error/status: This bit is set when a DQS signal has drifted further than the limit set in the MAX_DQS_DRIFT field of the DP16 Drift Limits Register. The drift limit can be configured very tightly, in which case the activation of this bit is typically informational. Alternatively, it can be configured to a larger value that might indicate rank-to-rank switching is unreliable. Even in such a case, it can be ignored if the application uses a parity of ECC code as the final arbiter.
63	RWX	MIN_EYE: Periodic read calibration error/status: This bit is set when a data eye has closed to a value less than the value set in the MIN_RD_EYE_SIZE field of the DP16 Drift Limits Register. The minimum eye size can be configured to a value that is informational, or it can be configured to a limit that reflects a customer's maximum tolerance for errors. In that case, it can be considered to be an error.

Register Name	**DP16 Read Status 0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_RD_STATUS0_P3_[n]
Address	8000001407011C3F (SCOM), +0x0400_0000_0000
Description	This register contains status information about read calibrations. The bits in this register can only be set by hardware when the corresponding mask bit is not set in the DP16 Read Error Mask 0 Register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RWX	NO_EYE_DETECTED: Read centering error. No eye was detected on at least one of the data pins by one of the DP16 logic blocks.
49	RWX	LEADING_EDGE_NOT_FOUND: Read centering error. This bit is set when at least one of the leading edges of the data eyes of the data bits are not found during a calibration.
50	RWX	TRAILING_EDGE_NOT_FOUND: Read centering error. This bit is set when at least one of the trailing edges of the data eyes of the data bits are not found during a calibration.
51	RWX	INCOMPLETE_RD_CAL_N0: Read centering/DQS alignment/coarse read alignment error. This bit is set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD00B - MEMINTD03B.
52	RWX	INCOMPLETE_RD_CAL_N1: Read centering/DQS alignment/coarse read alignment error. This bit is set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD04B - MEMINTD07B.
53	RWX	INCOMPLETE_RD_CAL_N2: Read centering/DQS alignment/coarse read alignment error. This bit is set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a a read calibration operation on pins MEMINTD08B - MEMINTD11B.

Bits	SCOM	Field Mnemonic: Description
54	RWX	INCOMPLETE_RD_CAL_N3: Read centering/DQS alignment/coarse read alignment error. This bit is set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD12B - MEMINTD15B.
55	RWX	COARSE_PATTERN_ERR_N0: Coarse read alignment error. This bit is set when the coarse read alignment algorithm does not receive a valid pattern fragment on pins MEMINTD00B - MEMINTD03B.
56	RWX	COARSE_PATTERN_ERR_N1: Coarse read alignment error. This bit is set when the coarse read alignment algorithm does not receive a valid pattern fragment on pins MEMINTD04B - MEMINTD07B.
57	RWX	COARSE_PATTERN_ERR_N2: Coarse read alignment error. This bit is set when the coarse read alignment algorithm does not receive a valid pattern fragment on pins MEMINTD08B - MEMINTD11B.
58	RWX	COARSE_PATTERN_ERR_N3: Coarse read alignment error. This bit is set when the coarse read alignment algorithm does not receive a valid pattern fragment on pins MEMINTD12B - MEMINTD15B.
59	RWX	EYE_CLIPPING: Read centering error/status. This bit activates whenever the eye center is out of the range of the strobe delay line. This is an expected condition for negative values of Trdqsdq (DQ arrives before DQS). The DDR PHY is usually capable of compensating for this. In a typical configuration, the EYE_CLIPPLING_MASK bit must be set to 1b so that this condition is not reported as an error. When EYE_CLIPPING_MASK is 1b, the read centering algorithm continues calibration by using an adjacent DQS edge to perform centering. This configures normal operation of the DDR PHY in most cases, with the margin for inter-symbol interference, and random noise is reduced. The extent of margin reduction is dependent on jitter and the DCD characteristics of the DRAM.
60	RWX	NO_DQS: DQS alignment error/status. This bit is set when a strobe edge was not detected during DQS alignment calibration. If a strobe is stuck or broken, its location cannot be determined. Thus, it is not possible to guarantee that rank-to-rank switching delays differ by no more than 1/2 UI. Therefore, an extra cycle of gap on rank-to-rank switching must be maintained. You can use the firmware to recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings that are associated with stuck or broken strobes to maintain the 1/2 UI rank-to-rank compression rule.
61	RWX	NO_LOCK: DQS alignment error and status. This bit is set when a phase rotator lock could not be attained on a strobe during DQS alignment calibration. The No Lock error detect circuit detects a DQS strobe that is always 1b or always 0b. When a DQS strobe is always 1b or 0b, it is considered missing or stuck. The No Lock circuit sets this bit when: It does not have a valid strobe for more than 30 samples (that is, 30 samples x 27 tCK per sample = 810 tCK) and The strobe then goes missing or stuck for at least 13 samples (that is, 13 samples x 27 tCK per sample = 351 tCK). If a strobe is stuck or broken, its location cannot be determined. Thus, it is not possible to guarantee that rank-to-rank switching delays differ by no more than 1/2 UI. Therefore, an extra cycle of gap on rank-to-rank switching must be maintained. Firmware can optionally recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings associated with stuck/broken strobes in a way that maintains the 1/2 UI rank-to-rank compression rule.
62	RWX	DRIFT_ERROR: Periodic read calibration error/status: This bit is set when a DQS signal has drifted further than the limit set in the MAX_DQS_DRIFT field of the DP16 Drift Limits Register. The drift limit can be configured very tightly, in which case the activation of this bit is typically informational. Alternatively, it can be configured to a larger value that might indicate rank-to-rank switching is unreliable. Even in such a case, it can be ignored if the application uses a parity of ECC code as the final arbiter.
63	RWX	MIN_EYE: Periodic read calibration error/status: This bit is set when a data eye has closed to a value less than the value set in the MIN_RD_EYE_SIZE field of the DP16 Drift Limits Register. The minimum eye size can be configured to a value that is informational, or it can be configured to a limit that reflects a customer's maximum tolerance for errors. In that case, it can be considered to be an error.

Register Name	DP16 Read Error Mask 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_ERROR_MASK0_P0_[n]
Address	800000150701103F (SCOM), +0x0400_0000_0000
Description	This register masks errors in the DP16 Read Status 0 Register. Thus, it prevents the RD_CNTL_ERROR bit from being set in the RC Error Status 0 Register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	NO_EYE_DETECTED_MASK: 1 = Mask the NO_EYE_DETECTED error.
49	RW	LEADING_EDGE_FOUND_MASK: 1 = Mask the LEADING_EDGE_FOUND error.
50	RW	TRAILING_EDGE_FOUND_MASK: 1 = Mask the TRAILING_EDGE_FOUND error.
51	RW	INCOMPLETE_RD_CAL_N0_MASK: 1 = Mask the INCOMPLETE_RD_CAL_N0 error.
52	RW	INCOMPLETE_RD_CAL_N1_MASK: 1 = Mask the INCOMPLETE_RD_CAL_N1 error.
53	RW	INCOMPLETE_RD_CAL_N2_MASK: 1 = Mask the INCOMPLETE_RD_CAL_N2 error.
54	RW	INCOMPLETE_RD_CAL_N3_MASK: 1 = Mask the INCOMPLETE_RD_CAL_N3 error.
55	RW	COARSE_PATTERN_ERR_N0_MASK: 1 = Mask the COARSE_PATTERN_ERR_N0 error.
56	RW	COARSE_PATTERN_ERR_N1_MASK: 1 = Mask the COARSE_PATTERN_ERR_N1 error.
57	RW	COARSE_PATTERN_ERR_N2_MASK: 1 = Mask the COARSE_PATTERN_ERR_N2 error.
58	RW	COARSE_PATTERN_ERR_N3_MASK: 1 = Mask the COARSE_PATTERN_ERR_N3 error.
59	RW	EYE_CLIPPING_MASK: 1 = Mask the EYE_CLIPPING error.
60	RW	NO_DQS_MASK: 1 = Mask the NO_DQS error.
61	RW	NO_LOCK_MASK: 1 = Mask the NO_LOCK error.
62	RW	DRIFT_ERROR_MASK: 1 = Mask the DRIFT_ERROR error.
63	RW	MIN_EYE_MASK: 1 = Mask the MIN_EYE error.

Register Name	DP16 Read Error Mask 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_ERROR_MASK0_P1_[n]
Address	800000150701143F (SCOM), +0x0400_0000_0000
Description	This register masks errors in the DP16 Read Status 0 Register. Thus, it prevents the RD_CNTL_ERROR bit from being set in the RC Error Status 0 Register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	NO_EYE_DETECTED_MASK: 1 = Mask the NO_EYE_DETECTED error.
49	RW	LEADING_EDGE_FOUND_MASK: 1 = Mask the LEADING_EDGE_FOUND error.
50	RW	TRAILING_EDGE_FOUND_MASK: 1 = Mask the TRAILING_EDGE_FOUND error.
51	RW	INCOMPLETE_RD_CAL_N0_MASK: 1 = Mask the INCOMPLETE_RD_CAL_N0 error.
52	RW	INCOMPLETE_RD_CAL_N1_MASK: 1 = Mask the INCOMPLETE_RD_CAL_N1 error.
53	RW	INCOMPLETE_RD_CAL_N2_MASK: 1 = Mask the INCOMPLETE_RD_CAL_N2 error.
54	RW	INCOMPLETE_RD_CAL_N3_MASK: 1 = Mask the INCOMPLETE_RD_CAL_N3 error.
55	RW	COARSE_PATTERN_ERR_N0_MASK: 1 = Mask the COARSE_PATTERN_ERR_N0 error.
56	RW	COARSE_PATTERN_ERR_N1_MASK: 1 = Mask the COARSE_PATTERN_ERR_N1 error.
57	RW	COARSE_PATTERN_ERR_N2_MASK: 1 = Mask the COARSE_PATTERN_ERR_N2 error.
58	RW	COARSE_PATTERN_ERR_N3_MASK: 1 = Mask the COARSE_PATTERN_ERR_N3 error.
59	RW	EYE_CLIPPING_MASK: 1 = Mask the EYE_CLIPPING error.
60	RW	NO_DQS_MASK: 1 = Mask the NO_DQS error.
61	RW	NO_LOCK_MASK: 1 = Mask the NO_LOCK error.
62	RW	DRIFT_ERROR_MASK: 1 = Mask the DRIFT_ERROR error.
63	RW	MIN_EYE_MASK: 1 = Mask the MIN_EYE error.

Register Name	DP16 Read Error Mask 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_ERROR_MASK0_P2_[n]
Address	800000150701183F (SCOM), +0x0400_0000_0000
Description	This register masks errors in the DP16 Read Status 0 Register. Thus, it prevents the RD_CNTL_ERROR bit from being set in the RC Error Status 0 Register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	NO_EYE_DETECTED_MASK: 1 = Mask the NO_EYE_DETECTED error.
49	RW	LEADING_EDGE_FOUND_MASK: 1 = Mask the LEADING_EDGE_FOUND error.
50	RW	TRAILING_EDGE_FOUND_MASK: 1 = Mask the TRAILING_EDGE_FOUND error.
51	RW	INCOMPLETE_RD_CAL_N0_MASK: 1 = Mask the INCOMPLETE_RD_CAL_N0 error.
52	RW	INCOMPLETE_RD_CAL_N1_MASK: 1 = Mask the INCOMPLETE_RD_CAL_N1 error.
53	RW	INCOMPLETE_RD_CAL_N2_MASK: 1 = Mask the INCOMPLETE_RD_CAL_N2 error.
54	RW	INCOMPLETE_RD_CAL_N3_MASK: 1 = Mask the INCOMPLETE_RD_CAL_N3 error.
55	RW	COARSE_PATTERN_ERR_N0_MASK: 1 = Mask the COARSE_PATTERN_ERR_N0 error.
56	RW	COARSE_PATTERN_ERR_N1_MASK: 1 = Mask the COARSE_PATTERN_ERR_N1 error.
57	RW	COARSE_PATTERN_ERR_N2_MASK: 1 = Mask the COARSE_PATTERN_ERR_N2 error.
58	RW	COARSE_PATTERN_ERR_N3_MASK: 1 = Mask the COARSE_PATTERN_ERR_N3 error.
59	RW	EYE_CLIPPING_MASK: 1 = Mask the EYE_CLIPPING error.
60	RW	NO_DQS_MASK: 1 = Mask the NO_DQS error.
61	RW	NO_LOCK_MASK: 1 = Mask the NO_LOCK error.
62	RW	DRIFT_ERROR_MASK: 1 = Mask the DRIFT_ERROR error.
63	RW	MIN_EYE_MASK: 1 = Mask the MIN_EYE error.

Register Name	**DP16 Read Error Mask 0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_RD_ERROR_MASK0_P3_[n]
Address	8000001507011C3F (SCOM), +0x0400_0000_0000
Description	This register masks errors in the DP16 Read Status 0 Register. Thus, it prevents the RD_CNTL_ERROR bit from being set in the RC Error Status 0 Register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	NO_EYE_DETECTED_MASK: 1 = Mask the NO_EYE_DETECTED error.

Bits	SCOM	Field Mnemonic: Description
49	RW	LEADING_EDGE_FOUND_MASK: 1 = Mask the LEADING_EDGE_FOUND error.
50	RW	TRAILING_EDGE_FOUND_MASK: 1 = Mask the TRAILING_EDGE_FOUND error.
51	RW	INCOMPLETE_RD_CAL_N0_MASK: 1 = Mask the INCOMPLETE_RD_CAL_N0 error.
52	RW	INCOMPLETE_RD_CAL_N1_MASK: 1 = Mask the INCOMPLETE_RD_CAL_N1 error.
53	RW	INCOMPLETE_RD_CAL_N2_MASK: 1 = Mask the INCOMPLETE_RD_CAL_N2 error.
54	RW	INCOMPLETE_RD_CAL_N3_MASK: 1 = Mask the INCOMPLETE_RD_CAL_N3 error.
55	RW	COARSE_PATTERN_ERR_N0_MASK: 1 = Mask the COARSE_PATTERN_ERR_N0 error.
56	RW	COARSE_PATTERN_ERR_N1_MASK: 1 = Mask the COARSE_PATTERN_ERR_N1 error.
57	RW	COARSE_PATTERN_ERR_N2_MASK: 1 = Mask the COARSE_PATTERN_ERR_N2 error.
58	RW	COARSE_PATTERN_ERR_N3_MASK: 1 = Mask the COARSE_PATTERN_ERR_N3 error.
59	RW	EYE_CLIPPING_MASK: 1 = Mask the EYE_CLIPPING error.
60	RW	NO_DQS_MASK: 1 = Mask the NO_DQS error.
61	RW	NO_LOCK_MASK: 1 = Mask the NO_LOCK error.
62	RW	DRIFT_ERROR_MASK: 1 = Mask the DRIFT_ERROR error.
63	RW	MIN_EYE_MASK: 1 = Mask the MIN_EYE error.

Register Name	**DP16 Read VREF DAC 0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_DAC_0_P0_[n]
Address	800000160701103F (SCOM), +0x0400_0000_0000
Description	This register controls the digital-to-analog converter (DAC) settings of the read reference voltage (VREF) in the DP16 unit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RWX	NIB0_EN_FORCE: This bit overrides the logic enabling the comparator in the analog DACs for nibble 0 (bits 0:3 of 0:15) to set them to the value specified in the DP16 Read VREF DAC Comparator Ouptut Register. The binary string sent to the DAC is the value in BIT0_VREF_DAC. This allows the user to manually set the enable bits and DAC value for each nibble. The output of the comparator is captured in the DP16 Read VREF DAC Comparator Output Register. While read VREF calibration is running, this bit has no effect.

Bits	SCOM	Field Mnemonic: Description
49:55	RWX	BIT0_VREF_DAC: DAC settings to control VREF on bit0 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE =1, this field reverts to the average of nibble 0.
56	RWX	NIB1_EN_FORCE: This bit overrides the logic enabling the comparator in the analog DACs for nibble 1 (bits 4:7 of 0:15) to set them to the value specified in the DP16 Read VREF DAC Comparator Ouptut Register. The binary string sent to the DAC is the value in BIT1_VREF_DAC. This allows the user to manually set the enable bits and DAC value for each nibble. The output of the comparator is captured in the DP16 Read VREF DAC Comparator Output Register. While read VREF calibration is running, this bit has no effect.
57:63	RWX	BIT1_VREF_DAC: DAC settings to control VREF on bit 1 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field reverts to the average of nibble 1.

Register Name	**DP16 Read VREF DAC 0 Register[n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_DAC_0_P1_[n]
Address	800000160701143F (SCOM), +0x0400_0000_0000
Description	This register controls the DAC settings of the read VREF in the DP16 unit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RWX	NIB0_EN_FORCE: This bit overrides the logic enabling the comparator in the analog DACs for nibble 0 (bits 0:3 of 0:15) to set them to the value specified in the DP16 Read VREF DAC Comparator Ouptut Register. The binary string sent to the DAC is the value in BIT0_VREF_DAC. This allows the user to manually set the enable bits and DAC value for each nibble. The output of the comparator is captured in the DP16 Read VREF DAC Comparator Output Register. While read VREF calibration is running, this bit has no effect.
49:55	RWX	BIT0_VREF_DAC: DAC settings to control VREF on bit0 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE =1, this field reverts to the average of nibble 0.
56	RWX	NIB1_EN_FORCE: This bit overrides the logic enabling the comparator in the analog DACs for nibble 1 (bits 4:7 of 0:15) to set them to the value specified in the DP16 Read VREF DAC Comparator Ouptut Register. The binary string sent to the DAC is the value in BIT1_VREF_DAC. This allows the user to manually set the enable bits and DAC value for each nibble. The output of the comparator is captured in the DP16 Read VREF DAC Comparator Output Register. While read VREF calibration is running, this bit has no effect.
57:63	RWX	BIT1_VREF_DAC: DAC settings to control VREF on bit 1 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field reverts to the average of nibble 1.

Register Name	**DP16 Read VREF DAC 0 Register[n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_DAC_0_P2_[n]
Address	800000160701183F (SCOM), +0x0400_0000_0000
Description	This register controls the DAC settings of the read VREF in the DP16 unit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	NIB0_EN_FORCE: This bit overrides the logic enabling the comparator in the analog DACs for nibble 0 (bits 0:3 of 0:15) to set them to the value specified in the DP16 Read VREF DAC Comparator Ouptut Register. The binary string sent to the DAC is the value in BIT0_VREF_DAC. This allows the user to manually set the enable bits and DAC value for each nibble. The output of the comparator is captured in the DP16 Read VREF DAC Comparator Output Register. While read VREF calibration is running, this bit has no effect.
49:55	RWX	BIT0_VREF_DAC: DAC settings to control VREF on bit0 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE =1, this field reverts to the average of nibble 0.
56	RWX	NIB1_EN_FORCE: This bit overrides the logic enabling the comparator in the analog DACs for nibble 1 (bits 4:7 of 0:15) to set them to the value specified in the DP16 Read VREF DAC Comparator Ouptut Register. The binary string sent to the DAC is the value in BIT1_VREF_DAC. This allows the user to manually set the enable bits and DAC value for each nibble. The output of the comparator is captured in the DP16 Read VREF DAC Comparator Output Register. While read VREF calibration is running, this bit has no effect.
57:63	RWX	BIT1_VREF_DAC: DAC settings to control VREF on bit 1 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field reverts to the average of nibble 1.

Register Name	**DP16 Read VREF DAC 0 Register[n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_DAC_0_P3_[n]
Address	8000001607011C3F (SCOM), +0x0400_0000_0000
Description	This register controls the DAC settings of the read VREF in the DP16 unit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RWX	NIB0_EN_FORCE: This bit overrides the logic enabling the comparator in the analog DACs for nibble 0 (bits 0:3 of 0:15) to set them to the value specified in the DP16 Read VREF DAC Comparator Ouptut Register. The binary string sent to the DAC is the value in BIT0_VREF_DAC. This allows the user to manually set the enable bits and DAC value for each nibble. The output of the comparator is captured in the DP16 Read VREF DAC Comparator Output Register. While read VREF calibration is running, this bit has no effect.
49:55	RWX	BIT0_VREF_DAC: DAC settings to control VREF on bit0 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE =1, this field reverts to the average of nibble 0.
56	RWX	NIB1_EN_FORCE: This bit overrides the logic enabling the comparator in the analog DACs for nibble 1 (bits 4:7 of 0:15) to set them to the value specified in the DP16 Read VREF DAC Comparator Ouptut Register. The binary string sent to the DAC is the value in BIT1_VREF_DAC. This allows the user to manually set the enable bits and DAC value for each nibble. The output of the comparator is captured in the DP16 Read VREF DAC Comparator Output Register. While read VREF calibration is running, this bit has no effect.
57:63	RWX	BIT1_VREF_DAC: DAC settings to control VREF on bit 1 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field reverts to the average of nibble 1.

Register Name	DP16 Write Leveling Status 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_LVL_STATUS0_P0_[n]
Address	800000170701103F (SCOM), +0x0400_0000_0000
Description	This register contains status information about write calibrations.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:49	RW	CLK_LEVEL: This field is valid when the DONE bit is set. This field indicates which DQS strobe/clock completed write leveling. 00 = CLK16. 01 = CLK18. 10 = CLK20. 11 = CLK22.
50	RW	FINE_STEPPING: 0 = The write-leveling algorithm is doing the BIG_STEP portion of the algorithm. 1 = The write-leveling algorithm is doing the SMALL_STEP portion of the algorithm.
51	RW	DONE: This bit is set when the write-leveling algorithm completes.
52	RW	WL_ERR_CLK16: This bit is set when the write-leveling algorithm cannot find a write-leveling solution for CLK 16.
53	RW	WL_ERR_CLK18: This bit is set when the write-leveling algorithm cannot find a write-leveling solution for CLK 18.
54	RW	WL_ERR_CLK20: This bit is set when the write-leveling algorithm cannot find a write-leveling solution for CLK 20.
55	RW	WL_ERR_CLK22: This bit is set when the write-leveling algorithm cannot find a write-leveling solution for CLK 22.
56	RW	ZERO_DETECTED: 0 = The write-leveling algorithm has not detected a low (0b) sample. 1 = The write-leveling algorithm has detected a low (0b) sample.
57:63	RO	Constant = 0b0000000

Register Name	DP16 Write Leveling Status 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_LVL_STATUS0_P1_[n]
Address	800000170701143F (SCOM), +0x0400_0000_0000
Description	This register contains status information about write calibrations.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:49	RW	CLK_LEVEL: This field is valid when the DONE bit is set. This field indicates which DQS strobe/clock completed write leveling. 00 = CLK16. 01 = CLK18. 10 = CLK20. 11 = CLK22.
50	RW	FINE_STEPPING: 0 = The write-leveling algorithm is doing the BIG_STEP portion of the algorithm. 1 = The write-leveling algorithm is doing the SMALL_STEP portion of the algorithm.
51	RW	DONE: This bit is set when the write-leveling algorithm completes.

Bits	SCOM	Field Mnemonic: Description
52	RW	WL_ERR_CLK16: This bit is set when the write-leveling algorithm cannot find a write-leveling solution for CLK 16.
53	RW	WL_ERR_CLK18: This bit is set when the write-leveling algorithm cannot find a write-leveling solution for CLK 18.
54	RW	WL_ERR_CLK20: This bit is set when the write-leveling algorithm cannot find a write-leveling solution for CLK 20.
55	RW	WL_ERR_CLK22: This bit is set when the write-leveling algorithm cannot find a write-leveling solution for CLK 22.
56	RW	ZERO_DETECTED: 0 = The write-leveling algorithm has not detected a low (0b) sample. 1 = The write-leveling algorithm has detected a low (0b) sample.
57:63	RO	Constant = 0b0000000

Register Name	**DP16 Write Leveling Status 0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_WR_LVL_STATUS0_P2_[n]
Address	800000170701183F (SCOM), +0x0400_0000_0000
Description	This register contains status information about write calibrations.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:49	RW	CLK_LEVEL: This field is valid when the DONE bit is set. This field indicates which DQS strobe/clock completed write leveling. 00 = CLK16. 01 = CLK18. 10 = CLK20. 11 = CLK22.
50	RW	FINE_STEPPING: 0 = The write-leveling algorithm is doing the BIG_STEP portion of the algorithm. 1 = The write-leveling algorithm is doing the SMALL_STEP portion of the algorithm.
51	RW	DONE: This bit is set when the write-leveling algorithm completes.
52	RW	WL_ERR_CLK16: This bit is set when the write-leveling algorithm cannot find a write-leveling solution for CLK 16.
53	RW	WL_ERR_CLK18: This bit is set when the write-leveling algorithm cannot find a write-leveling solution for CLK 18.
54	RW	WL_ERR_CLK20: This bit is set when the write-leveling algorithm cannot find a write-leveling solution for CLK 20.
55	RW	WL_ERR_CLK22: This bit is set when the write-leveling algorithm cannot find a write-leveling solution for CLK 22.
56	RW	ZERO_DETECTED: 0 = The write-leveling algorithm has not detected a low (0b) sample. 1 = The write-leveling algorithm has detected a low (0b) sample.
57:63	RO	Constant = 0b0000000

Register Name	DP16 Write Leveling Status 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_LVL_STATUS0_P3_[n]
Address	8000001707011C3F (SCOM), +0x0400_0000_0000
Description	This register contains status information about write calibrations.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:49	RW	CLK_LEVEL: This field is valid when the DONE bit is set. This field indicates which DQS strobe/clock completed write leveling. 00 = CLK16. 01 = CLK18. 10 = CLK20. 11 = CLK22.
50	RW	FINE_STEPPING: 0 = The write-leveling algorithm is doing the BIG_STEP portion of the algorithm. 1 = The write-leveling algorithm is doing the SMALL_STEP portion of the algorithm.
51	RW	DONE: This bit is set when the write-leveling algorithm completes.
52	RW	WL_ERR_CLK16: This bit is set when the write-leveling algorithm cannot find a write-leveling solution for CLK 16.
53	RW	WL_ERR_CLK18: This bit is set when the write-leveling algorithm cannot find a write-leveling solution for CLK 18.
54	RW	WL_ERR_CLK20: This bit is set when the write-leveling algorithm cannot find a write-leveling solution for CLK 20.
55	RW	WL_ERR_CLK22: This bit is set when the write-leveling algorithm cannot find a write-leveling solution for CLK 22.
56	RW	ZERO_DETECTED: 0 = The write-leveling algorithm has not detected a low (0b) sample. 1 = The write-leveling algorithm has detected a low (0b) sample.
57:63	RO	Constant = 0b0000000

Register Name	DP16 Write Centering Status 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_CNTR_STATUS0_P0_[n]
Address	800000180701103F (SCOM), +0x0400_0000_0000
Description	This register contains status information about write-centering calibrations.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:52	RW	BIT_CENTERED: When the DONE bit is set, this field contains the bit number (0 - 23) on which the write-centering algorithm has been applied.
53	RW	SMALL_STEP_LEFT: This bit is set when valid data is sampled when the write-centering algorithm is big stepping to the right to find the first valid data sample. When this bit is set, the write-centering algorithm begins to small step to the left to find the left edge of the eye, the first invalid data sample. This bit is reset when write-centering starts on a new bit (DONE = 0b or BIT_CENTERED does not equal the bit being write centered).

Bits	SCOM	Field Mnemonic: Description
54	RW	BIG_STEP_RIGHT: This bit is set when invalid data is sampled when the write-centering algorithm is small stepping to the left and finds the left edge of the eye. When this bit is set, the write-centering algorithm begins to big step to the right to find valid data again. This bit is reset when write-centering starts on a new bit (DONE = 0b or BIT_CENTERED does not equal the bit being write centered).
55	RW	MATCH_STEP_RIGHT: This bit is set when valid data is sampled when the write-centering algorithm is big stepping to the right after finding the left edge of the eye. When this bit is set, the write-centering algorithm continues to big step to the right to find the right edge of the eye. This bit is reset when write centering starts on a new bit (DONE = 0b or BIT_CENTERED does not equal the bit being write centered).
56	RW	JUMP_BACK_RIGHT: This bit is set when invalid data is sampled when the write-centering algorithm is big stepping to the right to find the right side of the eye. When this bit is set, the write-centering algorithm big steps to the left to find valid data. This bit is reset when write centering starts on a new bit (DONE = 0b or BIT_CENTERED does not equal the bit being write centered).
57	RW	SMALL_STEP_RIGHT: This bit is set when valid data is sampled when the write-centering algorithm is big stepping to the left to find valid data. When this bit is set, the write-centering algorithm small steps to the right to find the right side of the eye, the first invalid data sample. This bit is reset when write centering starts on a new bit (DONE = 0b or BIT_CENTERED does not equal the bit being write centered).
58	RW	DONE: This bit is set when invalid data is sampled when the write-centering algorithm is small stepping to the right to find the right side of the eye. When the write-centering algorithm completes successfully, this bit is set and the average of the left side and right side delay values is loaded into the DP16 Write Delay Value Register {0-23}, which corresponds to the bit being write centered. When the write-centering algorithm finds an error, this bit is set and the current delay value being used by the algorithm is loaded into the DP16 Write Delay Value Register {0-23}. The bit number being write centered is loaded into the BIT_CENTERED field when this bit is set. This bit is reset when write centering starts on a new bit (DONE = 0b or BIT_CENTERED does not equal the bit being write centered).
59:63	RO	Constant = 0b00000

Register Name	**DP16 Write Centering Status 0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_WR_CNTR_STATUS0_P1_[n]
Address	800000180701143F (SCOM), +0x0400_0000_0000
Description	This register contains status information about write-centering calibrations.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:52	RW	BIT_CENTERED: When the DONE bit is set, this field contains the bit number (0 - 23) on which the write-centering algorithm has been applied.
53	RW	SMALL_STEP_LEFT: This bit is set when valid data is sampled when the write-centering algorithm is big stepping to the right to find the first valid data sample. When this bit is set, the write-centering algorithm begins to small step to the left to find the left edge of the eye, the first invalid data sample. This bit is reset when write centering starts on a new bit (DONE = 0b or BIT_CENTERED does not equal the bit being write centered).
54	RW	BIG_STEP_RIGHT: This bit is set when invalid data is sampled when the write-centering algorithm is small stepping to the left and finds the left edge of the eye. When this bit is set, the write-centering algorithm begins to big step to the right to find valid data again. This bit is reset when write centering starts on a new bit (DONE = 0b or BIT_CENTERED does not equal the bit being write centered).

Bits	SCOM	Field Mnemonic: Description
55	RW	MATCH_STEP_RIGHT: This bit is set when valid data is sampled when the write-centering algorithm is big stepping to the right after finding the left edge of the eye. When this bit is set, the write-centering algorithm continues to big step to the right to find the right edge of the eye. This bit is reset when write centering starts on a new bit (DONE = 0b or BIT_CENTERED does not equal the bit being write centered).
56	RW	JUMP_BACK_RIGHT: This bit is set when invalid data is sampled when the write-centering algorithm is big stepping to the right to find the right side of the eye. When this bit is set, the write-centering algorithm big steps to the left to find valid data. This bit is reset when write centering starts on a new bit (DONE = 0b or BIT_CENTERED does not equal the bit being write centered).
57	RW	SMALL_STEP_RIGHT: This bit is set when valid data is sampled when the write-centering algorithm is big stepping to the left to find valid data. When this bit is set, the write-centering algorithm small steps to the right to find the right side of the eye, the first invalid data sample. This bit is reset when write centering starts on a new bit (DONE = 0b or BIT_CENTERED does not equal the bit being write centered).
58	RW	DONE: This bit is set when invalid data is sampled when the write-centering algorithm is small stepping to the right to find the right side of the eye. When the write-centering algorithm completes successfully, this bit is set and the average of the left side and right side delay values is loaded into the DP16 Write Delay Value Register {0-23}, which corresponds to the bit being write centered. When the write-centering algorithm finds an error, this bit is set and the current delay value being used by the algorithm is loaded into the DP16 Write Delay Value Register {0-23}. The bit number being write centered is loaded into the BIT_CENTERED field when this bit is set. This bit is reset when write centering starts on a new bit (DONE = 0b or BIT_CENTERED does not equal the bit being write centered).
59:63	RO	Constant = 0b00000

Register Name	**DP16 Write Centering Status 0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_WR_CNTR_STATUS0_P2_[n]
Address	800000180701183F (SCOM), +0x0400_0000_0000
Description	This register contains status information about write-centering calibrations.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48:52	RW	BIT_CENTERED: When the DONE bit is set, this field contains the bit number (0 - 23) on which the write-centering algorithm has been applied.
53	RW	SMALL_STEP_LEFT: This bit is set when valid data is sampled when the write-centering algorithm is big stepping to the right to find the first valid data sample. When this bit is set, the write-centering algorithm begins to small step to the left to find the left edge of the eye, the first invalid data sample. This bit is reset when write centering starts on a new bit (DONE = 0b or BIT_CENTERED does not equal the bit being write centered).
54	RW	BIG_STEP_RIGHT: This bit is set when invalid data is sampled when the write-centering algorithm is small stepping to the left and finds the left edge of the eye. When this bit is set, the write-centering algorithm begins to big step to the right to find valid data again. This bit is reset when write centering starts on a new bit (DONE = 0b or BIT_CENTERED does not equal the bit being write centered).
55	RW	MATCH_STEP_RIGHT: This bit is set when valid data is sampled when the write-centering algorithm is big stepping to the right after finding the left edge of the eye. When this bit is set, the write-centering algorithm continues to big step to the right to find the right edge of the eye. This bit is reset when write centering starts on a new bit (DONE = 0b or BIT_CENTERED does not equal the bit being write centered).

Bits	SCOM	Field Mnemonic: Description
56	RW	JUMP_BACK_RIGHT: This bit is set when invalid data is sampled when the write-centering algorithm is big stepping to the right to find the right side of the eye. When this bit is set, the write-centering algorithm big steps to the left to find valid data. This bit is reset when write centering starts on a new bit (DONE = 0b or BIT_CENTERED does not equal the bit being write centered).
57	RW	SMALL_STEP_RIGHT: This bit is set when valid data is sampled when the write-centering algorithm is big stepping to the left to find valid data. When this bit is set, the write-centering algorithm small steps to the right to find the right side of the eye, the first invalid data sample. This bit is reset when write centering starts on a new bit (DONE = 0b or BIT_CENTERED does not equal the bit being write centered).
58	RW	DONE: This bit is set when invalid data is sampled when the write-centering algorithm is small stepping to the right to find the right side of the eye. When the write-centering algorithm completes successfully, this bit is set and the average of the left side and right side delay values is loaded into the DP16 Write Delay Value Register {0-23}, which corresponds to the bit being write centered. When the write-centering algorithm finds an error, this bit is set and the current delay value being used by the algorithm is loaded into the DP16 Write Delay Value Register {0-23}. The bit number being write centered is loaded into the BIT_CENTERED field when this bit is set. This bit is reset when write centering starts on a new bit (DONE = 0b or BIT_CENTERED does not equal the bit being write centered).
59:63	RO	Constant = 0b00000

Register Name	**DP16 Write Centering Status 0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_WR_CNTR_STATUS0_P3_[n]
Address	8000001807011C3F (SCOM), +0x0400_0000_0000
Description	This register contains status information about write-centering calibrations.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48:52	RW	BIT_CENTERED: When the DONE bit is set, this field contains the bit number (0 - 23) on which the write-centering algorithm has been applied.
53	RW	SMALL_STEP_LEFT: This bit is set when valid data is sampled when the write-centering algorithm is big stepping to the right to find the first valid data sample. When this bit is set, the write-centering algorithm begins to small step to the left to find the left edge of the eye, the first invalid data sample. This bit is reset when write centering starts on a new bit (DONE = 0b or BIT_CENTERED does not equal the bit being write centered).
54	RW	BIG_STEP_RIGHT: This bit is set when invalid data is sampled when the write-centering algorithm is small stepping to the left and finds the left edge of the eye. When this bit is set, the write-centering algorithm begins to big step to the right to find valid data again. This bit is reset when write centering starts on a new bit (DONE = 0b or BIT_CENTERED does not equal the bit being write centered).
55	RW	MATCH_STEP_RIGHT: This bit is set when valid data is sampled when the write-centering algorithm is big stepping to the right after finding the left edge of the eye. When this bit is set, the write-centering algorithm continues to big step to the right to find the right edge of the eye. This bit is reset when write centering starts on a new bit (DONE = 0b or BIT_CENTERED does not equal the bit being write centered).
56	RW	JUMP_BACK_RIGHT: This bit is set when invalid data is sampled when the write-centering algorithm is big stepping to the right to find the right side of the eye. When this bit is set, the write-centering algorithm big steps to the left to find valid data. This bit is reset when write centering starts on a new bit (DONE = 0b or BIT_CENTERED does not equal the bit being write centered).

Bits	SCOM	Field Mnemonic: Description
57	RW	SMALL_STEP_RIGHT: This bit is set when valid data is sampled when the write-centering algorithm is big stepping to the left to find valid data. When this bit is set, the write-centering algorithm small steps to the right to find the right side of the eye, the first invalid data sample. This bit is reset when write centering starts on a new bit (DONE = 0b or BIT_CENTERED does not equal the bit being write centered).
58	RW	DONE: This bit is set when invalid data is sampled when the write-centering algorithm is small stepping to the right to find the right side of the eye. When the write-centering algorithm completes successfully, this bit is set and the average of the left side and right side delay values is loaded into the DP16 Write Delay Value Register {0-23}, which corresponds to the bit being write centered. When the write-centering algorithm finds an error, this bit is set and the current delay value being used by the algorithm is loaded into the DP16 Write Delay Value Register {0-23}. The bit number being write centered is loaded into the BIT_CENTERED field when this bit is set. This bit is reset when write centering starts on a new bit (DONE = 0b or BIT_CENTERED does not equal the bit being write centered).
59:63	RO	Constant = 0b00000

Register Name	DP16 Write Centering Status 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_CNTR_STATUS1_P0_[n]
Address	800000190701103F (SCOM), +0x0400_0000_0000
Description	This register contains status information about write-centering calibrations.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:58	RO	FW_LEFT_SIDE: This field contains the delay value of the left edge of the write data eye found by the write-centering algorithm.
59:63	RO	Constant = 0b00000

Register Name	DP16 Write Centering Status 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_CNTR_STATUS1_P1_[n]
Address	800000190701143F (SCOM), +0x0400_0000_0000
Description	This register contains status information about write-centering calibrations.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:58	RO	FW_LEFT_SIDE: This field contains the delay value of the left edge of the write data eye found by the write-centering algorithm.
59:63	RO	Constant = 0b00000

Register Name	DP16 Write Centering Status 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_CNTR_STATUS1_P2_[n]
Address	800000190701183F (SCOM), +0x0400_0000_0000
Description	This register contains status information about write-centering calibrations.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:58	RO	FW_LEFT_SIDE: This field contains the delay value of the left edge of the write data eye found by the write-centering algorithm.
59:63	RO	Constant = 0b00000

Register Name	DP16 Write Centering Status 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_CNTR_STATUS1_P3_[n]
Address	8000001907011C3F (SCOM), +0x0400_0000_0000
Description	This register contains status information about write-centering calibrations.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:58	RO	FW_LEFT_SIDE: This field contains the delay value of the left edge of the write data eye found by the write-centering algorithm.
59:63	RO	Constant = 0b00000

Register Name	DP16 Write Centering Status 2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_CNTR_STATUS2_P0_[n]
Address	8000001A0701103F (SCOM), +0x0400_0000_0000
Description	This register contains status information about write-centering calibrations.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:58	RO	FW_RIGHT_SIDE: This field contains the delay value of the right edge of the write data eye found by the write-centering algorithm.
59:63	RO	Constant = 0b00000

Register Name	DP16 Write Centering Status 2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_CNTR_STATUS2_P1_[n]
Address	8000001A0701143F (SCOM), +0x0400_0000_0000
Description	This register contains status information about write-centering calibrations.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:58	RO	FW_RIGHT_SIDE: This field contains the delay value of the right edge of the write data eye found by the write-centering algorithm.
59:63	RO	Constant = 0b00000

Register Name	DP16 Write Centering Status 2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_CNTR_STATUS2_P2_[n]
Address	8000001A0701183F (SCOM), +0x0400_0000_0000
Description	This register contains status information about write-centering calibrations.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:58	RO	FW_RIGHT_SIDE: This field contains the delay value of the right edge of the write data eye found by the write-centering algorithm.
59:63	RO	Constant = 0b00000

Register Name	DP16 Write Centering Status 2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_CNTR_STATUS2_P3_[n]
Address	8000001A07011C3F (SCOM), +0x0400_0000_0000
Description	This register contains status information about write-centering calibrations.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:58	RO	FW_RIGHT_SIDE: This field contains the delay value of the right edge of the write data eye found by the write-centering algorithm.
59:63	RO	Constant = 0b00000

Register Name	DP16 Write Error 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_ERROR0_P0_[n]
Address	8000001B0701103F (SCOM), +0x0400_0000_0000
Description	This register contains the errors detected during write-calibration algorithms.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RWX_RCLRPART	WL_ERR_CLK16: Write-leveling error. This bit is set when the write-leveling algorithm cannot find a write-leveling solution for CLK 16.
49	RWX_RCLRPART	WL_ERR_CLK18: Write-leveling error. This bit is set when the write-leveling algorithm cannot find a write-leveling solution for CLK 18.
50	RWX_RCLRPART	WL_ERR_CLK20: Write-leveling error. This bit is set when the write-leveling algorithm cannot find a write-leveling solution for CLK 20.
51	RWX_RCLRPART	WL_ERR_CLK22: Write-leveling error. This bit is set when the write-leveling algorithm cannot find a write-leveling solution for CLK 22.
52	RW	COARSE_ERR_CLK16: The DQS write delay exceeded the allowable delay range maximum of 0x1FF.
53	RW	COARSE_ERR_CLK18: The DQS write delay exceeded the allowable delay range maximum of 0x1FF.
54	RW	COARSE_ERR_CLK20: The DQS write delay exceeded the allowable delay range maximum of 0x1FF.
55	RW	COARSE_ERR_CLK22: The DQS write delay exceeded the allowable delay range maximum of 0x1FF.

Bits	SCOM	Field Mnemonic: Description
56	RWX_RCLRPART	VALID_NS_BIG_L: Write-centering error. This bit is set when the write-centering algorithm did not sample valid data during big steps to the right to find the left edge of the eye.
57	RWX_RCLRPART	INVALID_NS_SMALL_L: Write-centering error/status. This bit is set when the write-centering algorithm did not sample invalid data during small steps to the left to find the left edge of the eye. This status bit does not cause the write-centering algorithm to stop. It uses the starting delay point as the left edge of the eye. This bit lane might be functional, but it might not be an optimal centering solution.
58	RWX_RCLRPART	VALID_NS_BIG_R: Write-centering error. This bit is set when the write-centering algorithm did not sample valid data during big steps to the right to find the right side of the eye.
59	RWX_RCLRPART	INVALID_NS_BIG_R: Write-centering error. This bit is set when the write-centering algorithm did not sample invalid data during big steps to the right to find the right side of the eye.
60	RWX_RCLRPART	VALID_NS_JUMP_BACK: Write-centering error. This bit is set when the write-centering algorithm did not sample valid data during big steps to the left to find the right side of the eye.
61	RWX_RCLRPART	INVALID_NS_SMALL_R: Write-centering error. This bit is set when the write-centering algorithm did not sample invalid data during small steps to the right to find the right side of the eye.
62	RWX_RCLRPART	OFFSET_ERR: Write-centering error. This bit is set when the sum of the DQ_WR_OFFSET_N* value in the DP16 Write DQ Offset Value Register and the center value determined by the write-centering algorithm is a negative number.
63	RW	Reserved.

Register Name	**DP16 Write Error 0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_WR_ERROR0_P1_[n]
Address	8000001B0701143F (SCOM), +0x0400_0000_0000
Description	This register contains the errors detected during write-calibration algorithms.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RWX_RCLRPART	WL_ERR_CLK16: Write-leveling error. This bit is set when the write-leveling algorithm cannot find a write-leveling solution for CLK 16.
49	RWX_RCLRPART	WL_ERR_CLK18: Write-leveling error. This bit is set when the write-leveling algorithm cannot find a write-leveling solution for CLK 18.
50	RWX_RCLRPART	WL_ERR_CLK20: Write-leveling error. This bit is set when the write-leveling algorithm cannot find a write-leveling solution for CLK 20.
51	RWX_RCLRPART	WL_ERR_CLK22: Write-leveling error. This bit is set when the write-leveling algorithm cannot find a write-leveling solution for CLK 22.
52	RW	COARSE_ERR_CLK16: The DQS write delay exceeded the allowable delay range maximum of 0x1FF.
53	RW	COARSE_ERR_CLK18: The DQS write delay exceeded the allowable delay range maximum of 0x1FF.
54	RW	COARSE_ERR_CLK20: The DQS write delay exceeded the allowable delay range maximum of 0x1FF.
55	RW	COARSE_ERR_CLK22: The DQS write delay exceeded the allowable delay range maximum of 0x1FF.

Bits	SCOM	Field Mnemonic: Description
56	RWX_RCLRPART	VALID_NS_BIG_L: Write-centering error. This bit is set when the write-centering algorithm did not sample valid data during big steps to the right to find the left edge of the eye.
57	RWX_RCLRPART	INVALID_NS_SMALL_L: Write-centering error/status. This bit is set when the write-centering algorithm did not sample invalid data during small steps to the left to find the left edge of the eye. This status bit does not cause the write-centering algorithm to stop. It uses the starting delay point as the left edge of the eye. This bit lane might be functional, but it might not be an optimal centering solution.
58	RWX_RCLRPART	VALID_NS_BIG_R: Write-centering error. This bit is set when the write-centering algorithm did not sample valid data during big steps to the right to find the right side of the eye.
59	RWX_RCLRPART	INVALID_NS_BIG_R: Write-centering error. This bit is set when the write-centering algorithm did not sample invalid data during big steps to the right to find the right side of the eye.
60	RWX_RCLRPART	VALID_NS_JUMP_BACK: Write-centering error. This bit is set when the write-centering algorithm did not sample valid data during big steps to the left to find the right side of the eye.
61	RWX_RCLRPART	INVALID_NS_SMALL_R: Write-centering error. This bit is set when the write-centering algorithm did not sample invalid data during small steps to the right to find the right side of the eye.
62	RWX_RCLRPART	OFFSET_ERR: Write-centering error. This bit is set when the sum of the DQ_WR_OFFSET_N* value in the DP16 Write DQ Offset Value Register and the center value determined by the write-centering algorithm is a negative number.
63	RW	Reserved.

Register Name	**DP16 Write Error 0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_WR_ERROR0_P2_[n]
Address	8000001B0701183F (SCOM), +0x0400_0000_0000
Description	This register contains the errors detected during write-calibration algorithms.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RWX_RCLRPART	WL_ERR_CLK16: Write-leveling error. This bit is set when the write-leveling algorithm cannot find a write-leveling solution for CLK 16.
49	RWX_RCLRPART	WL_ERR_CLK18: Write-leveling error. This bit is set when the write-leveling algorithm cannot find a write-leveling solution for CLK 18.
50	RWX_RCLRPART	WL_ERR_CLK20: Write-leveling error. This bit is set when the write-leveling algorithm cannot find a write-leveling solution for CLK 20.
51	RWX_RCLRPART	WL_ERR_CLK22: Write-leveling error. This bit is set when the write-leveling algorithm cannot find a write-leveling solution for CLK 22.
52	RW	COARSE_ERR_CLK16: The DQS write delay exceeded the allowable delay range maximum of 0x1FF.
53	RW	COARSE_ERR_CLK18: The DQS write delay exceeded the allowable delay range maximum of 0x1FF.
54	RW	COARSE_ERR_CLK20: The DQS write delay exceeded the allowable delay range maximum of 0x1FF.
55	RW	COARSE_ERR_CLK22: The DQS write delay exceeded the allowable delay range maximum of 0x1FF.

Bits	SCOM	Field Mnemonic: Description
56	RWX_RCLRPART	VALID_NS_BIG_L: Write-centering error. This bit is set when the write-centering algorithm did not sample valid data during big steps to the right to find the left edge of the eye.
57	RWX_RCLRPART	INVALID_NS_SMALL_L: Write-centering error/status. This bit is set when the write-centering algorithm did not sample invalid data during small steps to the left to find the left edge of the eye. This status bit does not cause the write-centering algorithm to stop. It uses the starting delay point as the left edge of the eye. This bit lane might be functional, but it might not be an optimal centering solution.
58	RWX_RCLRPART	VALID_NS_BIG_R: Write-centering error. This bit is set when the write-centering algorithm did not sample valid data during big steps to the right to find the right side of the eye.
59	RWX_RCLRPART	INVALID_NS_BIG_R: Write-centering error. This bit is set when the write-centering algorithm did not sample invalid data during big steps to the right to find the right side of the eye.
60	RWX_RCLRPART	VALID_NS_JUMP_BACK: Write-centering error. This bit is set when the write-centering Algorithm did not sample valid data during big steps to the left to find the right side of the eye.
61	RWX_RCLRPART	INVALID_NS_SMALL_R: Write-centering error. This bit is set when the write-centering algorithm did not sample invalid data during small steps to the right to find the right side of the eye.
62	RWX_RCLRPART	OFFSET_ERR: Write-centering error. This bit is set when the sum of the DQ_WR_OFFSET_N* value in the DP16 Write DQ Offset Value Register and the center value determined by the write-centering algorithm is a negative number.
63	RW	Reserved.

Register Name	**DP16 Write Error 0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_WR_ERROR0_P3_[n]
Address	8000001B07011C3F (SCOM), +0x0400_0000_0000
Description	This register contains the errors detected during write-calibration algorithms.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RWX_RCLRPART	WL_ERR_CLK16: Write-leveling error. This bit is set when the write-leveling algorithm cannot find a write-leveling solution for CLK 16.
49	RWX_RCLRPART	WL_ERR_CLK18: Write-leveling error. This bit is set when the write-leveling algorithm cannot find a write-leveling solution for CLK 18.
50	RWX_RCLRPART	WL_ERR_CLK20: Write-leveling error. This bit is set when the write-leveling algorithm cannot find a write-leveling solution for CLK 20.
51	RWX_RCLRPART	WL_ERR_CLK22: Write-leveling error. This bit is set when the write-leveling algorithm cannot find a write-leveling solution for CLK 22.
52	RW	COARSE_ERR_CLK16: The DQS write delay exceeded the allowable delay range maximum of 0x1FF.
53	RW	COARSE_ERR_CLK18: The DQS write delay exceeded the allowable delay range maximum of 0x1FF.
54	RW	COARSE_ERR_CLK20: The DQS write delay exceeded the allowable delay range maximum of 0x1FF.
55	RW	COARSE_ERR_CLK22: The DQS write delay exceeded the allowable delay range maximum of 0x1FF.

Bits	SCOM	Field Mnemonic: Description
56	RWX_RCLRPART	VALID_NS_BIG_L: Write-centering error. This bit is set when the write-centering algorithm did not sample valid data during big steps to the right to find the left edge of the eye.
57	RWX_RCLRPART	INVALID_NS_SMALL_L: Write-centering error/status. This bit is set when the write-centering algorithm did not sample invalid data during small steps to the left to find the left edge of the eye. This status bit does not cause the write-centering algorithm to stop. It uses the starting delay point as the left edge of the eye. This bit lane might be functional, but it might not be an optimal centering solution.
58	RWX_RCLRPART	VALID_NS_BIG_R: Write-centering error. This bit is set when the write-centering algorithm did not sample valid data during big steps to the right to find the right side of the eye.
59	RWX_RCLRPART	INVALID_NS_BIG_R: Write-centering error. This bit is set when the write-centering algorithm did not sample invalid data during big steps to the right to find the right side of the eye.
60	RWX_RCLRPART	VALID_NS_JUMP_BACK: Write-centering error. This bit is set when the write-centering algorithm did not sample valid data during big steps to the left to find the right side of the eye.
61	RWX_RCLRPART	INVALID_NS_SMALL_R: Write-centering error. This bit is set when the write-centering algorithm did not sample invalid data during small steps to the right to find the right side of the eye.
62	RWX_RCLRPART	OFFSET_ERR: Write-centering error. This bit is set when the sum of the DQ_WR_OFFSET_N* value in the DP16 Write DQ Offset Value Register and the center value determined by the write-centering algorithm is a negative number.
63	RW	Reserved.

Register Name	**DP16 Write Error Mask 0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_WR_ERROR_MASK0_P0_[n]
Address	8000001C0701103F (SCOM), +0x0400_0000_0000
Description	This register masks errors in the DP16 Write Error 0 Register. Thus, it prevents the WR_CNTL_ERROR bit from being set in the WC Error Status 0 Register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	RW	WL_ERR_CLK16_MASK: 1 = Mask the WL_ERR_CLK16 error.
49	RW	WL_ERR_CLK18_MASK: 1 = Mask the WL_ERR_CLK18 error.
50	RW	WL_ERR_CLK20_MASK: 1 = Mask the WL_ERR_CLK20 error.
51	RW	WR_ERR_CLK22_MASK: 1 = Mask the WL_ERR_CLK22 error.
52:55	RW	Reserved.
56	RW	VALID_NS_BIG_L_MASK: 1 = Mask the VALID_NS_BIG_L error.
57	RW	INVALID_NS_SMALL_L_MASK: 1 = Mask the INVALID_NS_SMALL_L error.

Bits	SCOM	Field Mnemonic: Description
58	RW	VALID_NS_BIG_R_MASK: 1 = Mask the VALID_NS_BIG_R error.
59	RW	INVALID_NS_BIG_R_MASK: 1 = Mask the INVALID_NS_BIG_R error.
60	RW	VALID_NS_JUMP_BACK_MASK: 1 = Mask the VALID_NS_JUMP_BACK error.
61	RW	INVALID_NS_SMALL_R_MASK: 1 = Mask the INVALID_NS_SMALL_R error.
62	RW	OFFSET_ERR_MASK: 1 = Mask the OFFSET_ERR error.
63	RW	ADVANCE_PR_VALUE: Advance phase-rotator value control switch. 0 = Normal operation. 1 = Change the phase-rotator values going to the analog core 1 SysClk clock cycle earlier on pins 0 – 15, inclusive. This provides more settling and propagation time of the phase rotator values before output enable (OE), even data (EDAT), and odd data (ODAT) values are driven to the analog core.

Register Name	DP16 Write Error Mask 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_ERROR_MASK0_P1_[n]
Address	8000001C0701143F (SCOM), +0x0400_0000_0000
Description	This register masks errors in the DP16 Write Error 0 Register. Thus, it prevents the WR_CNTL_ERROR bit from being set in the WC Error Status 0 Register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	WL_ERR_CLK16_MASK: 1 = Mask the WL_ERR_CLK16 error.
49	RW	WL_ERR_CLK18_MASK: 1 = Mask the WL_ERR_CLK18 error.
50	RW	WL_ERR_CLK20_MASK: 1 = Mask the WL_ERR_CLK20 error.
51	RW	WR_ERR_CLK22_MASK: 1 = Mask the WL_ERR_CLK22 error.
52:55	RW	Reserved.
56	RW	VALID_NS_BIG_L_MASK: 1 = Mask the VALID_NS_BIG_L error.
57	RW	INVALID_NS_SMALL_L_MASK: 1 = Mask the INVALID_NS_SMALL_L error.
58	RW	VALID_NS_BIG_R_MASK: 1 = Mask the VALID_NS_BIG_R error.
59	RW	INVALID_NS_BIG_R_MASK: 1 = Mask the INVALID_NS_BIG_R error.
60	RW	VALID_NS_JUMP_BACK_MASK: 1 = Mask the VALID_NS_JUMP_BACK error.
61	RW	INVALID_NS_SMALL_R_MASK: 1 = Mask the INVALID_NS_SMALL_R error.

Bits	SCOM	Field Mnemonic: Description
62	RW	OFFSET_ERR_MASK: 1 = Mask the OFFSET_ERR error.
63	RW	ADVANCE_PR_VALUE: Advance phase-rotator value control switch. 0 = Normal operation. 1 = Change the phase-rotator values going to the analog core 1 SysClk clock cycle earlier on pins 0 – 15, inclusive. This provides more settling and propagation time of the phase rotator values before OE, EDAT, and ODAT values are driven to the analog core.

Register Name	**DP16 Write Error Mask 0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_WR_ERROR_MASK0_P2_[n]
Address	8000001C0701183F (SCOM), +0x0400_0000_0000
Description	This register masks errors in the DP16 Write Error 0 Register. Thus, it prevents the WR_CNTL_ERROR bit from being set in the WC Error Status 0 Register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	WL_ERR_CLK16_MASK: 1 = Mask the WL_ERR_CLK16 error.
49	RW	WL_ERR_CLK18_MASK: 1 = Mask the WL_ERR_CLK18 error.
50	RW	WL_ERR_CLK20_MASK: 1 = Mask the WL_ERR_CLK20 error.
51	RW	WR_ERR_CLK22_MASK: 1 = Mask the WL_ERR_CLK22 error.
52:55	RW	Reserved.
56	RW	VALID_NS_BIG_L_MASK: 1 = Mask the VALID_NS_BIG_L error.
57	RW	INVALID_NS_SMALL_L_MASK: 1 = Mask the INVALID_NS_SMALL_L error.
58	RW	VALID_NS_BIG_R_MASK: 1 = Mask the VALID_NS_BIG_R error.
59	RW	INVALID_NS_BIG_R_MASK: 1 = Mask the INVALID_NS_BIG_R error.
60	RW	VALID_NS_JUMP_BACK_MASK: 1 = Mask the VALID_NS_JUMP_BACK error.
61	RW	INVALID_NS_SMALL_R_MASK: 1 = Mask the INVALID_NS_SMALL_R error.
62	RW	OFFSET_ERR_MASK: 1 = Mask the OFFSET_ERR error.
63	RW	ADVANCE_PR_VALUE: Advance phase-rotator value control switch. 0 = Normal operation. 1 = Change the phase-rotator values going to the analog core 1 SysClk clock cycle earlier on pins 0 – 15, inclusive. This provides more settling and propagation time of the phase rotator values before OE, EDAT, and ODAT values are driven to the analog core.

Register Name	DP16 Write Error Mask 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_ERROR_MASK0_P3_[n]
Address	8000001C07011C3F (SCOM), +0x0400_0000_0000
Description	This register masks errors in the DP16 Write Error 0 Register. Thus, it prevents the WR_CNTL_ERROR bit from being set in the WC Error Status 0 Register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	WL_ERR_CLK16_MASK: 1 = Mask the WL_ERR_CLK16 error.
49	RW	WL_ERR_CLK18_MASK: 1 = Mask the WL_ERR_CLK18 error.
50	RW	WL_ERR_CLK20_MASK: 1 = Mask the WL_ERR_CLK20 error.
51	RW	WR_ERR_CLK22_MASK: 1 = Mask the WL_ERR_CLK22 error.
52:55	RW	Reserved.
56	RW	VALID_NS_BIG_L_MASK: 1 = Mask the VALID_NS_BIG_L error.
57	RW	INVALID_NS_SMALL_L_MASK: 1 = Mask the INVALID_NS_SMALL_L error.
58	RW	VALID_NS_BIG_R_MASK: 1 = Mask the VALID_NS_BIG_R error.
59	RW	INVALID_NS_BIG_R_MASK: 1 = Mask the INVALID_NS_BIG_R error.
60	RW	VALID_NS_JUMP_BACK_MASK: 1 = Mask the VALID_NS_JUMP_BACK error.
61	RW	INVALID_NS_SMALL_R_MASK: 1 = Mask the INVALID_NS_SMALL_R error.
62	RW	OFFSET_ERR_MASK: 1 = Mask the OFFSET_ERR error.
63	RW	ADVANCE_PR_VALUE: Advance phase-rotator value control switch. 0 = Normal operation. 1 = Change the phase-rotator values going to the analog core 1 SysClk clock cycle earlier on pins 0 – 15, inclusive. This provides more settling and propagation time of the phase rotator values before OE, EDAT, and ODAT values are driven to the analog core.

Register Name	DP16 DFT Wrap Status Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DFT_WRAP_STATUS_P0_[n]
Address	8000001D0701103F (SCOM), +0x0400_0000_0000
Description	This register provides the status of the DP16 wrap test. This register must be used only to perform diagnostic, manufacturing, or characterization testing. Contact your IBM representative before modifying this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	CHECKER_ENABLE: Writing this bit to a 1 enables the pseudo-random binary sequence (PRBS) checker function.
49	RWX	CHECKER_RESET: Writing this bit to a 1 causes the SYNC and ERROR fields to clear to zero, and this field self clears.
50:51	RO	Constant = 0b00
52:55	ROX	SYNC: Each bit of this field is set during wrap testing when the PRBS7 pattern is detected on the corresponding receive bit. The bits are tested in the following groups: Bit 52 = MEMINTD00B MEMINTD04B MEMINTD08B MEMINTD12B. Bit 53 = MEMINTD01B MEMINTD05B MEMINTD09B MEMINTD13B. Bit 54 = MEMINTD02B MEMINTD06B MEMINTD10B MEMINTD14B. Bit 55 = MEMINTD03B MEMINTD07B MEMINTD11B MEMINTD15B.
56:57	RO	Reserved.
58:61	ROX	ERROR: Each bit of this field is set during wrap testing when the corresponding SYNC bit has been set, but a subsequent received data bit does not match the PRBS7 pattern.
62:63	RO	Reserved.

Register Name	DP16 DFT Wrap Status Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DFT_WRAP_STATUS_P1_[n]
Address	8000001D0701143F (SCOM), +0x0400_0000_0000
Description	This register provides the status of the DP16 wrap test. This register must be used only to perform diagnostic, manufacturing, or characterization testing. Contact your IBM representative before modifying this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RWX	CHECKER_ENABLE: Writing this bit to a 1 enables the PRBS checker function.
49	RWX	CHECKER_RESET: Writing this bit to a 1 causes the SYNC and ERROR fields to clear to zero, and this field self clears.
50:51	RO	Constant = 0b00
52:55	ROX	SYNC: Each bit of this field is set during wrap testing when the PRBS7 pattern is detected on the corresponding receive bit. The bits are tested in the following groups: Bit 52 = MEMINTD00B MEMINTD04B MEMINTD08B MEMINTD12B. Bit 53 = MEMINTD01B MEMINTD05B MEMINTD09B MEMINTD13B. Bit 54 = MEMINTD02B MEMINTD06B MEMINTD10B MEMINTD14B. Bit 55 = MEMINTD03B MEMINTD07B MEMINTD11B MEMINTD15B.
56:57	RO	Reserved.
58:61	ROX	ERROR: Each bit of this field is set during wrap testing when the corresponding SYNC bit has been set, but a subsequent received data bit does not match the PRBS7 pattern.
62:63	RO	Reserved.

Register Name	DP16 DFT Wrap Status Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DFT_WRAP_STATUS_P2_[n]
Address	8000001D0701183F (SCOM), +0x0400_0000_0000
Description	This register provides the status of the DP16 wrap test. This register must be used only to perform diagnostic, manufacturing, or characterization testing. Contact your IBM representative before modifying this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RWX	CHECKER_ENABLE: Writing this bit to a 1 enables the PRBS checker function.
49	RWX	CHECKER_RESET: Writing this bit to a 1 causes the SYNC and ERROR fields to clear to zero, and this field self clears.
50:51	RO	Constant = 0b00
52:55	ROX	SYNC: Each bit of this field is set during wrap testing when the PRBS7 pattern is detected on the corresponding receive bit. The bits are tested in the following groups: Bit 52 = MEMINTD00B MEMINTD04B MEMINTD08B MEMINTD12B. Bit 53 = MEMINTD01B MEMINTD05B MEMINTD09B MEMINTD13B. Bit 54 = MEMINTD02B MEMINTD06B MEMINTD10B MEMINTD14B. Bit 55 = MEMINTD03B MEMINTD07B MEMINTD11B MEMINTD15B.
56:57	RO	Reserved.
58:61	ROX	ERROR: Each bit of this field is set during wrap testing when the corresponding SYNC bit has been set, but a subsequent received data bit does not match the PRBS7 pattern.
62:63	RO	Reserved.

Register Name	DP16 DFT Wrap Status Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DFT_WRAP_STATUS_P3_[n]
Address	8000001D07011C3F (SCOM), +0x0400_0000_0000
Description	This register provides the status of the DP16 wrap test. This register must be used only to perform diagnostic, manufacturing, or characterization testing. Contact your IBM representative before modifying this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RWX	CHECKER_ENABLE: Writing this bit to a 1 enables the PRBS checker function.
49	RWX	CHECKER_RESET: Writing this bit to a 1 causes the SYNC and ERROR fields to clear to zero, and this field self clears.
50:51	RO	Constant = 0b00
52:55	ROX	SYNC: Each bit of this field is set during wrap testing when the PRBS7 pattern is detected on the corresponding receive bit. The bits are tested in the following groups: Bit 52 = MEMINTD00B MEMINTD04B MEMINTD08B MEMINTD12B. Bit 53 = MEMINTD01B MEMINTD05B MEMINTD09B MEMINTD13B. Bit 54 = MEMINTD02B MEMINTD06B MEMINTD10B MEMINTD14B. Bit 55 = MEMINTD03B MEMINTD07B MEMINTD11B MEMINTD15B.
56:57	RO	Reserved.
58:61	ROX	ERROR: Each bit of this field is set during wrap testing when the corresponding SYNC bit has been set, but a subsequent received data bit does not match the PRBS7 pattern.
62:63	RO	Reserved.

Register Name	DP16 Read Diagnostic Configuration 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_DIA_CONFIG0_P0_[n]
Address	8000001E0701103F (SCOM), +0x0400_0000_0000
Description	This register is used for the diagnosis and characterization of the read function within the DP16. For correct functional mainline operation, this register must not be written. Contact your IBM representative before changing the value of this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	SYSCLK_DQSCLK_OFFSET: Contact your IBM representative.
56	RW	Reserved.
57:63	RW	SYSCLK_RDCLK_OFFSET: Contact your IBM representative.

Register Name	DP16 Read Diagnostic Configuration 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_DIA_CONFIG0_P1_[n]
Address	8000001E0701143F (SCOM), +0x0400_0000_0000
Description	This register is used for the diagnosis and characterization of the read function within the DP16. For correct functional mainline operation, this register must not be written. Contact your IBM representative before changing the value of this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	SYSCLK_DQSCLK_OFFSET: Contact your IBM representative.
56	RW	Reserved.
57:63	RW	SYSCLK_RDCLK_OFFSET: Contact your IBM representative.

Register Name	DP16 Read Diagnostic Configuration 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_DIA_CONFIG0_P2_[n]
Address	8000001E0701183F (SCOM), +0x0400_0000_0000
Description	This register is used for the diagnosis and characterization of the read function within the DP16. For correct functional mainline operation, this register must not be written. Contact your IBM representative before changing the value of this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	SYSCLK_DQSCLK_OFFSET: Contact your IBM representative.
56	RW	Reserved.
57:63	RW	SYSCLK_RDCLK_OFFSET: Contact your IBM representative.

Register Name	DP16 Read Diagnostic Configuration 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_DIA_CONFIG0_P3_[n]
Address	8000001E07011C3F (SCOM), +0x0400_0000_0000
Description	This register is used for the diagnosis and characterization of the read function within the DP16. For correct functional mainline operation, this register must not be written. Contact your IBM representative before changing the value of this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	SYSCLK_DQSCLK_OFFSET: Contact your IBM representative.
56	RW	Reserved.
57:63	RW	SYSCLK_RDCLK_OFFSET: Contact your IBM representative.

Register Name	DP16 Read VREF DAC 1 Register[n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_DAC_1_P0_[n]
Address	8000001F0701103F (SCOM), +0x0400_0000_0000
Description	This register controls the DAC settings of the read VREF in the DP16 unit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RWX	NIB2_EN_FORCE: This bit overrides the logic enabling the comparator in the analog DACs for nibble 2 (bits 8:11 of 0:15) to set them to the value specified in the DP16 Read VREF DAC Comparator Ouptut Register. The binary string sent to the DAC is the value in BIT2_VREF_DAC. This allows the user to manually set the enable bits and DAC value for each nibble. The output of the comparator is captured in the DP16 Read VREF DAC Comparator Output Register. While read VREF calibration is running, this bit has no effect.
49:55	RWX	BIT2_VREF_DAC: DAC setting to control VREF on bit 2 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field reverts to the average of nibble 2.
56	RWX	NIB3_EN_FORCE: This bit overrides the logic enabling the comparator in the analog DACs for nibble 3 (bits 12:15 of 0:15) to set them to the value specified in the DP16 Read VREF DAC Comparator Ouptut Register. The binary string sent to the DAC is the value in BIT3_VREF_DAC. This allows the user to manually set the enable bits and DAC value for each nibble. The output of the comparator is captured in the DP16 Read VREF DAC Comparator Output Register. While read VREF calibration is running, this bit has no effect.
57:63	RWX	BIT3_VREF_DAC: DAC setting to control VREF on bit 3 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field reverts to the average of nibble 3.

Register Name	DP16 Read VREF DAC 1 Register[n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_DAC_1_P1_[n]
Address	8000001F0701143F (SCOM), +0x0400_0000_0000
Description	This register controls the DAC settings of the read VREF in the DP16 unit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RWX	NIB2_EN_FORCE: This bit overrides the logic enabling the comparator in the analog DACs for nibble 2 (bits 8:11 of 0:15) to set them to the value specified in the DP16 Read VREF DAC Comparator Ouptut Register. The binary string sent to the DAC is the value in BIT2_VREF_DAC. This allows the user to manually set the enable bits and DAC value for each nibble. The output of the comparator is captured in the DP16 Read VREF DAC Comparator Output Register. While read VREF calibration is running, this bit has no effect.
49:55	RWX	BIT2_VREF_DAC: DAC setting to control VREF on bit 2 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field reverts to the average of nibble 2.
56	RWX	NIB3_EN_FORCE: This bit overrides the logic enabling the comparator in the analog DACs for nibble 3 (bits 12:15 of 0:15) to set them to the value specified in the DP16 Read VREF DAC Comparator Ouptut Register. The binary string sent to the DAC is the value in BIT3_VREF_DAC. This allows the user to manually set the enable bits and DAC value for each nibble. The output of the comparator is captured in the DP16 Read VREF DAC Comparator Output Register. While read VREF calibration is running, this bit has no effect.
57:63	RWX	BIT3_VREF_DAC: DAC setting to control VREF on bit 3 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field reverts to the average of nibble 3.

Register Name	**DP16 Read VREF DAC 1 Register[n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_DAC_1_P2_[n]
Address	8000001F0701183F (SCOM), +0x0400_0000_0000
Description	This register controls the DAC settings of the read VREF in the DP16 unit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RWX	NIB2_EN_FORCE: This bit overrides the logic enabling the comparator in the analog DACs for nibble 2 (bits 8:11 of 0:15) to set them to the value specified in the DP16 Read VREF DAC Comparator Ouptut Register. The binary string sent to the DAC is the value in BIT2_VREF_DAC. This allows the user to manually set the enable bits and DAC value for each nibble. The output of the comparator is captured in the DP16 Read VREF DAC Comparator Output Register. While read VREF calibration is running, this bit has no effect.
49:55	RWX	BIT2_VREF_DAC: DAC setting to control VREF on bit 2 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field reverts to the average of nibble 2.
56	RWX	NIB3_EN_FORCE: This bit overrides the logic enabling the comparator in the analog DACs for nibble 3 (bits 12:15 of 0:15) to set them to the value specified in the DP16 Read VREF DAC Comparator Ouptut Register. The binary string sent to the DAC is the value in BIT3_VREF_DAC. This allows the user to manually set the enable bits and DAC value for each nibble. The output of the comparator is captured in the DP16 Read VREF DAC Comparator Output Register. While read VREF calibration is running, this bit has no effect.
57:63	RWX	BIT3_VREF_DAC: DAC setting to control VREF on bit 3 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field reverts to the average of nibble 3.

Register Name	DP16 Read VREF DAC 1 Register[n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_DAC_1_P3_[n]
Address	8000001F07011C3F (SCOM), +0x0400_0000_0000
Description	This register controls the DAC settings of the read VREF in the DP16 unit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RWX	NIB2_EN_FORCE: This bit overrides the logic enabling the comparator in the analog DACs for nibble 2 (bits 8:11 of 0:15) to set them to the value specified in the DP16 Read VREF DAC Comparator Ouptut Register. The binary string sent to the DAC is the value in BIT2_VREF_DAC. This allows the user to manually set the enable bits and DAC value for each nibble. The output of the comparator is captured in the DP16 Read VREF DAC Comparator Output Register. While read VREF calibration is running, this bit has no effect.
49:55	RWX	BIT2_VREF_DAC: DAC setting to control VREF on bit 2 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field reverts to the average of nibble 2.
56	RWX	NIB3_EN_FORCE: This bit overrides the logic enabling the comparator in the analog DACs for nibble 3 (bits 12:15 of 0:15) to set them to the value specified in the DP16 Read VREF DAC Comparator Ouptut Register. The binary string sent to the DAC is the value in BIT3_VREF_DAC. This allows the user to manually set the enable bits and DAC value for each nibble. The output of the comparator is captured in the DP16 Read VREF DAC Comparator Output Register. While read VREF calibration is running, this bit has no effect.
57:63	RWX	BIT3_VREF_DAC: DAC setting to control VREF on bit 3 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field reverts to the average of nibble 3.

Register Name	DP16 CTLE Control Byte 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_CTLE_CTL_BYTE0_P0_[n]
Address	800000200701103F (SCOM), +0x0400_0000_0000
Description	These registers are used to control continuous time linear equalization (CTLE) on the DQ data bits. This is a new function for POWER9.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:49	RW	NIB_0_DQSEL_CAP: This field sets the capacitance value in the read control (RC) source degeneration, which defines the zero in the CTLEs transfer characteristic together with *_DQSEL_RES. The value is binary encoded. Higher values add more capacitance. 00 = No capacitor is selected. 01 to 10 = An increasing number of capacitors are selected. 11 = The maximum number of capacitors is selected.
50:52	RW	NIB{0,2}_BIAS_TRIM: This field sets the bias current in the CTLE circuit. 000 = Nominal current.
53:55	RW	NIB_0_DQSEL_RES: This field sets the resistance value in the RC source degeneration, which defines the zero in the CTLEs transfer characteristic together with *_DQSEL_CAP. In addition to setting the zero in the transfer characteristic, this also defines the CTLEs DC gain. The value is binary coded. Higher values decrease resistance. 000 = Maximum resistance; only a fixed resistor is used. 001 to 110 = Decreasing resistance. 111 = Minimum resistance.

Bits	SCOM	Field Mnemonic: Description
56:57	RW	NIB_1_DQSEL_CAP: This field sets the capacitance value in the RC source degeneration, which defines the zero in the CTLEs transfer characteristic together with *_DQSEL_RES. The value is binary encoded. Higher values add more capacitance. 00 = No capacitor is selected. 01 to 10 = An increasing number of capacitors are selected. 11 = The maximum number of capacitors is selected.
58:60	RW	NIB{1,3}_BIAS_TRIM: This field sets the bias current in the CTLE circuit. 000 = Nominal current.
61:63	RW	NIB_1_DQSEL_RES: This field sets the resistance value in the RC source degeneration, which defines the zero in the CTLEs transfer characteristic together with *_DQSEL_CAP. In addition to setting the zero in the transfer characteristic, this also defines the CTLEs DC gain. The value is binary coded. Higher values decrease resistance. 000 = Maximum resistance; only a fixed resistor is used. 001 to 110 = Decreasing resistance. 111 = Minimum resistance.

Register Name	DP16 CTLE Control Byte 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_CTLE_CTL_BYTE0_P1_[n]
Address	800000200701143F (SCOM), +0x0400_0000_0000
Description	These registers are used to control continuous time linear equalization (CTLE) on the DQ data bits. This is a new function for POWER9.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:49	RW	NIB_0_DQSEL_CAP: This field sets the capacitance value in the RC source degeneration, which defines the zero in the CTLEs transfer characteristic together with *_DQSEL_RES. The value is binary encoded. Higher values add more capacitance. 00 = No capacitor is selected. 01 to 10 = An increasing number of capacitors are selected. 11 = The maximum number of capacitors is selected.
50:52	RW	NIB{0,2}_BIAS_TRIM: This field sets the bias current in the CTLE circuit. 000 = Nominal current.
53:55	RW	NIB_0_DQSEL_RES: This field sets the resistance value in the RC source degeneration, which defines the zero in the CTLEs transfer characteristic together with *_DQSEL_CAP. In addition to setting the zero in the transfer characteristic, this also defines the CTLEs DC gain. The value is binary coded. Higher values decrease resistance. 000 = Maximum resistance; only a fixed resistor is used. 001 to 110 = Decreasing resistance. 111 = Minimum resistance.
56:57	RW	NIB_1_DQSEL_CAP: This field sets the capacitance value in the RC source degeneration, which defines the zero in the CTLEs transfer characteristic together with *_DQSEL_RES. The value is binary encoded. Higher values add more capacitance. 00 = No capacitor is selected. 01 to 10 = An increasing number of capacitors are selected. 11 = The maximum number of capacitors is selected.
58:60	RW	NIB{1,3}_BIAS_TRIM: This field sets the bias current in the CTLE circuit. 000 = Nominal current.

Bits	SCOM	Field Mnemonic: Description
61:63	RW	NIB_1_DQSEL_RES: This field sets the resistance value in the RC source degeneration, which defines the zero in the CTLEs transfer characteristic together with *_DQSEL_CAP. In addition to setting the zero in the transfer characteristic, this also defines the CTLEs DC gain. The value is binary coded. Higher values decrease resistance. 000 = Maximum resistance; only a fixed resistor is used. 001 to 110 = Decreasing resistance. 111 = Minimum resistance.

Register Name	DP16 CTLE Control Byte 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_CTLE_CTL_BYTE0_P2_[n]
Address	800000200701183F (SCOM), +0x0400_0000_0000
Description	These registers are used to control continuous time linear equalization (CTLE) on the DQ data bits. This is a new function for POWER9.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:49	RW	NIB_0_DQSEL_CAP: This field sets the capacitance value in the RC source degeneration, which defines the zero in the CTLEs transfer characteristic together with *_DQSEL_RES. The value is binary encoded. Higher values add more capacitance. 00 = No capacitor is selected. 01 to 10 = An increasing number of capacitors are selected. 11 = The maximum number of capacitors is selected.
50:52	RW	NIB{0,2}_BIAS_TRIM: This field sets the bias current in the CTLE circuit. 000 = Nominal current.
53:55	RW	NIB_0_DQSEL_RES: This field sets the resistance value in the RC source degeneration, which defines the zero in the CTLEs transfer characteristic together with *_DQSEL_CAP. In addition to setting the zero in the transfer characteristic, this also defines the CTLEs DC gain. The value is binary coded. Higher values decrease resistance. 000 = Maximum resistance; only a fixed resistor is used. 001 to 110 = Decreasing resistance. 111 = Minimum resistance.
56:57	RW	NIB_1_DQSEL_CAP: This field sets the capacitance value in the RC source degeneration, which defines the zero in the CTLEs transfer characteristic together with *_DQSEL_RES. The value is binary encoded. Higher values add more capacitance. 00 = No capacitor is selected. 01 to 10 = An increasing number of capacitors are selected. 11 = The maximum number of capacitors is selected.
58:60	RW	NIB{1,3}_BIAS_TRIM: This field sets the bias current in the CTLE circuit. 000 = Nominal current.
61:63	RW	NIB_1_DQSEL_RES: This field sets the resistance value in the RC source degeneration, which defines the zero in the CTLEs transfer characteristic together with *_DQSEL_CAP. In addition to setting the zero in the transfer characteristic, this also defines the CTLEs DC gain. The value is binary coded. Higher values decrease resistance. 000 = Maximum resistance; only a fixed resistor is used. 001 to 110 = Decreasing resistance. 111 = Minimum resistance.

Register Name	DP16 CTLE Control Byte 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_CTLE_CTL_BYTE0_P3_[n]
Address	8000002007011C3F (SCOM), +0x0400_0000_0000
Description	These registers are used to control continuous time linear equalization (CTLE) on the DQ data bits. This is a new function for POWER9.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:49	RW	NIB_0_DQSEL_CAP: This field sets the capacitance value in the RC source degeneration, which defines the zero in the CTLEs transfer characteristic together with *_DQSEL_RES. The value is binary encoded. Higher values add more capacitance. 00 = No capacitor is selected. 01 to 10 = An increasing number of capacitors are selected. 11 = The maximum number of capacitors is selected.
50:52	RW	NIB{0,2}_BIAS_TRIM: This field sets the bias current in the CTLE circuit. 000 = Nominal current.
53:55	RW	NIB_0_DQSEL_RES: This field sets the resistance value in the RC source degeneration, which defines the zero in the CTLEs transfer characteristic together with *_DQSEL_CAP. In addition to setting the zero in the transfer characteristic, this also defines the CTLEs DC gain. The value is binary coded. Higher values decrease resistance. 000 = Maximum resistance; only a fixed resistor is used. 001 to 110 = Decreasing resistance. 111 = Minimum resistance.
56:57	RW	NIB_1_DQSEL_CAP: This field sets the capacitance value in the RC source degeneration, which defines the zero in the CTLEs transfer characteristic together with *_DQSEL_RES. The value is binary encoded. Higher values add more capacitance. 00 = No capacitor is selected. 01 to 10 = An increasing number of capacitors are selected. 11 = The maximum number of capacitors is selected.
58:60	RW	NIB{1,3}_BIAS_TRIM: This field sets the bias current in the CTLE circuit. 000 = Nominal current.
61:63	RW	NIB_1_DQSEL_RES: This field sets the resistance value in the RC source degeneration, which defines the zero in the CTLEs transfer characteristic together with *_DQSEL_CAP. In addition to setting the zero in the transfer characteristic, this also defines the CTLEs DC gain. The value is binary coded. Higher values decrease resistance. 000 = Maximum resistance; only a fixed resistor is used. 001 to 110 = Decreasing resistance. 111 = Minimum resistance.

Register Name	DP16 CTLE Control Byte 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_CTLE_CTL_BYTE1_P0_[n]
Address	800000210701103F (SCOM), +0x0400_0000_0000
Description	These registers are used to control continuous time linear equalization (CTLE) on the DQ data bits. This is a new function for POWER9.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RW	NIB_2_DQSEL_CAP: This field sets the capacitance value in the RC source degeneration, which defines the zero in the CTLEs transfer characteristic together with *_DQSEL_RES. The value is binary encoded. Higher values add more capacitance. 00 = No capacitor is selected. 01 to 10 = An increasing number of capacitors are selected. 11 = The maximum number of capacitors is selected.
50:52	RW	NIB{0,2}_BIAS_TRIM: This field sets the bias current in the CTLE circuit. 000 = Nominal current.
53:55	RW	NIB_2_DQSEL_RES: This field sets the resistance value in the RC source degeneration, which defines the zero in the CTLEs transfer characteristic together with *_DQSEL_CAP. In addition to setting the zero in the transfer characteristic, this also defines the CTLEs DC gain. The value is binary coded. Higher values decrease resistance. 000 = Maximum resistance; only a fixed resistor is used. 001 to 110 = Decreasing resistance. 111 = Minimum resistance.
56:57	RW	NIB_3_DQSEL_CAP: This field sets the capacitance value in the RC source degeneration, which defines the zero in the CTLEs transfer characteristic together with *_DQSEL_RES. The value is binary encoded. Higher values add more capacitance. 00 = No capacitor is selected. 01 to 10 = An increasing number of capacitors are selected. 11 = The maximum number of capacitors is selected.
58:60	RW	NIB{1,3}_BIAS_TRIM: This field sets the bias current in the CTLE circuit. 000 = Nominal current.
61:63	RW	NIB_3_DQSEL_RES: This field sets the resistance value in the RC source degeneration, which defines the zero in the CTLEs transfer characteristic together with *_DQSEL_CAP. In addition to setting the zero in the transfer characteristic, this also defines the CTLEs DC gain. The value is binary coded. Higher values decrease resistance. 000 = Maximum resistance; only a fixed resistor is used. 001 to 110 = Decreasing resistance. 111 = Minimum resistance.

Register Name	DP16 CTLE Control Byte 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_CTLE_CTL_BYTE1_P1_[n]
Address	800000210701143F (SCOM), +0x0400_0000_0000
Description	These registers are used to control continuous time linear equalization (CTLE) on the DQ data bits. This is a new function for POWER9.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:49	RW	NIB_2_DQSEL_CAP: This field sets the capacitance value in the RC source degeneration, which defines the zero in the CTLEs transfer characteristic together with *_DQSEL_RES. The value is binary encoded. Higher values add more capacitance. 00 = No capacitor is selected. 01 to 10 = An increasing number of capacitors are selected. 11 = The maximum number of capacitors is selected.
50:52	RW	NIB{0,2}_BIAS_TRIM: This field sets the bias current in the CTLE circuit. 000 = Nominal current.

Bits	SCOM	Field Mnemonic: Description
53:55	RW	NIB_2_DQSEL_RES: This field sets the resistance value in the RC source degeneration, which defines the zero in the CTLEs transfer characteristic together with *_DQSEL_CAP. In addition to setting the zero in the transfer characteristic, this also defines the CTLEs DC gain. The value is binary coded. Higher values decrease resistance. 000 = Maximum resistance; only a fixed resistor is used. 001 to 110 = Decreasing resistance. 111 = Minimum resistance.
56:57	RW	NIB_3_DQSEL_CAP: This field sets the capacitance value in the RC source degeneration, which defines the zero in the CTLEs transfer characteristic together with *_DQSEL_RES. The value is binary encoded. Higher values add more capacitance. 00 = No capacitor is selected. 01 to 10 = An increasing number of capacitors are selected. 11 = The maximum number of capacitors is selected.
58:60	RW	NIB{1,3}_BIAS_TRIM: This field sets the bias current in the CTLE circuit. 000 = Nominal current.
61:63	RW	NIB_3_DQSEL_RES: This field sets the resistance value in the RC source degeneration, which defines the zero in the CTLEs transfer characteristic together with *_DQSEL_CAP. In addition to setting the zero in the transfer characteristic, this also defines the CTLEs DC gain. The value is binary coded. Higher values decrease resistance. 000 = Maximum resistance; only a fixed resistor is used. 001 to 110 = Decreasing resistance. 111 = Minimum resistance.

Register Name	**DP16 CTLE Control Byte 1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_CTLE_CTL_BYTE1_P2_[n]
Address	800000210701183F (SCOM), +0x0400_0000_0000
Description	These registers are used to control continuous time linear equalization (CTLE) on the DQ data bits. This is a new function for POWER9.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:49	RW	NIB_2_DQSEL_CAP: This field sets the capacitance value in the RC source degeneration, which defines the zero in the CTLEs transfer characteristic together with *_DQSEL_RES. The value is binary encoded. Higher values add more capacitance. 00 = No capacitor is selected. 01 to 10 = An increasing number of capacitors are selected. 11 = The maximum number of capacitors is selected.
50:52	RW	NIB{0,2}_BIAS_TRIM: This field sets the bias current in the CTLE circuit. 000 = Nominal current.
53:55	RW	NIB_2_DQSEL_RES: This field sets the resistance value in the RC source degeneration, which defines the zero in the CTLEs transfer characteristic together with *_DQSEL_CAP. In addition to setting the zero in the transfer characteristic, this also defines the CTLEs DC gain. The value is binary coded. Higher values decrease resistance. 000 = Maximum resistance; only a fixed resistor is used. 001 to 110 = Decreasing resistance. 111 = Minimum resistance.
56:57	RW	NIB_3_DQSEL_CAP: This field sets the capacitance value in the RC source degeneration, which defines the zero in the CTLEs transfer characteristic together with *_DQSEL_RES. The value is binary encoded. Higher values add more capacitance. 00 = No capacitor is selected. 01 to 10 = An increasing number of capacitors are selected. 11 = The maximum number of capacitors is selected.

Bits	SCOM	Field Mnemonic: Description
58:60	RW	NIB{1,3}_BIAS_TRIM: This field sets the bias current in the CTLE circuit. 000 = Nominal current.
61:63	RW	NIB_3_DQSEL_RES: This field sets the resistance value in the RC source degeneration, which defines the zero in the CTLEs transfer characteristic together with *_DQSEL_CAP. In addition to setting the zero in the transfer characteristic, this also defines the CTLEs DC gain. The value is binary coded. Higher values decrease resistance. 000 = Maximum resistance; only a fixed resistor is used. 001 to 110 = Decreasing resistance. 111 = Minimum resistance.

Register Name	**DP16 CTLE Control Byte 1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_CTLE_CTL_BYTE1_P3_[n]
Address	8000002107011C3F (SCOM), +0x0400_0000_0000
Description	These registers are used to control continuous time linear equalization (CTLE) on the DQ data bits. This is a new function for POWER9.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:49	RW	NIB_2_DQSEL_CAP: This field sets the capacitance value in the RC source degeneration, which defines the zero in the CTLEs transfer characteristic together with *_DQSEL_RES. The value is binary encoded. Higher values add more capacitance. 00 = No capacitor is selected. 01 to 10 = An increasing number of capacitors are selected. 11 = The maximum number of capacitors is selected.
50:52	RW	NIB{0,2}_BIAS_TRIM: This field sets the bias current in the CTLE circuit. 000 = Nominal current.
53:55	RW	NIB_2_DQSEL_RES: This field sets the resistance value in the RC source degeneration, which defines the zero in the CTLEs transfer characteristic together with *_DQSEL_CAP. In addition to setting the zero in the transfer characteristic, this also defines the CTLEs DC gain. The value is binary coded. Higher values decrease resistance. 000 = Maximum resistance; only a fixed resistor is used. 001 to 110 = Decreasing resistance. 111 = Minimum resistance.
56:57	RW	NIB_3_DQSEL_CAP: This field sets the capacitance value in the RC source degeneration, which defines the zero in the CTLEs transfer characteristic together with *_DQSEL_RES. The value is binary encoded. Higher values add more capacitance. 00 = No capacitor is selected. 01 to 10 = An increasing number of capacitors are selected. 11 = The maximum number of capacitors is selected.
58:60	RW	NIB{1,3}_BIAS_TRIM: This field sets the bias current in the CTLE circuit. 000 = Nominal current.
61:63	RW	NIB_3_DQSEL_RES: This field sets the resistance value in the RC source degeneration, which defines the zero in the CTLEs transfer characteristic together with *_DQSEL_CAP. In addition to setting the zero in the transfer characteristic, this also defines the CTLEs DC gain. The value is binary coded. Higher values decrease resistance. 000 = Maximum resistance; only a fixed resistor is used. 001 to 110 = Decreasing resistance. 111 = Minimum resistance.

Register Name	**DP16 AC Boost Control Byte 0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_ACBOOST_CTL_BYTE0_P0_[n]
Address	800000220701103F (SCOM), +0x0400_0000_0000
Description	These registers are used to control the AC boost on the DQ data bits. This is a new function for POWER9.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:50	RW	S0ACENSLICENDRV_DC: Selects the number of enabled pull-down branches in the AC-boost slices during WRITE mode. 000 = None selected. 001, 010, 100 = One branch selected. 011, 101, 110 = Two branches selected. 111 = All branches selected. All other values are invalid and have unpredictable effects.
51:53	RW	S0ACENSLICEPDRV_DC: Selects the number of enabled pull-up branches in the AC-boost slices during WRITE mode. 000 = None selected. 001, 010, 100 = One branch selected. 011, 101, 110 = Two branches selected. 111 = All branches selected. All other values are invalid and have unpredictable effects.
54:56	RW	S0ACENSLICEPTERM_DC: Selects the number of enabled pull-up branches in the AC-boost slices during READ mode. 000 = None selected. 001, 010, 100 = One branch selected. 011, 101, 110 = Two branches selected. 111 = All branches selected. All other values are invalid and have unpredictable effects.
57:63	RO	Constant = 0b0000000

Register Name	**DP16 AC Boost Control Byte 0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_ACBOOST_CTL_BYTE0_P1_[n]
Address	800000220701143F (SCOM), +0x0400_0000_0000
Description	These registers are used to control the AC boost on the DQ data bits. This is a new function for POWER9.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:50	RW	S0ACENSLICENDRV_DC: Selects the number of enabled pull-down branches in the AC-boost slices during WRITE mode. 000 = None selected. 001, 010, 100 = One branch selected. 011, 101, 110 = Two branches selected. 111 = All branches selected. All other values are invalid and have unpredictable effects.
51:53	RW	S0ACENSLICEPDRV_DC: Selects the number of enabled pull-up branches in the AC-boost slices during WRITE mode. 000 = None selected. 001, 010, 100 = One branch selected. 011, 101, 110 = Two branches selected. 111 = All branches selected. All other values are invalid and have unpredictable effects.

Bits	SCOM	Field Mnemonic: Description
54:56	RW	S0ACENSLICEPTERM_DC: Selects the number of enabled pull-up branches in the AC-boost slices during READ mode. 000 = None selected. 001, 010, 100 = One branch selected. 011, 101, 110 = Two branches selected. 111 = All branches selected. All other values are invalid and have unpredictable effects.
57:63	RO	Constant = 0b0000000

Register Name	DP16 AC Boost Control Byte 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_ACBOOST_CTL_BYTE0_P2_[n]
Address	800000220701183F (SCOM), +0x0400_0000_0000
Description	These registers are used to control the AC boost on the DQ data bits. This is a new function for POWER9.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	S0ACENSLICENDRV_DC: Selects the number of enabled pull-down branches in the AC-boost slices during WRITE mode. 000 = None selected. 001, 010, 100 = One branch selected. 011, 101, 110 = Two branches selected. 111 = All branches selected. All other values are invalid and have unpredictable effects.
51:53	RW	S0ACENSLICEPDRV_DC: Selects the number of enabled pull-up branches in the AC-boost slices during WRITE mode. 000 = None selected. 001, 010, 100 = One branch selected. 011, 101, 110 = Two branches selected. 111 = All branches selected. All other values are invalid and have unpredictable effects.
54:56	RW	S0ACENSLICEPTERM_DC: Selects the number of enabled pull-up branches in the AC-boost slices during READ mode. 000 = None selected. 001, 010, 100 = One branch selected. 011, 101, 110 = Two branches selected. 111 = All branches selected. All other values are invalid and have unpredictable effects.
57:63	RO	Constant = 0b0000000

Register Name	DP16 AC Boost Control Byte 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_ACBOOST_CTL_BYTE0_P3_[n]
Address	8000002207011C3F (SCOM), +0x0400_0000_0000
Description	These registers are used to control the AC boost on the DQ data bits. This is a new function for POWER9.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RW	S0ACENSLICENDRV_DC: Selects the number of enabled pull-down branches in the AC-boost slices during WRITE mode. 000 = None selected. 001, 010, 100 = One branch selected. 011, 101, 110 = Two branches selected. 111 = All branches selected. All other values are invalid and have unpredictable effects.
51:53	RW	S0ACENSLICEPDRV_DC: Selects the number of enabled pull-up branches in the AC-boost slices during WRITE mode. 000 = None selected. 001, 010, 100 = One branch selected. 011, 101, 110 = Two branches selected. 111 = All branches selected. All other values are invalid and have unpredictable effects.
54:56	RW	S0ACENSLICEPTERM_DC: Selects the number of enabled pull-up branches in the AC-boost slices during READ mode. 000 = None selected. 001, 010, 100 = One branch selected. 011, 101, 110 = Two branches selected. 111 = All branches selected. All other values are invalid and have unpredictable effects.
57:63	RO	Constant = 0b0000000

Register Name	**DP16 AC Boost Control Byte 1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_ACBOOST_CTL_BYTE1_P0_[n]
Address	800000230701103F (SCOM), +0x0400_0000_0000
Description	These registers are used to control the AC boost on the DQ data bits. This is a new function for POWER9.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	S1ACENSLICENDRV_DC: Selects the number of enabled pull-down branches in the AC-boost slices during WRITE mode. 000 = None selected. 001, 010, 100 = One branch selected. 011, 101, 110 = Two branches selected. 111 = All branches selected. All other values are invalid and have unpredictable effects.
51:53	RW	S1ACENSLICEPDRV_DC: Selects the number of enabled pull-up branches in the AC-boost slices during WRITE mode. 000 = None selected. 001, 010, 100 = One branch selected. 011, 101, 110 = Two branches selected. 111 = All branches selected. All other values are invalid and have unpredictable effects.
54:56	RW	S1ACENSLICEPTERM_DC: Selects the number of enabled pull-up branches in the AC-boost slices during READ mode. 000 = None selected. 001, 010, 100 = One branch selected. 011, 101, 110 = Two branches selected. 111 = All branches selected. All other values are invalid and have unpredictable effects.

Bits	SCOM	Field Mnemonic: Description
57:63	RO	Constant = 0b0000000

Register Name	DP16 AC Boost Control Byte 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_ACBOOST_CTL_BYTE1_P1_[n]
Address	800000230701143F (SCOM), +0x0400_0000_0000
Description	These registers are used to control the AC boost on the DQ data bits. This is a new function for POWER9.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:50	RW	S1ACENSLICENDRV_DC: Selects the number of enabled pull-down branches in the AC-boost slices during WRITE mode. 000 = None selected. 001, 010, 100 = One branch selected. 011, 101, 110 = Two branches selected. 111 = All branches selected. All other values are invalid and have unpredictable effects.
51:53	RW	S1ACENSLICEPDRV_DC: Selects the number of enabled pull-up branches in the AC-boost slices during WRITE mode. 000 = None selected. 001, 010, 100 = One branch selected. 011, 101, 110 = Two branches selected. 111 = All branches selected. All other values are invalid and have unpredictable effects.
54:56	RW	S1ACENSLICEPTERM_DC: Selects the number of enabled pull-up branches in the AC-boost slices during READ mode. 000 = None selected. 001, 010, 100 = One branch selected. 011, 101, 110 = Two branches selected. 111 = All branches selected. All other values are invalid and have unpredictable effects.
57:63	RO	Constant = 0b0000000

Register Name	DP16 AC Boost Control Byte 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_ACBOOST_CTL_BYTE1_P2_[n]
Address	800000230701183F (SCOM), +0x0400_0000_0000
Description	These registers are used to control the AC boost on the DQ data bits. This is a new function for POWER9.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:50	RW	S1ACENSLICENDRV_DC: Selects the number of enabled pull-down branches in the AC-boost slices during WRITE mode. 000 = None selected. 001, 010, 100 = One branch selected. 011, 101, 110 = Two branches selected. 111 = All branches selected. All other values are invalid and have unpredictable effects.

Bits	SCOM	Field Mnemonic: Description
51:53	RW	S1ACENSLICEPDRV_DC: Selects the number of enabled pull-up branches in the AC-boost slices during WRITE mode. 000 = None selected. 001, 010, 100 = One branch selected. 011, 101, 110 = Two branches selected. 111 = All branches selected. All other values are invalid and have unpredictable effects.
54:56	RW	S1ACENSLICEPTERM_DC: Selects the number of enabled pull-up branches in the AC-boost slices during READ mode. 000 = None selected. 001, 010, 100 = One branch selected. 011, 101, 110 = Two branches selected. 111 = All branches selected. All other values are invalid and have unpredictable effects.
57:63	RO	Constant = 0b0000000

Register Name	DP16 AC Boost Control Byte 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_ACBOOST_CTL_BYTE1_P3_[n]
Address	8000002307011C3F (SCOM), +0x0400_0000_0000
Description	These registers are used to control the AC boost on the DQ data bits. This is a new function for POWER9.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	S1ACENSLICENDRV_DC: Selects the number of enabled pull-down branches in the AC-boost slices during WRITE mode. 000 = None selected. 001, 010, 100 = One branch selected. 011, 101, 110 = Two branches selected. 111 = All branches selected. All other values are invalid and have unpredictable effects.
51:53	RW	S1ACENSLICEPDRV_DC: Selects the number of enabled pull-up branches in the AC-boost slices during WRITE mode. 000 = None selected. 001, 010, 100 = One branch selected. 011, 101, 110 = Two branches selected. 111 = All branches selected. All other values are invalid and have unpredictable effects.
54:56	RW	S1ACENSLICEPTERM_DC: Selects the number of enabled pull-up branches in the AC-boost slices during READ mode. 000 = None selected. 001, 010, 100 = One branch selected. 011, 101, 110 = Two branches selected. 111 = All branches selected. All other values are invalid and have unpredictable effects.
57:63	RO	Constant = 0b0000000

Register Name	**DP16 DLL Control 0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DLL_CNTL0_P0_[n]
Address	800000240701103F (SCOM), +0x0400_0000_0000
Description	This register controls the delay locked loop (DLL) calibration logic. CAUTION: This register must not be written while hardware calibration is active. Note: When writing the register, software must write bits (61:63) to 0b000 to avoid a parity error.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	RW	INIT_RXDLL_CAL_RESET: When 1, DLL calibration controls are set to default values and the DLL output clocks are not correct. Write to 0 to initiate full calibration. Leave at 0 after calibration. Note: Power must be on and stable to the analog DLL logic a minimum of 100 ns before deactivating reset.
49	RW	INIT_RXDLL_CAL_UPDATE: When 1, this bit requests DLL calibration to update/adjust fine delays only. Voltage regulation (VREG) and coarse calibration are skipped, although they must have completed successfully before writing this bit to 1. Note: This bit starts at 0, but hardware automatically sets it to 1 on the rising edge of "cal_good," which should occur after full calibration. This enables fine calibration to run continuously after full calibration. When software writes this bit to 0, reads of the bit might still show 1 until the current fine calibration sequence finishes. Note: Power must be on and stable to the analog DLL logic a minimum of 100 ns before activating CAL_UPDATE.
50:51	RW	REGS_RXDLL_CAL_SKIP: Skip calibration steps (requires manual presets too). Bit 0: When 1, skip VREG calibration. Bit 1: When 1, skip coarse delay calibration.
52	RW	REGS_RXDLL_COARSE_ADJ_BY2: At the end of coarse calibration, the DAC code is reduced to set the total delay under one period before entering fine calibration. This bit controls whether the reduction is one or two code increments. When 0, change the final coarse delay setting by 1 (default). When 1, change the final coarse delay setting by 2. Note: This bit has lower priority than REGS_RXDLL_COARSE_ADJ_BY0 if both are set.
53:55	RW	RXREG_DLL_FILTER_LENGTH_DC: This field adjusts the number of lead/lag samples to filter out. A smaller binary code gives a smaller number of samples.
56:58	RW	RXREG_DLL_LEAD_LAG_SEPARATION_DC: This field adjusts the number of lead-more-than-lag or lag-more than-lead to get a positive phase adjustment or a negative phase adjustment.
59	RW	DLL_EN_DRIVER_INVFB_DC: Enable driver inverter feedback. This bit controls when cross-coupled inverters are included across DLL output drivers. Adding the inverters can improve driver performance, but might introduce excessive current if the DLL outputs are not close to their final values. The intent is to exclude the cross-coupled inverters during initial calibration, but possibly include them, when repeating fine calibration only, because DLL outputs are close to their optimal values during fine calibration. 0 = Disable use of cross-coupled inverters on DLL output drivers. 1 = Enable use of cross-coupled inverters on DLL output drivers.
60	RW	Reserved.
61	ROX	CAL_GOOD: (Read only.) When 1, calibration finished successfully. When 0, calibration is on-going or resulted in an error if either CAL_ERROR or CAL_ERROR_FINE is set. Note: This is the local copy of CAL_GOOD directly from the DLL calibration logic. Thus, it alternates between 0 and 1 when fine calibration runs continuously.
62	ROX	CAL_ERROR: (Read only.) When 1, VREG or coarse calibration finished with an error.
63	ROX	CAL_ERROR_FINE: (Read only.) When 1, fine calibration finished with an error.

Register Name	DP16 DLL Control 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_CNTL0_P1_[n]
Address	800000240701143F (SCOM), +0x0400_0000_0000
Description	This register controls the DLL calibration logic. CAUTION: This register must not be written while hardware calibration is active. Note: When writing the register, software must write bits (61:63) to 0b000 to avoid a parity error.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	RW	INIT_RXDLL_CAL_RESET: When 1, DLL calibration controls are set to default values and the DLL output clocks are not correct. Write to 0 to initiate full calibration. Leave at 0 after calibration. Note: Power must be on and stable to the analog DLL logic a minimum of 100 ns before deactivating reset.
49	RW	INIT_RXDLL_CAL_UPDATE: When 1, this bit requests DLL calibration to update/adjust fine delays only. VREG and coarse calibration are skipped, although they must have completed successfully before writing this bit to 1. Note: This bit starts at 0, but hardware automatically sets it to 1 on the rising edge of "cal_good," which should occur after full calibration. This enables fine calibration to run continuously after full calibration. When software writes this bit to 0, reads of the bit might still show 1 until the current fine calibration sequence finishes. Note: Power must be on and stable to the analog DLL logic a minimum of 100 ns before activating CAL_UPDATE.
50:51	RW	REGS_RXDLL_CAL_SKIP: Skip calibration steps (requires manual presets too). Bit 0: When 1, skip VREG calibration. Bit 1: When 1, skip coarse delay calibration.
52	RW	REGS_RXDLL_COARSE_ADJ_BY2: At the end of coarse calibration, the DAC code is reduced to set the total delay under one period before entering fine calibration. This bit controls whether the reduction is one or two code increments. When 0, change the final coarse delay setting by 1 (default). When 1, change the final coarse delay setting by 2. Note: This bit has lower priority than REGS_RXDLL_COARSE_ADJ_BY0 if both are set.
53:55	RW	RXREG_DLL_FILTER_LENGTH_DC: This field adjusts the number of lead/lag samples to filter out. A smaller binary code gives a smaller number of samples.
56:58	RW	RXREG_DLL_LEAD_LAG_SEPARATION_DC: This field adjusts the number of lead-more-than-lag or lag-more than-lead to get a positive phase adjustment or a negative phase adjustment.
59	RW	DLL_EN_DRIVER_INVFB_DC: Enable driver inverter feedback. This bit controls when cross-coupled inverters are included across DLL output drivers. Adding the inverters can improve driver performance, but might introduce excessive current if the DLL outputs are not close to their final values. The intent is to exclude the cross-coupled inverters during initial calibration, but possibly include them, when repeating fine calibration only, because DLL outputs are close to their optimal values during fine calibration 0 = Disable use of cross-coupled inverters on DLL output drivers. 1 = Enable use of cross-coupled inverters on DLL output drivers.
60	RW	Reserved.
61	ROX	CAL_GOOD: (Read only.) When 1, calibration finished successfully. When 0, calibration is on-going or resulted in an error if either CAL_ERROR or CAL_ERROR_FINE is set. Note: This is the local copy of CAL_GOOD directly from the DLL calibration logic. Thus, it alternates between 0 and 1 when fine calibration runs continuously.
62	ROX	CAL_ERROR: (Read only.) When 1, VREG or coarse calibration finished with an error.
63	ROX	CAL_ERROR_FINE: (Read only.) When 1, fine calibration finished with an error.

Register Name	DP16 DLL Control 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_CNTL0_P2_[n]
Address	800000240701183F (SCOM), +0x0400_0000_0000
Description	This register controls the DLL calibration logic. CAUTION: This register must not be written while hardware calibration is active. Note: When writing the register, software must write bits (61:63) to 0b000 to avoid a parity error.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	RW	INIT_RXDLL_CAL_RESET: When 1, DLL calibration controls are set to default values and the DLL output clocks are not correct. Write to 0 to initiate full calibration. Leave at 0 after calibration. Note: Power must be on and stable to the analog DLL logic a minimum of 100 ns before deactivating reset.
49	RW	INIT_RXDLL_CAL_UPDATE: When 1, this bit requests DLL calibration to update/adjust fine delays only. VREG and coarse calibration are skipped, although they must have completed successfully before writing this bit to 1. Note: This bit starts at 0, but hardware automatically sets it to 1 on the rising edge of "cal_good," which should occur after full calibration. This enables fine calibration to run continuously after full calibration. When software writes this bit to 0, reads of the bit might still show 1 until the current fine calibration sequence finishes. Note: Power must be on and stable to the analog DLL logic a minimum of 100 ns before activating CAL_UPDATE.
50:51	RW	REGS_RXDLL_CAL_SKIP: Skip calibration steps (requires manual presets too). Bit 0: When 1, skip VREG calibration. Bit 1: When 1, skip coarse delay calibration.
52	RW	REGS_RXDLL_COARSE_ADJ_BY2: At the end of coarse calibration, the DAC code is reduced to set the total delay under one period before entering fine calibration. This bit controls whether the reduction is one or two code increments. When 0, change the final coarse delay setting by 1 (default). When 1, change the final coarse delay setting by 2. Note: This bit has lower priority than REGS_RXDLL_COARSE_ADJ_BY0 if both are set.
53:55	RW	RXREG_DLL_FILTER_LENGTH_DC: This field adjusts the number of lead/lag samples to filter out. A smaller binary code gives a smaller number of samples.
56:58	RW	RXREG_DLL_LEAD_LAG_SEPARATION_DC: This field adjusts the number of lead-more-than-lag or lag-more than-lead to get a positive phase adjustment or a negative phase adjustment.
59	RW	DLL_EN_DRIVER_INVFB_DC: Enable driver inverter feedback. This bit controls when cross-coupled inverters are included across DLL output drivers. Adding the inverters can improve driver performance, but might introduce excessive current if the DLL outputs are not close to their final values. The intent is to exclude the cross-coupled inverters during initial calibration, but possibly include them, when repeating fine calibration only, because DLL outputs are close to their optimal values during fine calibration 0 = Disable use of cross-coupled inverters on DLL output drivers. 1 = Enable use of cross-coupled inverters on DLL output drivers.
60	RW	Reserved.
61	ROX	CAL_GOOD: (Read only.) When 1, calibration finished successfully. When 0, calibration is on-going or resulted in an error if either CAL_ERROR or CAL_ERROR_FINE is set. Note: This is the local copy of CAL_GOOD directly from the DLL calibration logic. Thus, it alternates between 0 and 1 when fine calibration runs continuously.
62	ROX	CAL_ERROR: (Read only.) When 1, VREG or coarse calibration finished with an error.
63	ROX	CAL_ERROR_FINE: (Read only.) When 1, fine calibration finished with an error.

Register Name	DP16 DLL Control 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_CNTL0_P3_[n]
Address	8000002407011C3F (SCOM), +0x0400_0000_0000
Description	This register controls the DLL calibration logic. CAUTION: This register must not be written while hardware calibration is active. Note: When writing the register, software must write bits (61:63) to 0b000 to avoid a parity error.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	RW	INIT_RXDLL_CAL_RESET: When 1, DLL calibration controls are set to default values and the DLL output clocks are not correct. Write to 0 to initiate full calibration. Leave at 0 after calibration. Note: Power must be on and stable to the analog DLL logic a minimum of 100 ns before deactivating reset.
49	RW	INIT_RXDLL_CAL_UPDATE: When 1, this bit requests DLL calibration to update/adjust fine delays only. VREG and coarse calibration are skipped, although they must have completed successfully before writing this bit to 1. Note: This bit starts at 0, but hardware automatically sets it to 1 on the rising edge of "cal_good," which should occur after full calibration. This enables fine calibration to run continuously after full calibration. When software writes this bit to 0, reads of the bit might still show 1 until the current fine calibration sequence finishes. Note: Power must be on and stable to the analog DLL logic a minimum of 100 ns before activating CAL_UPDATE.
50:51	RW	REGS_RXDLL_CAL_SKIP: Skip calibration steps (requires manual presets too). Bit 0: When 1, skip VREG calibration. Bit 1: When 1, skip coarse delay calibration.
52	RW	REGS_RXDLL_COARSE_ADJ_BY2: At the end of coarse calibration, the DAC code is reduced to set the total delay under one period before entering fine calibration. This bit controls whether the reduction is one or two code increments. When 0, change the final coarse delay setting by 1 (default). When 1, change the final coarse delay setting by 2. Note: This bit has lower priority than REGS_RXDLL_COARSE_ADJ_BY0 if both are set.
53:55	RW	RXREG_DLL_FILTER_LENGTH_DC: This field adjusts the number of lead/lag samples to filter out. A smaller binary code gives a smaller number of samples.
56:58	RW	RXREG_DLL_LEAD_LAG_SEPARATION_DC: This field adjusts the number of lead-more-than-lag or lag-more than-lead to get a positive phase adjustment or a negative phase adjustment.
59	RW	DLL_EN_DRIVER_INVFB_DC: Enable driver inverter feedback. This bit controls when cross-coupled inverters are included across DLL output drivers. Adding the inverters can improve driver performance, but might introduce excessive current if the DLL outputs are not close to their final values. The intent is to exclude the cross-coupled inverters during initial calibration, but possibly include them, when repeating fine calibration only, because DLL outputs are close to their optimal values during fine calibration 0 = Disable use of cross-coupled inverters on DLL output drivers. 1 = Enable use of cross-coupled inverters on DLL output drivers.
60	RW	Reserved.
61	ROX	CAL_GOOD: (Read only.) When 1, calibration finished successfully. When 0, calibration is on-going or resulted in an error if either CAL_ERROR or CAL_ERROR_FINE is set. Note: This is the local copy of CAL_GOOD directly from the DLL calibration logic. Thus, it alternates between 0 and 1 when fine calibration runs continuously.
62	ROX	CAL_ERROR: (Read only.) When 1, VREG or coarse calibration finished with an error.
63	ROX	CAL_ERROR_FINE: (Read only.) When 1, fine calibration finished with an error.

Register Name	DP16 DLL Control 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_CNTL1_P0_[n]
Address	800000250701103F (SCOM), +0x0400_0000_0000
Description	This register controls the DLL calibration logic. CAUTION: This register must not be written while hardware calibration is active. Note: When writing the register, software must write bits (61:63) to 0b000 to avoid a parity error.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	RW	INIT_RXDLL_CAL_RESET: When 1, DLL calibration controls are set to default values and the DLL output clocks are not correct. Write to 0 to initiate full calibration. Leave at 0 after calibration. Note: Power must be on and stable to the analog DLL logic a minimum of 100 ns before deactivating reset.
49	RW	INIT_RXDLL_CAL_UPDATE: When 1, this bit requests DLL calibration to update/adjust fine delays only. VREG and coarse calibration are skipped, although they must have completed successfully before writing this bit to 1. Note: This bit starts at 0, but hardware automatically sets it to 1 on the rising edge of "cal_good," which should occur after full calibration. This enables fine calibration to run continuously after full calibration. When software writes this bit to 0, reads of the bit might still show 1 until the current fine calibration sequence finishes. Note: Power must be on and stable to the analog DLL logic a minimum of 100 ns before activating CAL_UPDATE.
50:51	RW	REGS_RXDLL_CAL_SKIP: Skip calibration steps (requires manual presets too). Bit 0: When 1, skip VREG calibration. Bit 1: When 1, skip coarse delay calibration.
52	RW	REGS_RXDLL_COARSE_ADJ_BY2: At the end of coarse calibration, the DAC code is reduced to set the total delay under one period before entering fine calibration. This bit controls whether the reduction is one or two code increments. When 0, change the final coarse delay setting by 1 (default). When 1, change the final coarse delay setting by 2. Note: This bit has lower priority than REGS_RXDLL_COARSE_ADJ_BY0 if both are set.
53:55	RW	RXREG_DLL_FILTER_LENGTH_DC: This field adjusts the number of lead/lag samples to filter out. A smaller binary code gives a smaller number of samples.
56:58	RW	RXREG_DLL_LEAD_LAG_SEPARATION_DC: This field adjusts the number of lead-more-than-lag or lag-more than-lead to get a positive phase adjustment or a negative phase adjustment.
59	RW	DLL_EN_DRIVER_INVFB_DC: Enable driver inverter feedback. This bit controls when cross-coupled inverters are included across DLL output drivers. Adding the inverters can improve driver performance, but might introduce excessive current if the DLL outputs are not close to their final values. The intent is to exclude the cross-coupled inverters during initial calibration, but possibly include them, when repeating fine calibration only, because DLL outputs are close to their optimal values during fine calibration 0 = Disable use of cross-coupled inverters on DLL output drivers. 1 = Enable use of cross-coupled inverters on DLL output drivers.
60	RW	Reserved.
61	ROX	CAL_GOOD: (Read only.) When 1, calibration finished successfully. When 0, calibration is on-going or resulted in an error if either CAL_ERROR or CAL_ERROR_FINE is set. Note: This is the local copy of CAL_GOOD directly from the DLL calibration logic. Thus, it alternates between 0 and 1 when fine calibration runs continuously.
62	ROX	CAL_ERROR: (Read only.) When 1, VREG or coarse calibration finished with an error.
63	ROX	CAL_ERROR_FINE: (Read only.) When 1, fine calibration finished with an error.

Register Name	DP16 DLL Control 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_CNTL1_P1_[n]
Address	800000250701143F (SCOM), +0x0400_0000_0000
Description	This register controls the DLL calibration logic. CAUTION: This register must not be written while hardware calibration is active. Note: When writing the register, software must write bits (61:63) to 0b000 to avoid a parity error.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	RW	INIT_RXDLL_CAL_RESET: When 1, DLL calibration controls are set to default values and the DLL output clocks are not correct. Write to 0 to initiate full calibration. Leave at 0 after calibration. Note: Power must be on and stable to the analog DLL logic a minimum of 100 ns before deactivating reset.
49	RW	INIT_RXDLL_CAL_UPDATE: When 1, this bit requests DLL calibration to update/adjust fine delays only. VREG and coarse calibration are skipped, although they must have completed successfully before writing this bit to 1. Note: This bit starts at 0, but hardware automatically sets it to 1 on the rising edge of "cal_good," which should occur after full calibration. This enables fine calibration to run continuously after full calibration. When software writes this bit to 0, reads of the bit might still show 1 until the current fine calibration sequence finishes. Note: Power must be on and stable to the analog DLL logic a minimum of 100 ns before activating CAL_UPDATE.
50:51	RW	REGS_RXDLL_CAL_SKIP: Skip calibration steps (requires manual presets too). Bit 0: When 1, skip VREG calibration. Bit 1: When 1, skip coarse delay calibration.
52	RW	REGS_RXDLL_COARSE_ADJ_BY2: At the end of coarse calibration, the DAC code is reduced to set the total delay under one period before entering fine calibration. This bit controls whether the reduction is one or two code increments. When 0, change the final coarse delay setting by 1 (default). When 1, change the final coarse delay setting by 2. Note: This bit has lower priority than REGS_RXDLL_COARSE_ADJ_BY0 if both are set.
53:55	RW	RXREG_DLL_FILTER_LENGTH_DC: This field adjusts the number of lead/lag samples to filter out. A smaller binary code gives a smaller number of samples.
56:58	RW	RXREG_DLL_LEAD_LAG_SEPARATION_DC: This field adjusts the number of lead-more-than-lag or lag-more than-lead to get a positive phase adjustment or a negative phase adjustment.
59	RW	DLL_EN_DRIVER_INVFB_DC: Enable driver inverter feedback. This bit controls when cross-coupled inverters are included across DLL output drivers. Adding the inverters can improve driver performance, but might introduce excessive current if the DLL outputs are not close to their final values. The intent is to exclude the cross-coupled inverters during initial calibration, but possibly include them, when repeating fine calibration only, because DLL outputs are close to their optimal values during fine calibration 0 = Disable use of cross-coupled inverters on DLL output drivers. 1 = Enable use of cross-coupled inverters on DLL output drivers.
60	RW	Reserved.
61	ROX	CAL_GOOD: (Read only.) When 1, calibration finished successfully. When 0, calibration is on-going or resulted in an error if either CAL_ERROR or CAL_ERROR_FINE is set. Note: This is the local copy of CAL_GOOD directly from the DLL calibration logic. Thus, it alternates between 0 and 1 when fine calibration runs continuously.
62	ROX	CAL_ERROR: (Read only.) When 1, VREG or coarse calibration finished with an error.
63	ROX	CAL_ERROR_FINE: (Read only.) When 1, fine calibration finished with an error.

Register Name	DP16 DLL Control 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_CNTL1_P2_[n]
Address	800000250701183F (SCOM), +0x0400_0000_0000
Description	This register controls the DLL calibration logic. CAUTION: This register must not be written while hardware calibration is active. Note: When writing the register, software must write bits (61:63) to 0b000 to avoid a parity error.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	RW	INIT_RXDLL_CAL_RESET: When 1, DLL calibration controls are set to default values and the DLL output clocks are not correct. Write to 0 to initiate full calibration. Leave at 0 after calibration. Note: Power must be on and stable to the analog DLL logic a minimum of 100 ns before deactivating reset.
49	RW	INIT_RXDLL_CAL_UPDATE: When 1, this bit requests DLL calibration to update/adjust fine delays only. VREG and coarse calibration are skipped, although they must have completed successfully before writing this bit to 1. Note: This bit starts at 0, but hardware automatically sets it to 1 on the rising edge of "cal_good," which should occur after full calibration. This enables fine calibration to run continuously after full calibration. When software writes this bit to 0, reads of the bit might still show 1 until the current fine calibration sequence finishes. Note: Power must be on and stable to the analog DLL logic a minimum of 100 ns before activating CAL_UPDATE.
50:51	RW	REGS_RXDLL_CAL_SKIP: Skip calibration steps (requires manual presets too). Bit 0: When 1, skip VREG calibration. Bit 1: When 1, skip coarse delay calibration.
52	RW	REGS_RXDLL_COARSE_ADJ_BY2: At the end of coarse calibration, the DAC code is reduced to set the total delay under one period before entering fine calibration. This bit controls whether the reduction is one or two code increments. When 0, change the final coarse delay setting by 1 (default). When 1, change the final coarse delay setting by 2. Note: This bit has lower priority than REGS_RXDLL_COARSE_ADJ_BY0 if both are set.
53:55	RW	RXREG_DLL_FILTER_LENGTH_DC: This field adjusts the number of lead/lag samples to filter out. A smaller binary code gives a smaller number of samples.
56:58	RW	RXREG_DLL_LEAD_LAG_SEPARATION_DC: This field adjusts the number of lead-more-than-lag or lag-more than-lead to get a positive phase adjustment or a negative phase adjustment.
59	RW	DLL_EN_DRIVER_INVFB_DC: Enable driver inverter feedback. This bit controls when cross-coupled inverters are included across DLL output drivers. Adding the inverters can improve driver performance, but might introduce excessive current if the DLL outputs are not close to their final values. The intent is to exclude the cross-coupled inverters during initial calibration, but possibly include them, when repeating fine calibration only, because DLL outputs are close to their optimal values during fine calibration 0 = Disable use of cross-coupled inverters on DLL output drivers. 1 = Enable use of cross-coupled inverters on DLL output drivers.
60	RW	Reserved.
61	ROX	CAL_GOOD: (Read only.) When 1, calibration finished successfully. When 0, calibration is on-going or resulted in an error if either CAL_ERROR or CAL_ERROR_FINE is set. Note: This is the local copy of CAL_GOOD directly from the DLL calibration logic. Thus, it alternates between 0 and 1 when fine calibration runs continuously.
62	ROX	CAL_ERROR: (Read only.) When 1, VREG or coarse calibration finished with an error.
63	ROX	CAL_ERROR_FINE: (Read only.) When 1, fine calibration finished with an error.

Register Name	DP16 DLL Control 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_CNTL1_P3_[n]
Address	8000002507011C3F (SCOM), +0x0400_0000_0000
Description	This register controls the DLL calibration logic. CAUTION: This register must not be written while hardware calibration is active. Note: When writing the register, software must write bits (61:63) to 0b000 to avoid a parity error.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	RW	INIT_RXDLL_CAL_RESET: When 1, DLL calibration controls are set to default values and the DLL output clocks are not correct. Write to 0 to initiate full calibration. Leave at 0 after calibration. Note: Power must be on and stable to the analog DLL logic a minimum of 100 ns before deactivating reset.
49	RW	INIT_RXDLL_CAL_UPDATE: When 1, this bit requests DLL calibration to update/adjust fine delays only. VREG and coarse calibration are skipped, although they must have completed successfully before writing this bit to 1. Note: This bit starts at 0, but hardware automatically sets it to 1 on the rising edge of "cal_good," which should occur after full calibration. This enables fine calibration to run continuously after full calibration. When software writes this bit to 0, reads of the bit might still show 1 until the current fine calibration sequence finishes. Note: Power must be on and stable to the analog DLL logic a minimum of 100 ns before activating CAL_UPDATE.
50:51	RW	REGS_RXDLL_CAL_SKIP: Skip calibration steps (requires manual presets too). Bit 0: When 1, skip VREG calibration. Bit 1: When 1, skip coarse delay calibration.
52	RW	REGS_RXDLL_COARSE_ADJ_BY2: At the end of coarse calibration, the DAC code is reduced to set the total delay under one period before entering fine calibration. This bit controls whether the reduction is one or two code increments. When 0, change the final coarse delay setting by 1 (default). When 1, change the final coarse delay setting by 2. Note: This bit has lower priority than REGS_RXDLL_COARSE_ADJ_BY0 if both are set.
53:55	RW	RXREG_DLL_FILTER_LENGTH_DC: This field adjusts the number of lead/lag samples to filter out. A smaller binary code gives a smaller number of samples.
56:58	RW	RXREG_DLL_LEAD_LAG_SEPARATION_DC: This field adjusts the number of lead-more-than-lag or lag-more than-lead to get a positive phase adjustment or a negative phase adjustment.
59	RW	DLL_EN_DRIVER_INVFB_DC: Enable driver inverter feedback. This bit controls when cross-coupled inverters are included across DLL output drivers. Adding the inverters can improve driver performance, but might introduce excessive current if the DLL outputs are not close to their final values. The intent is to exclude the cross-coupled inverters during initial calibration, but possibly include them, when repeating fine calibration only, because DLL outputs are close to their optimal values during fine calibration 0 = Disable use of cross-coupled inverters on DLL output drivers. 1 = Enable use of cross-coupled inverters on DLL output drivers.
60	RW	Reserved.
61	ROX	CAL_GOOD: (Read only.) When 1, calibration finished successfully. When 0, calibration is on-going or resulted in an error if either CAL_ERROR or CAL_ERROR_FINE is set. Note: This is the local copy of CAL_GOOD directly from the DLL calibration logic. Thus, it alternates between 0 and 1 when fine calibration runs continuously.
62	ROX	CAL_ERROR: (Read only.) When 1, VREG or coarse calibration finished with an error.
63	ROX	CAL_ERROR_FINE: (Read only.) When 1, fine calibration finished with an error.

Register Name	DP16 DLL DAC Lower 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_DAC_LOWER0_P0_[n]
Address	800000260701103F (SCOM), +0x0400_0000_0000
Description	This register holds the lower bound for DLL calibration logic. CAUTION: This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:62	RWX	REGS_RXDLL_VREG_DAC_LOWER: This field controls the value of VREG during fine calibration. Bits set to 1 are independent of each other. It is the total number of them that matter. For example, these settings have the same effect: b100...00, b001...00, b000...10. VREG and delay line element propagation time are inversely proportional because higher values of VREG mean faster delay elements. Therefore, adding more 1s increases VREG and makes faster delay elements. Recommendation: Change bits in thermometer code fashion because that is how the digital calibration logic does it.
63	RWX	RESERVED_63: Reserved.

Register Name	DP16 DLL DAC Lower 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_DAC_LOWER0_P1_[n]
Address	800000260701143F (SCOM), +0x0400_0000_0000
Description	This register holds the lower bound for DLL calibration logic. CAUTION: This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:62	RWX	REGS_RXDLL_VREG_DAC_LOWER: This field controls the value of VREG during fine calibration. Bits set to 1 are independent of each other. It is the total number of them that matter. For example, these settings have the same effect: b100...00, b001...00, b000...10. VREG and delay line element propagation time are inversely proportional because higher values of VREG mean faster delay elements. Therefore, adding more 1s increases VREG and makes faster delay elements. Recommendation: Change bits in thermometer code fashion because that is how the digital calibration logic does it.
63	RWX	RESERVED_63: Reserved.

Register Name	DP16 DLL DAC Lower 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_DAC_LOWER0_P2_[n]
Address	800000260701183F (SCOM), +0x0400_0000_0000
Description	This register holds the lower bound for DLL calibration logic. CAUTION: This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:62	RWX	REGS_RXDLL_VREG_DAC_LOWER: This field controls the value of VREG during fine calibration. Bits set to 1 are independent of each other. It is the total number of them that matter. For example, these settings have the same effect: b100...00, b001...00, b000...10. VREG and delay line element propagation time are inversely proportional because higher values of VREG mean faster delay elements. Therefore, adding more 1s increases VREG and makes faster delay elements. Recommendation: Change bits in thermometer code fashion because that is how the digital calibration logic does it.
63	RWX	RESERVED_63: Reserved.

Register Name	**DP16 DLL DAC Lower 0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DLL_DAC_LOWER0_P3_[n]
Address	8000002607011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the lower bound for DLL calibration logic. CAUTION: This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:62	RWX	REGS_RXDLL_VREG_DAC_LOWER: This field controls the value of VREG during fine calibration. Bits set to 1 are independent of each other. It is the total number of them that matter. For example, these settings have the same effect: b100...00, b001...00, b000...10. VREG and delay line element propagation time are inversely proportional because higher values of VREG mean faster delay elements. Therefore, adding more 1s increases VREG and makes faster delay elements. Recommendation: Change bits in thermometer code fashion because that is how the digital calibration logic does it.
63	RWX	RESERVED_63: Reserved.

Register Name	**DP16 DLL DAC Lower 1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DLL_DAC_LOWER1_P0_[n]
Address	8000002707011 03F (SCOM), +0x0400_0000_0000
Description	This register holds the lower bound for DLL calibration logic. CAUTION: This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:62	RWX	REGS_RXDLL_VREG_DAC_LOWER: This field controls the value of VREG during fine calibration. Bits set to 1 are independent of each other. It is the total number of them that matter. For example, these settings have the same effect: b100...00, b001...00, b000...10. VREG and delay line element propagation time are inversely proportional because higher values of VREG mean faster delay elements. Therefore, adding more 1s increases VREG and makes faster delay elements. Recommendation: Change bits in thermometer code fashion because that is how the digital calibration logic does it.
63	RWX	RESERVED_63: Reserved.

Register Name	DP16 DLL DAC Lower 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_DAC_LOWER1_P1_[n]
Address	800000270701143F (SCOM), +0x0400_0000_0000
Description	This register holds the lower bound for DLL calibration logic. CAUTION: This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:62	RWX	REGS_RXDLL_VREG_DAC_LOWER: This field controls the value of VREG during fine calibration. Bits set to 1 are independent of each other. It is the total number of them that matter. For example, these settings have the same effect: b100...00, b001...00, b000...10. VREG and delay line element propagation time are inversely proportional because higher values of VREG mean faster delay elements. Therefore, adding more 1s increases VREG and makes faster delay elements. Recommendation: Change bits in thermometer code fashion because that is how the digital calibration logic does it.
63	RWX	RESERVED_63: Reserved.

Register Name	DP16 DLL DAC Lower 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_DAC_LOWER1_P2_[n]
Address	800000270701183F (SCOM), +0x0400_0000_0000
Description	This register holds the lower bound for DLL calibration logic. CAUTION: This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:62	RWX	REGS_RXDLL_VREG_DAC_LOWER: This field controls the value of VREG during fine calibration. Bits set to 1 are independent of each other. It is the total number of them that matter. For example, these settings have the same effect: b100...00, b001...00, b000...10. VREG and delay line element propagation time are inversely proportional because higher values of VREG mean faster delay elements. Therefore, adding more 1s increases VREG and makes faster delay elements. Recommendation: Change bits in thermometer code fashion because that is how the digital calibration logic does it.
63	RWX	RESERVED_63: Reserved.

Register Name	DP16 DLL DAC Lower 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_DAC_LOWER1_P3_[n]
Address	8000002707011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the lower bound for DLL calibration logic. CAUTION: This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:62	RWX	REGS_RXDLL_VREG_DAC_LOWER: This field controls the value of VREG during fine calibration. Bits set to 1 are independent of each other. It is the total number of them that matter. For example, these settings have the same effect: b100...00, b001...00, b000...10. VREG and delay line element propagation time are inversely proportional because higher values of VREG mean faster delay elements. Therefore, adding more 1s increases VREG and makes faster delay elements. Recommendation: Change bits in thermometer code fashion because that is how the digital calibration logic does it.
63	RWX	RESERVED_63: Reserved.

Register Name	**DP16 DLL DAC Upper 0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DLL_DAC_UPPER0_P0_[n]
Address	800000280701103F (SCOM), +0x0400_0000_0000
Description	This register holds the upper bound for DLL calibration logic. CAUTION: This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:62	RWX	REGS_RXDLL_VREG_DAC_UPPER: This field behaves the same as REGS_RXDLL_VREG_DAC_LOWER, except the effect on VREG and delay is 16 times larger for each bit.
63	RWX	RESERVED_63: Reserved.

Register Name	**DP16 DLL DAC Upper 0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DLL_DAC_UPPER0_P1_[n]
Address	800000280701143F (SCOM), +0x0400_0000_0000
Description	This register holds the upper bound for DLL calibration logic. CAUTION: This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:62	RWX	REGS_RXDLL_VREG_DAC_UPPER: This field behaves the same as REGS_RXDLL_VREG_DAC_LOWER, except the effect on VREG and delay is 16 times larger for each bit.
63	RWX	RESERVED_63: Reserved.

Register Name	**DP16 DLL DAC Upper 0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DLL_DAC_UPPER0_P2_[n]
Address	800000280701183F (SCOM), +0x0400_0000_0000
Description	This register holds the upper bound for DLL calibration logic. CAUTION: This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:62	RWX	REGS_RXDLL_VREG_DAC_UPPER: This field behaves the same as REGS_RXDLL_VREG_DAC_LOWER, except the effect on VREG and delay is 16 times larger for each bit.

Bits	SCOM	Field Mnemonic: Description
63	RWX	RESERVED_63: Reserved.

Register Name	DP16 DLL DAC Upper 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_DAC_UPPER0_P3_[n]
Address	8000002807011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the upper bound for DLL calibration logic. CAUTION: This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:62	RWX	REGS_RXDLL_VREG_DAC_UPPER: This field behaves the same as REGS_RXDLL_VREG_DAC_LOWER, except the effect on VREG and delay is 16 times larger for each bit.
63	RWX	RESERVED_63: Reserved.

Register Name	DP16 DLL DAC Upper 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_DAC_UPPER1_P0_[n]
Address	800000290701103F (SCOM), +0x0400_0000_0000
Description	This register holds the upper bound for DLL calibration logic. CAUTION: This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:62	RWX	REGS_RXDLL_VREG_DAC_UPPER: This field behaves the same as REGS_RXDLL_VREG_DAC_LOWER, except the effect on VREG and delay is 16 times larger for each bit.
63	RWX	RESERVED_63: Reserved.

Register Name	DP16 DLL DAC Upper 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_DAC_UPPER1_P1_[n]
Address	800000290701143F (SCOM), +0x0400_0000_0000
Description	This register holds the upper bound for DLL calibration logic. CAUTION: This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:62	RWX	REGS_RXDLL_VREG_DAC_UPPER: This field behaves the same as REGS_RXDLL_VREG_DAC_LOWER, except the effect on VREG and delay is 16 times larger for each bit.
63	RWX	RESERVED_63: Reserved.

Register Name	DP16 DLL DAC Upper 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_DAC_UPPER1_P2_[n]
Address	800000290701183F (SCOM), +0x0400_0000_0000
Description	This register holds the upper bound for DLL calibration logic. CAUTION: This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:62	RWX	REGS_RXDLL_VREG_DAC_UPPER: This field behaves the same as REGS_RXDLL_VREG_DAC_LOWER, except the effect on VREG and delay is 16 times larger for each bit.
63	RWX	RESERVED_63: Reserved.

Register Name	DP16 DLL DAC Upper 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_DAC_UPPER1_P3_[n]
Address	8000002907011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the upper bound for DLL calibration logic. CAUTION: This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:62	RWX	REGS_RXDLL_VREG_DAC_UPPER: This field behaves the same as REGS_RXDLL_VREG_DAC_LOWER, except the effect on VREG and delay is 16 times larger for each bit.
63	RWX	RESERVED_63: Reserved.

Register Name	DP16 DLL VREG Control 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_VREG_CONTROL0_P0_[n]
Address	8000002A0701103F (SCOM), +0x0400_0000_0000
Description	This register controls the voltage regulator of the DLL calibration logic. CAUTION: This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	RXREG_VREG_COMPCON_DC: This field affects the compensation capacitor for the regulator. Contact your IBM representative for details.
51	RW	Reserved.
52	RW	RXREG_VREG_DAC_PULLUP_DC: This is a mode switch for the regulator. It is typically not changed.
53:55	RW	RXREG_VREG_DRVCON_DC: This field determines the positive field-effect transistor (PFET) size for the regulator. It is a mode switch that is typically not changed.
56:58	RW	RXREG_VREG_REF_SEL_DC: This field adjusts the target value of VREG for VREG calibration. The lowest value (b000) corresponds to the highest VREG target. The highest value (b111) corresponds to the lowest VREG target. The recommended value is b011.

Bits	SCOM	Field Mnemonic: Description
59	RW	REGS_RXDLL_COARSE_ADJ_BY0: Typically, the transition from coarse to fine calibration decrements the code by 1. Therefore, fine calibration always tries to increase the delay by lowering VREG. Sometimes, however, the typical calibration routine produces a less ideal setting. When set, this bit does not decrement the code. Therefore, fine calibration tries to decrease the delay by increasing VREG. 0 = This bit has no effect. 1 = Do not decrement the coarse code during the transition from coarse to fine calibration. Note: This bit takes priority over REGS_RXDLL_COARSE_ADJ_BY2 if both are set.
60:61	RO	Reserved.
62	RW	DLL_DRVREN_MODE: This bit selects which method is used to control DLL output driver disabling. 0 = POWER8 mode (thermometer style, enabling all drivers up to the one that is used). 1 = POWER9 mode (a sliding group of four drivers enabled).
63	RW	DLL_CAL_CKTS_ACTIVE: This mode switch forces DLL calibration analog circuits to always be powered on. 0 = After VREG calibration, some analog circuits are powered down. 1 = Override auto power down, keeping analog calibration circuits active.

Register Name	DP16 DLL VREG Control 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_VREG_CONTROL0_P1_[n]
Address	8000002A0701143F (SCOM), +0x0400_0000_0000
Description	This register controls the voltage regulator of the DLL calibration logic. CAUTION: This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	RXREG_VREG_COMPCON_DC: This field affects the compensation capacitor for the regulator. Contact your IBM representative for details.
51	RW	Reserved.
52	RW	RXREG_VREG_DAC_PULLUP_DC: This is a mode switch for the regulator. It is typically not changed.
53:55	RW	RXREG_VREG_DRVCON_DC: This field determines the PFET size for the regulator. It is a mode switch that is typically not changed.
56:58	RW	RXREG_VREG_REF_SEL_DC: This field adjusts the target value of VREG for VREG calibration. The lowest value (b000) corresponds to the highest VREG target. The highest value (b111) corresponds to the lowest VREG target. The recommended value is b011.
59	RW	REGS_RXDLL_COARSE_ADJ_BY0: Typically, the transition from coarse to fine calibration decrements the code by 1. Therefore, fine calibration always tries to increase the delay by lowering VREG. Sometimes, however, the typical calibration routine produces a less ideal setting. When set, this bit does not decrement the code. Therefore, fine calibration tries to decrease the delay by increasing VREG. 0 = This bit has no effect. 1 = Do not decrement the coarse code during the transition from coarse to fine calibration. Note: This bit takes priority over REGS_RXDLL_COARSE_ADJ_BY2 if both are set.
60:61	RO	Reserved.
62	RW	DLL_DRVREN_MODE: This bit selects which method is used to control DLL output driver disabling. 0 = POWER8 mode (thermometer style, enabling all drivers up to the one that is used). 1 = POWER9 mode (a sliding group of four drivers enabled).
63	RW	DLL_CAL_CKTS_ACTIVE: This mode switch forces DLL calibration analog circuits to always be powered on. 0 = After VREG calibration, some analog circuits are powered down. 1 = Override auto power down, keeping analog calibration circuits active.

Register Name	DP16 DLL VREG Control 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_VREG_CONTROL0_P2_[n]
Address	8000002A0701183F (SCOM), +0x0400_0000_0000
Description	This register controls the voltage regulator of the DLL calibration logic. CAUTION: This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:50	RW	RXREG_VREG_COMPCON_DC: This field affects the compensation capacitor for the regulator. Contact your IBM representative for details.
51	RW	Reserved.
52	RW	RXREG_VREG_DAC_PULLUP_DC: This is a mode switch for the regulator. It is typically not changed.
53:55	RW	RXREG_VREG_DRVCON_DC: This field determines the PFET size for the regulator. It is a mode switch that is typically not changed.
56:58	RW	RXREG_VREG_REF_SEL_DC: This field adjusts the target value of VREG for VREG calibration. The lowest value (b000) corresponds to the highest VREG target. The highest value (b111) corresponds to the lowest VREG target. The recommended value is b011.
59	RW	REGS_RXDLL_COARSE_ADJ_BY0: Typically, the transition from coarse to fine calibration decrements the code by 1. Therefore, fine calibration always tries to increase the delay by lowering VREG. Sometimes, however, the typical calibration routine produces a less ideal setting. When set, this bit does not decrement the code. Therefore, fine calibration tries to decrease the delay by increasing VREG. 0 = This bit has no effect. 1 = Do not decrement the coarse code during the transition from coarse to fine calibration. Note: This bit takes priority over REGS_RXDLL_COARSE_ADJ_BY2 if both are set.
60:61	RO	Reserved.
62	RW	DLL_DRVREN_MODE: This bit selects which method is used to control DLL output driver disabling. 0 = POWER8 mode (thermometer style, enabling all drivers up to the one that is used). 1 = POWER9 mode (a sliding group of four drivers enabled).
63	RW	DLL_CAL_CKTS_ACTIVE: This mode switch forces DLL calibration analog circuits to always be powered on. 0 = After VREG calibration, some analog circuits are powered down. 1 = Override auto power down, keeping analog calibration circuits active.

Register Name	DP16 DLL VREG Control 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_VREG_CONTROL0_P3_[n]
Address	8000002A07011C3F (SCOM), +0x0400_0000_0000
Description	This register controls the voltage regulator of the DLL calibration logic. CAUTION: This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:50	RW	RXREG_VREG_COMPCON_DC: This field affects the compensation capacitor for the regulator. Contact your IBM representative for details.
51	RW	Reserved.
52	RW	RXREG_VREG_DAC_PULLUP_DC: This is a mode switch for the regulator. It is typically not changed.
53:55	RW	RXREG_VREG_DRVCON_DC: This field determines the PFET size for the regulator. It is a mode switch that is typically not changed.

Bits	SCOM	Field Mnemonic: Description
56:58	RW	RXREG_VREG_REF_SEL_DC: This field adjusts the target value of VREG for VREG calibration. The lowest value (b000) corresponds to the highest VREG target. The highest value (b111) corresponds to the lowest VREG target. The recommended value is b011.
59	RW	REGS_RXDLL_COARSE_ADJ_BY0: Typically, the transition from coarse to fine calibration decrements the code by 1. Therefore, fine calibration always tries to increase the delay by lowering VREG. Sometimes, however, the typical calibration routine produces a less ideal setting. When set, this bit does not decrement the code. Therefore, fine calibration tries to decrease the delay by increasing VREG. 0 = This bit has no effect. 1 = Do not decrement the coarse code during the transition from coarse to fine calibration. Note: This bit takes priority over REGS_RXDLL_COARSE_ADJ_BY2 if both are set.
60:61	RO	Reserved.
62	RW	DLL_DRVREN_MODE: This bit selects which method is used to control DLL output driver disabling. 0 = POWER8 mode (thermometer style, enabling all drivers up to the one that is used). 1 = POWER9 mode (a sliding group of four drivers enabled).
63	RW	DLL_CAL_CKTS_ACTIVE: This mode switch forces DLL calibration analog circuits to always be powered on. 0 = After VREG calibration, some analog circuits are powered down. 1 = Override auto power down, keeping analog calibration circuits active.

Register Name	DP16 DLL VREG Control 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_VREG_CONTROL1_P0_[n]
Address	8000002B0701103F (SCOM), +0x0400_0000_0000
Description	This register controls the voltage regulator of the DLL calibration logic. CAUTION: This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	RXREG_VREG_COMPCON_DC: This field affects the compensation capacitor for the regulator. Contact your IBM representative for details.
51	RW	Reserved.
52	RW	RXREG_VREG_DAC_PULLUP_DC: This is a mode switch for the regulator. It is typically not changed.
53:55	RW	RXREG_VREG_DRVCON_DC: This field determines the PFET size for the regulator. It is a mode switch that is typically not changed.
56:58	RW	RXREG_VREG_REF_SEL_DC: This field adjusts the target value of VREG for VREG calibration. The lowest value (b000) corresponds to the highest VREG target. The highest value (b111) corresponds to the lowest VREG target. The recommended value is b011.
59	RW	REGS_RXDLL_COARSE_ADJ_BY0: Typically, the transition from coarse to fine calibration decrements the code by 1. Therefore, fine calibration always tries to increase the delay by lowering VREG. Sometimes, however, the typical calibration routine produces a less ideal setting. When set, this bit does not decrement the code. Therefore, fine calibration tries to decrease the delay by increasing VREG. 0 = This bit has no effect. 1 = Do not decrement the coarse code during the transition from coarse to fine calibration. Note: This bit takes priority over REGS_RXDLL_COARSE_ADJ_BY2 if both are set.
60:61	RO	Reserved.
62	RW	DLL_DRVREN_MODE: This bit selects which method is used to control DLL output driver disabling. 0 = POWER8 mode (thermometer style, enabling all drivers up to the one that is used). 1 = POWER9 mode (a sliding group of four drivers enabled).

Bits	SCOM	Field Mnemonic: Description
63	RW	DLL_CAL_CKTS_ACTIVE: This mode switch forces DLL calibration analog circuits to always be powered on. 0 = After VREG calibration, some analog circuits are powered down. 1 = Override auto power down, keeping analog calibration circuits active.

Register Name	DP16 DLL VREG Control 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_VREG_CONTROL1_P1_[n]
Address	8000002B0701143F (SCOM), +0x0400_0000_0000
Description	This register controls the voltage regulator of the DLL calibration logic. CAUTION: This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	RXREG_VREG_COMPCON_DC: This field affects the compensation capacitor for the regulator. Contact your IBM representative for details.
51	RW	Reserved.
52	RW	RXREG_VREG_DAC_PULLUP_DC: This is a mode switch for the regulator. It is typically not changed.
53:55	RW	RXREG_VREG_DRVCON_DC: This field determines the PFET size for the regulator. It is a mode switch that is typically not changed.
56:58	RW	RXREG_VREG_REF_SEL_DC: This field adjusts the target value of VREG for VREG calibration. The lowest value (b000) corresponds to the highest VREG target. The highest value (b111) corresponds to the lowest VREG target. The recommended value is b011.
59	RW	REGS_RXDLL_COARSE_ADJ_BY0: Typically, the transition from coarse to fine calibration decrements the code by 1. Therefore, fine calibration always tries to increase the delay by lowering VREG. Sometimes, however, the typical calibration routine produces a less ideal setting. When set, this bit does not decrement the code. Therefore, fine calibration tries to decrease the delay by increasing VREG. 0 = This bit has no effect. 1 = Do not decrement the coarse code during the transition from coarse to fine calibration. Note: This bit takes priority over REGS_RXDLL_COARSE_ADJ_BY2 if both are set.
60:61	RO	Reserved.
62	RW	DLL_DRVREN_MODE: This bit selects which method is used to control DLL output driver disabling. 0 = POWER8 mode (thermometer style, enabling all drivers up to the one that is used). 1 = POWER9 mode (a sliding group of four drivers enabled).
63	RW	DLL_CAL_CKTS_ACTIVE: This mode switch forces DLL calibration analog circuits to always be powered on. 0 = After VREG calibration, some analog circuits are powered down. 1 = Override auto power down, keeping analog calibration circuits active.

Register Name	DP16 DLL VREG Control 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_VREG_CONTROL1_P2_[n]
Address	8000002B0701183F (SCOM), +0x0400_0000_0000
Description	This register controls the voltage regulator of the DLL calibration logic. CAUTION: This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	RXREG_VREG_COMPCON_DC: This field affects the compensation capacitor for the regulator. Contact your IBM representative for details.

Bits	SCOM	Field Mnemonic: Description
51	RW	Reserved.
52	RW	RXREG_VREG_DAC_PULLUP_DC: This is a mode switch for the regulator. It is typically not changed.
53:55	RW	RXREG_VREG_DRVCON_DC: This field determines the PFET size for the regulator. It is a mode switch that is typically not changed.
56:58	RW	RXREG_VREG_REF_SEL_DC: This field adjusts the target value of VREG for VREG calibration. The lowest value (b000) corresponds to the highest VREG target. The highest value (b111) corresponds to the lowest VREG target. The recommended value is b011.
59	RW	REGS_RXDLL_COARSE_ADJ_BY0: Typically, the transition from coarse to fine calibration decrements the code by 1. Therefore, fine calibration always tries to increase the delay by lowering VREG. Sometimes, however, the typical calibration routine produces a less ideal setting. When set, this bit does not decrement the code. Therefore, fine calibration tries to decrease the delay by increasing VREG. 0 = This bit has no effect. 1 = Do not decrement the coarse code during the transition from coarse to fine calibration. Note: This bit takes priority over REGS_RXDLL_COARSE_ADJ_BY2 if both are set.
60:61	RO	Reserved.
62	RW	DLL_DRVREN_MODE: This bit selects which method is used to control DLL output driver disabling. 0 = POWER8 mode (thermometer style, enabling all drivers up to the one that is used). 1 = POWER9 mode (a sliding group of four drivers enabled).
63	RW	DLL_CAL_CKTS_ACTIVE: This mode switch forces DLL calibration analog circuits to always be powered on. 0 = After VREG calibration, some analog circuits are powered down. 1 = Override auto power down, keeping analog calibration circuits active.

Register Name	DP16 DLL VREG Control 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_VREG_CONTROL1_P3_[n]
Address	8000002B07011C3F (SCOM), +0x0400_0000_0000
Description	This register controls the voltage regulator of the DLL calibration logic. CAUTION: This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:50	RW	RXREG_VREG_COMPCON_DC: This field affects the compensation capacitor for the regulator. Contact your IBM representative for details.
51	RW	Reserved.
52	RW	RXREG_VREG_DAC_PULLUP_DC: This is a mode switch for the regulator. It is typically not changed.
53:55	RW	RXREG_VREG_DRVCON_DC: This field determines the PFET size for the regulator. It is a mode switch that is typically not changed.
56:58	RW	RXREG_VREG_REF_SEL_DC: This field adjusts the target value of VREG for VREG calibration. The lowest value (b000) corresponds to the highest VREG target. The highest value (b111) corresponds to the lowest VREG target. The recommended value is b011.
59	RW	REGS_RXDLL_COARSE_ADJ_BY0: Typically, the transition from coarse to fine calibration decrements the code by 1. Therefore, fine calibration always tries to increase the delay by lowering VREG. Sometimes, however, the typical calibration routine produces a less ideal setting. When set, this bit does not decrement the code. Therefore, fine calibration tries to decrease the delay by increasing VREG. 0 = This bit has no effect. 1 = Do not decrement the coarse code during the transition from coarse to fine calibration. Note: This bit takes priority over REGS_RXDLL_COARSE_ADJ_BY2 if both are set.
60:61	RO	Reserved.

Bits	SCOM	Field Mnemonic: Description
62	RW	DLL_DRVREN_MODE: This bit selects which method is used to control DLL output driver disabling. 0 = POWER8 mode (thermometer style, enabling all drivers up to the one that is used). 1 = POWER9 mode (a sliding group of four drivers enabled).
63	RW	DLL_CAL_CKTS_ACTIVE: This mode switch forces DLL calibration analog circuits to always be powered on. 0 = After VREG calibration, some analog circuits are powered down. 1 = Override auto power down, keeping analog calibration circuits active.

Register Name	**DP16 DLL VREG Coarse 0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DLL_VREG_COARSE0_P0_[n]
Address	8000002C0701103F (SCOM), +0x0400_0000_0000
Description	This register controls the coarse calibration of DLL calibration logic. CAUTION: This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48:53	RWX	REGS_RXDLL_COARSE_EN: This field adjusts the delay of each element in the delay line. The larger the code, the larger the delay. Usually, software reads this register at the end of coarse calibration to see where the setting ended up. However, under special situations (that is, lab testing), it can be written to force a specific delay. Note: The POWER9 version of analog DLL only uses 5 bits (48:52). Thus, only the lowest 5 bits of this register (49:53) are connected. Bit 48 exists in the digital logic, but is left unconnected at the digital/analog boundary.
54:55	RO	Constant = 0b00
56:62	RWX	REGS_RXDLL_VREG_DAC_COARSE: This field adjusts the value of VREG during VREG calibration. The smallest code (b0000000) produces the highest VREG voltage. The largest code (b1111111) produces the lowest VREG voltage. Usually, software reads this register at the end of VREG calibration to see where the setting ended up. However, under special situations (that is, lab testing), it can be written to force a VREG value.
63	RO	Constant = 0b0

Register Name	**DP16 DLL VREG Coarse 0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DLL_VREG_COARSE0_P1_[n]
Address	8000002C0701143F (SCOM), +0x0400_0000_0000
Description	This register controls the coarse calibration of DLL calibration logic. CAUTION: This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48:53	RWX	REGS_RXDLL_COARSE_EN: This field adjusts the delay of each element in the delay line. The larger the code, the larger the delay. Usually, software reads this register at the end of coarse calibration to see where the setting ended up. However, under special situations (that is, lab testing), it can be written to force a specific delay. Note: The POWER9 version of analog DLL only uses 5 bits (48:52). Thus, only the lowest 5 bits of this register (49:53) are connected. Bit 48 exists in the digital logic, but is left unconnected at the digital/analog boundary.
54:55	RO	Constant = 0b00

Bits	SCOM	Field Mnemonic: Description
56:62	RWX	REGS_RXDLL_VREG_DAC_COARSE: This field adjusts the value of VREG during VREG calibration. The smallest code (b0000000) produces the highest VREG voltage. The largest code (b1111111) produces the lowest VREG voltage. Usually, software reads this register at the end of VREG calibration to see where the setting ended up. However, under special situations (that is, lab testing), it can be written to force a VREG value.
63	RO	Constant = 0b0

Register Name	**DP16 DLL VREG Coarse 0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DLL_VREG_COARSE0_P2_[n]
Address	8000002C0701183F (SCOM), +0x0400_0000_0000
Description	This register controls the coarse calibration of DLL calibration logic. CAUTION: This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:53	RWX	REGS_RXDLL_COARSE_EN: This field adjusts the delay of each element in the delay line. The larger the code, the larger the delay. Usually, software reads this register at the end of coarse calibration to see where the setting ended up. However, under special situations (that is, lab testing), it can be written to force a specific delay. Note: The POWER9 version of analog DLL only uses 5 bits (48:52). Thus, only the lowest 5 bits of this register (49:53) are connected. Bit 48 exists in the digital logic, but is left unconnected at the digital/analog boundary.
54:55	RO	Constant = 0b00
56:62	RWX	REGS_RXDLL_VREG_DAC_COARSE: This field adjusts the value of VREG during VREG calibration. The smallest code (b0000000) produces the highest VREG voltage. The largest code (b1111111) produces the lowest VREG voltage. Usually, software reads this register at the end of VREG calibration to see where the setting ended up. However, under special situations (that is, lab testing), it can be written to force a VREG value.
63	RO	Constant = 0b0

Register Name	**DP16 DLL VREG Coarse 0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DLL_VREG_COARSE0_P3_[n]
Address	8000002C07011C3F (SCOM), +0x0400_0000_0000
Description	This register controls the coarse calibration of DLL calibration logic. CAUTION: This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:53	RWX	REGS_RXDLL_COARSE_EN: This field adjusts the delay of each element in the delay line. The larger the code, the larger the delay. Usually, software reads this register at the end of coarse calibration to see where the setting ended up. However, under special situations (that is, lab testing), it can be written to force a specific delay. Note: The POWER9 version of analog DLL only uses 5 bits (48:52). Thus, only the lowest 5 bits of this register (49:53) are connected. Bit 48 exists in the digital logic, but is left unconnected at the digital/analog boundary.
54:55	RO	Constant = 0b00

Bits	SCOM	Field Mnemonic: Description
56:62	RWX	REGS_RXDLL_VREG_DAC_COARSE: This field adjusts the value of VREG during VREG calibration. The smallest code (b0000000) produces the highest VREG voltage. The largest code (b1111111) produces the lowest VREG voltage. Usually, software reads this register at the end of VREG calibration to see where the setting ended up. However, under special situations (that is, lab testing), it can be written to force a VREG value.
63	RO	Constant = 0b0

Register Name	**DP16 DLL VREG Coarse 1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DLL_VREG_COARSE1_P0_[n]
Address	8000002D0701103F (SCOM), +0x0400_0000_0000
Description	This register controls the coarse calibration of DLL calibration logic. CAUTION: This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48:53	RWX	REGS_RXDLL_COARSE_EN: This field adjusts the delay of each element in the delay line. The larger the code, the larger the delay. Usually, software reads this register at the end of coarse calibration to see where the setting ended up. However, under special situations (that is, lab testing), it can be written to force a specific delay. Note: The POWER9 version of analog DLL only uses 5 bits (48:52). Thus, only the lowest 5 bits of this register (49:53) are connected. Bit 48 exists in the digital logic, but is left unconnected at the digital/analog boundary.
54:55	RO	Constant = 0b00
56:62	RWX	REGS_RXDLL_VREG_DAC_COARSE: This field adjusts the value of VREG during VREG calibration. The smallest code (b0000000) produces the highest VREG voltage. The largest code (b1111111) produces the lowest VREG voltage. Usually, software reads this register at the end of VREG calibration to see where the setting ended up. However, under special situations (that is, lab testing), it can be written to force a VREG value.
63	RO	Constant = 0b0

Register Name	**DP16 DLL VREG Coarse 1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DLL_VREG_COARSE1_P1_[n]
Address	8000002D0701143F (SCOM), +0x0400_0000_0000
Description	This register controls the coarse calibration of DLL calibration logic. CAUTION: This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48:53	RWX	REGS_RXDLL_COARSE_EN: This field adjusts the delay of each element in the delay line. The larger the code, the larger the delay. Usually, software reads this register at the end of coarse calibration to see where the setting ended up. However, under special situations (that is, lab testing), it can be written to force a specific delay. Note: The POWER9 version of analog DLL only uses 5 bits (48:52). Thus, only the lowest 5 bits of this register (49:53) are connected. Bit 48 exists in the digital logic, but is left unconnected at the digital/analog boundary.
54:55	RO	Constant = 0b00

Bits	SCOM	Field Mnemonic: Description
56:62	RWX	REGS_RXDLL_VREG_DAC_COARSE: This field adjusts the value of VREG during VREG calibration. The smallest code (b0000000) produces the highest VREG voltage. The largest code (b1111111) produces the lowest VREG voltage. Usually, software reads this register at the end of VREG calibration to see where the setting ended up. However, under special situations (that is, lab testing), it can be written to force a VREG value.
63	RO	Constant = 0b0

Register Name	**DP16 DLL VREG Coarse 1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DLL_VREG_COARSE1_P2_[n]
Address	8000002D0701183F (SCOM), +0x0400_0000_0000
Description	This register controls the coarse calibration of DLL calibration logic. CAUTION: This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:53	RWX	REGS_RXDLL_COARSE_EN: This field adjusts the delay of each element in the delay line. The larger the code, the larger the delay. Usually, software reads this register at the end of coarse calibration to see where the setting ended up. However, under special situations (that is, lab testing), it can be written to force a specific delay. Note: The POWER9 version of analog DLL only uses 5 bits (48:52). Thus, only the lowest 5 bits of this register (49:53) are connected. Bit 48 exists in the digital logic, but is left unconnected at the digital/analog boundary.
54:55	RO	Constant = 0b00
56:62	RWX	REGS_RXDLL_VREG_DAC_COARSE: This field adjusts the value of VREG during VREG calibration. The smallest code (b0000000) produces the highest VREG voltage. The largest code (b1111111) produces the lowest VREG voltage. Usually, software reads this register at the end of VREG calibration to see where the setting ended up. However, under special situations (that is, lab testing), it can be written to force a VREG value.
63	RO	Constant = 0b0

Register Name	**DP16 DLL VREG Coarse 1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DLL_VREG_COARSE1_P3_[n]
Address	8000002D07011C3F (SCOM), +0x0400_0000_0000
Description	This register controls the coarse calibration of DLL calibration logic. CAUTION: This register must not be written while hardware calibration is active.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:53	RWX	REGS_RXDLL_COARSE_EN: This field adjusts the delay of each element in the delay line. The larger the code, the larger the delay. Usually, software reads this register at the end of coarse calibration to see where the setting ended up. However, under special situations (that is, lab testing), it can be written to force a specific delay. Note: The POWER9 version of analog DLL only uses 5 bits (48:52). Thus, only the lowest 5 bits of this register (49:53) are connected. Bit 48 exists in the digital logic, but is left unconnected at the digital/analog boundary.
54:55	RO	Constant = 0b00

Bits	SCOM	Field Mnemonic: Description
56:62	RWX	REGS_RXDLL_VREG_DAC_COARSE: This field adjusts the value of VREG during VREG calibration. The smallest code (b0000000) produces the highest VREG voltage. The largest code (b1111111) produces the lowest VREG voltage. Usually, software reads this register at the end of VREG calibration to see where the setting ended up. However, under special situations (that is, lab testing), it can be written to force a VREG value.
63	RO	Constant = 0b0

Register Name	DP16 Write VREF Status 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_STATUS0_P0_[n]
Address	8000002E0701103F (SCOM), +0x0400_0000_0000
Description	This register reports information about the write VREF operation.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	WR_CTR_NUM_WRRDREQ_CNT: This field counts the number of full-loop iterations used in the 1-dimensional (1D) algorithm.

Register Name	DP16 Write VREF Status 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_STATUS0_P1_[n]
Address	8000002E0701143F (SCOM), +0x0400_0000_0000
Description	This register reports information about the write VREF operation.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	WR_CTR_NUM_WRRDREQ_CNT: This field counts the number of full-loop iterations used in the 1D algorithm.

Register Name	DP16 Write VREF Status 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_STATUS0_P2_[n]
Address	8000002E0701183F (SCOM), +0x0400_0000_0000
Description	This register reports information about the write VREF operation.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	WR_CTR_NUM_WRRDREQ_CNT: This field counts the number of full-loop iterations used in the 1D algorithm.

Register Name	DP16 Write VREF Status 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_STATUS0_P3_[n]
Address	8000002E07011C3F (SCOM), +0x0400_0000_0000
Description	This register reports information about the write VREF operation.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	WR_CTR_NUM_WRRDREQ_CNT: This field counts the number of full-loop iterations used in the 1D algorithm.

Register Name	DP16 Write VREF Status 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_STATUS1_P0_[n]
Address	8000002F0701103F (SCOM), +0x0400_0000_0000
Description	This register reports additional information about the write VREF operation.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:56	RW	WR_CTR_NUM_VREFREQ_CNT: This field counts the number of VREF update requests that have been called.
57:63	RW	WR_CTR_CUR_VREF: This field contains the current VREF.

Register Name	DP16 Write VREF Status 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_STATUS1_P1_[n]
Address	8000002F0701143F (SCOM), +0x0400_0000_0000
Description	This register reports additional information about the write VREF operation.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:56	RW	WR_CTR_NUM_VREFREQ_CNT: This field counts the number of VREF update requests that have been called.
57:63	RW	WR_CTR_CUR_VREF: This field contains the current VREF.

Register Name	DP16 Write VREF Status 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_STATUS1_P2_[n]
Address	8000002F0701183F (SCOM), +0x0400_0000_0000
Description	This register reports additional information about the write VREF operation.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:56	RW	WR_CTR_NUM_VREFREQ_CNT: This field counts the number of VREF update requests that have been called.
57:63	RW	WR_CTR_CUR_VREF: This field contains the current VREF.

Register Name	DP16 Write VREF Status 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_STATUS1_P3_[n]
Address	8000002F07011C3F (SCOM), +0x0400_0000_0000
Description	This register reports additional information about the write VREF operation.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:56	RW	WR_CTR_NUM_VREFREQ_CNT: This field counts the number of VREF update requests that have been called.
57:63	RW	WR_CTR_CUR_VREF: This field contains the current VREF.

Register Name	DP16 DQSClk Phase Rotator Value 0 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQSCLK_PR0_RANK_PAIR0_P0_[n]
Address	800000300701103F (SCOM), +0x0400_0000_0000
Description	Two phase rotator values are contained within each register. Two registers exist for each rank pair. These phase rotator values are the values needed to align the internal SysClk to the incoming DQS strobe for each group of data pins.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000000
49:55	RW	DQSCLK_ROT_CLK_N0: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD00B – MEMINTD03B in register 0 and MEMINTD08B – MEMINTD11B in register 1. This value is updated by hardware.
56	RO	Constant = 0b0
57:63	RW	DQSCLK_ROT_CLK_N1: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINTD15B in register 1. This value is updated by hardware.

Register Name	DP16 DQSClk Phase Rotator Value 0 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQSCLK_PR0_RANK_PAIR0_P1_[n]
Address	800000300701143F (SCOM), +0x0400_0000_0000
Description	Two phase rotator values are contained within each register. Two registers exist for each rank pair. These phase rotator values are the values needed to align the internal SysClk to the incoming DQS strobe for each group of data pins.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000000
49:55	RW	DQSCLK_ROT_CLK_N0: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD00B – MEMINTD03B in register 0 and MEMINTD08B – MEMINTD11B in register 1. This value is updated by hardware.
56	RO	Constant = 0b0
57:63	RW	DQSCLK_ROT_CLK_N1: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINTD15B in register 1. This value is updated by hardware.

Register Name	DP16 DQSClk Phase Rotator Value 0 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQSCLK_PR0_RANK_PAIR0_P2_[n]
Address	800000300701183F (SCOM), +0x0400_0000_0000
Description	Two phase rotator values are contained within each register. Two registers exist for each rank pair. These phase rotator values are the values needed to align the internal SysClk to the incoming DQS strobe for each group of data pins.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	DQSCLK_ROT_CLK_N0: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD00B – MEMINTD03B in register 0 and MEMINTD08B – MEMINTD11B in register 1. This value is updated by hardware.
56	RO	Constant = 0b0
57:63	RW	DQSCLK_ROT_CLK_N1: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINTD15B in register 1. This value is updated by hardware.

Register Name	DP16 DQSClk Phase Rotator Value 0 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQSCLK_PR0_RANK_PAIR0_P3_[n]
Address	8000003007011C3F (SCOM), +0x0400_0000_0000
Description	Two phase rotator values are contained within each register. Two registers exist for each rank pair. These phase rotator values are the values needed to align the internal SysClk to the incoming DQS strobe for each group of data pins.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	DQSCLK_ROT_CLK_N0: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD00B – MEMINTD03B in register 0 and MEMINTD08B – MEMINTD11B in register 1. This value is updated by hardware.
56	RO	Constant = 0b0
57:63	RW	DQSCLK_ROT_CLK_N1: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINTD15B in register 1. This value is updated by hardware.

Register Name	DP16 DQSClk Phase Rotator Value 1 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQSCLK_PR1_RANK_PAIR0_P0_[n]
Address	800000310701103F (SCOM), +0x0400_0000_0000
Description	Two phase rotator values are contained within each register. Two registers exist for each rank pair. These phase rotator values are the values needed to align the internal SysClk to the incoming DQS strobe for each group of data pins.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	DQSCLK_ROT_CLK_N2: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD00B – MEMINTD03B in register 0 and MEMINTD08B – MEMINTD11B in register 1. This value is updated by hardware.

Bits	SCOM	Field Mnemonic: Description
56	RO	Constant = 0b0
57:63	RW	DQSCLK_ROT_CLK_N3: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINTD15B in register 1. This value is updated by hardware.

Register Name	**DP16 DQSClk Phase Rotator Value 1 RP0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQSCLK_PR1_RANK_PAIR0_P1_[n]
Address	800000310701143F (SCOM), +0x0400_0000_0000
Description	Two phase rotator values are contained within each register. Two registers exist for each rank pair. These phase rotator values are the values needed to align the internal SysClk to the incoming DQS strobe for each group of data pins.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	DQSCLK_ROT_CLK_N2: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD00B – MEMINTD03B in register 0 and MEMINTD08B – MEMINTD11B in register 1. This value is updated by hardware.
56	RO	Constant = 0b0
57:63	RW	DQSCLK_ROT_CLK_N3: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINTD15B in register 1. This value is updated by hardware.

Register Name	**DP16 DQSClk Phase Rotator Value 1 RP0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQSCLK_PR1_RANK_PAIR0_P2_[n]
Address	800000310701183F (SCOM), +0x0400_0000_0000
Description	Two phase rotator values are contained within each register. Two registers exist for each rank pair. These phase rotator values are the values needed to align the internal SysClk to the incoming DQS strobe for each group of data pins.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	DQSCLK_ROT_CLK_N2: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD00B – MEMINTD03B in register 0 and MEMINTD08B – MEMINTD11B in register 1. This value is updated by hardware.
56	RO	Constant = 0b0
57:63	RW	DQSCLK_ROT_CLK_N3: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINTD15B in register 1. This value is updated by hardware.

Register Name	DP16 DQSClk Phase Rotator Value 1 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQSCLK_PR1_RANK_PAIR0_P3_[n]
Address	8000003107011C3F (SCOM), +0x0400_0000_0000
Description	Two phase rotator values are contained within each register. Two registers exist for each rank pair. These phase rotator values are the values needed to align the internal SysClk to the incoming DQS strobe for each group of data pins.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	DQSCLK_ROT_CLK_N2: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD00B – MEMINTD03B in register 0 and MEMINTD08B – MEMINTD11B in register 1. This value is updated by hardware.
56	RO	Constant = 0b0
57:63	RW	DQSCLK_ROT_CLK_N3: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINTD15B in register 1. This value is updated by hardware.

Register Name	DP16 Pattern Position 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_PATTERN_POS_0_P0_[n]
Address	800000320701103F (SCOM), +0x0400_0000_0000
Description	This register sets the relative position of data pins for calibration algorithms using custom patterns that use the reserved memory location. A position value of 00b indicates that the corresponding data pin is compared against SEQ Read/Write Data 0 bits 0 - 7 on the first 8 beats of data and rolls through the other SEQ Read/Write Data bits in order. A position value of 01b starts with SEQ Read/Write Data 0 bits 8 - 15. A position value of 10b starts with SEQ Read/Write Data 1 bits 0 - 7. A position value of 11b starts with SEQ Read/Write Data 1 bits 8 - 15. This register is typically set to 1B1Bh for custom write centering. The register is unused for custom read centering.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:49	RW	MEMINTD00_POS: MEMINTD00 pattern starting position.
50:51	RW	MEMINTD01_POS: MEMINTD01 pattern starting position.
52:53	RW	MEMINTD02_POS: MEMINTD02 pattern starting position.
54:55	RW	MEMINTD03_POS: MEMINTD03 pattern starting position.
56:57	RW	MEMINTD04_POS: MEMINTD04 pattern starting position.
58:59	RW	MEMINTD05_POS: MEMINTD05 pattern starting position.
60:61	RW	MEMINTD06_POS: MEMINTD06 pattern starting position.
62:63	RW	MEMINTD07_POS: MEMINTD07 pattern starting position.

Register Name	DP16 Pattern Position 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_PATTERN_POS_0_P1_[n]
Address	800000320701143F (SCOM), +0x0400_0000_0000
Description	This register sets the relative position of data pins for calibration algorithms using custom patterns that use the reserved memory location. A position value of 00b indicates that the corresponding data pin is compared against SEQ Read/Write Data 0 bits 0 - 7 on the first 8 beats of data and rolls through the other SEQ Read/Write Data bits in order. A position value of 01b starts with SEQ Read/Write Data 0 bits 8 - 15. A position value of 10b starts with SEQ Read/Write Data 1 bits 0 - 7. A position value of 11b starts with SEQ Read/Write Data 1 bits 8 - 15. This register is typically set to 1B1Bh for custom write centering. The register is unused for custom read centering.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:49	RW	MEMINTD00_POS: MEMINTD00 pattern starting position.
50:51	RW	MEMINTD01_POS: MEMINTD01 pattern starting position.
52:53	RW	MEMINTD02_POS: MEMINTD02 pattern starting position.
54:55	RW	MEMINTD03_POS: MEMINTD03 pattern starting position.
56:57	RW	MEMINTD04_POS: MEMINTD04 pattern starting position.
58:59	RW	MEMINTD05_POS: MEMINTD05 pattern starting position.
60:61	RW	MEMINTD06_POS: MEMINTD06 pattern starting position.
62:63	RW	MEMINTD07_POS: MEMINTD07 pattern starting position.

Register Name	DP16 Pattern Position 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_PATTERN_POS_0_P2_[n]
Address	800000320701183F (SCOM), +0x0400_0000_0000
Description	This register sets the relative position of data pins for calibration algorithms using custom patterns that use the reserved memory location. A position value of 00b indicates that the corresponding data pin is compared against SEQ Read/Write Data 0 bits 0 - 7 on the first 8 beats of data and rolls through the other SEQ Read/Write Data bits in order. A position value of 01b starts with SEQ Read/Write Data 0 bits 8 - 15. A position value of 10b starts with SEQ Read/Write Data 1 bits 0 - 7. A position value of 11b starts with SEQ Read/Write Data 1 bits 8 - 15. This register is typically set to 1B1Bh for custom write centering. The register is unused for custom read centering.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:49	RW	MEMINTD00_POS: MEMINTD00 pattern starting position.
50:51	RW	MEMINTD01_POS: MEMINTD01 pattern starting position.
52:53	RW	MEMINTD02_POS: MEMINTD02 pattern starting position.
54:55	RW	MEMINTD03_POS: MEMINTD03 pattern starting position.
56:57	RW	MEMINTD04_POS: MEMINTD04 pattern starting position.
58:59	RW	MEMINTD05_POS: MEMINTD05 pattern starting position.
60:61	RW	MEMINTD06_POS: MEMINTD06 pattern starting position.
62:63	RW	MEMINTD07_POS: MEMINTD07 pattern starting position.

Register Name	DP16 Pattern Position 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_PATTERN_POS_0_P3_[n]
Address	8000003207011C3F (SCOM), +0x0400_0000_0000
Description	This register sets the relative position of data pins for calibration algorithms using custom patterns that use the reserved memory location. A position value of 00b indicates that the corresponding data pin is compared against SEQ Read/Write Data 0 bits 0 - 7 on the first 8 beats of data and rolls through the other SEQ Read/Write Data bits in order. A position value of 01b starts with SEQ Read/Write Data 0 bits 8 - 15. A position value of 10b starts with SEQ Read/Write Data 1 bits 0 - 7. A position value of 11b starts with SEQ Read/Write Data 1 bits 8 - 15. This register is typically set to 1B1Bh for custom write centering. The register is unused for custom read centering.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:49	RW	MEMINTD00_POS: MEMINTD00 pattern starting position.
50:51	RW	MEMINTD01_POS: MEMINTD01 pattern starting position.
52:53	RW	MEMINTD02_POS: MEMINTD02 pattern starting position.
54:55	RW	MEMINTD03_POS: MEMINTD03 pattern starting position.
56:57	RW	MEMINTD04_POS: MEMINTD04 pattern starting position.
58:59	RW	MEMINTD05_POS: MEMINTD05 pattern starting position.
60:61	RW	MEMINTD06_POS: MEMINTD06 pattern starting position.
62:63	RW	MEMINTD07_POS: MEMINTD07 pattern starting position.

Register Name	DP16 Pattern Position 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_PATTERN_POS_1_P0_[n]
Address	800000330701103F (SCOM), +0x0400_0000_0000
Description	This register sets the relative position of data pins for calibration algorithms using custom patterns that use the reserved memory location. A position value of 00b indicates that the corresponding data pin is compared against SEQ Read/Write Data 0 bits 0 - 7 on the first 8 beats of data and rolls through the other SEQ Read/Write Data bits in order. A position value of 01b starts with SEQ Read/Write Data 0 bits 8 - 15. A position value of 10b starts with SEQ Read/Write Data 1 bits 0 - 7. A position value of 11b starts with SEQ Read/Write Data 1 bits 8 - 15. This register is typically set to 1B1Bh for custom write centering. The register is unused for custom read centering.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:49	RW	MEMINTD08_POS: MEMINTD08 pattern starting position.
50:51	RW	MEMINTD09_POS: MEMINTD09 pattern starting position.
52:53	RW	MEMINTD10_POS: MEMINTD10 pattern starting position.
54:55	RW	MEMINTD11_POS: MEMINTD11 pattern starting position.
56:57	RW	MEMINTD12_POS: MEMINTD12 pattern starting position.
58:59	RW	MEMINTD13_POS: MEMINTD13 pattern starting position.
60:61	RW	MEMINTD14_POS: MEMINTD14 pattern starting position.
62:63	RW	MEMINTD15_POS: MEMINTD15 pattern starting position.

Register Name	DP16 Pattern Position 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_PATTERN_POS_1_P1_[n]
Address	800000330701143F (SCOM), +0x0400_0000_0000
Description	This register sets the relative position of data pins for calibration algorithms using custom patterns that use the reserved memory location. A position value of 00b indicates that the corresponding data pin is compared against SEQ Read/Write Data 0 bits 0 - 7 on the first 8 beats of data and rolls through the other SEQ Read/Write Data bits in order. A position value of 01b starts with SEQ Read/Write Data 0 bits 8 - 15. A position value of 10b starts with SEQ Read/Write Data 1 bits 0 - 7. A position value of 11b starts with SEQ Read/Write Data 1 bits 8 - 15. This register is typically set to 1B1Bh for custom write centering. The register is unused for custom read centering.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:49	RW	MEMINTD08_POS: MEMINTD08 pattern starting position.
50:51	RW	MEMINTD09_POS: MEMINTD09 pattern starting position.
52:53	RW	MEMINTD10_POS: MEMINTD10 pattern starting position.
54:55	RW	MEMINTD11_POS: MEMINTD11 pattern starting position.
56:57	RW	MEMINTD12_POS: MEMINTD12 pattern starting position.
58:59	RW	MEMINTD13_POS: MEMINTD13 pattern starting position.
60:61	RW	MEMINTD14_POS: MEMINTD14 pattern starting position.
62:63	RW	MEMINTD15_POS: MEMINTD15 pattern starting position.

Register Name	DP16 Pattern Position 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_PATTERN_POS_1_P2_[n]
Address	800000330701183F (SCOM), +0x0400_0000_0000
Description	This register sets the relative position of data pins for calibration algorithms using custom patterns that use the reserved memory location. A position value of 00b indicates that the corresponding data pin is compared against SEQ Read/Write Data 0 bits 0 - 7 on the first 8 beats of data and rolls through the other SEQ Read/Write Data bits in order. A position value of 01b starts with SEQ Read/Write Data 0 bits 8 - 15. A position value of 10b starts with SEQ Read/Write Data 1 bits 0 - 7. A position value of 11b starts with SEQ Read/Write Data 1 bits 8 - 15. This register is typically set to 1B1Bh for custom write centering. The register is unused for custom read centering.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:49	RW	MEMINTD08_POS: MEMINTD08 pattern starting position.
50:51	RW	MEMINTD09_POS: MEMINTD09 pattern starting position.
52:53	RW	MEMINTD10_POS: MEMINTD10 pattern starting position.
54:55	RW	MEMINTD11_POS: MEMINTD11 pattern starting position.
56:57	RW	MEMINTD12_POS: MEMINTD12 pattern starting position.
58:59	RW	MEMINTD13_POS: MEMINTD13 pattern starting position.
60:61	RW	MEMINTD14_POS: MEMINTD14 pattern starting position.
62:63	RW	MEMINTD15_POS: MEMINTD15 pattern starting position.

Register Name	DP16 Pattern Position 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_PATTERN_POS_1_P3_[n]
Address	8000003307011C3F (SCOM), +0x0400_0000_0000
Description	This register sets the relative position of data pins for calibration algorithms using custom patterns that use the reserved memory location. A position value of 00b indicates that the corresponding data pin is compared against SEQ Read/Write Data 0 bits 0 - 7 on the first 8 beats of data and rolls through the other SEQ Read/Write Data bits in order. A position value of 01b starts with SEQ Read/Write Data 0 bits 8 - 15. A position value of 10b starts with SEQ Read/Write Data 1 bits 0 - 7. A position value of 11b starts with SEQ Read/Write Data 1 bits 8 - 15. This register is typically set to 1B1Bh for custom write centering. The register is unused for custom read centering.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:49	RW	MEMINTD08_POS: MEMINTD08 pattern starting position.
50:51	RW	MEMINTD09_POS: MEMINTD09 pattern starting position.
52:53	RW	MEMINTD10_POS: MEMINTD10 pattern starting position.
54:55	RW	MEMINTD11_POS: MEMINTD11 pattern starting position.
56:57	RW	MEMINTD12_POS: MEMINTD12 pattern starting position.
58:59	RW	MEMINTD13_POS: MEMINTD13 pattern starting position.
60:61	RW	MEMINTD14_POS: MEMINTD14 pattern starting position.
62:63	RW	MEMINTD15_POS: MEMINTD15 pattern starting position.

Register Name	DP16 Read Diagnostic Configuration 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_DIA_CONFIG1_P0_[n]
Address	800000350701103F (SCOM), +0x0400_0000_0000
Description	This register is used for the diagnosis and characterization of the read function within the DP16.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:52	ROX	DQS_ALIGN_SM: This field indicates the state of the DQS alignment state machine.
53:56	ROX	DQS_ALIGN_CNTR: This field is a generic counter for the DQS alignment state machine.
57:63	ROX	ITERATION_CNTR: This field is an iteration count indicator.

Register Name	DP16 Read Diagnostic Configuration 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_DIA_CONFIG1_P1_[n]
Address	800000350701143F (SCOM), +0x0400_0000_0000
Description	This register is used for the diagnosis and characterization of the read function within the DP16.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:52	ROX	DQS_ALIGN_SM: This field indicates the state of the DQS alignment state machine.
53:56	ROX	DQS_ALIGN_CNTR: This field is a generic counter for the DQS alignment state machine.

Bits	SCOM	Field Mnemonic: Description
57:63	ROX	ITERATION_CNTR: This field is an iteration count indicator.

Register Name	DP16 Read Diagnostic Configuration 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_DIA_CONFIG1_P2_[n]
Address	800000350701183F (SCOM), +0x0400_0000_0000
Description	This register is used for the diagnosis and characterization of the read function within the DP16.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:52	ROX	DQS_ALIGN_SM: This field indicates the state of the DQS alignment state machine.
53:56	ROX	DQS_ALIGN_CNTR: This field is a generic counter for the DQS alignment state machine.
57:63	ROX	ITERATION_CNTR: This field is an iteration count indicator.

Register Name	DP16 Read Diagnostic Configuration 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_DIA_CONFIG1_P3_[n]
Address	8000003507011C3F (SCOM), +0x0400_0000_0000
Description	This register is used for the diagnosis and characterization of the read function within the DP16.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:52	ROX	DQS_ALIGN_SM: This field indicates the state of the DQS alignment state machine.
53:56	ROX	DQS_ALIGN_CNTR: This field is a generic counter for the DQS alignment state machine.
57:63	ROX	ITERATION_CNTR: This field is an iteration count indicator.

Register Name	DP16 Read Diagnostic Configuration 2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_DIA_CONFIG2_P0_[n]
Address	800000360701103F (SCOM), +0x0400_0000_0000
Description	This register is used for the diagnosis, characterization, and control of the read function within the DP16. Contact your IBM representative before changing the value of this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:50	ROX	CALIBRATE_BIT: This is the current bit, 0 to 3, of the quadrant undergoing calibration (read only).
51:52	ROX	DQS_ALIGN_QUAD: This is the current quadrant undergoing DQS alignment (read only).
53:55	ROX	DQS_QUAD_CONFIG: DQS quadrant configuration (read only).
56:59	ROX	OPERATE_MODE: DP16 operating mode as generated by the RC (read only).
60	RWX	EN_DQS_OFFSET: Enable DQS offset.
61	RWX	DQS_ALIGN_JITTER: Increase DQS alignment jitter noise immunity.
62	RWX	DIS_CLK_GATE: Disable clock gating of DQS-alignment-related latches.

Bits	SCOM	Field Mnemonic: Description
63	RWX	MAX_DQS_ITER: Force the maximum DQS alignment iteration count.

Register Name	DP16 Read Diagnostic Configuration 2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_DIA_CONFIG2_P1_[n]
Address	800000360701143F (SCOM), +0x0400_0000_0000
Description	This register is used for the diagnosis, characterization, and control of the read function within the DP16. Contact your IBM representative before changing the value of this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:50	ROX	CALIBRATE_BIT: This is the current bit, 0 to 3, of the quadrant undergoing calibration (read only).
51:52	ROX	DQS_ALIGN_QUAD: This is the current quadrant undergoing DQS alignment (read only).
53:55	ROX	DQS_QUAD_CONFIG: DQS quadrant configuration (read only).
56:59	ROX	OPERATE_MODE: DP16 operating mode as generated by the RC (read only).
60	RWX	EN_DQS_OFFSET: Enable DQS offset.
61	RWX	DQS_ALIGN_JITTER: Increase DQS alignment jitter noise immunity.
62	RWX	DIS_CLK_GATE: Disable clock gating of DQS-alignment-related latches.
63	RWX	MAX_DQS_ITER: Force the maximum DQS alignment iteration count.

Register Name	DP16 Read Diagnostic Configuration 2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_DIA_CONFIG2_P2_[n]
Address	800000360701183F (SCOM), +0x0400_0000_0000
Description	This register is used for the diagnosis, characterization, and control of the read function within the DP16. Contact your IBM representative before changing the value of this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:50	ROX	CALIBRATE_BIT: This is the current bit, 0 to 3, of the quadrant undergoing calibration (read only).
51:52	ROX	DQS_ALIGN_QUAD: This is the current quadrant undergoing DQS alignment (read only).
53:55	ROX	DQS_QUAD_CONFIG: DQS quadrant configuration (read only).
56:59	ROX	OPERATE_MODE: DP16 operating mode as generated by the RC (read only).
60	RWX	EN_DQS_OFFSET: Enable DQS offset.
61	RWX	DQS_ALIGN_JITTER: Increase DQS alignment jitter noise immunity.
62	RWX	DIS_CLK_GATE: Disable clock gating of DQS-alignment-related latches.
63	RWX	MAX_DQS_ITER: Force the maximum DQS alignment iteration count.

Register Name	**DP16 Read Diagnostic Configuration 2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_RD_DIA_CONFIG2_P3_[n]
Address	8000003607011C3F (SCOM), +0x0400_0000_0000
Description	This register is used for the diagnosis, characterization, and control of the read function within the DP16. Contact your IBM representative before changing the value of this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:50	ROX	CALIBRATE_BIT: This is the current bit, 0 to 3, of the quadrant undergoing calibration (read only).
51:52	ROX	DQS_ALIGN_QUAD: This is the current quadrant undergoing DQS alignment (read only).
53:55	ROX	DQS_QUAD_CONFIG: DQS quadrant configuration (read only).
56:59	ROX	OPERATE_MODE: DP16 operating mode as generated by the RC (read only).
60	RWX	EN_DQS_OFFSET: Enable DQS offset.
61	RWX	DQS_ALIGN_JITTER: Increase DQS alignment jitter noise immunity.
62	RWX	DIS_CLK_GATE: Disable clock gating of DQS-alignment-related latches.
63	RWX	MAX_DQS_ITER: Force the maximum DQS alignment iteration count.

Register Name	**DP16 DQSClk Offset Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQSCLK_OFFSET_P0_[n]
Address	800000370701103F (SCOM), +0x0400_0000_0000
Description	This register controls switching to the live DQS.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000000000000
49:55	RW	DQS_OFFSET: This field prevents switching to the live DQS too early or during the calibration routines. Set this field to: DQS_OFFSET = 10 + ceiling(peak_to_peak_jitter_magnitude_in_ticks / 2). or more specifically: DQS_OFFSET= 2 + ceiling(peak_to_peak_jitter_magnitude_in_ticks / 2) + (peak_to_peak_periodic_drift_in_ticks/2) where peak_to_peak_jitter_magnitude_in_ticks is a whole number equal to the read clock strobe (DQS) peak-to-peak jitter rounded up to the nearest 128th memory clock. and peak_to_peak_periodic_drift_in_ticks is the peak-to-peak drift of the read clock strobe (DQS) rounded up to the nearest 128th memory clock. The + 2 term in the equation accounts for the jitter sources within the DDR PHY.
56:63	RO	Constant = 0b00000000

Register Name	**DP16 DQSClk Offset Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQSCLK_OFFSET_P1_[n]
Address	800000370701143F (SCOM), +0x0400_0000_0000
Description	This register controls switching to the live DQS.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	DQS_OFFSET: This field prevents switching to the live DQS too early or during the calibration routines. Set this field to: DQS_OFFSET = 10 + ceiling(peak_to_peak_jitter_magnitude_in_ticks / 2). or more specifically: DQS_OFFSET= 2 + ceiling(peak_to_peak_jitter_magnitude_in_ticks / 2) + (peak_to_peak_periodic_drift_in_ticks/2) where peak_to_peak_jitter_magnitude_in_ticks is a whole number equal to the read clock strobe (DQS) peak-to-peak jitter rounded up to the nearest 128th memory clock. And peak_to_peak_periodic_drift_in_ticks is the peak-to-peak drift of the read clock strobe (DQS) rounded up to the nearest 128th memory clock. The + 2 term in the equation accounts for the jitter sources within the DDR PHY.
56:63	RO	Constant = 0b00000000

Register Name	DP16 DQSClk Offset Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQSCLK_OFFSET_P2_[n]
Address	800000370701183F (SCOM), +0x0400_0000_0000
Description	This register controls switching to the live DQS.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	DQS_OFFSET: This field prevents switching to the live DQS too early or during the calibration routines. Set this field to: DQS_OFFSET = 10 + ceiling(peak_to_peak_jitter_magnitude_in_ticks / 2). or more specifically: DQS_OFFSET= 2 + ceiling(peak_to_peak_jitter_magnitude_in_ticks / 2) + (peak_to_peak_periodic_drift_in_ticks/2) where peak_to_peak_jitter_magnitude_in_ticks is a whole number equal to the read clock strobe (DQS) peak-to-peak jitter rounded up to the nearest 128th memory clock. and peak_to_peak_periodic_drift_in_ticks is the peak-to-peak drift of the read clock strobe (DQS) rounded up to the nearest 128th memory clock. The + 2 term in the equation accounts for the jitter sources within the DDR PHY.
56:63	RO	Constant = 0b00000000

Register Name	DP16 DQSClk Offset Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQSCLK_OFFSET_P3_[n]
Address	8000003707011C3F (SCOM), +0x0400_0000_0000
Description	This register controls switching to the live DQS.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DQS_OFFSET: This field prevents switching to the live DQS too early or during the calibration routines. Set this field to: DQS_OFFSET = 10 + ceiling(peak_to_peak_jitter_magnitude_in_ticks / 2). or more specifically: DQS_OFFSET= 2 + ceiling(peak_to_peak_jitter_magnitude_in_ticks / 2) + (peak_to_peak_periodic_drift_in_ticks/2) where peak_to_peak_jitter_magnitude_in_ticks is a whole number equal to the read clock strobe (DQS) peak-to-peak jitter rounded up to the nearest 128th memory clock. and peak_to_peak_periodic_drift_in_ticks is the peak-to-peak drift of the read clock strobe (DQS) rounded up to the nearest 128th memory clock. The + 2 term in the equation accounts for the jitter sources within the DDR PHY.
56:63	RO	Constant = 0b00000000

Register Name	DP16 Write Delay Value 0 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_0_RP0_REG_P0_[n]
Address	800000380701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 0 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_0_RP0_REG_P1_[n]
Address	800000380701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 0 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_0_RP0_REG_P2_[n]
Address	800000380701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 0 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_0_RP0_REG_P3_[n]
Address	8000003807011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 1 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_1_RP0_REG_P0_[n]
Address	800000390701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 1 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_1_RP0_REG_P1_[n]
Address	800000390701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 1 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_1_RP0_REG_P2_[n]
Address	800000390701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 1 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_1_RP0_REG_P3_[n]
Address	8000003907011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 2 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_2_RP0_REG_P0_[n]
Address	8000003A0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 2 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_2_RP0_REG_P1_[n]
Address	8000003A0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 2 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_2_RP0_REG_P2_[n]
Address	8000003A0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 2 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_2_RP0_REG_P3_[n]
Address	8000003A07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 3 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_3_RP0_REG_P0_[n]
Address	8000003B0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 3 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_3_RP0_REG_P1_[n]
Address	8000003B0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 3 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_3_RP0_REG_P2_[n]
Address	8000003B0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 3 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_3_RP0_REG_P3_[n]
Address	8000003B07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 4 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_4_RP0_REG_P0_[n]
Address	8000003C0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 4 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_4_RP0_REG_P1_[n]
Address	8000003C0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 4 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_4_RP0_REG_P2_[n]
Address	8000003C0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 4 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_4_RP0_REG_P3_[n]
Address	8000003C07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 5 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_5_RP0_REG_P0_[n]
Address	8000003D0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 5 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_5_RP0_REG_P1_[n]
Address	8000003D0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 5 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_5_RP0_REG_P2_[n]
Address	8000003D0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 5 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_5_RP0_REG_P3_[n]
Address	8000003D07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 6 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_6_RP0_REG_P0_[n]
Address	8000003E0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 6 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_6_RP0_REG_P1_[n]
Address	8000003E0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 6 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_6_RP0_REG_P2_[n]
Address	8000003E0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 6 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_6_RP0_REG_P3_[n]
Address	8000003E07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 7 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_7_RP0_REG_P0_[n]
Address	8000003F0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 7 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_7_RP0_REG_P1_[n]
Address	8000003F0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 7 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_7_RP0_REG_P2_[n]
Address	8000003F0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 7 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_7_RP0_REG_P3_[n]
Address	8000003F07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 8 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_8_RP0_REG_P0_[n]
Address	800000400701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 8 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_8_RP0_REG_P1_[n]
Address	800000400701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 8 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_8_RP0_REG_P2_[n]
Address	800000400701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 8 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_8_RP0_REG_P3_[n]
Address	8000004007011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 9 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_9_RP0_REG_P0_[n]
Address	800000410701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 9 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_9_RP0_REG_P1_[n]
Address	800000410701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 9 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_9_RP0_REG_P2_[n]
Address	800000410701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 9 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_9_RP0_REG_P3_[n]
Address	8000004107011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 10 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_10_RP0_REG_P0_[n]
Address	800000420701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 10 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_10_RP0_REG_P1_[n]
Address	800000420701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 10 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_10_RP0_REG_P2_[n]
Address	800000420701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 10 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_10_RP0_REG_P3_[n]
Address	8000004207011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 11 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_11_RP0_REG_P0_[n]
Address	800000430701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 11 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_11_RP0_REG_P1_[n]
Address	800000430701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 11 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_11_RP0_REG_P2_[n]
Address	800000430701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 11 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_11_RP0_REG_P3_[n]
Address	8000004307011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 12 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_12_RP0_REG_P0_[n]
Address	800000440701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 12 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_12_RP0_REG_P1_[n]
Address	800000440701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 12 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_12_RP0_REG_P2_[n]
Address	800000440701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 12 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_12_RP0_REG_P3_[n]
Address	8000004407011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 13 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_13_RP0_REG_P0_[n]
Address	800000450701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 13 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_13_RP0_REG_P1_[n]
Address	800000450701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 13 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_13_RP0_REG_P2_[n]
Address	800000450701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 13 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_13_RP0_REG_P3_[n]
Address	8000004507011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 14 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_14_RP0_REG_P0_[n]
Address	800000460701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 14 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_14_RP0_REG_P1_[n]
Address	800000460701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 14 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_14_RP0_REG_P2_[n]
Address	800000460701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 14 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_14_RP0_REG_P3_[n]
Address	8000004607011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 15 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_15_RP0_REG_P0_[n]
Address	800000470701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 15 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_15_RP0_REG_P1_[n]
Address	800000470701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 15 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_15_RP0_REG_P2_[n]
Address	800000470701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 15 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_15_RP0_REG_P3_[n]
Address	8000004707011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 16 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_16_RP0_REG_P0_[n]
Address	800000480701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 16 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_16_RP0_REG_P1_[n]
Address	800000480701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 16 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_16_RP0_REG_P2_[n]
Address	800000480701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 16 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_16_RP0_REG_P3_[n]
Address	8000004807011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 18 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_18_RP0_REG_P0_[n]
Address	8000004A0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 18 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_18_RP0_REG_P1_[n]
Address	8000004A0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 18 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_18_RP0_REG_P2_[n]
Address	8000004A0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 18 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_18_RP0_REG_P3_[n]
Address	8000004A07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 20 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_20_RP0_REG_P0_[n]
Address	8000004C0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 20 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_20_RP0_REG_P1_[n]
Address	8000004C0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 20 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_20_RP0_REG_P2_[n]
Address	8000004C0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 20 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_20_RP0_REG_P3_[n]
Address	8000004C07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 22 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_22_RP0_REG_P0_[n]
Address	8000004E0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 22 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_22_RP0_REG_P1_[n]
Address	8000004E0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 22 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_22_RP0_REG_P2_[n]
Address	8000004E0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 22 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_22_RP0_REG_P3_[n]
Address	8000004E07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Read Delay Value 0 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY0_RANK_PAIR0_P0_[n]
Address	800000500701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 0 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY0_RANK_PAIR0_P1_[n]
Address	800000500701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 0 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY0_RANK_PAIR0_P2_[n]
Address	800000500701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.

Bits	SCOM	Field Mnemonic: Description
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 0 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY0_RANK_PAIR0_P3_[n]
Address	8000005007011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 1 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY1_RANK_PAIR0_P0_[n]
Address	800000510701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	**DP16 Read Delay Value 1 RP0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY1_RANK_PAIR0_P1_[n]
Address	800000510701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	**DP16 Read Delay Value 1 RP0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY1_RANK_PAIR0_P2_[n]
Address	800000510701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 1 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY1_RANK_PAIR0_P3_[n]
Address	8000005107011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 2 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY2_RANK_PAIR0_P0_[n]
Address	800000520701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 2 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY2_RANK_PAIR0_P1_[n]
Address	800000520701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.

Bits	SCOM	Field Mnemonic: Description
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 2 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY2_RANK_PAIR0_P2_[n]
Address	800000520701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 2 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY2_RANK_PAIR0_P3_[n]
Address	8000005207011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	**DP16 Read Delay Value 3 RP0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY3_RANK_PAIR0_P0_[n]
Address	800000530701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	**DP16 Read Delay Value 3 RP0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY3_RANK_PAIR0_P1_[n]
Address	800000530701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	**DP16 Read Delay Value 3 RP0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY3_RANK_PAIR0_P2_[n]
Address	800000530701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 3 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY3_RANK_PAIR0_P3_[n]
Address	8000005307011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 4 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY4_RANK_PAIR0_P0_[n]
Address	800000540701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.

Bits	SCOM	Field Mnemonic: Description
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 4 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY4_RANK_PAIR0_P1_[n]
Address	800000540701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 4 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY4_RANK_PAIR0_P2_[n]
Address	800000540701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	**DP16 Read Delay Value 4 RP0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY4_RANK_PAIR0_P3_[n]
Address	8000005407011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	**DP16 Read Delay Value 5 RP0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY5_RANK_PAIR0_P0_[n]
Address	800000550701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 5 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY5_RANK_PAIR0_P1_[n]
Address	800000550701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 5 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY5_RANK_PAIR0_P2_[n]
Address	800000550701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 5 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY5_RANK_PAIR0_P3_[n]
Address	8000005507011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.

Bits	SCOM	Field Mnemonic: Description
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 6 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY6_RANK_PAIR0_P0_[n]
Address	800000560701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 6 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY6_RANK_PAIR0_P1_[n]
Address	800000560701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	**DP16 Read Delay Value 6 RP0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY6_RANK_PAIR0_P2_[n]
Address	800000560701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	**DP16 Read Delay Value 6 RP0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY6_RANK_PAIR0_P3_[n]
Address	8000005607011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	**DP16 Read Delay Value 7 RP0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY7_RANK_PAIR0_P0_[n]
Address	800000570701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 7 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY7_RANK_PAIR0_P1_[n]
Address	800000570701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 7 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY7_RANK_PAIR0_P2_[n]
Address	800000570701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.

Bits	SCOM	Field Mnemonic: Description
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 7 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY7_RANK_PAIR0_P3_[n]
Address	8000005707011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Initial DQS Alignment 0 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN0_RANK_PAIR0_P0_[n]
Address	8000005C0701103F (SCOM), +0x0400_0000_0000
Description	These registers hold the data strobe clock (DQSClk) phase rotator values computed by initial calibration, They are updated at multiple times during the calibration. Periodic DQS alignment uses the values to compare against for determining long-term drift.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b0000000000000000000000000000000000000000000000000
49:55	RO	INITIAL_DQS_ROT_N0: This field holds the initial DQSClk rotator value for pins MEMINTD00B - MEMINTD03B in register 0 and MEMINTD08B - MEMINGTD11B in register 1. This value is updated by hardware.
56	RO	Reserved.
57:63	RO	INITIAL_DQS_ROT_N1: This field holds the initial DQSClk rotator value for pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINGTD15B in register 1. This value is updated by hardware.

Register Name	DP16 Initial DQS Alignment 0 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN0_RANK_PAIR0_P1_[n]
Address	8000005C0701143F (SCOM), +0x0400_0000_0000
Description	These registers hold the DQSClk phase rotator values computed by initial calibration, They are updated at multiple times during the calibration. Periodic DQS alignment uses the values to compare against for determining long-term drift.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RO	INITIAL_DQS_ROT_N0: This field holds the initial DQSClk rotator value for pins MEMINTD00B - MEMINTD03B in register 0 and MEMINTD08B - MEMINGTD11B in register 1. This value is updated by hardware.
56	RO	Reserved.
57:63	RO	INITIAL_DQS_ROT_N1: This field holds the initial DQSClk rotator value for pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINGTD15B in register 1.This value is updated by hardware.

Register Name	DP16 Initial DQS Alignment 0 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN0_RANK_PAIR0_P2_[n]
Address	8000005C0701183F (SCOM), +0x0400_0000_0000
Description	These registers hold the DQSClk phase rotator values computed by initial calibration, They are updated at multiple times during the calibration. Periodic DQS alignment uses the values to compare against for determining long-term drift.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RO	INITIAL_DQS_ROT_N0: This field holds the initial DQSClk rotator value for pins MEMINTD00B - MEMINTD03B in register 0 and MEMINTD08B - MEMINGTD11B in register 1. This value is updated by hardware.
56	RO	Reserved.
57:63	RO	INITIAL_DQS_ROT_N1: This field holds the initial DQSClk rotator value for pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINGTD15B in register 1.This value is updated by hardware.

Register Name	DP16 Initial DQS Alignment 0 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN0_RANK_PAIR0_P3_[n]
Address	8000005C07011C3F (SCOM), +0x0400_0000_0000
Description	These registers hold the DQSClk phase rotator values computed by initial calibration, They are updated at multiple times during the calibration. Periodic DQS alignment uses the values to compare against for determining long-term drift.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RO	INITIAL_DQS_ROT_N0: This field holds the initial DQSClk rotator value for pins MEMINTD00B - MEMINTD03B in register 0 and MEMINTD08B - MEMINGTD11B in register 1. This value is updated by hardware.

Bits	SCOM	Field Mnemonic: Description
56	RO	Reserved.
57:63	RO	INITIAL_DQS_ROT_N1: This field holds the initial DQSClk rotator value for pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINGTD15B in register 1.This value is updated by hardware.

Register Name	DP16 Initial DQS Alignment 1 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN1_RANK_PAIR0_P0_[n]
Address	8000005D0701103F (SCOM), +0x0400_0000_0000
Description	These registers hold the DQSClk phase rotator values computed by initial calibration, They are updated at multiple times during the calibration. Periodic DQS alignment uses the values to compare against for determining long-term drift.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b00000000000000000000000000000000000000000000000
49:55	RO	INITIAL_DQS_ROT_N2: This field holds the initial DQSClk rotator value for pins MEMINTD00B - MEMINTD03B in register 0 and MEMINTD08B - MEMINGTD11B in register 1. This value is updated by hardware.
56	RO	Constant = 0b0
57:63	RO	INITIAL_DQS_ROT_N3: This field holds the initial DQSClk rotator value for pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINGTD15B in register 1.This value is updated by hardware.

Register Name	DP16 Initial DQS Alignment 1 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN1_RANK_PAIR0_P1_[n]
Address	8000005D0701143F (SCOM), +0x0400_0000_0000
Description	These registers hold the DQSClk phase rotator values computed by initial calibration, They are updated at multiple times during the calibration. Periodic DQS alignment uses the values to compare against for determining long-term drift.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b00000000000000000000000000000000000000000000000
49:55	RO	INITIAL_DQS_ROT_N2: This field holds the initial DQSClk rotator value for pins MEMINTD00B - MEMINTD03B in register 0 and MEMINTD08B - MEMINGTD11B in register 1. This value is updated by hardware.
56	RO	Constant = 0b0
57:63	RO	INITIAL_DQS_ROT_N3: This field holds the initial DQSClk rotator value for pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINGTD15B in register 1.This value is updated by hardware.

Register Name	DP16 Initial DQS Alignment 1 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN1_RANK_PAIR0_P2_[n]
Address	8000005D0701183F (SCOM), +0x0400_0000_0000
Description	These registers hold the DQSClk phase rotator values computed by initial calibration, They are updated at multiple times during the calibration. Periodic DQS alignment uses the values to compare against for determining long-term drift.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RO	INITIAL_DQS_ROT_N2: This field holds the initial DQSClk rotator value for pins MEMINTD00B - MEMINTD03B in register 0 and MEMINTD08B - MEMINGTD11B in register 1. This value is updated by hardware.
56	RO	Constant = 0b0
57:63	RO	INITIAL_DQS_ROT_N3: This field holds the initial DQSClk rotator value for pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINGTD15B in register 1.This value is updated by hardware.

Register Name	DP16 Initial DQS Alignment 1 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN1_RANK_PAIR0_P3_[n]
Address	8000005D07011C3F (SCOM), +0x0400_0000_0000
Description	These registers hold the DQSClk phase rotator values computed by initial calibration, They are updated at multiple times during the calibration. Periodic DQS alignment uses the values to compare against for determining long-term drift.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RO	INITIAL_DQS_ROT_N2: This field holds the initial DQSClk rotator value for pins MEMINTD00B - MEMINTD03B in register 0 and MEMINTD08B - MEMINGTD11B in register 1. This value is updated by hardware.
56	RO	Constant = 0b0
57:63	RO	INITIAL_DQS_ROT_N3: This field holds the initial DQSClk rotator value for pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINGTD15B in register 1.This value is updated by hardware.

Register Name	DP16 Write VREF Value 0 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_VALUE0_RANK_PAIR0_P0_[n]
Address	8000005E0701103F (SCOM), +0x0400_0000_0000
Description	This register contains the starting and ending values of calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	Reserved.

Bits	SCOM	Field Mnemonic: Description
49	RWX	WR_VREF_RANGE_DRAM0: This bit contains the default and current value of the DRAM write (WR) VREF range for DRAM0 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in the Mode 6 Register (MR6) in the double data rate 4 (DDR4) JEDEC specification. The algorithm overwrites the initial value with the final value.
50:55	RWX	WR_VREF_VALUE_DRAM0: This field contains the default and current value of the DRAM WR VREF value for DRAM0 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
56	RW	Reserved.
57	RWX	WR_VREF_RANGE_DRAM1: This bit contains the default and current value of the DRAM WR VREF range for DRAM1 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
58:63	RWX	WR_VREF_VALUE_DRAM1: This field contains the default and current value of the DRAM WR VREF value for DRAM1 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.

Register Name	**DP16 Write VREF Value 0 RP0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_VALUE0_RANK_PAIR0_P1_[n]
Address	8000005E0701143F (SCOM), +0x0400_0000_0000
Description	This register contains the starting and ending values of calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	Reserved.
49	RWX	WR_VREF_RANGE_DRAM0: This bit contains the default and current value of the DRAM WR VREF range for DRAM0 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
50:55	RWX	WR_VREF_VALUE_DRAM0: This field contains the default and current value of the DRAM WR VREF value for DRAM0 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
56	RW	Reserved.
57	RWX	WR_VREF_RANGE_DRAM1: This bit contains the default and current value of the DRAM WR VREF range for DRAM1 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
58:63	RWX	WR_VREF_VALUE_DRAM1: This field contains the default and current value of the DRAM WR VREF value for DRAM1 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.

Register Name	DP16 Write VREF Value 0 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_VALUE0_RANK_PAIR0_P2_[n]
Address	8000005E0701183F (SCOM), +0x0400_0000_0000
Description	This register contains the starting and ending values of calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	Reserved.
49	RWX	WR_VREF_RANGE_DRAM0: This bit contains the default and current value of the DRAM WR VREF range for DRAM0 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
50:55	RWX	WR_VREF_VALUE_DRAM0: This field contains the default and current value of the DRAM WR VREF value for DRAM0 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
56	RW	Reserved.
57	RWX	WR_VREF_RANGE_DRAM1: This bit contains the default and current value of the DRAM WR VREF range for DRAM1 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
58:63	RWX	WR_VREF_VALUE_DRAM1: This field contains the default and current value of the DRAM WR VREF value for DRAM1 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.

Register Name	DP16 Write VREF Value 0 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_VALUE0_RANK_PAIR0_P3_[n]
Address	8000005E07011C3F (SCOM), +0x0400_0000_0000
Description	This register contains the starting and ending values of calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	Reserved.
49	RWX	WR_VREF_RANGE_DRAM0: This bit contains the default and current value of the DRAM WR VREF range for DRAM0 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
50:55	RWX	WR_VREF_VALUE_DRAM0: This field contains the default and current value of the DRAM WR VREF value for DRAM0 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
56	RW	Reserved.
57	RWX	WR_VREF_RANGE_DRAM1: This bit contains the default and current value of the DRAM WR VREF range for DRAM1 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	WR_VREF_VALUE_DRAM1: This field contains the default and current value of the DRAM WR VREF value for DRAM1 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.

Register Name	**DP16 Write VREF Value 1 RP0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_VALUE1_RANK_PAIR0_P0_[n]
Address	8000005F0701103F (SCOM), +0x0400_0000_0000
Description	This register contains the starting and ending values of calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	RW	Reserved.
49	RWX	WR_VREF_RANGE_DRAM2: This bit contains the default and current value of the DRAM WR VREF range for DRAM2 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
50:55	RWX	WR_VREF_VALUE_DRAM2: This bit contains the default and current value of the DRAM WR VREF value for DRAM2 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
56	RW	Reserved.
57	RWX	WR_VREF_RANGE_DRAM3: This bit contains the default and current value of the DRAM WR VREF range for DRAM3 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
58:63	RWX	WR_VREF_VALUE_DRAM3: This bit contains the default and current value of the DRAM WR VREF value for DRAM3 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.

Register Name	**DP16 Write VREF Value 1 RP0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_VALUE1_RANK_PAIR0_P1_[n]
Address	8000005F0701143F (SCOM), +0x0400_0000_0000
Description	This register contains the starting and ending values of calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	RW	Reserved.
49	RWX	WR_VREF_RANGE_DRAM2: This bit contains the default and current value of the DRAM WR VREF range for DRAM2 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	WR_VREF_VALUE_DRAM2: This bit contains the default and current value of the DRAM WR VREF value for DRAM2 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
56	RW	Reserved.
57	RWX	WR_VREF_RANGE_DRAM3: This bit contains the default and current value of the DRAM WR VREF range for DRAM3 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
58:63	RWX	WR_VREF_VALUE_DRAM3: This bit contains the default and current value of the DRAM WR VREF value for DRAM3 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.

Register Name	**DP16 Write VREF Value 1 RP0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_VALUE1_RANK_PAIR0_P2_[n]
Address	8000005F0701183F (SCOM), +0x0400_0000_0000
Description	This register contains the starting and ending values of calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48	RW	Reserved.
49	RWX	WR_VREF_RANGE_DRAM2: This bit contains the default and current value of the DRAM WR VREF range for DRAM2 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
50:55	RWX	WR_VREF_VALUE_DRAM2: This bit contains the default and current value of the DRAM WR VREF value for DRAM2 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
56	RW	Reserved.
57	RWX	WR_VREF_RANGE_DRAM3: This bit contains the default and current value of the DRAM WR VREF range for DRAM3 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
58:63	RWX	WR_VREF_VALUE_DRAM3: This bit contains the default and current value of the DRAM WR VREF value for DRAM3 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.

Register Name	**DP16 Write VREF Value 1 RP0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_VALUE1_RANK_PAIR0_P3_[n]
Address	8000005F07011C3F (SCOM), +0x0400_0000_0000
Description	This register contains the starting and ending values of calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49	RWX	WR_VREF_RANGE_DRAM2: This bit contains the default and current value of the DRAM WR VREF range for DRAM2 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
50:55	RWX	WR_VREF_VALUE_DRAM2: This bit contains the default and current value of the DRAM WR VREF value for DRAM2 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
56	RW	Reserved.
57	RWX	WR_VREF_RANGE_DRAM3: This bit contains the default and current value of the DRAM WR VREF range for DRAM3 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
58:63	RWX	WR_VREF_VALUE_DRAM3: This bit contains the default and current value of the DRAM WR VREF value for DRAM3 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.

Register Name	**DP16 Read Eye Size 0 RP0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE0_RANK_PAIR0_P0_[n]
Address	800000600701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 0 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE0_RANK_PAIR0_P1_[n]
Address	800000600701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 0 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE0_RANK_PAIR0_P2_[n]
Address	800000600701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 0 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE0_RANK_PAIR0_P3_[n]
Address	8000006007011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 1 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE1_RANK_PAIR0_P0_[n]
Address	800000610701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 1 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE1_RANK_PAIR0_P1_[n]
Address	800000610701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 1 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE1_RANK_PAIR0_P2_[n]
Address	800000610701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 1 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE1_RANK_PAIR0_P3_[n]
Address	8000006107011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 2 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE2_RANK_PAIR0_P0_[n]
Address	800000620701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 2 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE2_RANK_PAIR0_P1_[n]
Address	800000620701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 2 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE2_RANK_PAIR0_P2_[n]
Address	800000620701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 2 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE2_RANK_PAIR0_P3_[n]
Address	8000006207011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 3 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE3_RANK_PAIR0_P0_[n]
Address	800000630701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 3 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE3_RANK_PAIR0_P1_[n]
Address	800000630701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 3 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE3_RANK_PAIR0_P2_[n]
Address	800000630701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 3 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE3_RANK_PAIR0_P3_[n]
Address	8000006307011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 4 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE4_RANK_PAIR0_P0_[n]
Address	800000640701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 4 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE4_RANK_PAIR0_P1_[n]
Address	800000640701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 4 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE4_RANK_PAIR0_P2_[n]
Address	800000640701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 4 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE4_RANK_PAIR0_P3_[n]
Address	8000006407011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 5 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE5_RANK_PAIR0_P0_[n]
Address	800000650701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 5 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE5_RANK_PAIR0_P1_[n]
Address	800000650701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 5 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE5_RANK_PAIR0_P2_[n]
Address	800000650701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 5 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE5_RANK_PAIR0_P3_[n]
Address	8000006507011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 6 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE6_RANK_PAIR0_P0_[n]
Address	800000660701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 6 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE6_RANK_PAIR0_P1_[n]
Address	800000660701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 6 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE6_RANK_PAIR0_P2_[n]
Address	800000660701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 6 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE6_RANK_PAIR0_P3_[n]
Address	8000006607011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 7 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE7_RANK_PAIR0_P0_[n]
Address	800000670701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 7 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE7_RANK_PAIR0_P1_[n]
Address	800000670701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 7 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE7_RANK_PAIR0_P2_[n]
Address	800000670701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 7 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE7_RANK_PAIR0_P3_[n]
Address	8000006707011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 8 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE8_RANK_PAIR0_P0_[n]
Address	800000680701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 8 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE8_RANK_PAIR0_P1_[n]
Address	800000680701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 8 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE8_RANK_PAIR0_P2_[n]
Address	800000680701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 8 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE8_RANK_PAIR0_P3_[n]
Address	8000006807011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 9 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE9_RANK_PAIR0_P0_[n]
Address	800000690701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 9 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE9_RANK_PAIR0_P1_[n]
Address	800000690701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 9 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE9_RANK_PAIR0_P2_[n]
Address	800000690701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 9 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE9_RANK_PAIR0_P3_[n]
Address	8000006907011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 10 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE10_RANK_PAIR0_P0_[n]
Address	8000006A0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 10 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE10_RANK_PAIR0_P1_[n]
Address	8000006A0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 10 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE10_RANK_PAIR0_P2_[n]
Address	8000006A0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 10 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE10_RANK_PAIR0_P3_[n]
Address	8000006A07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 11 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE11_RANK_PAIR0_P0_[n]
Address	8000006B0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 11 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE11_RANK_PAIR0_P1_[n]
Address	8000006B0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 11 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE11_RANK_PAIR0_P2_[n]
Address	8000006B0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 11 RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE11_RANK_PAIR0_P3_[n]
Address	8000006B07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Write VREF Configuration 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_CONFIG0_P0_[n]
Address	8000006C0701103F (SCOM), +0x0400_0000_0000
Description	This register controls the write VREF operation.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	WR_CTR_1D_MODE_SWITCH: This bit forces running only the POWER8 memory buffer write-centering algorithm or the new VREF write-centering algorithm. 0 = Run the VREF (2D) write-centering algorithm. 1 = Run only the POWER8 mode write-centering algorithm.
49	RW	WR_CTR_RUN_FULL_1D: Always run the full 1D write-centering solution. As the 2D algorithm tries to find the widest write-centering eye solution, it runs the 1D algorithm many times. To speed up the run time, approximations can be made. 0 = Use the approximate algorithm while trying to find the best VREF. This setting runs the full algorithm only at the start and final VREF cases. 1 = Always runs the full 1D algorithm.
50:52	RW	WR_CTR_2D_SMALL_STEP_VAL: This field indicates the number of VREF steps to take when small stepping. A 1 is added to the value programmed here. That is, a register value of b000 causes the algorithm to step by 1.
53:56	RW	WR_CTR_2D_BIG_STEP_VAL: This field indicates the number of VREF steps to take when big stepping. A 1 is added to the value programmed here. That is, a register value of b0000 causes the algorithm to step by 1.

Bits	SCOM	Field Mnemonic: Description
57:59	RW	WR_CTR_NUM_BITS_TO_SKIP: This field sets the number of bits to skip when running intermediary VREFs, to speed up run time. This is, nominally set to b111, skipping all but one bit in a given DRAM. For x8 devices, all bits are used. For x4 devices, only bits 10 and 11 are used. For example, a b101 value skips 5 bits in a x8 device but only skips 1 bit in a x4 device.
60:62	RW	WR_CTR_NUM_NO_INC_VREF_COMP: This field sets the number of times during a VREF loop that an increase must not be found from the current maximum VREF to the current VREF before it is determined that the algorithm found the maximum VREF. A value of b000 corresponds to needing to see the same value or a decreasing value for one time in a row.
63	RW	DD2_WR_VREF_FIX_DISABLE: 0 = Enable the DD2 function for the write VREF algorithm. 1 = Enable the DD1 function.

Register Name	**DP16 Write VREF Configuration 0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_CONFIG0_P1_[n]
Address	8000006C0701143F (SCOM), +0x0400_0000_0000
Description	This register controls the write VREF operation.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	WR_CTR_1D_MODE_SWITCH: This bit forces running only the POWER8 memory buffer write-centering algorithm or the new VREF write-centering algorithm. 0 = Run the VREF (2D) write-centering algorithm. 1 = Run only the POWER8 mode write-centering algorithm.
49	RW	WR_CTR_RUN_FULL_1D: Always run the full 1D write-centering solution. As the 2D algorithm tries to find the widest write-centering eye solution, it runs the 1D algorithm many times. To speed up the run time, approximations can be made. 0 = Use the approximate algorithm while trying to find the best VREF. This setting runs the full algorithm only at the start and final VREF cases. 1 = Always runs the full 1D algorithm.
50:52	RW	WR_CTR_2D_SMALL_STEP_VAL: This field indicates the number of VREF steps to take when small stepping. A 1 is added to the value programmed here. That is, a register value of b000 causes the algorithm to step by 1.
53:56	RW	WR_CTR_2D_BIG_STEP_VAL: This field indicates the number of VREF steps to take when big stepping. A 1 is added to the value programmed here. That is, a register value of b0000 causes the algorithm to step by 1.
57:59	RW	WR_CTR_NUM_BITS_TO_SKIP: This field sets the number of bits to skip when running intermediary VREFs, to speed up run time. This is, nominally set to b111, skipping all but one bit in a given DRAM. For x8 devices, all bits are used. For x4 devices, only bits 10 and 11 are used. For example, a b101 value skips 5 bits in a x8 device but only skips 1 bit in a x4 device.
60:62	RW	WR_CTR_NUM_NO_INC_VREF_COMP: This field sets the number of times during a VREF loop that an increase must not be found from the current maximum VREF to the current VREF before it is determined that the algorithm found the maximum VREF. A value of b000 corresponds to needing to see the same value or a decreasing value for one time in a row.
63	RW	DD2_WR_VREF_FIX_DISABLE: 0 = Enable the DD2 function for the write VREF algorithm. 1 = Enable the DD1 function.

Register Name	DP16 Write VREF Configuration 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_CONFIG0_P2_[n]
Address	8000006C0701183F (SCOM), +0x0400_0000_0000
Description	This register controls the write VREF operation.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	RW	WR_CTR_1D_MODE_SWITCH: This bit forces running only the POWER8 memory buffer write-centering algorithm or the new VREF write-centering algorithm. 0 = Run the VREF (2D) write-centering algorithm. 1 = Run only the POWER8 mode write-centering algorithm.
49	RW	WR_CTR_RUN_FULL_1D: Always run the full 1D write-centering solution. As the 2D algorithm tries to find the widest write-centering eye solution, it runs the 1D algorithm many times. To speed up the run time, approximations can be made. 0 = Use the approximate algorithm while trying to find the best VREF. This setting runs the full algorithm only at the start and final VREF cases. 1 = Always runs the full 1D algorithm.
50:52	RW	WR_CTR_2D_SMALL_STEP_VAL: This field indicates the number of VREF steps to take when small stepping. A 1 is added to the value programmed here. That is, a register value of b000 causes the algorithm to step by 1.
53:56	RW	WR_CTR_2D_BIG_STEP_VAL: This field indicates the number of VREF steps to take when big stepping. A 1 is added to the value programmed here. That is, a register value of b0000 causes the algorithm to step by 1.
57:59	RW	WR_CTR_NUM_BITS_TO_SKIP: This field sets the number of bits to skip when running intermediary VREFs, to speed up run time. This is, nominally set to b111, skipping all but one bit in a given DRAM. For x8 devices, all bits are used. For x4 devices, only bits 10 and 11 are used. For example, a b101 value skips 5 bits in a x8 device but only skips 1 bit in a x4 device.
60:62	RW	WR_CTR_NUM_NO_INC_VREF_COMP: This field sets the number of times during a VREF loop that an increase must not be found from the current maximum VREF to the current VREF before it is determined that the algorithm found the maximum VREF. A value of b000 corresponds to needing to see the same value or a decreasing value for one time in a row.
63	RW	DD2_WR_VREF_FIX_DISABLE: 0 = Enable the DD2 function for the write VREF algorithm. 1 = Enable the DD1 function.

Register Name	DP16 Write VREF Configuration 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_CONFIG0_P3_[n]
Address	8000006C07011C3F (SCOM), +0x0400_0000_0000
Description	This register controls the write VREF operation.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	RW	WR_CTR_1D_MODE_SWITCH: This bit forces running only the POWER8 memory buffer write-centering algorithm or the new VREF write-centering algorithm. 0 = Run the VREF (2D) write-centering algorithm. 1 = Run only the POWER8 mode write-centering algorithm.

Bits	SCOM	Field Mnemonic: Description
49	RW	WR_CTR_RUN_FULL_1D: Always run the full 1D write-centering solution. As the 2D algorithm tries to find the widest write-centering eye solution, it runs the 1D algorithm many times. To speed up the run time, approximations can be made. 0 = Use the approximate algorithm while trying to find the best VREF. This setting runs the full algorithm only at the start and final VREF cases. 1 = Always runs the full 1D algorithm.
50:52	RW	WR_CTR_2D_SMALL_STEP_VAL: This field indicates the number of VREF steps to take when small stepping. A 1 is added to the value programmed here. That is, a register value of b000 causes the algorithm to step by 1.
53:56	RW	WR_CTR_2D_BIG_STEP_VAL: This field indicates the number of VREF steps to take when big stepping. A 1 is added to the value programmed here. That is, a register value of b0000 causes the algorithm to step by 1.
57:59	RW	WR_CTR_NUM_BITS_TO_SKIP: This field sets the number of bits to skip when running intermediary VREFs, to speed up run time. This is, nominally set to b111, skipping all but one bit in a given DRAM. For x8 devices, all bits are used. For x4 devices, only bits 10 and 11 are used. For example, a b101 value skips 5 bits in a x8 device but only skips 1 bit in a x4 device.
60:62	RW	WR_CTR_NUM_NO_INC_VREF_COMP: This field sets the number of times during a VREF loop that an increase must not be found from the current maximum VREF to the current VREF before it is determined that the algorithm found the maximum VREF. A value of b000 corresponds to needing to see the same value or a decreasing value for one time in a row.
63	RW	DD2_WR_VREF_FIX_DISABLE: 0 = Enable the DD2 function for the write VREF algorithm. 1 = Enable the DD1 function.

Register Name	**DP16 Read Diagnostic Configuration 3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_RD_DIA_CONFIG3_P0_[n]
Address	8000006D0701103F (SCOM), +0x0400_0000_0000
Description	This register can be used to improve jitter filtering during the DQS-alignment calibration algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	DESIRED_EDGE_CNTR_TARGET_HIGH: This field allows firmware control over the maximum edges required before the initial DQS alignment algorithm stays locked into tracking mode. A larger count value makes the algorithm work harder before declaring that a phase lock between the DRAM DQS and the internal DQSCLK has occurred. This count value must always be greater than the DESIRED_EDGE_CNTR_TARGET_LOW value. Use the DESIRED_EDGE_CNTR_TARGET_HIGH value 12 to improve jitter filtering characteristics during the initial DQS alignment algorithm. This field is not used during the periodic DQS alignment algorithm.
56:63	RWX	DESIRED_EDGE_CNTR_TARGET_LOW: This field allows firmware control over the minimum edges required before the initial DQS alignment algorithm toggles between coarse search and tracking mode. A larger count value makes it simpler for the algorithm to return to coarse search mode, and harder to enter tracking mode. This count value must always be smaller than the DESIRED_EDGE_CNTR_TARGET_HIGH value and greater than zero. Use the DESIRED_EDGE_CNTR_TARGET_LOW value 8 to improve jitter filtering characteristics during the initial DQS alignment algorithm. This field is not used during the periodic DQS alignment algorithm.

Register Name	**DP16 Read Diagnostic Configuration 3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_RD_DIA_CONFIG3_P1_[n]
Address	8000006D0701143F (SCOM), +0x0400_0000_0000
Description	This register can be used to improve jitter filtering during the DQS-alignment calibration algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:55	RWX	DESIRED_EDGE_CNTR_TARGET_HIGH: This field allows firmware control over the maximum edges required before the initial DQS alignment algorithm stays locked into tracking mode. A larger count value makes the algorithm work harder before declaring that a phase lock between the DRAM DQS and the internal DQSCLK has occurred. This count value must always be greater than the DESIRED_EDGE_CNTR_TARGET_LOW value. Use the DESIRED_EDGE_CNTR_TARGET_HIGH value 12 to improve jitter filtering characteristics during the initial DQS alignment algorithm. This field is not used during the periodic DQS alignment algorithm.
56:63	RWX	DESIRED_EDGE_CNTR_TARGET_LOW: This field allows firmware control over the minimum edges required before the initial DQS alignment algorithm toggles between coarse search and tracking mode. A larger count value makes it simpler for the algorithm to return to coarse search mode, and harder to enter tracking mode. This count value must always be smaller than the DESIRED_EDGE_CNTR_TARGET_HIGH value and greater than zero. Use the DESIRED_EDGE_CNTR_TARGET_LOW value 8 to improve jitter filtering characteristics during the initial DQS alignment algorithm. This field is not used during the periodic DQS alignment algorithm.

Register Name	**DP16 Read Diagnostic Configuration 3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_RD_DIA_CONFIG3_P2_[n]
Address	8000006D0701183F (SCOM), +0x0400_0000_0000
Description	This register can be used to improve jitter filtering during the DQS-alignment calibration algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:55	RWX	DESIRED_EDGE_CNTR_TARGET_HIGH: This field allows firmware control over the maximum edges required before the initial DQS alignment algorithm stays locked into tracking mode. A larger count value makes the algorithm work harder before declaring that a phase lock between the DRAM DQS and the internal DQSCLK has occurred. This count value must always be greater than the DESIRED_EDGE_CNTR_TARGET_LOW value. Use the DESIRED_EDGE_CNTR_TARGET_HIGH value 12 to improve jitter filtering characteristics during the initial DQS alignment algorithm. This field is not used during the periodic DQS alignment algorithm.
56:63	RWX	DESIRED_EDGE_CNTR_TARGET_LOW: This field allows firmware control over the minimum edges required before the initial DQS alignment algorithm toggles between coarse search and tracking mode. A larger count value makes it simpler for the algorithm to return to coarse search mode, and harder to enter tracking mode. This count value must always be smaller than the DESIRED_EDGE_CNTR_TARGET_HIGH value and greater than zero. Use the DESIRED_EDGE_CNTR_TARGET_LOW value 8 to improve jitter filtering characteristics during the initial DQS alignment algorithm. This field is not used during the periodic DQS alignment algorithm.

Register Name	DP16 Read Diagnostic Configuration 3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_DIA_CONFIG3_P3_[n]
Address	8000006D07011C3F (SCOM), +0x0400_0000_0000
Description	This register can be used to improve jitter filtering during the DQS-alignment calibration algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	DESIRED_EDGE_CNTR_TARGET_HIGH: This field allows firmware control over the maximum edges required before the initial DQS alignment algorithm stays locked into tracking mode. A larger count value makes the algorithm work harder before declaring that a phase lock between the DRAM DQS and the internal DQSCLK has occurred. This count value must always be greater than the DESIRED_EDGE_CNTR_TARGET_LOW value. Use the DESIRED_EDGE_CNTR_TARGET_HIGH value 12 to improve jitter filtering characteristics during the initial DQS alignment algorithm. This field is not used during the periodic DQS alignment algorithm.
56:63	RWX	DESIRED_EDGE_CNTR_TARGET_LOW: This field allows firmware control over the minimum edges required before the initial DQS alignment algorithm toggles between coarse search and tracking mode. A larger count value makes it simpler for the algorithm to return to coarse search mode, and harder to enter tracking mode. This count value must always be smaller than the DESIRED_EDGE_CNTR_TARGET_HIGH value and greater than zero. Use the DESIRED_EDGE_CNTR_TARGET_LOW value 8 to improve jitter filtering characteristics during the initial DQS alignment algorithm. This field is not used during the periodic DQS alignment algorithm.

Register Name	DP16 Read Diagnostic Configuration 4 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_DIA_CONFIG4_P0_[n]
Address	8000006E0701103F (SCOM), +0x0400_0000_0000
Description	This register is used for the diagnosis and characterization of the read function within the DP16. For correct functional mainline operation, this register must not be written. Contact your IBM representative before changing the value of this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RWX	DQS_ALIGN_FIX_DIS: Reserved. This bit must be set to 0b for normal operation.
49	RWX	CDD2_RD_FIFO_FIX_DIS: Reserved. This bit must be set to 0b for normal operation.
50:63	RO	Reserved.

Register Name	DP16 Read Diagnostic Configuration 4 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_DIA_CONFIG4_P1_[n]
Address	8000006E0701143F (SCOM), +0x0400_0000_0000
Description	This register is used for the diagnosis and characterization of the read function within the DP16. For correct functional mainline operation, this register must not be written. Contact your IBM representative before changing the value of this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RWX	DQS_ALIGN_FIX_DIS: Reserved. This bit must be set to 0b for normal operation.

Bits	SCOM	Field Mnemonic: Description
49	RWX	CDD2_RD_FIFO_FIX_DIS: Reserved. This bit must be set to 0b for normal operation.
50:63	RO	Reserved.

Register Name	DP16 Read Diagnostic Configuration 4 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_DIA_CONFIG4_P2_[n]
Address	8000006E0701183F (SCOM), +0x0400_0000_0000
Description	This register is used for the diagnosis and characterization of the read function within the DP16. For correct functional mainline operation, this register must not be written. Contact your IBM representative before changing the value of this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RWX	DQS_ALIGN_FIX_DIS: Reserved. This bit must be set to 0b for normal operation.
49	RWX	CDD2_RD_FIFO_FIX_DIS: Reserved. This bit must be set to 0b for normal operation.
50:63	RO	Reserved.

Register Name	DP16 Read Diagnostic Configuration 4 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_DIA_CONFIG4_P3_[n]
Address	8000006E07011C3F (SCOM), +0x0400_0000_0000
Description	This register is used for the diagnosis and characterization of the read function within the DP16. For correct functional mainline operation, this register must not be written. Contact your IBM representative before changing the value of this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RWX	DQS_ALIGN_FIX_DIS: Reserved. This bit must be set to 0b for normal operation.
49	RWX	CDD2_RD_FIFO_FIX_DIS: Reserved. This bit must be set to 0b for normal operation.
50:63	RO	Reserved.

Register Name	DP16 Delay Line Power Control Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DELAY_LINE_PWR_CTL_P0_[n]
Address	8000006F0701103F (SCOM), +0x0400_0000_0000
Description	This register is used to control or observe the enables of the delay lines and, hence, the power used by the delay lines. For correct functional mainline operation, this register must not be written. Contact your IBM representative before changing the value of this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	QUAD0_PWR_CTL: Quadrant 0 delay line control.
52:55	RWX	QUAD1_PWR_CTL: Quadrant 1 delay line control.
56:59	RWX	QUAD2_PWR_CTL: Quadrant 2 delay line control.

Bits	SCOM	Field Mnemonic: Description
60:63	RWX	QUAD3_PWR_CTL: Quadrant 3 delay line control.

Register Name	DP16 Delay Line Power Control Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DELAY_LINE_PWR_CTL_P1_[n]
Address	8000006F0701143F (SCOM), +0x0400_0000_0000
Description	This register is used to control or observe the enables of the delay lines and, hence, the power used by the delay lines. For correct functional mainline operation, this register must not be written. Contact your IBM representative before changing the value of this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	QUAD0_PWR_CTL: Quadrant 0 delay line control.
52:55	RWX	QUAD1_PWR_CTL: Quadrant 1 delay line control.
56:59	RWX	QUAD2_PWR_CTL: Quadrant 2 delay line control.
60:63	RWX	QUAD3_PWR_CTL: Quadrant 3 delay line control.

Register Name	DP16 Delay Line Power Control Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DELAY_LINE_PWR_CTL_P2_[n]
Address	8000006F0701183F (SCOM), +0x0400_0000_0000
Description	This register is used to control or observe the enables of the delay lines and, hence, the power used by the delay lines. For correct functional mainline operation, this register must not be written. Contact your IBM representative before changing the value of this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	QUAD0_PWR_CTL: Quadrant 0 delay line control.
52:55	RWX	QUAD1_PWR_CTL: Quadrant 1 delay line control.
56:59	RWX	QUAD2_PWR_CTL: Quadrant 2 delay line control.
60:63	RWX	QUAD3_PWR_CTL: Quadrant 3 delay line control.

Register Name	DP16 Delay Line Power Control Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DELAY_LINE_PWR_CTL_P3_[n]
Address	8000006F07011C3F (SCOM), +0x0400_0000_0000
Description	This register is used to control or observe the enables of the delay lines and, hence, the power used by the delay lines. For correct functional mainline operation, this register must not be written. Contact your IBM representative before changing the value of this register.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RWX	QUAD0_PWR_CTL: Quadrant 0 delay line control.
52:55	RWX	QUAD1_PWR_CTL: Quadrant 1 delay line control.

Bits	SCOM	Field Mnemonic: Description
56:59	RWX	QUAD2_PWR_CTL: Quadrant 2 delay line control.
60:63	RWX	QUAD3_PWR_CTL: Quadrant 3 delay line control.

Register Name	DP16 Read Timing Reference 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_TIMING_REFERENCE0_P0_[n]
Address	800000700701103F (SCOM), +0x0400_0000_0000
Description	This register holds reference values used by the hardware during periodic calibrations to adjust internal timing relationships that might drift over time. This value must not be altered via the programming interface, except for diagnostic use.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	REFERENCE0: This field contains a reference value used by hardware for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03 and nn{1} = 08, 09, 10, 11 during calibration. This value must not be altered via the programming interface, except for diagnostic use.
56	RO	Constant = 0b0
57:63	RW	REFERENCE1: This field contains a reference value used by hardware for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07 and nn{1} = 12, 13, 14, 15 during calibration. This value must not be altered via the programming interface, except for diagnostic use.

Register Name	DP16 Read Timing Reference 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_TIMING_REFERENCE0_P1_[n]
Address	800000700701143F (SCOM), +0x0400_0000_0000
Description	This register holds reference values used by the hardware during periodic calibrations to adjust internal timing relationships that might drift over time. This value must not be altered via the programming interface, except for diagnostic use.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	REFERENCE0: This field contains a reference value used by hardware for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03 and nn{1} = 08, 09, 10, 11 during calibration. This value must not be altered via the programming interface, except for diagnostic use.
56	RO	Constant = 0b0
57:63	RW	REFERENCE1: This field contains a reference value used by hardware for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07 and nn{1} = 12, 13, 14, 15 during calibration. This value must not be altered via the programming interface, except for diagnostic use.

Register Name	DP16 Read Timing Reference 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_TIMING_REFERENCE0_P2_[n]
Address	800000700701183F (SCOM), +0x0400_0000_0000
Description	This register holds reference values used by the hardware during periodic calibrations to adjust internal timing relationships that might drift over time. This value must not be altered via the programming interface, except for diagnostic use.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	REFERENCE0: This field contains a reference value used by hardware for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03 and nn{1} = 08, 09, 10, 11 during calibration. This value must not be altered via the programming interface, except for diagnostic use.
56	RO	Constant = 0b0
57:63	RW	REFERENCE1: This field contains a reference value used by hardware for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07 and nn{1} = 12, 13, 14, 15 during calibration. This value must not be altered via the programming interface, except for diagnostic use.

Register Name	**DP16 Read Timing Reference 0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_TIMING_REFERENCE0_P3_[n]
Address	8000007007011C3F (SCOM), +0x0400_0000_0000
Description	This register holds reference values used by the hardware during periodic calibrations to adjust internal timing relationships that might drift over time. This value must not be altered via the programming interface, except for diagnostic use.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	REFERENCE0: This field contains a reference value used by hardware for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03 and nn{1} = 08, 09, 10, 11 during calibration. This value must not be altered via the programming interface, except for diagnostic use.
56	RO	Constant = 0b0
57:63	RW	REFERENCE1: This field contains a reference value used by hardware for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07 and nn{1} = 12, 13, 14, 15 during calibration. This value must not be altered via the programming interface, except for diagnostic use.

Register Name	**DP16 Read Timing Reference 1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_TIMING_REFERENCE1_P0_[n]
Address	8000007107011O3F (SCOM), +0x0400_0000_0000
Description	This register holds reference values used by the hardware during periodic calibrations to adjust internal timing relationships that might drift over time. This value must not be altered via the programming interface, except for diagnostic use.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	REFERENCE2: This field contains a reference value used by hardware for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value must not be altered via the programming interface, except for diagnostic use.
56	RO	Constant = 0b0
57:63	RW	REFERENCE3: This field contains a reference value used by hardware for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value must not be altered via the programming interface, except for diagnostic use.

Register Name	DP16 Read Timing Reference 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_TIMING_REFERENCE1_P1_[n]
Address	800000710701143F (SCOM), +0x0400_0000_0000
Description	This register holds reference values used by the hardware during periodic calibrations to adjust internal timing relationships that might drift over time. This value must not be altered via the programming interface, except for diagnostic use.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	REFERENCE2: This field contains a reference value used by hardware for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value must not be altered via the programming interface, except for diagnostic use.
56	RO	Constant = 0b0
57:63	RW	REFERENCE3: This field contains a reference value used by hardware for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value must not be altered via the programming interface, except for diagnostic use.

Register Name	DP16 Read Timing Reference 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_TIMING_REFERENCE1_P2_[n]
Address	800000710701183F (SCOM), +0x0400_0000_0000
Description	This register holds reference values used by the hardware during periodic calibrations to adjust internal timing relationships that might drift over time. This value must not be altered via the programming interface, except for diagnostic use.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	REFERENCE2: This field contains a reference value used by hardware for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value must not be altered via the programming interface, except for diagnostic use.
56	RO	Constant = 0b0
57:63	RW	REFERENCE3: This field contains a reference value used by hardware for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value must not be altered via the programming interface, except for diagnostic use.

Register Name	DP16 Read Timing Reference 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_TIMING_REFERENCE1_P3_[n]
Address	8000007107011C3F (SCOM), +0x0400_0000_0000
Description	This register holds reference values used by the hardware during periodic calibrations to adjust internal timing relationships that might drift over time. This value must not be altered via the programming interface, except for diagnostic use.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	REFERENCE2: This field contains a reference value used by hardware for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value must not be altered via the programming interface, except for diagnostic use.

Bits	SCOM	Field Mnemonic: Description
56	RO	Constant = 0b0
57:63	RW	REFERENCE3: This field contains a reference value used by hardware for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value must not be altered via the programming interface, except for diagnostic use.

Register Name	DP16 Read DQS Timing Reference Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DQS_TIMING_REFERENCE_P0_[n]
Address	800000720701103F (SCOM), +0x0400_0000_0000
Description	This register holds a reference value used by the hardware during periodic calibrations to adjust internal timing relationships that might drift over time. This value must not be altered via the programming interface, except for diagnostic use.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	REFERENCE: This field contains a reference value used by hardware for the DQS pins. This value must not be altered via the programming interface except for diagnostic use.
56:63	RO	Constant = 0b00000000

Register Name	DP16 Read DQS Timing Reference Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DQS_TIMING_REFERENCE_P1_[n]
Address	800000720701143F (SCOM), +0x0400_0000_0000
Description	This register holds a reference value used by the hardware during periodic calibrations to adjust internal timing relationships that might drift over time. This value must not be altered via the programming interface, except for diagnostic use.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	REFERENCE: This field contains a reference value used by hardware for the DQS pins. This value must not be altered via the programming interface except for diagnostic use.
56:63	RO	Constant = 0b00000000

Register Name	DP16 Read DQS Timing Reference Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DQS_TIMING_REFERENCE_P2_[n]
Address	800000720701183F (SCOM), +0x0400_0000_0000
Description	This register holds a reference value used by the hardware during periodic calibrations to adjust internal timing relationships that might drift over time. This value must not be altered via the programming interface, except for diagnostic use.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	REFERENCE: This field contains a reference value used by hardware for the DQS pins. This value must not be altered via the programming interface except for diagnostic use.
56:63	RO	Constant = 0b00000000

Register Name	DP16 Read DQS Timing Reference Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DQS_TIMING_REFERENCE_P3_[n]
Address	8000007207011C3F (SCOM), +0x0400_0000_0000
Description	This register holds a reference value used by the hardware during periodic calibrations to adjust internal timing relationships that might drift over time. This value must not be altered via the programming interface, except for diagnostic use.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	REFERENCE: This field contains a reference value used by hardware for the DQS pins. This value must not be altered via the programming interface except for diagnostic use.
56:63	RO	Constant = 0b00000000

Register Name	DP16 SysClk Phase Rotator Value Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_SYSCLK_PR_VALUE_P0_[n]
Address	800000730701103F (SCOM), +0x0400_0000_0000
Description	This register holds the current phase rotator value of the SysClk phase rotator.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	ROX	BB_LOCK0: For SysClk rotator 0. 1 = The dphy_gckn/SysClk phase alignment controller has reached alignment between the dphy_gckn and the SysClk as of the last update by the dphy_gckn/SysClk phase alignment controller. 0 = The dphy_gckn and SysClk are not in alignment as of the last update by the dphy_gckn/SysClk phase alignment controller. There are two types of locks. See the SYSCLK_ROT_OVERRIDE field in the DP16 SysClk 0 Phase Rotator Control Register.
49:55	ROX	SYSCLK_ROT0: For SysClk rotator 0. This is the internally calculated value of the memory controller clock (MEMCTLCLKI) phase to the SysClk (SYSCLK) phase offset. It is used to set the SysClk phase rotator when SYSCLK_ROT_OVERRIDE_EN = 0. These bits reset, but are continually loaded with the value that is calculated by the dphy_gckn to SysClk alignment circuit for the SysClk delay, exclusive of reset.
56	ROX	BB_LOCK1: For SysClk rotator 1. 1 = The dphy_gckn/SysClk phase alignment controller has reached alignment between the dphy_gckn and the SysClk as of the last update by the dphy_gckn/SysClk phase alignment controller. 0 = The dphy_gckn and SysClk are not in alignment as of the last update by the dphy_gckn/SysClk phase alignment controller. There are two types of locks. See the SYSCLK_ROT_OVERRIDE field in the DP16 SysClk 0 Phase Rotator Control Register.
57:63	ROX	SYSCLK_ROT1: For SysClk rotator 1. This is the internally calculated value of the memory controller clock (MEMCTLCLKI) phase to the SysClk (SYSCLK) phase offset. It is used to set the SysClk phase rotator when SYSCLK_ROT_OVERRIDE_EN = 0. These bits reset, but are continually loaded with the value that is calculated by the dphy_gckn to SysClk alignment circuit for the SysClk delay, exclusive of reset.

Register Name	DP16 SysClk Phase Rotator Value Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_SYSCLK_PR_VALUE_P1_[n]
Address	800000730701143F (SCOM), +0x0400_0000_0000
Description	This register holds the current phase rotator value of the SysClk phase rotator.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	ROX	BB_LOCK0: For SysClk rotator 0. 1 = The dphy_gckn/SysClk phase alignment controller has reached alignment between the dphy_gckn and the SysClk as of the last update by the dphy_gckn/SysClk phase alignment controller. 0 = The dphy_gckn and SysClk are not in alignment as of the last update by the dphy_gckn/SysClk phase alignment controller. There are two types of locks. See the SYSCLK_ROT_OVERRIDE field in the DP16 SysClk 0 Phase Rotator Control Register.
49:55	ROX	SYSCLK_ROT0: For SysClk rotator 0. This is the internally calculated value of the memory controller clock (MEMCTLCLKI) phase to the SysClk (SYSCLK) phase offset. It is used to set the SysClk phase rotator when SYSCLK_ROT_OVERRIDE_EN = 0. These bits reset, but are continually loaded with the value that is calculated by the dphy_gckn to SysClk alignment circuit for the SysClk delay, exclusive of reset.
56	ROX	BB_LOCK1: For SysClk rotator 1. 1 = The dphy_gckn/SysClk phase alignment controller has reached alignment between the dphy_gckn and the SysClk as of the last update by the dphy_gckn/SysClk phase alignment controller. 0 = The dphy_gckn and SysClk are not in alignment as of the last update by the dphy_gckn/SysClk phase alignment controller. There are two types of locks. See the SYSCLK_ROT_OVERRIDE field in the DP16 SysClk 0 Phase Rotator Control Register.
57:63	ROX	SYSCLK_ROT1: For SysClk rotator 1. This is the internally calculated value of the memory controller clock (MEMCTLCLKI) phase to the SysClk (SYSCLK) phase offset. It is used to set the SysClk phase rotator when SYSCLK_ROT_OVERRIDE_EN = 0. These bits reset, but are continually loaded with the value that is calculated by the dphy_gckn to SysClk alignment circuit for the SysClk delay, exclusive of reset.

Register Name	DP16 SysClk Phase Rotator Value Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_SYSCLK_PR_VALUE_P2_[n]
Address	800000730701183F (SCOM), +0x0400_0000_0000
Description	This register holds the current phase rotator value of the SysClk phase rotator.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	ROX	BB_LOCK0: For SysClk rotator 0. 1 = The dphy_gckn/SysClk phase alignment controller has reached alignment between the dphy_gckn and the SysClk as of the last update by the dphy_gckn/SysClk phase alignment controller. 0 = The dphy_gckn and SysClk are not in alignment as of the last update by the dphy_gckn/SysClk phase alignment controller. There are two types of locks. See the SYSCLK_ROT_OVERRIDE field in the DP16 SysClk 0 Phase Rotator Control Register.
49:55	ROX	SYSCLK_ROT0: For SysClk rotator 0. This is the internally calculated value of the memory controller clock (MEMCTLCLKI) phase to the SysClk (SYSCLK) phase offset. It is used to set the SysClk phase rotator when SYSCLK_ROT_OVERRIDE_EN = 0. These bits reset, but are continually loaded with the value that is calculated by the dphy_gckn to SysClk alignment circuit for the SysClk delay, exclusive of reset.

Bits	SCOM	Field Mnemonic: Description
56	ROX	BB_LOCK1: For SysClk rotator 1. 1 = The dphy_gckn/SysClk phase alignment controller has reached alignment between the dphy_gckn and the SysClk as of the last update by the dphy_gckn/SysClk phase alignment controller. 0 = The dphy_gckn and SysClk are not in alignment as of the last update by the dphy_gckn/SysClk phase alignment controller. There are two types of locks. See the SYSCLK_ROT_OVERRIDE field in the DP16 SysClk 0 Phase Rotator Control Register.
57:63	ROX	SYSCLK_ROT1: For SysClk rotator 1. This is the internally calculated value of the memory controller clock (MEMCTLCLKI) phase to the SysClk (SYSCLK) phase offset. It is used to set the SysClk phase rotator when SYSCLK_ROT_OVERRIDE_EN = 0. These bits reset, but are continually loaded with the value that is calculated by the dphy_gckn to SysClk alignment circuit for the SysClk delay, exclusive of reset.

Register Name	**DP16 SysClk Phase Rotator Value Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_SYSCLK_PR_VALUE_P3_[n]
Address	8000007307011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the current phase rotator value of the SysClk phase rotator.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	ROX	BB_LOCK0: For SysClk rotator 0. 1 = The dphy_gckn/SysClk phase alignment controller has reached alignment between the dphy_gckn and the SysClk as of the last update by the dphy_gckn/SysClk phase alignment controller. 0 = The dphy_gckn and SysClk are not in alignment as of the last update by the dphy_gckn/SysClk phase alignment controller. There are two types of locks. See the SYSCLK_ROT_OVERRIDE field in the DP16 SysClk 0 Phase Rotator Control Register.
49:55	ROX	SYSCLK_ROT0: For SysClk rotator 0. This is the internally calculated value of the memory controller clock (MEMCTLCLKI) phase to the SysClk (SYSCLK) phase offset. It is used to set the SysClk phase rotator when SYSCLK_ROT_OVERRIDE_EN = 0. These bits reset, but are continually loaded with the value that is calculated by the dphy_gckn to SysClk alignment circuit for the SysClk delay, exclusive of reset.
56	ROX	BB_LOCK1: For SysClk rotator 1. 1 = The dphy_gckn/SysClk phase alignment controller has reached alignment between the dphy_gckn and the SysClk as of the last update by the dphy_gckn/SysClk phase alignment controller. 0 = The dphy_gckn and SysClk are not in alignment as of the last update by the dphy_gckn/SysClk phase alignment controller. There are two types of locks. See the SYSCLK_ROT_OVERRIDE field in the DP16 SysClk 0 Phase Rotator Control Register.
57:63	ROX	SYSCLK_ROT1: For SysClk rotator 1. This is the internally calculated value of the memory controller clock (MEMCTLCLKI) phase to the SysClk (SYSCLK) phase offset. It is used to set the SysClk phase rotator when SYSCLK_ROT_OVERRIDE_EN = 0. These bits reset, but are continually loaded with the value that is calculated by the dphy_gckn to SysClk alignment circuit for the SysClk delay, exclusive of reset.

Register Name	DP16 WrClk Phase Rotator Offset Value Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WRCLK_PR_P0_[n]
Address	800000740701103F (SCOM), +0x0400_0000_0000
Description	This register holds the phase rotator static offset value that is used to determine the phase of the WrClk with respect to the SysClk.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	TSYS_WRCLK: This field contains the static value of the system clock (SysClk) phase rotator to the write clock (WrClk) phase rotator. Set to ‘12’h for 2666 MT/s. Set to ‘10’h for 2400 MT/s. Set to ‘0F’h for 2133 MT/s. Set to ‘0D’h for 1866 MT/s. For zero delay simulations, or simulations where the delay of the SysClk tree and the WrClk tree are equal, set this field to 60h.
56:63	RO	Constant = 0b00000000

Register Name	DP16 WrClk Phase Rotator Offset Value Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WRCLK_PR_P1_[n]
Address	800000740701143F (SCOM), +0x0400_0000_0000
Description	This register holds the phase rotator static offset value that is used to determine the phase of the WrClk with respect to the SysClk.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	TSYS_WRCLK: This field contains the static value of the system clock (SysClk) phase rotator to the write clock (WrClk) phase rotator. Set to ‘12’h for 2666 MT/s. Set to ‘10’h for 2400 MT/s. Set to ‘0F’h for 2133 MT/s. Set to ‘0D’h for 1866 MT/s. For zero delay simulations, or simulations where the delay of the SysClk tree and the WrClk tree are equal, set this field to 60h.
56:63	RO	Constant = 0b00000000

Register Name	DP16 WrClk Phase Rotator Offset Value Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WRCLK_PR_P2_[n]
Address	800000740701183F (SCOM), +0x0400_0000_0000
Description	This register holds the phase rotator static offset value that is used to determine the phase of the WrClk with respect to the SysClk.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RW	TSYS_WRCLK: This field contains the static value of the system clock (SysClk) phase rotator to the write clock (WrClk) phase rotator. Set to '12'h for 2666 MT/s. Set to '10'h for 2400 MT/s. Set to '0F'h for 2133 MT/s. Set to '0D'h for 1866 MT/s. For zero delay simulations, or simulations where the delay of the SysClk tree and the WrClk tree are equal, set this field to 60h.
56:63	RO	Constant = 0b00000000

Register Name	DP16 WrClk Phase Rotator Offset Value Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WRCLK_PR_P3_[n]
Address	8000007407011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the phase rotator static offset value that is used to determine the phase of the WrClk with respect to the SysClk.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	TSYS_WRCLK: This field contains the static value of the system clock (SysClk) phase rotator to the write clock (WrClk) phase rotator. Set to '12'h for 2666 MT/s. Set to '10'h for 2400 MT/s. Set to '0F'h for 2133 MT/s. Set to '0D'h for 1866 MT/s. For zero delay simulations, or simulations where the delay of the SysClk tree and the WrClk tree are equal, set this field to 60h.
56:63	RO	Constant = 0b00000000

Register Name	DP16 IO TX Configuration 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_IO_TX_CONFIG0_P0_[n]
Address	800000750701103F (SCOM), +0x0400_0000_0000
Description	This register contains the receiver configuration for the DP16.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	STRENGTH: Phase rotator strength bits. Set this field as follows for the given data rate: 0000 = DDR PHY is not operational 0001 = 1866 MT/s. 0010 = 2133 MT/s. 0100 = 2400 MT/s. 1000 = 2666 MT/s. All other values are reserved.
52	RW	DD2_RESET_READ_FIX_DISABLE: 0 = Enable the DD2 function to remove the register reset on read feature on status registers. 1 = Enable the DD1 function.
53:63	RW	Reserved.

Register Name	DP16 IO TX Configuration 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_IO_TX_CONFIG0_P1_[n]
Address	800000750701143F (SCOM), +0x0400_0000_0000
Description	This register contains the receiver configuration for the DP16.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	STRENGTH: Phase rotator strength bits. Set this field as follows for the given data rate: 0000 = DDR PHY is not operational 0001 = 1866 MT/s. 0010 = 2133 MT/s. 0100 = 2400 MT/s. 1000 = 2666 MT/s. All other values are reserved.
52	RW	DD2_RESET_READ_FIX_DISABLE: 0 = Enable the DD2 function to remove the register reset on read feature on status registers. 1 = Enable the DD1 function.
53:63	RW	Reserved.

Register Name	DP16 IO TX Configuration 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_IO_TX_CONFIG0_P2_[n]
Address	800000750701183F (SCOM), +0x0400_0000_0000
Description	This register contains the receiver configuration for the DP16.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	STRENGTH: Phase rotator strength bits. Set this field as follows for the given data rate: 0000 = DDR PHY is not operational 0001 = 1866 MT/s. 0010 = 2133 MT/s. 0100 = 2400 MT/s. 1000 = 2666 MT/s. All other values are reserved.
52	RW	DD2_RESET_READ_FIX_DISABLE: 0 = Enable the DD2 function to remove the register reset on read feature on status registers. 1 = Enable the DD1 function.
53:63	RW	Reserved.

Register Name	DP16 IO TX Configuration 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_IO_TX_CONFIG0_P3_[n]
Address	8000007507011C3F (SCOM), +0x0400_0000_0000
Description	This register contains the receiver configuration for the DP16.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	STRENGTH: Phase rotator strength bits. Set this field as follows for the given data rate: 0000 = DDR PHY is not operational 0001 = 1866 MT/s. 0010 = 2133 MT/s. 0100 = 2400 MT/s. 1000 = 2666 MT/s. All other values are reserved.
52	RW	DD2_RESET_READ_FIX_DISABLE: 0 = Enable the DD2 function to remove the register reset on read feature on status registers. 1 = Enable the DD1 function.
53:63	RW	Reserved.

Register Name	**DP16 Read VREF DAC Comparator Ouptut Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_CAL_EN_P0_[n]
Address	800000760701103F (SCOM), +0x0400_0000_0000
Description	Each bit of this register drives the read VREF calibration enable control to the analog logic controlling a DQ data bit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RWX	VREF_CAL_EN: Bits 48:63 drive analog controls for DQ 0:15. When 0, the bit is disabled and is not used in calibration. When 1, the bit is used if it is the lowest order enabled bit in each pair. If the lower bit of each pair is enabled, it is used. The higher order bit is used if and only if the lower-order bit is disabled. For example: 0xFFFF or 0xAAAA enable all the even bits; 0x5555 enables all the odd bits. 0xFFFF works in most cases.

Register Name	**DP16 Read VREF DAC Comparator Ouptut Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_CAL_EN_P1_[n]
Address	800000760701143F (SCOM), +0x0400_0000_0000
Description	Each bit of this register drives the read VREF calibration enable control to the analog logic controlling a DQ data bit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RWX	VREF_CAL_EN: Bits 48:63 drive analog controls for DQ 0:15. When 0, the bit is disabled and is not used in calibration. When 1, the bit is used if it is the lowest order enabled bit in each pair. If the lower bit of each pair is enabled, it is used. The higher order bit is used if and only if the lower-order bit is disabled. For example: 0xFFFF or 0xAAAA enable all the even bits; 0x5555 enables all the odd bits. 0xFFFF works in most cases.

Register Name	DP16 Read VREF DAC Comparator Ouptut Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_CAL_EN_P2_[n]
Address	800000760701183F (SCOM), +0x0400_0000_0000
Description	Each bit of this register drives the read VREF calibration enable control to the analog logic controlling a DQ data bit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RWX	VREF_CAL_EN: Bits 48:63 drive analog controls for DQ 0:15. When 0, the bit is disabled and is not used in calibration. When 1, the bit is used if it is the lowest order enabled bit in each pair. If the lower bit of each pair is enabled, it is used. The higher order bit is used if and only if the lower-order bit is disabled. For example: 0xFFFF or 0xAAAA enable all the even bits; 0x5555 enables all the odd bits. 0xFFFF works in most cases.

Register Name	DP16 Read VREF DAC Comparator Ouptut Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_CAL_EN_P3_[n]
Address	8000007607011C3F (SCOM), +0x0400_0000_0000
Description	Each bit of this register drives the read VREF calibration enable control to the analog logic controlling a DQ data bit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RWX	VREF_CAL_EN: Bits 48:63 drive analog controls for DQ 0:15. When 0, the bit is disabled and is not used in calibration. When 1, the bit is used if it is the lowest order enabled bit in each pair. If the lower bit of each pair is enabled, it is used. The higher order bit is used if and only if the lower-order bit is disabled. For example: 0xFFFF or 0xAAAA enable all the even bits; 0x5555 enables all the odd bits. 0xFFFF works in most cases.

Register Name	DP16 DLL/VREG Configuration 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_CONFIG1_P0_[n]
Address	800000770701103F (SCOM), +0x0400_0000_0000
Description	This is the second of two registers that provide configuration for a variety of DLL and VREG programming values.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:51	RW	HS_DLLMUX_SEL_0_0_3: Select 1 of 16 phases of DLL to send out to the high-speed multiplex structure (for DP8 associated with bits 0:7).
52	RW	Reserved. Hold for future expansion, HS_DLLMUX_SEL_0(4).
53:56	RW	HS_DLLMUX_SEL_1_0_3: Select 1 of 16 phases of DLL to send out to the high-speed multiplex structure (for DP8 associated with bits 8:15).
57	RW	Reserved.
58:59	RW	Reserved.

Bits	SCOM	Field Mnemonic: Description
60	RW	Reserved.
61	RW	S0INSDLYTAP: This register bit is connected to the S0INSDLYTAP input of the DP16 analog core. For proper functional operation, this bit must be 0b.
62	RW	S1INSDLYTAP: This register bit is connected to the S1INSDLYTAP input of the DP16 analog core. For proper functional operation, this bit must be 0b.
63	RW	Reserved.

Register Name	DP16 DLL/VREG Configuration 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_CONFIG1_P1_[n]
Address	800000770701143F (SCOM), +0x0400_0000_0000
Description	This is the second of two registers that provide configuration for a variety of DLL and VREG programming values.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000
48:51	RW	HS_DLLMUX_SEL_0_0_3: Select 1 of 16 phases of DLL to send out to the high-speed multiplex structure (for DP8 associated with bits 0:7).
52	RW	Reserved. Hold for future expansion, HS_DLLMUX_SEL_0(4).
53:56	RW	HS_DLLMUX_SEL_1_0_3: Select 1 of 16 phases of DLL to send out to the high-speed multiplex structure (for DP8 associated with bits 8:15).
57	RW	Reserved.
58:59	RW	Reserved.
60	RW	Reserved.
61	RW	S0INSDLYTAP: This register bit is connected to the S0INSDLYTAP input of the DP16 analog core. For proper functional operation, this bit must be 0b.
62	RW	S1INSDLYTAP: This register bit is connected to the S1INSDLYTAP input of the DP16 analog core. For proper functional operation, this bit must be 0b.
63	RW	Reserved.

Register Name	DP16 DLL/VREG Configuration 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_CONFIG1_P2_[n]
Address	800000770701183F (SCOM), +0x0400_0000_0000
Description	This is the second of two registers that provide configuration for a variety of DLL and VREG programming values.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000
48:51	RW	HS_DLLMUX_SEL_0_0_3: Select 1 of 16 phases of DLL to send out to the high-speed multiplex structure (for DP8 associated with bits 0:7).
52	RW	Reserved. Hold for future expansion, HS_DLLMUX_SEL_0(4).
53:56	RW	HS_DLLMUX_SEL_1_0_3: Select 1 of 16 phases of DLL to send out to the high-speed multiplex structure (for DP8 associated with bits 8:15).

Bits	SCOM	Field Mnemonic: Description
57	RW	Reserved.
58:59	RW	Reserved.
60	RW	Reserved.
61	RW	S0INSDLYTAP: This register bit is connected to the S0INSDLYTAP input of the DP16 analog core. For proper functional operation, this bit must be 0b.
62	RW	S1INSDLYTAP: This register bit is connected to the S1INSDLYTAP input of the DP16 analog core. For proper functional operation, this bit must be 0b.
63	RW	Reserved.

Register Name	**DP16 DLL/VREG Configuration 1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DLL_CONFIG1_P3_[n]
Address	8000007707011C3F (SCOM), +0x0400_0000_0000
Description	This is the second of two registers that provide configuration for a variety of DLL and VREG programming values.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	HS_DLLMUX_SEL_0_0_3: Select 1 of 16 phases of DLL to send out to the high-speed multiplex structure (for DP8 associated with bits 0:7).
52	RW	Reserved. Hold for future expansion, HS_DLLMUX_SEL_0(4).
53:56	RW	HS_DLLMUX_SEL_1_0_3: Select 1 of 16 phases of DLL to send out to the high-speed multiplex structure (for DP8 associated with bits 8:15).
57	RW	Reserved.
58:59	RW	Reserved.
60	RW	Reserved.
61	RW	S0INSDLYTAP: This register bit is connected to the S0INSDLYTAP input of the DP16 analog core. For proper functional operation, this bit must be 0b.
62	RW	S1INSDLYTAP: This register bit is connected to the S1INSDLYTAP input of the DP16 analog core. For proper functional operation, this bit must be 0b.
63	RW	Reserved.

Register Name	**DP16 IO Driver FET Slice Enable Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_IO_TX_FET_SLICE_P0_[n]
Address	800000780701103F (SCOM), +0x0400_0000_0000
Description	This register provides driver NFET and PFET slice enables. These values are used for all of the drivers on this DP16 instance when driving data out.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	Reserved.

Bits	SCOM	Field Mnemonic: Description
49:55	RW	EN_SLICE_N_WR: This field provides the driver NFET slice enable at 240 W/slice. Each bit in this multibit field controls one slice. 0 = Disable the FET slice. 1 = Enable the FET slice. The default value is 1111111b for 34 W.
56	RW	Reserved.
57:63	RW	EN_SLICE_P_WR: This field provides the driver PFET slice enable at 240 W/slice. Each bit in this multibit field controls one slice. 0 = Disable the FET slice. 1 = Enable the FET slice. The default value is 1111111b for 34 W.

Register Name	DP16 IO Driver FET Slice Enable Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_IO_TX_FET_SLICE_P1_[n]
Address	800000780701143F (SCOM), +0x0400_0000_0000
Description	This register provides driver NFET and PFET slice enables. These values are used for all of the drivers on this DP16 instance when driving data out.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	EN_SLICE_N_WR: This field provides the driver NFET slice enable at 240 W/slice. Each bit in this multibit field controls one slice. 0 = Disable the FET slice. 1 = Enable the FET slice. The default value is 1111111b for 34 W.
56	RW	Reserved.
57:63	RW	EN_SLICE_P_WR: This field provides the driver PFET slice enable at 240 W/slice. Each bit in this multibit field controls one slice. 0 = Disable the FET slice. 1 = Enable the FET slice. The default value is 1111111b for 34 W.

Register Name	DP16 IO Driver FET Slice Enable Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_IO_TX_FET_SLICE_P2_[n]
Address	800000780701183F (SCOM), +0x0400_0000_0000
Description	This register provides driver NFET and PFET slice enables. These values are used for all of the drivers on this DP16 instance when driving data out.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	EN_SLICE_N_WR: This field provides the driver NFET slice enable at 240 W/slice. Each bit in this multibit field controls one slice. 0 = Disable the FET slice. 1 = Enable the FET slice. The default value is 1111111b for 34 W.

Bits	SCOM	Field Mnemonic: Description
56	RW	Reserved.
57:63	RW	EN_SLICE_P_WR: This field provides the driver PFET slice enable at 240 W/slice. Each bit in this multibit field controls one slice. 0 = Disable the FET slice. 1 = Enable the FET slice. The default value is 1111111b for 34 W.

Register Name	DP16 IO Driver FET Slice Enable Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_IO_TX_FET_SLICE_P3_[n]
Address	8000007807011C3F (SCOM), +0x0400_0000_0000
Description	This register provides driver NFET and PFET slice enables. These values are used for all of the drivers on this DP16 instance when driving data out.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	EN_SLICE_N_WR: This field provides the driver NFET slice enable at 240 W/slice. Each bit in this multibit field controls one slice. 0 = Disable the FET slice. 1 = Enable the FET slice. The default value is 1111111b for 34 W.
56	RW	Reserved.
57:63	RW	EN_SLICE_P_WR: This field provides the driver PFET slice enable at 240 W/slice. Each bit in this multibit field controls one slice. 0 = Disable the FET slice. 1 = Enable the FET slice. The default value is 1111111b for 34 W.

Register Name	DP16 Low Speed Probe Select Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_LO_PROBE_SELECT_P0_[n]
Address	8000007907011O3F (SCOM), +0x0400_0000_0000
Description	This register selects the sources of low-speed probing in DP16.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:49	RW	Reserved.
50:55	RW	LO_PROBE_SEL_A: Select source A into the low-speed probe tree.
56:57	RW	Reserved.
58:63	RW	LO_PROBE_SEL_B: Select source B into the low-speed probe tree.

Register Name	DP16 Low Speed Probe Select Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_LO_PROBE_SELECT_P1_[n]
Address	800000790701143F (SCOM), +0x0400_0000_0000
Description	This register selects the sources of low-speed probing in DP16.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:49	RW	Reserved.
50:55	RW	LO_PROBE_SEL_A: Select source A into the low-speed probe tree.
56:57	RW	Reserved.
58:63	RW	LO_PROBE_SEL_B: Select source B into the low-speed probe tree.

Register Name	DP16 Low Speed Probe Select Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_LO_PROBE_SELECT_P2_[n]
Address	800000790701183F (SCOM), +0x0400_0000_0000
Description	This register selects the sources of low-speed probing in DP16.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:49	RW	Reserved.
50:55	RW	LO_PROBE_SEL_A: Select source A into the low-speed probe tree.
56:57	RW	Reserved.
58:63	RW	LO_PROBE_SEL_B: Select source B into the low-speed probe tree.

Register Name	DP16 Low Speed Probe Select Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_LO_PROBE_SELECT_P3_[n]
Address	8000007907011C3F (SCOM), +0x0400_0000_0000
Description	This register selects the sources of low-speed probing in DP16.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:49	RW	Reserved.
50:55	RW	LO_PROBE_SEL_A: Select source A into the low-speed probe tree.
56:57	RW	Reserved.
58:63	RW	LO_PROBE_SEL_B: Select source B into the low-speed probe tree.

Register Name	DP16 Read VREF Calibration Error Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_CAL_ERROR_P0_[n]
Address	8000007A0701103F (SCOM), +0x0400_0000_0000
Description	The status of VREF calibration is reported in this register. Bits 48:63 correspond to the read VREF calibration circuitry in each bit of DQ 0:15.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RWX	VREF_CAL_ERROR: The status of VREF calibration for each bit of DQ 0:15 is reported in this register. When 1, no acceptable answer was found for the bit the last time calibration was run. No 0 →1 transition was found.

Register Name	DP16 Read VREF Calibration Error Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_CAL_ERROR_P1_[n]
Address	8000007A0701143F (SCOM), +0x0400_0000_0000
Description	The status of VREF calibration is reported in this register. Bits 48:63 correspond to the read VREF calibration circuitry in each bit of DQ 0:15.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RWX	VREF_CAL_ERROR: The status of VREF calibration for each bit of DQ 0:15 is reported in this register. When 1, no acceptable answer was found for the bit the last time calibration was run. No 0 →1 transition was found.

Register Name	DP16 Read VREF Calibration Error Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_CAL_ERROR_P2_[n]
Address	8000007A0701183F (SCOM), +0x0400_0000_0000
Description	The status of VREF calibration is reported in this register. Bits 48:63 correspond to the read VREF calibration circuitry in each bit of DQ 0:15.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RWX	VREF_CAL_ERROR: The status of VREF calibration for each bit of DQ 0:15 is reported in this register. When 1, no acceptable answer was found for the bit the last time calibration was run. No 0 →1 transition was found.

Register Name	DP16 Read VREF Calibration Error Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_CAL_ERROR_P3_[n]
Address	8000007A07011C3F (SCOM), +0x0400_0000_0000
Description	The status of VREF calibration is reported in this register. Bits 48:63 correspond to the read VREF calibration circuitry in each bit of DQ 0:15.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RWX	VREF_CAL_ERROR: The status of VREF calibration for each bit of DQ 0:15 is reported in this register. When 1, no acceptable answer was found for the bit the last time calibration was run. No 0 →1 transition was found.

Register Name	DP16 IO Driver P FET Slice Termination Enable Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_IO_TX_PFET_TERM_P0_[n]
Address	8000007B0701103F (SCOM), +0x0400_0000_0000
Description	This register provides driver PFET slice enables. These values are used for all of the drivers on this DP16 instance.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	EN_TERM_P_WR: This field provides the driver PFET slice enable. Each bit in this multibit field controls one slice. 1 = Enable the FET slice. 0 = Disable the FET slice. Bits 49:55 are connected to inputs ENSLICEPTERM_DC{1-7} on the analog core. Contact your IBM representative for the hardware values.
56:63	RW	Reserved.

Register Name	DP16 IO Driver P FET Slice Termination Enable Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_IO_TX_PFET_TERM_P1_[n]
Address	8000007B0701143F (SCOM), +0x0400_0000_0000
Description	This register provides driver PFET slice enables. These values are used for all of the drivers on this DP16 instance.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	EN_TERM_P_WR: This field provides the driver PFET slice enable. Each bit in this multibit field controls one slice. 1 = Enable the FET slice. 0 = Disable the FET slice. Bits 49:55 are connected to inputs ENSLICEPTERM_DC{1-7} on the analog core. Contact your IBM representative for the hardware values.
56:63	RW	Reserved.

Register Name	DP16 IO Driver P FET Slice Termination Enable Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_IO_TX_PFET_TERM_P2_[n]
Address	8000007B0701183F (SCOM), +0x0400_0000_0000
Description	This register provides driver PFET slice enables. These values are used for all of the drivers on this DP16 instance.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	EN_TERM_P_WR: This field provides the driver PFET slice enable. Each bit in this multibit field controls one slice. 1 = Enable the FET slice. 0 = Disable the FET slice. Bits 49:55 are connected to inputs ENSLICEPTERM_DC{1-7} on the analog core. Contact your IBM representative for the hardware values.
56:63	RW	Reserved.

Register Name	DP16 IO Driver P FET Slice Termination Enable Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_IO_TX_PFET_TERM_P3_[n]
Address	8000007B07011C3F (SCOM), +0x0400_0000_0000
Description	This register provides driver PFET slice enables. These values are used for all of the drivers on this DP16 instance.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	EN_TERM_P_WR: This field provides the driver PFET slice enable. Each bit in this multibit field controls one slice. 1 = Enable the FET slice. 0 = Disable the FET slice. Bits 49:55 are connected to inputs ENSLICEPTERM_DC{1-7} on the analog core. Contact your IBM representative for the hardware values.
56:63	RW	Reserved.

Register Name	DP16 DQ Bit Disable RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQ_BIT_DISABLE_RP0_P0_[n]
Address	8000007C0701103F (SCOM), +0x0400_0000_0000
Description	This register is used to disable each of the 16 pins on the DP16. During calibration operations, the hardware sets the bit in this register that corresponds to a pin on the DP16 that failed a calibration step. This register indicates which DQ pins on the DP16 failed a calibration step. This register does not indicate which calibration step failed.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DQ_BIT_DISABLE_0_15: 1 = Indicates that the DP16 bit is disabled and does not participate in any calibration steps. 0 = Indicates that the DP16 bit is not disabled. Bit 48 controls MEMINTD00B(n). Bit 49 controls MEMINTD01B(n). Bit 50 controls MEMINTD02B(n). ... Bit 63 controls MEMINTD15B(n). where n is the DP16 instance number.

Register Name	**DP16 DQ Bit Disable RP0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQ_BIT_DISABLE_RP0_P1_[n]
Address	8000007C0701143F (SCOM), +0x0400_0000_0000
Description	This register is used to disable each of the 16 pins on the DP16. During calibration operations, the hardware sets the bit in this register that corresponds to a pin on the DP16 that failed a calibration step. This register indicates which DQ pins on the DP16 failed a calibration step. This register does not indicate which calibration step failed.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DQ_BIT_DISABLE_0_15: 1 = Indicates that the DP16 bit is disabled and does not participate in any calibration steps. 0 = Indicates that the DP16 bit is not disabled. Bit 48 controls MEMINTD00B(n). Bit 49 controls MEMINTD01B(n). Bit 50 controls MEMINTD02B(n). ... Bit 63 controls MEMINTD15B(n). where n is the DP16 instance number.

Register Name	**DP16 DQ Bit Disable RP0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQ_BIT_DISABLE_RP0_P2_[n]
Address	8000007C0701183F (SCOM), +0x0400_0000_0000
Description	This register is used to disable each of the 16 pins on the DP16. During calibration operations, the hardware sets the bit in this register that corresponds to a pin on the DP16 that failed a calibration step. This register indicates which DQ pins on the DP16 failed a calibration step. This register does not indicate which calibration step failed.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DQ_BIT_DISABLE_0_15: 1 = Indicates that the DP16 bit is disabled and does not participate in any calibration steps. 0 = Indicates that the DP16 bit is not disabled. Bit 48 controls MEMINTD00B(n). Bit 49 controls MEMINTD01B(n). Bit 50 controls MEMINTD02B(n). ... Bit 63 controls MEMINTD15B(n). where n is the DP16 instance number.

Register Name	**DP16 DQ Bit Disable RP0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQ_BIT_DISABLE_RP0_P3_[n]
Address	8000007C07011C3F (SCOM), +0x0400_0000_0000
Description	This register is used to disable each of the 16 pins on the DP16. During calibration operations, the hardware sets the bit in this register that corresponds to a pin on the DP16 that failed a calibration step. This register indicates which DQ pins on the DP16 failed a calibration step. This register does not indicate which calibration step failed.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	DQ_BIT_DISABLE_0_15: 1 = Indicates that the DP16 bit is disabled and does not participate in any calibration steps. 0 = Indicates that the DP16 bit is not disabled. Bit 48 controls MEMINTD00B(n). Bit 49 controls MEMINTD01B(n). Bit 50 controls MEMINTD02B(n). ... Bit 63 controls MEMINTD15B(n). where n is the DP16 instance number.

Register Name	DP16 DQS Bit Disable RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQS_BIT_DISABLE_RP0_P0_[n]
Address	8000007D0701103F (SCOM), +0x0400_0000_0000
Description	This register is used to disable each of the eight DQS pins on the DP16. During calibration operations, the hardware sets the bit in this register that corresponds to a pin on the DP16 that failed a calibration step. This register indicates which DQS pins on the DP16 failed a calibration step. This register does not indicate which calibration step failed.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:55	RW	DQS_BIT_DISABLE_16_23: Bits are grouped in pairs. Bits 48:49, 50:51, 52:53, and 54:55 correspond to the differential DQS bits for each pair. 1 = Indicates that the DQS bits are disabled and do not participate in any calibration steps. Both DQS bits in the pair are set to 1b. 0 = Indicates that the DQS bits are not disabled. Both DQS bits in the pair are set to 0b. Bits 48:49 indicate the disable state of the DQS associated with QUAD0, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 50:51 indicate the disable state of the DQS associated with QUAD1, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 52:53 indicate the disable state of the DQS associated with QUAD2, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 54:55 indicate the disable state of the DQS associated with QUAD3, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register.
56:63	RO	Constant = 0b00000000

Register Name	DP16 DQS Bit Disable RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQS_BIT_DISABLE_RP0_P1_[n]
Address	8000007D0701143F (SCOM), +0x0400_0000_0000
Description	This register is used to disable each of the eight DQS pins on the DP16. During calibration operations, the hardware sets the bit in this register that corresponds to a pin on the DP16 that failed a calibration step. This register indicates which DQS pins on the DP16 failed a calibration step. This register does not indicate which calibration step failed.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:55	RW	DQS_BIT_DISABLE_16_23: Bits are grouped in pairs. Bits 48:49, 50:51, 52:53, and 54:55 correspond to the differential DQS bits for each pair. 1 = Indicates that the DQS bits are disabled and do not participate in any calibration steps. Both DQS bits in the pair are set to 1b. 0 = Indicates that the DQS bits are not disabled. Both DQS bits in the pair are set to 0b. Bits 48:49 indicate the disable state of the DQS associated with QUAD0, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 50:51 indicate the disable state of the DQS associated with QUAD1, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 52:53 indicate the disable state of the DQS associated with QUAD2, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 54:55 indicate the disable state of the DQS associated with QUAD3, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register.
56:63	RO	Constant = 0b00000000

Register Name	**DP16 DQS Bit Disable RP0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQS_BIT_DISABLE_RP0_P2_[n]
Address	8000007D0701183F (SCOM), +0x0400_0000_0000
Description	This register is used to disable each of the eight DQS pins on the DP16. During calibration operations, the hardware sets the bit in this register that corresponds to a pin on the DP16 that failed a calibration step. This register indicates which DQS pins on the DP16 failed a calibration step. This register does not indicate which calibration step failed.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:55	RW	DQS_BIT_DISABLE_16_23: Bits are grouped in pairs. Bits 48:49, 50:51, 52:53, and 54:55 correspond to the differential DQS bits for each pair. 1 = Indicates that the DQS bits are disabled and do not participate in any calibration steps. Both DQS bits in the pair are set to 1b. 0 = Indicates that the DQS bits are not disabled. Both DQS bits in the pair are set to 0b. Bits 48:49 indicate the disable state of the DQS associated with QUAD0, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 50:51 indicate the disable state of the DQS associated with QUAD1, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 52:53 indicate the disable state of the DQS associated with QUAD2, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 54:55 indicate the disable state of the DQS associated with QUAD3, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register.
56:63	RO	Constant = 0b00000000

Register Name	DP16 DQS Bit Disable RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQS_BIT_DISABLE_RP0_P3_[n]
Address	8000007D07011C3F (SCOM), +0x0400_0000_0000
Description	This register is used to disable each of the eight DQS pins on the DP16. During calibration operations, the hardware sets the bit in this register that corresponds to a pin on the DP16 that failed a calibration step. This register indicates which DQS pins on the DP16 failed a calibration step. This register does not indicate which calibration step failed.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:55	RW	DQS_BIT_DISABLE_16_23: Bits are grouped in pairs. Bits 48:49, 50:51, 52:53, and 54:55 correspond to the differential DQS bits for each pair. 1 = Indicates that the DQS bits are disabled and do not participate in any calibration steps. Both DQS bits in the pair are set to 1b. 0 = Indicates that the DQS bits are not disabled. Both DQS bits in the pair are set to 0b. Bits 48:49 indicate the disable state of the DQS associated with QUAD0, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 50:51 indicate the disable state of the DQS associated with QUAD1, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 52:53 indicate the disable state of the DQS associated with QUAD2, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 54:55 indicate the disable state of the DQS associated with QUAD3, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register.
56:63	RO	Constant = 0b00000000

Register Name	DP16 Write DQ Offset Value RP0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQ_WR_OFFSET_RP0_P0_[n]
Address	8000007E0701103F (SCOM), +0x0400_0000_0000
Description	This register contains an offset value for each quadrant. This offset allows the centered write data bits in each quadrant to be offset from the center as determined by the write-centering calibration algorithm. This register is used by the write-centering calibration state machine. This register must be configured, if needed, before the write-centering calibration algorithm is initiated. Changing the value of this register without running the write-centering calibration algorithm has no effect on the data bit write delay values.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:51	RW	DQ_WR_OFFSET_N0: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). The least-significant bit of the 5-bit value is always 0b.

Bits	SCOM	Field Mnemonic: Description
52:55	RW	DQ_WR_OFFSET_N1: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). The least-significant bit of the 5-bit value is always 0b.
56:59	RW	DQ_WR_OFFSET_N2: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). The least-significant bit of the 5-bit value is always 0b.
60:63	RW	DQ_WR_OFFSET_N3: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). The least-significant bit of the 5-bit value is always 0b.

Register Name	**DP16 Write DQ Offset Value RP0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQ_WR_OFFSET_RP0_P1_[n]
Address	8000007E0701143F (SCOM), +0x0400_0000_0000
Description	This register contains an offset value for each quadrant. This offset allows the centered write data bits in each quadrant to be offset from the center as determined by the write-centering calibration algorithm. This register is used by the write-centering calibration state machine. This register must be configured, if needed, before the write-centering calibration algorithm is initiated. Changing the value of this register without running the write-centering calibration algorithm has no effect on the data bit write delay values.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	DQ_WR_OFFSET_N0: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). The least-significant bit of the 5-bit value is always 0b.

Bits	SCOM	Field Mnemonic: Description
52:55	RW	DQ_WR_OFFSET_N1: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). The least-significant bit of the 5-bit value is always 0b.
56:59	RW	DQ_WR_OFFSET_N2: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). The least-significant bit of the 5-bit value is always 0b.
60:63	RW	DQ_WR_OFFSET_N3: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). The least-significant bit of the 5-bit value is always 0b.

Register Name	**DP16 Write DQ Offset Value RP0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQ_WR_OFFSET_RP0_P2_[n]
Address	8000007E0701183F (SCOM), +0x0400_0000_0000
Description	This register contains an offset value for each quadrant. This offset allows the centered write data bits in each quadrant to be offset from the center as determined by the write-centering calibration algorithm. This register is used by the write-centering calibration state machine. This register must be configured, if needed, before the write-centering calibration algorithm is initiated. Changing the value of this register without running the write-centering calibration algorithm has no effect on the data bit write delay values.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	DQ_WR_OFFSET_N0: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). The least-significant bit of the 5-bit value is always 0b.

Bits	SCOM	Field Mnemonic: Description
52:55	RW	DQ_WR_OFFSET_N1: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). The least-significant bit of the 5-bit value is always 0b.
56:59	RW	DQ_WR_OFFSET_N2: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). The least-significant bit of the 5-bit value is always 0b.
60:63	RW	DQ_WR_OFFSET_N3: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). The least-significant bit of the 5-bit value is always 0b.

Register Name	**DP16 Write DQ Offset Value RP0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQ_WR_OFFSET_RP0_P3_[n]
Address	8000007E07011C3F (SCOM), +0x0400_0000_0000
Description	This register contains an offset value for each quadrant. This offset allows the centered write data bits in each quadrant to be offset from the center as determined by the write-centering calibration algorithm. This register is used by the write-centering calibration state machine. This register must be configured, if needed, before the write-centering calibration algorithm is initiated. Changing the value of this register without running the write-centering calibration algorithm has no effect on the data bit write delay values.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	DQ_WR_OFFSET_N0: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). The least-significant bit of the 5-bit value is always 0b.

Bits	SCOM	Field Mnemonic: Description
52:55	RW	DQ_WR_OFFSET_N1: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). The least-significant bit of the 5-bit value is always 0b.
56:59	RW	DQ_WR_OFFSET_N2: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). The least-significant bit of the 5-bit value is always 0b.
60:63	RW	DQ_WR_OFFSET_N3: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). The least-significant bit of the 5-bit value is always 0b.

Register Name	DP16 SysClk 1 Phase Rotator Control Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_SYSCLK_PR1_P0_[n]
Address	8000007F0701103F (SCOM), +0x0400_0000_0000
Description	This register controls the circuit that aligns the internal SysClk 1 to the incoming dphy_gckn clock.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	Reserved.

Bits	SCOM	Field Mnemonic: Description
49:55	RW	SYSCLK_ROT_OVERRIDE: System clock (SysClk) phase rotator override value. This field has a dual purpose: override control and lock control. When SYSCLK_ROT_OVERRIDE_EN = 1b, this field is in override control mode. When SYSCLK_ROT_OVERRIDE_EN = 0b, this field is in lock control mode. For override control: The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by four dphy_gckn clock cycles. Back-to-back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field in the DP16 SysClk 1 Phase Rotator Control Register is reserved. For lock control: Write this field to all zeros unless instructed otherwise by your IBM representative. Bit 50: Lock select: Selects between lock status and sticky lock. 0 = Selects the status of the lock. When the dphy_gckn detects that it has reached alignment between the dphy_gckn and SysClk, the BB_LOCK field in the DP16 SysClk 1 Phase Rotator Control Register is asserted. 1 = Selects the sticky lock to the BB_LOCK field in the DP16 SysClk 1 Phase Rotator Control Register. The sticky lock is controlled by bit 52, sticky lock enable. After the sticky lock is set, it remains set. Bit 52: Sticky lock enable. Bits 53:55 000 = At most, a 1-count increment or decrement occurs to indicate a lock. 001 = At most, a 2-count increment or decrement occurs to indicate a lock. 010 = At most, a 3-count increment or decrement occurs to indicate a lock. 011 = At most, a 4-count increment or decrement occurs to indicate a lock. 100 = At most, a 5-count increment or decrement occurs to indicate a lock.
56	RW	SYSCLK_ROT_OVERRIDE_EN: This field enables the use of the SYSCLK_ROT_OVERRIDE field, rather than the internally calculated SYSCLK_ROT value, when set to 1b. The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by four dphy_gckn clock cycles. Back-to-back advanced peripheral bus (APB) write operations to this register provide the required separation. When this bit is written to 0b and was 1b, the SYSCLK_ROT value in the DP16 SysClk 1 Phase Rotator Control Register resets to zero.
57	RW	SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_gckn, the SysClk phase alignment controller. Must be asserted after the PLL locks, and must be active for at least five SysClk cycles.
58	RW	SYSCLK_PHASE_CNTL_EN: Alignment enable to dphy_gckn, the SysClk phase alignment controller. Must be asserted low at least 25 SysClk cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.
59	RW	SYSCLK_PHASE_DEFAULT_EN: This field enables default startup values to be output by dphy_gckn, the SysClk phase alignment controller. This bit must be asserted during system reset and de-asserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	SYSCLK_POS_EDGE_ALIGN: This field must be 0b for proper functional operation. It is an edge-alignment strap to dphy_gckn, the SysClk phase alignment controller. 0 = Negative edge alignment of the SysClk to the positive edge of dphy_gckn. 1 = Positive edge alignment of the SysClk to the positive edge of dphy_gckn.
61	RW	CONTINUOUS_UPDATE: 0 = The dphy_gckn, the SysClk phase alignment controller, is only updated periodically under hardware control when an update does not interfere with the PHY functional operations. 1 = The dphy_gckn, the SysClk phase alignment controller, runs continuously. Thus, it continuously aligns the dphy_gckn clock to the internal SysClk clock.
62:63	RO	Constant = 0b00

Register Name	DP16 SysClk 1 Phase Rotator Control Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_SYSCLK_PR1_P1_[n]
Address	8000007F0701143F (SCOM), +0x0400_0000_0000
Description	This register controls the circuit that aligns the internal SysClk 1 to the incoming dphy_gckn clock.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	SYSCLK_ROT_OVERRIDE: System clock (SysClk) phase rotator override value. This field has a dual purpose: override control and lock control. When SYSCLK_ROT_OVERRIDE_EN = 1b, this field is in override control mode. When SYSCLK_ROT_OVERRIDE_EN = 0b, this field is in lock control mode. For override control: The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by four dphy_gckn clock cycles. Back-to-back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field in the DP16 SysClk 1 Phase Rotator Control Register is reserved. For lock control: Write this field to all zeros unless instructed otherwise by your IBM representative. Bit 50: Lock select: Selects between lock status and sticky lock. 0 = Selects the status of the lock. When the dphy_gckn detects that it has reached alignment between the dphy_gckn and SysClk, the BB_LOCK field in the DP16 SysClk 1 Phase Rotator Control Register is asserted. 1 = Selects the sticky lock to the BB_LOCK field in the DP16 SysClk 1 Phase Rotator Control Register. The sticky lock is controlled by bit 52, sticky lock enable. After the sticky lock is set, it remains set. Bit 52: Sticky lock enable. Bits 53:55 000 = At most, a 1-count increment or decrement occurs to indicate a lock. 001 = At most, a 2-count increment or decrement occurs to indicate a lock. 010 = At most, a 3-count increment or decrement occurs to indicate a lock. 011 = At most, a 4-count increment or decrement occurs to indicate a lock. 100 = At most, a 5-count increment or decrement occurs to indicate a lock.
56	RW	SYSCLK_ROT_OVERRIDE_EN: This field enables the use of the SYSCLK_ROT_OVERRIDE field, rather than the internally calculated SYSCLK_ROT value, when set to 1b. The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by four dphy_gckn clock cycles. Back-to-back APB write operations to this register provide the required separation. When this bit is written to 0b and was 1b, the SYSCLK_ROT value in the DP16 SysClk 1 Phase Rotator Control Register resets to zero.
57	RW	SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_gckn, the SysClk phase alignment controller. Must be asserted after the PLL locks, and must be active for at least five SysClk cycles.
58	RW	SYSCLK_PHASE_CNTL_EN: Alignment enable to dphy_gckn, the SysClk phase alignment controller. Must be asserted low at least 25 SysClk cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.
59	RW	SYSCLK_PHASE_DEFAULT_EN: This field enables default startup values to be output by dphy_gckn, the SysClk phase alignment controller. This bit must be asserted during system reset and de-asserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	SYSCLK_POS_EDGE_ALIGN: This field must be 0b for proper functional operation. It is an edge-alignment strap to dphy_gckn, the SysClk phase alignment controller. 0 = Negative edge alignment of the SysClk to the positive edge of dphy_gckn. 1 = Positive edge alignment of the SysClk to the positive edge of dphy_gckn.

Bits	SCOM	Field Mnemonic: Description
61	RW	CONTINUOUS_UPDATE: 0 = The dphy_gckn, the SysClk phase alignment controller, is only updated periodically under hardware control when an update does not interfere with the PHY functional operations. 1 = The dphy_gckn, the SysClk phase alignment controller, runs continuously. Thus, it continuously aligns the dphy_gckn clock to the internal SysClk clock.
62:63	RO	Constant = 0b00

Register Name	DP16 SysClk 1 Phase Rotator Control Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_SYSCLK_PR1_P2_[n]
Address	8000007F0701183F (SCOM), +0x0400_0000_0000
Description	This register controls the circuit that aligns the internal SysClk 1 to the incoming dphy_gckn clock.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	SYSCLK_ROT_OVERRIDE: System clock (SysClk) phase rotator override value. This field has a dual purpose: override control and lock control. When SYSCLK_ROT_OVERRIDE_EN = 1b, this field is in override control mode. When SYSCLK_ROT_OVERRIDE_EN = 0b, this field is in lock control mode. For override control: The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by four dphy_gckn clock cycles. Back-to-back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field in the DP16 SysClk 1 Phase Rotator Control Register is reserved. For lock control: Write this field to all zeros unless instructed otherwise by your IBM representative. Bit 50: Lock select: Selects between lock status and sticky lock. 0 = Selects the status of the lock. When the dphy_gckn detects that it has reached alignment between the dphy_gckn and SysClk, the BB_LOCK field in the DP16 SysClk 1 Phase Rotator Control Register is asserted. 1 = Selects the sticky lock to the BB_LOCK field in the DP16 SysClk 1 Phase Rotator Control Register. The sticky lock is controlled by bit 52, sticky lock enable. After the sticky lock is set, it remains set. Bit 52: Sticky lock enable. Bits 53:55 000 = At most, a 1-count increment or decrement occurs to indicate a lock. 001 = At most, a 2-count increment or decrement occurs to indicate a lock. 010 = At most, a 3-count increment or decrement occurs to indicate a lock. 011 = At most, a 4-count increment or decrement occurs to indicate a lock. 100 = At most, a 5-count increment or decrement occurs to indicate a lock.
56	RW	SYSCLK_ROT_OVERRIDE_EN: This field enables the use of the SYSCLK_ROT_OVERRIDE field, rather than the internally calculated SYSCLK_ROT value, when set to 1b. The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by four dphy_gckn clock cycles. Back-to-back APB write operations to this register provide the required separation. When this bit is written to 0b and was 1b, the SYSCLK_ROT value in the DP16 SysClk 1 Phase Rotator Control Register resets to zero.
57	RW	SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_gckn, the SysClk phase alignment controller. Must be asserted after the PLL locks, and must be active for at least five SysClk cycles.
58	RW	SYSCLK_PHASE_CNTL_EN: Alignment enable to dphy_gckn, the SysClk phase alignment controller. Must be asserted low at least 25 SysClk cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.

Bits	SCOM	Field Mnemonic: Description
59	RW	SYSCLK_PHASE_DEFAULT_EN: This field enables default startup values to be output by dphy_gckn, the SysClk phase alignment controller. This bit must be asserted during system reset and de-asserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	SYSCLK_POS_EDGE_ALIGN: This field must be 0b for proper functional operation. It is an edge-alignment strap to dphy_gckn, the SysClk phase alignment controller. 0 = Negative edge alignment of the SysClk to the positive edge of dphy_gckn. 1 = Positive edge alignment of the SysClk to the positive edge of dphy_gckn.
61	RW	CONTINUOUS_UPDATE: 0 = The dphy_gckn, the SysClk phase alignment controller, is only updated periodically under hardware control when an update does not interfere with the PHY functional operations. 1 = The dphy_gckn, the SysClk phase alignment controller, runs continuously. Thus, it continuously aligns the dphy_gckn clock to the internal SysClk clock.
62:63	RO	Constant = 0b00

Register Name	DP16 SysClk 1 Phase Rotator Control Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_SYSCLK_PR1_P3_[n]
Address	8000007F07011C3F (SCOM), +0x0400_0000_0000
Description	This register controls the circuit that aligns the internal SysClk 1 to the incoming dphy_gckn clock.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	SYSCLK_ROT_OVERRIDE: System clock (SysClk) phase rotator override value. This field has a dual purpose: override control and lock control. When SYSCLK_ROT_OVERRIDE_EN = 1b, this field is in override control mode. When SYSCLK_ROT_OVERRIDE_EN = 0b, this field is in lock control mode. For override control: The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by four dphy_gckn clock cycles. Back-to-back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field in the DP16 SysClk 1 Phase Rotator Control Register is reserved. For lock control: Write this field to all zeros unless instructed otherwise by your IBM representative. Bit 50: Lock select: Selects between lock status and sticky lock. 0 = Selects the status of the lock. When the dphy_gckn detects that it has reached alignment between the dphy_gckn and SysClk, the BB_LOCK field in the DP16 SysClk 1 Phase Rotator Control Register is asserted. 1 = Selects the sticky lock to the BB_LOCK field in the DP16 SysClk 1 Phase Rotator Control Register. The sticky lock is controlled by bit 52, sticky lock enable. After the sticky lock is set, it remains set. Bit 52: Sticky lock enable. Bits 53:55 000 = At most, a 1-count increment or decrement occurs to indicate a lock. 001 = At most, a 2-count increment or decrement occurs to indicate a lock. 010 = At most, a 3-count increment or decrement occurs to indicate a lock. 011 = At most, a 4-count increment or decrement occurs to indicate a lock. 100 = At most, a 5-count increment or decrement occurs to indicate a lock.

Bits	SCOM	Field Mnemonic: Description
56	RW	SYSCLK_ROT_OVERRIDE_EN: This field enables the use of the SYSCLK_ROT_OVERRIDE field, rather than the internally calculated SYSCLK_ROT value, when set to 1b. The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by four dphy_gckn clock cycles. Back-to-back APB write operations to this register provide the required separation. When this bit is written to 0b and was 1b, the SYSCLK_ROT value in the DP16 SysClk 1 Phase Rotator Control Register resets to zero.
57	RW	SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_gckn, the SysClk phase alignment controller. Must be asserted after the PLL locks, and must be active for at least five SysClk cycles.
58	RW	SYSCLK_PHASE_CNTL_EN: Alignment enable to dphy_gckn, the SysClk phase alignment controller. Must be asserted low at least 25 SysClk cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.
59	RW	SYSCLK_PHASE_DEFAULT_EN: This field enables default startup values to be output by dphy_gckn, the SysClk phase alignment controller. This bit must be asserted during system reset and de-asserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	SYSCLK_POS_EDGE_ALIGN: This field must be 0b for proper functional operation. It is an edge-alignment strap to dphy_gckn, the SysClk phase alignment controller. 0 = Negative edge alignment of the SysClk to the positive edge of dphy_gckn. 1 = Positive edge alignment of the SysClk to the positive edge of dphy_gckn.
61	RW	CONTINUOUS_UPDATE: 0 = The dphy_gckn, the SysClk phase alignment controller, is only updated periodically under hardware control when an update does not interfere with the PHY functional operations. 1 = The dphy_gckn, the SysClk phase alignment controller, runs continuously. Thus, it continuously aligns the dphy_gckn clock to the internal SysClk clock.
62:63	RO	Constant = 0b00

Register Name	DP16 DCD Control 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DCD_CONTROL0_P0_[n]
Address	800000A40701103F (SCOM), +0x0400_0000_0000
Description	This register controls the duty cycle distortion (DCD) analog circuitry on the clock feeding the DLL. Note: When writing the register, software must write bit 63 to b0 to avoid a parity error.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	DLL_DCD_ADJUST: This value controls the amount of duty cycle correction that occurs on the grid clock before it enters the DLL. As the value increases, the clock = 1 part gets longer. As values decrease, the clock = 0 part gets longer. This is the seed value for the DCD calibration algorithm.
56	RW	DLL_DCD_CORRECT_EN: This bit determines whether the duty cycle distortion logic in the DLL includes a loop to further correct for DCD. 0 = The loop is not included. 1 = The loop is included.
57	RW	DLL_DCD_ITER_A: This bit controls the connection of the DCD comparator input to the null out comparator offset. 0 = B answer. 1 = A answer. The A and B answers must be averaged to determine the DLL_DCD_ADJUST value.
58	RW	DLL_DCD_CAL_ENABLE: This is the DCD calibration enable bit. 0 = Resets the calibration state machine (clears DLL_DCD_CAL_DONE and DLL_DCD_CAL_ERROR). 1 = Enables calibration (calibration is complete with the assertion of DLL_DCD_CAL_DONE).

Bits	SCOM	Field Mnemonic: Description
59	RO	Reserved.
60	RW	DLL_DCD_POWERDOWN: 0 = Normal operation. 1 = Power down the DCD circuit for power savings.
61	RWX	DLL_DCD_CAL_DONE: When DCD_CAL_ENABLE is set, this bit indicates that the calibration is complete and the calibrated value has been loaded into the DLL_DCD_ADJUST field of this register.
62	RWX	DLL_DCD_CAL_ERROR: If this bit is asserted along with DLL_DCD_CAL_DONE, it indicates that the calibration failed to find a solution. Either DLL_DCD_ADJUST reached a maximum value of 0xFF, or a minimum value of 0x00.
63	RO	DLL_DCD_COMPARE_OUT: (Read only.) This bit indicates the result of the DCD comparator. 0 = Need to increase DLL_DCD_ADJUST. 1 = Need to decrease DLL_DCD_ADJUST.

Register Name	**DP16 DCD Control 0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DCD_CONTROL0_P1_[n]
Address	800000A40701143F (SCOM), +0x0400_0000_0000
Description	This register controls the duty cycle distortion (DCD) analog circuitry on the clock feeding the DLL. Note: When writing the register, software must write bit 63 to b0 to avoid a parity error.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	DLL_DCD_ADJUST: This value controls the amount of duty cycle correction that occurs on the grid clock before it enters the DLL. As the value increases, the clock = 1 part gets longer. As values decrease, the clock = 0 part gets longer. This is the seed value for the DCD calibration algorithm.
56	RW	DLL_DCD_CORRECT_EN: This bit determines whether the duty cycle distortion logic in the DLL includes a loop to further correct for DCD. 0 = The loop is not included. 1 = The loop is included.
57	RW	DLL_DCD_ITER_A: This bit controls the connection of the DCD comparator input to the null out comparator offset. 0 = B answer. 1 = A answer. The A and B answers must be averaged to determine the DLL_DCD_ADJUST value.
58	RW	DLL_DCD_CAL_ENABLE: This is the DCD calibration enable bit. 0 = Resets the calibration state machine (clears DLL_DCD_CAL_DONE and DLL_DCD_CAL_ERROR). 1 = Enables calibration (calibration is complete with the assertion of DLL_DCD_CAL_DONE).
59	RO	Reserved.
60	RW	DLL_DCD_POWERDOWN: 0 = Normal operation. 1 = Power down the DCD circuit for power savings.
61	RWX	DLL_DCD_CAL_DONE: When DCD_CAL_ENABLE is set, this bit indicates that the calibration is complete and the calibrated value has been loaded into the DLL_DCD_ADJUST field of this register.
62	RWX	DLL_DCD_CAL_ERROR: If this bit is asserted along with DLL_DCD_CAL_DONE, it indicates that the calibration failed to find a solution. Either DLL_DCD_ADJUST reached a maximum value of 0xFF, or a minimum value of 0x00.
63	RO	DLL_DCD_COMPARE_OUT: (Read only.) This bit indicates the result of the DCD comparator. 0 = Need to increase DLL_DCD_ADJUST. 1 = Need to decrease DLL_DCD_ADJUST.

Register Name	DP16 DCD Control 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DCD_CONTROL0_P2_[n]
Address	800000A40701183F (SCOM), +0x0400_0000_0000
Description	This register controls the duty cycle distortion (DCD) analog circuitry on the clock feeding the DLL. Note: When writing the register, software must write bit 63 to b0 to avoid a parity error.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:55	RWX	DLL_DCD_ADJUST: This value controls the amount of duty cycle correction that occurs on the grid clock before it enters the DLL. As the value increases, the clock = 1 part gets longer. As values decrease, the clock = 0 part gets longer. This is the seed value for the DCD calibration algorithm.
56	RW	DLL_DCD_CORRECT_EN: This bit determines whether the duty cycle distortion logic in the DLL includes a loop to further correct for DCD. 0 = The loop is not included. 1 = The loop is included.
57	RW	DLL_DCD_ITER_A: This bit controls the connection of the DCD comparator input to the null out comparator offset. 0 = B answer. 1 = A answer. The A and B answers must be averaged to determine the DLL_DCD_ADJUST value.
58	RW	DLL_DCD_CAL_ENABLE: This is the DCD calibration enable bit. 0 = Resets the calibration state machine (clears DLL_DCD_CAL_DONE and DLL_DCD_CAL_ERROR). 1 = Enables calibration (calibration is complete with the assertion of DLL_DCD_CAL_DONE).
59	RO	Reserved.
60	RW	DLL_DCD_POWERDOWN: 0 = Normal operation. 1 = Power down the DCD circuit for power savings.
61	RWX	DLL_DCD_CAL_DONE: When DCD_CAL_ENABLE is set, this bit indicates that the calibration is complete and the calibrated value has been loaded into the DLL_DCD_ADJUST field of this register.
62	RWX	DLL_DCD_CAL_ERROR: If this bit is asserted along with DLL_DCD_CAL_DONE, it indicates that the calibration failed to find a solution. Either DLL_DCD_ADJUST reached a maximum value of 0xFF, or a minimum value of 0x00.
63	RO	DLL_DCD_COMPARE_OUT: (Read only.) This bit indicates the result of the DCD comparator. 0 = Need to increase DLL_DCD_ADJUST. 1 = Need to decrease DLL_DCD_ADJUST.

Register Name	DP16 DCD Control 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DCD_CONTROL0_P3_[n]
Address	800000A407011C3F (SCOM), +0x0400_0000_0000
Description	This register controls the duty cycle distortion (DCD) analog circuitry on the clock feeding the DLL. Note: When writing the register, software must write bit 63 to b0 to avoid a parity error.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:55	RWX	DLL_DCD_ADJUST: This value controls the amount of duty cycle correction that occurs on the grid clock before it enters the DLL. As the value increases, the clock = 1 part gets longer. As values decrease, the clock = 0 part gets longer. This is the seed value for the DCD calibration algorithm.

Bits	SCOM	Field Mnemonic: Description
56	RW	DLL_DCD_CORRECT_EN: This bit determines whether the duty cycle distortion logic in the DLL includes a loop to further correct for DCD. 0 = The loop is not included. 1 = The loop is included.
57	RW	DLL_DCD_ITER_A: This bit controls the connection of the DCD comparator input to the null out comparator offset. 0 = B answer. 1 = A answer. The A and B answers must be averaged to determine the DLL_DCD_ADJUST value.
58	RW	DLL_DCD_CAL_ENABLE: This is the DCD calibration enable bit. 0 = Resets the calibration state machine (clears DLL_DCD_CAL_DONE and DLL_DCD_CAL_ERROR). 1 = Enables calibration (calibration is complete with the assertion of DLL_DCD_CAL_DONE).
59	RO	Reserved.
60	RW	DLL_DCD_POWERDOWN: 0 = Normal operation. 1 = Power down the DCD circuit for power savings.
61	RWX	DLL_DCD_CAL_DONE: When DCD_CAL_ENABLE is set, this bit indicates that the calibration is complete and the calibrated value has been loaded into the DLL_DCD_ADJUST field of this register.
62	RWX	DLL_DCD_CAL_ERROR: If this bit is asserted along with DLL_DCD_CAL_DONE, it indicates that the calibration failed to find a solution. Either DLL_DCD_ADJUST reached a maximum value of 0xFF, or a minimum value of 0x00.
63	RO	DLL_DCD_COMPARE_OUT: (Read only.) This bit indicates the result of the DCD comparator. 0 = Need to increase DLL_DCD_ADJUST. 1 = Need to decrease DLL_DCD_ADJUST.

Register Name	DP16 DCD Control 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DCD_CONTROL1_P0_[n]
Address	800000A50701103F (SCOM), +0x0400_0000_0000
Description	This register controls the duty cycle distortion (DCD) analog circuitry on the clock feeding the DLL. Note: When writing the register, software must write bit 63 to b0 to avoid a parity error.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	DLL_DCD_ADJUST: This value controls the amount of duty cycle correction that occurs on the grid clock before it enters the DLL. As the value increases, the clock = 1 part gets longer. As values decrease, the clock = 0 part gets longer. This is the seed value for the DCD calibration algorithm.
56	RW	DLL_DCD_CORRECT_EN: This bit determines whether the duty cycle distortion logic in the DLL includes a loop to further correct for DCD. 0 = The loop is not included. 1 = The loop is included.
57	RW	DLL_DCD_ITER_A: This bit controls the connection of the DCD comparator input to the null out comparator offset. 0 = B answer. 1 = A answer. The A and B answers must be averaged to determine the DLL_DCD_ADJUST value.
58	RW	DLL_DCD_CAL_ENABLE: This is the DCD calibration enable bit. 0 = Resets the calibration state machine (clears DLL_DCD_CAL_DONE and DLL_DCD_CAL_ERROR). 1 = Enables calibration (calibration is complete with the assertion of DLL_DCD_CAL_DONE).
59	RO	Reserved.

Bits	SCOM	Field Mnemonic: Description
60	RW	DLL_DCD_POWERDOWN: 0 = Normal operation. 1 = Power down the DCD circuit for power savings.
61	RWX	DLL_DCD_CAL_DONE: When DCD_CAL_ENABLE is set, this bit indicates that the calibration is complete and the calibrated value has been loaded into the DLL_DCD_ADJUST field of this register.
62	RWX	DLL_DCD_CAL_ERROR: If this bit is asserted along with DLL_DCD_CAL_DONE, it indicates that the calibration failed to find a solution. Either DLL_DCD_ADJUST reached a maximum value of 0xFF, or a minimum value of 0x00.
63	RO	DLL_DCD_COMPARE_OUT: (Read only.) This bit indicates the result of the DCD comparator. 0 = Need to increase DLL_DCD_ADJUST. 1 = Need to decrease DLL_DCD_ADJUST.

Register Name	DP16 DCD Control 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DCD_CONTROL1_P1_[n]
Address	800000A50701143F (SCOM), +0x0400_0000_0000
Description	This register controls the duty cycle distortion (DCD) analog circuitry on the clock feeding the DLL. Note: When writing the register, software must write bit 63 to b0 to avoid a parity error.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:55	RWX	DLL_DCD_ADJUST: This value controls the amount of duty cycle correction that occurs on the grid clock before it enters the DLL. As the value increases, the clock = 1 part gets longer. As values decrease, the clock = 0 part gets longer. This is the seed value for the DCD calibration algorithm.
56	RW	DLL_DCD_CORRECT_EN: This bit determines whether the duty cycle distortion logic in the DLL includes a loop to further correct for DCD. 0 = The loop is not included. 1 = The loop is included.
57	RW	DLL_DCD_ITER_A: This bit controls the connection of the DCD comparator input to the null out comparator offset. 0 = B answer. 1 = A answer. The A and B answers must be averaged to determine the DLL_DCD_ADJUST value.
58	RW	DLL_DCD_CAL_ENABLE: This is the DCD calibration enable bit. 0 = Resets the calibration state machine (clears DLL_DCD_CAL_DONE and DLL_DCD_CAL_ERROR). 1 = Enables calibration (calibration is complete with the assertion of DLL_DCD_CAL_DONE).
59	RO	Reserved.
60	RW	DLL_DCD_POWERDOWN: 0 = Normal operation. 1 = Power down the DCD circuit for power savings.
61	RWX	DLL_DCD_CAL_DONE: When DCD_CAL_ENABLE is set, this bit indicates that the calibration is complete and the calibrated value has been loaded into the DLL_DCD_ADJUST field of this register.
62	RWX	DLL_DCD_CAL_ERROR: If this bit is asserted along with DLL_DCD_CAL_DONE, it indicates that the calibration failed to find a solution. Either DLL_DCD_ADJUST reached a maximum value of 0xFF, or a minimum value of 0x00.
63	RO	DLL_DCD_COMPARE_OUT: (Read only.) This bit indicates the result of the DCD comparator. 0 = Need to increase DLL_DCD_ADJUST. 1 = Need to decrease DLL_DCD_ADJUST.

Register Name	DP16 DCD Control 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DCD_CONTROL1_P2_[n]
Address	800000A50701183F (SCOM), +0x0400_0000_0000
Description	This register controls the duty cycle distortion (DCD) analog circuitry on the clock feeding the DLL. Note: When writing the register, software must write bit 63 to b0 to avoid a parity error.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:55	RWX	DLL_DCD_ADJUST: This value controls the amount of duty cycle correction that occurs on the grid clock before it enters the DLL. As the value increases, the clock = 1 part gets longer. As values decrease, the clock = 0 part gets longer. This is the seed value for the DCD calibration algorithm.
56	RW	DLL_DCD_CORRECT_EN: This bit determines whether the duty cycle distortion logic in the DLL includes a loop to further correct for DCD. 0 = The loop is not included. 1 = The loop is included.
57	RW	DLL_DCD_ITER_A: This bit controls the connection of the DCD comparator input to the null out comparator offset. 0 = B answer. 1 = A answer. The A and B answers must be averaged to determine the DLL_DCD_ADJUST value.
58	RW	DLL_DCD_CAL_ENABLE: This is the DCD calibration enable bit. 0 = Resets the calibration state machine (clears DLL_DCD_CAL_DONE and DLL_DCD_CAL_ERROR). 1 = Enables calibration (calibration is complete with the assertion of DLL_DCD_CAL_DONE).
59	RO	Reserved.
60	RW	DLL_DCD_POWERDOWN: 0 = Normal operation. 1 = Power down the DCD circuit for power savings.
61	RWX	DLL_DCD_CAL_DONE: When DCD_CAL_ENABLE is set, this bit indicates that the calibration is complete and the calibrated value has been loaded into the DLL_DCD_ADJUST field of this register.
62	RWX	DLL_DCD_CAL_ERROR: If this bit is asserted along with DLL_DCD_CAL_DONE, it indicates that the calibration failed to find a solution. Either DLL_DCD_ADJUST reached a maximum value of 0xFF, or a minimum value of 0x00.
63	RO	DLL_DCD_COMPARE_OUT: (Read only.) This bit indicates the result of the DCD comparator. 0 = Need to increase DLL_DCD_ADJUST. 1 = Need to decrease DLL_DCD_ADJUST.

Register Name	DP16 DCD Control 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DCD_CONTROL1_P3_[n]
Address	800000A507011C3F (SCOM), +0x0400_0000_0000
Description	This register controls the duty cycle distortion (DCD) analog circuitry on the clock feeding the DLL. Note: When writing the register, software must write bit 63 to b0 to avoid a parity error.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:55	RWX	DLL_DCD_ADJUST: This value controls the amount of duty cycle correction that occurs on the grid clock before it enters the DLL. As the value increases, the clock = 1 part gets longer. As values decrease, the clock = 0 part gets longer. This is the seed value for the DCD calibration algorithm.

Bits	SCOM	Field Mnemonic: Description
56	RW	DLL_DCD_CORRECT_EN: This bit determines whether the duty cycle distortion logic in the DLL includes a loop to further correct for DCD. 0 = The loop is not included. 1 = The loop is included.
57	RW	DLL_DCD_ITER_A: This bit controls the connection of the DCD comparator input to the null out comparator offset. 0 = B answer. 1 = A answer. The A and B answers must be averaged to determine the DLL_DCD_ADJUST value.
58	RW	DLL_DCD_CAL_ENABLE: This is the DCD calibration enable bit. 0 = Resets the calibration state machine (clears DLL_DCD_CAL_DONE and DLL_DCD_CAL_ERROR). 1 = Enables calibration (calibration is complete with the assertion of DLL_DCD_CAL_DONE).
59	RO	Reserved.
60	RW	DLL_DCD_POWERDOWN: 0 = Normal operation. 1 = Power down the DCD circuit for power savings.
61	RWX	DLL_DCD_CAL_DONE: When DCD_CAL_ENABLE is set, this bit indicates that the calibration is complete and the calibrated value has been loaded into the DLL_DCD_ADJUST field of this register.
62	RWX	DLL_DCD_CAL_ERROR: If this bit is asserted along with DLL_DCD_CAL_DONE, it indicates that the calibration failed to find a solution. Either DLL_DCD_ADJUST reached a maximum value of 0xFF, or a minimum value of 0x00.
63	RO	DLL_DCD_COMPARE_OUT: (Read only.) This bit indicates the result of the DCD comparator. 0 = Need to increase DLL_DCD_ADJUST. 1 = Need to decrease DLL_DCD_ADJUST.

Register Name	**DP16 DLL Software Control 0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DLL_SW_CONTROL0_P0_[n]
Address	800000A60701103F (SCOM), +0x0400_0000_0000
Description	This register exposes internal DLL signals to software to allow it to override the hardware DLL calibration algorithm. "META" indicates that the signals have safely crossed into the grid clock domain, so they should not exhibit metastability. Non-meta signals can be read after they stabilize.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	DLL_SW_OVERRIDE: When 0, the hardware DLL algorithm is used. When 1, this register takes control over the DLL analog inputs and outputs, allowing firmware to perform calibration.
49	RW	DLL_SW_CAL_PD_ENABLE: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_CAL_PD_ENABLE_SLOW.
50	RW	DLL_SW_MAIN_PD_ENABLE: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_MAIN_PD_ENABLE_SLOW.
51	RW	DLL_SW_DETECT_REQ: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_DETECT_REQ_SLOW.
52	RW	SLAVE_CAL_CKT_POWERDOWN: This bit controls the CAL_CIRCUIT_POWERDOWN input to the slave regulators. When 1, regulators are powered down. When 0, regulators are powered up.

Bits	SCOM	Field Mnemonic: Description
53:55	RO	Constant = 0b000
56	ROX	VREG_RXCAL_COMP_OUT_META: (Read only.) This bit indicates the result of the master VREG comparator, used during VREG calibration. 1 = VREG is less than the reference set by REF_SEL(0:2). 0 = VREG is greater than the reference set by REF_SEL(0:2).
57	ROX	RXCAL_DETECT_DONE_META: (Read only.) This bit is used during coarse and fine calibration. When 0, it means that the analog lead/lag comparator values are still being determined. When 1, it means that the analog lead/lag comparator values are valid and ready to read.
58	ROX	RXCAL_PD_CAL_LAG_META: (Read only.) This bit is used during coarse and fine calibration. 1 = The grid clock and 67.5 degree delay line output clock are in a lag relationship. 0 = Indeterminate. Either the calibration (CAL) filter/phase detector (PD) needs more time to evaluate, or clocks are in a lead relationship.
59	ROX	RXCAL_PD_MAIN_LEAD_META: (Read only.) This bit is used during coarse and fine calibration. 1 = The grid clock and 360 degree delay line output clock are in a lead relationship. 0 = Indeterminate. Either the main PD filter/phase detector needs more time to evaluate, or clocks are in a lag relationship.
60	ROX	RXCAL_PD_MAIN_LAG_META: (Read only.) This bit is used during coarse and fine calibration. 1 = The grid clock and 360 degree delay line output clock are in a lag relationship. 0 = Indeterminate. Either the main PD filter/phase detector needs more time to evaluate, or clocks are in a lead relationship.
61	ROX	VREG_SLAVE_COMP_OUT: (Read only.) This bit indicates the result of the slave VREG comparator. 1 = VREG is less than the reference set by REF_SEL(0:2). 0 = VREG is greater than the reference set by REF_SEL(0:2). It is safe to read after 256 grid clock cycles after REF_SEL is changed.
62:63	RO	Constant = 0b00

Register Name	DP16 DLL Software Control 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_SW_CONTROL0_P1_[n]
Address	800000A60701143F (SCOM), +0x0400_0000_0000
Description	This register exposes internal DLL signals to software to allow it to override the hardware DLL calibration algorithm. "META" indicates that the signals have safely crossed into the grid clock domain, so they should not exhibit metastability. Non-meta signals can be read after they stabilize.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	DLL_SW_OVERRIDE: When 0, the hardware DLL algorithm is used. When 1, this register takes control over the DLL analog inputs and outputs, allowing firmware to perform calibration.
49	RW	DLL_SW_CAL_PD_ENABLE: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_CAL_PD_ENABLE_SLOW.
50	RW	DLL_SW_MAIN_PD_ENABLE: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_MAIN_PD_ENABLE_SLOW.
51	RW	DLL_SW_DETECT_REQ: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_DETECT_REQ_SLOW.
52	RW	SLAVE_CAL_CKT_POWERDOWN: This bit controls the CAL_CIRCUIT_POWERDOWN input to the slave regulators. When 1, regulators are powered down. When 0, regulators are powered up.

Bits	SCOM	Field Mnemonic: Description
53:55	RO	Constant = 0b000
56	ROX	VREG_RXCAL_COMP_OUT_META: (Read only.) This bit indicates the result of the master VREG comparator, used during VREG calibration. 1 = VREG is less than the reference set by REF_SEL(0:2). 0 = VREG is greater than the reference set by REF_SEL(0:2).
57	ROX	RXCAL_DETECT_DONE_META: (Read only.) This bit is used during coarse and fine calibration. When 0, it means that the analog lead/lag comparator values are still being determined. When 1, it means that the analog lead/lag comparator values are valid and ready to read.
58	ROX	RXCAL_PD_CAL_LAG_META: (Read only.) This bit is used during coarse and fine calibration. 1 = The grid clock and 67.5 degree delay line output clock are in a lag relationship. 0 = Indeterminate. Either the calibration (CAL) filter/phase detector (PD) needs more time to evaluate, or clocks are in a lead relationship.
59	ROX	RXCAL_PD_MAIN_LEAD_META: (Read only.) This bit is used during coarse and fine calibration. 1 = The grid clock and 360 degree delay line output clock are in a lead relationship. 0 = Indeterminate. Either the main PD filter/phase detector needs more time to evaluate, or clocks are in a lag relationship.
60	ROX	RXCAL_PD_MAIN_LAG_META: (Read only.) This bit is used during coarse and fine calibration. 1 = The grid clock and 360 degree delay line output clock are in a lag relationship. 0 = Indeterminate. Either the main PD filter/phase detector needs more time to evaluate, or clocks are in a lead relationship.
61	ROX	VREG_SLAVE_COMP_OUT: (Read only.) This bit indicates the result of the slave VREG comparator. 1 = VREG is less than the reference set by REF_SEL(0:2). 0 = VREG is greater than the reference set by REF_SEL(0:2). It is safe to read after 256 grid clock cycles after REF_SEL is changed.
62:63	RO	Constant = 0b00

Register Name	**DP16 DLL Software Control 0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DLL_SW_CONTROL0_P2_[n]
Address	800000A60701183F (SCOM), +0x0400_0000_0000
Description	This register exposes internal DLL signals to software to allow it to override the hardware DLL calibration algorithm. "META" indicates that the signals have safely crossed into the grid clock domain, so they should not exhibit metastability. Non-meta signals can be read after they stabilize.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	DLL_SW_OVERRIDE: When 0, the hardware DLL algorithm is used. When 1, this register takes control over the DLL analog inputs and outputs, allowing firmware to perform calibration.
49	RW	DLL_SW_CAL_PD_ENABLE: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_CAL_PD_ENABLE_SLOW.
50	RW	DLL_SW_MAIN_PD_ENABLE: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_MAIN_PD_ENABLE_SLOW.
51	RW	DLL_SW_DETECT_REQ: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_DETECT_REQ_SLOW.
52	RW	SLAVE_CAL_CKT_POWERDOWN: This bit controls the CAL_CIRCUIT_POWERDOWN input to the slave regulators. When 1, regulators are powered down. When 0, regulators are powered up.

Bits	SCOM	Field Mnemonic: Description
53:55	RO	Constant = 0b000
56	ROX	VREG_RXCAL_COMP_OUT_META: (Read only.) This bit indicates the result of the master VREG comparator, used during VREG calibration. 1 = VREG is less than the reference set by REF_SEL(0:2). 0 = VREG is greater than the reference set by REF_SEL(0:2).
57	ROX	RXCAL_DETECT_DONE_META: (Read only.) This bit is used during coarse and fine calibration. When 0, it means that the analog lead/lag comparator values are still being determined. When 1, it means that the analog lead/lag comparator values are valid and ready to read.
58	ROX	RXCAL_PD_CAL_LAG_META: (Read only.) This bit is used during coarse and fine calibration. 1 = The grid clock and 67.5 degree delay line output clock are in a lag relationship. 0 = Indeterminate. Either the calibration (CAL) filter/phase detector (PD) needs more time to evaluate, or clocks are in a lead relationship.
59	ROX	RXCAL_PD_MAIN_LEAD_META: (Read only.) This bit is used during coarse and fine calibration. 1 = The grid clock and 360 degree delay line output clock are in a lead relationship. 0 = Indeterminate. Either the main PD filter/phase detector needs more time to evaluate, or clocks are in a lag relationship.
60	ROX	RXCAL_PD_MAIN_LAG_META: (Read only.) This bit is used during coarse and fine calibration. 1 = The grid clock and 360 degree delay line output clock are in a lag relationship. 0 = Indeterminate. Either the main PD filter/phase detector needs more time to evaluate, or clocks are in a lead relationship.
61	ROX	VREG_SLAVE_COMP_OUT: (Read only.) This bit indicates the result of the slave VREG comparator. 1 = VREG is less than the reference set by REF_SEL(0:2). 0 = VREG is greater than the reference set by REF_SEL(0:2). It is safe to read after 256 grid clock cycles after REF_SEL is changed.
62:63	RO	Constant = 0b00

Register Name	**DP16 DLL Software Control 0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DLL_SW_CONTROL0_P3_[n]
Address	800000A607011C3F (SCOM), +0x0400_0000_0000
Description	This register exposes internal DLL signals to software to allow it to override the hardware DLL calibration algorithm. "META" indicates that the signals have safely crossed into the grid clock domain, so they should not exhibit metastability. Non-meta signals can be read after they stabilize.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	DLL_SW_OVERRIDE: When 0, the hardware DLL algorithm is used. When 1, this register takes control over the DLL analog inputs and outputs, allowing firmware to perform calibration.
49	RW	DLL_SW_CAL_PD_ENABLE: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_CAL_PD_ENABLE_SLOW.
50	RW	DLL_SW_MAIN_PD_ENABLE: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_MAIN_PD_ENABLE_SLOW.
51	RW	DLL_SW_DETECT_REQ: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_DETECT_REQ_SLOW.
52	RW	SLAVE_CAL_CKT_POWERDOWN: This bit controls the CAL_CIRCUIT_POWERDOWN input to the slave regulators. When 1, regulators are powered down. When 0, regulators are powered up.

Bits	SCOM	Field Mnemonic: Description
53:55	RO	Constant = 0b000
56	ROX	VREG_RXCAL_COMP_OUT_META: (Read only.) This bit indicates the result of the master VREG comparator, used during VREG calibration. 1 = VREG is less than the reference set by REF_SEL(0:2). 0 = VREG is greater than the reference set by REF_SEL(0:2).
57	ROX	RXCAL_DETECT_DONE_META: (Read only.) This bit is used during coarse and fine calibration. When 0, it means that the analog lead/lag comparator values are still being determined. When 1, it means that the analog lead/lag comparator values are valid and ready to read.
58	ROX	RXCAL_PD_CAL_LAG_META: (Read only.) This bit is used during coarse and fine calibration. 1 = The grid clock and 67.5 degree delay line output clock are in a lag relationship. 0 = Indeterminate. Either the calibration (CAL) filter/phase detector (PD) needs more time to evaluate, or clocks are in a lead relationship.
59	ROX	RXCAL_PD_MAIN_LEAD_META: (Read only.) This bit is used during coarse and fine calibration. 1 = The grid clock and 360 degree delay line output clock are in a lead relationship. 0 = Indeterminate. Either the main PD filter/phase detector needs more time to evaluate, or clocks are in a lag relationship.
60	ROX	RXCAL_PD_MAIN_LAG_META: (Read only.) This bit is used during coarse and fine calibration. 1 = The grid clock and 360 degree delay line output clock are in a lag relationship. 0 = Indeterminate. Either the main PD filter/phase detector needs more time to evaluate, or clocks are in a lead relationship.
61	ROX	VREG_SLAVE_COMP_OUT: (Read only.) This bit indicates the result of the slave VREG comparator. 1 = VREG is less than the reference set by REF_SEL(0:2). 0 = VREG is greater than the reference set by REF_SEL(0:2). It is safe to read after 256 grid clock cycles after REF_SEL is changed.
62:63	RO	Constant = 0b00

Register Name	**DP16 DLL Software Control 1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DLL_SW_CONTROL1_P0_[n]
Address	800000A70701103F (SCOM), +0x0400_0000_0000
Description	This register exposes internal DLL signals to software to allow it to override the hardware DLL calibration algorithm. "META" indicates that the signals have safely crossed into the grid clock domain, so they should not exhibit metastability. Non-meta signals can be read after they stabilize.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	DLL_SW_OVERRIDE: When 0, the hardware DLL algorithm is used. When 1, this register takes control over the DLL analog inputs and outputs, allowing firmware to perform calibration.
49	RW	DLL_SW_CAL_PD_ENABLE: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_CAL_PD_ENABLE_SLOW.
50	RW	DLL_SW_MAIN_PD_ENABLE: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_MAIN_PD_ENABLE_SLOW.
51	RW	DLL_SW_DETECT_REQ: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_DETECT_REQ_SLOW.
52	RW	SLAVE_CAL_CKT_POWERDOWN: This bit controls the CAL_CIRCUIT_POWERDOWN input to the slave regulators. When 1, regulators are powered down. When 0, regulators are powered up.

Bits	SCOM	Field Mnemonic: Description
53:55	RO	Constant = 0b000
56	ROX	VREG_RXCAL_COMP_OUT_META: (Read only.) This bit indicates the result of the master VREG comparator, used during VREG calibration. 1 = VREG is less than the reference set by REF_SEL(0:2). 0 = VREG is greater than the reference set by REF_SEL(0:2).
57	ROX	RXCAL_DETECT_DONE_META: (Read only.) This bit is used during coarse and fine calibration. When 0, it means that the analog lead/lag comparator values are still being determined. When 1, it means that the analog lead/lag comparator values are valid and ready to read.
58	ROX	RXCAL_PD_CAL_LAG_META: (Read only.) This bit is used during coarse and fine calibration. 1 = The grid clock and 67.5 degree delay line output clock are in a lag relationship. 0 = Indeterminate. Either the calibration (CAL) filter/phase detector (PD) needs more time to evaluate, or clocks are in a lead relationship.
59	ROX	RXCAL_PD_MAIN_LEAD_META: (Read only.) This bit is used during coarse and fine calibration. 1 = The grid clock and 360 degree delay line output clock are in a lead relationship. 0 = Indeterminate. Either the main PD filter/phase detector needs more time to evaluate, or clocks are in a lag relationship.
60	ROX	RXCAL_PD_MAIN_LAG_META: (Read only.) This bit is used during coarse and fine calibration. 1 = The grid clock and 360 degree delay line output clock are in a lag relationship. 0 = Indeterminate. Either the main PD filter/phase detector needs more time to evaluate, or clocks are in a lead relationship.
61	ROX	VREG_SLAVE_COMP_OUT: (Read only.) This bit indicates the result of the slave VREG comparator. 1 = VREG is less than the reference set by REF_SEL(0:2). 0 = VREG is greater than the reference set by REF_SEL(0:2). It is safe to read after 256 grid clock cycles after REF_SEL is changed.
62:63	RO	Constant = 0b00

Register Name	**DP16 DLL Software Control 1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DLL_SW_CONTROL1_P1_[n]
Address	800000A70701143F (SCOM), +0x0400_0000_0000
Description	This register exposes internal DLL signals to software to allow it to override the hardware DLL calibration algorithm. "META" indicates that the signals have safely crossed into the grid clock domain, so they should not exhibit metastability. Non-meta signals can be read after they stabilize.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	DLL_SW_OVERRIDE: When 0, the hardware DLL algorithm is used. When 1, this register takes control over the DLL analog inputs and outputs, allowing firmware to perform calibration.
49	RW	DLL_SW_CAL_PD_ENABLE: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_CAL_PD_ENABLE_SLOW.
50	RW	DLL_SW_MAIN_PD_ENABLE: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_MAIN_PD_ENABLE_SLOW.
51	RW	DLL_SW_DETECT_REQ: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_DETECT_REQ_SLOW.
52	RW	SLAVE_CAL_CKT_POWERDOWN: This bit controls the CAL_CIRCUIT_POWERDOWN input to the slave regulators. When 1, regulators are powered down. When 0, regulators are powered up.

Bits	SCOM	Field Mnemonic: Description
53:55	RO	Constant = 0b000
56	ROX	VREG_RXCAL_COMP_OUT_META: (Read only.) This bit indicates the result of the master VREG comparator, used during VREG calibration. 1 = VREG is less than the reference set by REF_SEL(0:2). 0 = VREG is greater than the reference set by REF_SEL(0:2).
57	ROX	RXCAL_DETECT_DONE_META: (Read only.) This bit is used during coarse and fine calibration. When 0, it means that the analog lead/lag comparator values are still being determined. When 1, it means that the analog lead/lag comparator values are valid and ready to read.
58	ROX	RXCAL_PD_CAL_LAG_META: (Read only.) This bit is used during coarse and fine calibration. 1 = The grid clock and 67.5 degree delay line output clock are in a lag relationship. 0 = Indeterminate. Either the calibration (CAL) filter/phase detector (PD) needs more time to evaluate, or clocks are in a lead relationship.
59	ROX	RXCAL_PD_MAIN_LEAD_META: (Read only.) This bit is used during coarse and fine calibration. 1 = The grid clock and 360 degree delay line output clock are in a lead relationship. 0 = Indeterminate. Either the main PD filter/phase detector needs more time to evaluate, or clocks are in a lag relationship.
60	ROX	RXCAL_PD_MAIN_LAG_META: (Read only.) This bit is used during coarse and fine calibration. 1 = The grid clock and 360 degree delay line output clock are in a lag relationship. 0 = Indeterminate. Either the main PD filter/phase detector needs more time to evaluate, or clocks are in a lead relationship.
61	ROX	VREG_SLAVE_COMP_OUT: (Read only.) This bit indicates the result of the slave VREG comparator. 1 = VREG is less than the reference set by REF_SEL(0:2). 0 = VREG is greater than the reference set by REF_SEL(0:2). It is safe to read after 256 grid clock cycles after REF_SEL is changed.
62:63	RO	Constant = 0b00

Register Name	**DP16 DLL Software Control 1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DLL_SW_CONTROL1_P2_[n]
Address	800000A70701183F (SCOM), +0x0400_0000_0000
Description	This register exposes internal DLL signals to software to allow it to override the hardware DLL calibration algorithm. "META" indicates that the signals have safely crossed into the grid clock domain, so they should not exhibit metastability. Non-meta signals can be read after they stabilize.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	DLL_SW_OVERRIDE: When 0, the hardware DLL algorithm is used. When 1, this register takes control over the DLL analog inputs and outputs, allowing firmware to perform calibration.
49	RW	DLL_SW_CAL_PD_ENABLE: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_CAL_PD_ENABLE_SLOW.
50	RW	DLL_SW_MAIN_PD_ENABLE: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_MAIN_PD_ENABLE_SLOW.
51	RW	DLL_SW_DETECT_REQ: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_DETECT_REQ_SLOW.
52	RW	SLAVE_CAL_CKT_POWERDOWN: This bit controls the CAL_CIRCUIT_POWERDOWN input to the slave regulators. When 1, regulators are powered down. When 0, regulators are powered up.

Bits	SCOM	Field Mnemonic: Description
53:55	RO	Constant = 0b000
56	ROX	VREG_RXCAL_COMP_OUT_META: (Read only.) This bit indicates the result of the master VREG comparator, used during VREG calibration. 1 = VREG is less than the reference set by REF_SEL(0:2). 0 = VREG is greater than the reference set by REF_SEL(0:2).
57	ROX	RXCAL_DETECT_DONE_META: (Read only.) This bit is used during coarse and fine calibration. When 0, it means that the analog lead/lag comparator values are still being determined. When 1, it means that the analog lead/lag comparator values are valid and ready to read.
58	ROX	RXCAL_PD_CAL_LAG_META: (Read only.) This bit is used during coarse and fine calibration. 1 = The grid clock and 67.5 degree delay line output clock are in a lag relationship. 0 = Indeterminate. Either the calibration (CAL) filter/phase detector (PD) needs more time to evaluate, or clocks are in a lead relationship.
59	ROX	RXCAL_PD_MAIN_LEAD_META: (Read only.) This bit is used during coarse and fine calibration. 1 = The grid clock and 360 degree delay line output clock are in a lead relationship. 0 = Indeterminate. Either the main PD filter/phase detector needs more time to evaluate, or clocks are in a lag relationship.
60	ROX	RXCAL_PD_MAIN_LAG_META: (Read only.) This bit is used during coarse and fine calibration. 1 = The grid clock and 360 degree delay line output clock are in a lag relationship. 0 = Indeterminate. Either the main PD filter/phase detector needs more time to evaluate, or clocks are in a lead relationship.
61	ROX	VREG_SLAVE_COMP_OUT: (Read only.) This bit indicates the result of the slave VREG comparator. 1 = VREG is less than the reference set by REF_SEL(0:2). 0 = VREG is greater than the reference set by REF_SEL(0:2). It is safe to read after 256 grid clock cycles after REF_SEL is changed.
62:63	RO	Constant = 0b00

Register Name	**DP16 DLL Software Control 1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DLL_SW_CONTROL1_P3_[n]
Address	800000A707011C3F (SCOM), +0x0400_0000_0000
Description	This register exposes internal DLL signals to software to allow it to override the hardware DLL calibration algorithm. "META" indicates that the signals have safely crossed into the grid clock domain, so they should not exhibit metastability. Non-meta signals can be read after they stabilize.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	DLL_SW_OVERRIDE: When 0, the hardware DLL algorithm is used. When 1, this register takes control over the DLL analog inputs and outputs, allowing firmware to perform calibration.
49	RW	DLL_SW_CAL_PD_ENABLE: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_CAL_PD_ENABLE_SLOW.
50	RW	DLL_SW_MAIN_PD_ENABLE: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_MAIN_PD_ENABLE_SLOW.
51	RW	DLL_SW_DETECT_REQ: When DLL_SW_OVERRIDE = 1, this value is sent to the analog DLL as RXCAL_DLL_DETECT_REQ_SLOW.
52	RW	SLAVE_CAL_CKT_POWERDOWN: This bit controls the CAL_CIRCUIT_POWERDOWN input to the slave regulators. When 1, regulators are powered down. When 0, regulators are powered up.

Bits	SCOM	Field Mnemonic: Description
53:55	RO	Constant = 0b000
56	ROX	VREG_RXCAL_COMP_OUT_META: (Read only.) This bit indicates the result of the master VREG comparator, used during VREG calibration. 1 = VREG is less than the reference set by REF_SEL(0:2). 0 = VREG is greater than the reference set by REF_SEL(0:2).
57	ROX	RXCAL_DETECT_DONE_META: (Read only.) This bit is used during coarse and fine calibration. When 0, it means that the analog lead/lag comparator values are still being determined. When 1, it means that the analog lead/lag comparator values are valid and ready to read.
58	ROX	RXCAL_PD_CAL_LAG_META: (Read only.) This bit is used during coarse and fine calibration. 1 = The grid clock and 67.5 degree delay line output clock are in a lag relationship. 0 = Indeterminate. Either the calibration (CAL) filter/phase detector (PD) needs more time to evaluate, or clocks are in a lead relationship.
59	ROX	RXCAL_PD_MAIN_LEAD_META: (Read only.) This bit is used during coarse and fine calibration. 1 = The grid clock and 360 degree delay line output clock are in a lead relationship. 0 = Indeterminate. Either the main PD filter/phase detector needs more time to evaluate, or clocks are in a lag relationship.
60	ROX	RXCAL_PD_MAIN_LAG_META: (Read only.) This bit is used during coarse and fine calibration. 1 = The grid clock and 360 degree delay line output clock are in a lag relationship. 0 = Indeterminate. Either the main PD filter/phase detector needs more time to evaluate, or clocks are in a lead relationship.
61	ROX	VREG_SLAVE_COMP_OUT: (Read only.) This bit indicates the result of the slave VREG comparator. 1 = VREG is less than the reference set by REF_SEL(0:2). 0 = VREG is greater than the reference set by REF_SEL(0:2). It is safe to read after 256 grid clock cycles after REF_SEL is changed.
62:63	RO	Constant = 0b00

Register Name	DP16 DLL Slave VREG Lower 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_SLAVE_VREG_LOWER0_P0_[n]
Address	800000A80701103F (SCOM), +0x0400_0000_0000
Description	This register holds the "lower" control for the slave voltage regulators.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:62	RW	SLAVE_VREG_LOWER: This field controls the value of the VREG of the slave regulators. Bits set to 1 are independent of each other. It is the total number of them that matter. For example, these settings have the same effect: b100...00, b001...00, b000...10. Adding more 1s increases the VREG. Recommendation: Change bits in thermometer code fashion.
63	RO	Constant = 0b0

Register Name	DP16 DLL Slave VREG Lower 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_SLAVE_VREG_LOWER0_P1_[n]
Address	800000A80701143F (SCOM), +0x0400_0000_0000
Description	This register holds the "lower" control for the slave voltage regulators.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:62	RW	SLAVE_VREG_LOWER: This field controls the value of the VREG of the slave regulators. Bits set to 1 are independent of each other. It is the total number of them that matter. For example, these settings have the same effect: b100...00, b001...00, b000...10. Adding more 1s increases the VREG. Recommendation: Change bits in thermometer code fashion.
63	RO	Constant = 0b0

Register Name	DP16 DLL Slave VREG Lower 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_SLAVE_VREG_LOWER0_P2_[n]
Address	800000A80701183F (SCOM), +0x0400_0000_0000
Description	This register holds the "lower" control for the slave voltage regulators.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:62	RW	SLAVE_VREG_LOWER: This field controls the value of the VREG of the slave regulators. Bits set to 1 are independent of each other. It is the total number of them that matter. For example, these settings have the same effect: b100...00, b001...00, b000...10. Adding more 1s increases the VREG. Recommendation: Change bits in thermometer code fashion.
63	RO	Constant = 0b0

Register Name	DP16 DLL Slave VREG Lower 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_SLAVE_VREG_LOWER0_P3_[n]
Address	800000A807011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the "lower" control for the slave voltage regulators.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:62	RW	SLAVE_VREG_LOWER: This field controls the value of the VREG of the slave regulators. Bits set to 1 are independent of each other. It is the total number of them that matter. For example, these settings have the same effect: b100...00, b001...00, b000...10. Adding more 1s increases the VREG. Recommendation: Change bits in thermometer code fashion.
63	RO	Constant = 0b0

Register Name	DP16 DLL Slave VREG Lower 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_SLAVE_VREG_LOWER1_P0_[n]
Address	800000A90701103F (SCOM), +0x0400_0000_0000
Description	This register holds the "lower" control for the slave voltage regulators.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:62	RW	SLAVE_VREG_LOWER: This field controls the value of the VREG of the slave regulators. Bits set to 1 are independent of each other. It is the total number of them that matter. For example, these settings have the same effect: b100...00, b001...00, b000...10. Adding more 1s increases the VREG. Recommendation: Change bits in thermometer code fashion.

Bits	SCOM	Field Mnemonic: Description
63	RO	Constant = 0b0

Register Name	DP16 DLL Slave VREG Lower 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_SLAVE_VREG_LOWER1_P1_[n]
Address	800000A90701143F (SCOM), +0x0400_0000_0000
Description	This register holds the "lower" control for the slave voltage regulators.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:62	RW	SLAVE_VREG_LOWER: This field controls the value of the VREG of the slave regulators. Bits set to 1 are independent of each other. It is the total number of them that matter. For example, these settings have the same effect: b100...00, b001...00, b000...10. Adding more 1s increases the VREG. Recommendation: Change bits in thermometer code fashion.
63	RO	Constant = 0b0

Register Name	DP16 DLL Slave VREG Lower 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_SLAVE_VREG_LOWER1_P2_[n]
Address	800000A90701183F (SCOM), +0x0400_0000_0000
Description	This register holds the "lower" control for the slave voltage regulators.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:62	RW	SLAVE_VREG_LOWER: This field controls the value of the VREG of the slave regulators. Bits set to 1 are independent of each other. It is the total number of them that matter. For example, these settings have the same effect: b100...00, b001...00, b000...10. Adding more 1s increases the VREG. Recommendation: Change bits in thermometer code fashion.
63	RO	Constant = 0b0

Register Name	DP16 DLL Slave VREG Lower 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_SLAVE_VREG_LOWER1_P3_[n]
Address	800000A907011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the "lower" control for the slave voltage regulators.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:62	RW	SLAVE_VREG_LOWER: This field controls the value of the VREG of the slave regulators. Bits set to 1 are independent of each other. It is the total number of them that matter. For example, these settings have the same effect: b100...00, b001...00, b000...10. Adding more 1s increases the VREG. Recommendation: Change bits in thermometer code fashion.
63	RO	Constant = 0b0

Register Name	DP16 DLL Slave VREG Upper 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_SLAVE_VREG_UPPER0_P0_[n]
Address	800000AA0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the "upper" control for the slave voltage regulators.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:62	RW	SLAVE_VREG_UPPER: This field behaves the same as SLAVE_VREG_LOWER, except the effect on VREG is 16 times larger for each bit.
63	RO	Constant = 0b0

Register Name	DP16 DLL Slave VREG Upper 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_SLAVE_VREG_UPPER0_P1_[n]
Address	800000AA0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the "upper" control for the slave voltage regulators.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:62	RW	SLAVE_VREG_UPPER: This field behaves the same as SLAVE_VREG_LOWER, except the effect on VREG is 16 times larger for each bit.
63	RO	Constant = 0b0

Register Name	DP16 DLL Slave VREG Upper 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_SLAVE_VREG_UPPER0_P2_[n]
Address	800000AA0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the "upper" control for the slave voltage regulators.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:62	RW	SLAVE_VREG_UPPER: This field behaves the same as SLAVE_VREG_LOWER, except the effect on VREG is 16 times larger for each bit.
63	RO	Constant = 0b0

Register Name	DP16 DLL Slave VREG Upper 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_SLAVE_VREG_UPPER0_P3_[n]
Address	800000AA07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the "upper" control for the slave voltage regulators.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:62	RW	SLAVE_VREG_UPPER: This field behaves the same as SLAVE_VREG_LOWER, except the effect on VREG is 16 times larger for each bit.
63	RO	Constant = 0b0

Register Name	DP16 DLL Slave VREG Upper 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_SLAVE_VREG_UPPER1_P0_[n]
Address	800000AB0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the "upper" control for the slave voltage regulators.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:62	RW	SLAVE_VREG_UPPER: This field behaves the same as SLAVE_VREG_LOWER, except the effect on VREG is 16 times larger for each bit.
63	RO	Constant = 0b0

Register Name	DP16 DLL Slave VREG Upper 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_SLAVE_VREG_UPPER1_P1_[n]
Address	800000AB0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the "upper" control for the slave voltage regulators.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:62	RW	SLAVE_VREG_UPPER: This field behaves the same as SLAVE_VREG_LOWER, except the effect on VREG is 16 times larger for each bit.
63	RO	Constant = 0b0

Register Name	DP16 DLL Slave VREG Upper 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_SLAVE_VREG_UPPER1_P2_[n]
Address	800000AB0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the "upper" control for the slave voltage regulators.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:62	RW	SLAVE_VREG_UPPER: This field behaves the same as SLAVE_VREG_LOWER, except the effect on VREG is 16 times larger for each bit.
63	RO	Constant = 0b0

Register Name	DP16 DLL Slave VREG Upper 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_SLAVE_VREG_UPPER1_P3_[n]
Address	800000AB07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the "upper" control for the slave voltage regulators.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:62	RW	SLAVE_VREG_UPPER: This field behaves the same as SLAVE_VREG_LOWER, except the effect on VREG is 16 times larger for each bit.
63	RO	Constant = 0b0

Register Name	DP16 DLL Extra 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_EXTRA0_P0_[n]
Address	800000AC0701103F (SCOM), +0x0400_0000_0000
Description	Originally this register was for the extra fields needed after scan net optimization enhancement (SNOE) is fed back. For DD1, parts of it were re-tasked to allow software to take control of the slave regulators' VREG controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	SLAVE_VREG_OVERRIDE: When 0, the master regulator controls for REF_SEL and NVT/PVT (derived from VREG_DAC_COARSE) are sent to the slave regulators. This allows the slave to track the master's settings during VREG calibration. When 1, this register takes control over the slave regulator REF_SEL and NVT/PVT (via VREG_DAC_COARSE) inputs. This allows software to manage the master and slave regulators completely independently.
49:51	RW	SLAVE_VREG_REF_SEL_DC: When SLAVE_VREG_OVERRIDE = 0, this field is not used. The master and slave share the master's VREG_REF_SEL_DC(0:2) setting. When SLAVE_VREG_OVERRIDE = 1, this field is sent to the slave regulators as VREG_REF_SEL_DC(0:2).
52:58	RW	SLAVE_VREG_DAC_COARSE: When SLAVE_VREG_OVERRIDE = 0, this field is not used. The master and slave share the master's VREG_DAC_COARSE(0:6) setting. When SLAVE_VREG_OVERRIDE = 1, this field is sent to the slave regulators as VREG_DAC_COARSE(0:6), which is converted to NVT(0:3) and PVT(0:3) by the DLL logic.
59:63	RO	Constant = 0b00000

Register Name	DP16 DLL Extra 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_EXTRA0_P1_[n]
Address	800000AC0701143F (SCOM), +0x0400_0000_0000
Description	Originally this register was for the extra fields needed after SNOE is fed back. For DD1, parts of it were re-tasked to allow software to take control of the slave regulators' VREG controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RW	SLAVE_VREG_OVERRIDE: When 0, the master regulator controls for REF_SEL and NVT/PVT (derived from VREG_DAC_COARSE) are sent to the slave regulators. This allows the slave to track the master's settings during VREG calibration. When 1, this register takes control over the slave regulator REF_SEL and NVT/PVT (via VREG_DAC_COARSE) inputs. This allows software to manage the master and slave regulators completely independently.
49:51	RW	SLAVE_VREG_REF_SEL_DC: When SLAVE_VREG_OVERRIDE = 0, this field is not used. The master and slave share the master's VREG_REF_SEL_DC(0:2) setting. When SLAVE_VREG_OVERRIDE = 1, this field is sent to the slave regulators as VREG_REF_SEL_DC(0:2).
52:58	RW	SLAVE_VREG_DAC_COARSE: When SLAVE_VREG_OVERRIDE = 0, this field is not used. The master and slave share the master's VREG_DAC_COARSE(0:6) setting. When SLAVE_VREG_OVERRIDE = 1, this field is sent to the slave regulators as VREG_DAC_COARSE(0:6), which is converted to NVT(0:3) and PVT(0:3) by the DLL logic.
59:63	RO	Constant = 0b00000

Register Name	DP16 DLL Extra 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_EXTRA0_P2_[n]
Address	800000AC0701183F (SCOM), +0x0400_0000_0000
Description	Originally this register was for the extra fields needed after SNOE is fed back. For DD1, parts of it were re-tasked to allow software to take control of the slave regulators' VREG controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	SLAVE_VREG_OVERRIDE: When 0, the master regulator controls for REF_SEL and NVT/PVT (derived from VREG_DAC_COARSE) are sent to the slave regulators. This allows the slave to track the master's settings during VREG calibration. When 1, this register takes control over the slave regulator REF_SEL and NVT/PVT (via VREG_DAC_COARSE) inputs. This allows software to manage the master and slave regulators completely independently.
49:51	RW	SLAVE_VREG_REF_SEL_DC: When SLAVE_VREG_OVERRIDE = 0, this field is not used. The master and slave share the master's VREG_REF_SEL_DC(0:2) setting. When SLAVE_VREG_OVERRIDE = 1, this field is sent to the slave regulators as VREG_REF_SEL_DC(0:2).
52:58	RW	SLAVE_VREG_DAC_COARSE: When SLAVE_VREG_OVERRIDE = 0, this field is not used. The master and slave share the master's VREG_DAC_COARSE(0:6) setting. When SLAVE_VREG_OVERRIDE = 1, this field is sent to the slave regulators as VREG_DAC_COARSE(0:6), which is converted to NVT(0:3) and PVT(0:3) by the DLL logic.
59:63	RO	Constant = 0b00000

Register Name	DP16 DLL Extra 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_EXTRA0_P3_[n]
Address	800000AC07011C3F (SCOM), +0x0400_0000_0000
Description	Originally this register was for the extra fields needed after SNOE is fed back. For DD1, parts of it were re-tasked to allow software to take control of the slave regulators' VREG controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RW	SLAVE_VREG_OVERRIDE: When 0, the master regulator controls for REF_SEL and NVT/PVT (derived from VREG_DAC_COARSE) are sent to the slave regulators. This allows the slave to track the master's settings during VREG calibration. When 1, this register takes control over the slave regulator REF_SEL and NVT/PVT (via VREG_DAC_COARSE) inputs. This allows software to manage the master and slave regulators completely independently.
49:51	RW	SLAVE_VREG_REF_SEL_DC: When SLAVE_VREG_OVERRIDE = 0, this field is not used. The master and slave share the master's VREG_REF_SEL_DC(0:2) setting. When SLAVE_VREG_OVERRIDE = 1, this field is sent to the slave regulators as VREG_REF_SEL_DC(0:2).
52:58	RW	SLAVE_VREG_DAC_COARSE: When SLAVE_VREG_OVERRIDE = 0, this field is not used. The master and slave share the master's VREG_DAC_COARSE(0:6) setting. When SLAVE_VREG_OVERRIDE = 1, this field is sent to the slave regulators as VREG_DAC_COARSE(0:6), which is converted to NVT(0:3) and PVT(0:3) by the DLL logic.
59:63	RO	Constant = 0b00000

Register Name	DP16 DLL Extra 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_EXTRA1_P0_[n]
Address	800000AD0701103F (SCOM), +0x0400_0000_0000
Description	Originally this register was for the extra fields needed after SNOE is fed back. For DD1, parts of it were re-tasked to allow software to take control of the slave regulators' VREG controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	SLAVE_VREG_OVERRIDE: When 0, the master regulator controls for REF_SEL and NVT/PVT (derived from VREG_DAC_COARSE) are sent to the slave regulators. This allows the slave to track the master's settings during VREG calibration. When 1, this register takes control over the slave regulator REF_SEL and NVT/PVT (via VREG_DAC_COARSE) inputs. This allows software to manage the master and slave regulators completely independently.
49:51	RW	SLAVE_VREG_REF_SEL_DC: When SLAVE_VREG_OVERRIDE = 0, this field is not used. The master and slave share the master's VREG_REF_SEL_DC(0:2) setting. When SLAVE_VREG_OVERRIDE = 1, this field is sent to the slave regulators as VREG_REF_SEL_DC(0:2).
52:58	RW	SLAVE_VREG_DAC_COARSE: When SLAVE_VREG_OVERRIDE = 0, this field is not used. The master and slave share the master's VREG_DAC_COARSE(0:6) setting. When SLAVE_VREG_OVERRIDE = 1, this field is sent to the slave regulators as VREG_DAC_COARSE(0:6), which is converted to NVT(0:3) and PVT(0:3) by the DLL logic.
59:63	RO	Constant = 0b00000

Register Name	DP16 DLL Extra 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_EXTRA1_P1_[n]
Address	800000AD0701143F (SCOM), +0x0400_0000_0000
Description	Originally this register was for the extra fields needed after SNOE is fed back. For DD1, parts of it were re-tasked to allow software to take control of the slave regulators' VREG controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RW	SLAVE_VREG_OVERRIDE: When 0, the master regulator controls for REF_SEL and NVT/PVT (derived from VREG_DAC_COARSE) are sent to the slave regulators. This allows the slave to track the master's settings during VREG calibration. When 1, this register takes control over the slave regulator REF_SEL and NVT/PVT (via VREG_DAC_COARSE) inputs. This allows software to manage the master and slave regulators completely independently.
49:51	RW	SLAVE_VREG_REF_SEL_DC: When SLAVE_VREG_OVERRIDE = 0, this field is not used. The master and slave share the master's VREG_REF_SEL_DC(0:2) setting. When SLAVE_VREG_OVERRIDE = 1, this field is sent to the slave regulators as VREG_REF_SEL_DC(0:2).
52:58	RW	SLAVE_VREG_DAC_COARSE: When SLAVE_VREG_OVERRIDE = 0, this field is not used. The master and slave share the master's VREG_DAC_COARSE(0:6) setting. When SLAVE_VREG_OVERRIDE = 1, this field is sent to the slave regulators as VREG_DAC_COARSE(0:6), which is converted to NVT(0:3) and PVT(0:3) by the DLL logic.
59:63	RO	Constant = 0b00000

Register Name	DP16 DLL Extra 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_EXTRA1_P2_[n]
Address	800000AD0701183F (SCOM), +0x0400_0000_0000
Description	Originally this register was for the extra fields needed after SNOE is fed back. For DD1, parts of it were re-tasked to allow software to take control of the slave regulators' VREG controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	SLAVE_VREG_OVERRIDE: When 0, the master regulator controls for REF_SEL and NVT/PVT (derived from VREG_DAC_COARSE) are sent to the slave regulators. This allows the slave to track the master's settings during VREG calibration. When 1, this register takes control over the slave regulator REF_SEL and NVT/PVT (via VREG_DAC_COARSE) inputs. This allows software to manage the master and slave regulators completely independently.
49:51	RW	SLAVE_VREG_REF_SEL_DC: When SLAVE_VREG_OVERRIDE = 0, this field is not used. The master and slave share the master's VREG_REF_SEL_DC(0:2) setting. When SLAVE_VREG_OVERRIDE = 1, this field is sent to the slave regulators as VREG_REF_SEL_DC(0:2).
52:58	RW	SLAVE_VREG_DAC_COARSE: When SLAVE_VREG_OVERRIDE = 0, this field is not used. The master and slave share the master's VREG_DAC_COARSE(0:6) setting. When SLAVE_VREG_OVERRIDE = 1, this field is sent to the slave regulators as VREG_DAC_COARSE(0:6), which is converted to NVT(0:3) and PVT(0:3) by the DLL logic.
59:63	RO	Constant = 0b00000

Register Name	DP16 DLL Extra 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DLL_EXTRA1_P3_[n]
Address	800000AD07011C3F (SCOM), +0x0400_0000_0000
Description	Originally this register was for the extra fields needed after SNOE is fed back. For DD1, parts of it were re-tasked to allow software to take control of the slave regulators' VREG controls.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RW	SLAVE_VREG_OVERRIDE: When 0, the master regulator controls for REF_SEL and NVT/PVT (derived from VREG_DAC_COARSE) are sent to the slave regulators. This allows the slave to track the master's settings during VREG calibration. When 1, this register takes control over the slave regulator REF_SEL and NVT/PVT (via VREG_DAC_COARSE) inputs. This allows software to manage the master and slave regulators completely independently.
49:51	RW	SLAVE_VREG_REF_SEL_DC: When SLAVE_VREG_OVERRIDE = 0, this field is not used. The master and slave share the master's VREG_REF_SEL_DC(0:2) setting. When SLAVE_VREG_OVERRIDE = 1, this field is sent to the slave regulators as VREG_REF_SEL_DC(0:2).
52:58	RW	SLAVE_VREG_DAC_COARSE: When SLAVE_VREG_OVERRIDE = 0, this field is not used. The master and slave share the master's VREG_DAC_COARSE(0:6) setting. When SLAVE_VREG_OVERRIDE = 1, this field is sent to the slave regulators as VREG_DAC_COARSE(0:6), which is converted to NVT(0:3) and PVT(0:3) by the DLL logic.
59:63	RO	Constant = 0b00000

Register Name	DP16 Write VREF Error 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_ERROR0_P0_[n]
Address	800000AE0701103F (SCOM), +0x0400_0000_0000
Description	This register provides error information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	RWX	WR_VREF_MAX_RANGE_ERR0: DRAM 0. 0 = No error. 1 = The current VREF goes outside of the maximum range.
49	RWX	WR_VREF_MIN_RANGE_ERR0: DRAM 0. 0 = No error. 1 = The current VREF is 0, the minimum VREF.
50	RWX	WR_VREF_TWO_RANGE_BEST_CASE_ERR0: DRAM 0. 0 = No error. 1 = There are maximums found above and below the nominal VREF.
51	RWX	WR_VREF_BIT_STEP_DELTA_ERR0: DRAM 0. 0 = No error. 1 = The maximum and minimum VREF values are at least one big step apart.
52	RWX	WR_VREF_STEP_RANGE_EDGE_ERR0: DRAM 0. 0 = No error. 1 = Small stepping is on the edge of, or outside of, previously tested ranges.
53	RWX	WR_VREF_NO_INCREASE_ERR0: DRAM 0. 0 = No error. 1 = No increase was found.
54	RWX	WR_VREF_1D_EYE_NOISE_ERR0: DRAM 0. 0 = No error. 1 = A current-to-previous delta greater than a coarse_step was found.
55	RWX	WR_VREF_BAD_BIT_ERR0: DRAM 0. 0 = No error. 1 = A bad bit is found, but not during the first or last VREF.
56	RWX	WR_VREF_MAX_RANGE_ERR1: DRAM 1. 0 = No error. 1 = The current VREF goes outside of the maximum range.

Bits	SCOM	Field Mnemonic: Description
57	RWX	WR_VREF_MIN_RANGE_ERR1: DRAM 1. 0 = No error. 1 = The current VREF is 0, the minimum VREF.
58	RWX	WR_VREF_TWO_RANGE_BEST_CASE_ERR1: DRAM 1. 0 = No error. 1 = There are maximums found above and below the nominal VREF.
59	RWX	WR_VREF_BIT_STEP_DELTA_ERR1: DRAM 1. 0 = No error. 1 = The maximum and minimum VREF values are at least one big step apart.
60	RWX	WR_VREF_STEP_RANGE_EDGE_ERR1: DRAM 1. 0 = No error. 1 = Small stepping is on the edge of, or outside of, previously tested ranges.
61	RWX	WR_VREF_NO_INCREASE_ERR1: DRAM 1. 0 = No error. 1 = No increase was found.
62	RWX	WR_VREF_1D_EYE_NOISE_ERR1: DRAM 1. 0 = No error. 1 = A current-to-previous delta greater than a coarse_step was found.
63	RWX	WR_VREF_BAD_BIT_ERR1: DRAM 1. 0 = No error. 1 = A bad bit is found, but not during the first or last VREF.

Register Name	DP16 Write VREF Error 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_ERROR0_P1_[n]
Address	800000AE0701143F (SCOM), +0x0400_0000_0000
Description	This register provides error information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RWX	WR_VREF_MAX_RANGE_ERR0: DRAM 0. 0 = No error. 1 = The current VREF goes outside of the maximum range.
49	RWX	WR_VREF_MIN_RANGE_ERR0: DRAM 0. 0 = No error. 1 = The current VREF is 0, the minimum VREF.
50	RWX	WR_VREF_TWO_RANGE_BEST_CASE_ERR0: DRAM 0. 0 = No error. 1 = There are maximums found above and below the nominal VREF.
51	RWX	WR_VREF_BIT_STEP_DELTA_ERR0: DRAM 0. 0 = No error. 1 = The maximum and minimum VREF values are at least one big step apart.
52	RWX	WR_VREF_STEP_RANGE_EDGE_ERR0: DRAM 0. 0 = No error. 1 = Small stepping is on the edge of, or outside of, previously tested ranges.
53	RWX	WR_VREF_NO_INCREASE_ERR0: DRAM 0. 0 = No error. 1 = No increase was found.

Bits	SCOM	Field Mnemonic: Description
54	RWX	WR_VREF_1D_EYE_NOISE_ERR0: DRAM 0. 0 = No error. 1 = A current-to-previous delta greater than a coarse_step was found.
55	RWX	WR_VREF_BAD_BIT_ERR0: DRAM 0. 0 = No error. 1 = A bad bit is found, but not during the first or last VREF.
56	RWX	WR_VREF_MAX_RANGE_ERR1: DRAM 1. 0 = No error. 1 = The current VREF goes outside of the maximum range.
57	RWX	WR_VREF_MIN_RANGE_ERR1: DRAM 1. 0 = No error. 1 = The current VREF is 0, the minimum VREF.
58	RWX	WR_VREF_TWO_RANGE_BEST_CASE_ERR1: DRAM 1. 0 = No error. 1 = There are maximums found above and below the nominal VREF.
59	RWX	WR_VREF_BIT_STEP_DELTA_ERR1: DRAM 1. 0 = No error. 1 = The maximum and minimum VREF values are at least one big step apart.
60	RWX	WR_VREF_STEP_RANGE_EDGE_ERR1: DRAM 1. 0 = No error. 1 = Small stepping is on the edge of, or outside of, previously tested ranges.
61	RWX	WR_VREF_NO_INCREASE_ERR1: DRAM 1. 0 = No error. 1 = No increase was found.
62	RWX	WR_VREF_1D_EYE_NOISE_ERR1: DRAM 1. 0 = No error. 1 = A current-to-previous delta greater than a coarse_step was found.
63	RWX	WR_VREF_BAD_BIT_ERR1: DRAM 1. 0 = No error. 1 = A bad bit is found, but not during the first or last VREF.

Register Name	**DP16 Write VREF Error 0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_ERROR0_P2_[n]
Address	800000AE0701183F (SCOM), +0x0400_0000_0000
Description	This register provides error information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RWX	WR_VREF_MAX_RANGE_ERR0: DRAM 0. 0 = No error. 1 = The current VREF goes outside of the maximum range.
49	RWX	WR_VREF_MIN_RANGE_ERR0: DRAM 0. 0 = No error. 1 = The current VREF is 0, the minimum VREF.
50	RWX	WR_VREF_TWO_RANGE_BEST_CASE_ERR0: DRAM 0. 0 = No error. 1 = There are maximums found above and below the nominal VREF.

Bits	SCOM	Field Mnemonic: Description
51	RWX	WR_VREF_BIT_STEP_DELTA_ERR0: DRAM 0. 0 = No error. 1 = The maximum and minimum VREF values are at least one big step apart.
52	RWX	WR_VREF_STEP_RANGE_EDGE_ERR0: DRAM 0. 0 = No error. 1 = Small stepping is on the edge of, or outside of, previously tested ranges.
53	RWX	WR_VREF_NO_INCREASE_ERR0: DRAM 0. 0 = No error. 1 = No increase was found.
54	RWX	WR_VREF_1D_EYE_NOISE_ERR0: DRAM 0. 0 = No error. 1 = A current-to-previous delta greater than a coarse_step was found.
55	RWX	WR_VREF_BAD_BIT_ERR0: DRAM 0. 0 = No error. 1 = A bad bit is found, but not during the first or last VREF.
56	RWX	WR_VREF_MAX_RANGE_ERR1: DRAM 1. 0 = No error. 1 = The current VREF goes outside of the maximum range.
57	RWX	WR_VREF_MIN_RANGE_ERR1: DRAM 1. 0 = No error. 1 = The current VREF is 0, the minimum VREF.
58	RWX	WR_VREF_TWO_RANGE_BEST_CASE_ERR1: DRAM 1. 0 = No error. 1 = There are maximums found above and below the nominal VREF.
59	RWX	WR_VREF_BIT_STEP_DELTA_ERR1: DRAM 1. 0 = No error. 1 = The maximum and minimum VREF values are at least one big step apart.
60	RWX	WR_VREF_STEP_RANGE_EDGE_ERR1: DRAM 1. 0 = No error. 1 = Small stepping is on the edge of, or outside of, previously tested ranges.
61	RWX	WR_VREF_NO_INCREASE_ERR1: DRAM 1. 0 = No error. 1 = No increase was found.
62	RWX	WR_VREF_1D_EYE_NOISE_ERR1: DRAM 1. 0 = No error. 1 = A current-to-previous delta greater than a coarse_step was found.
63	RWX	WR_VREF_BAD_BIT_ERR1: DRAM 1. 0 = No error. 1 = A bad bit is found, but not during the first or last VREF.

Register Name	DP16 Write VREF Error 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_ERROR0_P3_[n]
Address	800000AE07011C3F (SCOM), +0x0400_0000_0000
Description	This register provides error information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	WR_VREF_MAX_RANGE_ERR0: DRAM 0. 0 = No error. 1 = The current VREF goes outside of the maximum range.
49	RWX	WR_VREF_MIN_RANGE_ERR0: DRAM 0. 0 = No error. 1 = The current VREF is 0, the minimum VREF.
50	RWX	WR_VREF_TWO_RANGE_BEST_CASE_ERR0: DRAM 0. 0 = No error. 1 = There are maximums found above and below the nominal VREF.
51	RWX	WR_VREF_BIT_STEP_DELTA_ERR0: DRAM 0. 0 = No error. 1 = The maximum and minimum VREF values are at least one big step apart.
52	RWX	WR_VREF_STEP_RANGE_EDGE_ERR0: DRAM 0. 0 = No error. 1 = Small stepping is on the edge of, or outside of, previously tested ranges.
53	RWX	WR_VREF_NO_INCREASE_ERR0: DRAM 0. 0 = No error. 1 = No increase was found.
54	RWX	WR_VREF_1D_EYE_NOISE_ERR0: DRAM 0. 0 = No error. 1 = A current-to-previous delta greater than a coarse_step was found.
55	RWX	WR_VREF_BAD_BIT_ERR0: DRAM 0. 0 = No error. 1 = A bad bit is found, but not during the first or last VREF.
56	RWX	WR_VREF_MAX_RANGE_ERR1: DRAM 1. 0 = No error. 1 = The current VREF goes outside of the maximum range.
57	RWX	WR_VREF_MIN_RANGE_ERR1: DRAM 1. 0 = No error. 1 = The current VREF is 0, the minimum VREF.
58	RWX	WR_VREF_TWO_RANGE_BEST_CASE_ERR1: DRAM 1. 0 = No error. 1 = There are maximums found above and below the nominal VREF.
59	RWX	WR_VREF_BIT_STEP_DELTA_ERR1: DRAM 1. 0 = No error. 1 = The maximum and minimum VREF values are at least one big step apart.
60	RWX	WR_VREF_STEP_RANGE_EDGE_ERR1: DRAM 1. 0 = No error. 1 = Small stepping is on the edge of, or outside of, previously tested ranges.
61	RWX	WR_VREF_NO_INCREASE_ERR1: DRAM 1. 0 = No error. 1 = No increase was found.
62	RWX	WR_VREF_1D_EYE_NOISE_ERR1: DRAM 1. 0 = No error. 1 = A current-to-previous delta greater than a coarse_step was found.
63	RWX	WR_VREF_BAD_BIT_ERR1: DRAM 1. 0 = No error. 1 = A bad bit is found, but not during the first or last VREF.

Register Name	DP16 Write VREF Error 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_ERROR1_P0_[n]
Address	800000AF0701103F (SCOM), +0x0400_0000_0000
Description	This register provides error information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RWX	WR_VREF_MAX_RANGE_ERR2: DRAM 2. 0 = No error. 1 = The current VREF goes outside of the maximum range.
49	RWX	WR_VREF_MIN_RANGE_ERR2: DRAM 2. 0 = No error. 1 = The current VREF is 0, the minimum VREF.
50	RWX	WR_VREF_TWO_RANGE_BEST_CASE_ERR2: DRAM 2. 0 = No error. 1 = There are maximums found above and below the nominal VREF.
51	RWX	WR_VREF_BIT_STEP_DELTA_ERR2: DRAM 2. 0 = No error. 1 = The maximum and minimum VREF values are at least one big step apart.
52	RWX	WR_VREF_STEP_RANGE_EDGE_ERR2: DRAM 2. 0 = No error. 1 = Small stepping is on the edge of, or outside of, previously tested ranges.
53	RWX	WR_VREF_NO_INCREASE_ERR2: DRAM 2. 0 = No error. 1 = No increase was found.
54	RWX	WR_VREF_1D_EYE_NOISE_ERR2: DRAM 2. 0 = No error. 1 = A current-to-previous delta greater than a coarse_step was found.
55	RWX	WR_VREF_BAD_BIT_ERR2: DRAM 2. 0 = No error. 1 = A bad bit is found, but not during the first or last VREF.
56	RWX	WR_VREF_MAX_RANGE_ERR3: DRAM 3. 0 = No error. 1 = The current VREF goes outside of the maximum range.
57	RWX	WR_VREF_MIN_RANGE_ERR3: DRAM 3. 0 = No error. 1 = The current VREF is 0, the minimum VREF.
58	RWX	WR_VREF_TWO_RANGE_BEST_CASE_ERR3: DRAM 3. 0 = No error. 1 = There are maximums found above and below the nominal VREF.
59	RWX	WR_VREF_BIT_STEP_DELTA_ERR3: DRAM 3. 0 = No error. 1 = The maximum and minimum VREF values are at least one big step apart.
60	RWX	WR_VREF_STEP_RANGE_EDGE_ERR3: DRAM 3. 0 = No error. 1 = Small stepping is on the edge of, or outside of, previously tested ranges.
61	RWX	WR_VREF_NO_INCREASE_ERR3: DRAM 3. 0 = No error. 1 = No increase was found.

Bits	SCOM	Field Mnemonic: Description
62	RWX	WR_VREF_1D_EYE_NOISE_ERR3: DRAM 3. 0 = No error. 1 = A current-to-previous delta greater than a coarse_step was found.
63	RWX	WR_VREF_BAD_BIT_ERR3: DRAM 3. 0 = No error. 1 = A bad bit is found, but not during the first or last VREF.

Register Name	**DP16 Write VREF Error 1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_ERROR1_P1_[n]
Address	800000AF0701143F (SCOM), +0x0400_0000_0000
Description	This register provides error information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RWX	WR_VREF_MAX_RANGE_ERR2: DRAM 2. 0 = No error. 1 = The current VREF goes outside of the maximum range.
49	RWX	WR_VREF_MIN_RANGE_ERR2: DRAM 2. 0 = No error. 1 = The current VREF is 0, the minimum VREF.
50	RWX	WR_VREF_TWO_RANGE_BEST_CASE_ERR2: DRAM 2. 0 = No error. 1 = There are maximums found above and below the nominal VREF.
51	RWX	WR_VREF_BIT_STEP_DELTA_ERR2: DRAM 2. 0 = No error. 1 = The maximum and minimum VREF values are at least one big step apart.
52	RWX	WR_VREF_STEP_RANGE_EDGE_ERR2: DRAM 2. 0 = No error. 1 = Small stepping is on the edge of, or outside of, previously tested ranges.
53	RWX	WR_VREF_NO_INCREASE_ERR2: DRAM 2. 0 = No error. 1 = No increase was found.
54	RWX	WR_VREF_1D_EYE_NOISE_ERR2: DRAM 2. 0 = No error. 1 = A current-to-previous delta greater than a coarse_step was found.
55	RWX	WR_VREF_BAD_BIT_ERR2: DRAM 2. 0 = No error. 1 = A bad bit is found, but not during the first or last VREF.
56	RWX	WR_VREF_MAX_RANGE_ERR3: DRAM 3. 0 = No error. 1 = The current VREF goes outside of the maximum range.
57	RWX	WR_VREF_MIN_RANGE_ERR3: DRAM 3. 0 = No error. 1 = The current VREF is 0, the minimum VREF.
58	RWX	WR_VREF_TWO_RANGE_BEST_CASE_ERR3: DRAM 3. 0 = No error. 1 = There are maximums found above and below the nominal VREF.

Bits	SCOM	Field Mnemonic: Description
59	RWX	WR_VREF_BIT_STEP_DELTA_ERR3: DRAM 3. 0 = No error. 1 = The maximum and minimum VREF values are at least one big step apart.
60	RWX	WR_VREF_STEP_RANGE_EDGE_ERR3: DRAM 3. 0 = No error. 1 = Small stepping is on the edge of, or outside of, previously tested ranges.
61	RWX	WR_VREF_NO_INCREASE_ERR3: DRAM 3. 0 = No error. 1 = No increase was found.
62	RWX	WR_VREF_1D_EYE_NOISE_ERR3: DRAM 3. 0 = No error. 1 = A current-to-previous delta greater than a coarse_step was found.
63	RWX	WR_VREF_BAD_BIT_ERR3: DRAM 3. 0 = No error. 1 = A bad bit is found, but not during the first or last VREF.

Register Name	DP16 Write VREF Error 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_ERROR1_P2_[n]
Address	800000AF0701183F (SCOM), +0x0400_0000_0000
Description	This register provides error information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RWX	WR_VREF_MAX_RANGE_ERR2: DRAM 2. 0 = No error. 1 = The current VREF goes outside of the maximum range.
49	RWX	WR_VREF_MIN_RANGE_ERR2: DRAM 2. 0 = No error. 1 = The current VREF is 0, the minimum VREF.
50	RWX	WR_VREF_TWO_RANGE_BEST_CASE_ERR2: DRAM 2. 0 = No error. 1 = There are maximums found above and below the nominal VREF.
51	RWX	WR_VREF_BIT_STEP_DELTA_ERR2: DRAM 2. 0 = No error. 1 = The maximum and minimum VREF values are at least one big step apart.
52	RWX	WR_VREF_STEP_RANGE_EDGE_ERR2: DRAM 2. 0 = No error. 1 = Small stepping is on the edge of, or outside of, previously tested ranges.
53	RWX	WR_VREF_NO_INCREASE_ERR2: DRAM 2. 0 = No error. 1 = No increase was found.
54	RWX	WR_VREF_1D_EYE_NOISE_ERR2: DRAM 2. 0 = No error. 1 = A current-to-previous delta greater than a coarse_step was found.
55	RWX	WR_VREF_BAD_BIT_ERR2: DRAM 2. 0 = No error. 1 = A bad bit is found, but not during the first or last VREF.

Bits	SCOM	Field Mnemonic: Description
56	RWX	WR_VREF_MAX_RANGE_ERR3: DRAM 3. 0 = No error. 1 = The current VREF goes outside of the maximum range.
57	RWX	WR_VREF_MIN_RANGE_ERR3: DRAM 3. 0 = No error. 1 = The current VREF is 0, the minimum VREF.
58	RWX	WR_VREF_TWO_RANGE_BEST_CASE_ERR3: DRAM 3. 0 = No error. 1 = There are maximums found above and below the nominal VREF.
59	RWX	WR_VREF_BIT_STEP_DELTA_ERR3: DRAM 3. 0 = No error. 1 = The maximum and minimum VREF values are at least one big step apart.
60	RWX	WR_VREF_STEP_RANGE_EDGE_ERR3: DRAM 3. 0 = No error. 1 = Small stepping is on the edge of, or outside of, previously tested ranges.
61	RWX	WR_VREF_NO_INCREASE_ERR3: DRAM 3. 0 = No error. 1 = No increase was found.
62	RWX	WR_VREF_1D_EYE_NOISE_ERR3: DRAM 3. 0 = No error. 1 = A current-to-previous delta greater than a coarse_step was found.
63	RWX	WR_VREF_BAD_BIT_ERR3: DRAM 3. 0 = No error. 1 = A bad bit is found, but not during the first or last VREF.

Register Name	**DP16 Write VREF Error 1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_ERROR1_P3_[n]
Address	800000AF07011C3F (SCOM), +0x0400_0000_0000
Description	This register provides error information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RWX	WR_VREF_MAX_RANGE_ERR2: DRAM 2. 0 = No error. 1 = The current VREF goes outside of the maximum range.
49	RWX	WR_VREF_MIN_RANGE_ERR2: DRAM 2. 0 = No error. 1 = The current VREF is 0, the minimum VREF.
50	RWX	WR_VREF_TWO_RANGE_BEST_CASE_ERR2: DRAM 2. 0 = No error. 1 = There are maximums found above and below the nominal VREF.
51	RWX	WR_VREF_BIT_STEP_DELTA_ERR2: DRAM 2. 0 = No error. 1 = The maximum and minimum VREF values are at least one big step apart.
52	RWX	WR_VREF_STEP_RANGE_EDGE_ERR2: DRAM 2. 0 = No error. 1 = Small stepping is on the edge of, or outside of, previously tested ranges.

Bits	SCOM	Field Mnemonic: Description
53	RWX	WR_VREF_NO_INCREASE_ERR2: DRAM 2. 0 = No error. 1 = No increase was found.
54	RWX	WR_VREF_1D_EYE_NOISE_ERR2: DRAM 2. 0 = No error. 1 = A current-to-previous delta greater than a coarse_step was found.
55	RWX	WR_VREF_BAD_BIT_ERR2: DRAM 2. 0 = No error. 1 = A bad bit is found, but not during the first or last VREF.
56	RWX	WR_VREF_MAX_RANGE_ERR3: DRAM 3. 0 = No error. 1 = The current VREF goes outside of the maximum range.
57	RWX	WR_VREF_MIN_RANGE_ERR3: DRAM 3. 0 = No error. 1 = The current VREF is 0, the minimum VREF.
58	RWX	WR_VREF_TWO_RANGE_BEST_CASE_ERR3: DRAM 3. 0 = No error. 1 = There are maximums found above and below the nominal VREF.
59	RWX	WR_VREF_BIT_STEP_DELTA_ERR3: DRAM 3. 0 = No error. 1 = The maximum and minimum VREF values are at least one big step apart.
60	RWX	WR_VREF_STEP_RANGE_EDGE_ERR3: DRAM 3. 0 = No error. 1 = Small stepping is on the edge of, or outside of, previously tested ranges.
61	RWX	WR_VREF_NO_INCREASE_ERR3: DRAM 3. 0 = No error. 1 = No increase was found.
62	RWX	WR_VREF_1D_EYE_NOISE_ERR3: DRAM 3. 0 = No error. 1 = A current-to-previous delta greater than a coarse_step was found.
63	RWX	WR_VREF_BAD_BIT_ERR3: DRAM 3. 0 = No error. 1 = A bad bit is found, but not during the first or last VREF.

Register Name	**DP16 Read VREF DAC 2 [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_DAC_2_P0_[n]
Address	800000C00701103F (SCOM), +0x0400_0000_0000
Description	This register controls the DAC settings of the read VREF in the DP16 unit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	BIT4_VREF_DAC: DAC setting to control VREF on bit 4 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.
56	RW	Reserved.

Bits	SCOM	Field Mnemonic: Description
57:63	RW	BIT5_VREF_DAC: DAC setting to control VREF on bit 5 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.

Register Name	DP16 Read VREF DAC 2 [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_DAC_2_P1_[n]
Address	800000C00701143F (SCOM), +0x0400_0000_0000
Description	This register controls the DAC settings of the read VREF in the DP16 unit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	BIT4_VREF_DAC: DAC setting to control VREF on bit 4 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.
56	RW	Reserved.
57:63	RW	BIT5_VREF_DAC: DAC setting to control VREF on bit 5 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.

Register Name	DP16 Read VREF DAC 2 [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_DAC_2_P2_[n]
Address	800000C00701183F (SCOM), +0x0400_0000_0000
Description	This register controls the DAC settings of the read VREF in the DP16 unit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	BIT4_VREF_DAC: DAC setting to control VREF on bit 4 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.
56	RW	Reserved.
57:63	RW	BIT5_VREF_DAC: DAC setting to control VREF on bit 5 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.

Register Name	DP16 Read VREF DAC 2 [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_DAC_2_P3_[n]
Address	800000C007011C3F (SCOM), +0x0400_0000_0000
Description	This register controls the DAC settings of the read VREF in the DP16 unit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	BIT4_VREF_DAC: DAC setting to control VREF on bit 4 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.
56	RW	Reserved.
57:63	RW	BIT5_VREF_DAC: DAC setting to control VREF on bit 5 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.

Register Name	DP16 Read VREF DAC 3 [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_DAC_3_P0_[n]
Address	800000C10701103F (SCOM), +0x0400_0000_0000
Description	This register controls the DAC settings of the read VREF in the DP16 unit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	BIT6_VREF_DAC: DAC setting to control VREF on bit 6 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.
56	RW	Reserved.
57:63	RW	BIT7_VREF_DAC: DAC setting to control VREF on bit 7 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.

Register Name	DP16 Read VREF DAC 3 [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_DAC_3_P1_[n]
Address	800000C10701143F (SCOM), +0x0400_0000_0000
Description	This register controls the DAC settings of the read VREF in the DP16 unit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.

Bits	SCOM	Field Mnemonic: Description
49:55	RW	BIT6_VREF_DAC: DAC setting to control VREF on bit 6 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.
56	RW	Reserved.
57:63	RW	BIT7_VREF_DAC: DAC setting to control VREF on bit 7 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.

Register Name	DP16 Read VREF DAC 3 [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_DAC_3_P2_[n]
Address	800000C10701183F (SCOM), +0x0400_0000_0000
Description	This register controls the DAC settings of the read VREF in the DP16 unit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	BIT6_VREF_DAC: DAC setting to control VREF on bit 6 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.
56	RW	Reserved.
57:63	RW	BIT7_VREF_DAC: DAC setting to control VREF on bit 7 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.

Register Name	DP16 Read VREF DAC 3 [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_DAC_3_P3_[n]
Address	800000C107011C3F (SCOM), +0x0400_0000_0000
Description	This register controls the DAC settings of the read VREF in the DP16 unit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	BIT6_VREF_DAC: DAC setting to control VREF on bit 6 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.
56	RW	Reserved.
57:63	RW	BIT7_VREF_DAC: DAC setting to control VREF on bit 7 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.

Register Name	DP16 Read VREF DAC 4 [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_DAC_4_P0_[n]
Address	800000C20701103F (SCOM), +0x0400_0000_0000
Description	This register controls the DAC settings of the read VREF in the DP16 unit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	BIT8_VREF_DAC: DAC setting to control VREF on bit 8 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.
56	RW	Reserved.
57:63	RW	BIT9_VREF_DAC: DAC setting to control VREF on bit 9 in DP16. This value is overwritten by the hardware when Read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.

Register Name	DP16 Read VREF DAC 4 [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_DAC_4_P1_[n]
Address	800000C20701143F (SCOM), +0x0400_0000_0000
Description	This register controls the DAC settings of the read VREF in the DP16 unit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	BIT8_VREF_DAC: DAC setting to control VREF on bit 8 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.
56	RW	Reserved.
57:63	RW	BIT9_VREF_DAC: DAC setting to control VREF on bit 9 in DP16. This value is overwritten by the hardware when Read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.

Register Name	DP16 Read VREF DAC 4 [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_DAC_4_P2_[n]
Address	800000C20701183F (SCOM), +0x0400_0000_0000
Description	This register controls the DAC settings of the read VREF in the DP16 unit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RW	Reserved.
49:55	RW	BIT8_VREF_DAC: DAC setting to control VREF on bit 8 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.
56	RW	Reserved.
57:63	RW	BIT9_VREF_DAC: DAC setting to control VREF on bit 9 in DP16. This value is overwritten by the hardware when Read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.

Register Name	**DP16 Read VREF DAC 4 [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_DAC_4_P3_[n]
Address	800000C207011C3F (SCOM), +0x0400_0000_0000
Description	This register controls the DAC settings of the read VREF in the DP16 unit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	BIT8_VREF_DAC: DAC setting to control VREF on bit 8 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.
56	RW	Reserved.
57:63	RW	BIT9_VREF_DAC: DAC setting to control VREF on bit 9 in DP16. This value is overwritten by the hardware when Read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.

Register Name	**DP16 Read VREF DAC 5 [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_DAC_5_P0_[n]
Address	800000C30701103F (SCOM), +0x0400_0000_0000
Description	This register controls the DAC settings of the read VREF in the DP16 unit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	BIT10_VREF_DAC: DAC setting to control VREF on bit 10 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.
56	RW	Reserved.

Bits	SCOM	Field Mnemonic: Description
57:63	RW	BIT11_VREF_DAC: DAC setting to control VREF on bit 11 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.

Register Name	**DP16 Read VREF DAC 5 [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_DAC_5_P1_[n]
Address	800000C30701143F (SCOM), +0x0400_0000_0000
Description	This register controls the DAC settings of the read VREF in the DP16 unit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	BIT10_VREF_DAC: DAC setting to control VREF on bit 10 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.
56	RW	Reserved.
57:63	RW	BIT11_VREF_DAC: DAC setting to control VREF on bit 11 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.

Register Name	**DP16 Read VREF DAC 5 [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_DAC_5_P2_[n]
Address	800000C30701183F (SCOM), +0x0400_0000_0000
Description	This register controls the DAC settings of the read VREF in the DP16 unit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	BIT10_VREF_DAC: DAC setting to control VREF on bit 10 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.
56	RW	Reserved.
57:63	RW	BIT11_VREF_DAC: DAC setting to control VREF on bit 11 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.

Register Name	DP16 Read VREF DAC 5 [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_DAC_5_P3_[n]
Address	800000C307011C3F (SCOM), +0x0400_0000_0000
Description	This register controls the DAC settings of the read VREF in the DP16 unit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	BIT10_VREF_DAC: DAC setting to control VREF on bit 10 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.
56	RW	Reserved.
57:63	RW	BIT11_VREF_DAC: DAC setting to control VREF on bit 11 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.

Register Name	DP16 Read VREF DAC 6 [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_DAC_6_P0_[n]
Address	800000C40701103F (SCOM), +0x0400_0000_0000
Description	This register controls the DAC settings of the read VREF in the DP16 unit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	BIT12_VREF_DAC: DAC setting to control VREF on bit 12 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.
56	RW	Reserved.
57:63	RW	BIT13_VREF_DAC: DAC setting to control VREF on bit 13 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.

Register Name	DP16 Read VREF DAC 6 [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_DAC_6_P1_[n]
Address	800000C40701143F (SCOM), +0x0400_0000_0000
Description	This register controls the DAC settings of the read VREF in the DP16 unit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.

Bits	SCOM	Field Mnemonic: Description
49:55	RW	BIT12_VREF_DAC: DAC setting to control VREF on bit 12 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.
56	RW	Reserved.
57:63	RW	BIT13_VREF_DAC: DAC setting to control VREF on bit 13 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.

Register Name	**DP16 Read VREF DAC 6 [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_DAC_6_P2_[n]
Address	800000C40701183F (SCOM), +0x0400_0000_0000
Description	This register controls the DAC settings of the read VREF in the DP16 unit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	BIT12_VREF_DAC: DAC setting to control VREF on bit 12 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.
56	RW	Reserved.
57:63	RW	BIT13_VREF_DAC: DAC setting to control VREF on bit 13 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.

Register Name	**DP16 Read VREF DAC 6 [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_DAC_6_P3_[n]
Address	800000C407011C3F (SCOM), +0x0400_0000_0000
Description	This register controls the DAC settings of the read VREF in the DP16 unit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	Reserved.
49:55	RW	BIT12_VREF_DAC: DAC setting to control VREF on bit 12 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.
56	RW	Reserved.
57:63	RW	BIT13_VREF_DAC: DAC setting to control VREF on bit 13 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.

Register Name	DP16 Read VREF DAC 7 [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_DAC_7_P0_[n]
Address	800000C50701103F (SCOM), +0x0400_0000_0000
Description	This register controls the DAC settings of the read VREF in the DP16 unit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	DD2_PERBIT_RDVREF_DISABLE: 0 = Enable DD2 per-bit read VREF support. 1 = Enable averaging function per nibble.
49:55	RW	BIT14_VREF_DAC: DAC setting to control VREF on bit 14 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.
56	RW	Reserved.
57:63	RW	BIT15_VREF_DAC: DAC setting to control VREF on bit 15 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.

Register Name	DP16 Read VREF DAC 7 [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_DAC_7_P1_[n]
Address	800000C50701143F (SCOM), +0x0400_0000_0000
Description	This register controls the DAC settings of the read VREF in the DP16 unit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	DD2_PERBIT_RDVREF_DISABLE: 0 = Enable DD2 per-bit read VREF support. 1 = Enable averaging function per nibble.
49:55	RW	BIT14_VREF_DAC: DAC setting to control VREF on bit 14 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.
56	RW	Reserved.
57:63	RW	BIT15_VREF_DAC: DAC setting to control VREF on bit 15 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.

Register Name	DP16 Read VREF DAC 7 [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_DAC_7_P2_[n]
Address	800000C50701183F (SCOM), +0x0400_0000_0000
Description	This register controls the DAC settings of the read VREF in the DP16 unit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	DD2_PERBIT_RDVREF_DISABLE: 0 = Enable DD2 per-bit read VREF support. 1 = Enable averaging function per nibble.
49:55	RW	BIT14_VREF_DAC: DAC setting to control VREF on bit 14 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.
56	RW	Reserved.
57:63	RW	BIT15_VREF_DAC: DAC setting to control VREF on bit 15 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.

Register Name	**DP16 Read VREF DAC 7 [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_DAC_7_P3_[n]
Address	800000C507011C3F (SCOM), +0x0400_0000_0000
Description	This register controls the DAC settings of the read VREF in the DP16 unit.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	DD2_PERBIT_RDVREF_DISABLE: 0 = Enable DD2 per-bit read VREF support. 1 = Enable averaging function per nibble.
49:55	RW	BIT14_VREF_DAC: DAC setting to control VREF on bit 14 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.
56	RW	Reserved.
57:63	RW	BIT15_VREF_DAC: DAC setting to control VREF on bit 15 in DP16. This value is overwritten by the hardware when read VREF calibration is performed with the value calculated by the algorithm. If a value is written in here manually, it is used in the read VREF DAC functionally unless read VREF calibration is performed again. If DD2_PERBIT_RDVREF_DISABLE = 1, this field has no function.

Register Name	**DP16 Write VREF Configuration 1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_CONFIG1_P0_[n]
Address	800000EC0701103F (SCOM), +0x0400_0000_0000
Description	This register controls the write VREF operation.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	WR_CTR_VREF_RANGE_SELECT: This bit controls the default write VREF range. Set this to the desired MR6 A6 value. 0 = Use the write VREF range 1. 1 = Use the write VREF range 2.

Bits	SCOM	Field Mnemonic: Description
49:55	RW	WR_CTR_VREF_RANGE_CROSSOVER: This field enables the user to configure the crossover point between the write VREF ranges. The default value is where the range 2 value equals the range 1 value of all zeros. The value must always be greater than or equal to this crossover point. Note: This value is taken from the JEDEC specification.
56:62	RW	WR_CTR_VREF_SINGLE_RANGE_MAX: This field enables the user to configure the maximum value in a single write VREF range. If the user wants to change this from the default value, it must have a value less than the default value. (wr_ctr_vref_single_range_max + wr_ctr_vref_range_crossover = wr_ctr_max_vref_range) is the maximum value to which the algorithm will run. Note: This value is taken from the JEDEC specification.
63	RW	Reserved.

Register Name	DP16 Write VREF Configuration 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_CONFIG1_P1_[n]
Address	800000EC0701143F (SCOM), +0x0400_0000_0000
Description	This register controls the write VREF operation.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	WR_CTR_VREF_RANGE_SELECT: This bit controls the default write VREF range. Set this to the desired MR6 A6 value. 0 = Use the write VREF range 1. 1 = Use the write VREF range 2.
49:55	RW	WR_CTR_VREF_RANGE_CROSSOVER: This field enables the user to configure the crossover point between the write VREF ranges. The default value is where the range 2 value equals the range 1 value of all zeros. The value must always be greater than or equal to this crossover point. Note: This value is taken from the JEDEC specification.
56:62	RW	WR_CTR_VREF_SINGLE_RANGE_MAX: This field enables the user to configure the maximum value in a single write VREF range. If the user wants to change this from the default value, it must have a value less than the default value. (wr_ctr_vref_single_range_max + wr_ctr_vref_range_crossover = wr_ctr_max_vref_range) is the maximum value to which the algorithm will run. Note: This value is taken from the JEDEC specification.
63	RW	Reserved.

Register Name	DP16 Write VREF Configuration 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_CONFIG1_P2_[n]
Address	800000EC0701183F (SCOM), +0x0400_0000_0000
Description	This register controls the write VREF operation.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	WR_CTR_VREF_RANGE_SELECT: This bit controls the default write VREF range. Set this to the desired MR6 A6 value. 0 = Use the write VREF range 1. 1 = Use the write VREF range 2.

Bits	SCOM	Field Mnemonic: Description
49:55	RW	WR_CTR_VREF_RANGE_CROSSOVER: This field enables the user to configure the crossover point between the write VREF ranges. The default value is where the range 2 value equals the range 1 value of all zeros. The value must always be greater than or equal to this crossover point. Note: This value is taken from the JEDEC specification.
56:62	RW	WR_CTR_VREF_SINGLE_RANGE_MAX: This field enables the user to configure the maximum value in a single write VREF range. If the user wants to change this from the default value, it must have a value less than the default value. (wr_ctr_vref_single_range_max + wr_ctr_vref_range_crossover = wr_ctr_max_vref_range) is the maximum value to which the algorithm will run. Note: This value is taken from the JEDEC specification.
63	RW	Reserved.

Register Name	DP16 Write VREF Configuration 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_CONFIG1_P3_[n]
Address	800000EC07011C3F (SCOM), +0x0400_0000_0000
Description	This register controls the write VREF operation.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	WR_CTR_VREF_RANGE_SELECT: This bit controls the default write VREF range. Set this to the desired MR6 A6 value. 0 = Use the write VREF range 1. 1 = Use the write VREF range 2.
49:55	RW	WR_CTR_VREF_RANGE_CROSSOVER: This field enables the user to configure the crossover point between the write VREF ranges. The default value is where the range 2 value equals the range 1 value of all zeros. The value must always be greater than or equal to this crossover point. Note: This value is taken from the JEDEC specification.
56:62	RW	WR_CTR_VREF_SINGLE_RANGE_MAX: This field enables the user to configure the maximum value in a single write VREF range. If the user wants to change this from the default value, it must have a value less than the default value. (wr_ctr_vref_single_range_max + wr_ctr_vref_range_crossover = wr_ctr_max_vref_range) is the maximum value to which the algorithm will run. Note: This value is taken from the JEDEC specification.
63	RW	Reserved.

Register Name	DP16 Read VREF DAC Comparator Output Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_DAC_COMP_OUT_P0_[n]
Address	800000F60701103F (SCOM), +0x0400_0000_0000
Description	The output of the read VREF DAC comparators is captured in this register. Bits 48:63 correspond to the read VREF calibration circuitry in each bit of DQ 0:15.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	ROX	VREF_DAC_COMP_OUT: This field captures the output of the comparators in the read VREF circuitry. The DAC value to be used is entered in the corresponding nibble field in the DP16 Read VREF DAC 0 and DP16 Read VREF DAC 1 Registers. The enable bits are set in the DP16 Read VREF DAC Comparator Ouptut Register. The enable bits are forced to the analog circuitry by forcing the appropriate nibble in the DP16 Read VREF DAC 0 and DP16 Read VREF DAC 1 Registers. The value captured is the result of the following relationship: Output = 0 when Vpad < VREF and enable = 1. Output = 1 when Vpad > VREF or enable = 0.

Register Name	**DP16 Read VREF DAC Comparator Output Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_DAC_COMP_OUT_P1_[n]
Address	800000F60701143F (SCOM), +0x0400_0000_0000
Description	The output of the read VREF DAC comparators is captured in this register. Bits 48:63 correspond to the read VREF calibration circuitry in each bit of DQ 0:15.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	ROX	VREF_DAC_COMP_OUT: This field captures the output of the comparators in the read VREF circuitry. The DAC value to be used is entered in the corresponding nibble field in the DP16 Read VREF DAC 0 and DP16 Read VREF DAC 1 Registers. The enable bits are set in the DP16 Read VREF DAC Comparator Ouptut Register. The enable bits are forced to the analog circuitry by forcing the appropriate nibble in the DP16 Read VREF DAC 0 and DP16 Read VREF DAC 1 Registers. The value captured is the result of the following relationship: Output = 0 when Vpad < VREF and enable = 1. Output = 1 when Vpad > VREF or enable = 0.

Register Name	**DP16 Read VREF DAC Comparator Output Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_DAC_COMP_OUT_P2_[n]
Address	800000F60701183F (SCOM), +0x0400_0000_0000
Description	The output of the read VREF DAC comparators is captured in this register. Bits 48:63 correspond to the read VREF calibration circuitry in each bit of DQ 0:15.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	ROX	VREF_DAC_COMP_OUT: This field captures the output of the comparators in the read VREF circuitry. The DAC value to be used is entered in the corresponding nibble field in the DP16 Read VREF DAC 0 and DP16 Read VREF DAC 1 Registers. The enable bits are set in the DP16 Read VREF DAC Comparator Ouptut Register. The enable bits are forced to the analog circuitry by forcing the appropriate nibble in the DP16 Read VREF DAC 0 and DP16 Read VREF DAC 1 Registers. The value captured is the result of the following relationship: Output = 0 when Vpad < VREF and enable = 1. Output = 1 when Vpad > VREF or enable = 0.

Register Name	DP16 Read VREF DAC Comparator Output Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_RD_VREF_DAC_COMP_OUT_P3_[n]
Address	800000F607011C3F (SCOM), +0x0400_0000_0000
Description	The output of the read VREF DAC comparators is captured in this register. Bits 48:63 correspond to the read VREF calibration circuitry in each bit of DQ 0:15.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	ROX	VREF_DAC_COMP_OUT: This field captures the output of the comparators in the read VREF circuitry. The DAC value to be used is entered in the corresponding nibble field in the DP16 Read VREF DAC 0 and DP16 Read VREF DAC 1 Registers. The enable bits are set in the DP16 Read VREF DAC Comparator Ouptut Register. The enable bits are forced to the analog circuitry by forcing the appropriate nibble in the DP16 Read VREF DAC 0 and DP16 Read VREF DAC 1 Registers. The value captured is the result of the following relationship: Output = 0 when Vpad < VREF and enable = 1. Output = 1 when Vpad > VREF or enable = 0.

Register Name	DP16 Write VREF Error Mask 1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_ERROR_MASK1_P0_[n]
Address	800000FA0701103F (SCOM), +0x0400_0000_0000
Description	This register provides masks for error information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	WR_VREF_MAX_RANGE_MASK2: DRAM 2. 0 = No mask. 1 = The error is masked.
49	RW	WR_VREF_MIN_RANGE_MASK2: DRAM 2. 0 = No mask. 1 = The error is masked.
50	RW	WR_VREF_TWO_RANGE_BEST_CASE_MASK2: DRAM 2. 0 = No mask. 1 = The error is masked.
51	RW	WR_VREF_BIT_STEP_DELTA_MASK2: DRAM 2. 0 = No mask. 1 = The error is masked.
52	RW	WR_VREF_STEP_RANGE_EDGE_MASK2: DRAM 2. 0 = No mask. 1 = The error is masked.
53	RW	WR_VREF_NO_INCREASE_MASK2: DRAM 2. 0 = No mask. 1 = The error is masked.
54	RW	WR_VREF_1D_EYE_NOISE_MASK2: DRAM 2. 0 = No mask. 1 = The error is masked.
55	RW	WR_VREF_BAD_BIT_MASK2: DRAM 2. 0 = No mask. 1 = The error is masked.

Bits	SCOM	Field Mnemonic: Description
56	RW	WR_VREF_MAX_RANGE_MASK3: DRAM 3. 0 = No mask. 1 = The error is masked.
57	RW	WR_VREF_MIN_RANGE_MASK3: DRAM 3. 0 = No mask. 1 = The error is masked.
58	RW	WR_VREF_TWO_RANGE_BEST_CASE_MASK3: DRAM 3. 0 = No mask. 1 = The error is masked.
59	RW	WR_VREF_BIT_STEP_DELTA_MASK3: DRAM 3. 0 = No mask. 1 = The error is masked.
60	RW	WR_VREF_STEP_RANGE_EDGE_MASK3: DRAM 3. 0 = No mask. 1 = The error is masked.
61	RW	WR_VREF_NO_INCREASE_MASK3: DRAM 3. 0 = No mask. 1 = The error is masked.
62	RW	WR_VREF_1D_EYE_NOISE_MASK3: DRAM 3. 0 = No mask. 1 = The error is masked.
63	RW	WR_VREF_BAD_BIT_MASK3: DRAM 3. 0 = No mask. 1 = The error is masked.

Register Name	**DP16 Write VREF Error Mask 1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_ERROR_MASK1_P1_[n]
Address	800000FA0701143F (SCOM), +0x0400_0000_0000
Description	This register provides masks for error information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	WR_VREF_MAX_RANGE_MASK2: DRAM 2. 0 = No mask. 1 = The error is masked.
49	RW	WR_VREF_MIN_RANGE_MASK2: DRAM 2. 0 = No mask. 1 = The error is masked.
50	RW	WR_VREF_TWO_RANGE_BEST_CASE_MASK2: DRAM 2. 0 = No mask. 1 = The error is masked.
51	RW	WR_VREF_BIT_STEP_DELTA_MASK2: DRAM 2. 0 = No mask. 1 = The error is masked.
52	RW	WR_VREF_STEP_RANGE_EDGE_MASK2: DRAM 2. 0 = No mask. 1 = The error is masked.

Bits	SCOM	Field Mnemonic: Description
53	RW	WR_VREF_NO_INCREASE_MASK2: DRAM 2. 0 = No mask. 1 = The error is masked.
54	RW	WR_VREF_1D_EYE_NOISE_MASK2: DRAM 2. 0 = No mask. 1 = The error is masked.
55	RW	WR_VREF_BAD_BIT_MASK2: DRAM 2. 0 = No mask. 1 = The error is masked.
56	RW	WR_VREF_MAX_RANGE_MASK3: DRAM 3. 0 = No mask. 1 = The error is masked.
57	RW	WR_VREF_MIN_RANGE_MASK3: DRAM 3. 0 = No mask. 1 = The error is masked.
58	RW	WR_VREF_TWO_RANGE_BEST_CASE_MASK3: DRAM 3. 0 = No mask. 1 = The error is masked.
59	RW	WR_VREF_BIT_STEP_DELTA_MASK3: DRAM 3. 0 = No mask. 1 = The error is masked.
60	RW	WR_VREF_STEP_RANGE_EDGE_MASK3: DRAM 3. 0 = No mask. 1 = The error is masked.
61	RW	WR_VREF_NO_INCREASE_MASK3: DRAM 3. 0 = No mask. 1 = The error is masked.
62	RW	WR_VREF_1D_EYE_NOISE_MASK3: DRAM 3. 0 = No mask. 1 = The error is masked.
63	RW	WR_VREF_BAD_BIT_MASK3: DRAM 3. 0 = No mask. 1 = The error is masked.

Register Name	**DP16 Write VREF Error Mask 1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_ERROR_MASK1_P2_[n]
Address	800000FA0701183F (SCOM), +0x0400_0000_0000
Description	This register provides masks for error information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	WR_VREF_MAX_RANGE_MASK2: DRAM 2. 0 = No mask. 1 = The error is masked.
49	RW	WR_VREF_MIN_RANGE_MASK2: DRAM 2. 0 = No mask. 1 = The error is masked.

Bits	SCOM	Field Mnemonic: Description
50	RW	WR_VREF_TWO_RANGE_BEST_CASE_MASK2: DRAM 2. 0 = No mask. 1 = The error is masked.
51	RW	WR_VREF_BIT_STEP_DELTA_MASK2: DRAM 2. 0 = No mask. 1 = The error is masked.
52	RW	WR_VREF_STEP_RANGE_EDGE_MASK2: DRAM 2. 0 = No mask. 1 = The error is masked.
53	RW	WR_VREF_NO_INCREASE_MASK2: DRAM 2. 0 = No mask. 1 = The error is masked.
54	RW	WR_VREF_1D_EYE_NOISE_MASK2: DRAM 2. 0 = No mask. 1 = The error is masked.
55	RW	WR_VREF_BAD_BIT_MASK2: DRAM 2. 0 = No mask. 1 = The error is masked.
56	RW	WR_VREF_MAX_RANGE_MASK3: DRAM 3. 0 = No mask. 1 = The error is masked.
57	RW	WR_VREF_MIN_RANGE_MASK3: DRAM 3. 0 = No mask. 1 = The error is masked.
58	RW	WR_VREF_TWO_RANGE_BEST_CASE_MASK3: DRAM 3. 0 = No mask. 1 = The error is masked.
59	RW	WR_VREF_BIT_STEP_DELTA_MASK3: DRAM 3. 0 = No mask. 1 = The error is masked.
60	RW	WR_VREF_STEP_RANGE_EDGE_MASK3: DRAM 3. 0 = No mask. 1 = The error is masked.
61	RW	WR_VREF_NO_INCREASE_MASK3: DRAM 3. 0 = No mask. 1 = The error is masked.
62	RW	WR_VREF_1D_EYE_NOISE_MASK3: DRAM 3. 0 = No mask. 1 = The error is masked.
63	RW	WR_VREF_BAD_BIT_MASK3: DRAM 3. 0 = No mask. 1 = The error is masked.

Register Name	**DP16 Write VREF Error Mask 1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_ERROR_MASK1_P3_[n]
Address	800000FA07011C3F (SCOM), +0x0400_0000_0000
Description	This register provides masks for error information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	WR_VREF_MAX_RANGE_MASK2: DRAM 2. 0 = No mask. 1 = The error is masked.
49	RW	WR_VREF_MIN_RANGE_MASK2: DRAM 2. 0 = No mask. 1 = The error is masked.
50	RW	WR_VREF_TWO_RANGE_BEST_CASE_MASK2: DRAM 2. 0 = No mask. 1 = The error is masked.
51	RW	WR_VREF_BIT_STEP_DELTA_MASK2: DRAM 2. 0 = No mask. 1 = The error is masked.
52	RW	WR_VREF_STEP_RANGE_EDGE_MASK2: DRAM 2. 0 = No mask. 1 = The error is masked.
53	RW	WR_VREF_NO_INCREASE_MASK2: DRAM 2. 0 = No mask. 1 = The error is masked.
54	RW	WR_VREF_1D_EYE_NOISE_MASK2: DRAM 2. 0 = No mask. 1 = The error is masked.
55	RW	WR_VREF_BAD_BIT_MASK2: DRAM 2. 0 = No mask. 1 = The error is masked.
56	RW	WR_VREF_MAX_RANGE_MASK3: DRAM 3. 0 = No mask. 1 = The error is masked.
57	RW	WR_VREF_MIN_RANGE_MASK3: DRAM 3. 0 = No mask. 1 = The error is masked.
58	RW	WR_VREF_TWO_RANGE_BEST_CASE_MASK3: DRAM 3. 0 = No mask. 1 = The error is masked.
59	RW	WR_VREF_BIT_STEP_DELTA_MASK3: DRAM 3. 0 = No mask. 1 = The error is masked.
60	RW	WR_VREF_STEP_RANGE_EDGE_MASK3: DRAM 3. 0 = No mask. 1 = The error is masked.
61	RW	WR_VREF_NO_INCREASE_MASK3: DRAM 3. 0 = No mask. 1 = The error is masked.
62	RW	WR_VREF_1D_EYE_NOISE_MASK3: DRAM 3. 0 = No mask. 1 = The error is masked.
63	RW	WR_VREF_BAD_BIT_MASK3: DRAM 3. 0 = No mask. 1 = The error is masked.

Register Name	DP16 Write VREF Error Mask 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_ERROR_MASK0_P0_[n]
Address	800000FB0701103F (SCOM), +0x0400_0000_0000
Description	This register provides masks for error information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	WR_VREF_MAX_RANGE_MASK0: DRAM 0. 0 = No mask. 1 = The error is masked.
49	RW	WR_VREF_MIN_RANGE_MASK0: DRAM 0. 0 = No mask. 1 = The error is masked.
50	RW	WR_VREF_TWO_RANGE_BEST_CASE_MASK0: DRAM 0. 0 = No mask. 1 = The error is masked.
51	RW	WR_VREF_BIT_STEP_DELTA_MASK0: DRAM 0. 0 = No mask. 1 = The error is masked.
52	RW	WR_VREF_STEP_RANGE_EDGE_MASK0: DRAM 0. 0 = No mask. 1 = The error is masked.
53	RW	WR_VREF_NO_INCREASE_MASK0: DRAM 0. 0 = No mask. 1 = The error is masked.
54	RW	WR_VREF_1D_EYE_NOISE_MASK0: DRAM 0. 0 = No mask. 1 = The error is masked.
55	RW	WR_VREF_BAD_BIT_MASK0: DRAM 0. 0 = No mask. 1 = The error is masked.
56	RW	WR_VREF_MAX_RANGE_MASK1: DRAM 1. 0 = No mask. 1 = The error is masked.
57	RW	WR_VREF_MIN_RANGE_MASK1: DRAM 1. 0 = No mask. 1 = The error is masked.
58	RW	WR_VREF_TWO_RANGE_BEST_CASE_MASK1: DRAM 1. 0 = No mask. 1 = The error is masked.
59	RW	WR_VREF_BIT_STEP_DELTA_MASK1: DRAM 1. 0 = No mask. 1 = The error is masked.
60	RW	WR_VREF_STEP_RANGE_EDGE_MASK1: DRAM 1. 0 = No mask. 1 = The error is masked.
61	RW	WR_VREF_NO_INCREASE_MASK1: DRAM 1. 0 = No mask. 1 = The error is masked.

Bits	SCOM	Field Mnemonic: Description
62	RW	WR_VREF_1D_EYE_NOISE_MASK1: DRAM 1. 0 = No mask. 1 = The error is masked.
63	RW	WR_VREF_BAD_BIT_MASK1: DRAM 1. 0 = No mask. 1 = The error is masked.

Register Name	**DP16 Write VREF Error Mask 0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_ERROR_MASK0_P1_[n]
Address	800000FB0701143F (SCOM), +0x0400_0000_0000
Description	This register provides masks for error information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	RW	WR_VREF_MAX_RANGE_MASK0: DRAM 0. 0 = No mask. 1 = The error is masked.
49	RW	WR_VREF_MIN_RANGE_MASK0: DRAM 0. 0 = No mask. 1 = The error is masked.
50	RW	WR_VREF_TWO_RANGE_BEST_CASE_MASK0: DRAM 0. 0 = No mask. 1 = The error is masked.
51	RW	WR_VREF_BIT_STEP_DELTA_MASK0: DRAM 0. 0 = No mask. 1 = The error is masked.
52	RW	WR_VREF_STEP_RANGE_EDGE_MASK0: DRAM 0. 0 = No mask. 1 = The error is masked.
53	RW	WR_VREF_NO_INCREASE_MASK0: DRAM 0. 0 = No mask. 1 = The error is masked.
54	RW	WR_VREF_1D_EYE_NOISE_MASK0: DRAM 0. 0 = No mask. 1 = The error is masked.
55	RW	WR_VREF_BAD_BIT_MASK0: DRAM 0. 0 = No mask. 1 = The error is masked.
56	RW	WR_VREF_MAX_RANGE_MASK1: DRAM 1. 0 = No mask. 1 = The error is masked.
57	RW	WR_VREF_MIN_RANGE_MASK1: DRAM 1. 0 = No mask. 1 = The error is masked.
58	RW	WR_VREF_TWO_RANGE_BEST_CASE_MASK1: DRAM 1. 0 = No mask. 1 = The error is masked.

Bits	SCOM	Field Mnemonic: Description
59	RW	WR_VREF_BIT_STEP_DELTA_MASK1: DRAM 1. 0 = No mask. 1 = The error is masked.
60	RW	WR_VREF_STEP_RANGE_EDGE_MASK1: DRAM 1. 0 = No mask. 1 = The error is masked.
61	RW	WR_VREF_NO_INCREASE_MASK1: DRAM 1. 0 = No mask. 1 = The error is masked.
62	RW	WR_VREF_1D_EYE_NOISE_MASK1: DRAM 1. 0 = No mask. 1 = The error is masked.
63	RW	WR_VREF_BAD_BIT_MASK1: DRAM 1. 0 = No mask. 1 = The error is masked.

Register Name	DP16 Write VREF Error Mask 0 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_ERROR_MASK0_P2_[n]
Address	800000FB0701183F (SCOM), +0x0400_0000_0000
Description	This register provides masks for error information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	WR_VREF_MAX_RANGE_MASK0: DRAM 0. 0 = No mask. 1 = The error is masked.
49	RW	WR_VREF_MIN_RANGE_MASK0: DRAM 0. 0 = No mask. 1 = The error is masked.
50	RW	WR_VREF_TWO_RANGE_BEST_CASE_MASK0: DRAM 0. 0 = No mask. 1 = The error is masked.
51	RW	WR_VREF_BIT_STEP_DELTA_MASK0: DRAM 0. 0 = No mask. 1 = The error is masked.
52	RW	WR_VREF_STEP_RANGE_EDGE_MASK0: DRAM 0. 0 = No mask. 1 = The error is masked.
53	RW	WR_VREF_NO_INCREASE_MASK0: DRAM 0. 0 = No mask. 1 = The error is masked.
54	RW	WR_VREF_1D_EYE_NOISE_MASK0: DRAM 0. 0 = No mask. 1 = The error is masked.
55	RW	WR_VREF_BAD_BIT_MASK0: DRAM 0. 0 = No mask. 1 = The error is masked.

Bits	SCOM	Field Mnemonic: Description
56	RW	WR_VREF_MAX_RANGE_MASK1: DRAM 1. 0 = No mask. 1 = The error is masked.
57	RW	WR_VREF_MIN_RANGE_MASK1: DRAM 1. 0 = No mask. 1 = The error is masked.
58	RW	WR_VREF_TWO_RANGE_BEST_CASE_MASK1: DRAM 1. 0 = No mask. 1 = The error is masked.
59	RW	WR_VREF_BIT_STEP_DELTA_MASK1: DRAM 1. 0 = No mask. 1 = The error is masked.
60	RW	WR_VREF_STEP_RANGE_EDGE_MASK1: DRAM 1. 0 = No mask. 1 = The error is masked.
61	RW	WR_VREF_NO_INCREASE_MASK1: DRAM 1. 0 = No mask. 1 = The error is masked.
62	RW	WR_VREF_1D_EYE_NOISE_MASK1: DRAM 1. 0 = No mask. 1 = The error is masked.
63	RW	WR_VREF_BAD_BIT_MASK1: DRAM 1. 0 = No mask. 1 = The error is masked.

Register Name	**DP16 Write VREF Error Mask 0 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_ERROR_MASK0_P3_[n]
Address	800000FB07011C3F (SCOM), +0x0400_0000_0000
Description	This register provides masks for error information.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	WR_VREF_MAX_RANGE_MASK0: DRAM 0. 0 = No mask. 1 = The error is masked.
49	RW	WR_VREF_MIN_RANGE_MASK0: DRAM 0. 0 = No mask. 1 = The error is masked.
50	RW	WR_VREF_TWO_RANGE_BEST_CASE_MASK0: DRAM 0. 0 = No mask. 1 = The error is masked.
51	RW	WR_VREF_BIT_STEP_DELTA_MASK0: DRAM 0. 0 = No mask. 1 = The error is masked.
52	RW	WR_VREF_STEP_RANGE_EDGE_MASK0: DRAM 0. 0 = No mask. 1 = The error is masked.

Bits	SCOM	Field Mnemonic: Description
53	RW	WR_VREF_NO_INCREASE_MASK0: DRAM 0. 0 = No mask. 1 = The error is masked.
54	RW	WR_VREF_1D_EYE_NOISE_MASK0: DRAM 0. 0 = No mask. 1 = The error is masked.
55	RW	WR_VREF_BAD_BIT_MASK0: DRAM 0. 0 = No mask. 1 = The error is masked.
56	RW	WR_VREF_MAX_RANGE_MASK1: DRAM 1. 0 = No mask. 1 = The error is masked.
57	RW	WR_VREF_MIN_RANGE_MASK1: DRAM 1. 0 = No mask. 1 = The error is masked.
58	RW	WR_VREF_TWO_RANGE_BEST_CASE_MASK1: DRAM 1. 0 = No mask. 1 = The error is masked.
59	RW	WR_VREF_BIT_STEP_DELTA_MASK1: DRAM 1. 0 = No mask. 1 = The error is masked.
60	RW	WR_VREF_STEP_RANGE_EDGE_MASK1: DRAM 1. 0 = No mask. 1 = The error is masked.
61	RW	WR_VREF_NO_INCREASE_MASK1: DRAM 1. 0 = No mask. 1 = The error is masked.
62	RW	WR_VREF_1D_EYE_NOISE_MASK1: DRAM 1. 0 = No mask. 1 = The error is masked.
63	RW	WR_VREF_BAD_BIT_MASK1: DRAM 1. 0 = No mask. 1 = The error is masked.

Register Name	**DP16 Read Clock Enable and Selection RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_CLOCK_RANK_PAIR1_P0_[n]
Address	800001040701103F (SCOM), +0x0400_0000_0000
Description	This register configures which input pins on the DP16 are used as strobes to capture incoming data on which data pins. This register must be configured the same as the DP16 Write Clock Enable and Selection Register. The following are legal configurations on POWER9 for bits 48:53: 110000 = By-8 memory using CLK16. 000011 = By-8 memory using CLK18. 100001 = By-4 memory, not cross-coupled. 010010 = By-4 memory, cross-coupled. 000000 = Byte is not used. Other values are reserved. The following are legal configurations on POWER9 for bits 54:57: 1100 = By-8 memory using CLK20. 0011 = By-8 memory using CLK22. 1001 = By-4 memory, not cross-coupled. 0110 = By-4 memory, cross-coupled. 0000 = Byte is not used. Other values are reserved.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	QUAD0_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an incoming clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
49	RW	QUAD1_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an incoming clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
50:51	RO	Reserved.
52	RW	QUAD0_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an incoming clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n).. where n is the DP16 instance number.
53	RW	QUAD1_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an incoming clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.

Bits	SCOM	Field Mnemonic: Description
54	RW	QUAD2_CLK20: 1 = MEMINTD20B(n) and MEMINTD21B(n) are used as an incoming clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
55	RW	QUAD3_CLK20: 1 = MEMINTD20B(n) and MEMINTD21B(n) are used as an incoming clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
56	RW	QUAD2_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an incoming clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
57	RW	QUAD3_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an incoming clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
58:63	RO	Reserved.

Register Name	**DP16 Read Clock Enable and Selection RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_CLOCK_RANK_PAIR1_P1_[n]
Address	800001040701143F (SCOM), +0x0400_0000_0000
Description	This register configures which input pins on the DP16 are used as strobes to capture incoming data on which data pins. This register must be configured the same as the DP16 Write Clock Enable and Selection Register. The following are legal configurations on POWER9 for bits 48:53: 110000 = By-8 memory using CLK16. 000011 = By-8 memory using CLK18. 100001 = By-4 memory, not cross-coupled. 010010 = By-4 memory, cross-coupled. 000000 = Byte is not used. Other values are reserved. The following are legal configurations on POWER9 for bits 54:57: 1100 = By-8 memory using CLK20. 0011 = By-8 memory using CLK22. 1001 = By-4 memory, not cross-coupled. 0110 = By-4 memory, cross-coupled. 0000 = Byte is not used. Other values are reserved.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	QUAD0_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an incoming clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
49	RW	QUAD1_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an incoming clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
50:51	RO	Reserved.
52	RW	QUAD0_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an incoming clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
53	RW	QUAD1_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an incoming clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
54	RW	QUAD2_CLK20: 1 = MEMINTD20B(n) and MEMINTD21B(n) are used as an incoming clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
55	RW	QUAD3_CLK20: 1 = MEMINTD20B(n) and MEMINTD21B(n) are used as an incoming clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.

Bits	SCOM	Field Mnemonic: Description
56	RW	QUAD2_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an incoming clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
57	RW	QUAD3_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an incoming clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
58:63	RO	Reserved.

Register Name	**DP16 Read Clock Enable and Selection RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_CLOCK_RANK_PAIR1_P2_[n]
Address	800001040701183F (SCOM), +0x0400_0000_0000
Description	This register configures which input pins on the DP16 are used as strobes to capture incoming data on which data pins. This register must be configured the same as the DP16 Write Clock Enable and Selection Register. The following are legal configurations on POWER9 for bits 48:53: 110000 = By-8 memory using CLK16. 000011 = By-8 memory using CLK18. 100001 = By-4 memory, not cross-coupled. 010010 = By-4 memory, cross-coupled. 000000 = Byte is not used. Other values are reserved. The following are legal configurations on POWER9 for bits 54:57: 1100 = By-8 memory using CLK20. 0011 = By-8 memory using CLK22. 1001 = By-4 memory, not cross-coupled. 0110 = By-4 memory, cross-coupled. 0000 = Byte is not used. Other values are reserved.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	QUAD0_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an incoming clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.

Bits	SCOM	Field Mnemonic: Description
49	RW	QUAD1_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an incoming clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
50:51	RO	Reserved.
52	RW	QUAD0_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an incoming clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
53	RW	QUAD1_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an incoming clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
54	RW	QUAD2_CLK20: 1 = MEMINTD20B(n) and MEMINTD21B(n) are used as an incoming clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
55	RW	QUAD3_CLK20: 1 = MEMINTD20B(n) and MEMINTD21B(n) are used as an incoming clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
56	RW	QUAD2_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an incoming clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.

Bits	SCOM	Field Mnemonic: Description
57	RW	QUAD3_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an incoming clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
58:63	RO	Reserved.

Register Name	**DP16 Read Clock Enable and Selection RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_CLOCK_RANK_PAIR1_P3_[n]
Address	8000010407011C3F (SCOM), +0x0400_0000_0000
Description	This register configures which input pins on the DP16 are used as strobes to capture incoming data on which data pins. This register must be configured the same as the DP16 Write Clock Enable and Selection Register. The following are legal configurations on POWER9 for bits 48:53: 110000 = By-8 memory using CLK16. 000011 = By-8 memory using CLK18. 100001 = By-4 memory, not cross-coupled. 010010 = By-4 memory, cross-coupled. 000000 = Byte is not used. Other values are reserved. The following are legal configurations on POWER9 for bits 54:57: 1100 = By-8 memory using CLK20. 0011 = By-8 memory using CLK22. 1001 = By-4 memory, not cross-coupled. 0110 = By-4 memory, cross-coupled. 0000 = Byte is not used. Other values are reserved.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	QUAD0_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an incoming clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
49	RW	QUAD1_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an incoming clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
50:51	RO	Reserved.

Bits	SCOM	Field Mnemonic: Description
52	RW	QUAD0_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an incoming clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
53	RW	QUAD1_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an incoming clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
54	RW	QUAD2_CLK20: 1 = MEMINTD20B(n) and MEMINTD21B(n) are used as an incoming clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
55	RW	QUAD3_CLK20: 1 = MEMINTD20B(n) and MEMINTD21B(n) are used as an incoming clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
56	RW	QUAD2_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an incoming clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
57	RW	QUAD3_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an incoming clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
58:63	RO	Reserved.

Register Name	DP16 Write Clock Enable and Selection RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WRCLK_EN_RP1_P0_[n]
Address	800001050701103F (SCOM), +0x0400_0000_0000
Description	This register configures which output pins on the DP16 are used as clocks or strobes to capture outgoing data on which data pins. This register must be configured exactly the same as the DP16 Read Clock Enable and Selection Register. The following are legal configurations for bits 48:53: 110000 = by-8 memory using CLK16 000011 = by-8 memory using CLK18 100001 = by-4 memory, not cross-coupled 010010 = by-4 memory, cross-coupled 000000 = Byte is not used. Other values are reserved. The following are legal configurations for bits 54:57: 1100 = by-8 memory using CLK20 0011 = by-8 memory using CLK22 1001 = by-4 memory, not cross-coupled 0110 = by-4 memory, cross-coupled 0000 = Byte is not used. Other values are reserved. The same configuration should be loaded for all active ranks.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	QUAD0_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an outgoing clock to capture data on the following pins when the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
49	RW	QUAD1_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an outgoing clock to capture data on the following pins when the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
50:51	RW	Reserved.
52	RW	QUAD0_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.

Bits	SCOM	Field Mnemonic: Description
53	RW	QUAD1_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
54	RW	QUAD2_CLK20: 1 = MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
55	RW	QUAD3_CLK20: 1 = MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
56	RW	QUAD2_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
57	RW	QUAD3_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
58:63	RW	Reserved.

Register Name	DP16 Write Clock Enable and Selection RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WRCLK_EN_RP1_P1_[n]
Address	800001050701143F (SCOM), +0x0400_0000_0000
Description	This register configures which output pins on the DP16 are used as clocks or strobes to capture outgoing data on which data pins. This register must be configured exactly the same as the DP16 Read Clock Enable and Selection Register. The following are legal configurations for bits 48:53: 110000 = by-8 memory using CLK16 000011 = by-8 memory using CLK18 100001 = by-4 memory, not cross-coupled 010010 = by-4 memory, cross-coupled 000000 = Byte is not used. Other values are reserved. The following are legal configurations for bits 54:57: 1100 = by-8 memory using CLK20 0011 = by-8 memory using CLK22 1001 = by-4 memory, not cross-coupled 0110 = by-4 memory, cross-coupled 0000 = Byte is not used. Other values are reserved. The same configuration should be loaded for all active ranks.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	QUAD0_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an outgoing clock to capture data on the following pins when the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
49	RW	QUAD1_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an outgoing clock to capture data on the following pins when the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
50:51	RW	Reserved.
52	RW	QUAD0_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.

Bits	SCOM	Field Mnemonic: Description
53	RW	QUAD1_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
54	RW	QUAD2_CLK20: 1 = MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
55	RW	QUAD3_CLK20: 1 = MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
56	RW	QUAD2_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
57	RW	QUAD3_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
58:63	RW	Reserved.

Register Name	**DP16 Write Clock Enable and Selection RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_WRCLK_EN_RP1_P2_[n]
Address	800001050701183F (SCOM), +0x0400_0000_0000
Description	This register configures which output pins on the DP16 are used as clocks or strobes to capture outgoing data on which data pins. This register must be configured exactly the same as the DP16 Read Clock Enable and Selection Register. The following are legal configurations for bits 48:53: 110000 = by-8 memory using CLK16 000011 = by-8 memory using CLK18 100001 = by-4 memory, not cross-coupled 010010 = by-4 memory, cross-coupled 000000 = Byte is not used. Other values are reserved. The following are legal configurations for bits 54:57: 1100 = by-8 memory using CLK20 0011 = by-8 memory using CLK22 1001 = by-4 memory, not cross-coupled 0110 = by-4 memory, cross-coupled 0000 = Byte is not used. Other values are reserved. The same configuration should be loaded for all active ranks.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	QUAD0_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an outgoing clock to capture data on the following pins when the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
49	RW	QUAD1_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an outgoing clock to capture data on the following pins when the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
50:51	RW	Reserved.
52	RW	QUAD0_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.

Bits	SCOM	Field Mnemonic: Description
53	RW	QUAD1_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
54	RW	QUAD2_CLK20: 1 = MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
55	RW	QUAD3_CLK20: 1 = MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
56	RW	QUAD2_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
57	RW	QUAD3_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
58:63	RW	Reserved.

Register Name	**DP16 Write Clock Enable and Selection RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_WRCLK_EN_RP1_P3_[n]
Address	8000010507011C3F (SCOM), +0x0400_0000_0000
Description	This register configures which output pins on the DP16 are used as clocks or strobes to capture outgoing data on which data pins. This register must be configured exactly the same as the DP16 Read Clock Enable and Selection Register. The following are legal configurations for bits 48:53: 110000 = by-8 memory using CLK16 000011 = by-8 memory using CLK18 100001 = by-4 memory, not cross-coupled 010010 = by-4 memory, cross-coupled 000000 = Byte is not used. Other values are reserved. The following are legal configurations for bits 54:57: 1100 = by-8 memory using CLK20 0011 = by-8 memory using CLK22 1001 = by-4 memory, not cross-coupled 0110 = by-4 memory, cross-coupled 0000 = Byte is not used. Other values are reserved. The same configuration should be loaded for all active ranks.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	QUAD0_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an outgoing clock to capture data on the following pins when the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
49	RW	QUAD1_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an outgoing clock to capture data on the following pins when the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
50:51	RW	Reserved.
52	RW	QUAD0_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.

Bits	SCOM	Field Mnemonic: Description
53	RW	QUAD1_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
54	RW	QUAD2_CLK20: 1 = MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
55	RW	QUAD3_CLK20: 1 = MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
56	RW	QUAD2_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
57	RW	QUAD3_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
58:63	RW	Reserved.

Register Name	DP16 DQS Read Phase Select RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_[n]
Address	800001090701103F (SCOM), +0x0400_0000_0000
Description	This register contains a dynamic value that represents the phase differences between the memory clock, strobes, and the receiver clocks. Hardware determines these values during initial calibration and maintains them during periodic calibrations. One register stores phase selects for each rank pair for a total of four registers. This register is provided for diagnostic use. Do not use software to write to this register during normal use.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RW	DQSCLK_SELECT0: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03.
50:51	RW	RDCLK_SELECT0: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03.
52:53	RW	DQSCLK_SELECT1: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07.
54:55	RW	RDCLK_SELECT1: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07.
56:57	RW	DQSCLK_SELECT2: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11.
58:59	RW	RDCLK_SELECT2: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11.
60:61	RW	DQSCLK_SELECT3: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15.
62:63	RW	RDCLK_SELECT3: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15.

Register Name	**DP16 DQS Read Phase Select RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_[n]
Address	800001090701143F (SCOM), +0x0400_0000_0000
Description	This register contains a dynamic value that represents the phase differences between the memory clock, strobes, and the receiver clocks. Hardware determines these values during initial calibration and maintains them during periodic calibrations. One register stores phase selects for each rank pair for a total of four registers. This register is provided for diagnostic use. Do not use software to write to this register during normal use.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:49	RW	DQSCLK_SELECT0: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03.
50:51	RW	RDCLK_SELECT0: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03.
52:53	RW	DQSCLK_SELECT1: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07.
54:55	RW	RDCLK_SELECT1: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07.
56:57	RW	DQSCLK_SELECT2: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11.
58:59	RW	RDCLK_SELECT2: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11.
60:61	RW	DQSCLK_SELECT3: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15.
62:63	RW	RDCLK_SELECT3: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15.

Register Name	DP16 DQS Read Phase Select RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQS_RD_PHASE_SELECT_RANK_PAIR1_P2_[n]
Address	800001090701183F (SCOM), +0x0400_0000_0000
Description	This register contains a dynamic value that represents the phase differences between the memory clock, strobes, and the receiver clocks. Hardware determines these values during initial calibration and maintains them during periodic calibrations. One register stores phase selects for each rank pair for a total of four registers. This register is provided for diagnostic use. Do not use software to write to this register during normal use.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:49	RW	DQSCLK_SELECT0: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03.
50:51	RW	RDCLK_SELECT0: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03.
52:53	RW	DQSCLK_SELECT1: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07.
54:55	RW	RDCLK_SELECT1: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07.
56:57	RW	DQSCLK_SELECT2: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11.
58:59	RW	RDCLK_SELECT2: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11.
60:61	RW	DQSCLK_SELECT3: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15.
62:63	RW	RDCLK_SELECT3: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15.

Register Name	DP16 DQS Read Phase Select RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQS_RD_PHASE_SELECT_RANK_PAIR1_P3_[n]
Address	8000010907011C3F (SCOM), +0x0400_0000_0000
Description	This register contains a dynamic value that represents the phase differences between the memory clock, strobes, and the receiver clocks. Hardware determines these values during initial calibration and maintains them during periodic calibrations. One register stores phase selects for each rank pair for a total of four registers. This register is provided for diagnostic use. Do not use software to write to this register during normal use.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:49	RW	DQSCLK_SELECT0: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03.
50:51	RW	RDCLK_SELECT0: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03.
52:53	RW	DQSCLK_SELECT1: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07.
54:55	RW	RDCLK_SELECT1: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07.

Bits	SCOM	Field Mnemonic: Description
56:57	RW	DQSCLK_SELECT2: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11.
58:59	RW	RDCLK_SELECT2: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11.
60:61	RW	DQSCLK_SELECT3: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15.
62:63	RW	RDCLK_SELECT3: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15.

Register Name	**DP16 Read Delay Offset 0 RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY_OFFSET0_RANK_PAIR1_P0_[n]
Address	8000010C0701103F (SCOM), +0x0400_0000_0000
Description	Each register field holds the read delay offsets for four of the MEMINTDnnB pins for one rank pair in the DP16.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	OFFSET0: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03 and nn{1} = 08, 09, 10, 11. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.
56	RO	Constant = 0b0
57:63	RW	OFFSET1: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07 and nn{1} = 12, 13, 14, 15. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.

Register Name	**DP16 Read Delay Offset 0 RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY_OFFSET0_RANK_PAIR1_P1_[n]
Address	8000010C0701143F (SCOM), +0x0400_0000_0000
Description	Each register field holds the read delay offsets for four of the MEMINTDnnB pins for one rank pair in the DP16.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	OFFSET0: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03 and nn{1} = 08, 09, 10, 11. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.
56	RO	Constant = 0b0

Bits	SCOM	Field Mnemonic: Description
57:63	RW	OFFSET1: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07 and nn{1} = 12, 13, 14, 15. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.

Register Name	**DP16 Read Delay Offset 0 RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY_OFFSET0_RANK_PAIR1_P2_[n]
Address	8000010C0701183F (SCOM), +0x0400_0000_0000
Description	Each register field holds the read delay offsets for four of the MEMINTDnnB pins for one rank pair in the DP16.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	OFFSET0: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03 and nn{1} = 08, 09, 10, 11. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.
56	RO	Constant = 0b0
57:63	RW	OFFSET1: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07 and nn{1} = 12, 13, 14, 15. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.

Register Name	**DP16 Read Delay Offset 0 RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY_OFFSET0_RANK_PAIR1_P3_[n]
Address	8000010C07011C3F (SCOM), +0x0400_0000_0000
Description	Each register field holds the read delay offsets for four of the MEMINTDnnB pins for one rank pair in the DP16.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	OFFSET0: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03 and nn{1} = 08, 09, 10, 11. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.
56	RO	Constant = 0b0

Bits	SCOM	Field Mnemonic: Description
57:63	RW	OFFSET1: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07 and nn{1} = 12, 13, 14, 15. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.

Register Name	DP16 Read Delay Offset 1 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY_OFFSET1_RANK_PAIR1_P0_[n]
Address	8000010D0701103F (SCOM), +0x0400_0000_0000
Description	Each register field holds the read delay offsets for four of the MEMINTDnnB pins for one rank pair in the DP16.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	OFFSET2: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03 and nn{1} = 08, 09, 10, 11. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.
56	RO	Constant = 0b0
57:63	RW	OFFSET3: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07 and nn{1} = 12, 13, 14, 15. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.

Register Name	DP16 Read Delay Offset 1 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY_OFFSET1_RANK_PAIR1_P1_[n]
Address	8000010D0701143F (SCOM), +0x0400_0000_0000
Description	Each register field holds the read delay offsets for four of the MEMINTDnnB pins for one rank pair in the DP16.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	OFFSET2: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03 and nn{1} = 08, 09, 10, 11. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.
56	RO	Constant = 0b0

Bits	SCOM	Field Mnemonic: Description
57:63	RW	OFFSET3: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07 and nn{1} = 12, 13, 14, 15. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.

Register Name	**DP16 Read Delay Offset 1 RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY_OFFSET1_RANK_PAIR1_P2_[n]
Address	8000010D0701183F (SCOM), +0x0400_0000_0000
Description	Each register field holds the read delay offsets for four of the MEMINTDnnB pins for one rank pair in the DP16.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	OFFSET2: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03 and nn{1} = 08, 09, 10, 11. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.
56	RO	Constant = 0b0
57:63	RW	OFFSET3: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07 and nn{1} = 12, 13, 14, 15. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.

Register Name	**DP16 Read Delay Offset 1 RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY_OFFSET1_RANK_PAIR1_P3_[n]
Address	8000010D07011C3F (SCOM), +0x0400_0000_0000
Description	Each register field holds the read delay offsets for four of the MEMINTDnnB pins for one rank pair in the DP16.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	OFFSET2: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03 and nn{1} = 08, 09, 10, 11. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.
56	RO	Constant = 0b0

Bits	SCOM	Field Mnemonic: Description
57:63	RW	OFFSET3: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07 and nn{1} = 12, 13, 14, 15. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.

Register Name	**DP16 DQS Gate Delay RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQS_GATE_DELAY_RP1_P0_[n]
Address	800001130701103F (SCOM), +0x0400_0000_0000
Description	This register contains the DQS gate delay settings for each incoming read clock. One register exists for each rank pair. This register must be reset or written to its reset value before running or rerunning initial calibration.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:51	RW	DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00 - DQ03 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
52	RO	Constant = 0b0
53:55	RW	DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04 - DQ07 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
56	RO	Constant = 0b0
57:59	RW	DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08 - DQ11 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
60	RO	Constant = 0b0
61:63	RW	DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12 - DQ15 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.

Register Name	**DP16 DQS Gate Delay RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQS_GATE_DELAY_RP1_P1_[n]
Address	800001130701143F (SCOM), +0x0400_0000_0000
Description	This register contains the DQS gate delay settings for each incoming read clock. One register exists for each rank pair. This register must be reset or written to its reset value before running or rerunning initial calibration.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:51	RW	DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00 - DQ03 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
52	RO	Constant = 0b0
53:55	RW	DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04 - DQ07 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
56	RO	Constant = 0b0
57:59	RW	DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08 - DQ11 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
60	RO	Constant = 0b0
61:63	RW	DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12 - DQ15 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.

Register Name	**DP16 DQS Gate Delay RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQS_GATE_DELAY_RP1_P2_[n]
Address	800001130701183F (SCOM), +0x0400_0000_0000
Description	This register contains the DQS gate delay settings for each incoming read clock. One register exists for each rank pair. This register must be reset or written to its reset value before running or rerunning initial calibration.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:51	RW	DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00 - DQ03 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
52	RO	Constant = 0b0
53:55	RW	DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04 - DQ07 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
56	RO	Constant = 0b0
57:59	RW	DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08 - DQ11 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.

Bits	SCOM	Field Mnemonic: Description
60	RO	Constant = 0b0
61:63	RW	DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12 - DQ15 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.

Register Name	**DP16 DQS Gate Delay RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQS_GATE_DELAY_RP1_P3_[n]
Address	8000011307011C3F (SCOM), +0x0400_0000_0000
Description	This register contains the DQS gate delay settings for each incoming read clock. One register exists for each rank pair. This register must be reset or written to its reset value before running or rerunning initial calibration.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:51	RW	DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00 - DQ03 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
52	RO	Constant = 0b0
53:55	RW	DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04 - DQ07 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
56	RO	Constant = 0b0
57:59	RW	DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08 - DQ11 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
60	RO	Constant = 0b0
61:63	RW	DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12 - DQ15 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.

Register Name	**DP16 DQSClk Phase Rotator Value 0 RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQSCLK_PR0_RANK_PAIR1_P0_[n]
Address	800001300701103F (SCOM), +0x0400_0000_0000
Description	Two phase rotator values are contained within each register. Two registers exist for each rank pair. These phase rotator values are the values needed to align the internal SysClk to the incoming DQS strobe for each group of data pins.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	DQSCLK_ROT_CLK_N0: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD00B – MEMINTD03B in register 0 and MEMINTD08B – MEMINTD11B in register 1. This value is updated by hardware.
56	RO	Constant = 0b0
57:63	RW	DQSCLK_ROT_CLK_N1: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINTD15B in register 1. This value is updated by hardware.

Register Name	DP16 DQSClk Phase Rotator Value 0 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQSCLK_PR0_RANK_PAIR1_P1_[n]
Address	800001300701143F (SCOM), +0x0400_0000_0000
Description	Two phase rotator values are contained within each register. Two registers exist for each rank pair. These phase rotator values are the values needed to align the internal SysClk to the incoming DQS strobe for each group of data pins.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	DQSCLK_ROT_CLK_N0: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD00B – MEMINTD03B in register 0 and MEMINTD08B – MEMINTD11B in register 1. This value is updated by hardware.
56	RO	Constant = 0b0
57:63	RW	DQSCLK_ROT_CLK_N1: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINTD15B in register 1. This value is updated by hardware.

Register Name	DP16 DQSClk Phase Rotator Value 0 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQSCLK_PR0_RANK_PAIR1_P2_[n]
Address	800001300701183F (SCOM), +0x0400_0000_0000
Description	Two phase rotator values are contained within each register. Two registers exist for each rank pair. These phase rotator values are the values needed to align the internal SysClk to the incoming DQS strobe for each group of data pins.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	DQSCLK_ROT_CLK_N0: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD00B – MEMINTD03B in register 0 and MEMINTD08B – MEMINTD11B in register 1. This value is updated by hardware.
56	RO	Constant = 0b0
57:63	RW	DQSCLK_ROT_CLK_N1: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINTD15B in register 1. This value is updated by hardware.

Register Name	DP16 DQSClk Phase Rotator Value 0 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQSCLK_PR0_RANK_PAIR1_P3_[n]
Address	8000013007011C3F (SCOM), +0x0400_0000_0000
Description	Two phase rotator values are contained within each register. Two registers exist for each rank pair. These phase rotator values are the values needed to align the internal SysClk to the incoming DQS strobe for each group of data pins.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	DQSCLK_ROT_CLK_N0: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD00B – MEMINTD03B in register 0 and MEMINTD08B – MEMINTD11B in register 1. This value is updated by hardware.
56	RO	Constant = 0b0
57:63	RW	DQSCLK_ROT_CLK_N1: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINTD15B in register 1. This value is updated by hardware.

Register Name	DP16 DQSClk Phase Rotator Value 1 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQSCLK_PR1_RANK_PAIR1_P0_[n]
Address	800001310701103F (SCOM), +0x0400_0000_0000
Description	Two phase rotator values are contained within each register. Two registers exist for each rank pair. These phase rotator values are the values needed to align the internal SysClk to the incoming DQS strobe for each group of data pins.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	DQSCLK_ROT_CLK_N2: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD00B – MEMINTD03B in register 0 and MEMINTD08B – MEMINTD11B in register 1. This value is updated by hardware.
56	RO	Constant = 0b0
57:63	RW	DQSCLK_ROT_CLK_N3: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINTD15B in register 1. This value is updated by hardware.

Register Name	DP16 DQSClk Phase Rotator Value 1 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQSCLK_PR1_RANK_PAIR1_P1_[n]
Address	800001310701143F (SCOM), +0x0400_0000_0000
Description	Two phase rotator values are contained within each register. Two registers exist for each rank pair. These phase rotator values are the values needed to align the internal SysClk to the incoming DQS strobe for each group of data pins.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	DQSCLK_ROT_CLK_N2: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD00B – MEMINTD03B in register 0 and MEMINTD08B – MEMINTD11B in register 1. This value is updated by hardware.

Bits	SCOM	Field Mnemonic: Description
56	RO	Constant = 0b0
57:63	RW	DQSCLK_ROT_CLK_N3: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINTD15B in register 1. This value is updated by hardware.

Register Name	**DP16 DQSClk Phase Rotator Value 1 RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQSCLK_PR1_RANK_PAIR1_P2_[n]
Address	800001310701183F (SCOM), +0x0400_0000_0000
Description	Two phase rotator values are contained within each register. Two registers exist for each rank pair. These phase rotator values are the values needed to align the internal SysClk to the incoming DQS strobe for each group of data pins.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	DQSCLK_ROT_CLK_N2: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD00B – MEMINTD03B in register 0 and MEMINTD08B – MEMINTD11B in register 1. This value is updated by hardware.
56	RO	Constant = 0b0
57:63	RW	DQSCLK_ROT_CLK_N3: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINTD15B in register 1. This value is updated by hardware.

Register Name	**DP16 DQSClk Phase Rotator Value 1 RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQSCLK_PR1_RANK_PAIR1_P3_[n]
Address	8000013107011C3F (SCOM), +0x0400_0000_0000
Description	Two phase rotator values are contained within each register. Two registers exist for each rank pair. These phase rotator values are the values needed to align the internal SysClk to the incoming DQS strobe for each group of data pins.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	DQSCLK_ROT_CLK_N2: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD00B – MEMINTD03B in register 0 and MEMINTD08B – MEMINTD11B in register 1. This value is updated by hardware.
56	RO	Constant = 0b0
57:63	RW	DQSCLK_ROT_CLK_N3: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINTD15B in register 1. This value is updated by hardware.

Register Name	DP16 Write Delay Value 0 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_0_RP1_REG_P0_[n]
Address	800001380701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 0 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_0_RP1_REG_P1_[n]
Address	800001380701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 0 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_0_RP1_REG_P2_[n]
Address	800001380701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 0 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_0_RP1_REG_P3_[n]
Address	8000013807011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 1 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_1_RP1_REG_P0_[n]
Address	800001390701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 1 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_1_RP1_REG_P1_[n]
Address	800001390701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 1 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_1_RP1_REG_P2_[n]
Address	800001390701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 1 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_1_RP1_REG_P3_[n]
Address	8000013907011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 2 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_2_RP1_REG_P0_[n]
Address	8000013A0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 2 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_2_RP1_REG_P1_[n]
Address	8000013A0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 2 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_2_RP1_REG_P2_[n]
Address	8000013A0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 2 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_2_RP1_REG_P3_[n]
Address	8000013A07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 3 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_3_RP1_REG_P0_[n]
Address	8000013B0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 3 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_3_RP1_REG_P1_[n]
Address	8000013B0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 3 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_3_RP1_REG_P2_[n]
Address	8000013B0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 3 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_3_RP1_REG_P3_[n]
Address	8000013B07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 4 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_4_RP1_REG_P0_[n]
Address	8000013C0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 4 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_4_RP1_REG_P1_[n]
Address	8000013C0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	**DP16 Write Delay Value 4 RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_4_RP1_REG_P2_[n]
Address	8000013C0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	**DP16 Write Delay Value 4 RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_4_RP1_REG_P3_[n]
Address	8000013C07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 5 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_5_RP1_REG_P0_[n]
Address	8000013D0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 5 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_5_RP1_REG_P1_[n]
Address	8000013D0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 5 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_5_RP1_REG_P2_[n]
Address	8000013D0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 5 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_5_RP1_REG_P3_[n]
Address	8000013D07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 6 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_6_RP1_REG_P0_[n]
Address	8000013E0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 6 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_6_RP1_REG_P1_[n]
Address	8000013E0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 6 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_6_RP1_REG_P2_[n]
Address	8000013E0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 6 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_6_RP1_REG_P3_[n]
Address	8000013E07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 7 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_7_RP1_REG_P0_[n]
Address	8000013F0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 7 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_7_RP1_REG_P1_[n]
Address	8000013F0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 7 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_7_RP1_REG_P2_[n]
Address	8000013F0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 7 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_7_RP1_REG_P3_[n]
Address	8000013F07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 8 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_8_RP1_REG_P0_[n]
Address	800001400701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 8 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_8_RP1_REG_P1_[n]
Address	800001400701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 8 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_8_RP1_REG_P2_[n]
Address	800001400701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 8 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_8_RP1_REG_P3_[n]
Address	8000014007011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 9 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_9_RP1_REG_P0_[n]
Address	800001410701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 9 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_9_RP1_REG_P1_[n]
Address	800001410701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 9 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_9_RP1_REG_P2_[n]
Address	800001410701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 9 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_9_RP1_REG_P3_[n]
Address	8000014107011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 10 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_10_RP1_REG_P0_[n]
Address	800001420701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 10 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_10_RP1_REG_P1_[n]
Address	800001420701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 10 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_10_RP1_REG_P2_[n]
Address	800001420701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 10 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_10_RP1_REG_P3_[n]
Address	8000014207011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 11 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_11_RP1_REG_P0_[n]
Address	800001430701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 11 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_11_RP1_REG_P1_[n]
Address	800001430701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 11 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_11_RP1_REG_P2_[n]
Address	800001430701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 11 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_11_RP1_REG_P3_[n]
Address	8000014307011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 12 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_12_RP1_REG_P0_[n]
Address	800001440701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 12 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_12_RP1_REG_P1_[n]
Address	800001440701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 12 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_12_RP1_REG_P2_[n]
Address	800001440701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 12 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_12_RP1_REG_P3_[n]
Address	8000014407011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 13 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_13_RP1_REG_P0_[n]
Address	800001450701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 13 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_13_RP1_REG_P1_[n]
Address	800001450701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 13 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_13_RP1_REG_P2_[n]
Address	800001450701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 13 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_13_RP1_REG_P3_[n]
Address	8000014507011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 14 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_14_RP1_REG_P0_[n]
Address	800001460701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 14 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_14_RP1_REG_P1_[n]
Address	800001460701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 14 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_14_RP1_REG_P2_[n]
Address	800001460701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 14 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_14_RP1_REG_P3_[n]
Address	8000014607011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 15 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_15_RP1_REG_P0_[n]
Address	800001470701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 15 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_15_RP1_REG_P1_[n]
Address	800001470701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 15 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_15_RP1_REG_P2_[n]
Address	800001470701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 15 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_15_RP1_REG_P3_[n]
Address	8000014707011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 16 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_16_RP1_REG_P0_[n]
Address	800001480701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 16 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_16_RP1_REG_P1_[n]
Address	800001480701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 16 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_16_RP1_REG_P2_[n]
Address	800001480701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 16 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_16_RP1_REG_P3_[n]
Address	8000014807011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 18 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_18_RP1_REG_P0_[n]
Address	8000014A0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 18 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_18_RP1_REG_P1_[n]
Address	8000014A0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 18 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_18_RP1_REG_P2_[n]
Address	8000014A0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 18 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_18_RP1_REG_P3_[n]
Address	8000014A07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 20 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_20_RP1_REG_P0_[n]
Address	8000014C0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 20 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_20_RP1_REG_P1_[n]
Address	8000014C0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 20 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_20_RP1_REG_P2_[n]
Address	8000014C0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 20 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_20_RP1_REG_P3_[n]
Address	8000014C07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 22 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_22_RP1_REG_P0_[n]
Address	8000014E0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 22 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_22_RP1_REG_P1_[n]
Address	8000014E0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 22 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_22_RP1_REG_P2_[n]
Address	8000014E0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 22 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_22_RP1_REG_P3_[n]
Address	8000014E07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Read Delay Value 0 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY0_RANK_PAIR1_P0_[n]
Address	800001500701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 0 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY0_RANK_PAIR1_P1_[n]
Address	800001500701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.

Bits	SCOM	Field Mnemonic: Description
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 0 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY0_RANK_PAIR1_P2_[n]
Address	800001500701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 0 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY0_RANK_PAIR1_P3_[n]
Address	8000015007011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	**DP16 Read Delay Value 1 RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY1_RANK_PAIR1_P0_[n]
Address	800001510701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	**DP16 Read Delay Value 1 RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY1_RANK_PAIR1_P1_[n]
Address	800001510701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 1 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY1_RANK_PAIR1_P2_[n]
Address	800001510701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 1 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY1_RANK_PAIR1_P3_[n]
Address	8000015107011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 2 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY2_RANK_PAIR1_P0_[n]
Address	800001520701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.

Bits	SCOM	Field Mnemonic: Description
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 2 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY2_RANK_PAIR1_P1_[n]
Address	800001520701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 2 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY2_RANK_PAIR1_P2_[n]
Address	800001520701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	**DP16 Read Delay Value 2 RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY2_RANK_PAIR1_P3_[n]
Address	8000015207011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	**DP16 Read Delay Value 3 RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY3_RANK_PAIR1_P0_[n]
Address	800001530701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 3 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY3_RANK_PAIR1_P1_[n]
Address	800001530701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 3 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY3_RANK_PAIR1_P2_[n]
Address	800001530701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 3 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY3_RANK_PAIR1_P3_[n]
Address	8000015307011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.

Bits	SCOM	Field Mnemonic: Description
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 4 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY4_RANK_PAIR1_P0_[n]
Address	800001540701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 4 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY4_RANK_PAIR1_P1_[n]
Address	800001540701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	**DP16 Read Delay Value 4 RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY4_RANK_PAIR1_P2_[n]
Address	800001540701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	**DP16 Read Delay Value 4 RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY4_RANK_PAIR1_P3_[n]
Address	8000015407011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 5 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY5_RANK_PAIR1_P0_[n]
Address	800001550701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 5 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY5_RANK_PAIR1_P1_[n]
Address	800001550701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 5 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY5_RANK_PAIR1_P2_[n]
Address	800001550701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.

Bits	SCOM	Field Mnemonic: Description
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 5 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY5_RANK_PAIR1_P3_[n]
Address	8000015507011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 6 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY6_RANK_PAIR1_P0_[n]
Address	800001560701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	**DP16 Read Delay Value 6 RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY6_RANK_PAIR1_P1_[n]
Address	800001560701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	**DP16 Read Delay Value 6 RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY6_RANK_PAIR1_P2_[n]
Address	800001560701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 6 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY6_RANK_PAIR1_P3_[n]
Address	8000015607011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 7 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY7_RANK_PAIR1_P0_[n]
Address	800001570701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 7 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY7_RANK_PAIR1_P1_[n]
Address	800001570701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.

Bits	SCOM	Field Mnemonic: Description
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 7 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY7_RANK_PAIR1_P2_[n]
Address	800001570701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 7 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY7_RANK_PAIR1_P3_[n]
Address	8000015707011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	**DP16 Initial DQS Alignment 0 RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN0_RANK_PAIR1_P0_[n]
Address	8000015C0701103F (SCOM), +0x0400_0000_0000
Description	These registers hold the DQSClk phase rotator values computed by initial calibration, They are updated at multiple times during the calibration. Periodic DQS alignment uses the values to compare against for determining long-term drift.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RO	INITIAL_DQS_ROT_N0: This field holds the initial DQSClk rotator value for pins MEMINTD00B - MEMINTD03B in register 0 and MEMINTD08B - MEMINGTD11B in register 1. This value is updated by hardware.
56	RO	Reserved.
57:63	RO	INITIAL_DQS_ROT_N1: This field holds the initial DQSClk rotator value for pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINGTD15B in register 1.This value is updated by hardware.

Register Name	**DP16 Initial DQS Alignment 0 RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN0_RANK_PAIR1_P1_[n]
Address	8000015C0701143F (SCOM), +0x0400_0000_0000
Description	These registers hold the DQSClk phase rotator values computed by initial calibration, They are updated at multiple times during the calibration. Periodic DQS alignment uses the values to compare against for determining long-term drift.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RO	INITIAL_DQS_ROT_N0: This field holds the initial DQSClk rotator value for pins MEMINTD00B - MEMINTD03B in register 0 and MEMINTD08B - MEMINGTD11B in register 1. This value is updated by hardware.
56	RO	Reserved.
57:63	RO	INITIAL_DQS_ROT_N1: This field holds the initial DQSClk rotator value for pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINGTD15B in register 1.This value is updated by hardware.

Register Name	DP16 Initial DQS Alignment 0 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN0_RANK_PAIR1_P2_[n]
Address	8000015C0701183F (SCOM), +0x0400_0000_0000
Description	These registers hold the DQSClk phase rotator values computed by initial calibration, They are updated at multiple times during the calibration. Periodic DQS alignment uses the values to compare against for determining long-term drift.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RO	INITIAL_DQS_ROT_N0: This field holds the initial DQSClk rotator value for pins MEMINTD00B - MEMINTD03B in register 0 and MEMINTD08B - MEMINGTD11B in register 1. This value is updated by hardware.
56	RO	Reserved.
57:63	RO	INITIAL_DQS_ROT_N1: This field holds the initial DQSClk rotator value for pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINGTD15B in register 1.This value is updated by hardware.

Register Name	DP16 Initial DQS Alignment 0 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN0_RANK_PAIR1_P3_[n]
Address	8000015C07011C3F (SCOM), +0x0400_0000_0000
Description	These registers hold the DQSClk phase rotator values computed by initial calibration, They are updated at multiple times during the calibration. Periodic DQS alignment uses the values to compare against for determining long-term drift.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RO	INITIAL_DQS_ROT_N0: This field holds the initial DQSClk rotator value for pins MEMINTD00B - MEMINTD03B in register 0 and MEMINTD08B - MEMINGTD11B in register 1. This value is updated by hardware.
56	RO	Reserved.
57:63	RO	INITIAL_DQS_ROT_N1: This field holds the initial DQSClk rotator value for pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINGTD15B in register 1.This value is updated by hardware.

Register Name	DP16 Initial DQS Alignment 1 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN1_RANK_PAIR1_P0_[n]
Address	8000015D0701103F (SCOM), +0x0400_0000_0000
Description	These registers hold the DQSClk phase rotator values computed by initial calibration, They are updated at multiple times during the calibration. Periodic DQS alignment uses the values to compare against for determining long-term drift.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RO	INITIAL_DQS_ROT_N2: This field holds the initial DQSClk rotator value for pins MEMINTD00B - MEMINTD03B in register 0 and MEMINTD08B - MEMINGTD11B in register 1. This value is updated by hardware.

Bits	SCOM	Field Mnemonic: Description
56	RO	Constant = 0b0
57:63	RO	INITIAL_DQS_ROT_N3: This field holds the initial DQSClk rotator value for pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINGTD15B in register 1.This value is updated by hardware.

Register Name	DP16 Initial DQS Alignment 1 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN1_RANK_PAIR1_P1_[n]
Address	8000015D0701143F (SCOM), +0x0400_0000_0000
Description	These registers hold the DQSClk phase rotator values computed by initial calibration, They are updated at multiple times during the calibration. Periodic DQS alignment uses the values to compare against for determining long-term drift.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RO	INITIAL_DQS_ROT_N2: This field holds the initial DQSClk rotator value for pins MEMINTD00B - MEMINTD03B in register 0 and MEMINTD08B - MEMINGTD11B in register 1. This value is updated by hardware.
56	RO	Constant = 0b0
57:63	RO	INITIAL_DQS_ROT_N3: This field holds the initial DQSClk rotator value for pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINGTD15B in register 1.This value is updated by hardware.

Register Name	DP16 Initial DQS Alignment 1 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN1_RANK_PAIR1_P2_[n]
Address	8000015D0701183F (SCOM), +0x0400_0000_0000
Description	These registers hold the DQSClk phase rotator values computed by initial calibration, They are updated at multiple times during the calibration. Periodic DQS alignment uses the values to compare against for determining long-term drift.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RO	INITIAL_DQS_ROT_N2: This field holds the initial DQSClk rotator value for pins MEMINTD00B - MEMINTD03B in register 0 and MEMINTD08B - MEMINGTD11B in register 1. This value is updated by hardware.
56	RO	Constant = 0b0
57:63	RO	INITIAL_DQS_ROT_N3: This field holds the initial DQSClk rotator value for pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINGTD15B in register 1.This value is updated by hardware.

Register Name	DP16 Initial DQS Alignment 1 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN1_RANK_PAIR1_P3_[n]
Address	8000015D07011C3F (SCOM), +0x0400_0000_0000
Description	These registers hold the DQSClk phase rotator values computed by initial calibration, They are updated at multiple times during the calibration. Periodic DQS alignment uses the values to compare against for determining long-term drift.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RO	INITIAL_DQS_ROT_N2: This field holds the initial DQSClk rotator value for pins MEMINTD00B - MEMINTD03B in register 0 and MEMINTD08B - MEMINGTD11B in register 1. This value is updated by hardware.
56	RO	Constant = 0b0
57:63	RO	INITIAL_DQS_ROT_N3: This field holds the initial DQSClk rotator value for pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINGTD15B in register 1.This value is updated by hardware.

Register Name	DP16 Write VREF Value 0 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_VALUE0_RANK_PAIR1_P0_[n]
Address	8000015E0701103F (SCOM), +0x0400_0000_0000
Description	This register contains the starting and ending values of calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48	RW	Reserved.
49	RWX	WR_VREF_RANGE_DRAM0: This bit contains the default and current value of the DRAM WR VREF range for DRAM0 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
50:55	RWX	WR_VREF_VALUE_DRAM0: This field contains the default and current value of the DRAM WR VREF value for DRAM0 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
56	RW	Reserved.
57	RWX	WR_VREF_RANGE_DRAM1: This bit contains the default and current value of the DRAM WR VREF range for DRAM1 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
58:63	RWX	WR_VREF_VALUE_DRAM1: This field contains the default and current value of the DRAM WR VREF value for DRAM1 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.

Register Name	DP16 Write VREF Value 0 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_VALUE0_RANK_PAIR1_P1_[n]
Address	8000015E0701143F (SCOM), +0x0400_0000_0000
Description	This register contains the starting and ending values of calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49	RWX	WR_VREF_RANGE_DRAM0: This bit contains the default and current value of the DRAM WR VREF range for DRAM0 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
50:55	RWX	WR_VREF_VALUE_DRAM0: This field contains the default and current value of the DRAM WR VREF value for DRAM0 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
56	RW	Reserved.
57	RWX	WR_VREF_RANGE_DRAM1: This bit contains the default and current value of the DRAM WR VREF range for DRAM1 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
58:63	RWX	WR_VREF_VALUE_DRAM1: This field contains the default and current value of the DRAM WR VREF value for DRAM1 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.

Register Name	DP16 Write VREF Value 0 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_VALUE0_RANK_PAIR1_P2_[n]
Address	8000015E0701183F (SCOM), +0x0400_0000_0000
Description	This register contains the starting and ending values of calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49	RWX	WR_VREF_RANGE_DRAM0: This bit contains the default and current value of the DRAM WR VREF range for DRAM0 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
50:55	RWX	WR_VREF_VALUE_DRAM0: This field contains the default and current value of the DRAM WR VREF value for DRAM0 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
56	RW	Reserved.
57	RWX	WR_VREF_RANGE_DRAM1: This bit contains the default and current value of the DRAM WR VREF range for DRAM1 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	WR_VREF_VALUE_DRAM1: This field contains the default and current value of the DRAM WR VREF value for DRAM1 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.

Register Name	**DP16 Write VREF Value 0 RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_VALUE0_RANK_PAIR1_P3_[n]
Address	8000015E07011C3F (SCOM), +0x0400_0000_0000
Description	This register contains the starting and ending values of calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49	RWX	WR_VREF_RANGE_DRAM0: This bit contains the default and current value of the DRAM WR VREF range for DRAM0 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
50:55	RWX	WR_VREF_VALUE_DRAM0: This field contains the default and current value of the DRAM WR VREF value for DRAM0 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
56	RW	Reserved.
57	RWX	WR_VREF_RANGE_DRAM1: This bit contains the default and current value of the DRAM WR VREF range for DRAM1 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
58:63	RWX	WR_VREF_VALUE_DRAM1: This field contains the default and current value of the DRAM WR VREF value for DRAM1 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.

Register Name	**DP16 Write VREF Value 1 RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_VALUE1_RANK_PAIR1_P0_[n]
Address	8000015F0701103F (SCOM), +0x0400_0000_0000
Description	This register contains the starting and ending values of calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49	RWX	WR_VREF_RANGE_DRAM2: This bit contains the default and current value of the DRAM WR VREF range for DRAM2 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	WR_VREF_VALUE_DRAM2: This bit contains the default and current value of the DRAM WR VREF value for DRAM2 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
56	RW	Reserved.
57	RWX	WR_VREF_RANGE_DRAM3: This bit contains the default and current value of the DRAM WR VREF range for DRAM3 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
58:63	RWX	WR_VREF_VALUE_DRAM3: This bit contains the default and current value of the DRAM WR VREF value for DRAM3 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.

Register Name	**DP16 Write VREF Value 1 RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_VALUE1_RANK_PAIR1_P1_[n]
Address	8000015F0701143F (SCOM), +0x0400_0000_0000
Description	This register contains the starting and ending values of calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48	RW	Reserved.
49	RWX	WR_VREF_RANGE_DRAM2: This bit contains the default and current value of the DRAM WR VREF range for DRAM2 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
50:55	RWX	WR_VREF_VALUE_DRAM2: This bit contains the default and current value of the DRAM WR VREF value for DRAM2 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
56	RW	Reserved.
57	RWX	WR_VREF_RANGE_DRAM3: This bit contains the default and current value of the DRAM WR VREF range for DRAM3 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
58:63	RWX	WR_VREF_VALUE_DRAM3: This bit contains the default and current value of the DRAM WR VREF value for DRAM3 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.

Register Name	**DP16 Write VREF Value 1 RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_VALUE1_RANK_PAIR1_P2_[n]
Address	8000015F0701183F (SCOM), +0x0400_0000_0000
Description	This register contains the starting and ending values of calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49	RWX	WR_VREF_RANGE_DRAM2: This bit contains the default and current value of the DRAM WR VREF range for DRAM2 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
50:55	RWX	WR_VREF_VALUE_DRAM2: This bit contains the default and current value of the DRAM WR VREF value for DRAM2 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
56	RW	Reserved.
57	RWX	WR_VREF_RANGE_DRAM3: This bit contains the default and current value of the DRAM WR VREF range for DRAM3 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
58:63	RWX	WR_VREF_VALUE_DRAM3: This bit contains the default and current value of the DRAM WR VREF value for DRAM3 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.

Register Name	**DP16 Write VREF Value 1 RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_VALUE1_RANK_PAIR1_P3_[n]
Address	8000015F07011C3F (SCOM), +0x0400_0000_0000
Description	This register contains the starting and ending values of calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49	RWX	WR_VREF_RANGE_DRAM2: This bit contains the default and current value of the DRAM WR VREF range for DRAM2 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
50:55	RWX	WR_VREF_VALUE_DRAM2: This bit contains the default and current value of the DRAM WR VREF value for DRAM2 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
56	RW	Reserved.
57	RWX	WR_VREF_RANGE_DRAM3: This bit contains the default and current value of the DRAM WR VREF range for DRAM3 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
58:63	RWX	WR_VREF_VALUE_DRAM3: This bit contains the default and current value of the DRAM WR VREF value for DRAM3 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.

Register Name	DP16 Read Eye Size 0 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE0_RANK_PAIR1_P0_[n]
Address	800001600701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 0 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE0_RANK_PAIR1_P1_[n]
Address	800001600701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	**DP16 Read Eye Size 0 RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE0_RANK_PAIR1_P2_[n]
Address	800001600701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	**DP16 Read Eye Size 0 RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE0_RANK_PAIR1_P3_[n]
Address	8000016007011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 1 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE1_RANK_PAIR1_P0_[n]
Address	800001610701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 1 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE1_RANK_PAIR1_P1_[n]
Address	800001610701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 1 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE1_RANK_PAIR1_P2_[n]
Address	800001610701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 1 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE1_RANK_PAIR1_P3_[n]
Address	8000016107011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 2 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE2_RANK_PAIR1_P0_[n]
Address	800001620701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 2 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE2_RANK_PAIR1_P1_[n]
Address	800001620701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 2 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE2_RANK_PAIR1_P2_[n]
Address	800001620701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 2 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE2_RANK_PAIR1_P3_[n]
Address	8000016207011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 3 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE3_RANK_PAIR1_P0_[n]
Address	800001630701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 3 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE3_RANK_PAIR1_P1_[n]
Address	800001630701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 3 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE3_RANK_PAIR1_P2_[n]
Address	800001630701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 3 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE3_RANK_PAIR1_P3_[n]
Address	8000016307011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 4 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE4_RANK_PAIR1_P0_[n]
Address	800001640701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 4 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE4_RANK_PAIR1_P1_[n]
Address	800001640701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 4 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE4_RANK_PAIR1_P2_[n]
Address	800001640701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 4 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE4_RANK_PAIR1_P3_[n]
Address	8000016407011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 5 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE5_RANK_PAIR1_P0_[n]
Address	800001650701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 5 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE5_RANK_PAIR1_P1_[n]
Address	800001650701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	**DP16 Read Eye Size 5 RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE5_RANK_PAIR1_P2_[n]
Address	800001650701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	**DP16 Read Eye Size 5 RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE5_RANK_PAIR1_P3_[n]
Address	8000016507011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 6 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE6_RANK_PAIR1_P0_[n]
Address	800001660701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 6 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE6_RANK_PAIR1_P1_[n]
Address	800001660701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	**DP16 Read Eye Size 6 RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE6_RANK_PAIR1_P2_[n]
Address	800001660701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	**DP16 Read Eye Size 6 RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE6_RANK_PAIR1_P3_[n]
Address	8000016607011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 7 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE7_RANK_PAIR1_P0_[n]
Address	800001670701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 7 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE7_RANK_PAIR1_P1_[n]
Address	800001670701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 7 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE7_RANK_PAIR1_P2_[n]
Address	800001670701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 7 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE7_RANK_PAIR1_P3_[n]
Address	8000016707011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 8 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE8_RANK_PAIR1_P0_[n]
Address	800001680701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 8 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE8_RANK_PAIR1_P1_[n]
Address	800001680701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 8 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE8_RANK_PAIR1_P2_[n]
Address	800001680701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 8 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE8_RANK_PAIR1_P3_[n]
Address	8000016807011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 9 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE9_RANK_PAIR1_P0_[n]
Address	800001690701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 9 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE9_RANK_PAIR1_P1_[n]
Address	800001690701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	**DP16 Read Eye Size 9 RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE9_RANK_PAIR1_P2_[n]
Address	800001690701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	**DP16 Read Eye Size 9 RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE9_RANK_PAIR1_P3_[n]
Address	8000016907011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 10 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE10_RANK_PAIR1_P0_[n]
Address	8000016A0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 10 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE10_RANK_PAIR1_P1_[n]
Address	8000016A0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 10 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE10_RANK_PAIR1_P2_[n]
Address	8000016A0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 10 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE10_RANK_PAIR1_P3_[n]
Address	8000016A07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 11 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE11_RANK_PAIR1_P0_[n]
Address	8000016B0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 11 RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE11_RANK_PAIR1_P1_[n]
Address	8000016B0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	**DP16 Read Eye Size 11 RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE11_RANK_PAIR1_P2_[n]
Address	8000016B0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	**DP16 Read Eye Size 11 RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE11_RANK_PAIR1_P3_[n]
Address	8000016B07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 DQ Bit Disable RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQ_BIT_DISABLE_RP1_P0_[n]
Address	8000017C0701103F (SCOM), +0x0400_0000_0000
Description	This register is used to disable each of the 16 pins on the DP16. During calibration operations, the hardware sets the bit in this register that corresponds to a pin on the DP16 that failed a calibration step. This register indicates which DQ pins on the DP16 failed a calibration step. This register does not indicate which calibration step failed.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DQ_BIT_DISABLE_0_15: 1 = Indicates that the DP16 bit is disabled and does not participate in any calibration steps. 0 = Indicates that the DP16 bit is not disabled. Bit 48 controls MEMINTD00B(n). Bit 49 controls MEMINTD01B(n). Bit 50 controls MEMINTD02B(n). ... Bit 63 controls MEMINTD15B(n). where n is the DP16 instance number.

Register Name	DP16 DQ Bit Disable RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQ_BIT_DISABLE_RP1_P1_[n]
Address	8000017C0701143F (SCOM), +0x0400_0000_0000
Description	This register is used to disable each of the 16 pins on the DP16. During calibration operations, the hardware sets the bit in this register that corresponds to a pin on the DP16 that failed a calibration step. This register indicates which DQ pins on the DP16 failed a calibration step. This register does not indicate which calibration step failed.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DQ_BIT_DISABLE_0_15: 1 = Indicates that the DP16 bit is disabled and does not participate in any calibration steps. 0 = Indicates that the DP16 bit is not disabled. Bit 48 controls MEMINTD00B(n). Bit 49 controls MEMINTD01B(n). Bit 50 controls MEMINTD02B(n). ... Bit 63 controls MEMINTD15B(n). where n is the DP16 instance number.

Register Name	DP16 DQ Bit Disable RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQ_BIT_DISABLE_RP1_P2_[n]
Address	8000017C0701183F (SCOM), +0x0400_0000_0000
Description	This register is used to disable each of the 16 pins on the DP16. During calibration operations, the hardware sets the bit in this register that corresponds to a pin on the DP16 that failed a calibration step. This register indicates which DQ pins on the DP16 failed a calibration step. This register does not indicate which calibration step failed.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	DQ_BIT_DISABLE_0_15: 1 = Indicates that the DP16 bit is disabled and does not participate in any calibration steps. 0 = Indicates that the DP16 bit is not disabled. Bit 48 controls MEMINTD00B(n). Bit 49 controls MEMINTD01B(n). Bit 50 controls MEMINTD02B(n). ... Bit 63 controls MEMINTD15B(n). where n is the DP16 instance number.

Register Name	**DP16 DQ Bit Disable RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQ_BIT_DISABLE_RP1_P3_[n]
Address	8000017C07011C3F (SCOM), +0x0400_0000_0000
Description	This register is used to disable each of the 16 pins on the DP16. During calibration operations, the hardware sets the bit in this register that corresponds to a pin on the DP16 that failed a calibration step. This register indicates which DQ pins on the DP16 failed a calibration step. This register does not indicate which calibration step failed.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	DQ_BIT_DISABLE_0_15: 1 = Indicates that the DP16 bit is disabled and does not participate in any calibration steps. 0 = Indicates that the DP16 bit is not disabled. Bit 48 controls MEMINTD00B(n). Bit 49 controls MEMINTD01B(n). Bit 50 controls MEMINTD02B(n). ... Bit 63 controls MEMINTD15B(n). where n is the DP16 instance number.

Register Name	**DP16 DQS Bit Disable RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQS_BIT_DISABLE_RP1_P0_[n]
Address	8000017D0701103F (SCOM), +0x0400_0000_0000
Description	This register is used to disable each of the eight DQS pins on the DP16. During calibration operations, the hardware sets the bit in this register that corresponds to a pin on the DP16 that failed a calibration step. This register indicates which DQS pins on the DP16 failed a calibration step. This register does not indicate which calibration step failed.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DQS_BIT_DISABLE_16_23: Bits are grouped in pairs. Bits 48:49, 50:51, 52:53, and 54:55 correspond to the differential DQS bits for each pair. 1 = Indicates that the DQS bits are disabled and do not participate in any calibration steps. Both DQS bits in the pair are set to 1b. 0 = Indicates that the DQS bits are not disabled. Both DQS bits in the pair are set to 0b. Bits 48:49 indicate the disable state of the DQS associated with QUAD0, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 50:51 indicate the disable state of the DQS associated with QUAD1, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 52:53 indicate the disable state of the DQS associated with QUAD2, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 54:55 indicate the disable state of the DQS associated with QUAD3, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register.
56:63	RO	Constant = 0b00000000

Register Name	**DP16 DQS Bit Disable RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQS_BIT_DISABLE_RP1_P1_[n]
Address	8000017D0701143F (SCOM), +0x0400_0000_0000
Description	This register is used to disable each of the eight DQS pins on the DP16. During calibration operations, the hardware sets the bit in this register that corresponds to a pin on the DP16 that failed a calibration step. This register indicates which DQS pins on the DP16 failed a calibration step. This register does not indicate which calibration step failed.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:55	RW	DQS_BIT_DISABLE_16_23: Bits are grouped in pairs. Bits 48:49, 50:51, 52:53, and 54:55 correspond to the differential DQS bits for each pair. 1 = Indicates that the DQS bits are disabled and do not participate in any calibration steps. Both DQS bits in the pair are set to 1b. 0 = Indicates that the DQS bits are not disabled. Both DQS bits in the pair are set to 0b. Bits 48:49 indicate the disable state of the DQS associated with QUAD0, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 50:51 indicate the disable state of the DQS associated with QUAD1, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 52:53 indicate the disable state of the DQS associated with QUAD2, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 54:55 indicate the disable state of the DQS associated with QUAD3, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register.
56:63	RO	Constant = 0b00000000

Register Name	DP16 DQS Bit Disable RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQS_BIT_DISABLE_RP1_P2_[n]
Address	8000017D0701183F (SCOM), +0x0400_0000_0000
Description	This register is used to disable each of the eight DQS pins on the DP16. During calibration operations, the hardware sets the bit in this register that corresponds to a pin on the DP16 that failed a calibration step. This register indicates which DQS pins on the DP16 failed a calibration step. This register does not indicate which calibration step failed.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:55	RW	DQS_BIT_DISABLE_16_23: Bits are grouped in pairs. Bits 48:49, 50:51, 52:53, and 54:55 correspond to the differential DQS bits for each pair. 1 = Indicates that the DQS bits are disabled and do not participate in any calibration steps. Both DQS bits in the pair are set to 1b. 0 = Indicates that the DQS bits are not disabled. Both DQS bits in the pair are set to 0b. Bits 48:49 indicate the disable state of the DQS associated with QUAD0, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 50:51 indicate the disable state of the DQS associated with QUAD1, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 52:53 indicate the disable state of the DQS associated with QUAD2, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 54:55 indicate the disable state of the DQS associated with QUAD3, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register.
56:63	RO	Constant = 0b00000000

Register Name	DP16 DQS Bit Disable RP1 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQS_BIT_DISABLE_RP1_P3_[n]
Address	8000017D07011C3F (SCOM), +0x0400_0000_0000
Description	This register is used to disable each of the eight DQS pins on the DP16. During calibration operations, the hardware sets the bit in this register that corresponds to a pin on the DP16 that failed a calibration step. This register indicates which DQS pins on the DP16 failed a calibration step. This register does not indicate which calibration step failed.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DQS_BIT_DISABLE_16_23: Bits are grouped in pairs. Bits 48:49, 50:51, 52:53, and 54:55 correspond to the differential DQS bits for each pair. 1 = Indicates that the DQS bits are disabled and do not participate in any calibration steps. Both DQS bits in the pair are set to 1b. 0 = Indicates that the DQS bits are not disabled. Both DQS bits in the pair are set to 0b. Bits 48:49 indicate the disable state of the DQS associated with QUAD0, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 50:51 indicate the disable state of the DQS associated with QUAD1, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 52:53 indicate the disable state of the DQS associated with QUAD2, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 54:55 indicate the disable state of the DQS associated with QUAD3, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register.
56:63	RO	Constant = 0b00000000

Register Name	**DP16 Write DQ Offset Value RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQ_WR_OFFSET_RP1_P0_[n]
Address	8000017E0701103F (SCOM), +0x0400_0000_0000
Description	This register contains an offset value for each quadrant. This offset allows the centered write data bits in each quadrant to be offset from the center as determined by the write-centering calibration algorithm. This register is used by the write-centering calibration state machine. This register must be configured, if needed, before the write-centering calibration algorithm is initiated. Changing the value of this register without running the write-centering calibration algorithm has no effect on the data bit write delay values.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	DQ_WR_OFFSET_N0: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). The least-significant bit of the 5-bit value is always 0b.
52:55	RW	DQ_WR_OFFSET_N1: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). The least-significant bit of the 5-bit value is always 0b.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	DQ_WR_OFFSET_N2: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). The least-significant bit of the 5-bit value is always 0b.
60:63	RW	DQ_WR_OFFSET_N3: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). The least-significant bit of the 5-bit value is always 0b.

Register Name	**DP16 Write DQ Offset Value RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQ_WR_OFFSET_RP1_P1_[n]
Address	8000017E0701143F (SCOM), +0x0400_0000_0000
Description	This register contains an offset value for each quadrant. This offset allows the centered write data bits in each quadrant to be offset from the center as determined by the write-centering calibration algorithm. This register is used by the write-centering calibration state machine. This register must be configured, if needed, before the write-centering calibration algorithm is initiated. Changing the value of this register without running the write-centering calibration algorithm has no effect on the data bit write delay values.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	DQ_WR_OFFSET_N0: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). The least-significant bit of the 5-bit value is always 0b.
52:55	RW	DQ_WR_OFFSET_N1: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). The least-significant bit of the 5-bit value is always 0b.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	DQ_WR_OFFSET_N2: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). The least-significant bit of the 5-bit value is always 0b.
60:63	RW	DQ_WR_OFFSET_N3: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). The least-significant bit of the 5-bit value is always 0b.

Register Name	**DP16 Write DQ Offset Value RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQ_WR_OFFSET_RP1_P2_[n]
Address	8000017E0701183F (SCOM), +0x0400_0000_0000
Description	This register contains an offset value for each quadrant. This offset allows the centered write data bits in each quadrant to be offset from the center as determined by the write-centering calibration algorithm. This register is used by the write-centering calibration state machine. This register must be configured, if needed, before the write-centering calibration algorithm is initiated. Changing the value of this register without running the write-centering calibration algorithm has no effect on the data bit write delay values.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	DQ_WR_OFFSET_N0: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). The least-significant bit of the 5-bit value is always 0b.
52:55	RW	DQ_WR_OFFSET_N1: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). The least-significant bit of the 5-bit value is always 0b.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	DQ_WR_OFFSET_N2: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). The least-significant bit of the 5-bit value is always 0b.
60:63	RW	DQ_WR_OFFSET_N3: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). The least-significant bit of the 5-bit value is always 0b.

Register Name	**DP16 Write DQ Offset Value RP1 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQ_WR_OFFSET_RP1_P3_[n]
Address	8000017E07011C3F (SCOM), +0x0400_0000_0000
Description	This register contains an offset value for each quadrant. This offset allows the centered write data bits in each quadrant to be offset from the center as determined by the write-centering calibration algorithm. This register is used by the write-centering calibration state machine. This register must be configured, if needed, before the write-centering calibration algorithm is initiated. Changing the value of this register without running the write-centering calibration algorithm has no effect on the data bit write delay values.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	DQ_WR_OFFSET_N0: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). The least-significant bit of the 5-bit value is always 0b.
52:55	RW	DQ_WR_OFFSET_N1: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). The least-significant bit of the 5-bit value is always 0b.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	DQ_WR_OFFSET_N2: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). The least-significant bit of the 5-bit value is always 0b.
60:63	RW	DQ_WR_OFFSET_N3: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). The least-significant bit of the 5-bit value is always 0b.

Register Name	DP16 Read Clock Enable and Selection RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_CLOCK_RANK_PAIR2_P0_[n]
Address	800002040701103F (SCOM), +0x0400_0000_0000
Description	This register configures which input pins on the DP16 are used as strobes to capture incoming data on which data pins. This register must be configured the same as the DP16 Write Clock Enable and Selection Register. The following are legal configurations on POWER9 for bits 48:53: 110000 = By-8 memory using CLK16. 000011 = By-8 memory using CLK18. 100001 = By-4 memory, not cross-coupled. 010010 = By-4 memory, cross-coupled. 000000 = Byte is not used. Other values are reserved. The following are legal configurations on POWER9 for bits 54:57: 1100 = By-8 memory using CLK20. 0011 = By-8 memory using CLK22. 1001 = By-4 memory, not cross-coupled. 0110 = By-4 memory, cross-coupled. 0000 = Byte is not used. Other values are reserved.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	QUAD0_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an incoming clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.

Bits	SCOM	Field Mnemonic: Description
49	RW	QUAD1_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an incoming clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
50:51	RO	Reserved.
52	RW	QUAD0_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an incoming clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
53	RW	QUAD1_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an incoming clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
54	RW	QUAD2_CLK20: 1 = MEMINTD20B(n) and MEMINTD21B(n) are used as an incoming clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
55	RW	QUAD3_CLK20: 1 = MEMINTD20B(n) and MEMINTD21B(n) are used as an incoming clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
56	RW	QUAD2_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an incoming clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.

Bits	SCOM	Field Mnemonic: Description
57	RW	QUAD3_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an incoming clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
58:63	RO	Reserved.

Register Name	**DP16 Read Clock Enable and Selection RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_CLOCK_RANK_PAIR2_P1_[n]
Address	800002040701143F (SCOM), +0x0400_0000_0000
Description	This register configures which input pins on the DP16 are used as strobes to capture incoming data on which data pins. This register must be configured the same as the DP16 Write Clock Enable and Selection Register. The following are legal configurations on POWER9 for bits 48:53: 110000 = By-8 memory using CLK16. 000011 = By-8 memory using CLK18. 100001 = By-4 memory, not cross-coupled. 010010 = By-4 memory, cross-coupled. 000000 = Byte is not used. Other values are reserved. The following are legal configurations on POWER9 for bits 54:57: 1100 = By-8 memory using CLK20. 0011 = By-8 memory using CLK22. 1001 = By-4 memory, not cross-coupled. 0110 = By-4 memory, cross-coupled. 0000 = Byte is not used. Other values are reserved.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	QUAD0_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an incoming clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
49	RW	QUAD1_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an incoming clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
50:51	RO	Reserved.

Bits	SCOM	Field Mnemonic: Description
52	RW	QUAD0_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an incoming clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
53	RW	QUAD1_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an incoming clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
54	RW	QUAD2_CLK20: 1 = MEMINTD20B(n) and MEMINTD21B(n) are used as an incoming clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
55	RW	QUAD3_CLK20: 1 = MEMINTD20B(n) and MEMINTD21B(n) are used as an incoming clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
56	RW	QUAD2_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an incoming clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
57	RW	QUAD3_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an incoming clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
58:63	RO	Reserved.

Register Name	**DP16 Read Clock Enable and Selection RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_CLOCK_RANK_PAIR2_P2_[n]
Address	800002040701183F (SCOM), +0x0400_0000_0000
Description	This register configures which input pins on the DP16 are used as strobes to capture incoming data on which data pins. This register must be configured the same as the DP16 Write Clock Enable and Selection Register. The following are legal configurations on POWER9 for bits 48:53: 110000 = By-8 memory using CLK16. 000011 = By-8 memory using CLK18. 100001 = By-4 memory, not cross-coupled. 010010 = By-4 memory, cross-coupled. 000000 = Byte is not used. Other values are reserved. The following are legal configurations on POWER9 for bits 54:57: 1100 = By-8 memory using CLK20. 0011 = By-8 memory using CLK22. 1001 = By-4 memory, not cross-coupled. 0110 = By-4 memory, cross-coupled. 0000 = Byte is not used. Other values are reserved.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	QUAD0_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an incoming clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
49	RW	QUAD1_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an incoming clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
50:51	RO	Reserved.
52	RW	QUAD0_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an incoming clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
53	RW	QUAD1_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an incoming clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.

Bits	SCOM	Field Mnemonic: Description
54	RW	QUAD2_CLK20: 1 = MEMINTD20B(n) and MEMINTD21B(n) are used as an incoming clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
55	RW	QUAD3_CLK20: 1 = MEMINTD20B(n) and MEMINTD21B(n) are used as an incoming clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
56	RW	QUAD2_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an incoming clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
57	RW	QUAD3_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an incoming clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
58:63	RO	Reserved.

Register Name	**DP16 Read Clock Enable and Selection RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_CLOCK_RANK_PAIR2_P3_[n]
Address	8000020407011C3F (SCOM), +0x0400_0000_0000
Description	This register configures which input pins on the DP16 are used as strobes to capture incoming data on which data pins. This register must be configured the same as the DP16 Write Clock Enable and Selection Register. The following are legal configurations on POWER9 for bits 48:53: 110000 = By-8 memory using CLK16. 000011 = By-8 memory using CLK18. 100001 = By-4 memory, not cross-coupled. 010010 = By-4 memory, cross-coupled. 000000 = Byte is not used. Other values are reserved. The following are legal configurations on POWER9 for bits 54:57: 1100 = By-8 memory using CLK20. 0011 = By-8 memory using CLK22. 1001 = By-4 memory, not cross-coupled. 0110 = By-4 memory, cross-coupled. 0000 = Byte is not used. Other values are reserved.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	QUAD0_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an incoming clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
49	RW	QUAD1_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an incoming clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
50:51	RO	Reserved.
52	RW	QUAD0_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an incoming clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
53	RW	QUAD1_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an incoming clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
54	RW	QUAD2_CLK20: 1 = MEMINTD20B(n) and MEMINTD21B(n) are used as an incoming clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
55	RW	QUAD3_CLK20: 1 = MEMINTD20B(n) and MEMINTD21B(n) are used as an incoming clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.

Bits	SCOM	Field Mnemonic: Description
56	RW	QUAD2_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an incoming clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
57	RW	QUAD3_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an incoming clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
58:63	RO	Reserved.

Register Name	DP16 Write Clock Enable and Selection RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WRCLK_EN_RP2_P0_[n]
Address	800002050701103F (SCOM), +0x0400_0000_0000
Description	This register configures which output pins on the DP16 are used as clocks or strobes to capture outgoing data on which data pins. This register must be configured exactly the same as the DP16 Read Clock Enable and Selection Register. The following are legal configurations for bits 48:53: 110000 = by-8 memory using CLK16 000011 = by-8 memory using CLK18 100001 = by-4 memory, not cross-coupled 010010 = by-4 memory, cross-coupled 000000 = Byte is not used. Other values are reserved. The following are legal configurations for bits 54:57: 1100 = by-8 memory using CLK20 0011 = by-8 memory using CLK22 1001 = by-4 memory, not cross-coupled 0110 = by-4 memory, cross-coupled 0000 = Byte is not used. Other values are reserved. The same configuration should be loaded for all active ranks.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	QUAD0_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an outgoing clock to capture data on the following pins when the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.

Bits	SCOM	Field Mnemonic: Description
49	RW	QUAD1_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an outgoing clock to capture data on the following pins when the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
50:51	RW	Reserved.
52	RW	QUAD0_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
53	RW	QUAD1_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
54	RW	QUAD2_CLK20: 1 = MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
55	RW	QUAD3_CLK20: 1 = MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
56	RW	QUAD2_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.

Bits	SCOM	Field Mnemonic: Description
57	RW	QUAD3_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
58:63	RW	Reserved.

Register Name	**DP16 Write Clock Enable and Selection RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_WRCLK_EN_RP2_P1_[n]
Address	800002050701143F (SCOM), +0x0400_0000_0000
Description	This register configures which output pins on the DP16 are used as clocks or strobes to capture outgoing data on which data pins. This register must be configured exactly the same as the DP16 Read Clock Enable and Selection Register. The following are legal configurations for bits 48:53: 110000 = by-8 memory using CLK16 000011 = by-8 memory using CLK18 100001 = by-4 memory, not cross-coupled 010010 = by-4 memory, cross-coupled 000000 = Byte is not used. Other values are reserved. The following are legal configurations for bits 54:57: 1100 = by-8 memory using CLK20 0011 = by-8 memory using CLK22 1001 = by-4 memory, not cross-coupled 0110 = by-4 memory, cross-coupled 0000 = Byte is not used. Other values are reserved. The same configuration should be loaded for all active ranks.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	QUAD0_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an outgoing clock to capture data on the following pins when the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
49	RW	QUAD1_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an outgoing clock to capture data on the following pins when the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
50:51	RW	Reserved.

Bits	SCOM	Field Mnemonic: Description
52	RW	QUAD0_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
53	RW	QUAD1_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
54	RW	QUAD2_CLK20: 1 = MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
55	RW	QUAD3_CLK20: 1 = MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
56	RW	QUAD2_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
57	RW	QUAD3_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
58:63	RW	Reserved.

Register Name	DP16 Write Clock Enable and Selection RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WRCLK_EN_RP2_P2_[n]
Address	800002050701183F (SCOM), +0x0400_0000_0000
Description	This register configures which output pins on the DP16 are used as clocks or strobes to capture outgoing data on which data pins. This register must be configured exactly the same as the DP16 Read Clock Enable and Selection Register. The following are legal configurations for bits 48:53: 110000 = by-8 memory using CLK16 000011 = by-8 memory using CLK18 100001 = by-4 memory, not cross-coupled 010010 = by-4 memory, cross-coupled 000000 = Byte is not used. Other values are reserved. The following are legal configurations for bits 54:57: 1100 = by-8 memory using CLK20 0011 = by-8 memory using CLK22 1001 = by-4 memory, not cross-coupled 0110 = by-4 memory, cross-coupled 0000 = Byte is not used. Other values are reserved. The same configuration should be loaded for all active ranks.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	QUAD0_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an outgoing clock to capture data on the following pins when the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
49	RW	QUAD1_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an outgoing clock to capture data on the following pins when the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
50:51	RW	Reserved.
52	RW	QUAD0_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.

Bits	SCOM	Field Mnemonic: Description
53	RW	QUAD1_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
54	RW	QUAD2_CLK20: 1 = MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
55	RW	QUAD3_CLK20: 1 = MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
56	RW	QUAD2_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
57	RW	QUAD3_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
58:63	RW	Reserved.

Register Name	DP16 Write Clock Enable and Selection RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WRCLK_EN_RP2_P3_[n]
Address	8000020507011C3F (SCOM), +0x0400_0000_0000
Description	This register configures which output pins on the DP16 are used as clocks or strobes to capture outgoing data on which data pins. This register must be configured exactly the same as the DP16 Read Clock Enable and Selection Register. The following are legal configurations for bits 48:53: 110000 = by-8 memory using CLK16 000011 = by-8 memory using CLK18 100001 = by-4 memory, not cross-coupled 010010 = by-4 memory, cross-coupled 000000 = Byte is not used. Other values are reserved. The following are legal configurations for bits 54:57: 1100 = by-8 memory using CLK20 0011 = by-8 memory using CLK22 1001 = by-4 memory, not cross-coupled 0110 = by-4 memory, cross-coupled 0000 = Byte is not used. Other values are reserved. The same configuration should be loaded for all active ranks.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	QUAD0_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an outgoing clock to capture data on the following pins when the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
49	RW	QUAD1_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an outgoing clock to capture data on the following pins when the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
50:51	RW	Reserved.
52	RW	QUAD0_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.

Bits	SCOM	Field Mnemonic: Description
53	RW	QUAD1_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
54	RW	QUAD2_CLK20: 1 = MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
55	RW	QUAD3_CLK20: 1 = MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
56	RW	QUAD2_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
57	RW	QUAD3_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
58:63	RW	Reserved.

Register Name	DP16 DQS Read Phase Select RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_[n]
Address	800002090701103F (SCOM), +0x0400_0000_0000
Description	This register contains a dynamic value that represents the phase differences between the memory clock, strobes, and the receiver clocks. Hardware determines these values during initial calibration and maintains them during periodic calibrations. One register stores phase selects for each rank pair for a total of four registers. This register is provided for diagnostic use. Do not use software to write to this register during normal use.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RW	DQSCLK_SELECT0: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03.
50:51	RW	RDCLK_SELECT0: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03.
52:53	RW	DQSCLK_SELECT1: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07.
54:55	RW	RDCLK_SELECT1: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07.
56:57	RW	DQSCLK_SELECT2: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11.
58:59	RW	RDCLK_SELECT2: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11.
60:61	RW	DQSCLK_SELECT3: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15.
62:63	RW	RDCLK_SELECT3: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15.

Register Name	**DP16 DQS Read Phase Select RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_[n]
Address	800002090701143F (SCOM), +0x0400_0000_0000
Description	This register contains a dynamic value that represents the phase differences between the memory clock, strobes, and the receiver clocks. Hardware determines these values during initial calibration and maintains them during periodic calibrations. One register stores phase selects for each rank pair for a total of four registers. This register is provided for diagnostic use. Do not use software to write to this register during normal use.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:49	RW	DQSCLK_SELECT0: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03.
50:51	RW	RDCLK_SELECT0: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03.
52:53	RW	DQSCLK_SELECT1: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07.
54:55	RW	RDCLK_SELECT1: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07.
56:57	RW	DQSCLK_SELECT2: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11.
58:59	RW	RDCLK_SELECT2: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11.
60:61	RW	DQSCLK_SELECT3: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15.
62:63	RW	RDCLK_SELECT3: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15.

Register Name	DP16 DQS Read Phase Select RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQS_RD_PHASE_SELECT_RANK_PAIR2_P2_[n]
Address	800002090701183F (SCOM), +0x0400_0000_0000
Description	This register contains a dynamic value that represents the phase differences between the memory clock, strobes, and the receiver clocks. Hardware determines these values during initial calibration and maintains them during periodic calibrations. One register stores phase selects for each rank pair for a total of four registers. This register is provided for diagnostic use. Do not use software to write to this register during normal use.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:49	RW	DQSCLK_SELECT0: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03.
50:51	RW	RDCLK_SELECT0: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03.
52:53	RW	DQSCLK_SELECT1: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07.
54:55	RW	RDCLK_SELECT1: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07.
56:57	RW	DQSCLK_SELECT2: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11.
58:59	RW	RDCLK_SELECT2: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11.
60:61	RW	DQSCLK_SELECT3: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15.
62:63	RW	RDCLK_SELECT3: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15.

Register Name	DP16 DQS Read Phase Select RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQS_RD_PHASE_SELECT_RANK_PAIR2_P3_[n]
Address	8000020907011C3F (SCOM), +0x0400_0000_0000
Description	This register contains a dynamic value that represents the phase differences between the memory clock, strobes, and the receiver clocks. Hardware determines these values during initial calibration and maintains them during periodic calibrations. One register stores phase selects for each rank pair for a total of four registers. This register is provided for diagnostic use. Do not use software to write to this register during normal use.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:49	RW	DQSCLK_SELECT0: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03.
50:51	RW	RDCLK_SELECT0: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03.
52:53	RW	DQSCLK_SELECT1: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07.
54:55	RW	RDCLK_SELECT1: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07.

Bits	SCOM	Field Mnemonic: Description
56:57	RW	DQSCLK_SELECT2: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11.
58:59	RW	RDCLK_SELECT2: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11.
60:61	RW	DQSCLK_SELECT3: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15.
62:63	RW	RDCLK_SELECT3: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15.

Register Name	**DP16 Read Delay Offset 0 RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY_OFFSET0_RANK_PAIR2_P0_[n]
Address	8000020C0701103F (SCOM), +0x0400_0000_0000
Description	Each register field holds the read delay offsets for four of the MEMINTDnnB pins for one rank pair in the DP16.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	OFFSET0: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03 and nn{1} = 08, 09, 10, 11. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.
56	RO	Constant = 0b0
57:63	RW	OFFSET1: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07 and nn{1} = 12, 13, 14, 15. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.

Register Name	**DP16 Read Delay Offset 0 RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY_OFFSET0_RANK_PAIR2_P1_[n]
Address	8000020C0701143F (SCOM), +0x0400_0000_0000
Description	Each register field holds the read delay offsets for four of the MEMINTDnnB pins for one rank pair in the DP16.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	OFFSET0: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03 and nn{1} = 08, 09, 10, 11. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.
56	RO	Constant = 0b0

Bits	SCOM	Field Mnemonic: Description
57:63	RW	OFFSET1: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07 and nn{1} = 12, 13, 14, 15. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.

Register Name	**DP16 Read Delay Offset 0 RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY_OFFSET0_RANK_PAIR2_P2_[n]
Address	8000020C0701183F (SCOM), +0x0400_0000_0000
Description	Each register field holds the read delay offsets for four of the MEMINTDnnB pins for one rank pair in the DP16.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	OFFSET0: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03 and nn{1} = 08, 09, 10, 11. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.
56	RO	Constant = 0b0
57:63	RW	OFFSET1: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07 and nn{1} = 12, 13, 14, 15. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.

Register Name	**DP16 Read Delay Offset 0 RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY_OFFSET0_RANK_PAIR2_P3_[n]
Address	8000020C07011C3F (SCOM), +0x0400_0000_0000
Description	Each register field holds the read delay offsets for four of the MEMINTDnnB pins for one rank pair in the DP16.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	OFFSET0: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03 and nn{1} = 08, 09, 10, 11. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.
56	RO	Constant = 0b0

Bits	SCOM	Field Mnemonic: Description
57:63	RW	OFFSET1: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07 and nn{1} = 12, 13, 14, 15. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.

Register Name	**DP16 Read Delay Offset 1 RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY_OFFSET1_RANK_PAIR2_P0_[n]
Address	8000020D0701103F (SCOM), +0x0400_0000_0000
Description	Each register field holds the read delay offsets for four of the MEMINTDnnB pins for one rank pair in the DP16.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	OFFSET2: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03 and nn{1} = 08, 09, 10, 11. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.
56	RO	Constant = 0b0
57:63	RW	OFFSET3: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07 and nn{1} = 12, 13, 14, 15. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.

Register Name	**DP16 Read Delay Offset 1 RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY_OFFSET1_RANK_PAIR2_P1_[n]
Address	8000020D0701143F (SCOM), +0x0400_0000_0000
Description	Each register field holds the read delay offsets for four of the MEMINTDnnB pins for one rank pair in the DP16.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	OFFSET2: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03 and nn{1} = 08, 09, 10, 11. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.
56	RO	Constant = 0b0

Bits	SCOM	Field Mnemonic: Description
57:63	RW	OFFSET3: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07 and nn{1} = 12, 13, 14, 15. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.

Register Name	**DP16 Read Delay Offset 1 RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY_OFFSET1_RANK_PAIR2_P2_[n]
Address	8000020D0701183F (SCOM), +0x0400_0000_0000
Description	Each register field holds the read delay offsets for four of the MEMINTDnnB pins for one rank pair in the DP16.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	OFFSET2: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03 and nn{1} = 08, 09, 10, 11. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.
56	RO	Constant = 0b0
57:63	RW	OFFSET3: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07 and nn{1} = 12, 13, 14, 15. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.

Register Name	**DP16 Read Delay Offset 1 RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY_OFFSET1_RANK_PAIR2_P3_[n]
Address	8000020D07011C3F (SCOM), +0x0400_0000_0000
Description	Each register field holds the read delay offsets for four of the MEMINTDnnB pins for one rank pair in the DP16.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	OFFSET2: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03 and nn{1} = 08, 09, 10, 11. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.
56	RO	Constant = 0b0

Bits	SCOM	Field Mnemonic: Description
57:63	RW	OFFSET3: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07 and nn{1} = 12, 13, 14, 15. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.

Register Name	**DP16 DQS Gate Delay RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQS_GATE_DELAY_RP2_P0_[n]
Address	800002130701103F (SCOM), +0x0400_0000_0000
Description	This register contains the DQS gate delay settings for each incoming read clock. One register exists for each rank pair. This register must be reset or written to its reset value before running or rerunning initial calibration.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:51	RW	DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00 - DQ03 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
52	RO	Constant = 0b0
53:55	RW	DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04 - DQ07 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
56	RO	Constant = 0b0
57:59	RW	DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08 - DQ11 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
60	RO	Constant = 0b0
61:63	RW	DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12 - DQ15 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.

Register Name	**DP16 DQS Gate Delay RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQS_GATE_DELAY_RP2_P1_[n]
Address	800002130701143F (SCOM), +0x0400_0000_0000
Description	This register contains the DQS gate delay settings for each incoming read clock. One register exists for each rank pair. This register must be reset or written to its reset value before running or rerunning initial calibration.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:51	RW	DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00 - DQ03 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
52	RO	Constant = 0b0
53:55	RW	DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04 - DQ07 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
56	RO	Constant = 0b0
57:59	RW	DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08 - DQ11 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
60	RO	Constant = 0b0
61:63	RW	DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12 - DQ15 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.

Register Name	**DP16 DQS Gate Delay RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQS_GATE_DELAY_RP2_P2_[n]
Address	800002130701183F (SCOM), +0x0400_0000_0000
Description	This register contains the DQS gate delay settings for each incoming read clock. One register exists for each rank pair. This register must be reset or written to its reset value before running or rerunning initial calibration.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:51	RW	DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00 - DQ03 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
52	RO	Constant = 0b0
53:55	RW	DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04 - DQ07 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
56	RO	Constant = 0b0
57:59	RW	DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08 - DQ11 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.

Bits	SCOM	Field Mnemonic: Description
60	RO	Constant = 0b0
61:63	RW	DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12 - DQ15 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.

Register Name	**DP16 DQS Gate Delay RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQS_GATE_DELAY_RP2_P3_[n]
Address	8000021307011C3F (SCOM), +0x0400_0000_0000
Description	This register contains the DQS gate delay settings for each incoming read clock. One register exists for each rank pair. This register must be reset or written to its reset value before running or rerunning initial calibration.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:51	RW	DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00 - DQ03 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
52	RO	Constant = 0b0
53:55	RW	DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04 - DQ07 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
56	RO	Constant = 0b0
57:59	RW	DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08 - DQ11 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
60	RO	Constant = 0b0
61:63	RW	DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12 - DQ15 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.

Register Name	**DP16 DQSClk Phase Rotator Value 0 RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQSCLK_PR0_RANK_PAIR2_P0_[n]
Address	800002300701103F (SCOM), +0x0400_0000_0000
Description	Two phase rotator values are contained within each register. Two registers exist for each rank pair. These phase rotator values are the values needed to align the internal SysClk to the incoming DQS strobe for each group of data pins.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	DQSCLK_ROT_CLK_N0: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD00B – MEMINTD03B in register 0 and MEMINTD08B – MEMINTD11B in register 1. This value is updated by hardware.
56	RO	Constant = 0b0
57:63	RW	DQSCLK_ROT_CLK_N1: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINTD15B in register 1. This value is updated by hardware.

Register Name	DP16 DQSClk Phase Rotator Value 0 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQSCLK_PR0_RANK_PAIR2_P1_[n]
Address	800002300701143F (SCOM), +0x0400_0000_0000
Description	Two phase rotator values are contained within each register. Two registers exist for each rank pair. These phase rotator values are the values needed to align the internal SysClk to the incoming DQS strobe for each group of data pins.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	DQSCLK_ROT_CLK_N0: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD00B – MEMINTD03B in register 0 and MEMINTD08B – MEMINTD11B in register 1. This value is updated by hardware.
56	RO	Constant = 0b0
57:63	RW	DQSCLK_ROT_CLK_N1: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINTD15B in register 1. This value is updated by hardware.

Register Name	DP16 DQSClk Phase Rotator Value 0 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQSCLK_PR0_RANK_PAIR2_P2_[n]
Address	800002300701183F (SCOM), +0x0400_0000_0000
Description	Two phase rotator values are contained within each register. Two registers exist for each rank pair. These phase rotator values are the values needed to align the internal SysClk to the incoming DQS strobe for each group of data pins.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	DQSCLK_ROT_CLK_N0: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD00B – MEMINTD03B in register 0 and MEMINTD08B – MEMINTD11B in register 1. This value is updated by hardware.
56	RO	Constant = 0b0
57:63	RW	DQSCLK_ROT_CLK_N1: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINTD15B in register 1. This value is updated by hardware.

Register Name	DP16 DQSClk Phase Rotator Value 0 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQSCLK_PR0_RANK_PAIR2_P3_[n]
Address	8000023007011C3F (SCOM), +0x0400_0000_0000
Description	Two phase rotator values are contained within each register. Two registers exist for each rank pair. These phase rotator values are the values needed to align the internal SysClk to the incoming DQS strobe for each group of data pins.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	DQSCLK_ROT_CLK_N0: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD00B – MEMINTD03B in register 0 and MEMINTD08B – MEMINTD11B in register 1. This value is updated by hardware.
56	RO	Constant = 0b0
57:63	RW	DQSCLK_ROT_CLK_N1: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINTD15B in register 1. This value is updated by hardware.

Register Name	DP16 DQSClk Phase Rotator Value 1 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQSCLK_PR1_RANK_PAIR2_P0_[n]
Address	800002310701103F (SCOM), +0x0400_0000_0000
Description	Two phase rotator values are contained within each register. Two registers exist for each rank pair. These phase rotator values are the values needed to align the internal SysClk to the incoming DQS strobe for each group of data pins.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	DQSCLK_ROT_CLK_N2: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD00B – MEMINTD03B in register 0 and MEMINTD08B – MEMINTD11B in register 1. This value is updated by hardware.
56	RO	Constant = 0b0
57:63	RW	DQSCLK_ROT_CLK_N3: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINTD15B in register 1. This value is updated by hardware.

Register Name	DP16 DQSClk Phase Rotator Value 1 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQSCLK_PR1_RANK_PAIR2_P1_[n]
Address	800002310701143F (SCOM), +0x0400_0000_0000
Description	Two phase rotator values are contained within each register. Two registers exist for each rank pair. These phase rotator values are the values needed to align the internal SysClk to the incoming DQS strobe for each group of data pins.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	DQSCLK_ROT_CLK_N2: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD00B – MEMINTD03B in register 0 and MEMINTD08B – MEMINTD11B in register 1. This value is updated by hardware.

Bits	SCOM	Field Mnemonic: Description
56	RO	Constant = 0b0
57:63	RW	DQSCLK_ROT_CLK_N3: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINTD15B in register 1. This value is updated by hardware.

Register Name	**DP16 DQSClk Phase Rotator Value 1 RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQSCLK_PR1_RANK_PAIR2_P2_[n]
Address	800002310701183F (SCOM), +0x0400_0000_0000
Description	Two phase rotator values are contained within each register. Two registers exist for each rank pair. These phase rotator values are the values needed to align the internal SysClk to the incoming DQS strobe for each group of data pins.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	DQSCLK_ROT_CLK_N2: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD00B – MEMINTD03B in register 0 and MEMINTD08B – MEMINTD11B in register 1. This value is updated by hardware.
56	RO	Constant = 0b0
57:63	RW	DQSCLK_ROT_CLK_N3: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINTD15B in register 1. This value is updated by hardware.

Register Name	**DP16 DQSClk Phase Rotator Value 1 RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQSCLK_PR1_RANK_PAIR2_P3_[n]
Address	8000023107011C3F (SCOM), +0x0400_0000_0000
Description	Two phase rotator values are contained within each register. Two registers exist for each rank pair. These phase rotator values are the values needed to align the internal SysClk to the incoming DQS strobe for each group of data pins.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	DQSCLK_ROT_CLK_N2: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD00B – MEMINTD03B in register 0 and MEMINTD08B – MEMINTD11B in register 1. This value is updated by hardware.
56	RO	Constant = 0b0
57:63	RW	DQSCLK_ROT_CLK_N3: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINTD15B in register 1. This value is updated by hardware.

Register Name	DP16 Write Delay Value 0 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_0_RP2_REG_P0_[n]
Address	800002380701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 0 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_0_RP2_REG_P1_[n]
Address	800002380701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 0 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_0_RP2_REG_P2_[n]
Address	800002380701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 0 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_0_RP2_REG_P3_[n]
Address	8000023807011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 1 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_1_RP2_REG_P0_[n]
Address	800002390701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 1 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_1_RP2_REG_P1_[n]
Address	800002390701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 1 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_1_RP2_REG_P2_[n]
Address	800002390701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 1 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_1_RP2_REG_P3_[n]
Address	8000023907011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 2 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_2_RP2_REG_P0_[n]
Address	8000023A0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 2 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_2_RP2_REG_P1_[n]
Address	8000023A0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 2 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_2_RP2_REG_P2_[n]
Address	8000023A0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 2 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_2_RP2_REG_P3_[n]
Address	8000023A07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 3 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_3_RP2_REG_P0_[n]
Address	8000023B0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 3 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_3_RP2_REG_P1_[n]
Address	8000023B0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 3 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_3_RP2_REG_P2_[n]
Address	8000023B0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 3 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_3_RP2_REG_P3_[n]
Address	8000023B07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 4 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_4_RP2_REG_P0_[n]
Address	8000023C0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 4 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_4_RP2_REG_P1_[n]
Address	8000023C0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 4 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_4_RP2_REG_P2_[n]
Address	8000023C0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 4 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_4_RP2_REG_P3_[n]
Address	8000023C07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 5 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_5_RP2_REG_P0_[n]
Address	8000023D0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 5 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_5_RP2_REG_P1_[n]
Address	8000023D0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 5 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_5_RP2_REG_P2_[n]
Address	8000023D0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 5 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_5_RP2_REG_P3_[n]
Address	8000023D07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 6 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_6_RP2_REG_P0_[n]
Address	8000023E0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 6 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_6_RP2_REG_P1_[n]
Address	8000023E0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 6 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_6_RP2_REG_P2_[n]
Address	8000023E0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 6 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_6_RP2_REG_P3_[n]
Address	8000023E07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 7 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_7_RP2_REG_P0_[n]
Address	8000023F0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 7 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_7_RP2_REG_P1_[n]
Address	8000023F0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 7 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_7_RP2_REG_P2_[n]
Address	8000023F0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 7 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_7_RP2_REG_P3_[n]
Address	8000023F07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 8 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_8_RP2_REG_P0_[n]
Address	800002400701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 8 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_8_RP2_REG_P1_[n]
Address	800002400701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 8 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_8_RP2_REG_P2_[n]
Address	800002400701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 8 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_8_RP2_REG_P3_[n]
Address	8000024007011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 9 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_9_RP2_REG_P0_[n]
Address	800002410701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 9 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_9_RP2_REG_P1_[n]
Address	800002410701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 9 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_9_RP2_REG_P2_[n]
Address	800002410701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 9 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_9_RP2_REG_P3_[n]
Address	8000024107011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 10 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_10_RP2_REG_P0_[n]
Address	800002420701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 10 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_10_RP2_REG_P1_[n]
Address	800002420701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 10 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_10_RP2_REG_P2_[n]
Address	800002420701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 10 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_10_RP2_REG_P3_[n]
Address	8000024207011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 11 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_11_RP2_REG_P0_[n]
Address	800002430701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 11 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_11_RP2_REG_P1_[n]
Address	800002430701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 11 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_11_RP2_REG_P2_[n]
Address	800002430701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 11 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_11_RP2_REG_P3_[n]
Address	8000024307011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 12 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_12_RP2_REG_P0_[n]
Address	800002440701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 12 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_12_RP2_REG_P1_[n]
Address	800002440701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 12 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_12_RP2_REG_P2_[n]
Address	800002440701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 12 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_12_RP2_REG_P3_[n]
Address	8000024407011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 13 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_13_RP2_REG_P0_[n]
Address	800002450701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 13 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_13_RP2_REG_P1_[n]
Address	800002450701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 13 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_13_RP2_REG_P2_[n]
Address	800002450701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 13 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_13_RP2_REG_P3_[n]
Address	8000024507011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 14 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_14_RP2_REG_P0_[n]
Address	800002460701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 14 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_14_RP2_REG_P1_[n]
Address	800002460701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 14 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_14_RP2_REG_P2_[n]
Address	800002460701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 14 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_14_RP2_REG_P3_[n]
Address	8000024607011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 15 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_15_RP2_REG_P0_[n]
Address	800002470701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 15 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_15_RP2_REG_P1_[n]
Address	800002470701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 15 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_15_RP2_REG_P2_[n]
Address	800002470701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 15 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_15_RP2_REG_P3_[n]
Address	8000024707011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 16 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_16_RP2_REG_P0_[n]
Address	800002480701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 16 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_16_RP2_REG_P1_[n]
Address	800002480701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 16 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_16_RP2_REG_P2_[n]
Address	800002480701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 16 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_16_RP2_REG_P3_[n]
Address	8000024807011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 18 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_18_RP2_REG_P0_[n]
Address	8000024A0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 18 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_18_RP2_REG_P1_[n]
Address	8000024A0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 18 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_18_RP2_REG_P2_[n]
Address	8000024A0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 18 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_18_RP2_REG_P3_[n]
Address	8000024A07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 20 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_20_RP2_REG_P0_[n]
Address	8000024C0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 20 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_20_RP2_REG_P1_[n]
Address	8000024C0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 20 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_20_RP2_REG_P2_[n]
Address	8000024C0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 20 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_20_RP2_REG_P3_[n]
Address	8000024C07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 22 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_22_RP2_REG_P0_[n]
Address	8000024E0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 22 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_22_RP2_REG_P1_[n]
Address	8000024E0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 22 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_22_RP2_REG_P2_[n]
Address	8000024E0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 22 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_22_RP2_REG_P3_[n]
Address	8000024E07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Read Delay Value 0 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY0_RANK_PAIR2_P0_[n]
Address	800002500701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 0 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY0_RANK_PAIR2_P1_[n]
Address	800002500701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.

Bits	SCOM	Field Mnemonic: Description
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 0 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY0_RANK_PAIR2_P2_[n]
Address	800002500701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 0 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY0_RANK_PAIR2_P3_[n]
Address	8000025007011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	**DP16 Read Delay Value 1 RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY1_RANK_PAIR2_P0_[n]
Address	800002510701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	**DP16 Read Delay Value 1 RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY1_RANK_PAIR2_P1_[n]
Address	800002510701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	**DP16 Read Delay Value 1 RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY1_RANK_PAIR2_P2_[n]
Address	800002510701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 1 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY1_RANK_PAIR2_P3_[n]
Address	8000025107011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 2 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY2_RANK_PAIR2_P0_[n]
Address	800002520701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.

Bits	SCOM	Field Mnemonic: Description
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 2 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY2_RANK_PAIR2_P1_[n]
Address	800002520701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 2 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY2_RANK_PAIR2_P2_[n]
Address	800002520701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	**DP16 Read Delay Value 2 RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY2_RANK_PAIR2_P3_[n]
Address	8000025207011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	**DP16 Read Delay Value 3 RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY3_RANK_PAIR2_P0_[n]
Address	800002530701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	**DP16 Read Delay Value 3 RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY3_RANK_PAIR2_P1_[n]
Address	800002530701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 3 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY3_RANK_PAIR2_P2_[n]
Address	800002530701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 3 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY3_RANK_PAIR2_P3_[n]
Address	8000025307011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.

Bits	SCOM	Field Mnemonic: Description
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 4 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY4_RANK_PAIR2_P0_[n]
Address	800002540701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 4 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY4_RANK_PAIR2_P1_[n]
Address	800002540701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	**DP16 Read Delay Value 4 RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY4_RANK_PAIR2_P2_[n]
Address	800002540701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	**DP16 Read Delay Value 4 RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY4_RANK_PAIR2_P3_[n]
Address	8000025407011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 5 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY5_RANK_PAIR2_P0_[n]
Address	800002550701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 5 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY5_RANK_PAIR2_P1_[n]
Address	800002550701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 5 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY5_RANK_PAIR2_P2_[n]
Address	800002550701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.

Bits	SCOM	Field Mnemonic: Description
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 5 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY5_RANK_PAIR2_P3_[n]
Address	8000025507011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 6 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY6_RANK_PAIR2_P0_[n]
Address	800002560701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	**DP16 Read Delay Value 6 RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY6_RANK_PAIR2_P1_[n]
Address	800002560701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	**DP16 Read Delay Value 6 RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY6_RANK_PAIR2_P2_[n]
Address	800002560701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 6 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY6_RANK_PAIR2_P3_[n]
Address	8000025607011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 7 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY7_RANK_PAIR2_P0_[n]
Address	800002570701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 7 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY7_RANK_PAIR2_P1_[n]
Address	800002570701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.

Bits	SCOM	Field Mnemonic: Description
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 7 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY7_RANK_PAIR2_P2_[n]
Address	800002570701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 7 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY7_RANK_PAIR2_P3_[n]
Address	8000025707011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	**DP16 Initial DQS Alignment 0 RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN0_RANK_PAIR2_P0_[n]
Address	8000025C0701103F (SCOM), +0x0400_0000_0000
Description	These registers hold the DQSClk phase rotator values computed by initial calibration, They are updated at multiple times during the calibration. Periodic DQS alignment uses the values to compare against for determining long-term drift.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RO	INITIAL_DQS_ROT_N0: This field holds the initial DQSClk rotator value for pins MEMINTD00B - MEMINTD03B in register 0 and MEMINTD08B - MEMINGTD11B in register 1. This value is updated by hardware.
56	RO	Reserved.
57:63	RO	INITIAL_DQS_ROT_N1: This field holds the initial DQSClk rotator value for pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINGTD15B in register 1.This value is updated by hardware.

Register Name	**DP16 Initial DQS Alignment 0 RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN0_RANK_PAIR2_P1_[n]
Address	8000025C0701143F (SCOM), +0x0400_0000_0000
Description	These registers hold the DQSClk phase rotator values computed by initial calibration, They are updated at multiple times during the calibration. Periodic DQS alignment uses the values to compare against for determining long-term drift.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RO	INITIAL_DQS_ROT_N0: This field holds the initial DQSClk rotator value for pins MEMINTD00B - MEMINTD03B in register 0 and MEMINTD08B - MEMINGTD11B in register 1. This value is updated by hardware.
56	RO	Reserved.
57:63	RO	INITIAL_DQS_ROT_N1: This field holds the initial DQSClk rotator value for pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINGTD15B in register 1.This value is updated by hardware.

Register Name	DP16 Initial DQS Alignment 0 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN0_RANK_PAIR2_P2_[n]
Address	8000025C0701183F (SCOM), +0x0400_0000_0000
Description	These registers hold the DQSClk phase rotator values computed by initial calibration, They are updated at multiple times during the calibration. Periodic DQS alignment uses the values to compare against for determining long-term drift.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RO	INITIAL_DQS_ROT_N0: This field holds the initial DQSClk rotator value for pins MEMINTD00B - MEMINTD03B in register 0 and MEMINTD08B - MEMINGTD11B in register 1. This value is updated by hardware.
56	RO	Reserved.
57:63	RO	INITIAL_DQS_ROT_N1: This field holds the initial DQSClk rotator value for pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINGTD15B in register 1.This value is updated by hardware.

Register Name	DP16 Initial DQS Alignment 0 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN0_RANK_PAIR2_P3_[n]
Address	8000025C07011C3F (SCOM), +0x0400_0000_0000
Description	These registers hold the DQSClk phase rotator values computed by initial calibration, They are updated at multiple times during the calibration. Periodic DQS alignment uses the values to compare against for determining long-term drift.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RO	INITIAL_DQS_ROT_N0: This field holds the initial DQSClk rotator value for pins MEMINTD00B - MEMINTD03B in register 0 and MEMINTD08B - MEMINGTD11B in register 1. This value is updated by hardware.
56	RO	Reserved.
57:63	RO	INITIAL_DQS_ROT_N1: This field holds the initial DQSClk rotator value for pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINGTD15B in register 1.This value is updated by hardware.

Register Name	DP16 Initial DQS Alignment 1 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN1_RANK_PAIR2_P0_[n]
Address	8000025D0701103F (SCOM), +0x0400_0000_0000
Description	These registers hold the DQSClk phase rotator values computed by initial calibration, They are updated at multiple times during the calibration. Periodic DQS alignment uses the values to compare against for determining long-term drift.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RO	INITIAL_DQS_ROT_N2: This field holds the initial DQSClk rotator value for pins MEMINTD00B - MEMINTD03B in register 0 and MEMINTD08B - MEMINGTD11B in register 1. This value is updated by hardware.

Bits	SCOM	Field Mnemonic: Description
56	RO	Constant = 0b0
57:63	RO	INITIAL_DQS_ROT_N3: This field holds the initial DQSClk rotator value for pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINGTD15B in register 1.This value is updated by hardware.

Register Name	**DP16 Initial DQS Alignment 1 RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN1_RANK_PAIR2_P1_[n]
Address	8000025D0701143F (SCOM), +0x0400_0000_0000
Description	These registers hold the DQSClk phase rotator values computed by initial calibration, They are updated at multiple times during the calibration. Periodic DQS alignment uses the values to compare against for determining long-term drift.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RO	INITIAL_DQS_ROT_N2: This field holds the initial DQSClk rotator value for pins MEMINTD00B - MEMINTD03B in register 0 and MEMINTD08B - MEMINGTD11B in register 1. This value is updated by hardware.
56	RO	Constant = 0b0
57:63	RO	INITIAL_DQS_ROT_N3: This field holds the initial DQSClk rotator value for pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINGTD15B in register 1.This value is updated by hardware.

Register Name	**DP16 Initial DQS Alignment 1 RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN1_RANK_PAIR2_P2_[n]
Address	8000025D0701183F (SCOM), +0x0400_0000_0000
Description	These registers hold the DQSClk phase rotator values computed by initial calibration, They are updated at multiple times during the calibration. Periodic DQS alignment uses the values to compare against for determining long-term drift.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RO	INITIAL_DQS_ROT_N2: This field holds the initial DQSClk rotator value for pins MEMINTD00B - MEMINTD03B in register 0 and MEMINTD08B - MEMINGTD11B in register 1. This value is updated by hardware.
56	RO	Constant = 0b0
57:63	RO	INITIAL_DQS_ROT_N3: This field holds the initial DQSClk rotator value for pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINGTD15B in register 1.This value is updated by hardware.

Register Name	DP16 Initial DQS Alignment 1 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN1_RANK_PAIR2_P3_[n]
Address	8000025D07011C3F (SCOM), +0x0400_0000_0000
Description	These registers hold the DQSClk phase rotator values computed by initial calibration, They are updated at multiple times during the calibration. Periodic DQS alignment uses the values to compare against for determining long-term drift.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RO	INITIAL_DQS_ROT_N2: This field holds the initial DQSClk rotator value for pins MEMINTD00B - MEMINTD03B in register 0 and MEMINTD08B - MEMINGTD11B in register 1. This value is updated by hardware.
56	RO	Constant = 0b0
57:63	RO	INITIAL_DQS_ROT_N3: This field holds the initial DQSClk rotator value for pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINGTD15B in register 1.This value is updated by hardware.

Register Name	DP16 Write VREF Value 0 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_VALUE0_RANK_PAIR2_P0_[n]
Address	8000025E0701103F (SCOM), +0x0400_0000_0000
Description	This register contains the starting and ending values of calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48	RW	Reserved.
49	RWX	WR_VREF_RANGE_DRAM0: This bit contains the default and current value of the DRAM WR VREF range for DRAM0 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
50:55	RWX	WR_VREF_VALUE_DRAM0: This field contains the default and current value of the DRAM WR VREF value for DRAM0 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
56	RW	Reserved.
57	RWX	WR_VREF_RANGE_DRAM1: This bit contains the default and current value of the DRAM WR VREF range for DRAM1 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
58:63	RWX	WR_VREF_VALUE_DRAM1: This field contains the default and current value of the DRAM WR VREF value for DRAM1 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.

Register Name	DP16 Write VREF Value 0 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_VALUE0_RANK_PAIR2_P1_[n]
Address	8000025E0701143F (SCOM), +0x0400_0000_0000
Description	This register contains the starting and ending values of calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	Reserved.
49	RWX	WR_VREF_RANGE_DRAM0: This bit contains the default and current value of the DRAM WR VREF range for DRAM0 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
50:55	RWX	WR_VREF_VALUE_DRAM0: This field contains the default and current value of the DRAM WR VREF value for DRAM0 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
56	RW	Reserved.
57	RWX	WR_VREF_RANGE_DRAM1: This bit contains the default and current value of the DRAM WR VREF range for DRAM1 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
58:63	RWX	WR_VREF_VALUE_DRAM1: This field contains the default and current value of the DRAM WR VREF value for DRAM1 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.

Register Name	DP16 Write VREF Value 0 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_VALUE0_RANK_PAIR2_P2_[n]
Address	8000025E0701183F (SCOM), +0x0400_0000_0000
Description	This register contains the starting and ending values of calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	Reserved.
49	RWX	WR_VREF_RANGE_DRAM0: This bit contains the default and current value of the DRAM WR VREF range for DRAM0 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
50:55	RWX	WR_VREF_VALUE_DRAM0: This field contains the default and current value of the DRAM WR VREF value for DRAM0 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
56	RW	Reserved.
57	RWX	WR_VREF_RANGE_DRAM1: This bit contains the default and current value of the DRAM WR VREF range for DRAM1 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	WR_VREF_VALUE_DRAM1: This field contains the default and current value of the DRAM WR VREF value for DRAM1 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.

Register Name	DP16 Write VREF Value 0 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_VALUE0_RANK_PAIR2_P3_[n]
Address	8000025E07011C3F (SCOM), +0x0400_0000_0000
Description	This register contains the starting and ending values of calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48	RW	Reserved.
49	RWX	WR_VREF_RANGE_DRAM0: This bit contains the default and current value of the DRAM WR VREF range for DRAM0 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
50:55	RWX	WR_VREF_VALUE_DRAM0: This field contains the default and current value of the DRAM WR VREF value for DRAM0 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
56	RW	Reserved.
57	RWX	WR_VREF_RANGE_DRAM1: This bit contains the default and current value of the DRAM WR VREF range for DRAM1 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
58:63	RWX	WR_VREF_VALUE_DRAM1: This field contains the default and current value of the DRAM WR VREF value for DRAM1 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.

Register Name	DP16 Write VREF Value 1 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_VALUE1_RANK_PAIR2_P0_[n]
Address	8000025F0701103F (SCOM), +0x0400_0000_0000
Description	This register contains the starting and ending values of calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48	RW	Reserved.
49	RWX	WR_VREF_RANGE_DRAM2: This bit contains the default and current value of the DRAM WR VREF range for DRAM2 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	WR_VREF_VALUE_DRAM2: This bit contains the default and current value of the DRAM WR VREF value for DRAM2 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
56	RW	Reserved.
57	RWX	WR_VREF_RANGE_DRAM3: This bit contains the default and current value of the DRAM WR VREF range for DRAM3 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
58:63	RWX	WR_VREF_VALUE_DRAM3: This bit contains the default and current value of the DRAM WR VREF value for DRAM3 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.

Register Name	**DP16 Write VREF Value 1 RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_VALUE1_RANK_PAIR2_P1_[n]
Address	8000025F0701143F (SCOM), +0x0400_0000_0000
Description	This register contains the starting and ending values of calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48	RW	Reserved.
49	RWX	WR_VREF_RANGE_DRAM2: This bit contains the default and current value of the DRAM WR VREF range for DRAM2 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
50:55	RWX	WR_VREF_VALUE_DRAM2: This bit contains the default and current value of the DRAM WR VREF value for DRAM2 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
56	RW	Reserved.
57	RWX	WR_VREF_RANGE_DRAM3: This bit contains the default and current value of the DRAM WR VREF range for DRAM3 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
58:63	RWX	WR_VREF_VALUE_DRAM3: This bit contains the default and current value of the DRAM WR VREF value for DRAM3 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.

Register Name	**DP16 Write VREF Value 1 RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_VALUE1_RANK_PAIR2_P2_[n]
Address	8000025F0701183F (SCOM), +0x0400_0000_0000
Description	This register contains the starting and ending values of calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49	RWX	WR_VREF_RANGE_DRAM2: This bit contains the default and current value of the DRAM WR VREF range for DRAM2 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
50:55	RWX	WR_VREF_VALUE_DRAM2: This bit contains the default and current value of the DRAM WR VREF value for DRAM2 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
56	RW	Reserved.
57	RWX	WR_VREF_RANGE_DRAM3: This bit contains the default and current value of the DRAM WR VREF range for DRAM3 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
58:63	RWX	WR_VREF_VALUE_DRAM3: This bit contains the default and current value of the DRAM WR VREF value for DRAM3 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.

Register Name	DP16 Write VREF Value 1 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_VALUE1_RANK_PAIR2_P3_[n]
Address	8000025F07011C3F (SCOM), +0x0400_0000_0000
Description	This register contains the starting and ending values of calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49	RWX	WR_VREF_RANGE_DRAM2: This bit contains the default and current value of the DRAM WR VREF range for DRAM2 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
50:55	RWX	WR_VREF_VALUE_DRAM2: This bit contains the default and current value of the DRAM WR VREF value for DRAM2 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
56	RW	Reserved.
57	RWX	WR_VREF_RANGE_DRAM3: This bit contains the default and current value of the DRAM WR VREF range for DRAM3 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
58:63	RWX	WR_VREF_VALUE_DRAM3: This bit contains the default and current value of the DRAM WR VREF value for DRAM3 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.

Register Name	**DP16 Read Eye Size 0 RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE0_RANK_PAIR2_P0_[n]
Address	800002600701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	**DP16 Read Eye Size 0 RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE0_RANK_PAIR2_P1_[n]
Address	800002600701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 0 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE0_RANK_PAIR2_P2_[n]
Address	800002600701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 0 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE0_RANK_PAIR2_P3_[n]
Address	8000026007011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 1 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE1_RANK_PAIR2_P0_[n]
Address	800002610701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 1 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE1_RANK_PAIR2_P1_[n]
Address	800002610701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 1 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE1_RANK_PAIR2_P2_[n]
Address	800002610701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 1 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE1_RANK_PAIR2_P3_[n]
Address	8000026107011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 2 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE2_RANK_PAIR2_P0_[n]
Address	800002620701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 2 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE2_RANK_PAIR2_P1_[n]
Address	800002620701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 2 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE2_RANK_PAIR2_P2_[n]
Address	800002620701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 2 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE2_RANK_PAIR2_P3_[n]
Address	8000026207011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 3 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE3_RANK_PAIR2_P0_[n]
Address	800002630701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 3 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE3_RANK_PAIR2_P1_[n]
Address	800002630701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 3 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE3_RANK_PAIR2_P2_[n]
Address	800002630701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 3 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE3_RANK_PAIR2_P3_[n]
Address	8000026307011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 4 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE4_RANK_PAIR2_P0_[n]
Address	800002640701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 4 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE4_RANK_PAIR2_P1_[n]
Address	800002640701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 4 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE4_RANK_PAIR2_P2_[n]
Address	800002640701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 4 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE4_RANK_PAIR2_P3_[n]
Address	8000026407011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	**DP16 Read Eye Size 5 RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE5_RANK_PAIR2_P0_[n]
Address	800002650701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	**DP16 Read Eye Size 5 RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE5_RANK_PAIR2_P1_[n]
Address	800002650701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 5 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE5_RANK_PAIR2_P2_[n]
Address	800002650701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 5 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE5_RANK_PAIR2_P3_[n]
Address	8000026507011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 6 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE6_RANK_PAIR2_P0_[n]
Address	800002660701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 6 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE6_RANK_PAIR2_P1_[n]
Address	800002660701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 6 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE6_RANK_PAIR2_P2_[n]
Address	800002660701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 6 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE6_RANK_PAIR2_P3_[n]
Address	8000026607011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 7 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE7_RANK_PAIR2_P0_[n]
Address	800002670701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 7 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE7_RANK_PAIR2_P1_[n]
Address	800002670701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 7 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE7_RANK_PAIR2_P2_[n]
Address	800002670701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 7 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE7_RANK_PAIR2_P3_[n]
Address	8000026707011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 8 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE8_RANK_PAIR2_P0_[n]
Address	800002680701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 8 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE8_RANK_PAIR2_P1_[n]
Address	800002680701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 8 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE8_RANK_PAIR2_P2_[n]
Address	800002680701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 8 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE8_RANK_PAIR2_P3_[n]
Address	8000026807011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 9 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE9_RANK_PAIR2_P0_[n]
Address	800002690701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 9 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE9_RANK_PAIR2_P1_[n]
Address	800002690701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 9 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE9_RANK_PAIR2_P2_[n]
Address	800002690701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 9 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE9_RANK_PAIR2_P3_[n]
Address	8000026907011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 10 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE10_RANK_PAIR2_P0_[n]
Address	8000026A0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 10 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE10_RANK_PAIR2_P1_[n]
Address	8000026A0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 10 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE10_RANK_PAIR2_P2_[n]
Address	8000026A0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 10 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE10_RANK_PAIR2_P3_[n]
Address	8000026A07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	**DP16 Read Eye Size 11 RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE11_RANK_PAIR2_P0_[n]
Address	8000026B0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	**DP16 Read Eye Size 11 RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE11_RANK_PAIR2_P1_[n]
Address	8000026B0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 11 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE11_RANK_PAIR2_P2_[n]
Address	8000026B0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 11 RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE11_RANK_PAIR2_P3_[n]
Address	8000026B07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	**DP16 DQ Bit Disable RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQ_BIT_DISABLE_RP2_P0_[n]
Address	8000027C0701103F (SCOM), +0x0400_0000_0000
Description	This register is used to disable each of the 16 pins on the DP16. During calibration operations, the hardware sets the bit in this register that corresponds to a pin on the DP16 that failed a calibration step. This register indicates which DQ pins on the DP16 failed a calibration step. This register does not indicate which calibration step failed.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DQ_BIT_DISABLE_0_15: 1 = Indicates that the DP16 bit is disabled and does not participate in any calibration steps. 0 = Indicates that the DP16 bit is not disabled. Bit 48 controls MEMINTD00B(n). Bit 49 controls MEMINTD01B(n). Bit 50 controls MEMINTD02B(n). ... Bit 63 controls MEMINTD15B(n). where n is the DP16 instance number.

Register Name	**DP16 DQ Bit Disable RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQ_BIT_DISABLE_RP2_P1_[n]
Address	8000027C0701143F (SCOM), +0x0400_0000_0000
Description	This register is used to disable each of the 16 pins on the DP16. During calibration operations, the hardware sets the bit in this register that corresponds to a pin on the DP16 that failed a calibration step. This register indicates which DQ pins on the DP16 failed a calibration step. This register does not indicate which calibration step failed.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DQ_BIT_DISABLE_0_15: 1 = Indicates that the DP16 bit is disabled and does not participate in any calibration steps. 0 = Indicates that the DP16 bit is not disabled. Bit 48 controls MEMINTD00B(n). Bit 49 controls MEMINTD01B(n). Bit 50 controls MEMINTD02B(n). ... Bit 63 controls MEMINTD15B(n). where n is the DP16 instance number.

Register Name	**DP16 DQ Bit Disable RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQ_BIT_DISABLE_RP2_P2_[n]
Address	8000027C0701183F (SCOM), +0x0400_0000_0000
Description	This register is used to disable each of the 16 pins on the DP16. During calibration operations, the hardware sets the bit in this register that corresponds to a pin on the DP16 that failed a calibration step. This register indicates which DQ pins on the DP16 failed a calibration step. This register does not indicate which calibration step failed.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	DQ_BIT_DISABLE_0_15: 1 = Indicates that the DP16 bit is disabled and does not participate in any calibration steps. 0 = Indicates that the DP16 bit is not disabled. Bit 48 controls MEMINTD00B(n). Bit 49 controls MEMINTD01B(n). Bit 50 controls MEMINTD02B(n). ... Bit 63 controls MEMINTD15B(n). where n is the DP16 instance number.

Register Name	**DP16 DQ Bit Disable RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQ_BIT_DISABLE_RP2_P3_[n]
Address	8000027C07011C3F (SCOM), +0x0400_0000_0000
Description	This register is used to disable each of the 16 pins on the DP16. During calibration operations, the hardware sets the bit in this register that corresponds to a pin on the DP16 that failed a calibration step. This register indicates which DQ pins on the DP16 failed a calibration step. This register does not indicate which calibration step failed.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	DQ_BIT_DISABLE_0_15: 1 = Indicates that the DP16 bit is disabled and does not participate in any calibration steps. 0 = Indicates that the DP16 bit is not disabled. Bit 48 controls MEMINTD00B(n). Bit 49 controls MEMINTD01B(n). Bit 50 controls MEMINTD02B(n). ... Bit 63 controls MEMINTD15B(n). where n is the DP16 instance number.

Register Name	**DP16 DQS Bit Disable RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQS_BIT_DISABLE_RP2_P0_[n]
Address	8000027D0701103F (SCOM), +0x0400_0000_0000
Description	This register is used to disable each of the eight DQS pins on the DP16. During calibration operations, the hardware sets the bit in this register that corresponds to a pin on the DP16 that failed a calibration step. This register indicates which DQS pins on the DP16 failed a calibration step. This register does not indicate which calibration step failed.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DQS_BIT_DISABLE_16_23: Bits are grouped in pairs. Bits 48:49, 50:51, 52:53, and 54:55 correspond to the differential DQS bits for each pair. 1 = Indicates that the DQS bits are disabled and do not participate in any calibration steps. Both DQS bits in the pair are set to 1b. 0 = Indicates that the DQS bits are not disabled. Both DQS bits in the pair are set to 0b. Bits 48:49 indicate the disable state of the DQS associated with QUAD0, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 50:51 indicate the disable state of the DQS associated with QUAD1, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 52:53 indicate the disable state of the DQS associated with QUAD2, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 54:55 indicate the disable state of the DQS associated with QUAD3, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register.
56:63	RO	Constant = 0b00000000

Register Name	**DP16 DQS Bit Disable RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQS_BIT_DISABLE_RP2_P1_[n]
Address	8000027D0701143F (SCOM), +0x0400_0000_0000
Description	This register is used to disable each of the eight DQS pins on the DP16. During calibration operations, the hardware sets the bit in this register that corresponds to a pin on the DP16 that failed a calibration step. This register indicates which DQS pins on the DP16 failed a calibration step. This register does not indicate which calibration step failed.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:55	RW	DQS_BIT_DISABLE_16_23: Bits are grouped in pairs. Bits 48:49, 50:51, 52:53, and 54:55 correspond to the differential DQS bits for each pair. 1 = Indicates that the DQS bits are disabled and do not participate in any calibration steps. Both DQS bits in the pair are set to 1b. 0 = Indicates that the DQS bits are not disabled. Both DQS bits in the pair are set to 0b. Bits 48:49 indicate the disable state of the DQS associated with QUAD0, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 50:51 indicate the disable state of the DQS associated with QUAD1, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 52:53 indicate the disable state of the DQS associated with QUAD2, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 54:55 indicate the disable state of the DQS associated with QUAD3, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register.
56:63	RO	Constant = 0b00000000

Register Name	DP16 DQS Bit Disable RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQS_BIT_DISABLE_RP2_P2_[n]
Address	8000027D0701183F (SCOM), +0x0400_0000_0000
Description	This register is used to disable each of the eight DQS pins on the DP16. During calibration operations, the hardware sets the bit in this register that corresponds to a pin on the DP16 that failed a calibration step. This register indicates which DQS pins on the DP16 failed a calibration step. This register does not indicate which calibration step failed.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:55	RW	DQS_BIT_DISABLE_16_23: Bits are grouped in pairs. Bits 48:49, 50:51, 52:53, and 54:55 correspond to the differential DQS bits for each pair. 1 = Indicates that the DQS bits are disabled and do not participate in any calibration steps. Both DQS bits in the pair are set to 1b. 0 = Indicates that the DQS bits are not disabled. Both DQS bits in the pair are set to 0b. Bits 48:49 indicate the disable state of the DQS associated with QUAD0, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 50:51 indicate the disable state of the DQS associated with QUAD1, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 52:53 indicate the disable state of the DQS associated with QUAD2, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 54:55 indicate the disable state of the DQS associated with QUAD3, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register.
56:63	RO	Constant = 0b00000000

Register Name	DP16 DQS Bit Disable RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQS_BIT_DISABLE_RP2_P3_[n]
Address	8000027D07011C3F (SCOM), +0x0400_0000_0000
Description	This register is used to disable each of the eight DQS pins on the DP16. During calibration operations, the hardware sets the bit in this register that corresponds to a pin on the DP16 that failed a calibration step. This register indicates which DQS pins on the DP16 failed a calibration step. This register does not indicate which calibration step failed.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	Bits are grouped in pairs. Bits 48:49, 50:51, 52:53, and 54:55 correspond to the differential DQS bits for each pair. 1 = Indicates that the DQS bits are disabled and do not participate in any calibration steps. Both DQS bits in the pair are set to 1b. 0 = Indicates that the DQS bits are not disabled. Both DQS bits in the pair are set to 0b. Bits 48:49 indicate the disable state of the DQS associated with QUAD0, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 50:51 indicate the disable state of the DQS associated with QUAD1, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 52:53 indicate the disable state of the DQS associated with QUAD2, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 54:55 indicate the disable state of the DQS associated with QUAD3, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register.
56:63	RO	Constant = 0b00000000

Register Name	**DP16 Write DQ Offset Value RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQ_WR_OFFSET_RP2_P0_[n]
Address	8000027E0701103F (SCOM), +0x0400_0000_0000
Description	This register contains an offset value for each quadrant. This offset allows the centered write data bits in each quadrant to be offset from the center as determined by the write-centering calibration algorithm. This register is used by the write-centering calibration state machine. This register must be configured, if needed, before the write-centering calibration algorithm is initiated. Changing the value of this register without running the write-centering calibration algorithm has no effect on the data bit write delay values.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	DQ_WR_OFFSET_N0: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). The least-significant bit of the 5-bit value is always 0b.
52:55	RW	DQ_WR_OFFSET_N1: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). The least-significant bit of the 5-bit value is always 0b.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	DQ_WR_OFFSET_N2: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). The least-significant bit of the 5-bit value is always 0b.
60:63	RW	DQ_WR_OFFSET_N3: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). The least-significant bit of the 5-bit value is always 0b.

Register Name	DP16 Write DQ Offset Value RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQ_WR_OFFSET_RP2_P1_[n]
Address	8000027E0701143F (SCOM), +0x0400_0000_0000
Description	This register contains an offset value for each quadrant. This offset allows the centered write data bits in each quadrant to be offset from the center as determined by the write-centering calibration algorithm. This register is used by the write-centering calibration state machine. This register must be configured, if needed, before the write-centering calibration algorithm is initiated. Changing the value of this register without running the write-centering calibration algorithm has no effect on the data bit write delay values.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	DQ_WR_OFFSET_N0: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). The least-significant bit of the 5-bit value is always 0b.
52:55	RW	DQ_WR_OFFSET_N1: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). The least-significant bit of the 5-bit value is always 0b.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	DQ_WR_OFFSET_N2: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). The least-significant bit of the 5-bit value is always 0b.
60:63	RW	DQ_WR_OFFSET_N3: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). The least-significant bit of the 5-bit value is always 0b.

Register Name	DP16 Write DQ Offset Value RP2 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQ_WR_OFFSET_RP2_P2_[n]
Address	8000027E0701183F (SCOM), +0x0400_0000_0000
Description	This register contains an offset value for each quadrant. This offset allows the centered write data bits in each quadrant to be offset from the center as determined by the write-centering calibration algorithm. This register is used by the write-centering calibration state machine. This register must be configured, if needed, before the write-centering calibration algorithm is initiated. Changing the value of this register without running the write-centering calibration algorithm has no effect on the data bit write delay values.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	DQ_WR_OFFSET_N0: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). The least-significant bit of the 5-bit value is always 0b.
52:55	RW	DQ_WR_OFFSET_N1: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). The least-significant bit of the 5-bit value is always 0b.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	DQ_WR_OFFSET_N2: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). The least-significant bit of the 5-bit value is always 0b.
60:63	RW	DQ_WR_OFFSET_N3: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). The least-significant bit of the 5-bit value is always 0b.

Register Name	**DP16 Write DQ Offset Value RP2 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQ_WR_OFFSET_RP2_P3_[n]
Address	8000027E07011C3F (SCOM), +0x0400_0000_0000
Description	This register contains an offset value for each quadrant. This offset allows the centered write data bits in each quadrant to be offset from the center as determined by the write-centering calibration algorithm. This register is used by the write-centering calibration state machine. This register must be configured, if needed, before the write-centering calibration algorithm is initiated. Changing the value of this register without running the write-centering calibration algorithm has no effect on the data bit write delay values.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	DQ_WR_OFFSET_N0: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). The least-significant bit of the 5-bit value is always 0b.
52:55	RW	DQ_WR_OFFSET_N1: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). The least-significant bit of the 5-bit value is always 0b.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	DQ_WR_OFFSET_N2: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). The least-significant bit of the 5-bit value is always 0b.
60:63	RW	DQ_WR_OFFSET_N3: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). The least-significant bit of the 5-bit value is always 0b.

Register Name	**DP16 Read Clock Enable and Selection RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_CLOCK_RANK_PAIR3_P0_[n]
Address	800003040701103F (SCOM), +0x0400_0000_0000
Description	This register configures which input pins on the DP16 are used as strobes to capture incoming data on which data pins. This register must be configured the same as the DP16 Write Clock Enable and Selection Register. The following are legal configurations on POWER9 for bits 48:53: 110000 = By-8 memory using CLK16. 000011 = By-8 memory using CLK18. 100001 = By-4 memory, not cross-coupled. 010010 = By-4 memory, cross-coupled. 000000 = Byte is not used. Other values are reserved. The following are legal configurations on POWER9 for bits 54:57: 1100 = By-8 memory using CLK20. 0011 = By-8 memory using CLK22. 1001 = By-4 memory, not cross-coupled. 0110 = By-4 memory, cross-coupled. 0000 = Byte is not used. Other values are reserved.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	QUAD0_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an incoming clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.

Bits	SCOM	Field Mnemonic: Description
49	RW	QUAD1_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an incoming clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
50:51	RO	Reserved.
52	RW	QUAD0_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an incoming clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
53	RW	QUAD1_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an incoming clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
54	RW	QUAD2_CLK20: 1 = MEMINTD20B(n) and MEMINTD21B(n) are used as an incoming clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
55	RW	QUAD3_CLK20: 1 = MEMINTD20B(n) and MEMINTD21B(n) are used as an incoming clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
56	RW	QUAD2_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an incoming clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.

Bits	SCOM	Field Mnemonic: Description
57	RW	QUAD3_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an incoming clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
58:63	RO	Reserved.

Register Name	**DP16 Read Clock Enable and Selection RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_CLOCK_RANK_PAIR3_P1_[n]
Address	800003040701143F (SCOM), +0x0400_0000_0000
Description	This register configures which input pins on the DP16 are used as strobes to capture incoming data on which data pins. This register must be configured the same as the DP16 Write Clock Enable and Selection Register. The following are legal configurations on POWER9 for bits 48:53: 110000 = By-8 memory using CLK16. 000011 = By-8 memory using CLK18. 100001 = By-4 memory, not cross-coupled. 010010 = By-4 memory, cross-coupled. 000000 = Byte is not used. Other values are reserved. The following are legal configurations on POWER9 for bits 54:57: 1100 = By-8 memory using CLK20. 0011 = By-8 memory using CLK22. 1001 = By-4 memory, not cross-coupled. 0110 = By-4 memory, cross-coupled. 0000 = Byte is not used. Other values are reserved.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	QUAD0_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an incoming clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
49	RW	QUAD1_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an incoming clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
50:51	RO	Reserved.

Bits	SCOM	Field Mnemonic: Description
52	RW	QUAD0_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an incoming clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
53	RW	QUAD1_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an incoming clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
54	RW	QUAD2_CLK20: 1 = MEMINTD20B(n) and MEMINTD21B(n) are used as an incoming clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
55	RW	QUAD3_CLK20: 1 = MEMINTD20B(n) and MEMINTD21B(n) are used as an incoming clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
56	RW	QUAD2_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an incoming clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
57	RW	QUAD3_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an incoming clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
58:63	RO	Reserved.

Register Name	**DP16 Read Clock Enable and Selection RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_CLOCK_RANK_PAIR3_P2_[n]
Address	800003040701183F (SCOM), +0x0400_0000_0000
Description	This register configures which input pins on the DP16 are used as strobes to capture incoming data on which data pins. This register must be configured the same as the DP16 Write Clock Enable and Selection Register. The following are legal configurations on POWER9 for bits 48:53: 110000 = By-8 memory using CLK16. 000011 = By-8 memory using CLK18. 100001 = By-4 memory, not cross-coupled. 010010 = By-4 memory, cross-coupled. 000000 = Byte is not used. Other values are reserved. The following are legal configurations on POWER9 for bits 54:57: 1100 = By-8 memory using CLK20. 0011 = By-8 memory using CLK22. 1001 = By-4 memory, not cross-coupled. 0110 = By-4 memory, cross-coupled. 0000 = Byte is not used. Other values are reserved.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	QUAD0_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an incoming clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
49	RW	QUAD1_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an incoming clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
50:51	RO	Reserved.
52	RW	QUAD0_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an incoming clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n).. where n is the DP16 instance number.
53	RW	QUAD1_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an incoming clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.

Bits	SCOM	Field Mnemonic: Description
54	RW	QUAD2_CLK20: 1 = MEMINTD20B(n) and MEMINTD21B(n) are used as an incoming clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
55	RW	QUAD3_CLK20: 1 = MEMINTD20B(n) and MEMINTD21B(n) are used as an incoming clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
56	RW	QUAD2_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an incoming clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
57	RW	QUAD3_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an incoming clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
58:63	RO	Reserved.

Register Name	**DP16 Read Clock Enable and Selection RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_CLOCK_RANK_PAIR3_P3_[n]
Address	8000030407011C3F (SCOM), +0x0400_0000_0000
Description	This register configures which input pins on the DP16 are used as strobes to capture incoming data on which data pins. This register must be configured the same as the DP16 Write Clock Enable and Selection Register. The following are legal configurations on POWER9 for bits 48:53: 110000 = By-8 memory using CLK16. 000011 = By-8 memory using CLK18. 100001 = By-4 memory, not cross-coupled. 010010 = By-4 memory, cross-coupled. 000000 = Byte is not used. Other values are reserved. The following are legal configurations on POWER9 for bits 54:57: 1100 = By-8 memory using CLK20. 0011 = By-8 memory using CLK22. 1001 = By-4 memory, not cross-coupled. 0110 = By-4 memory, cross-coupled. 0000 = Byte is not used. Other values are reserved.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	QUAD0_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an incoming clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
49	RW	QUAD1_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an incoming clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
50:51	RO	Reserved.
52	RW	QUAD0_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an incoming clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
53	RW	QUAD1_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an incoming clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
54	RW	QUAD2_CLK20: 1 = MEMINTD20B(n) and MEMINTD21B(n) are used as an incoming clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
55	RW	QUAD3_CLK20: 1 = MEMINTD20B(n) and MEMINTD21B(n) are used as an incoming clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.

Bits	SCOM	Field Mnemonic: Description
56	RW	QUAD2_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an incoming clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
57	RW	QUAD3_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an incoming clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
58:63	RO	Reserved.

Register Name	DP16 Write Clock Enable and Selection RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WRCLK_EN_RP3_P0_[n]
Address	800003050701103F (SCOM), +0x0400_0000_0000
Description	This register configures which output pins on the DP16 are used as clocks or strobes to capture outgoing data on which data pins. This register must be configured exactly the same as the DP16 Read Clock Enable and Selection Register. The following are legal configurations for bits 48:53: 110000 = by-8 memory using CLK16 000011 = by-8 memory using CLK18 100001 = by-4 memory, not cross-coupled 010010 = by-4 memory, cross-coupled 000000 = Byte is not used. Other values are reserved. The following are legal configurations for bits 54:57: 1100 = by-8 memory using CLK20 0011 = by-8 memory using CLK22 1001 = by-4 memory, not cross-coupled 0110 = by-4 memory, cross-coupled 0000 = Byte is not used. Other values are reserved. The same configuration should be loaded for all active ranks.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	QUAD0_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an outgoing clock to capture data on the following pins when the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.

Bits	SCOM	Field Mnemonic: Description
49	RW	QUAD1_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an outgoing clock to capture data on the following pins when the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
50:51	RW	Reserved.
52	RW	QUAD0_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
53	RW	QUAD1_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
54	RW	QUAD2_CLK20: 1 = MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
55	RW	QUAD3_CLK20: 1 = MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
56	RW	QUAD2_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.

Bits	SCOM	Field Mnemonic: Description
57	RW	QUAD3_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
58:63	RW	Reserved.

Register Name	DP16 Write Clock Enable and Selection RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WRCLK_EN_RP3_P1_[n]
Address	800003050701143F (SCOM), +0x0400_0000_0000
Description	This register configures which output pins on the DP16 are used as clocks or strobes to capture outgoing data on which data pins. This register must be configured exactly the same as the DP16 Read Clock Enable and Selection Register. The following are legal configurations for bits 48:53: 110000 = by-8 memory using CLK16 000011 = by-8 memory using CLK18 100001 = by-4 memory, not cross-coupled 010010 = by-4 memory, cross-coupled 000000 = Byte is not used. Other values are reserved. The following are legal configurations for bits 54:57: 1100 = by-8 memory using CLK20 0011 = by-8 memory using CLK22 1001 = by-4 memory, not cross-coupled 0110 = by-4 memory, cross-coupled 0000 = Byte is not used. Other values are reserved. The same configuration should be loaded for all active ranks.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48	RW	QUAD0_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an outgoing clock to capture data on the following pins when the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
49	RW	QUAD1_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an outgoing clock to capture data on the following pins when the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
50:51	RW	Reserved.

Bits	SCOM	Field Mnemonic: Description
52	RW	QUAD0_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
53	RW	QUAD1_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
54	RW	QUAD2_CLK20: 1 = MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
55	RW	QUAD3_CLK20: 1 = MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
56	RW	QUAD2_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
57	RW	QUAD3_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
58:63	RW	Reserved.

Register Name	**DP16 Write Clock Enable and Selection RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_WRCLK_EN_RP3_P2_[n]
Address	800003050701183F (SCOM), +0x0400_0000_0000
Description	This register configures which output pins on the DP16 are used as clocks or strobes to capture outgoing data on which data pins. This register must be configured exactly the same as the DP16 Read Clock Enable and Selection Register. The following are legal configurations for bits 48:53: 110000 = by-8 memory using CLK16 000011 = by-8 memory using CLK18 100001 = by-4 memory, not cross-coupled 010010 = by-4 memory, cross-coupled 000000 = Byte is not used. Other values are reserved. The following are legal configurations for bits 54:57: 1100 = by-8 memory using CLK20 0011 = by-8 memory using CLK22 1001 = by-4 memory, not cross-coupled 0110 = by-4 memory, cross-coupled 0000 = Byte is not used. Other values are reserved. The same configuration should be loaded for all active ranks.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	QUAD0_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an outgoing clock to capture data on the following pins when the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
49	RW	QUAD1_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an outgoing clock to capture data on the following pins when the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
50:51	RW	Reserved.
52	RW	QUAD0_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.

Bits	SCOM	Field Mnemonic: Description
53	RW	QUAD1_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
54	RW	QUAD2_CLK20: 1 = MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
55	RW	QUAD3_CLK20: 1 = MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
56	RW	QUAD2_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
57	RW	QUAD3_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
58:63	RW	Reserved.

Register Name	DP16 Write Clock Enable and Selection RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WRCLK_EN_RP3_P3_[n]
Address	8000030507011C3F (SCOM), +0x0400_0000_0000
Description	This register configures which output pins on the DP16 are used as clocks or strobes to capture outgoing data on which data pins. This register must be configured exactly the same as the DP16 Read Clock Enable and Selection Register. The following are legal configurations for bits 48:53: 110000 = by-8 memory using CLK16 000011 = by-8 memory using CLK18 100001 = by-4 memory, not cross-coupled 010010 = by-4 memory, cross-coupled 000000 = Byte is not used. Other values are reserved. The following are legal configurations for bits 54:57: 1100 = by-8 memory using CLK20 0011 = by-8 memory using CLK22 1001 = by-4 memory, not cross-coupled 0110 = by-4 memory, cross-coupled 0000 = Byte is not used. Other values are reserved. The same configuration should be loaded for all active ranks.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	QUAD0_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an outgoing clock to capture data on the following pins when the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.
49	RW	QUAD1_CLK16: 1 = MEMINTD16B(n) and MEMINTD17B(n) are used as an outgoing clock to capture data on the following pins when the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
50:51	RW	Reserved.
52	RW	QUAD0_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). where n is the DP16 instance number.

Bits	SCOM	Field Mnemonic: Description
53	RW	QUAD1_CLK18: 1 = MEMINTD18B(n) and MEMINTD19B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). where n is the DP16 instance number.
54	RW	QUAD2_CLK20: 1 = MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
55	RW	QUAD3_CLK20: 1 = MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
56	RW	QUAD2_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). where n is the DP16 instance number.
57	RW	QUAD3_CLK22: 1 = MEMINTD22B(n) and MEMINTD23B(n) are used as an outgoing clock to capture data on the following pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). where n is the DP16 instance number.
58:63	RW	Reserved.

Register Name	DP16 DQS Read Phase Select RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_[n]
Address	800003090701103F (SCOM), +0x0400_0000_0000
Description	This register contains a dynamic value that represents the phase differences between the memory clock, strobes, and the receiver clocks. Hardware determines these values during initial calibration and maintains them during periodic calibrations. One register stores phase selects for each rank pair for a total of four registers. This register is provided for diagnostic use. Do not use software to write to this register during normal use.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RW	DQSCLK_SELECT0: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03.
50:51	RW	RDCLK_SELECT0: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03.
52:53	RW	DQSCLK_SELECT1: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07.
54:55	RW	RDCLK_SELECT1: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07.
56:57	RW	DQSCLK_SELECT2: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11.
58:59	RW	RDCLK_SELECT2: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11.
60:61	RW	DQSCLK_SELECT3: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15.
62:63	RW	RDCLK_SELECT3: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15.

Register Name	**DP16 DQS Read Phase Select RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_[n]
Address	800003090701143F (SCOM), +0x0400_0000_0000
Description	This register contains a dynamic value that represents the phase differences between the memory clock, strobes, and the receiver clocks. Hardware determines these values during initial calibration and maintains them during periodic calibrations. One register stores phase selects for each rank pair for a total of four registers. This register is provided for diagnostic use. Do not use software to write to this register during normal use.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:49	RW	DQSCLK_SELECT0: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03.
50:51	RW	RDCLK_SELECT0: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03.
52:53	RW	DQSCLK_SELECT1: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07.
54:55	RW	RDCLK_SELECT1: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07.
56:57	RW	DQSCLK_SELECT2: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11.
58:59	RW	RDCLK_SELECT2: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11.
60:61	RW	DQSCLK_SELECT3: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15.
62:63	RW	RDCLK_SELECT3: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15.

Register Name	DP16 DQS Read Phase Select RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQS_RD_PHASE_SELECT_RANK_PAIR3_P2_[n]
Address	800003090701183F (SCOM), +0x0400_0000_0000
Description	This register contains a dynamic value that represents the phase differences between the memory clock, strobes, and the receiver clocks. Hardware determines these values during initial calibration and maintains them during periodic calibrations. One register stores phase selects for each rank pair for a total of four registers. This register is provided for diagnostic use. Do not use software to write to this register during normal use.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:49	RW	DQSCLK_SELECT0: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03.
50:51	RW	RDCLK_SELECT0: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03.
52:53	RW	DQSCLK_SELECT1: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07.
54:55	RW	RDCLK_SELECT1: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07.
56:57	RW	DQSCLK_SELECT2: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11.
58:59	RW	RDCLK_SELECT2: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11.
60:61	RW	DQSCLK_SELECT3: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15.
62:63	RW	RDCLK_SELECT3: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15.

Register Name	DP16 DQS Read Phase Select RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQS_RD_PHASE_SELECT_RANK_PAIR3_P3_[n]
Address	8000030907011C3F (SCOM), +0x0400_0000_0000
Description	This register contains a dynamic value that represents the phase differences between the memory clock, strobes, and the receiver clocks. Hardware determines these values during initial calibration and maintains them during periodic calibrations. One register stores phase selects for each rank pair for a total of four registers. This register is provided for diagnostic use. Do not use software to write to this register during normal use.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:49	RW	DQSCLK_SELECT0: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03.
50:51	RW	RDCLK_SELECT0: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03.
52:53	RW	DQSCLK_SELECT1: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07.
54:55	RW	RDCLK_SELECT1: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07.

Bits	SCOM	Field Mnemonic: Description
56:57	RW	DQSCLK_SELECT2: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11.
58:59	RW	RDCLK_SELECT2: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11.
60:61	RW	DQSCLK_SELECT3: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15.
62:63	RW	RDCLK_SELECT3: This field contains the phase select for the MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15.

Register Name	**DP16 Read Delay Offset 0 RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY_OFFSET0_RANK_PAIR3_P0_[n]
Address	8000030C0701103F (SCOM), +0x0400_0000_0000
Description	Each register field holds the read delay offsets for four of the MEMINTDnnB pins for one rank pair in the DP16.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	OFFSET0: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03 and nn{1} = 08, 09, 10, 11. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.
56	RO	Constant = 0b0
57:63	RW	OFFSET1: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07 and nn{1} = 12, 13, 14, 15. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.

Register Name	**DP16 Read Delay Offset 0 RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY_OFFSET0_RANK_PAIR3_P1_[n]
Address	8000030C0701143F (SCOM), +0x0400_0000_0000
Description	Each register field holds the read delay offsets for four of the MEMINTDnnB pins for one rank pair in the DP16.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	OFFSET0: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03 and nn{1} = 08, 09, 10, 11. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.
56	RO	Constant = 0b0

Bits	SCOM	Field Mnemonic: Description
57:63	RW	OFFSET1: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07 and nn{1} = 12, 13, 14, 15. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.

Register Name	**DP16 Read Delay Offset 0 RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY_OFFSET0_RANK_PAIR3_P2_[n]
Address	8000030C0701183F (SCOM), +0x0400_0000_0000
Description	Each register field holds the read delay offsets for four of the MEMINTDnnB pins for one rank pair in the DP16.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	OFFSET0: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03 and nn{1} = 08, 09, 10, 11. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.
56	RO	Constant = 0b0
57:63	RW	OFFSET1: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07 and nn{1} = 12, 13, 14, 15. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.

Register Name	**DP16 Read Delay Offset 0 RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY_OFFSET0_RANK_PAIR3_P3_[n]
Address	8000030C07011C3F (SCOM), +0x0400_0000_0000
Description	Each register field holds the read delay offsets for four of the MEMINTDnnB pins for one rank pair in the DP16.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	OFFSET0: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03 and nn{1} = 08, 09, 10, 11. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.
56	RO	Constant = 0b0

Bits	SCOM	Field Mnemonic: Description
57:63	RW	OFFSET1: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07 and nn{1} = 12, 13, 14, 15. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.

Register Name	**DP16 Read Delay Offset 1 RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY_OFFSET1_RANK_PAIR3_P0_[n]
Address	8000030D0701103F (SCOM), +0x0400_0000_0000
Description	Each register field holds the read delay offsets for four of the MEMINTDnnB pins for one rank pair in the DP16.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	OFFSET2: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03 and nn{1} = 08, 09, 10, 11. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.
56	RO	Constant = 0b0
57:63	RW	OFFSET3: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07 and nn{1} = 12, 13, 14, 15. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.

Register Name	**DP16 Read Delay Offset 1 RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY_OFFSET1_RANK_PAIR3_P1_[n]
Address	8000030D0701143F (SCOM), +0x0400_0000_0000
Description	Each register field holds the read delay offsets for four of the MEMINTDnnB pins for one rank pair in the DP16.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	OFFSET2: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03 and nn{1} = 08, 09, 10, 11. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.
56	RO	Constant = 0b0

Bits	SCOM	Field Mnemonic: Description
57:63	RW	OFFSET3: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07 and nn{1} = 12, 13, 14, 15. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.

Register Name	**DP16 Read Delay Offset 1 RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY_OFFSET1_RANK_PAIR3_P2_[n]
Address	8000030D0701183F (SCOM), +0x0400_0000_0000
Description	Each register field holds the read delay offsets for four of the MEMINTDnnB pins for one rank pair in the DP16.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	OFFSET2: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03 and nn{1} = 08, 09, 10, 11. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.
56	RO	Constant = 0b0
57:63	RW	OFFSET3: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07 and nn{1} = 12, 13, 14, 15. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.

Register Name	**DP16 Read Delay Offset 1 RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY_OFFSET1_RANK_PAIR3_P3_[n]
Address	8000030D07011C3F (SCOM), +0x0400_0000_0000
Description	Each register field holds the read delay offsets for four of the MEMINTDnnB pins for one rank pair in the DP16.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	OFFSET2: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03 and nn{1} = 08, 09, 10, 11. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.
56	RO	Constant = 0b0

Bits	SCOM	Field Mnemonic: Description
57:63	RW	OFFSET3: This field holds the read delay offset for the MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07 and nn{1} = 12, 13, 14, 15. This value can be written via the programming interface. It is stored in twos complement form; therefore, the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register must not be set to a nonzero value unless detailed timing analysis shows that, for a particular configuration, the read-centering algorithm places the sampling point off from the eye center.

Register Name	**DP16 DQS Gate Delay RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQS_GATE_DELAY_RP3_P0_[n]
Address	800003130701103F (SCOM), +0x0400_0000_0000
Description	This register contains the DQS gate delay settings for each incoming read clock. One register exists for each rank pair. This register must be reset or written to its reset value before running or rerunning initial calibration.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:51	RW	DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00 - DQ03 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
52	RO	Constant = 0b0
53:55	RW	DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04 - DQ07 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
56	RO	Constant = 0b0
57:59	RW	DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08 - DQ11 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
60	RO	Constant = 0b0
61:63	RW	DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12 - DQ15 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.

Register Name	**DP16 DQS Gate Delay RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQS_GATE_DELAY_RP3_P1_[n]
Address	800003130701143F (SCOM), +0x0400_0000_0000
Description	This register contains the DQS gate delay settings for each incoming read clock. One register exists for each rank pair. This register must be reset or written to its reset value before running or rerunning initial calibration.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:51	RW	DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00 - DQ03 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
52	RO	Constant = 0b0
53:55	RW	DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04 - DQ07 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
56	RO	Constant = 0b0
57:59	RW	DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08 - DQ11 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
60	RO	Constant = 0b0
61:63	RW	DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12 - DQ15 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.

Register Name	**DP16 DQS Gate Delay RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQS_GATE_DELAY_RP3_P2_[n]
Address	800003130701183F (SCOM), +0x0400_0000_0000
Description	This register contains the DQS gate delay settings for each incoming read clock. One register exists for each rank pair. This register must be reset or written to its reset value before running or rerunning initial calibration.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:51	RW	DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00 - DQ03 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
52	RO	Constant = 0b0
53:55	RW	DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04 - DQ07 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
56	RO	Constant = 0b0
57:59	RW	DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08 - DQ11 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.

Bits	SCOM	Field Mnemonic: Description
60	RO	Constant = 0b0
61:63	RW	DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12 - DQ15 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.

Register Name	**DP16 DQS Gate Delay RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQS_GATE_DELAY_RP3_P3_[n]
Address	8000031307011C3F (SCOM), +0x0400_0000_0000
Description	This register contains the DQS gate delay settings for each incoming read clock. One register exists for each rank pair. This register must be reset or written to its reset value before running or rerunning initial calibration.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:51	RW	DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00 - DQ03 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
52	RO	Constant = 0b0
53:55	RW	DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04 - DQ07 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
56	RO	Constant = 0b0
57:59	RW	DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08 - DQ11 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.
60	RO	Constant = 0b0
61:63	RW	DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12 - DQ15 inputs. This field determines when the read gate is opened. It contains the number of MEMINTCLKO clock cycles. ‘0’h to ‘5’h = 0 - 5 MEMINTCLKO clock cycles. ‘6’h to ‘7’h = Unused.

Register Name	**DP16 DQSClk Phase Rotator Value 0 RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQSCLK_PR0_RANK_PAIR3_P0_[n]
Address	800003300701103F (SCOM), +0x0400_0000_0000
Description	Two phase rotator values are contained within each register. Two registers exist for each rank pair. These phase rotator values are the values needed to align the internal SysClk to the incoming DQS strobe for each group of data pins.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	DQSCLK_ROT_CLK_N0: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD00B – MEMINTD03B in register 0 and MEMINTD08B – MEMINTD11B in register 1. This value is updated by hardware.
56	RO	Constant = 0b0
57:63	RW	DQSCLK_ROT_CLK_N1: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINTD15B in register 1. This value is updated by hardware.

Register Name	DP16 DQSClk Phase Rotator Value 0 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQSCLK_PR0_RANK_PAIR3_P1_[n]
Address	800003300701143F (SCOM), +0x0400_0000_0000
Description	Two phase rotator values are contained within each register. Two registers exist for each rank pair. These phase rotator values are the values needed to align the internal SysClk to the incoming DQS strobe for each group of data pins.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	DQSCLK_ROT_CLK_N0: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD00B – MEMINTD03B in register 0 and MEMINTD08B – MEMINTD11B in register 1. This value is updated by hardware.
56	RO	Constant = 0b0
57:63	RW	DQSCLK_ROT_CLK_N1: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINTD15B in register 1. This value is updated by hardware.

Register Name	DP16 DQSClk Phase Rotator Value 0 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQSCLK_PR0_RANK_PAIR3_P2_[n]
Address	800003300701183F (SCOM), +0x0400_0000_0000
Description	Two phase rotator values are contained within each register. Two registers exist for each rank pair. These phase rotator values are the values needed to align the internal SysClk to the incoming DQS strobe for each group of data pins.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	DQSCLK_ROT_CLK_N0: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD00B – MEMINTD03B in register 0 and MEMINTD08B – MEMINTD11B in register 1. This value is updated by hardware.
56	RO	Constant = 0b0
57:63	RW	DQSCLK_ROT_CLK_N1: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINTD15B in register 1. This value is updated by hardware.

Register Name	DP16 DQSClk Phase Rotator Value 0 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQSCLK_PR0_RANK_PAIR3_P3_[n]
Address	8000033007011C3F (SCOM), +0x0400_0000_0000
Description	Two phase rotator values are contained within each register. Two registers exist for each rank pair. These phase rotator values are the values needed to align the internal SysClk to the incoming DQS strobe for each group of data pins.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	DQSCLK_ROT_CLK_N0: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD00B – MEMINTD03B in register 0 and MEMINTD08B – MEMINTD11B in register 1. This value is updated by hardware.
56	RO	Constant = 0b0
57:63	RW	DQSCLK_ROT_CLK_N1: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINTD15B in register 1. This value is updated by hardware.

Register Name	DP16 DQSClk Phase Rotator Value 1 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQSCLK_PR1_RANK_PAIR3_P0_[n]
Address	800003310701103F (SCOM), +0x0400_0000_0000
Description	Two phase rotator values are contained within each register. Two registers exist for each rank pair. These phase rotator values are the values needed to align the internal SysClk to the incoming DQS strobe for each group of data pins.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	DQSCLK_ROT_CLK_N2: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD00B – MEMINTD03B in register 0 and MEMINTD08B – MEMINTD11B in register 1. This value is updated by hardware.
56	RO	Constant = 0b0
57:63	RW	DQSCLK_ROT_CLK_N3: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINTD15B in register 1. This value is updated by hardware.

Register Name	DP16 DQSClk Phase Rotator Value 1 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQSCLK_PR1_RANK_PAIR3_P1_[n]
Address	800003310701143F (SCOM), +0x0400_0000_0000
Description	Two phase rotator values are contained within each register. Two registers exist for each rank pair. These phase rotator values are the values needed to align the internal SysClk to the incoming DQS strobe for each group of data pins.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	DQSCLK_ROT_CLK_N2: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD00B – MEMINTD03B in register 0 and MEMINTD08B – MEMINTD11B in register 1. This value is updated by hardware.

Bits	SCOM	Field Mnemonic: Description
56	RO	Constant = 0b0
57:63	RW	DQSCLK_ROT_CLK_N3: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINTD15B in register 1. This value is updated by hardware.

Register Name	**DP16 DQSClk Phase Rotator Value 1 RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQSCLK_PR1_RANK_PAIR3_P2_[n]
Address	800003310701183F (SCOM), +0x0400_0000_0000
Description	Two phase rotator values are contained within each register. Two registers exist for each rank pair. These phase rotator values are the values needed to align the internal SysClk to the incoming DQS strobe for each group of data pins.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	DQSCLK_ROT_CLK_N2: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD00B – MEMINTD03B in register 0 and MEMINTD08B – MEMINTD11B in register 1. This value is updated by hardware.
56	RO	Constant = 0b0
57:63	RW	DQSCLK_ROT_CLK_N3: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINTD15B in register 1. This value is updated by hardware.

Register Name	**DP16 DQSClk Phase Rotator Value 1 RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQSCLK_PR1_RANK_PAIR3_P3_[n]
Address	8000033107011C3F (SCOM), +0x0400_0000_0000
Description	Two phase rotator values are contained within each register. Two registers exist for each rank pair. These phase rotator values are the values needed to align the internal SysClk to the incoming DQS strobe for each group of data pins.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RW	DQSCLK_ROT_CLK_N2: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD00B – MEMINTD03B in register 0 and MEMINTD08B – MEMINTD11B in register 1. This value is updated by hardware.
56	RO	Constant = 0b0
57:63	RW	DQSCLK_ROT_CLK_N3: This field contains the DQS clock rotator value used to align the SysClk to the incoming DQS strobe for DQ pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINTD15B in register 1. This value is updated by hardware.

Register Name	DP16 Write Delay Value 0 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_0_RP3_REG_P0_[n]
Address	800003380701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 0 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_0_RP3_REG_P1_[n]
Address	800003380701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 0 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_0_RP3_REG_P2_[n]
Address	800003380701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 0 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_0_RP3_REG_P3_[n]
Address	8000033807011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 1 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_1_RP3_REG_P0_[n]
Address	800003390701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 1 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_1_RP3_REG_P1_[n]
Address	800003390701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 1 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_1_RP3_REG_P2_[n]
Address	800003390701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 1 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_1_RP3_REG_P3_[n]
Address	8000033907011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 2 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_2_RP3_REG_P0_[n]
Address	8000033A0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 2 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_2_RP3_REG_P1_[n]
Address	8000033A0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 2 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_2_RP3_REG_P2_[n]
Address	8000033A0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 2 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_2_RP3_REG_P3_[n]
Address	8000033A07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 3 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_3_RP3_REG_P0_[n]
Address	8000033B0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 3 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_3_RP3_REG_P1_[n]
Address	8000033B0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 3 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_3_RP3_REG_P2_[n]
Address	8000033B0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 3 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_3_RP3_REG_P3_[n]
Address	8000033B07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 4 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_4_RP3_REG_P0_[n]
Address	8000033C0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 4 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_4_RP3_REG_P1_[n]
Address	8000033C0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	**DP16 Write Delay Value 4 RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_4_RP3_REG_P2_[n]
Address	8000033C0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	**DP16 Write Delay Value 4 RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_4_RP3_REG_P3_[n]
Address	8000033C07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 5 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_5_RP3_REG_P0_[n]
Address	8000033D0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 5 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_5_RP3_REG_P1_[n]
Address	8000033D0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 5 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_5_RP3_REG_P2_[n]
Address	8000033D0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 5 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_5_RP3_REG_P3_[n]
Address	8000033D07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 6 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_6_RP3_REG_P0_[n]
Address	8000033E0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 6 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_6_RP3_REG_P1_[n]
Address	8000033E0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 6 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_6_RP3_REG_P2_[n]
Address	8000033E0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 6 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_6_RP3_REG_P3_[n]
Address	8000033E07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 7 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_7_RP3_REG_P0_[n]
Address	8000033F0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 7 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_7_RP3_REG_P1_[n]
Address	8000033F0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 7 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_7_RP3_REG_P2_[n]
Address	8000033F0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 7 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_7_RP3_REG_P3_[n]
Address	8000033F07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 8 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_8_RP3_REG_P0_[n]
Address	800003400701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 8 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_8_RP3_REG_P1_[n]
Address	800003400701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 8 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_8_RP3_REG_P2_[n]
Address	800003400701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 8 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_8_RP3_REG_P3_[n]
Address	8000034007011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 9 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_9_RP3_REG_P0_[n]
Address	800003410701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 9 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_9_RP3_REG_P1_[n]
Address	800003410701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 9 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_9_RP3_REG_P2_[n]
Address	800003410701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 9 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_9_RP3_REG_P3_[n]
Address	8000034107011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 10 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_10_RP3_REG_P0_[n]
Address	800003420701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 10 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_10_RP3_REG_P1_[n]
Address	800003420701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 10 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_10_RP3_REG_P2_[n]
Address	800003420701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 10 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_10_RP3_REG_P3_[n]
Address	8000034207011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 11 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_11_RP3_REG_P0_[n]
Address	800003430701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 11 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_11_RP3_REG_P1_[n]
Address	800003430701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 11 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_11_RP3_REG_P2_[n]
Address	800003430701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 11 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_11_RP3_REG_P3_[n]
Address	8000034307011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 12 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_12_RP3_REG_P0_[n]
Address	800003440701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 12 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_12_RP3_REG_P1_[n]
Address	800003440701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 12 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_12_RP3_REG_P2_[n]
Address	800003440701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 12 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_12_RP3_REG_P3_[n]
Address	8000034407011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 13 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_13_RP3_REG_P0_[n]
Address	800003450701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 13 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_13_RP3_REG_P1_[n]
Address	800003450701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 13 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_13_RP3_REG_P2_[n]
Address	800003450701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 13 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_13_RP3_REG_P3_[n]
Address	8000034507011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 14 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_14_RP3_REG_P0_[n]
Address	800003460701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 14 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_14_RP3_REG_P1_[n]
Address	800003460701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 14 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_14_RP3_REG_P2_[n]
Address	800003460701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 14 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_14_RP3_REG_P3_[n]
Address	8000034607011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 15 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_15_RP3_REG_P0_[n]
Address	800003470701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 15 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_15_RP3_REG_P1_[n]
Address	800003470701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 15 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_15_RP3_REG_P2_[n]
Address	800003470701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 15 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_15_RP3_REG_P3_[n]
Address	8000034707011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 16 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_16_RP3_REG_P0_[n]
Address	800003480701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 16 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_16_RP3_REG_P1_[n]
Address	800003480701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 16 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_16_RP3_REG_P2_[n]
Address	800003480701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 16 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_16_RP3_REG_P3_[n]
Address	8000034807011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 18 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_18_RP3_REG_P0_[n]
Address	8000034A0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 18 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_18_RP3_REG_P1_[n]
Address	8000034A0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 18 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_18_RP3_REG_P2_[n]
Address	8000034A0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 18 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_18_RP3_REG_P3_[n]
Address	8000034A07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 20 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_20_RP3_REG_P0_[n]
Address	8000034C0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 20 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_20_RP3_REG_P1_[n]
Address	8000034C0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 20 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_20_RP3_REG_P2_[n]
Address	8000034C0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 20 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_20_RP3_REG_P3_[n]
Address	8000034C07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 22 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_22_RP3_REG_P0_[n]
Address	8000034E0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 22 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_22_RP3_REG_P1_[n]
Address	8000034E0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 22 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_22_RP3_REG_P2_[n]
Address	8000034E0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Write Delay Value 22 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_DELAY_VALUE_22_RP3_REG_P3_[n]
Address	8000034E07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the write delay values for one of the MEMINTDnnB pins for one rank pair within the DP16. The write-leveling calibration algorithms write this register. The write-leveling algorithm does not reset this register. The write eye-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:57	RW	WR_DELAY: This field contains the write delay for the MEMINTD{0-23}B pin. This value can be written via the programming interface or determined by the write eye-centering algorithm. This value is used to determine the final write phase rotator value for the given DP16 pin. The valid range of values for this field is 0 - 1FFh, which represents WR_DELAY/128 memory clock cycles of delay. These registers must be reset before running or rerunning the initial calibration. Refer to the EN_RESET_WR_DELAY_WL bit in the WC Configuration 2 Register. If this value is written via the programming interface, bit 0 must be set to 0.
58:63	RO	Constant = 0b000000

Register Name	DP16 Read Delay Value 0 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY0_RANK_PAIR3_P0_[n]
Address	800003500701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 0 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY0_RANK_PAIR3_P1_[n]
Address	800003500701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.

Bits	SCOM	Field Mnemonic: Description
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 0 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY0_RANK_PAIR3_P2_[n]
Address	800003500701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 0 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY0_RANK_PAIR3_P3_[n]
Address	8000035007011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	**DP16 Read Delay Value 1 RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY1_RANK_PAIR3_P0_[n]
Address	800003510701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	**DP16 Read Delay Value 1 RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY1_RANK_PAIR3_P1_[n]
Address	800003510701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 1 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY1_RANK_PAIR3_P2_[n]
Address	800003510701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 1 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY1_RANK_PAIR3_P3_[n]
Address	8000035107011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 2 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY2_RANK_PAIR3_P0_[n]
Address	800003520701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.

Bits	SCOM	Field Mnemonic: Description
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 2 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY2_RANK_PAIR3_P1_[n]
Address	800003520701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 2 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY2_RANK_PAIR3_P2_[n]
Address	800003520701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	**DP16 Read Delay Value 2 RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY2_RANK_PAIR3_P3_[n]
Address	8000035207011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	**DP16 Read Delay Value 3 RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY3_RANK_PAIR3_P0_[n]
Address	800003530701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 3 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY3_RANK_PAIR3_P1_[n]
Address	800003530701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 3 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY3_RANK_PAIR3_P2_[n]
Address	800003530701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 3 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY3_RANK_PAIR3_P3_[n]
Address	8000035307011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.

Bits	SCOM	Field Mnemonic: Description
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 4 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY4_RANK_PAIR3_P0_[n]
Address	800003540701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 4 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY4_RANK_PAIR3_P1_[n]
Address	800003540701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	**DP16 Read Delay Value 4 RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY4_RANK_PAIR3_P2_[n]
Address	800003540701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	**DP16 Read Delay Value 4 RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY4_RANK_PAIR3_P3_[n]
Address	8000035407011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 5 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY5_RANK_PAIR3_P0_[n]
Address	800003550701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 5 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY5_RANK_PAIR3_P1_[n]
Address	800003550701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 5 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY5_RANK_PAIR3_P2_[n]
Address	800003550701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.

Bits	SCOM	Field Mnemonic: Description
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 5 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY5_RANK_PAIR3_P3_[n]
Address	8000035507011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 6 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY6_RANK_PAIR3_P0_[n]
Address	8000035607011103F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	**DP16 Read Delay Value 6 RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY6_RANK_PAIR3_P1_[n]
Address	800003560701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	**DP16 Read Delay Value 6 RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY6_RANK_PAIR3_P2_[n]
Address	800003560701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 6 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY6_RANK_PAIR3_P3_[n]
Address	8000035607011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 7 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY7_RANK_PAIR3_P0_[n]
Address	800003570701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 7 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY7_RANK_PAIR3_P1_[n]
Address	800003570701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.

Bits	SCOM	Field Mnemonic: Description
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 7 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY7_RANK_PAIR3_P2_[n]
Address	800003570701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	DP16 Read Delay Value 7 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_DELAY7_RANK_PAIR3_P3_[n]
Address	8000035707011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read delay values for two of the MEMINTDnnB pins for one rank pair within the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:54	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	Constant = 0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	RD_DELAY: This field holds the read delay for the MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface or determined by the read-centering algorithm. This value is used to determine the final read phase rotator value for the given DP16 pin. If a calibration algorithm that modifies this field sets the corresponding disable bit in the DP16 DQ Bit Disable and DP16 DQS Bit Disable Registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	Constant = 0b0

Register Name	**DP16 Initial DQS Alignment 0 RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN0_RANK_PAIR3_P0_[n]
Address	8000035C0701103F (SCOM), +0x0400_0000_0000
Description	These registers hold the DQSClk phase rotator values computed by initial calibration, They are updated at multiple times during the calibration. Periodic DQS alignment uses the values to compare against for determining long-term drift.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RO	INITIAL_DQS_ROT_N0: This field holds the initial DQSClk rotator value for pins MEMINTD00B - MEMINTD03B in register 0 and MEMINTD08B - MEMINGTD11B in register 1. This value is updated by hardware.
56	RO	Reserved.
57:63	RO	INITIAL_DQS_ROT_N1: This field holds the initial DQSClk rotator value for pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINGTD15B in register 1.This value is updated by hardware.

Register Name	**DP16 Initial DQS Alignment 0 RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN0_RANK_PAIR3_P1_[n]
Address	8000035C0701143F (SCOM), +0x0400_0000_0000
Description	These registers hold the DQSClk phase rotator values computed by initial calibration, They are updated at multiple times during the calibration. Periodic DQS alignment uses the values to compare against for determining long-term drift.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RO	INITIAL_DQS_ROT_N0: This field holds the initial DQSClk rotator value for pins MEMINTD00B - MEMINTD03B in register 0 and MEMINTD08B - MEMINGTD11B in register 1. This value is updated by hardware.
56	RO	Reserved.
57:63	RO	INITIAL_DQS_ROT_N1: This field holds the initial DQSClk rotator value for pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINGTD15B in register 1.This value is updated by hardware.

Register Name	DP16 Initial DQS Alignment 0 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN0_RANK_PAIR3_P2_[n]
Address	8000035C0701183F (SCOM), +0x0400_0000_0000
Description	These registers hold the DQSClk phase rotator values computed by initial calibration, They are updated at multiple times during the calibration. Periodic DQS alignment uses the values to compare against for determining long-term drift.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RO	INITIAL_DQS_ROT_N0: This field holds the initial DQSClk rotator value for pins MEMINTD00B - MEMINTD03B in register 0 and MEMINTD08B - MEMINGTD11B in register 1. This value is updated by hardware.
56	RO	Reserved.
57:63	RO	INITIAL_DQS_ROT_N1: This field holds the initial DQSClk rotator value for pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINGTD15B in register 1.This value is updated by hardware.

Register Name	DP16 Initial DQS Alignment 0 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN0_RANK_PAIR3_P3_[n]
Address	8000035C07011C3F (SCOM), +0x0400_0000_0000
Description	These registers hold the DQSClk phase rotator values computed by initial calibration, They are updated at multiple times during the calibration. Periodic DQS alignment uses the values to compare against for determining long-term drift.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RO	INITIAL_DQS_ROT_N0: This field holds the initial DQSClk rotator value for pins MEMINTD00B - MEMINTD03B in register 0 and MEMINTD08B - MEMINGTD11B in register 1. This value is updated by hardware.
56	RO	Reserved.
57:63	RO	INITIAL_DQS_ROT_N1: This field holds the initial DQSClk rotator value for pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINGTD15B in register 1.This value is updated by hardware.

Register Name	DP16 Initial DQS Alignment 1 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN1_RANK_PAIR3_P0_[n]
Address	8000035D0701103F (SCOM), +0x0400_0000_0000
Description	These registers hold the DQSClk phase rotator values computed by initial calibration, They are updated at multiple times during the calibration. Periodic DQS alignment uses the values to compare against for determining long-term drift.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RO	INITIAL_DQS_ROT_N2: This field holds the initial DQSClk rotator value for pins MEMINTD00B - MEMINTD03B in register 0 and MEMINTD08B - MEMINGTD11B in register 1. This value is updated by hardware.

Bits	SCOM	Field Mnemonic: Description
56	RO	Constant = 0b0
57:63	RO	INITIAL_DQS_ROT_N3: This field holds the initial DQSClk rotator value for pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINGTD15B in register 1.This value is updated by hardware.

Register Name	DP16 Initial DQS Alignment 1 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN1_RANK_PAIR3_P1_[n]
Address	8000035D0701143F (SCOM), +0x0400_0000_0000
Description	These registers hold the DQSClk phase rotator values computed by initial calibration, They are updated at multiple times during the calibration. Periodic DQS alignment uses the values to compare against for determining long-term drift.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RO	INITIAL_DQS_ROT_N2: This field holds the initial DQSClk rotator value for pins MEMINTD00B - MEMINTD03B in register 0 and MEMINTD08B - MEMINGTD11B in register 1. This value is updated by hardware.
56	RO	Constant = 0b0
57:63	RO	INITIAL_DQS_ROT_N3: This field holds the initial DQSClk rotator value for pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINGTD15B in register 1.This value is updated by hardware.

Register Name	DP16 Initial DQS Alignment 1 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN1_RANK_PAIR3_P2_[n]
Address	8000035D0701183F (SCOM), +0x0400_0000_0000
Description	These registers hold the DQSClk phase rotator values computed by initial calibration, They are updated at multiple times during the calibration. Periodic DQS alignment uses the values to compare against for determining long-term drift.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RO	INITIAL_DQS_ROT_N2: This field holds the initial DQSClk rotator value for pins MEMINTD00B - MEMINTD03B in register 0 and MEMINTD08B - MEMINGTD11B in register 1. This value is updated by hardware.
56	RO	Constant = 0b0
57:63	RO	INITIAL_DQS_ROT_N3: This field holds the initial DQSClk rotator value for pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINGTD15B in register 1.This value is updated by hardware.

Register Name	DP16 Initial DQS Alignment 1 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_INITIAL_DQS_ALIGN1_RANK_PAIR3_P3_[n]
Address	8000035D07011C3F (SCOM), +0x0400_0000_0000
Description	These registers hold the DQSClk phase rotator values computed by initial calibration, They are updated at multiple times during the calibration. Periodic DQS alignment uses the values to compare against for determining long-term drift.

Bits	SCOM	Field Mnemonic: Description
0:48	RO	Constant = 0b000000000000000000000000000000000000000000000000
49:55	RO	INITIAL_DQS_ROT_N2: This field holds the initial DQSClk rotator value for pins MEMINTD00B - MEMINTD03B in register 0 and MEMINTD08B - MEMINGTD11B in register 1. This value is updated by hardware.
56	RO	Constant = 0b0
57:63	RO	INITIAL_DQS_ROT_N3: This field holds the initial DQSClk rotator value for pins MEMINTD04B - MEMINTD07B in register 0 and MEMINTD12B - MEMINGTD15B in register 1.This value is updated by hardware.

Register Name	DP16 Write VREF Value 0 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_VALUE0_RANK_PAIR3_P0_[n]
Address	8000035E0701103F (SCOM), +0x0400_0000_0000
Description	This register contains the starting and ending values of calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48	RW	Reserved.
49	RWX	WR_VREF_RANGE_DRAM0: This bit contains the default and current value of the DRAM WR VREF range for DRAM0 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
50:55	RWX	WR_VREF_VALUE_DRAM0: This field contains the default and current value of the DRAM WR VREF value for DRAM0 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
56	RW	Reserved.
57	RWX	WR_VREF_RANGE_DRAM1: This bit contains the default and current value of the DRAM WR VREF range for DRAM1 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
58:63	RWX	WR_VREF_VALUE_DRAM1: This field contains the default and current value of the DRAM WR VREF value for DRAM1 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.

Register Name	DP16 Write VREF Value 0 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_VALUE0_RANK_PAIR3_P1_[n]
Address	8000035E0701143F (SCOM), +0x0400_0000_0000
Description	This register contains the starting and ending values of calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49	RWX	WR_VREF_RANGE_DRAM0: This bit contains the default and current value of the DRAM WR VREF range for DRAM0 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
50:55	RWX	WR_VREF_VALUE_DRAM0: This field contains the default and current value of the DRAM WR VREF value for DRAM0 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
56	RW	Reserved.
57	RWX	WR_VREF_RANGE_DRAM1: This bit contains the default and current value of the DRAM WR VREF range for DRAM1 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
58:63	RWX	WR_VREF_VALUE_DRAM1: This field contains the default and current value of the DRAM WR VREF value for DRAM1 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.

Register Name	DP16 Write VREF Value 0 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_VALUE0_RANK_PAIR3_P2_[n]
Address	8000035E0701183F (SCOM), +0x0400_0000_0000
Description	This register contains the starting and ending values of calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49	RWX	WR_VREF_RANGE_DRAM0: This bit contains the default and current value of the DRAM WR VREF range for DRAM0 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
50:55	RWX	WR_VREF_VALUE_DRAM0: This field contains the default and current value of the DRAM WR VREF value for DRAM0 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
56	RW	Reserved.
57	RWX	WR_VREF_RANGE_DRAM1: This bit contains the default and current value of the DRAM WR VREF range for DRAM1 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	WR_VREF_VALUE_DRAM1: This field contains the default and current value of the DRAM WR VREF value for DRAM1 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.

Register Name	**DP16 Write VREF Value 0 RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_VALUE0_RANK_PAIR3_P3_[n]
Address	8000035E07011C3F (SCOM), +0x0400_0000_0000
Description	This register contains the starting and ending values of calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49	RWX	WR_VREF_RANGE_DRAM0: This bit contains the default and current value of the DRAM WR VREF range for DRAM0 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
50:55	RWX	WR_VREF_VALUE_DRAM0: This field contains the default and current value of the DRAM WR VREF value for DRAM0 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
56	RW	Reserved.
57	RWX	WR_VREF_RANGE_DRAM1: This bit contains the default and current value of the DRAM WR VREF range for DRAM1 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
58:63	RWX	WR_VREF_VALUE_DRAM1: This field contains the default and current value of the DRAM WR VREF value for DRAM1 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.

Register Name	**DP16 Write VREF Value 1 RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_VALUE1_RANK_PAIR3_P0_[n]
Address	8000035F0701103F (SCOM), +0x0400_0000_0000
Description	This register contains the starting and ending values of calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49	RWX	WR_VREF_RANGE_DRAM2: This bit contains the default and current value of the DRAM WR VREF range for DRAM2 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	WR_VREF_VALUE_DRAM2: This bit contains the default and current value of the DRAM WR VREF value for DRAM2 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
56	RW	Reserved.
57	RWX	WR_VREF_RANGE_DRAM3: This bit contains the default and current value of the DRAM WR VREF range for DRAM3 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
58:63	RWX	WR_VREF_VALUE_DRAM3: This bit contains the default and current value of the DRAM WR VREF value for DRAM3 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.

Register Name	DP16 Write VREF Value 1 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_VALUE1_RANK_PAIR3_P1_[n]
Address	8000035F0701143F (SCOM), +0x0400_0000_0000
Description	This register contains the starting and ending values of calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000
48	RW	Reserved.
49	RWX	WR_VREF_RANGE_DRAM2: This bit contains the default and current value of the DRAM WR VREF range for DRAM2 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
50:55	RWX	WR_VREF_VALUE_DRAM2: This bit contains the default and current value of the DRAM WR VREF value for DRAM2 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
56	RW	Reserved.
57	RWX	WR_VREF_RANGE_DRAM3: This bit contains the default and current value of the DRAM WR VREF range for DRAM3 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
58:63	RWX	WR_VREF_VALUE_DRAM3: This bit contains the default and current value of the DRAM WR VREF value for DRAM3 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.

Register Name	DP16 Write VREF Value 1 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_VALUE1_RANK_PAIR3_P2_[n]
Address	8000035F0701183F (SCOM), +0x0400_0000_0000
Description	This register contains the starting and ending values of calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49	RWX	WR_VREF_RANGE_DRAM2: This bit contains the default and current value of the DRAM WR VREF range for DRAM2 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
50:55	RWX	WR_VREF_VALUE_DRAM2: This bit contains the default and current value of the DRAM WR VREF value for DRAM2 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
56	RW	Reserved.
57	RWX	WR_VREF_RANGE_DRAM3: This bit contains the default and current value of the DRAM WR VREF range for DRAM3 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
58:63	RWX	WR_VREF_VALUE_DRAM3: This bit contains the default and current value of the DRAM WR VREF value for DRAM3 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.

Register Name	DP16 Write VREF Value 1 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_WR_VREF_VALUE1_RANK_PAIR3_P3_[n]
Address	8000035F07011C3F (SCOM), +0x0400_0000_0000
Description	This register contains the starting and ending values of calibration.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48	RW	Reserved.
49	RWX	WR_VREF_RANGE_DRAM2: This bit contains the default and current value of the DRAM WR VREF range for DRAM2 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
50:55	RWX	WR_VREF_VALUE_DRAM2: This bit contains the default and current value of the DRAM WR VREF value for DRAM2 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
56	RW	Reserved.
57	RWX	WR_VREF_RANGE_DRAM3: This bit contains the default and current value of the DRAM WR VREF range for DRAM3 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. This bit corresponds to bit A6 in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.
58:63	RWX	WR_VREF_VALUE_DRAM3: This bit contains the default and current value of the DRAM WR VREF value for DRAM3 (both x8 and x4 DRAM), as referenced by the PHY. The user configures the starting value to the value programmed by initial MRS commands. These bits correspond to bits A5 - A0 (bit 2 corresponds to bit A5) in MR6 in the DDR4 JEDEC specification. The algorithm overwrites the initial value with the final value.

Register Name	DP16 Read Eye Size 0 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE0_RANK_PAIR3_P0_[n]
Address	800003600701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 0 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE0_RANK_PAIR3_P1_[n]
Address	800003600701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	**DP16 Read Eye Size 0 RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE0_RANK_PAIR3_P2_[n]
Address	800003600701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	**DP16 Read Eye Size 0 RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE0_RANK_PAIR3_P3_[n]
Address	8000036007011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 1 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE1_RANK_PAIR3_P0_[n]
Address	800003610701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 1 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE1_RANK_PAIR3_P1_[n]
Address	800003610701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 1 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE1_RANK_PAIR3_P2_[n]
Address	800003610701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 1 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE1_RANK_PAIR3_P3_[n]
Address	8000036107011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 2 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE2_RANK_PAIR3_P0_[n]
Address	800003620701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 2 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE2_RANK_PAIR3_P1_[n]
Address	800003620701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 2 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE2_RANK_PAIR3_P2_[n]
Address	800003620701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 2 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE2_RANK_PAIR3_P3_[n]
Address	8000036207011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 3 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE3_RANK_PAIR3_P0_[n]
Address	800003630701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 3 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE3_RANK_PAIR3_P1_[n]
Address	800003630701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 3 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE3_RANK_PAIR3_P2_[n]
Address	800003630701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 3 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE3_RANK_PAIR3_P3_[n]
Address	8000036307011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 4 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE4_RANK_PAIR3_P0_[n]
Address	800003640701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 4 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE4_RANK_PAIR3_P1_[n]
Address	800003640701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 4 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE4_RANK_PAIR3_P2_[n]
Address	800003640701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 4 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE4_RANK_PAIR3_P3_[n]
Address	8000036407011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 5 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE5_RANK_PAIR3_P0_[n]
Address	800003650701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 5 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE5_RANK_PAIR3_P1_[n]
Address	800003650701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 5 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE5_RANK_PAIR3_P2_[n]
Address	800003650701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 5 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE5_RANK_PAIR3_P3_[n]
Address	8000036507011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 6 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE6_RANK_PAIR3_P0_[n]
Address	800003660701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 6 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE6_RANK_PAIR3_P1_[n]
Address	800003660701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 6 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE6_RANK_PAIR3_P2_[n]
Address	800003660701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 6 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE6_RANK_PAIR3_P3_[n]
Address	8000036607011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 7 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE7_RANK_PAIR3_P0_[n]
Address	800003670701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 7 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE7_RANK_PAIR3_P1_[n]
Address	800003670701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 7 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE7_RANK_PAIR3_P2_[n]
Address	800003670701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 7 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE7_RANK_PAIR3_P3_[n]
Address	8000036707011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 8 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE8_RANK_PAIR3_P0_[n]
Address	800003680701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 8 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE8_RANK_PAIR3_P1_[n]
Address	800003680701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 8 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE8_RANK_PAIR3_P2_[n]
Address	800003680701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 8 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE8_RANK_PAIR3_P3_[n]
Address	8000036807011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 9 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE9_RANK_PAIR3_P0_[n]
Address	800003690701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 9 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE9_RANK_PAIR3_P1_[n]
Address	800003690701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 9 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE9_RANK_PAIR3_P2_[n]
Address	800003690701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 9 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE9_RANK_PAIR3_P3_[n]
Address	8000036907011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 10 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE10_RANK_PAIR3_P0_[n]
Address	8000036A0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 10 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE10_RANK_PAIR3_P1_[n]
Address	8000036A0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	**DP16 Read Eye Size 10 RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE10_RANK_PAIR3_P2_[n]
Address	8000036A0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	**DP16 Read Eye Size 10 RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE10_RANK_PAIR3_P3_[n]
Address	8000036A07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 11 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE11_RANK_PAIR3_P0_[n]
Address	8000036B0701103F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 Read Eye Size 11 RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE11_RANK_PAIR3_P1_[n]
Address	8000036B0701143F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	**DP16 Read Eye Size 11 RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE11_RANK_PAIR3_P2_[n]
Address	8000036B0701183F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	**DP16 Read Eye Size 11 RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_READ_EYE_SIZE11_RANK_PAIR3_P3_[n]
Address	8000036B07011C3F (SCOM), +0x0400_0000_0000
Description	This register holds the read eye size for two of the MEMINTDnnB pins for one rank pair in the DP16. The read-centering calibration algorithm writes this register. The read-centering algorithm does not reset this register. The read-centering algorithm uses this register value as a starting point for the algorithm.

Bits	SCOM	Field Mnemonic: Description
0:49	RO	Constant = 0b00000000000000000000000000000000000000000000000000
50:55	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.
56:57	RO	Constant = 0b00
58:63	RWX	RD_EYE_SIZE: This field contains the read eye size for the MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps that captured valid data during the read-centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface or determined by the read-centering algorithm. This value, in addition to the corresponding RD_DELAY field in the DP16 Read Delay Value {0-11} Register, determines the left, right, and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the read delay value.

Register Name	DP16 DQ Bit Disable RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQ_BIT_DISABLE_RP3_P0_[n]
Address	8000037C0701103F (SCOM), +0x0400_0000_0000
Description	This register is used to disable each of the 16 pins on the DP16. During calibration operations, the hardware sets the bit in this register that corresponds to a pin on the DP16 that failed a calibration step. This register indicates which DQ pins on the DP16 failed a calibration step. This register does not indicate which calibration step failed.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DQ_BIT_DISABLE_0_15: 1 = Indicates that the DP16 bit is disabled and does not participate in any calibration steps. 0 = Indicates that the DP16 bit is not disabled. Bit 48 controls MEMINTD00B(n). Bit 49 controls MEMINTD01B(n). Bit 50 controls MEMINTD02B(n). ... Bit 63 controls MEMINTD15B(n). where n is the DP16 instance number.

Register Name	DP16 DQ Bit Disable RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQ_BIT_DISABLE_RP3_P1_[n]
Address	8000037C0701143F (SCOM), +0x0400_0000_0000
Description	This register is used to disable each of the 16 pins on the DP16. During calibration operations, the hardware sets the bit in this register that corresponds to a pin on the DP16 that failed a calibration step. This register indicates which DQ pins on the DP16 failed a calibration step. This register does not indicate which calibration step failed.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DQ_BIT_DISABLE_0_15: 1 = Indicates that the DP16 bit is disabled and does not participate in any calibration steps. 0 = Indicates that the DP16 bit is not disabled. Bit 48 controls MEMINTD00B(n). Bit 49 controls MEMINTD01B(n). Bit 50 controls MEMINTD02B(n). ... Bit 63 controls MEMINTD15B(n). where n is the DP16 instance number.

Register Name	DP16 DQ Bit Disable RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQ_BIT_DISABLE_RP3_P2_[n]
Address	8000037C0701183F (SCOM), +0x0400_0000_0000
Description	This register is used to disable each of the 16 pins on the DP16. During calibration operations, the hardware sets the bit in this register that corresponds to a pin on the DP16 that failed a calibration step. This register indicates which DQ pins on the DP16 failed a calibration step. This register does not indicate which calibration step failed.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	DQ_BIT_DISABLE_0_15: 1 = Indicates that the DP16 bit is disabled and does not participate in any calibration steps. 0 = Indicates that the DP16 bit is not disabled. Bit 48 controls MEMINTD00B(n). Bit 49 controls MEMINTD01B(n). Bit 50 controls MEMINTD02B(n). ... Bit 63 controls MEMINTD15B(n). where n is the DP16 instance number.

Register Name	**DP16 DQ Bit Disable RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQ_BIT_DISABLE_RP3_P3_[n]
Address	8000037C07011C3F (SCOM), +0x0400_0000_0000
Description	This register is used to disable each of the 16 pins on the DP16. During calibration operations, the hardware sets the bit in this register that corresponds to a pin on the DP16 that failed a calibration step. This register indicates which DQ pins on the DP16 failed a calibration step. This register does not indicate which calibration step failed.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:63	RW	DQ_BIT_DISABLE_0_15: 1 = Indicates that the DP16 bit is disabled and does not participate in any calibration steps. 0 = Indicates that the DP16 bit is not disabled. Bit 48 controls MEMINTD00B(n). Bit 49 controls MEMINTD01B(n). Bit 50 controls MEMINTD02B(n). ... Bit 63 controls MEMINTD15B(n). where n is the DP16 instance number.

Register Name	**DP16 DQS Bit Disable RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQS_BIT_DISABLE_RP3_P0_[n]
Address	8000037D0701103F (SCOM), +0x0400_0000_0000
Description	This register is used to disable each of the eight DQS pins on the DP16. During calibration operations, the hardware sets the bit in this register that corresponds to a pin on the DP16 that failed a calibration step. This register indicates which DQS pins on the DP16 failed a calibration step. This register does not indicate which calibration step failed.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DQS_BIT_DISABLE_16_23: Bits are grouped in pairs. Bits 48:49, 50:51, 52:53, and 54:55 correspond to the differential DQS bits for each pair. 1 = Indicates that the DQS bits are disabled and do not participate in any calibration steps. Both DQS bits in the pair are set to 1b. 0 = Indicates that the DQS bits are not disabled. Both DQS bits in the pair are set to 0b. Bits 48:49 indicate the disable state of the DQS associated with QUAD0, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 50:51 indicate the disable state of the DQS associated with QUAD1, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 52:53 indicate the disable state of the DQS associated with QUAD2, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 54:55 indicate the disable state of the DQS associated with QUAD3, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register.
56:63	RO	Constant = 0b00000000

Register Name	**DP16 DQS Bit Disable RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQS_BIT_DISABLE_RP3_P1_[n]
Address	8000037D0701143F (SCOM), +0x0400_0000_0000
Description	This register is used to disable each of the eight DQS pins on the DP16. During calibration operations, the hardware sets the bit in this register that corresponds to a pin on the DP16 that failed a calibration step. This register indicates which DQS pins on the DP16 failed a calibration step. This register does not indicate which calibration step failed.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:55	RW	DQS_BIT_DISABLE_16_23: Bits are grouped in pairs. Bits 48:49, 50:51, 52:53, and 54:55 correspond to the differential DQS bits for each pair. 1 = Indicates that the DQS bits are disabled and do not participate in any calibration steps. Both DQS bits in the pair are set to 1b. 0 = Indicates that the DQS bits are not disabled. Both DQS bits in the pair are set to 0b. Bits 48:49 indicate the disable state of the DQS associated with QUAD0, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 50:51 indicate the disable state of the DQS associated with QUAD1, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 52:53 indicate the disable state of the DQS associated with QUAD2, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 54:55 indicate the disable state of the DQS associated with QUAD3, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register.
56:63	RO	Constant = 0b00000000

Register Name	DP16 DQS Bit Disable RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQS_BIT_DISABLE_RP3_P2_[n]
Address	8000037D0701183F (SCOM), +0x0400_0000_0000
Description	This register is used to disable each of the eight DQS pins on the DP16. During calibration operations, the hardware sets the bit in this register that corresponds to a pin on the DP16 that failed a calibration step. This register indicates which DQS pins on the DP16 failed a calibration step. This register does not indicate which calibration step failed.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000
48:55	RW	DQS_BIT_DISABLE_16_23: Bits are grouped in pairs. Bits 48:49, 50:51, 52:53, and 54:55 correspond to the differential DQS bits for each pair. 1 = Indicates that the DQS bits are disabled and do not participate in any calibration steps. Both DQS bits in the pair are set to 1b. 0 = Indicates that the DQS bits are not disabled. Both DQS bits in the pair are set to 0b.Bits 48:49 indicate the disable state of the DQS associated with QUAD0, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 50:51 indicate the disable state of the DQS associated with QUAD1, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 52:53 indicate the disable state of the DQS associated with QUAD2, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 54:55 indicate the disable state of the DQS associated with QUAD3, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register.
56:63	RO	Constant = 0b00000000

Register Name	DP16 DQS Bit Disable RP3 Register [n] (n=0:4)
Mnemonic	IOM0.DDRPHY_DP16_DQS_BIT_DISABLE_RP3_P3_[n]
Address	8000037D07011C3F (SCOM), +0x0400_0000_0000
Description	This register is used to disable each of the eight DQS pins on the DP16. During calibration operations, the hardware sets the bit in this register that corresponds to a pin on the DP16 that failed a calibration step. This register indicates which DQS pins on the DP16 failed a calibration step. This register does not indicate which calibration step failed.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DQS_BIT_DISABLE_16_23: Bits are grouped in pairs. Bits 48:49, 50:51, 52:53, and 54:55 correspond to the differential DQS bits for each pair. 1 = Indicates that the DQS bits are disabled and do not participate in any calibration steps. Both DQS bits in the pair are set to 1b. Bits 48:49 indicate the disable state of the DQS associated with QUAD0, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 50:51 indicate the disable state of the DQS associated with QUAD1, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 52:53 indicate the disable state of the DQS associated with QUAD2, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register. Bits 54:55 indicate the disable state of the DQS associated with QUAD3, as defined by the configurations of the DP16 Read Clock Enable and Selection Register and the DP16 Write Clock Enable and Selection Register.
56:63	RO	Constant = 0b00000000

Register Name	**DP16 Write DQ Offset Value RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQ_WR_OFFSET_RP3_P0_[n]
Address	8000037E0701103F (SCOM), +0x0400_0000_0000
Description	This register contains an offset value for each quadrant. This offset allows the centered write data bits in each quadrant to be offset from the center as determined by the write-centering calibration algorithm. This register is used by the write-centering calibration state machine. This register must be configured, if needed, before the write-centering calibration algorithm is initiated. Changing the value of this register without running the write-centering calibration algorithm has no effect on the data bit write delay values.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	DQ_WR_OFFSET_N0: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). The least-significant bit of the 5-bit value is always 0b.
52:55	RW	DQ_WR_OFFSET_N1: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). The least-significant bit of the 5-bit value is always 0b.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	DQ_WR_OFFSET_N2: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). The least-significant bit of the 5-bit value is always 0b.
60:63	RW	DQ_WR_OFFSET_N3: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). The least-significant bit of the 5-bit value is always 0b.

Register Name	**DP16 Write DQ Offset Value RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQ_WR_OFFSET_RP3_P1_[n]
Address	8000037E0701143F (SCOM), +0x0400_0000_0000
Description	This register contains an offset value for each quadrant. This offset allows the centered write data bits in each quadrant to be offset from the center as determined by the write-centering calibration algorithm. This register is used by the write-centering calibration state machine. This register must be configured, if needed, before the write-centering calibration algorithm is initiated. Changing the value of this register without running the write-centering calibration algorithm has no effect on the data bit write delay values.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	DQ_WR_OFFSET_N0: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). The least-significant bit of the 5-bit value is always 0b.
52:55	RW	DQ_WR_OFFSET_N1: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). The least-significant bit of the 5-bit value is always 0b.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	DQ_WR_OFFSET_N2: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). The least-significant bit of the 5-bit value is always 0b.
60:63	RW	DQ_WR_OFFSET_N3: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). The least-significant bit of the 5-bit value is always 0b.

Register Name	**DP16 Write DQ Offset Value RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQ_WR_OFFSET_RP3_P2_[n]
Address	8000037E0701183F (SCOM), +0x0400_0000_0000
Description	This register contains an offset value for each quadrant. This offset allows the centered write data bits in each quadrant to be offset from the center as determined by the write-centering calibration algorithm. This register is used by the write-centering calibration state machine. This register must be configured, if needed, before the write-centering calibration algorithm is initiated. Changing the value of this register without running the write-centering calibration algorithm has no effect on the data bit write delay values.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	DQ_WR_OFFSET_N0: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). The least-significant bit of the 5-bit value is always 0b.
52:55	RW	DQ_WR_OFFSET_N1: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). The least-significant bit of the 5-bit value is always 0b.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	DQ_WR_OFFSET_N2: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). The least-significant bit of the 5-bit value is always 0b.
60:63	RW	DQ_WR_OFFSET_N3: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). The least-significant bit of the 5-bit value is always 0b.

Register Name	**DP16 Write DQ Offset Value RP3 Register [n] (n=0:4)**
Mnemonic	IOM0.DDRPHY_DP16_DQ_WR_OFFSET_RP3_P3_[n]
Address	8000037E07011C3F (SCOM), +0x0400_0000_0000
Description	This register contains an offset value for each quadrant. This offset allows the centered write data bits in each quadrant to be offset from the center as determined by the write-centering calibration algorithm. This register is used by the write-centering calibration state machine. This register must be configured, if needed, before the write-centering calibration algorithm is initiated. Changing the value of this register without running the write-centering calibration algorithm has no effect on the data bit write delay values.

Bits	SCOM	Field Mnemonic: Description
0:47	RO	Constant = 0b000000000000000000000000000000000000000000000000
48:51	RW	DQ_WR_OFFSET_N0: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD00B(n). MEMINTD01B(n). MEMINTD02B(n). MEMINTD03B(n). The least-significant bit of the 5-bit value is always 0b.
52:55	RW	DQ_WR_OFFSET_N1: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD04B(n). MEMINTD05B(n). MEMINTD06B(n). MEMINTD07B(n). The least-significant bit of the 5-bit value is always 0b.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	DQ_WR_OFFSET_N2: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD08B(n). MEMINTD09B(n). MEMINTD10B(n). MEMINTD11B(n). The least-significant bit of the 5-bit value is always 0b.
60:63	RW	DQ_WR_OFFSET_N3: This field contains the four most-significant bits of a 5-bit value. The 5-bit value is a twos complement number added to the center phase-rotator value determined by the write-centering calibration algorithm. This value is added to the center value by the write-centering calibration algorithm as the final step of write centering these pins: MEMINTD12B(n). MEMINTD13B(n). MEMINTD14B(n). MEMINTD15B(n). The least-significant bit of the 5-bit value is always 0b.