POWER9 Platform Supervisor with I2C Interface

1 Features

- Platform power rail and clock output startup / shutdown sequencing
- Platform Protection cuts power to platform if power rail fault detected
- Boot Status outputs provide early IPL feedback via NIC, IPMI Indicator, and Power LEDs
- Full control and platform status monitoring functionality over I^2C
- Manufacturing Mode allows power rail test and diagnostics
- BMC boot watchdog functionality
- HDL source available

2 Applications

- POWER9 system planar cards

3 Description

The POWER9 Platform Supervisor (P9PS) is a soft logic core that provides basic electrical safety and supervisory functions required to support POWER9 CPU and platform operation. The P9PS is responsible for power rail sequencing during platform startup and shutdown, as well as rail fault detection and clock enable / disable according to POWER9 electrical timing requirements. In addition, early startup indication and front panel control logic is provided to reduce external discrete logic component requirements.

The P9PS primarily communicates over a standard I^2C interface. As a low level device, it is anticipated that an external Baseboard Management Controller (BMC) will handle higher level functions, such as power and reset signal processing, according to current system state. This higher level BMC is then expected to command the P9PS to switch low level electrical state as appropriate. There is no minimum functional level for the platform BMC beyond being able to effectively interface with the P9PS over I^2C.

The P9PS provides an optional early boot indication mechanism using the front panel LED outputs. In normal system operation, or when the system is quiesced, the front panel outputs are driven directly via corresponding logic level inputs from the system planar. When the early boot indicator system is activated via I^2C, these front panel outputs are overridden to display the provided early boot codes in modified binary format. In an attempt to add an additional bit of information, the early boot code MSB controls the fade in / fade out period of the front panel LEDs.

Diagnostic information is available over the I^2C link. The current status of all power rails, in addition to the rail that caused the platform protection to last trip, is available via the appropriate I^2C registers at all times. A related manufacturing mode is also able to be used to force power on to all regulators for diagnostic purposes, however the use of this mode outside of manufacturing and low level electrical diagnostics is strongly discouraged.

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4 Revision History

Initial Revision (November 2019)

5 Pin Configuration and Functions

Pin Functions

PIN			I / O	DESCRIPTION
NAME	PLANAR			
	TALOS II	BLACKBIRD		
FPGA_CLOCK	81		I	Primary FPGA logic clock
LPC_CLOCK	13		I	Platform LPC clock
SYSEN	15		I	Platform chassis power on request (logic level, active high)
SYSGOOD	53		O	Platform chassis power on sequence complete (logic level, active high)
BMC_BOOT_PHASE_IN	100		I	BMC early boot phase logic level signal
VDDA_EN	72		O	CPU1 VDD regulator enable (logic level, active high)
VDDB_EN	79		O	CPU2 VDD regulator enable (logic level, active high)
VCSA_EN	71		O	CPU1 VCS regulator enable (logic level, active high)
VCSB_EN	78		O	CPU2 VCS regulator enable (logic level, active high)
VDNA_EN	68		O	CPU1 VDN regulator enable (logic level, active high)
VDNB_EN	51		O	CPU2 VDN regulator enable (logic level, active high)
VIOA_EN	66		O	CPU1 VIO regulator enable (logic level, active high)
VIOB_EN	69		O	CPU2 VIO regulator enable (logic level, active high)
VPPAB_EN	52		O	CPU1 DDR VPP A/B enable (logic level, active high)
VPPCD_EN	60		O	CPU2 DDR VPP C/D enable (logic level, active high)
VDDRAB_EN	65		O	CPU1 DDR A/B enable (logic level, active high)
VTTAB_EN	62		O	CPU1 DDR VTT A/B enable (logic level, active high)
VDDRCD_EN	64		O	CPU2 DDR C/D enable (logic level, active high)
VTTCD_EN	63		O	CPU2 DDR VTT C/D enable (logic level, active high)
AVDD_EN	59		O	Common CPU AVDD enable (logic level, active high)
MISCIO_EN	56		O	Common CPU miscellaneous I/O rail enable (logic level, active high)
ATX_EN	57		O	ATX power supply enable (logic level, active low)
VDDA_PG	28		I	CPU1 VDD regulator power good (logic level, active high)
VDDB_PG	26		I	CPU2 VDD regulator power good (logic level, active high)
VCSA_PG	29		I	CPU1 VCS regulator power good (logic level, active high)
VCSB_PG	27		I	CPU2 VCS regulator power good (logic level, active high)
VDNA_PG	34		I	CPU1 VDN regulator power good (logic level, active high)
VDNB_PG	30		I	CPU2 VDN regulator power good (logic level, active high)
VIOA_PG	36		I	CPU1 VIO regulator power good (logic level, active high)
VIOB_PG	33		I	CPU2 VIO regulator power good (logic level, active high)
VPPAB_PG	42		I	CPU1 DDR VPP A/B power good (logic level, active high)
VPPCD_PG	41		I	CPU2 DDR VPP C/D power good (logic level, active high)
VDDRAB_PG	37		I	CPU1 DDR A/B and VTT power good (logic level, active high)

Pin Functions (cont.)

PIN			I / O	DESCRIPTION
NAME	PLANAR			
	TALOS II	BLACKBIRD		
VDDRCD_PG	40		I	CPU2 DDR C/D and VTT power good (logic level, active high)
AVDD_PG	19		I	Common CPU AVDD power good (logic level, active high)
MISCIO_PG	24		I	Common CPU miscellaneous I/O rail power good (logic level, active high)
ATX_PG	20		I	ATX power supply power good (logic level, active high)
BMC_VR_PG	18		I	BMC voltage regulator power good (logic level, active high)
I2C_SCL	86		I	I^2C clock
I2C_SDA	85		I/O	I^2C data
CPUB_PRESENT_L	4		I	CPU2 presence detect (logic level, active low)
CPUB_CLK_OEA	10		O	CPU2 clock phase A enable (logic level, active high)
CPUB_CLK_OEB	9		O	CPU2 clock phase B enable (logic level, active high)
LPC_RST	82		O	Master LPC clock reset (logic level, active low)
BMC_BOOT_COMPLETE_N	8		I	BMC startup complete (logic level, active low)
BMC_RST	83		O	BMC reset signal from watchdog (logic level, active low)
FAN_RST	1		O	Fan controller reset signal (logic level, active low)
USBHUB_RST	87		O	USB hub reset signal (logic level, active low)
CPU_STBY_RST	54		O	CPU standby reset signal (logic level, active high)
DUAL_5V_CTRL	80		-	RESERVED
WINDOW_OPEN_N	99		-	RESERVED
BMC_SYS_RESET_REQ_N	12		O	Platform reset request from front panel (logic level, active low)
PMC_DISABLE_N	21		O	SAS controller disable (logic level, active low)
AST_VGA_DISABLE_N	16		I	ASpeed VGA function block disable request (logic level, active low)
MODE_SET_N	25		I	RESERVED
NIC1_ACT_LED_N	93		I	BCM5719 port 1 ACT_LED signal
NIC2_ACT_LED_N	96		I	BCM5719 port 2 ACT_LED signal
NIC1_LINK_LED_N	94		I	BCM5719 port 1 LINK_LED signal
NIC2_LINK_LED_N	97		I	BCM5719 port 2 LINK_LED signal
NIC1_GREEN_LED_N	2		I	BCM5719 port 1 GREEN_LED signal
NIC2_GREEN_LED_N	3		I	BCM5719 port 2 GREEN_LED signal
BMC_UID_LED_REQ	90		I	Platform IPMI ID LED activity request (logic level, active low)
PANEL_NIC1_LED_CATHODE	91		O	Front panel NIC1 LED active (logic level, active low)
PANEL_NIC2_LED_CATHODE	95		O	Front panel NIC1 LED active (logic level, active low)
PANEL_UID_LED	89		O	Front panel IPMI ID LED active (logic level, active low)
PANEL_RESET_IN_L	73		I	Front panel reset switch (logic level, active low)
FLEXVER_RESET_IN_L	74		I	Auxiliary reset request signal (from optional FlexVer module)

6 Feature Description

6.1 Serial Interface

The P9PS operates exclusively as a slave device on the SMBus / I2C compatible bus. Bus connections are via two open drain lines, I2C_SDA and I2C_SCL. I2C_SDA is the bidirectional data line, and I2C_SCL is the input for the clock signal provided by the external master device. I2C communication is half duplex, meaning only the master or the slave can transmit at any given time. All data bytes are transmitted MSB first.

6.1.1 Bus Overview

Whichever device initiates a transfer is the *master* device, and the devices responding to transfers are the *slave* devices. The master device is responsible for bus control, and must generate the serial clock (I2C_SCL) in addition to the START and STOP conditions.

To initiate a transfer to a specified device address, a START condition is signalled on the bus by pulling I2C_SDA logic low while I2C_CLK is allowed to remain logic high. I2C_CLK is then pulled low in preparation for data transfer. Each bit of the 6-bit target device address is then placed on the bus in sequence, followed by the R/W bit. Each rising edge of I2C_CLK loads the data placed on I2C_SDA into all slave devices on the bus. After the 6th address bits and single R/W bit have been clocked onto the bus, the slave corresponding to the requested address will send an ACK by pulling I2C_SDA logic low for sampling by the master at the next clock rising edge. If I2C_SDA remains logic high when sampled by the master, no device has responded to the specified slave address and no further communication is possible in this cycle.

If a slave has acknowledged the destination address, data is then clocked onto the bus from the master or slave, depending on the value of the R/W bit. After each byte, a single ACK bit is required to be sent. During data transfer, it is critical that I2C_SDA remains stable during the period in which I2C_SCL is logic high, as I2C control signals are sent by changing I2C_SDA state while I2C_SCL is high.

Once all data has been transferred, the master halts the active bus transaction by sending a STOP control signal. STOP is sent by releasing I2C_SDA logic high while I2C_CLK is logic high.

6.1.2 Reading and Writing to the P9SP

Accessing a specific register for read or write is accomplished by sending the address of the desired register inside the device, then reading or writing the register data. When writing, set R/W to logic 0 (write), then transmit the value of the 8-bit register you want to write to. After the P9PS responds with an ACK bit, send the 8-bit data value with which you want to program the register, followed by a STOP bus control signal.

To read, a repeated start is used. When addressing the device for read, set R/W to logic 0 (write),

then transmit the value of the 8-bit register you want to read from. After the P9PS responds with an ACK bit, send another START bus control signal without transmitting a STOP bus control signal first. This leaves the bus transaction open, but allows the R/W bit to be changed. Next, transmit the identical device address, but set the R/W bit to logic 1 (read). After the device response with an ACK bit, the data inside the device starting at the specified register can be clocked out of the device in single byte chunks with a single ACK bit appended to each byte. When finished reading, send a STOP bus control signal to terminate the bus transaction.

6.1.3 Slave Address

As it is expected that there will only ever be a single P9PS installed on any given system planar, there is no provision to change the slave address. The slave address is standardized as 0x31 hexadecimal.

6.1.4 Power On Reset

The P9PS has internal reset systems that ensure all registers are cleared to a known consistent state on initial power on. This initial state corresponds to a planar with no regulators under the control of the P9PS powered on, which also indicates that unwanted post-initialization reset of the P9PS will immediately drop all active power rails under the control of the P9PS. As such, care should be taken to ensure that the P9PS will not be reset while the system planar is powered on or otherwise activated, as damage may occur to the processor due to incorrect power sequencing during uncontrolled rail shutdown.

7 Device Operation

7.1 Device Functional Modes

7.1.1 BMC Boot Mode

After initial power on or FPGA reset, and while the planar BMC has not yet signaled ready status, the P9PS remains in BMC Boot mode. This mode is a superset of Shutdown mode, described below, with the following additions:

In this mode, the planar is locked out from leaving the Shutdown mode. The only valid transition from BMC Boot mode is directly to Shutdown mode. This transition is accomplished with the following logic levels applied in sequence:

1. BMC_RST logic level deassert (logic high, output from P9PS after BMC regulator power good asserted). BMC_BOOT_PHASE_IN and BMC_BOOT_COMPLETE_N are allowed to float logic level high prior to and during BMC_RST deassertion.
2. BMC_BOOT_PHASE_IN is pulled logic level low to signal transition from initial bootloader phase to active BMC startup phase. If BMC_BOOT_COMPLETE_N is asserted (logic low) prior to BMC_BOOT_PHASE_IN, this step will be skipped.
3.) BMC_BOOT_COMPLETE_N is asserted (logic low). The P9PS immediately enters

Shutdown mode and releases the BMC startup planar lockouts.

Additionally, a BMC watchdog mode is provided. If the P9PS does not detect a transition out of initial bootloader phase within approximately 40 seconds after BMC_RST deassertion, the P9PS will assume the BMC boot process has failed, then strobe BMC_RST in an attempt to bring the BMC device online. When the watchdog fires, the watchdog timers are reset and rearmed; the P9PS will continue to attempt BMC reset at the determined interval for as long as power is applied to the system planar and the BMC has not asserted entry into the active BMC startup phase.

Even if the BMC functionality is implemented with a rapid-start device, such as an FPGA without a processor that requires a boot process, it is strongly recommended to retain the BMC Boot mode functionality to avoid unwanted planar operation during initial standby power application. It is acceptable in this situation to bypass the BMC bootloader phase by directly asserting BMC_BOOT_COMPLETE_N after BMC device startup, and tying BMC_BOOT_PHASE_IN either logic high or logic low. If BMC_BOOT_PHASE_IN is tied logic high, the BMC watchdog functionality described above will continue to operate, tying BMC_BOOT_PHASE_IN logic low will disable the BMC watchdog functionality entirely.

7.1.2 Shutdown Mode

In shutdown mode all regulators under the control of the P9PS are deactivated, and all processor and clock system resets are asserted. This is the state entered immediately after power on reset or after device reset from external source (e.g. the P9PS external reset pin). All I^2C registers are available for read and write, however some registers may have no effect until planar state reaches operational level. In this mode, all failure lockouts are reset, but any previously set failure codes remain latched in for external diagnostic purposes.

7.1.3 Power On Sequencing Mode

In this mode, reached by a logic level assertion on the SYSEN pin or via the appropriate register override bit, the system runs through operational status checks and attempts to power on all of the required power rails prior to releasing clock and processor resets. If any checks fail during this process, any previously activated rails will be deactivated and a failure bit will be set in the appropriate diagnostic I^2C register bank. The sole exception to this rule is if a pre-start check fails; if this occurs, no failure code will be set. The only signals that can cause a pre-start check failure are the BMC startup mode lines; the BMC must be indicated as operational before the lockout on the logic level planar start line will be released.

If a failure occurs, and a failure code is latched in, the platform start signal must be deactivated to clear the platform start lockout prior to a restart attempt. If the platform start signal remains asserted from any source, the lockout will not release and the planar will remain powered down with the P9PS indicating failure status. Clearing the failure lockout will not reset the failure code itself; only a new failure code or reset of the P9PS will clear the last set failure code. However, clearing the lockout will clear the failure set indication, therefore the BMC will still be able to

determine if the failure code is related to a presently occurring failure or if it is latched from a prior failure.

7.1.4 Planar Active Mode

This is the normal operating mode during host system operation. In this mode, the system planar is active and all resets are released. All regulators are monitored for dropout; if regulator dropout occurs from any source including ATX_PG, the failure mode logic described in detail above will immediately deactivate all regulators and lock out the platform enable signal. This mode may be exited normally by deasserting the platform enable signal, in which case the power rail shutdown procedure described below will be executed to bring the platform safely offline.

7.1.5 Power Off Sequencing Mode

This mode is reached if both SYS_EN and the I^2C-based platform enable signals are both deasserted and the system was previously in the Planar Active mode. Resets will be enabled and power rails will be taken offline in sequence to bring the planar and processor safely into the fully quiesced Shutdown mode. Note that this mode should not be triggered under normal conditions until the system is in a known safe state, e.g. after a normal host OS shutdown. If the host processor crashes or otherwise terminates abnormally, entering this mode is the safest means to fully reset all system state via reset and power down.

7.2 Control and Status Registers

7.2.1 Register Map

REGISTER NAME	OFFSET	DESCRIPTION
VERSION	0x00	Read only version register (single byte)
ERR_CLEAR	0x03	Read only register to optionally clear faults without dropping SYSEN
RESERVED	0x05	Reserved
RESERVED	0x06	Reserved
STATUS	0x07	Read only register containing planar status bitfield
PWR_EN_STAT_1	0x08	Read only register with Bank 1 Power Enable bitfield
PWR_EN_STAT_2	0x09	Read only register with Bank 2 Power Enable bitfield
PG_BANK_1	0x0a	Read only register with Bank 1 Power Good bitfield
PG_BANK_2	0x0b	Read only register with Bank 2 Power Good bitfield
VENDOR_ID	0x0c - 0x0f	Four byte read only ASCII string containing P9PS vendor ID (e.g. 'RCS ' for Talos II / Blackbird planars)
PANEL_LED_OVERRIDE	0x10	Single byte read / write register containing current boot status code for display on front panel LEDs
PWR_FAULT_STAT_1	0x18	Read only register with Bank 1 Power Fault bitfield
PWR_FAULT_STAT_2	0x19	Read only register with Bank 2 Power Fault bitfield
MFR_OVERRIDE	0x33	Read / write manufacturing override / battle short bitfield. **DO NOT USE IN NORMAL OPERATION**

7.2.2 Register Descriptions

7.2.2.1 Version Register (0x00)

This register is a single byte containing the current revision of the P9PS soft logic. It will vary between planars due to OEM/ODM customization, but in all cases a higher revision number means the soft core is of a later date revision than a lower revision number. This register is read-only.

7.2.2.2 Force Error Clear Register (0x03)

If a power rail enters a faulted condition, and it is not possible or feasible to drop the system enable signal (SYSEN and any asserted system enable bits in the control registers), executing a single read to this register will clear the fault lockout. If the system enable signal is asserted when this register is read, the P9PS will immediately attempt planar startup by re-entering the Power On Sequencing mode. This register is read-only.

7.2.2.3 Status Register (0x07)

This register is a read-only bitfield containing the high level operational status of the system planar, and the settings of any on-card mode set jumpers.

BIT NUMBER	DESCRIPTION
7	Mode Set 2 – 1 if MODE_SET_N asserted, 0 if deasserted

6	ASpeed VGA code disable request – 1 if AST_VGA_DISABLE_N asserted, 0 if deasserted
5	Second CPU installed – 1 if installed, 0 if not present
4	Power sequencing timeout fault detected – 1 if fault status asserted, 0 if no fault asserted
3	Power sequencing offline fault detected – 1 if fault status asserted, 0 if no fault asserted
2	General power sequencing fault detected – 1 if fault status asserted, 0 if no fault asserted
1	System enable request – 1 if system power on request asserted, 0 if system shutdown requested
0	System online status – 1 if in Planar Active mode, 0 if in any other mode

7.2.2.4 Power Enable Status Bank 1 Register (0x08) / Bank 2 Register (0x09)

These two registers comprise a two-byte (16 bit) read-only bitfield containing the current status of all regulator power enable signals attached to the P9PS. All bits use standard Enable (1), Disable (0) levels. Byte ordering is little endian, [0x09, 0x08]. Power rail sequencing proceeds from LSB to MSB during Power On Sequencing mode.

Along with the Power Good Status and Power Fault Status registers, the exact bit mapping of this register is planar specific, and will vary between planar revisions, models, and manufacturers.

BIT NUMBER	TALOS II	BLACKBIRD
15	UNUSED (RESERVED)	UNUSED (RESERVED)
14	CPU2 VTT / DIMM banks C/D	
13	CPU1 VTT / DIMM banks A/B	
12	CPU2 VPP for DIMM banks C/D	
11	CPU1 VPP for DIMM banks A/B	
10	CPU2 VCS	
9	CPU1 VCS	
8	CPU2 VDD	
7	CPU1 VDD	
6	CPU2 VIO	
5	CPU1 VIO	
4	Shared CPU analog VDD	
3	CPU2 VDN	
2	CPU1 VDN	
1	Shared CPU miscellaneous I/O power rail	
0	ATX power supply	ATX power supply

7.2.2.5 Power Good Status Bank 1 Register (0x0a) / Bank 2 Register (0x0b)

These two registers comprise a two-byte (16 bit) read-only bitfield containing the current status of all regulator power good signals attached to the P9PS. All bits use standard Good (1), Faulted (0) levels. Byte ordering is little endian, [0x0b, 0x0a].

Along with the Power Enable Status and Power Fault Status registers, the exact bit mapping of this register is planar specific, and will vary between planar revisions, models, and manufacturers.

BIT NUMBER	TALOS II	BLACKBIRD
15	UNUSED (RESERVED)	UNUSED (RESERVED)
14	CPU2 VTT / DIMM banks C/D	
13	CPU1 VTT / DIMM banks A/B	
12	CPU2 VPP for DIMM banks C/D	
11	CPU1 VPP for DIMM banks A/B	
10	CPU2 VCS	
9	CPU1 VCS	
8	CPU2 VDD	
7	CPU1 VDD	
6	CPU2 VIO	
5	CPU1 VIO	
4	Shared CPU analog VDD	
3	CPU2 VDN	
2	CPU1 VDN	
1	Shared CPU miscellaneous I/O power rail	
0	ATX power supply	ATX power supply

7.2.2.6 Vendor ID Registers (0x0c – 0x0f Inclusive)

Four bytes are reserved for a combined P9PS / planar vendor ID string. This vendor ID should reflect the planar the P9PS is installed on, and is recommended to be standard ASCII for ease of higher level system parsing. These four bytes are read-only, and are stored in little endian format.

For all Raptor Engineering / Raptor Computing Systems products, this ID is set to “RCS “. Care should be taken if the ID is modified, as higher level sofware may check the ID for compatibility before enabling or disabling certain features or protective code paths.

7.2.2.7 Panel LED Override Status Code (0x10)

The P9PS offers a front panel status indicator using the three standard front panel LEDs, with an optional fourth LED output usable on certain system planar designs. This front panel status indicator is partially controlled by the single byte, read-write Override register, and operates in three distinct modes:

Mode 1
Normal operation. This mode is active when the Override register is set to 0x00 and the BMC is online. Power, NIC1, NIC2, and (optionally) HDD logic level signaling is passed directly from the system planar to the front panel connectors, with any required logic level inversion for the LED drivers applied.

Mode 2
BMC boot phase. This mode is used to indicate the status of the BMC boot process to the system operator. The P9PS supports a bootloader phase, with fading, sequentially pulsing front panel LEDs, and a kernel phase, with all front panel LEDs gently pulsing in unison. This design presents a striking user-visible indication the system is not yet ready to operate while the BMC is still running startup processes.

The P9PS automatically reverts to Mode 1 operation once the BMC boot process has completed. Please see Section 7.1.1 “BMC Boot Mode” for more details on the BMC boot monitoring functionality.

Mode 3
Status indicator override. This mode is used by the low level boot firmware to indicate boot status to the system operator. When the Override register is set to any value other than 0x00, and the BMC is online, this mode will be entered.

This mode attempts to provide as much status information as possible via the three or four front panel LEDs present on most systems. It does this by assigning the lower three or four bits of the Override register directly to the front panel LEDs, and using the fourth or fifth bit (MSB) to select the fading pattern mode. All other bits are ignored.

If the MSB is 0, a slow fade pattern on all asserted bits with timing dim-dim-dim-bright is presented to the operator. If the MSB is 1, a fast fade pattern on all asserted bits with timing dim-bright-dim-bright is presented to the operator. In practice, this allows the operator to determine at a glance what state the system planar is in during system IPL, before the graphics adapter(s) are initialized. Once the system IPL is complete, the firmware must set the Override register back to 0x00 to allow normal operation of the front panel status LEDs.

7.2.2.8 Power Fault Status Bank 1 Register (0x18) / Bank 2 Register (0x19)

These two registers comprise a two-byte (16 bit) read-only bitfield containing the current status of all regulator power faults detected by the P9PS. All bits use standard Faulted (1), No Error (0) levels. Byte ordering is little endian, [0x19, 0x18].

Along with the Power Enable Status and Power Good Status registers, the exact bit mapping of this register is planar specific, and will vary between planar revisions, models, and manufacturers.

BIT NUMBER	TALOS II	BLACKBIRD
15	UNUSED (RESERVED)	UNUSED (RESERVED)
14	CPU2 VTT / DIMM banks C/D	
13	CPU1 VTT / DIMM banks A/B	
12	CPU2 VPP for DIMM banks C/D	

11	CPU1 VPP for DIMM banks A/B	
10	CPU2 VCS	
9	CPU1 VCS	
8	CPU2 VDD	
7	CPU1 VDD	
6	CPU2 VIO	
5	CPU1 VIO	
4	Shared CPU analog VDD	
3	CPU2 VDN	
2	CPU1 VDN	
1	Shared CPU miscellaneous I/O power rail	
0	ATX power supply	ATX power supply

7.2.2.9 Manufacturer Override (0x33)

This single byte, read-write register allows access to manufacturing-specific and battle short operating modes. It should not be used outside of those conditions, as irreversible hardware damage may result. The default state for this register is 0x00, writing 1 to any of the bits below will cause that mode to be enabled.

BIT NUMBER	DESCRIPTION
7	RESERVED for future Battle Short mode
6	RESERVED
5	RESERVED
4	RESERVED
3	RESERVED
2	Force CPU2 presence detect. Stops CPU2 regulator PG forced high when CPU2 regulators forced on w/ no CPU via Bit 1.
1	Force CPU2 regulator power on. Allows CPU2 regulator smoke test without any CPUs installed.
0	Signal Power On Sequencing Mode request. This is logically ORed with the SYSEN signal from the system planar.